

DATA SHEET

TDA3681A

Multiple voltage regulator with
switch and ignition buffer

Product specification

2003 Aug 29

Multiple voltage regulator with switch and ignition buffer

TDA3681A

FEATURES

General

- Extremely low noise behaviour and good stability with very small output capacitors
- Second supply pin for regulators 3 and 4 to reduce power dissipation (e.g. via a DC-to-DC converter)
- Three V_P -state controlled regulators (regulators 1, 3 and 4) and a power switch
- Regulator 2, reset and ignition buffer operational during load dump and thermal shutdown
- Combined control pin for switching regulators 1 and 3
- Separate control pins for switching regulator 4 and the power switch
- Supply voltage range from -18 V to $+50\text{ V}$
- Low quiescent current in standby mode (when regulators 1, 3 and 4 and power switch are switched off and ignition input is low)
- Hold output for low V_P , load dump and temperature protection
- Reset (push-pull output stage) for regulator 2 and hold output (open-collector output)
- Adjustable reset delay time
- High supply voltage ripple rejection
- Backup capacitor for regulator 2
- One independent ignition buffer (active HIGH).

Protections

- Reverse polarity safe (down to -18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short-circuited)
- ESD protection on all pins
- Thermal protections
- Load dump protection

- Foldback current limit protection for regulators 1, 2, 3 and 4
- Delayed second current limit protection for the power switch (at short circuit)
- The regulator outputs and the power switch are DC short-circuit safe to ground and supply (V_P).

GENERAL DESCRIPTION

The TDA3681A is a multiple output voltage regulator with a power switch and an ignition buffer. It is intended for use in car radios with or without a microcontroller.

The TDA3681A contains the following:

- Four fixed voltage regulators with a foldback current protection (regulators 1, 2, 3 and 4). Regulator 2, which is intended to supply a microcontroller, also operates during load dump and thermal shutdown
- Regulators 3 and 4 have a second supply pin that can be connected to a lower supply voltage ($> 6.5\text{ V}$) to reduce the power dissipation
- A power switch with protection, operated by a control input
- Reset and hold outputs that can be used to interface with the microcontroller; the reset signal can be used to call up the microcontroller
- Both supply pins can withstand load dump pulses and negative supply voltages
- Regulator 2, which is in regulation at a backup voltage above 6.5 V
- A provision for the use of a reserve supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage
- An ignition input Schmitt trigger with push-pull output stage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3681ATH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-3

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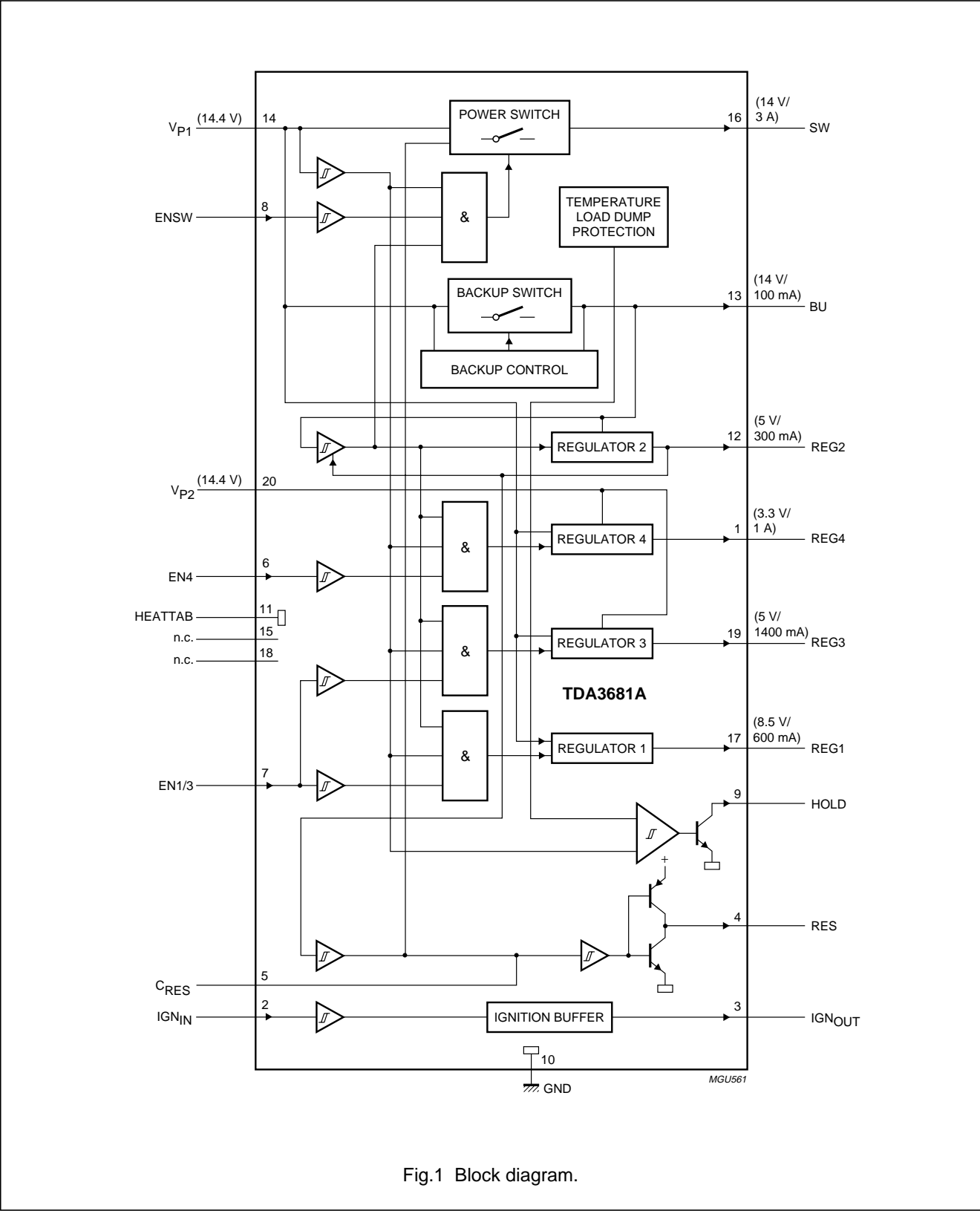
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{P1}	supply voltage 1		9.5	14.4	18	V
	operating					
	reverse polarity	non-operating	–	–	18	V
	regulator 2 on		4	14.4	50	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
V_{P2}	supply voltage 2		6.5	14.4	18	V
	operating					
	reverse polarity	non-operating	–	–	18	V
	regulator 2 on		0	–	50	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	standby mode	–	110	150	μ A
T_j	junction temperature		–	–	150	$^{\circ}$ C
Voltage regulators						
$V_{o(REG1)}$	output voltage of regulator 1	$1 \text{ mA} \leq I_{REG1} \leq 600 \text{ mA}$; $V_P = 14.4 \text{ V}$	8.0	8.5	9.0	V
$V_{o(REG2)}$	output voltage of regulator 2	$1 \text{ mA} \leq I_{REG2} \leq 300 \text{ mA}$; $V_P = 14.4 \text{ V}$	4.75	5.0	5.25	V
$V_{o(REG3)}$	output voltage of regulator 3	$1 \text{ mA} \leq I_{REG3} \leq 1400 \text{ mA}$; $V_P = 14.4 \text{ V}$	4.75	5.0	5.25	V
$V_{o(REG4)}$	output voltage of regulator 4	$1 \text{ mA} \leq I_{REG4} \leq 1 \text{ A}$; $V_P = 14.4 \text{ V}$	3.14	3.3	3.46	V
Power switch						
$V_{drop(SW)}$	drop-out voltage	$I_{SW} = 1 \text{ A}$; $V_{P1} = 13.5 \text{ V}$	–	0.45	0.65	V
		$I_{SW} = 1.8 \text{ A}$; $V_{P1} = 13.5 \text{ V}$	–	1.0	1.8	V
$I_{M(SW)}$	peak current		3	–	–	A

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BLOCK DIAGRAM



Multiple voltage regulator with switch and ignition buffer

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PINNING

SYMBOL	PIN	DESCRIPTION
REG4	1	regulator 4 output
IGN _{IN}	2	ignition input
IGN _{OUT}	3	ignition output (active HIGH)
RES	4	reset output (active LOW)
C _{RES}	5	reset delay capacitor
EN4	6	enable input for regulator 4
EN1/3	7	enable input for regulators 1 and 3
ENSW	8	enable input for power switch
HOLD	9	hold output (active LOW)
GND	10	ground
HEATTAB	11	heat tab connection; note 1
REG2	12	regulator 2 output
BU	13	backup switch output
V _{P1}	14	first supply voltage
n.c.	15	not connected
SW	16	power switch output
REG1	17	regulator 1 output
n.c.	18	not connected
REG3	19	regulator 3 output
V _{P2}	20	second supply voltage

Note

1. The pin is used for final test purposes. In the application it should be connected directly to ground.

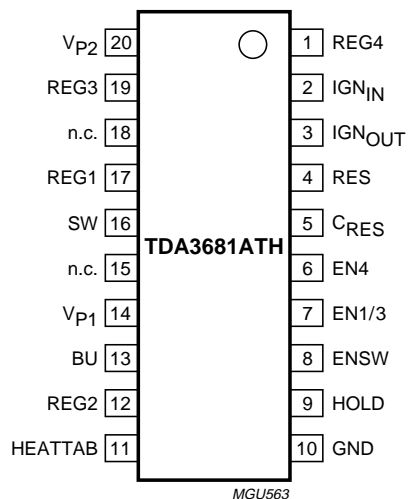


Fig.2 Pin configuration.

Multiple voltage regulator with switch and ignition buffer

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FUNCTIONAL DESCRIPTION

The TDA3681A is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of the low voltage operation of the car radio, low voltage drop regulators are used.

Regulator 2 is in regulation when the backup voltage exceeds 6.5 V for the first time. When regulator 2 is switched on and its output voltage is within its voltage range, the reset output is disabled to release the microcontroller. The reset delay time before release can be extended by an external capacitor (C_{CRES}). This start-up feature is included to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

The charge on the backup capacitor can be used to supply regulator 2 for a short period when the external supply voltage drops to 0 V (the time depends on the value of the backup capacitor).

The output stages of all switchable regulators have an extremely low noise behaviour and good stability, even for small values of the output capacitors.

When both regulator 2 and the supply voltages (V_{P1} and $V_{P2} > 4.5$ V) are available, regulators 1 and 3 can be operated by means of one enable input.

Regulator 4 and the power switch have a separate enable input.

Pin HOLD is normally HIGH but is active LOW. Pin HOLD is connected to an open-collector NPN transistor and must have an external pull-up resistor to operate. The hold output is controlled by a low battery voltage (V_{P1}) detection circuit which, when activated, pulls the hold output LOW (enabled).

The hold circuit is also controlled by the temperature and load dump protection. Activating the temperature or load dump protection causes a hold (LOW) during the time that the protection is activated.

The hold circuit is enabled at low battery voltages. This indicates that it is not possible to get regulator 1 into regulation when switching it on: regulator 1 has the highest output voltage (8.5 V) of all switchable regulators. Therefore, regulator 1 is the most critical regulator with respect to an out of regulation condition caused by a low battery voltage.

The hold function includes hysteresis to avoid oscillations when the battery voltage crosses the hold threshold levels for low V_P and load dump. The block diagram of the hold function is illustrated in Fig.3.

All output pins are fully protected. The regulators are protected against load dump (regulators 1, 3 and 4 switch off at supply voltages > 18 V) and short-circuit (foldback current protection).

The power switch contains a current protection. However, this protection is delayed at short-circuit by the reset delay capacitor (it should be noted that this is the second function of the reset delay capacitor C_{CRES}). During this time, the output current is limited to a peak value of at least 3 A (after a delay, the power switch can deliver 1.8 A continuous if $V_P \leq 18$ V).

In a normal situation, the voltage on the reset delay capacitor is approximately 3.5 V (depending on the temperature). The power switch output is approximately $V_P - 0.4$ V. At operating temperature, the power switch can deliver at least 3 A. At high temperature, the switch can deliver approximately 2 A.

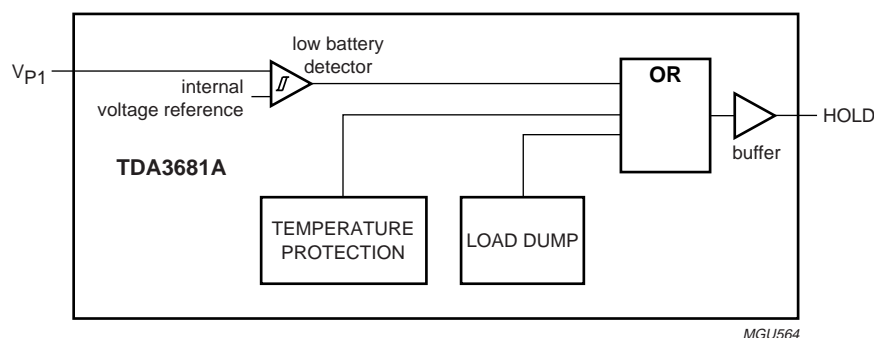


Fig.3 Block diagram of the hold circuit.

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During an overload condition or a short circuit ($V_{SW} < V_P - 3.7\text{ V}$), the voltage on the reset delay capacitor rises 0.6 V above the voltage of regulator 2. This rise time depends on the capacitor connected to pin C_{CRES} . During this time, the power switch can deliver more than 3 A. When regulator 2 is out of regulation and generates a reset, the power switch can only deliver 2 A and will immediately go into foldback protection.

At supply voltages $> 17\text{ V}$, the power switch is clamped at 16 V maximum (to avoid externally connected circuits being damaged by an overvoltage) and the power switch will switch off at load dump.

Interfacing with the microcontroller (simple full or semi on/off logic applications) can be realized with an independent ignition Schmitt trigger and ignition output buffer (push-pull output).

The timing diagrams are illustrated in Figs 4 and 5.

The second supply voltage V_{P2} is used for the switchable regulators 3 and 4. This input can be connected to a lower supply voltage of $\geq 6\text{ V}$ to reduce the power dissipation of the TDA3681A. A DC-to-DC converter could be used for this purpose.

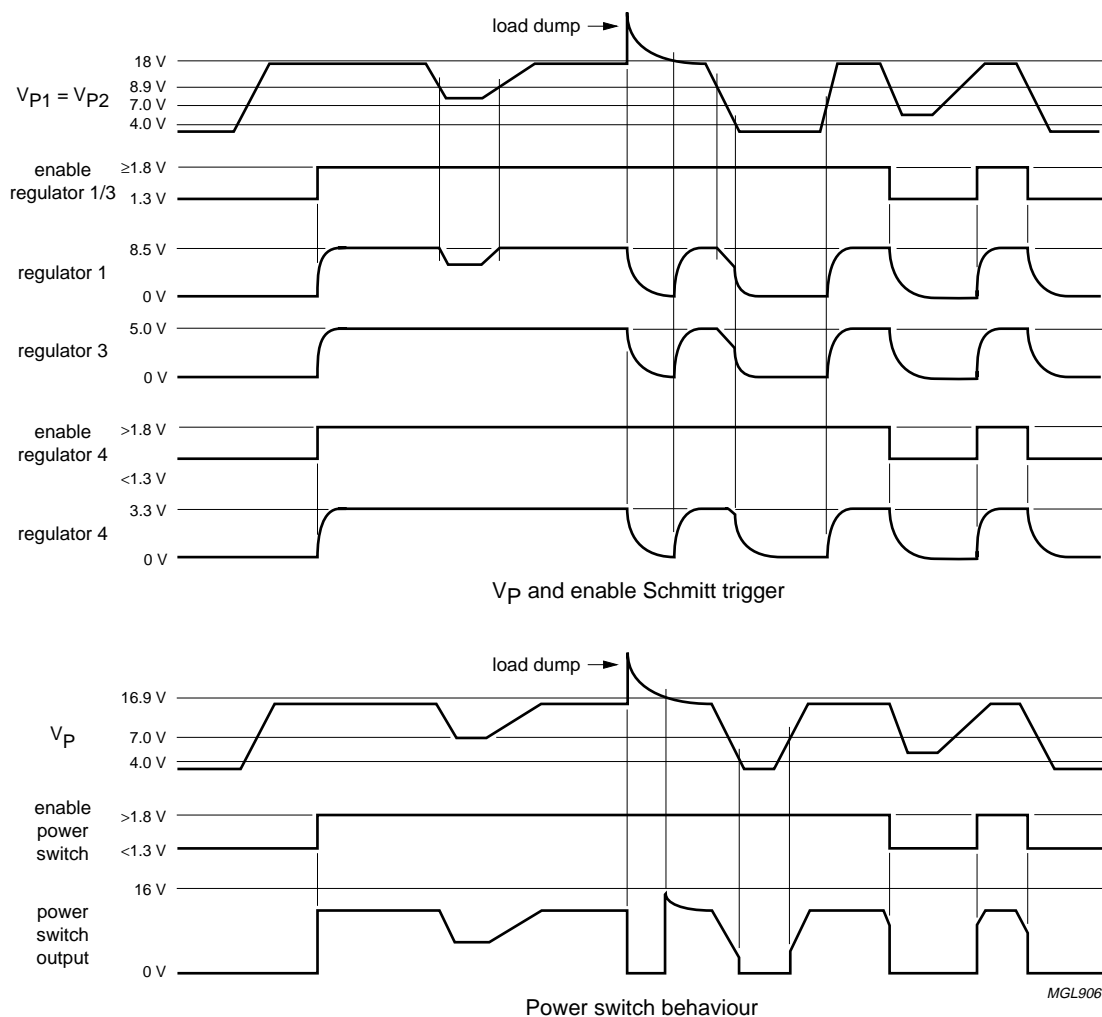


Fig.4 Timing diagram of regulators and power switch.

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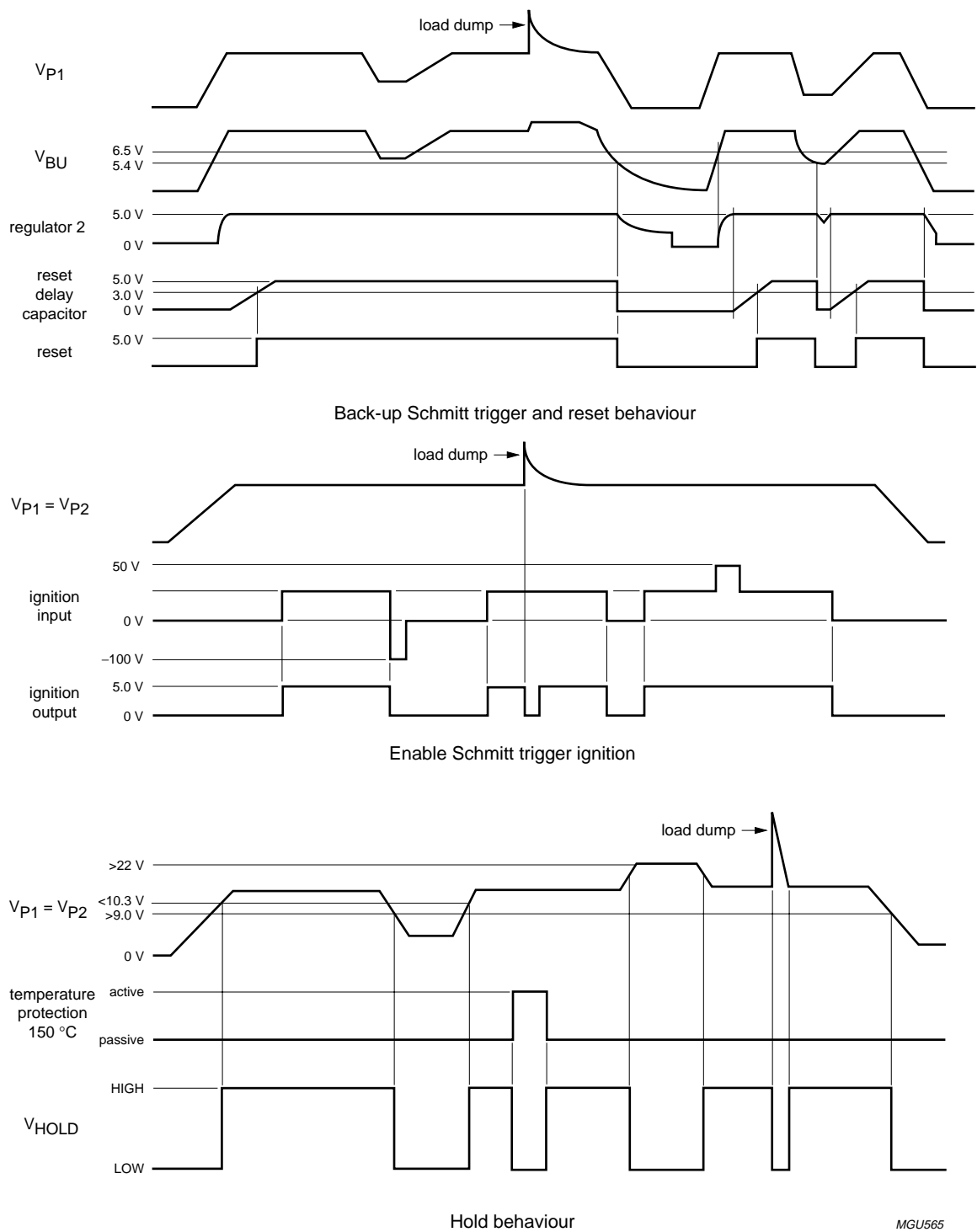


Fig.5 Timing diagram of ignition Schmitt triggers and hold circuit.

Multiple voltage regulator with switch and ignition buffer

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{P1}	supply voltage 1				
	operating		–	18	V
	reverse polarity	non-operating	–	18	V
	jump start	t ≤ 10 minutes	–	30	V
	load dump protection	t ≤ 50 ms; t _r ≥ 2.5 ms	–	50	V
V _{P2}	supply voltage 2				
	operating		–	18	V
	reverse polarity	non-operating	–	18	V
	jump start	t ≤ 10 minutes	–	30	V
	load dump protection	t ≤ 50 ms; t _r ≥ 2.5 ms	–	50	V
P _{tot}	total power dissipation		–	62	W
T _{stg}	storage temperature	non-operating	–55	+150	°C
T _{amb}	ambient temperature	operating	–40	+85	°C
T _j	junction temperature	operating	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-c)}	thermal resistance from junction to case		2	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	50	K/W

QUALITY SPECIFICATION

In accordance with "General Quality Specification For Integrated Circuits (SNW-FQ-611)".

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CHARACTERISTICS

$V_{P1} = V_{P2} = 14.4 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$; measured in test circuit of Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V _{P1}	supply voltage 1					
	operating		9.5	14.4	18	V
	reverse polarity	non-operating	–	–	18	V
	regulator 2 on	note 1	4	14.4	50	V
	jump start	t ≤ 10 minutes	–	–	30	V
	load dump protection	t ≤ 50 ms; t _r ≥ 2.5 ms	–	–	50	V
V _{P2}	supply voltage 2					
	operating		6.5	14.4	18	V
	reverse polarity	non-operating	–	–	18	V
	regulator 2 on		0	–	50	V
	jump start	t ≤ 10 minutes	–	–	30	V
	load dump protection	t ≤ 50 ms; t _r ≥ 2.5 ms	–	–	50	V
V _{bat(loadump)}	battery overvoltage shutdown	V _{P1} and/or V _{P2}	18	20	22	V
I _{q(tot)}	total quiescent supply current	V _P = 12.4 V; note 2	–	105	145	μA
		V _P = 14.4 V; note 2	–	110	150	μA
Schmitt trigger for power supply (regulators 1, 3 and 4)						
V _{th(r)}	rising threshold voltage	V _{P1} rising	6.5	7.0	7.5	V
V _{th(f)}	falling threshold voltage	V _{P1} falling	4.0	4.5	5.0	V
V _{hys}	hysteresis voltage		–	2.5	–	V
Schmitt trigger for enable input (regulators 1, 3, 4 and power switch)						
V _{th(r)}	rising threshold voltage		1.4	1.8	2.4	V
V _{th(f)}	falling threshold voltage		0.9	1.3	1.9	V
V _{hys}	hysteresis voltage	I _{REG} = I _{SW} = 1 mA	–	0.5	–	V
I _{LI}	input leakage current	V _{EN} = 5 V	1	5	20	μA
Reset trigger level of regulator 2						
V _{th(r)}	rising threshold voltage	V _{P1} rising; I _{REG1} = 50 mA; note 3	4.43	V _{REG2} – 0.15	V _{REG2} – 0.1	V
V _{th(f)}	falling threshold voltage	V _{P1} falling; I _{REG1} = 50 mA; note 3	4.4	V _{REG2} – 0.25	V _{REG2} – 0.13	V
Schmitt triggers for hold circuit output						
V _{th(r)(VP)}	rising threshold voltage of supply voltage		9.1	9.7	10.3	V
V _{th(f)(VP)}	falling threshold voltage of supply voltage		9.0	9.4	9.8	V
V _{hys(VP)}	hysteresis voltage of supply voltage		–	0.3	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset and hold buffer						
$I_{\text{sink(L)}}$	LOW-level sink current	$V_{\text{RES}} \leq 0.8 \text{ V}$; $V_{\text{HOLD}} \leq 0.8 \text{ V}$	2	–	–	mA
I_{LO}	output leakage current	$V_{\text{HOLD}} = 5 \text{ V}$	–	0.1	5	μA
$I_{\text{source(H)}}$	HIGH-level source current	$V_{\text{RES}} = 5 \text{ V}$	240	400	900	μA
t_{r}	rise time	note 4	–	7	50	μs
t_{f}	fall time	note 4	–	1	50	μs
Reset delay						
I_{ch}	reset delay capacitor charge current	$V_{\text{CRES}} = 0 \text{ V}$	2	4	8	μA
I_{dch}	reset delay capacitor discharge current	$V_{\text{CRES}} = 3 \text{ V}$; $V_{\text{P1}} = V_{\text{P2}} = 4.3 \text{ V}$	1.0	1.6	–	mA
$V_{\text{th(r)(RES)}}$	rising voltage threshold reset signal		2.5	3.0	3.5	V
$V_{\text{th(f)(RES)}}$	falling voltage threshold reset signal		1.0	1.2	1.4	V
$t_{\text{d(RES)}}$	delay reset signal	$C_{\text{CRES}} = 47 \text{ nF}$; note 5	20	35	70	ms
$t_{\text{d(SW)}}$	delay power switch foldback protection	$C_{\text{CRES}} = 47 \text{ nF}$; note 6	8	17.6	40	ms
Regulator 1 ($I_{\text{REG1}} = 5 \text{ mA}$; unless otherwise specified)						
$V_{\text{o(off)}}$	output voltage off		–	1	400	mV
$V_{\text{o(REG1)}}$	output voltage	$1 \text{ mA} \leq I_{\text{REG1}} \leq 600 \text{ mA}$	8.0	8.5	9.0	V
		$9.5 \text{ V} \leq V_{\text{P1}} \leq 18 \text{ V}$	8.0	8.5	9.0	V
ΔV_{line}	line regulation	$9.5 \text{ V} \leq V_{\text{P1}} \leq 18 \text{ V}$	–	2	75	mV
ΔV_{load}	load regulation	$1 \text{ mA} \leq I_{\text{REG1}} \leq 600 \text{ mA}$	–	20	85	mV
I_{q}	quiescent current	$I_{\text{REG1}} = 600 \text{ mA}$	–	25	60	mA
SVRR	supply voltage ripple rejection	$f_{\text{i}} = 3 \text{ kHz}$; $V_{\text{i}} = 2 \text{ V (p-p)}$	60	70	–	dB
$V_{\text{drop(REG1)}}$	drop-out voltage	$I_{\text{REG1}} = 550 \text{ mA}$; $V_{\text{P1}} = 8.55 \text{ V}$; note 7	–	0.4	0.7	V
$I_{\text{m(REG1)}}$	current limit	$V_{\text{REG1}} > 7 \text{ V}$; note 8	0.65	1.2	–	A
$I_{\text{sc(REG1)}}$	short-circuit current	$R_{\text{L}} \leq 0.5 \Omega$; note 9	250	800	–	mA
Regulator 2 ($I_{\text{REG2}} = 5 \text{ mA}$; unless otherwise specified)						
$V_{\text{o(REG2)}}$	output voltage	$0.5 \text{ mA} \leq I_{\text{REG2}} \leq 300 \text{ mA}$	4.75	5.0	5.25	V
		$7 \text{ V} \leq V_{\text{P1}} \leq 18 \text{ V}$	4.75	5.0	5.25	V
		$18 \text{ V} \leq V_{\text{P1}} \leq 50 \text{ V}$; $I_{\text{REG2}} \leq 150 \text{ mA}$	4.75	5.0	5.25	V
ΔV_{line}	line regulation	$6 \text{ V} \leq V_{\text{P1}} \leq 18 \text{ V}$	–	2	50	mV
		$6 \text{ V} \leq V_{\text{P1}} \leq 50 \text{ V}$	–	15	75	mV
ΔV_{load}	load regulation	$1 \text{ mA} \leq I_{\text{REG2}} \leq 150 \text{ mA}$	–	20	50	mV
		$1 \text{ mA} \leq I_{\text{REG2}} \leq 300 \text{ mA}$	–	–	100	mV

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SVRR	supply voltage ripple rejection	$f_i = 3 \text{ kHz}$; $V_i = 2 \text{ V (p-p)}$	50	55	–	dB
$V_{\text{drop(REG2)}}$	drop-out voltage	$I_{\text{REG2}} = 100 \text{ mA}$; $V_{P1} = 4.75 \text{ V}$; note 7	–	0.4	0.6	V
		$I_{\text{REG2}} = 200 \text{ mA}$; $V_{P1} = 5.75 \text{ V}$; note 7	–	0.8	1.2	V
		$I_{\text{REG2}} = 100 \text{ mA}$; $V_{BU} = 4.75 \text{ V}$; note 10	–	0.2	0.5	V
		$I_{\text{REG2}} = 200 \text{ mA}$; $V_{BU} = 5.75 \text{ V}$; note 10	–	0.8	1.0	V
$I_{m(\text{REG2})}$	current limit	$V_{\text{REG2}} > 4.5 \text{ V}$; note 8	0.32	0.37	–	A
$I_{sc(\text{REG2})}$	short-circuit current	$R_L \leq 0.5 \Omega$; note 9	95	120	–	mA
Regulator 3 ($I_{\text{REG3}} = 5 \text{ mA}$; unless otherwise specified)						
$V_{o(\text{off})}$	output voltage off		–	1	400	mV
$V_{o(\text{REG3})}$	output voltage	$1 \text{ mA} \leq I_{\text{REG3}} \leq 1400 \text{ mA}$	4.75	5.0	5.25	V
		$7 \text{ V} \leq V_{P1}$ and/or $V_{P2} \leq 18 \text{ V}$	4.75	5.0	5.25	V
ΔV_{line}	line regulation	$7 \text{ V} \leq V_{P1}$ and/or $V_{P2} \leq 18 \text{ V}$	–	2	50	mV
ΔV_{load}	load regulation	$1 \text{ mA} \leq I_{\text{REG3}} \leq 1400 \text{ mA}$	–	20	150	mV
I_q	quiescent current	$I_{\text{REG3}} = 1400 \text{ mA}$	–	19	45	mA
SVRR	supply voltage ripple rejection	$f_i = 3 \text{ kHz}$; $V_i = 2 \text{ V (p-p)}$	60	70	–	dB
$V_{\text{drop(REG3)}}$	drop-out voltage	$I_{\text{REG3}} = 1400 \text{ mA}$; $V_{P2} = 6 \text{ V}$; note 7	–	1	1.5	V
$I_{m(\text{REG3})}$	current limit	$V_{\text{REG3}} > 4.5 \text{ V}$; note 8	1.5	1.7	–	A
$I_{sc(\text{REG3})}$	short-circuit current	$R_L \leq 0.5 \Omega$; note 9	430	750	–	mA
Regulator 4 ($I_{\text{REG4}} = 5 \text{ mA}$; unless otherwise specified)						
$V_{o(\text{off})}$	output voltage off		–	1	400	mV
$V_{o(\text{REG4})}$	output voltage	$1 \text{ mA} \leq I_{\text{REG4}} \leq 1 \text{ A}$	3.14	3.3	3.46	V
		$6.5 \text{ V} \leq V_{P1}$ and/or $V_{P2} \leq 18 \text{ V}$	3.14	3.3	3.46	V
ΔV_{line}	line regulation	$6.5 \text{ V} \leq V_{P1}$ and/or $V_{P2} \leq 18 \text{ V}$	–	2	50	mV
ΔV_{load}	load regulation	$1 \text{ mA} \leq I_{\text{REG4}} \leq 1 \text{ A}$	–	20	50	mV
I_q	quiescent current	$I_{\text{REG4}} = 1 \text{ A}$	–	15	40	mA
SVRR	supply voltage ripple rejection	$f_i = 3 \text{ kHz}$; $V_i = 2 \text{ V (p-p)}$	60	70	–	dB
$V_{\text{drop(REG4)}}$	drop-out voltage	$I_{\text{REG4}} = 1 \text{ A}$; $V_{P2} = 5 \text{ V}$; note 7	–	1.7	2.4	V
$I_{m(\text{REG4})}$	current limit	$V_{\text{REG4}} > 3.0 \text{ V}$; note 8	1.1	1.5	–	A
$I_{sc(\text{REG4})}$	short-circuit current	$R_L \leq 0.5 \Omega$; note 9	470	750	–	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power switch						
$V_{\text{drop(SW)}}$	drop-out voltage	$I_{\text{SW}} = 1 \text{ A}$; $V_{\text{P1}} = 13.5 \text{ V}$; note 11	–	0.45	0.65	V
		$I_{\text{SW}} = 1.8 \text{ A}$; $V_{\text{P1}} = 13.5 \text{ V}$; note 11	–	1.0	1.8	V
$I_{\text{DC(SW)}}$	continuous current	$V_{\text{P1}} = 16 \text{ V}$; $V_{\text{SW}} = 13.5 \text{ V}$	1.8	2.0	–	A
$V_{\text{clamp(SW)}}$	clamping voltage	$V_{\text{P1}} \geq 17 \text{ V}$; $1 \text{ mA} < I_{\text{SW}} < 1.8 \text{ A}$	13.5	15.0	16.0	V
$I_{\text{M(SW)}}$	peak current	$V_{\text{P1}} < 17 \text{ V}$; notes 6, 12 and 13	3	–	–	A
$V_{\text{fb(SW)}}$	flyback voltage behaviour	$I_{\text{SW}} = -100 \text{ mA}$	–	$V_{\text{P1}} + 3$	22	V
$I_{\text{sc(SW)}}$	short-circuit current	$V_{\text{SW}} < 1.2 \text{ V}$; note 13	0.5	1.7	–	A
Backup switch						
$I_{\text{DC(BU)}}$	continuous current	$V_{\text{BU}} > 5 \text{ V}$	0.3	0.35	–	A
$V_{\text{clamp(BU)}}$	clamping voltage	$V_{\text{P1}} \geq 16.7 \text{ V}$; $I_{\text{REG2}} = 100 \text{ mA}$	–	–	16	V
$I_{\text{r(BU)}}$	reverse current	$V_{\text{P1}} = 0 \text{ V}$; $V_{\text{BU}} = 12.4 \text{ V}$	–	–	900	μA
Schmitt trigger for enable of ignition input						
$V_{\text{th(r)(IGNIN)}}$	rising threshold voltage of ignition input	$V_{\text{P1}} > 3.5 \text{ V}$	1.9	2.2	2.5	V
$V_{\text{th(f)(IGNIN)}}$	falling threshold voltage of ignition input	$V_{\text{P1}} > 3.5 \text{ V}$	1.7	2.0	2.3	V
$V_{\text{hys(IGNIN)}}$	hysteresis voltage	$V_{\text{P}} > 3.5 \text{ V}$	0.1	0.2	0.5	V
I_{LI}	input leakage current	$V_{\text{IGNIN}} = 5 \text{ V}$	–	–	1.0	μA
$I_{\text{i(clamp)}}$	input clamp current	$V_{\text{IGNIN}} > 50 \text{ V}$	–	–	50	mA
$V_{\text{IH(clamp)}}$	HIGH-level input clamping voltage		V_{P1}	–	50	V
$V_{\text{IL(clamp)}}$	LOW-level input clamping voltage		–0.6	–	0	V
Ignition buffer						
V_{OL}	LOW-level output voltage	$I_{\text{IGNOUT}} = 0 \text{ mA}$	0	0.2	0.8	V
V_{OH}	HIGH-level output voltage	$I_{\text{IGNOUT}} = 0 \text{ mA}$	4.5	5.0	5.25	V
I_{OL}	LOW-level output current	$V_{\text{IGNOUT}} \leq 0.8 \text{ V}$	0.45	0.8	–	mA
I_{OH}	HIGH-level output current	$V_{\text{IGNOUT}} \geq 4.5 \text{ V}$	–0.45	–2.0	–	mA
I_{LO}	output leakage current (source)	$V_{\text{IGNOUT}} = 5 \text{ V}$; $V_{\text{IGNIN}} = 0 \text{ V}$	–	–	1.0	μA
t_{PLH}	LOW-to-HIGH propagation time	V_{IGNIN} rising from 1.7 to 2.5 V	–	–	500	μs
t_{PHL}	HIGH-to-LOW propagation time	V_{IGNIN} falling from 2.5 to 1.7 V	–	–	500	μs

Multiple voltage regulator with switch and ignition buffer

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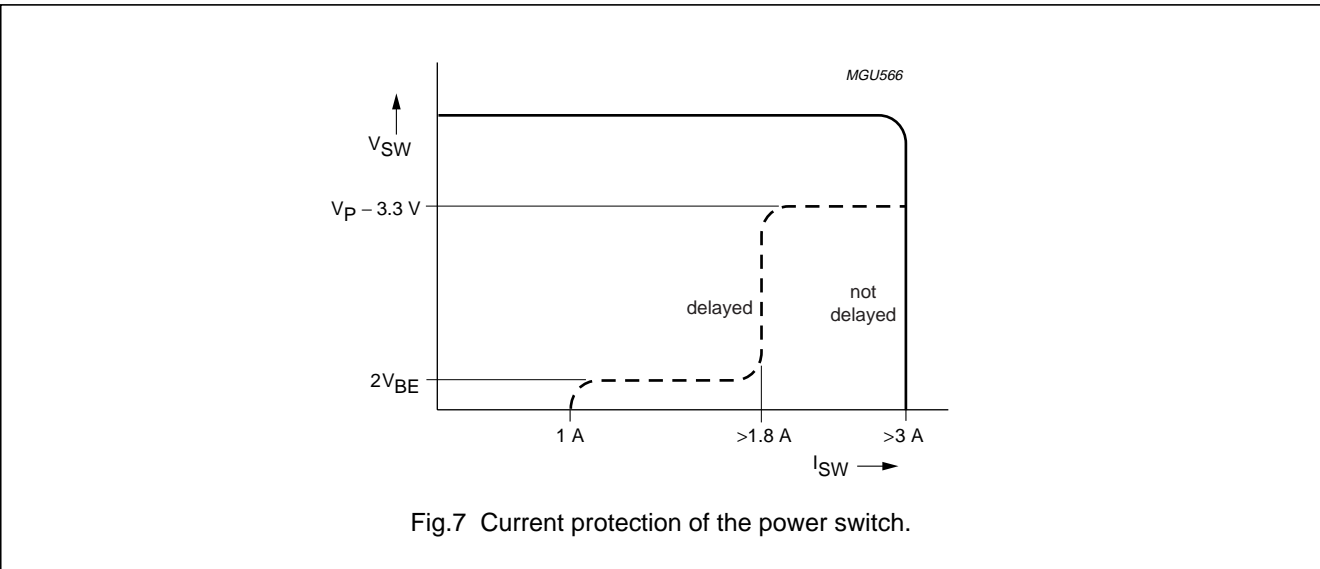
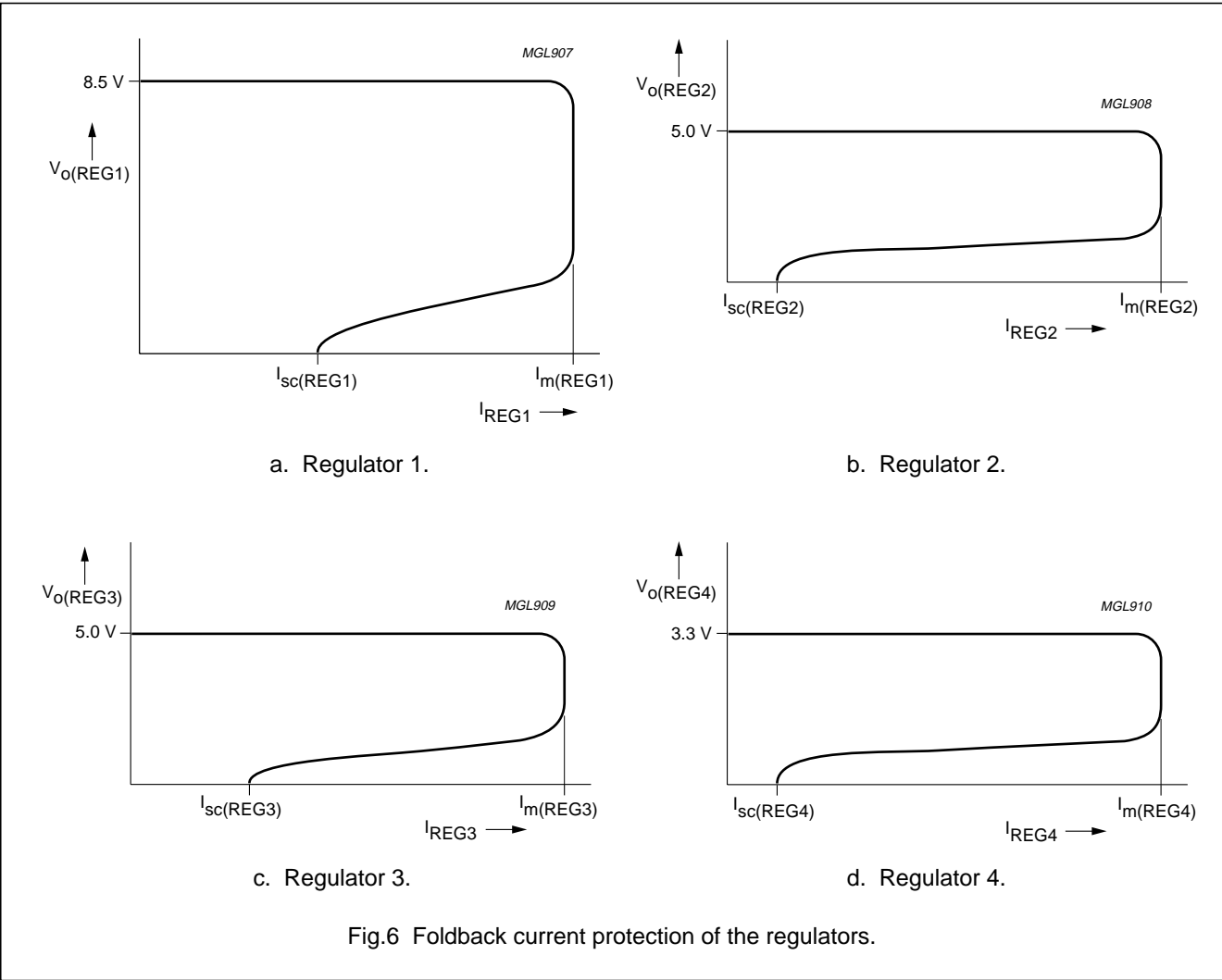
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Temperature protection						
$T_{j(sd)}$	junction temperature for shutdown		150	160	170	°C
$T_{j(hold)}$	junction temperature for hold trigger		150	160	170	°C

Notes

- Minimum operating voltage, only if V_{P1} has exceeded 6.5 V.
- The total quiescent current is measured in the standby mode. Therefore, the enable inputs of regulators 1, 3, 4 and the power switch are grounded and $R_{L(REG2)} = \infty$ (see Fig.8).
- The voltage of the regulator drops as a result of a V_{P1} drop for regulators 1 and 2. Regulators 3 and 4 drop as a result of V_{P2} drop.
- The rise and fall times are measured with a 10 kΩ pull-up resistor and a 50 pF load capacitor.
- The delay time depends on the value of the reset delay capacitor: $t_{d(RES)} = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (750 \times 10^3)[s]$
- The delay time depends on the value of the reset delay capacitor: $t_{d(SW)} = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (375 \times 10^3)[s]$
- The drop-out voltage of regulators 1 and 2 is measured between pins V_{P1} and REGn. The drop-out voltage of regulators 3 and 4 is measured between pins V_{P2} and REGn.
- At current limit, $I_{m(REGn)}$ is held constant (see Fig.6).
- The foldback current protection limits the dissipated power at short-circuit (see Fig.6).
- The drop-out voltage is measured between pins BU and REG2.
- The drop-out voltage of the power switch is measured between pins V_{P1} and SW.
- The maximum output current of the power switch is limited to 1.8 A when the supply voltage exceeds 18 V.
- At short-circuit, $I_{sc(SW)}$ of the power switch is held constant to a lower value than the continuous current after a delay of at least 10 ms (see Fig.7).

Multiple voltage regulator with
switch and ignition buffer

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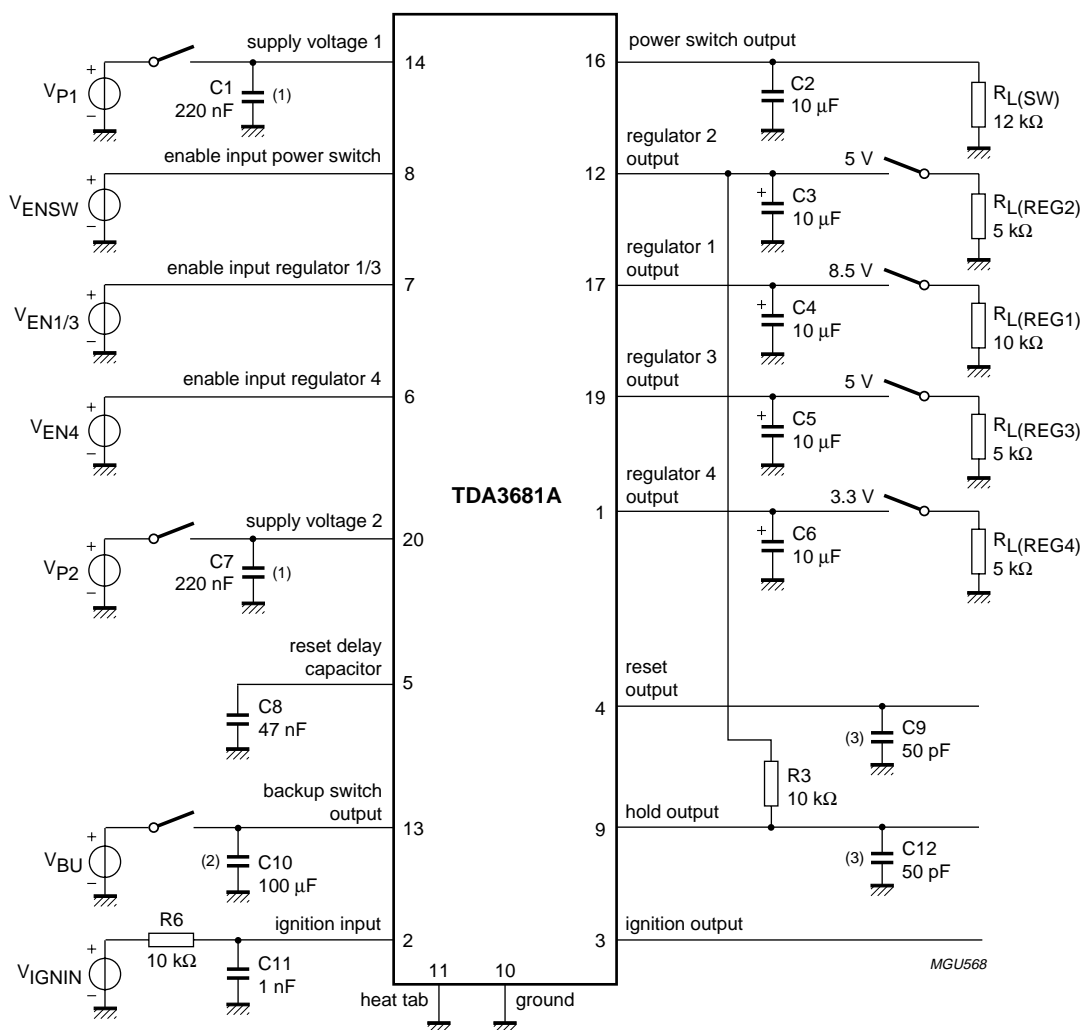


Multiple voltage regulator with switch and ignition buffer

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TEST AND APPLICATION INFORMATION

Test information



- (1) A minimum capacitor of 220 nF on the supply lines V_{P1} and V_{P2} is required for stability.
- (2) A minimum capacitor of 1 μ F for backup supply is required for stability.
- (3) These capacitors represent the typical input capacitance of CMOS logic connected to the reset and hold outputs.

Fig.8 Test circuit.

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Application information

NOISE

Table 1 Noise figures

REGULATOR	NOISE FIGURE (μV) ⁽¹⁾		
	$C_o = 10\ \mu\text{F}$	$C_o = 47\ \mu\text{F}$	$C_o = 100\ \mu\text{F}$
1	170	110	110
2	440	240	190
3	120	100	80
4	85	70	55

Note

1. Measured at a bandwidth of 30 kHz.

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (the output noise of the regulators is translated to a current noise by the output capacitors). The noise is minimal when a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100 μF is connected directly to the supply pins V_{P1} , V_{P2} and GND.

STABILITY

The regulators are stabilized by the externally connected output capacitors.

The output capacitors can be selected by using the graphs given in Figs 9 and 10. When an electrolytic capacitor is used, its temperature behaviour can cause oscillations at a low temperature. The two examples below show how an output capacitor value is selected.

Example 1

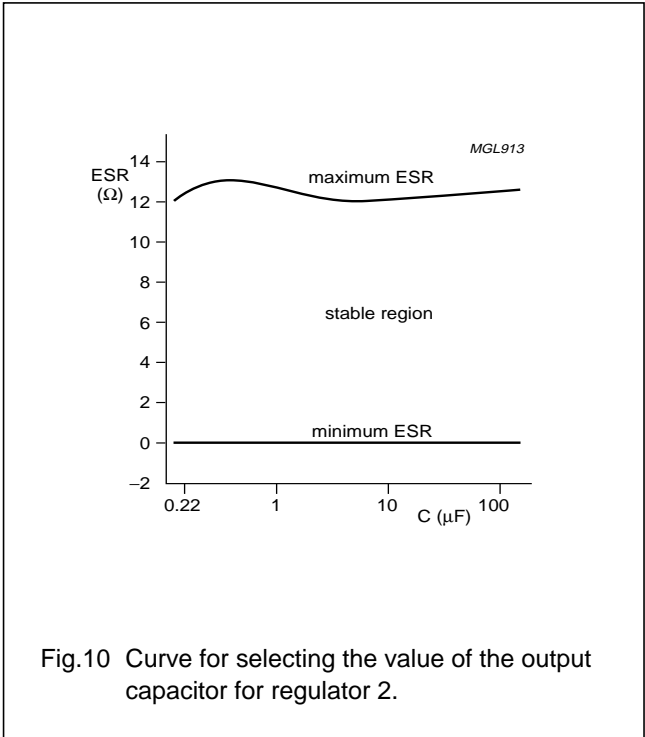
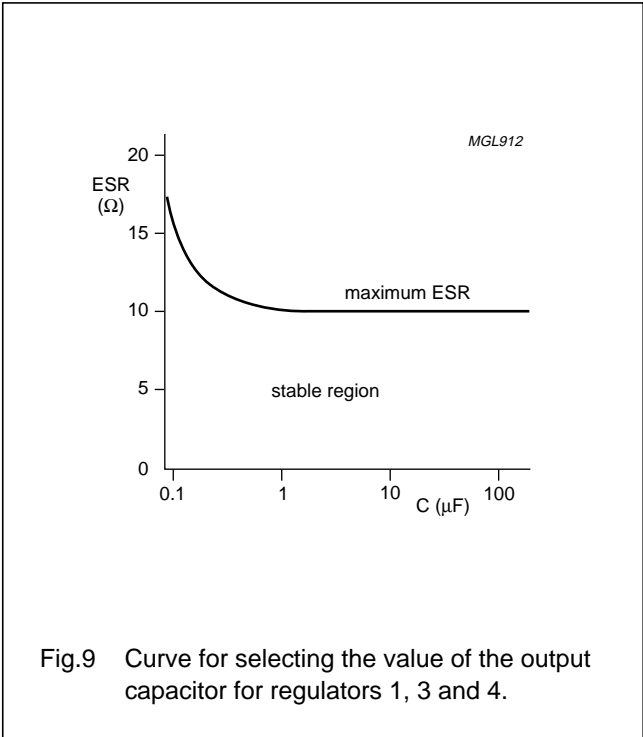
Regulators 1, 3 and 4 are stabilized with an electrolytic output capacitor of 220 μF (ESR = 0.15 Ω). At $T_{\text{amb}} = -30\ ^\circ\text{C}$, the capacitor value is decreased to 73 μF and the ESR is increased to 1.1 Ω . The regulator remains stable at $T_{\text{amb}} = -30\ ^\circ\text{C}$ (see Fig.9).

Example 2

Regulator 2 is stabilized with a 10 μF electrolytic capacitor (ESR = 3 Ω). At $T_{\text{amb}} = -30\ ^\circ\text{C}$, the capacitor value is decreased to 3 μF and the ESR is increased to 23.1 Ω . As can be seen from Fig.10, the regulator will be unstable at $T_{\text{amb}} = -30\ ^\circ\text{C}$.

Solution

To avoid problems with stability at low temperatures, the use of tantalum capacitors is recommended. Use a tantalum capacitor of 10 μF or a larger electrolytic capacitor.



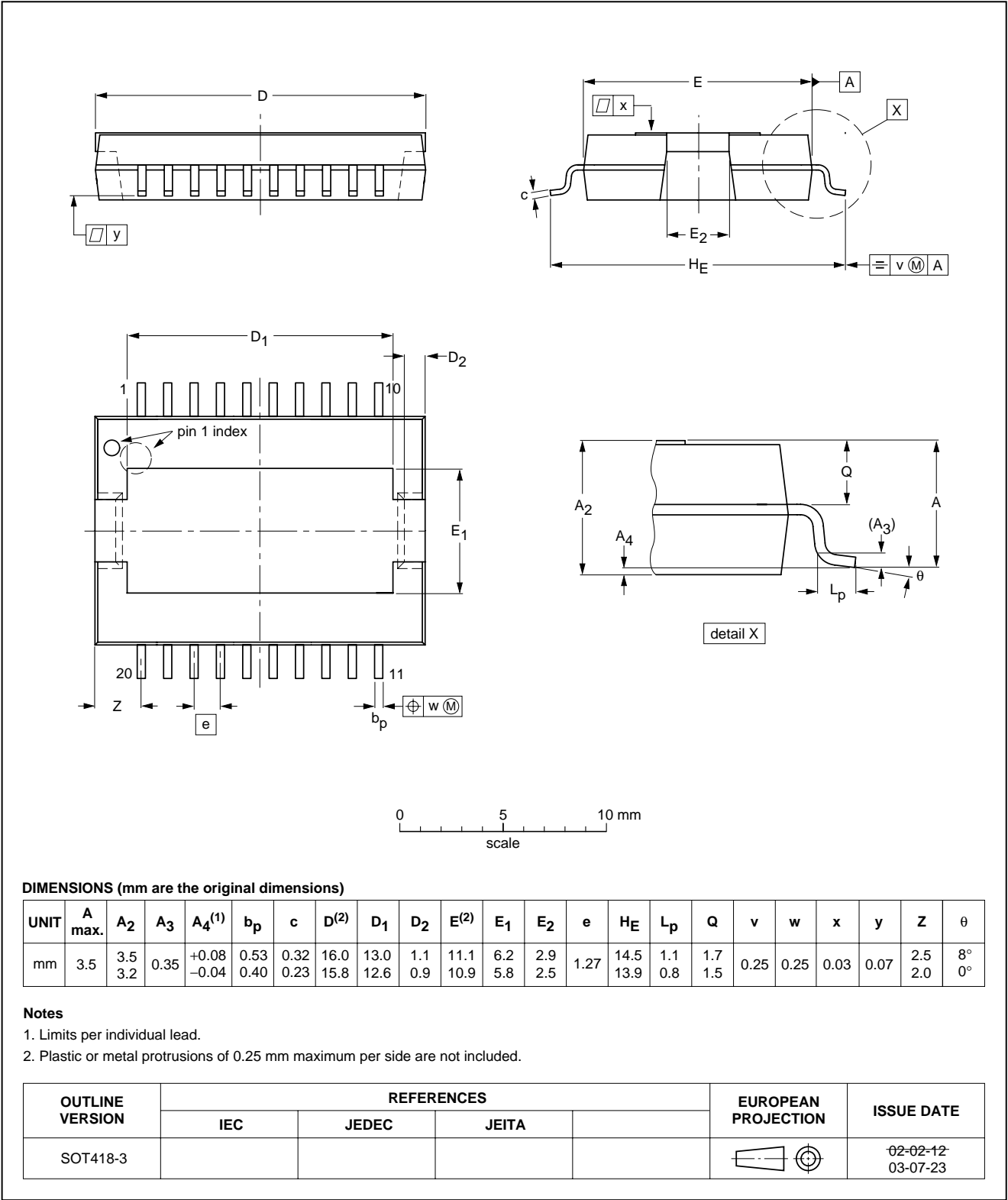
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PACKAGE OUTLINE

HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height

SOT418-3



Multiple voltage regulator with switch and ignition buffer

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA and SSOP-T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Multiple voltage regulator with switch and ignition buffer

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE ⁽¹⁾	SOLDERING METHOD	
	WAVE	REFLOW ⁽²⁾
BGA, LBGA, LFBGA, SQFP, SSOP-T ⁽³⁾ , TFBGA, VFBGA DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS PLCC ⁽⁵⁾ , SO, SOJ LQFP, QFP, TQFP SSOP, TSSOP, VSO, VSSOP PMFP ⁽⁸⁾	not suitable not suitable ⁽⁴⁾ suitable not recommended ⁽⁵⁾⁽⁶⁾ not recommended ⁽⁷⁾ not suitable	suitable suitable suitable suitable suitable not suitable

Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding $217\text{ °C} \pm 10\text{ °C}$ measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- Hot bar or manual soldering is suitable for PMFP packages.

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DATA SHEET STATUS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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