

**SN74BCT2245**  
**OCTAL TRANSCEIVER AND LINE/MOS DRIVER**  
**WITH 3-STATE OUTPUTS**

SCBS102C – FEBRUARY 1992 – REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design  
Significantly Reduces  $I_{CCZ}$
- B Port Has Equivalent 33- $\Omega$  Series  
Resistors, So No External Resistors  
Are Required
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description/ordering information

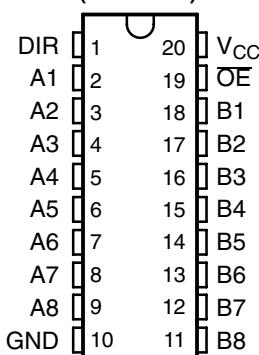
The SN74BCT2245 octal transceiver and line/MOS driver is designed for asynchronous communication between data buses.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can disable the devices so that both buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The B-port outputs, which are designed to source or sink up to 12 mA, include 33- $\Omega$  series resistors to reduce overshoot and undershoot.

**DB, DW, N, OR NS PACKAGE  
(TOP VIEW)**



#### ORDERING INFORMATION

<b>T<sub>A</sub></b>	<b>PACKAGE<sup>†</sup></b>		<b>ORDERABLE PART NUMBER</b>	<b>TOP-SIDE MARKING</b>
0°C to 70°C	PDIP – N	Tube	SN74BCT2245N	SN74BCT2245N
	SOIC – DW	Tube	SN74BCT2245DW	BCT2245
		Tape and reel	SN74BCT2245DWR	
	SOP – NS	Tape and reel	SN74BCT2245NSR	BCT2245
	SSOP – DB	Tape and reel	SN74BCT2245DBR	BA245

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE

<b>INPUTS</b>		<b>OPERATION</b>
<b>OE</b>	<b>DIR</b>	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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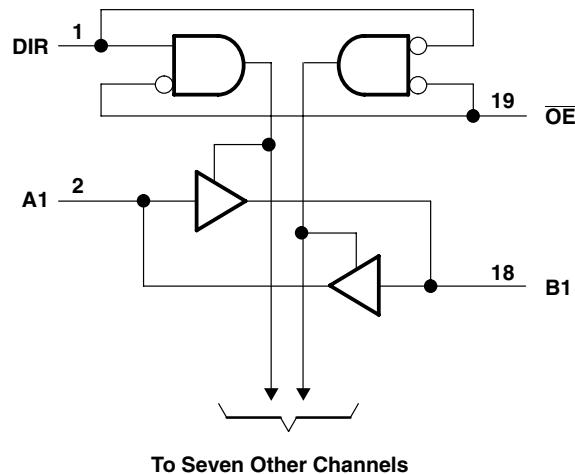


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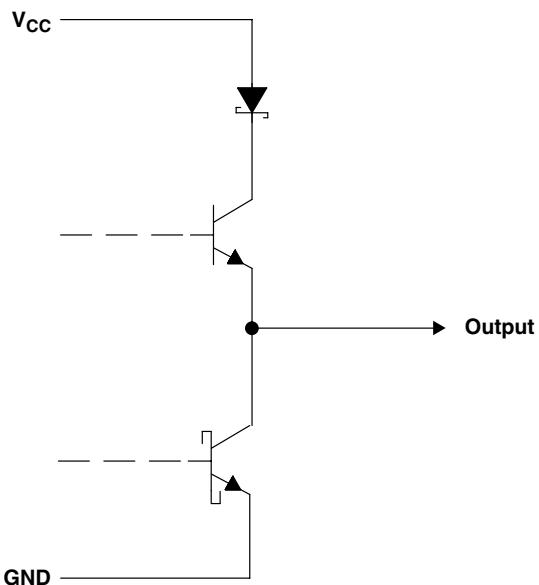
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SCBS102C – FEBRUARY 1992 – REVISED MARCH 2003

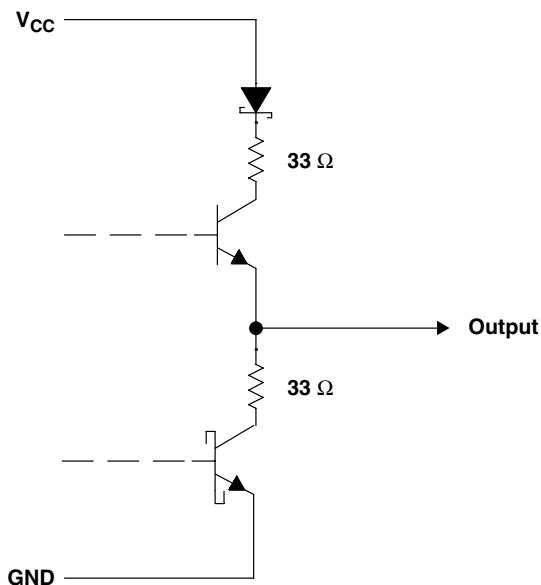
**logic diagram (positive logic)**



**schematic of A-port outputs**



**schematic of B-port outputs**



All resistor values shown are nominal.

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SCBS102C – FEBRUARY 1992 – REVISED MARCH 2003

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ .....	-0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ .....	-30 mA
Current into any output in the low state, $I_O$ .....	60 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current	A port		-3	mA
		B port		-12	
$I_{OL}$	Low-level output current	A port		24	mA
		B port		12	
$T_A$	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74BCT2245****OCTAL TRANSCEIVER AND LINE/MOS DRIVER  
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SCBS102C – FEBRUARY 1992 – REVISED MARCH 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

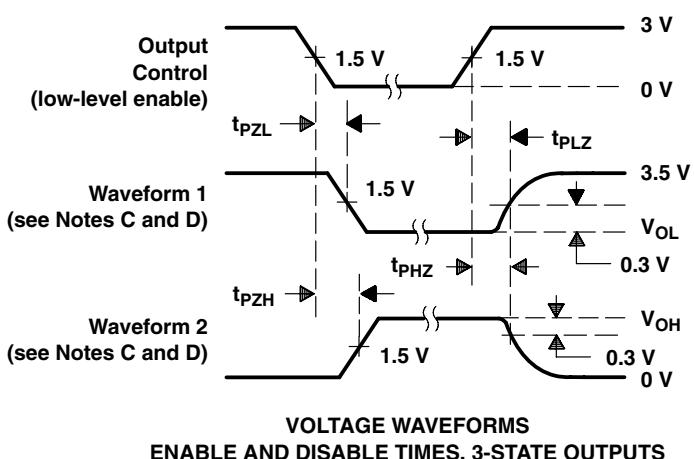
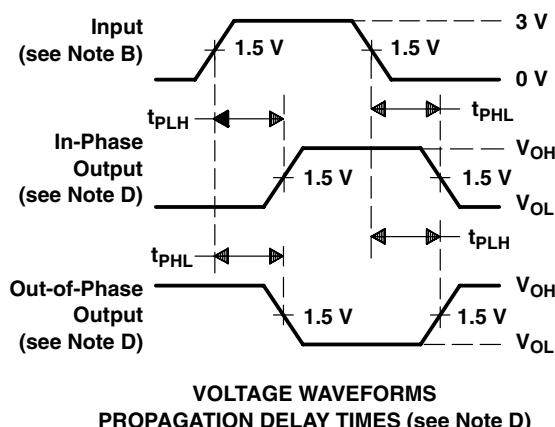
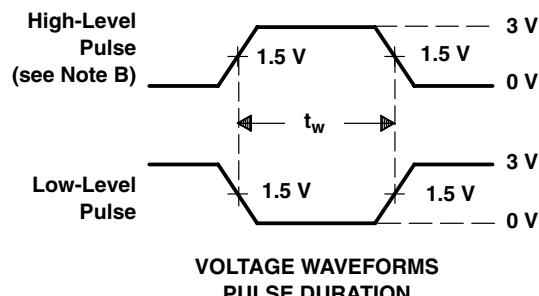
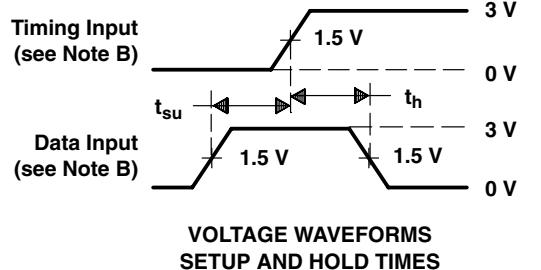
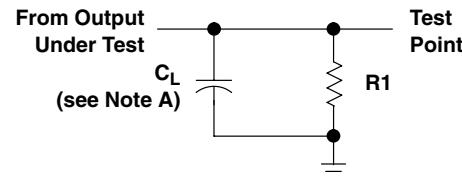
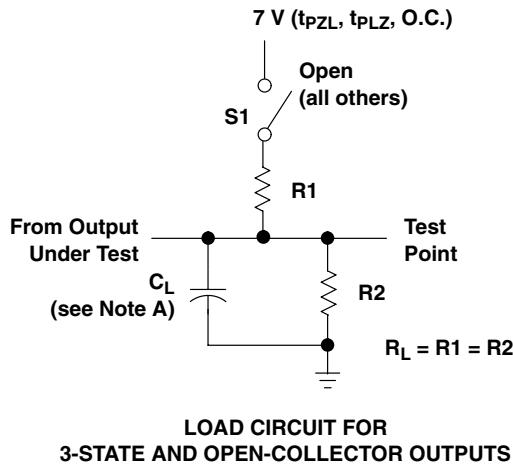
PARAMETER		TEST CONDITIONS			MIN	TYP <sup>†</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5$ V, $I_I = -18$ mA					-1.2	V
$V_{OH}$	A port	$V_{CC} = 4.5$ V	$I_{OH} = -1$ mA		2.5	3.4		V
			$I_{OH} = -3$ mA		2.4	3.3		
	B port	$V_{CC} = 4.5$ V	$I_{OH} = -1$ mA		2.4	3.3		
			$I_{OH} = -12$ mA		2	3.2		
$V_{OL}$	A port	$V_{CC} = 4.5$ V	$I_{OL} = 24$ mA		0.35	0.5		V
			$I_{OL} = 1$ mA			0.5		
	B port	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA			0.8		
$I_I$		$V_{CC} = 5.5$ V, $V_I = 5.5$ V				0.1		mA
$I_{IH}^{\ddagger}$	A or B port Control input	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V		70			$\mu$ A
						20		
$I_{IL}^{\ddagger}$		$V_{CC} = 5.5$ V, $V_I = 0.5$ V				-0.65		mA
$I_{OS}^{\$}$	A port B port	$V_{CC} = 5.5$ V,	$V_O = 0$		-60	-150		mA
					-100	-225		
$I_{CCL}$	A to B B to A	$V_{CC} = 5.5$ V,	Outputs open		63	100		mA
					40	64		
$I_{CCH}$	A to B B to A	$V_{CC} = 5.5$ V,	Outputs open		37	59		mA
					29	46		
$I_{CCZ}$	A to B B to A	$V_{CC} = 5.5$ V,	Outputs open		9	15		mA
					8	14		
$C_i$	Control input	$V_{CC} = 5$ V, $V_I = 2.5$ V or 0.5 V			7			pF
$C_{io}$	A to B B to A	$V_{CC} = 5$ V,	$V_O = 2.5$ V or 0.5 V		9			pF
					12			

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^{\circ}\text{C}$ .<sup>‡</sup> For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^{\circ}\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A	B	1	3.3	4.9	1	5.8	ns
			1.7	4.2	6.1	1.7	7	
$t_{PHL}$	A	B	2.5	5.1	6.9	2.5	7.8	ns
			2.2	4.7	7.1	2.2	7.7	
$t_{PZH}$	$\overline{OE}$	B	3.2	6.2	8.6	3.2	9.9	ns
			3.8	7.2	9.5	3.8	11.1	
$t_{PZL}$	$\overline{OE}$	B	5.6	8.3	10.9	5.6	12.2	ns
			4.2	7.6	10.1	4.2	11.4	
$t_{PHZ}$	$\overline{OE}$	B	2.6	5.2	7.1	2.6	8.2	ns
			3.1	5.7	8	3.1	9.4	
$t_{PLZ}$	$\overline{OE}$	B	3.5	6	7.9	3.5	9.2	ns
			2.3	4.7	6.5	2.3	7.6	

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PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
 F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74BCT2245DBLE	OBsolete	SSOP	DB	20		TBD	Call TI	Call TI
SN74BCT2245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2245DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2245DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2245DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2245DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT2245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT2245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2245NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2245NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

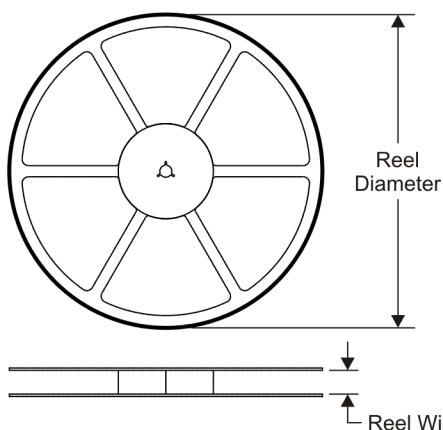
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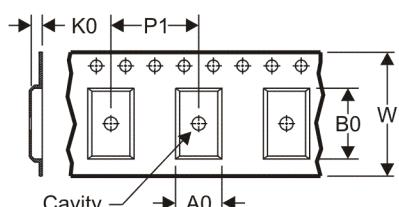
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## TAPE AND REEL INFORMATION

## REEL DIMENSIONS

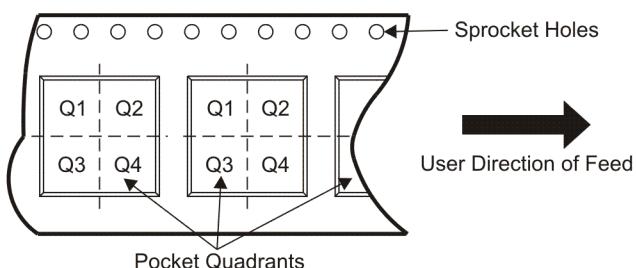


## TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

All dimensions are nominal													
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
SN74BCT2245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1	
SN74BCT2245NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1	

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT2245DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74BCT2245NSR	SO	NS	20	2000	346.0	346.0	41.0

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



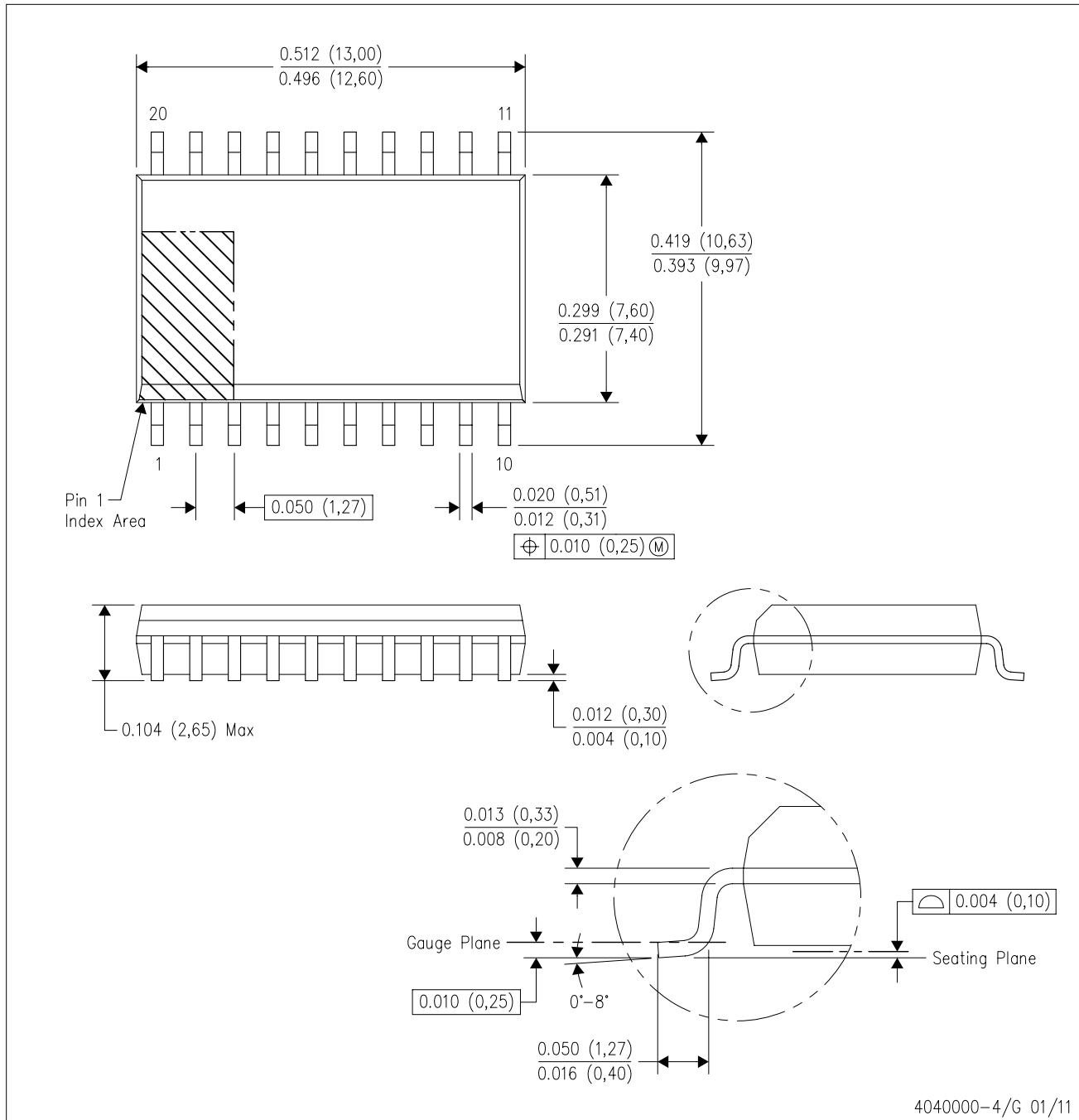
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

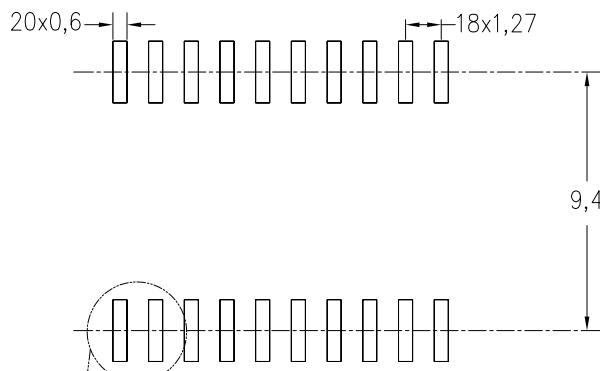
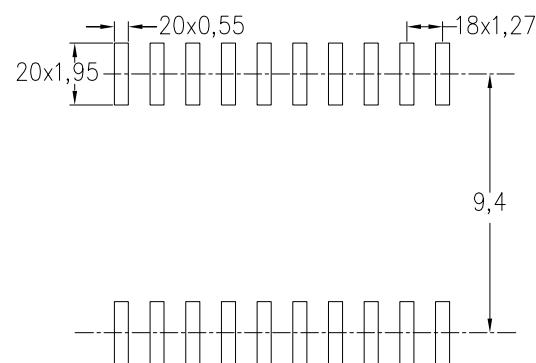


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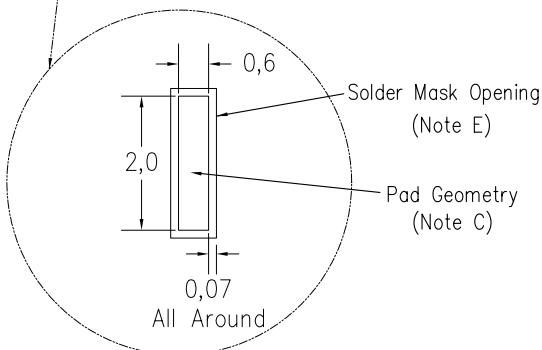
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



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NOTES:

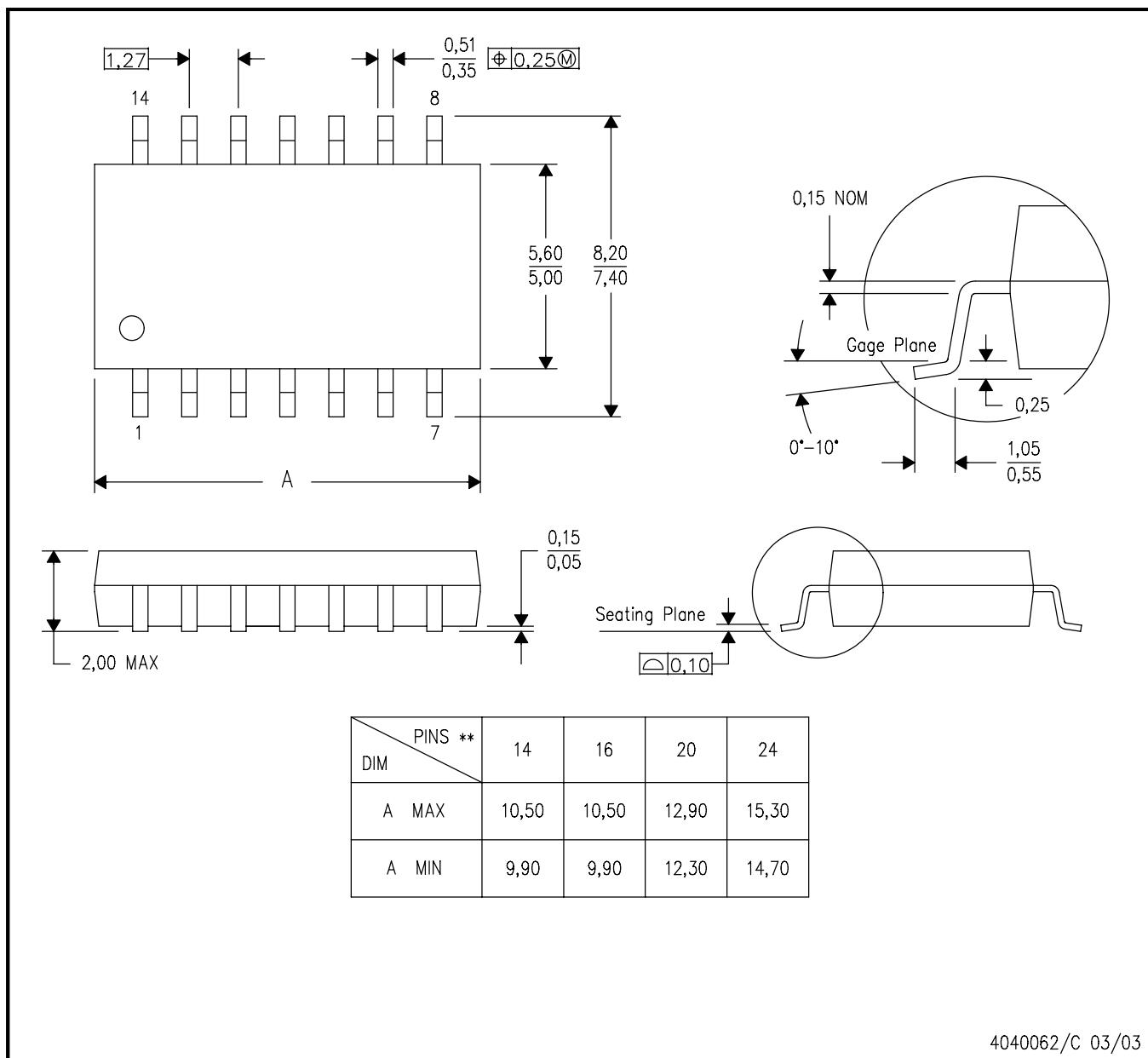
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



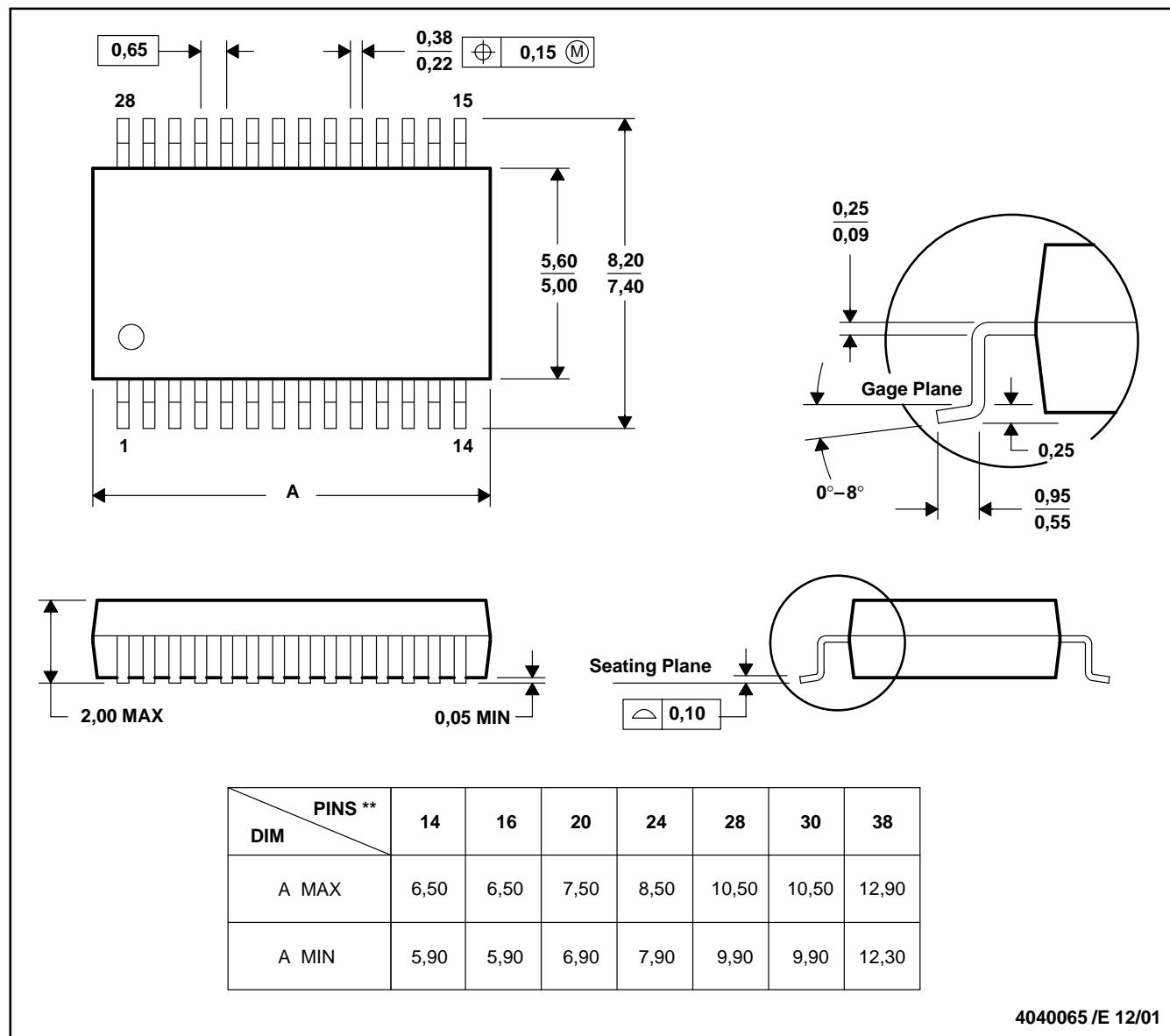
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NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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