

Active Clamp Synchronous Forward Controllers with Internal Housekeeping Controller

FEATURES

- **Input Voltage Range:** LT3752: 6.5V to 100V, LT3752-1: Limited Only by External Components
- **Internal Housekeeping DC/DC Controller**
- **Programmable Volt-Second Clamp**
- **High Efficiency Control: Active Clamp, Synchronous Rectification, Programmable Delays**
- Short-Circuit (Hiccup Mode) Overcurrent Protection
- Programmable Soft-Start/Stop
- Programmable OVLO and UVLO with Hysteresis
- Programmable Frequency (100kHz to 500kHz)
- Synchronizable to an External Clock

APPLICATIONS

- Offline and HV Car Battery Isolated Power Supplies
- 48V Telecommunication Isolated Power Supplies
- Industrial, Automotive and Military Systems

DESCRIPTION

The LT[®]3752/LT3752-1 are current mode PWM controllers optimized for an active clamp forward converter topology. A DC/DC housekeeping controller is included for improved efficiency and performance. The LT3752 allows operation up to 100V input and the LT3752-1 is optimized for applications with input voltages greater than 100V.

A programmable volt-second clamp allows primary switch duty cycles above 50% for high switch, transformer and rectifier utilization. Active clamp control reduces switch voltage stress and increases efficiency. A synchronous output is available for controlling secondary side synchronous rectification.

The LT3752/LT3752-1 are available in a 38-lead plastic TSSOP package with missing pins for high voltage spacings.

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TYPICAL APPLICATION

18V to 72V, 12V/12.5A, 150W Active Clamp Isolated Forward Converter

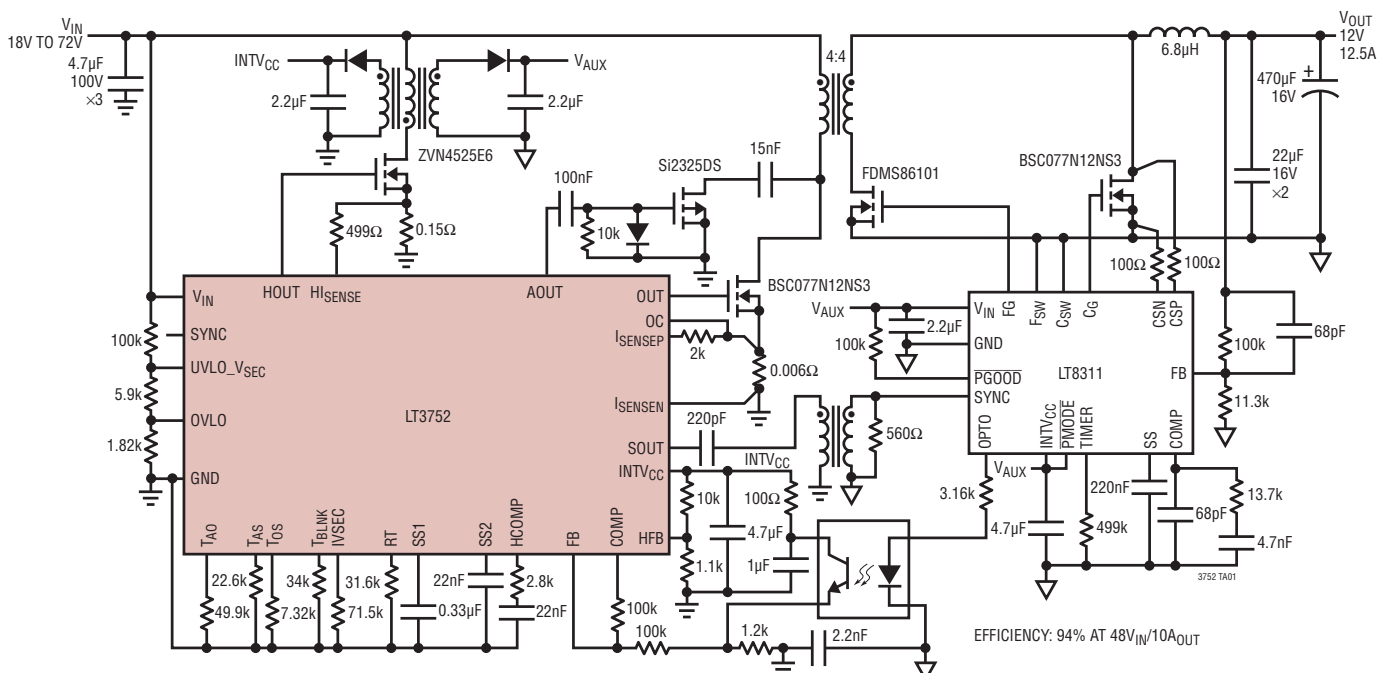


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ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} (LT3752)	100V
UVLO_VSEC, OVLO	20V
V_{IN} (LT3752-1)	16V, 8mA
INTV _{CC} , SS2	16V
FB, SYNC	6V
SS1, COMP, HCOMP, HFB, RT	3V
I _{SENSEP} , I _{SENSEN} , OC, HI _{SENSE}	0.35V
IVSEC	-250μA

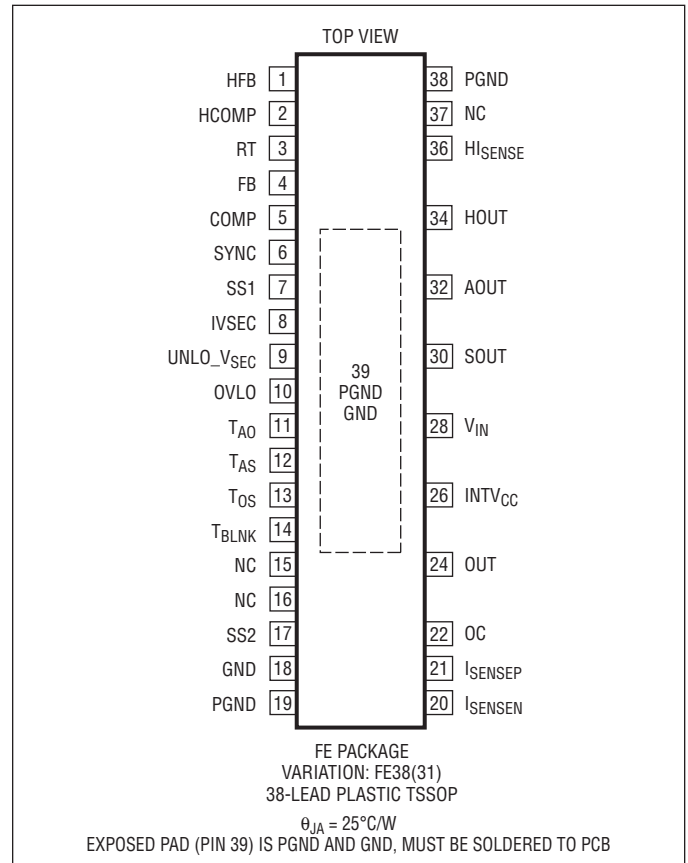
Operating Junction Temperature Range (Notes 2, 3)

LT3752EFE, LT3752EFE-1	-40°C to 125°C
LT3752IFE, LT3752IFE-1	-40°C to 125°C
LT3752HFE, LT3752HFE-1	-40°C to 150°C
LT3752MPFE, LT3752MPFE-1	-55°C to 150°C

Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10 Sec) 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3752EFE#PBF	LT3752EFE#TRPBF	LT3752FE	38-Lead Plastic TSSOP	-40°C to 125°C
LT3752IFE#PBF	LT3752IFE#TRPBF	LT3752FE	38-Lead Plastic TSSOP	-40°C to 125°C
LT3752HFE#PBF	LT3752HFE#TRPBF	LT3752FE	38-Lead Plastic TSSOP	-40°C to 150°C
LT3752MPFE#PBF	LT3752MPFE#TRPBF	LT3752FE	38-Lead Plastic TSSOP	-55°C to 150°C
LT3752EFE-1#PBF	LT3752EFE-1#TRPBF	LT3752FE-1	38-Lead Plastic TSSOP	-40°C to 125°C
LT3752IFE-1#PBF	LT3752IFE-1#TRPBF	LT3752FE-1	38-Lead Plastic TSSOP	-40°C to 125°C
LT3752HFE-1#PBF	LT3752HFE-1#TRPBF	LT3752FE-1	38-Lead Plastic TSSOP	-40°C to 150°C
LT3752MPFE-1#PBF	LT3752MPFE-1#TRPBF	LT3752FE-1	38-Lead Plastic TSSOP	-55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

LT3752/LT3752-1

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 12\text{V}$, $UVLO_V_{SEC} = 2.5\text{V}$.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operational Input Voltage (LT3752)		●	6.5		100	V
Operational Input Voltage (LT3752-1)		●	10.5		16	V
$V_{IN(ON)}$ (LT3752)		●		5.8	6.4	V
$V_{IN(OFF)}$ (LT3752)				5.5	5.9	V
$V_{IN(ON/OFF)}$ Hysteresis (LT3752)		●	0.1	0.3	0.5	V
$V_{IN(ON)}$ (LT3752-1)		●		9.5	10.4	V
$V_{IN(OFF)}$ (LT3752-1)				7.6		V
$V_{IN(ON/OFF)}$ Hysteresis (LT3752-1)		●	1.61	1.9	2.19	V
V_{IN} Start-Up Current (LT3752-1)	(Notes 6, 7)	●		170	265	μA
V_{IN} Quiescent Current (Housekeeping Controller Only) (LT3752)	HCOMP = 1V (Housekeeping Not Switching), HFB = 0.85V	●		4	6.2	mA
V_{IN} Quiescent Current (Housekeeping Controller Only) (LT3752-1)	HCOMP = 1V (Housekeeping Not Switching), HFB = 0.85V	●		3	4.6	mA
V_{IN} Quiescent Current (Housekeeping Controller + Forward Controller)	HCOMP = 1V (Housekeeping Not Switching), HFB = 1.35V, FB = 1.5V (Main Loop Not Switching)			7.5	9.5	mA
UVLO_ V_{SEC} Micropower Threshold (V_{SD})	$I_{VIN} < 20\mu\text{A}$	●	0.2	0.4	0.6	V
V_{IN} Shutdown Current (Micropower)	UVLO_ $V_{SEC} = 0.2\text{V}$			20	40	μA
UVLO_ V_{SEC} Threshold (V_{SYS_UV})		●	1.180	1.250	1.320	V
V_{IN} Shutdown Current (After Soft-Stop)	UVLO_ $V_{SEC} = 1\text{V}$			165	220	μA
UVLO_ V_{SEC} (ON) Current	UVLO_ $V_{SEC} = V_{SYS_UV} + 50\text{mV}$			0		μA
UVLO_ V_{SEC} (OFF) Current Hysteresis Current With One-Shot Communication Current	UVLO_ $V_{SEC} = V_{SYS_UV} - 50\text{mV}$ (Note 15)	●	4.0	5 25	6.0	μA μA
OVLO (Rising) (No Switching, Reset SS1)		●	1.220	1.250	1.280	V
OVLO (Falling) (Restart SS1)				1.215		V
OVLO Hysteresis		●	23	35	47	mV
OVLO Pin Current (Note 10)	OVLO = 0V OVLO = 1.5V (SS1 = 2.7V) OVLO = 1.5V (SS1 = 1.0V)			5 0.9 5	100	nA mA nA

Oscillator (Forward Controller: OUT, SOUT, AOUT)

Frequency: $f_{OSC} = 100\text{kHz}$	$R_T = 82.5\text{k}$		94	100	106	kHz
Frequency: $f_{OSC} = 300\text{kHz}$	$R_T = 24.9\text{k}$	●	279	300	321	kHz
Frequency: $f_{OSC} = 500\text{kHz}$	$R_T = 14\text{k}$		470	500	530	kHz
f_{OSC} Line Regulation	$R_T = 24.9\text{k}$ $6.5\text{V} < V_{IN} < 100\text{V}$ (LT3752) $10.5\text{V} < V_{IN} < 16\text{V}$ (LT3752-1)			0.05 0.05	0.1 0.1	%/V %/V
Frequency and D_{VSEC} Foldback Ratio (LT3752) (Fold)	SS1 = $V_{SSACT} + 25\text{mV}$, SS2 = 2.7V			4		
Frequency and D_{VSEC} Foldback Ratio (LT3752-1) (Fold)	SS1 = $V_{SS1ACT} + 25\text{mV}$, SS2 = 2.7V			2		
SYNC Input High Threshold	(Note 4)	●		1.2	1.8	V
SYNC Input Low Threshold	(Note 4)	●	0.6	1.025		V
SYNC Pin Current	SYNC = 6V			75		μA
SYNC Frequency/Programmed f_{OSC}			1.0		1.25	kHz/kHz

Linear Regulator (INTV_{CC}) (LT3752)

INTV _{CC} Regulation Voltage			6.6	7	7.2	V
Dropout ($V_{IN} - \text{INTV}_{CC}$)	$V_{IN} = 6.5\text{V}$, $I_{INTVCC} = 10\text{mA}$			0.8		V
INTV _{CC} UVLO(+)	(Start Switching)			4.75	5	V

3752fb

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 12\text{V}$, $UVLO_V_{SEC} = 2.5\text{V}$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTV _{CC} UVLO(–)	(Stop Switching)		4.6	4.85	V
INTV _{CC} UVLO Hysteresis		0.075	0.15	0.24	V
Linear Regulator (INTV_{CC}) (LT3752-1)					
INTV _{CC} Regulation Voltage		9.4	10	10.4	V
Dropout ($V_{IN} - \text{INTV}_{CC}$)	$V_{IN} = 8.75\text{V}$, $I_{\text{INTV}_{CC}} = 10\text{mA}$		0.6		V
INTV _{CC} UVLO(+)	(Start Switching)		7	7.4	V
INTV _{CC} UVLO(–)	(Stop Switching)		6.8	7.2	V
INTV _{CC} UVLO Hysteresis		0.1	0.2	0.3	V
Linear Regulator (INTV_{CC}) (LT3752/LT3752-1)					
INTV _{CC} OVLO(+)	(Stop Switching)	15.9	16.5	17.2	V
INTV _{CC} OVLO(–)	(Start Switching)	15.4	16	16.7	V
INTV _{CC} OVLO Hysteresis		0.38	0.5	0.67	V
INTV _{CC} Current Limit	INTV _{CC} = 0V	● 17	23	29	mA
	INTV _{CC} = 5.75V (LT3752)	● 35	50	60	mA
	INTV _{CC} = 8.75V (LT3752-1)	● 35	50	60	mA
Error Amplifier					
FB Reference Voltage		● 1.220	1.250	1.275	V
FB Line Reg	$6.5\text{V} < V_{IN} < 100\text{V}$ (LT3752)		0.1	0.3	mV/V
	$10.5\text{V} < V_{IN} < 16\text{V}$ (LT3752-1)		0.1	0.3	mV/V
FB Load Reg	$\text{COMP_SW} - 0.1\text{V} < \text{COMP} < \text{COMP_V}_{OH} - 0.1\text{V}$		0.1	0.3	mV/V
FB Input Bias Current	(Note 10)		50	200	nA
Open-Loop Voltage Gain			85		dB
Unity-Gain Bandwidth	(Note 8)		2.5		MHz
COMP Source Current	FB = 1V, COMP = 1.75V (Note 10)	6	11		mA
COMP Sink Current	FB = 1.5V, COMP = 1.75V	6.5	11.5		mA
COMP Output High Clamp	FB = 1V		2.6		V
COMP Switching Threshold			1.25		V
Current Sense (Main Loop)					
I _{SENSE} Maximum Threshold	FB = 1V, OC = 0V	180	220	260	mV
COMP Current Mode Gain	$\Delta V_{\text{COMP}} / \Delta V_{\text{I}_{\text{SENSE}}}$		6.1		V/V
I _{SENSE} Input Current (D = 0%)	(Note 10)		2		μA
I _{SENSE} Input Current (D = 80%)	(Note 10)		33		μA
I _{SENSE} Input Current	FB = 1.5V (COMP Open) (Note 10)		20	30	μA
	FB = 1V (COMP Open) (Note 10)		90	135	μA
OC Overcurrent Threshold		● 82.5	96	107.5	mV
OC Input Current			200	500	nA
AOUT Driver (Active Clamp Switch Control) (LT3752 External PMOS; LT3752-1 External NMOS)					
AOUT Rise Time	$C_L = 1\text{nF}$ (Note 5), INTV _{CC} = 12V		23		ns
AOUT Fall Time	$C_L = 1\text{nF}$ (Note 5), INTV _{CC} = 12V		19		ns
AOUT Low Level			0.1		V
AOUT High Level	INTV _{CC} = 12V	11.9			V
AOUT High Level in Shutdown (LT3752)	UVLO_V _{SEC} = 0V, INTV _{CC} = 8V, I _{AOUT} = 1mA Out of the Pin	7.8			V
AOUT Low Level in Shutdown (LT3752-1)	UVLO_V _{SEC} = 0V, INTV _{CC} = 12V, I _{AOUT} = 1mA Into the Pin		0.25		V

LT3752/LT3752-1

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 12\text{V}$, $UVLO_V_{SEC} = 2.5\text{V}$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AOUT Edge to OUT (Rise): (t_{AO})	$C_{SOUT} = 1\text{nF}$, $C_{OUT} = 3.3\text{nF}$, $INTV_{CC} = 12\text{V}$ $R_{TAO} = 44.2\text{k}$ $R_{TAO} = 73.2\text{k}$ (Note 11)	168 253	218 328	268 403	ns ns
OUT (Fall) to AOUT Edge: (t_{OA})	$C_{SOUT} = 1\text{nF}$, $C_{OUT} = 3.3\text{nF}$, $INTV_{CC} = 12\text{V}$ $R_{TAO} = 44.2\text{k}$ $R_{TAO} = 73.2\text{k}$ (Note 12)	150 214	196 295	250 376	ns ns
SOUT Driver (Synchronous Rectification Control)					
SOUT Rise Time	$C_{OUT} = 1\text{nF}$, $INTV_{CC} = 12\text{V}$ (Note 5)		21		ns
SOUT Fall Time	$C_{OUT} = 1\text{nF}$, $INTV_{CC} = 12\text{V}$ (Note 5)		19		ns
SOUT Low Level			0.1		V
SOUT High Level	$INTV_{CC} = 12\text{V}$	11.9			V
SOUT High Level in Shutdown	$UVLO_V_{SEC} = 0\text{V}$, $INTV_{CC} = 8\text{V}$, $I_{SOUT} = 1\text{mA}$ Out of the Pin	7.8			V
AOUT Edge to SOUT (Fall): (t_{AS})	$C_{AOUT} = C_{SOUT} = 1\text{nF}$, $INTV_{CC} = 12\text{V}$ $R_{TAS} = 44.2\text{k}$ (Note 13) $R_{TAS} = 73.2\text{k}$	168 253	218 328	268 403	ns ns
SOUT (Fall) to OUT (Rise): ($t_{SO} = t_{AO} - t_{AS}$)	$C_{SOUT} = 1\text{nF}$, $C_{OUT} = 3.3\text{nF}$, $INTV_{CC} = 12\text{V}$ $R_{TAO} = 73.2\text{k}$, $R_{TAS} = 44.2\text{k}$ (Notes 11, 13) $R_{TAO} = 44.2\text{k}$, $R_{TAS} = 73.2\text{k}$	70 -70	110 -110	132 -132	ns ns
OUT (Fall) to SOUT (Rise): (t_{OS})	$C_{SOUT} = 1\text{nF}$, $C_{OUT} = 3.3\text{nF}$, $INTV_{CC} = 12\text{V}$ $R_{TOS} = 14.7\text{k}$ $R_{TOS} = 44.2\text{k}$ (Note 14)	52 102	68 133	84 164	ns ns
OUT Driver (Main Power Switch Control)					
OUT Rise Time	$C_{OUT} = 3.3\text{nF}$, $INTV_{CC} = 12\text{V}$ (Note 5)		19		ns
OUT Fall Time	$C_{OUT} = 3.3\text{nF}$, $INTV_{CC} = 12\text{V}$ (Note 5)		20		ns
OUT Low Level			0.1		V
OUT High Level	$INTV_{CC} = 12\text{V}$	11.9			V
OUT Low Level in Shutdown	$UVLO_V_{SEC} = 0\text{V}$, $INTV_{CC} = 8\text{V}$, $I_{OUT} = 1\text{mA}$ Into the Pin		0.25		V
OUT (Volt-Sec) Max Duty Cycle Clamp D_{VSEC} (1 • System Input (Min)) $\times 100$ D_{VSEC} (2 • System Input (Min)) $\times 100$ D_{VSEC} (4 • System Input (Min)) $\times 100$	$R_T = 24.9\text{k}$, $R_{IVSEC} = 51.1\text{k}$, $FB = 1\text{V}$, $SS1 = 2.7\text{V}$ $UVLO_V_{SEC} = 1.25\text{V}$ $UVLO_V_{SEC} = 2.50\text{V}$ $UVLO_V_{SEC} = 5.00\text{V}$	68.5 34.3 17.5	72.5 36.5 18.6	76.2 38.7 19.7	% % %
OUT Minimum ON Time	$C_{OUT} = 3.3\text{nF}$, $INTV_{CC} = 12\text{V}$ (Note 9) $R_{TBLNK} = 14.7\text{k}$ $R_{TBLNK} = 73.2\text{k}$ (Note 16)		325 454		ns ns
SS1 Pin (Soft-Start: Frequency and D_{VSEC}) (Soft-Stop: COMP Pin, Frequency and D_{VSEC})					
SS1 Reset Threshold ($V_{SS1(RTH)}$)			150		mV
SS1 Active Threshold ($V_{SS1(ACT)}$)	(Allow Switching)		1.25		V
SS1 Charge Current (Soft-Start)	$SS1 = 1.5\text{V}$ (Note 10)	7	11.5	16	μA
SS1 Discharge Current (Soft-Stop)	$SS1 = 1\text{V}$, $UVLO_V_{SEC} = V_{SYS_UV} - 50\text{mV}$	6.4	10.5	14.6	μA
SS1 Discharge Current (Hard Stop) OC > OC Threshold $INTV_{CC} < INTV_{CC} UVLO(-)$ $OVLO > OVLO(+)$	$SS1 = 1\text{V}$		0.9 0.9 0.9		mA mA mA
SS2 Pin (Soft-Start: Comp Pin)					
SS2 Discharge Current	$SS1 < V_{SS(ACT)}$, $SS2 = 2.5\text{V}$		2.8		mA
SS2 Charge Current	$SS1 > V_{SS(ACT)}$, $SS2 = 1.5\text{V}$	11	21	28	μA

3752fb

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 12\text{V}$, $UVLO_V_{SEC} = 2.5\text{V}$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (Housekeeping Controller)					
HFB Reference Voltage		0.90	1.000	1.10	V
HFB Line Reg	$6.5\text{V} < V_{IN} < 100\text{V}$ (LT3752) $10.5\text{V} < V_{IN} < 16\text{V}$ (LT3752-1)		0.1 0.1		mV/V mV/V
HFB Load Reg	$HCOMP\ V_{SW} - 0.1\text{V} < HCOMP < HCOMP\ V_{OH} - 0.1\text{V}$		-6		mV/V
HFB Input Bias Current	HFB = 1.1V (Note 10)		85	170	nA
Transconductance	$\Delta I_{HCOMP} \pm 5\mu\text{A}$		250		μS
Voltage Gain			175		V/V
Power Good(+) (HFB Level)			0.96		V
Power Good(-) (HFB Level)			0.92		V
HFB OVLO(+)	(Disable HOUT Switching)		1.206		V
HFB OVLO(-)	(Enable Housekeeping Operation)		1.150		V
HCOMP Source Current	HCOMP = 1.75V (Note 10)	11	15	19	μA
HCOMP Sink Current	HCOMP = 1.75V	13	18	23	μA
HCOMP Output High Clamp			2.9		V
HCOMP Switching Threshold			1.28		V
Current Sense (Housekeeping Controller)					
I_{SENSE} Peak Current Threshold	HFB = 0.8V	69	79	86.5	mV
HCOMP Current Mode Gain	$\Delta V_{HCOMP}/\Delta V_{HISENSE}$		9.1		V/V
I_{SENSE} Input Current (D = 0%)	(Note 10)		2		μA
I_{SENSE} Input Current (D = 80%)			52		μA
I_{SENSE} Overcurrent Threshold		84.6	98	105.4	mV
HOUT Driver (Housekeeping Controller)					
HOUT Rise Time	$C_L = 1\text{nF}$ (Note 5), $INTV_{CC} = 12\text{V}$		13		ns
HOUT Fall Time	$C_L = 1\text{nF}$ (Note 5), $INTV_{CC} = 12\text{V}$		12		ns
HOUT Low Level			0.1		V
HOUT High Level	$INTV_{CC} = 12\text{V}$	11.9			V
LT3752		11.9			V
LT3752-1					
HOUT Low Level in Shutdown	$UVLO_V_{SEC} = 0\text{V}$, $INTV_{CC} = 12\text{V}$, $I_{HOUT} = 1\text{mA}$ Into the Pin		0.25		V
HOUT Maximum Duty Cycle	HCOMP = 2.7V, $R_T = 24.9\text{k}$	90	95		%
HOUT Minimum ON Time	$C_L = 1\text{nF}$ (Note 9), $INTV_{CC} = 12\text{V}$		350		ns
Soft-Start (HSS) (Housekeeping Controller)					
HSS (Internal) Ramp Time (t_{HSS})	$HCOMP\ SW \geq HCOMP\ V_{OH} - 0.1\text{V}$		2.2	4	ms
Oscillator (Housekeeping Controller)					
Frequency (f_{HOUT}) (f_{OSC} Folded Back) (LT3752)	HFB = 0.8V, $R_T = 24.9\text{k}$, $SS1 = 0\text{V}$	55	65	75	kHz
Frequency (f_{HOUT}) (f_{OSC} Folded Back) (LT3752-1)	HFB = 0.8V, $R_T = 24.9\text{k}$, $SS1 = 0\text{V}$	119	141	163	kHz
Frequency (f_{HOUT}) (Full-Scale f_{OSC})	HFB = 1.15V, HCOMP = 2.7V	● 279	300	321	kHz

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3752EFE/LT3752EFE-1 are guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3752IFE/LT3752IFE-1 are guaranteed to meet performance specifications from -40°C to 125°C junction temperature. The LT3752HFE/LT3752HFE-1 are guaranteed to meet performance specifications from -40°C to 150°C junction temperature. The LT3752MPFE/LT3752MPFE-1 are tested and guaranteed to meet performance specifications from -55°C to 150°C junction temperature.

Note 3: For maximum operating ambient temperature, see the Thermal Calculations section in the Applications Information section.

Note 4: SYNC minimum and maximum thresholds are guaranteed by SYNC frequency range test using a clock input with guard banded SYNC levels of 0.7V low level and 1.7V high level.

Note 5: Rise and fall times are measured between 10% and 90% of gate driver supply voltage.

Note 6: Guaranteed by correlation to static test.

Note 7: V_{IN} start-up current is measured at $V_{IN} = V_{IN(ON)} - 0.25V$ and then scaled by 1.18× to correlate to worst-case V_{IN} current required for part start-up at $V_{IN} = V_{IN(ON)}$.

Note 8: Guaranteed by design.

Note 9: ON times are measured between rising and falling edges at 50% of gate driver supply voltage.

Note 10: Current flows out of pin.

Note 11: Guaranteed by correlation to $R_{TAS} = 73.2k$ test.

Note 12: t_{OA} timing guaranteed by design based on correlation to measured t_{AO} timing.

Note 13: Guaranteed by correlation to $R_{TAO} = 44.2k$ test.

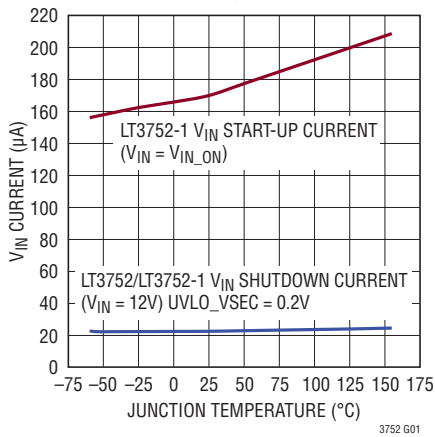
Note 14: Guaranteed by correlation to $R_{TOS} = 14.7k$ test.

Note 15: A 2μs one-shot of 20μA from the UVLO_VSEC pin allows communication between ICs to begin shutdown (useful when stacking supplies for more power (= inputs in parallel/outputs in series)). The current is tested in a static test mode. The 2μs one-shot is guaranteed by design.

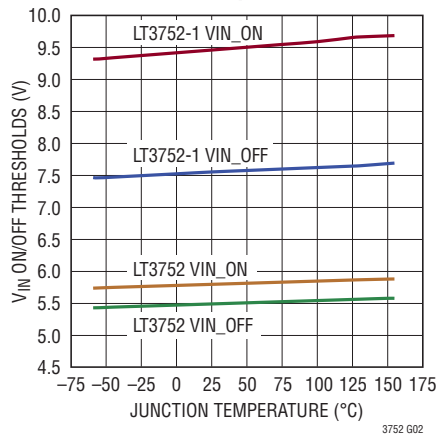
Note 16: Guaranteed by correlation to $R_{TBLNK} = 14.7k$ test.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.

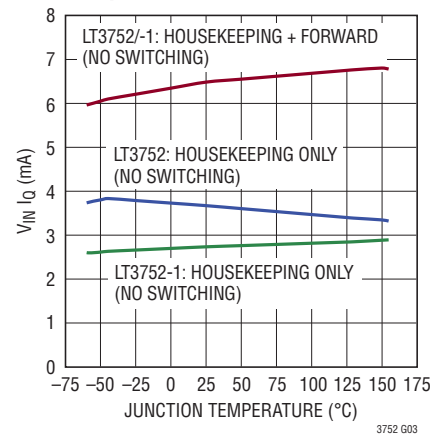
V_{IN} Start-Up and Shutdown Current vs Junction Temperature



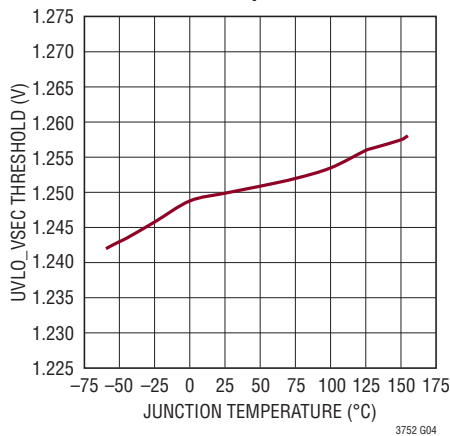
$V_{IN(ON)}$, $V_{IN(OFF)}$ Thresholds vs Junction Temperature



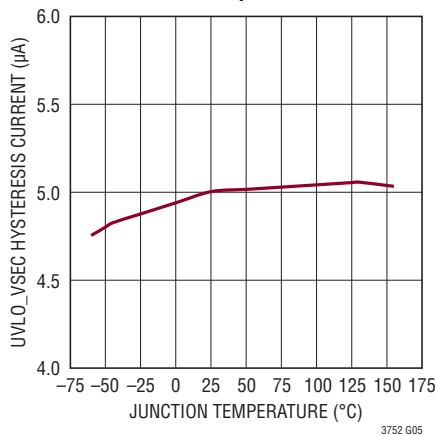
V_{IN} Quiescent Current vs Junction Temperature



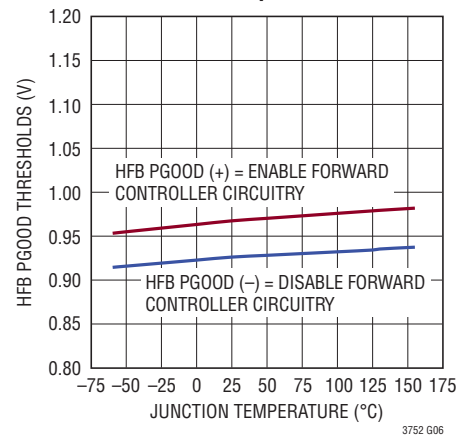
$UVLO_VSEC$ Turn-On Threshold vs Junction Temperature



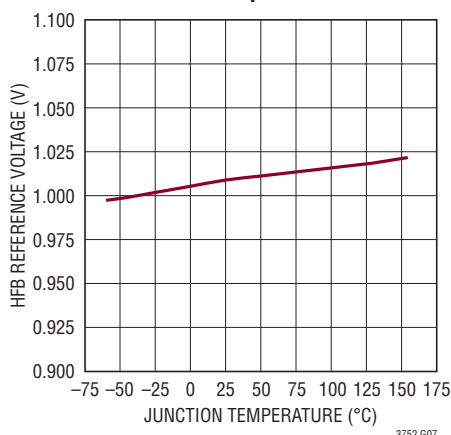
$UVLO_VSEC$ Hysteresis Current vs Junction Temperature



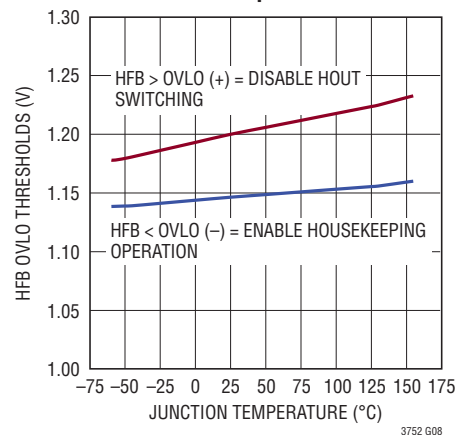
HFB PGOOD Thresholds vs Junction Temperature



HFB Reference Voltage vs Junction Temperature

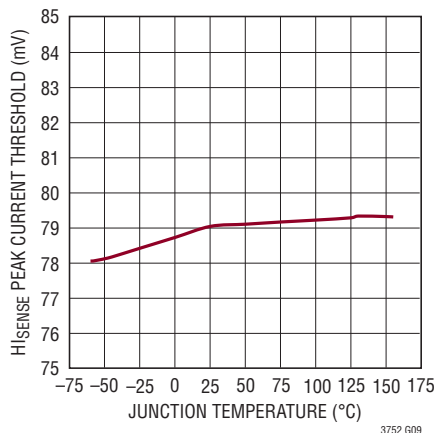


HFB OVLO Thresholds vs Junction Temperature

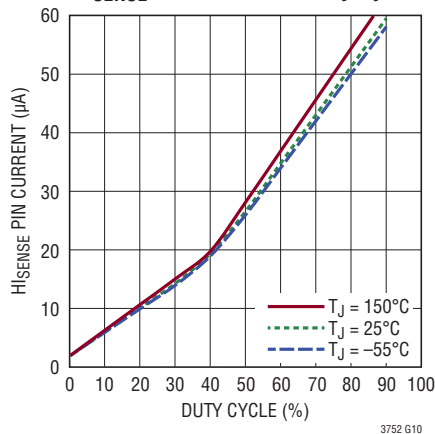


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.

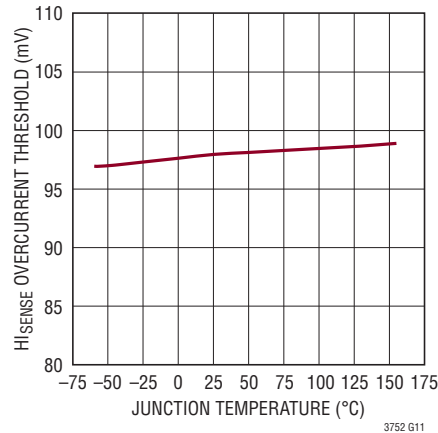
HI_{SENSE} Peak Current Threshold vs Junction Temperature



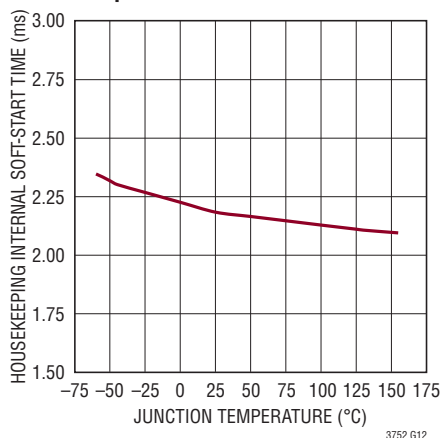
HI_{SENSE} Pin Current vs Duty Cycle



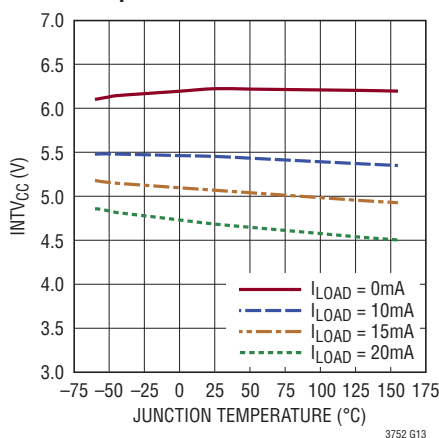
HI_{SENSE} Overcurrent (Hiccup Mode) Threshold vs Junction Temperature



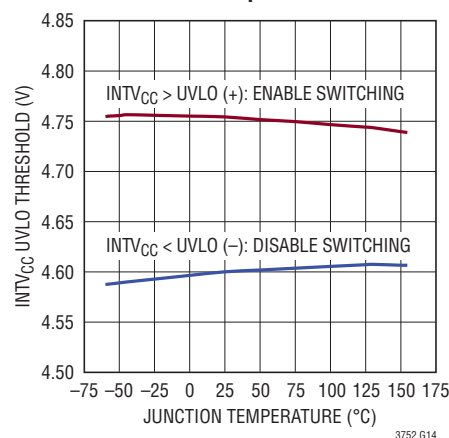
Housekeeping Internal Soft-Start Time (HSS) vs Junction Temperature



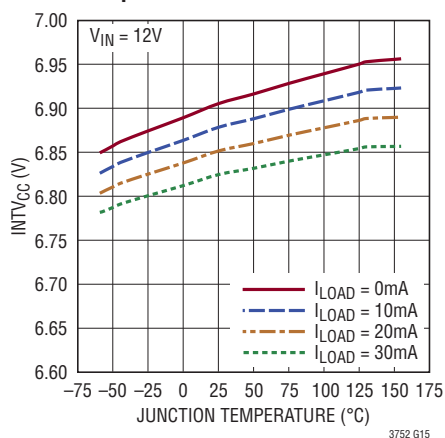
LT3752: INTV_{CC} in Dropout at V_{IN} = 6.5V vs Current, Junction Temperature



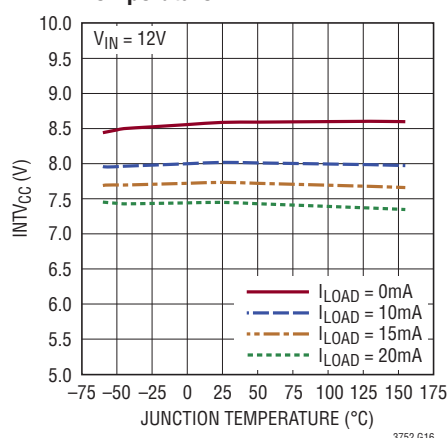
LT3752: INTV_{CC} UVLO Thresholds vs Junction Temperature



LT3752: INTV_{CC} Regulation Voltage vs Current, Junction Temperature

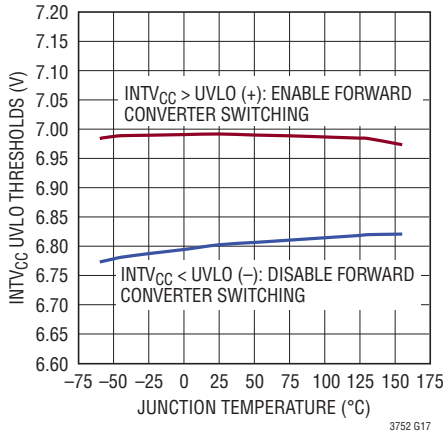


LT3752-1: INTV_{CC} in Dropout at V_{IN} = 8.75V vs Current, Junction Temperature

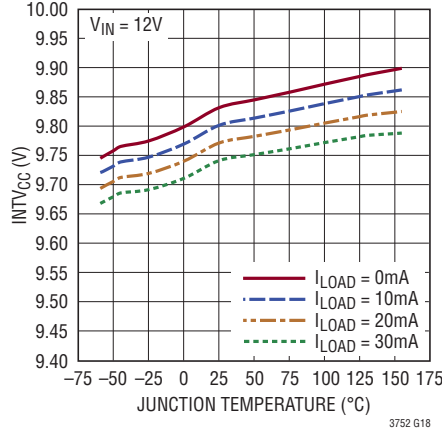


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.

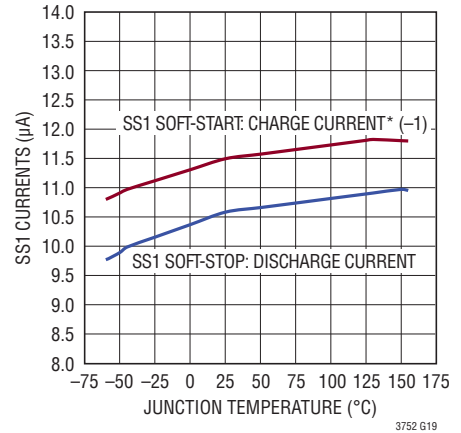
LT3752-1: INTV_{CC} UVLO Thresholds vs Junction Temperature



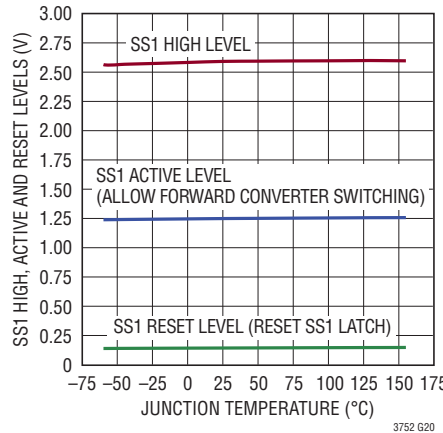
LT3752-1: INTV_{CC} Regulation Voltage vs Current, Junction Temperature



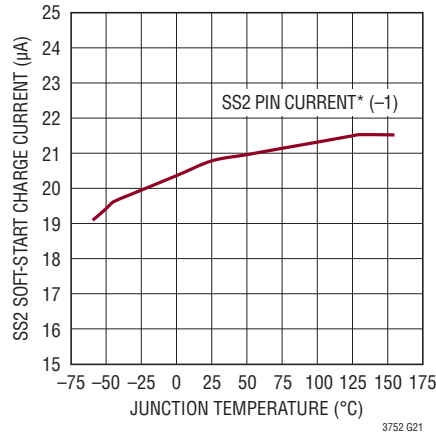
SS1 Soft-Start/Soft-Stop Pin Currents vs Junction Temperature



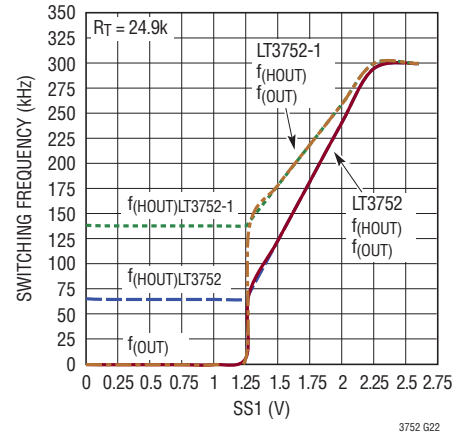
SS1 High, Active and Reset Levels vs Junction Temperature



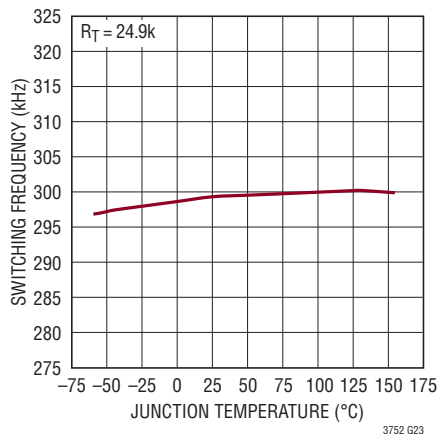
SS2 Soft-Start Charge Current vs Junction Temperature



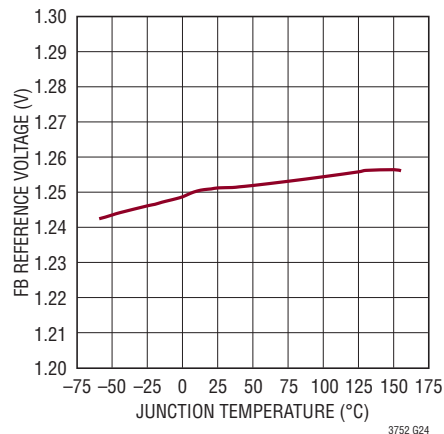
Switching Frequency vs SS1 Pin Voltage



Switching Frequency vs Junction Temperature

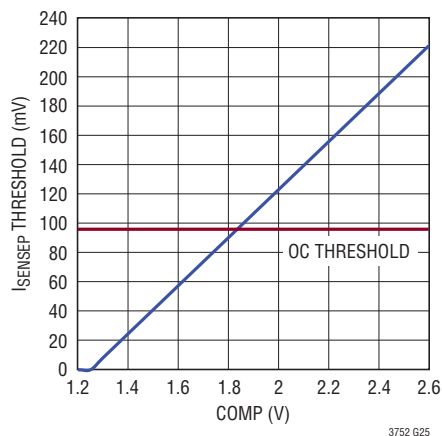


FB Reference Voltage vs Junction Temperature

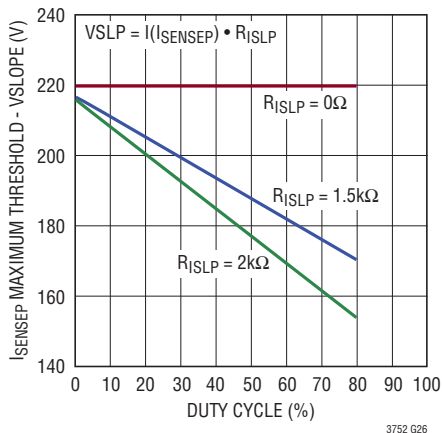


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.

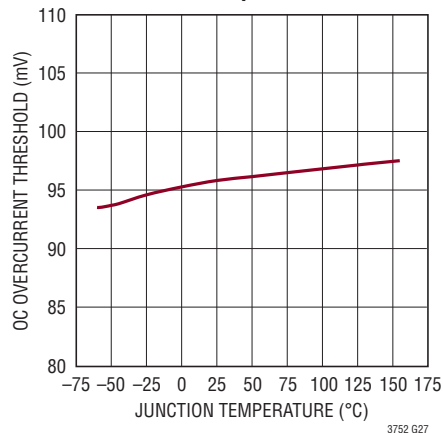
I_{SENSE} Maximum Threshold vs COMP



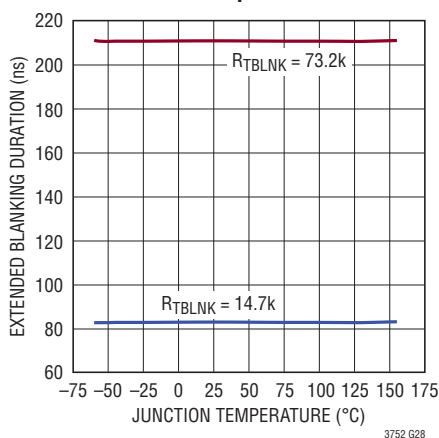
I_{SENSE} Maximum Threshold – VSLP vs Duty Cycle (Programming Slope Compensation)



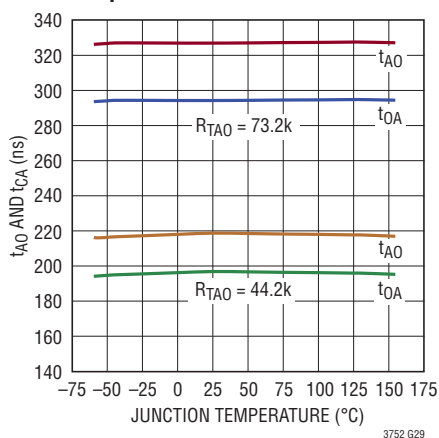
OC Overcurrent (Hiccup Mode) Threshold vs Junction Temperature



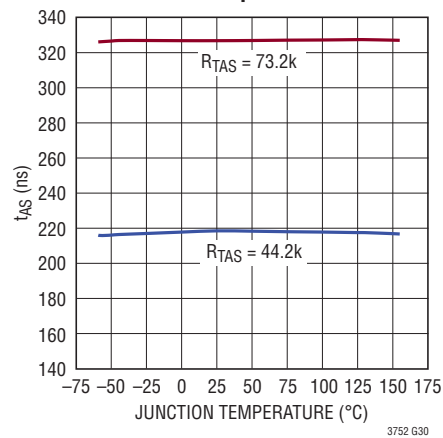
Extended Blanking Duration vs Junction Temperature



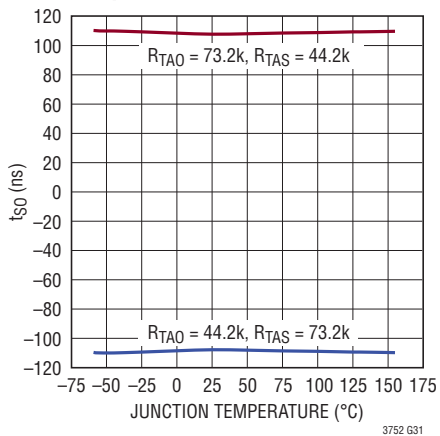
AOUT to OUT Delay (t_{AO}) and OUT to AOUT Delay (t_{OA}) vs Junction Temperature



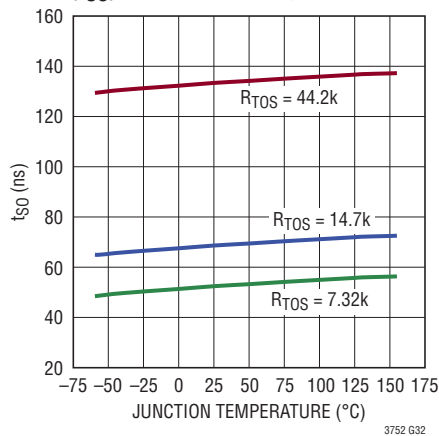
AOUT to SOUT Delay (t_{AS}) vs Junction Temperature



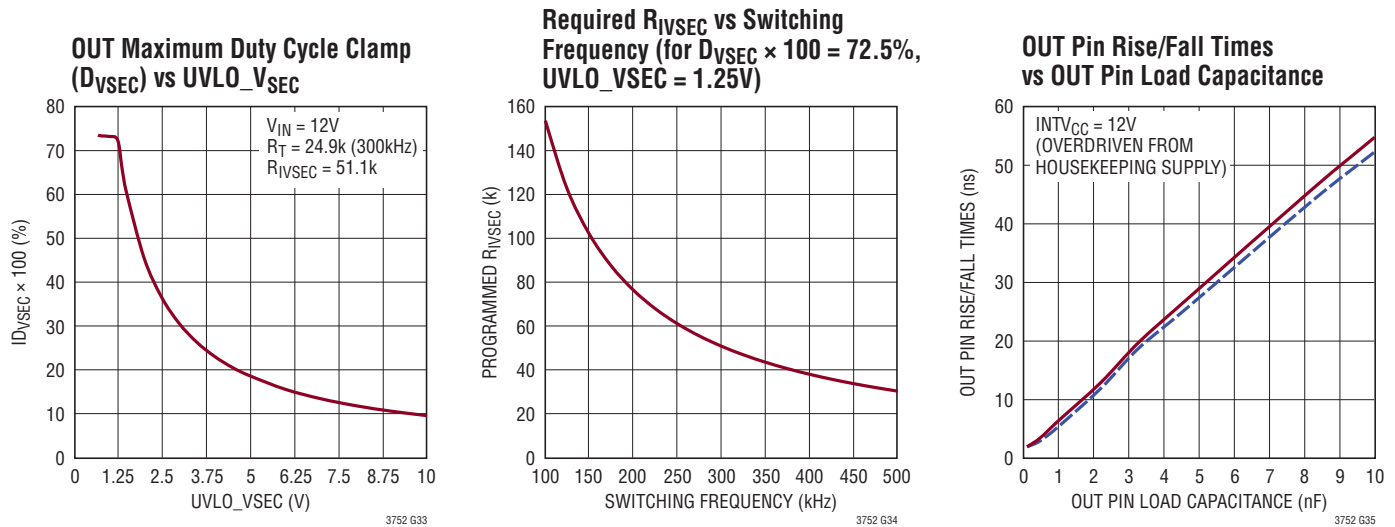
SOUT (Fall) to OUT (Rise) Delay ($t_{SO} = t_{AO} - t_{AS}$) vs Junction Temperature



OUT (Fall) to SOUT (Rise) Delay (t_{OS}) vs Junction Temperature



TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.



PIN FUNCTIONS

HFB (Pin 1): Housekeeping Supply Error Amplifier Inverting Input.

HCOMP (Pin 2): Housekeeping Supply Error Amplifier Output and Compensation Pin.

RT (Pin 3): A resistor to ground programs switching frequency.

FB (Pin 4): Error Amplifier Inverting Input.

COMP (Pin 5): Error Amplifier Output. Allows various compensation networks for nonisolated applications.

SYNC (Pin 6): Allows synchronization of internal oscillator to an external clock. f_{SYNC} equal to f_{OSC} allowed.

SS1 (Pin 7): Capacitor controls soft-start/stop of switching frequency and volt-second clamp. During soft-stop it also controls the COMP pin.

IVSEC (Pin 8): Resistor Programs OUT Pin Maximum Duty Cycle Clamp (D_{VSEC}). This clamp moves inversely proportional to system input voltage to provide a volt-second clamp.

UVLO_VSEC (Pin 9): A resistor divider from system input allows switch maximum duty cycle to vary inversely proportional with system input. This volt-second clamp prevents transformer saturation for duty cycles above

50%. Resistor divider ratio programs undervoltage lockout (UVLO) threshold. A $5\mu\text{A}$ pin current hysteresis allows programming of UVLO hysteresis. Pin below 0.4V reduces V_{IN} currents to microamps.

OVLO (Pin 10): A resistor divider from system input programs overvoltage lockout (OVLO) threshold. Fixed hysteresis included.

TAO (Pin 11): A resistor programs nonoverlap timing between AOUT rise and OUT rise control signals.

TAS (Pin 12): Resistors at T_{AO} and T_{AS} define delay between SOUT fall and OUT rise ($= t_{AO} - t_{AS}$).

TOS (Pin 13): Resistor programs delay between OUT fall and SOUT rise.

TBLNK (Pin 14): Resistor programs extended blanking of I_{SENSEP} and OC signals during MOSFET turn-on.

NC (Pins 15, 16, 37): No Connect Pins. These pins are not connected inside the IC. These pins should be left open.

SS2 (Pin 17): Capacitor controls soft-start of COMP pin. Alternatively can connect to OPTO to communicate start of switching to secondary side. If unused, leave the pin open.

GND (Pin 18): Analog Signal Ground. Electrical connection exists inside the IC to the exposed pad (Pin 39).

PIN FUNCTIONS

PGND (Pins 19, 38, 39): The Power Grounds for the IC. The package has an exposed pad (Pin 39) underneath the IC which is the best path for heat out of the package. Pin 39 should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT3752/LT3752-1.

ISENSE (Pin 20): Negative input for the current sense comparator. Kelvin connect to the sense resistor in the source of the power MOSFET.

ISENSEP (Pin 21): Positive input for the current sense comparator. Kelvin connect to the sense resistor in the source of the power MOSFET. A resistor in series with ISENSEP programs slope compensation.

OC (Pin 22): An accurate 96mV threshold, independent of duty cycle, for detection of primary side MOSFET over-current and trigger of hiccup mode. Connect directly to sense resistor in the source of the primary side MOSFET.

Missing Pins 23, 25, 27, 29, 31, 33, 35: Pins removed for high voltage spacings and improved reliability.

OUT (Pin 24): Drives the gate of an N-channel MOSFET between 0V and INTV_{CC}. Active pull-off exists in shutdown.

INTV_{CC} (Pin 26): A linear regulator supply generated from V_{IN}. LT3752 supplies 7V for AOUT, SOUT, OUT and HOUT gate drivers. LT3752-1 supplies 10V for AOUT, SOUT, and OUT gate drivers (HOUT supplied from V_{IN}). INTV_{CC} must be bypassed with a 4.7μF capacitor to power ground. Can be externally driven by the housekeeping supply to remove power from within the IC.

V_{IN} (Pin 28): Input Supply Pin. Bypass with 1μF to ground.

SOUT (Pin 30): Sync signal for secondary side synchronous rectifier controller.

AOUT (Pin 32): Control signal for external active clamp switch. (P-channel LT3752, N-channel LT3752-1).

HOUT (Pin 34): Drives the gate of an N-channel MOSFET used for the housekeeping supply. Active pull-off exists in shutdown.

HI_{SENSE} (Pin 36): Current sense input for the house keeping supply. Connect to sense resistor in the source of the power MOSFET. A resistor in series with HI_{SENSE} programs slope compensation.

TIMING DIAGRAMS

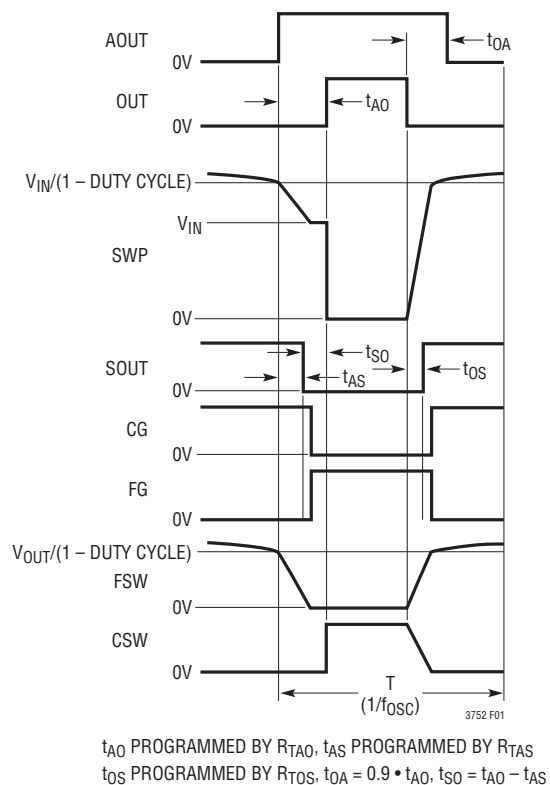


Figure 1. LT3752 Timing Diagram
(LT3752-1 Inverts AOUT Phase for N-Channel Control)

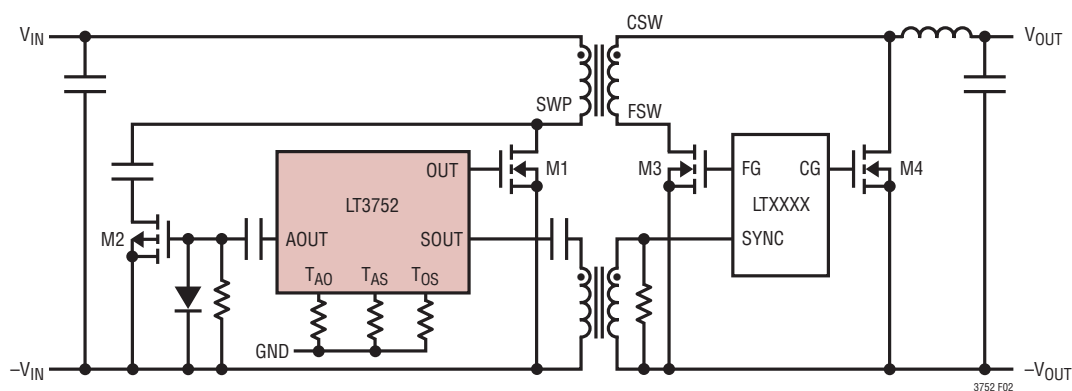


Figure 2. Timing Reference Circuit

TIMING DIAGRAMS

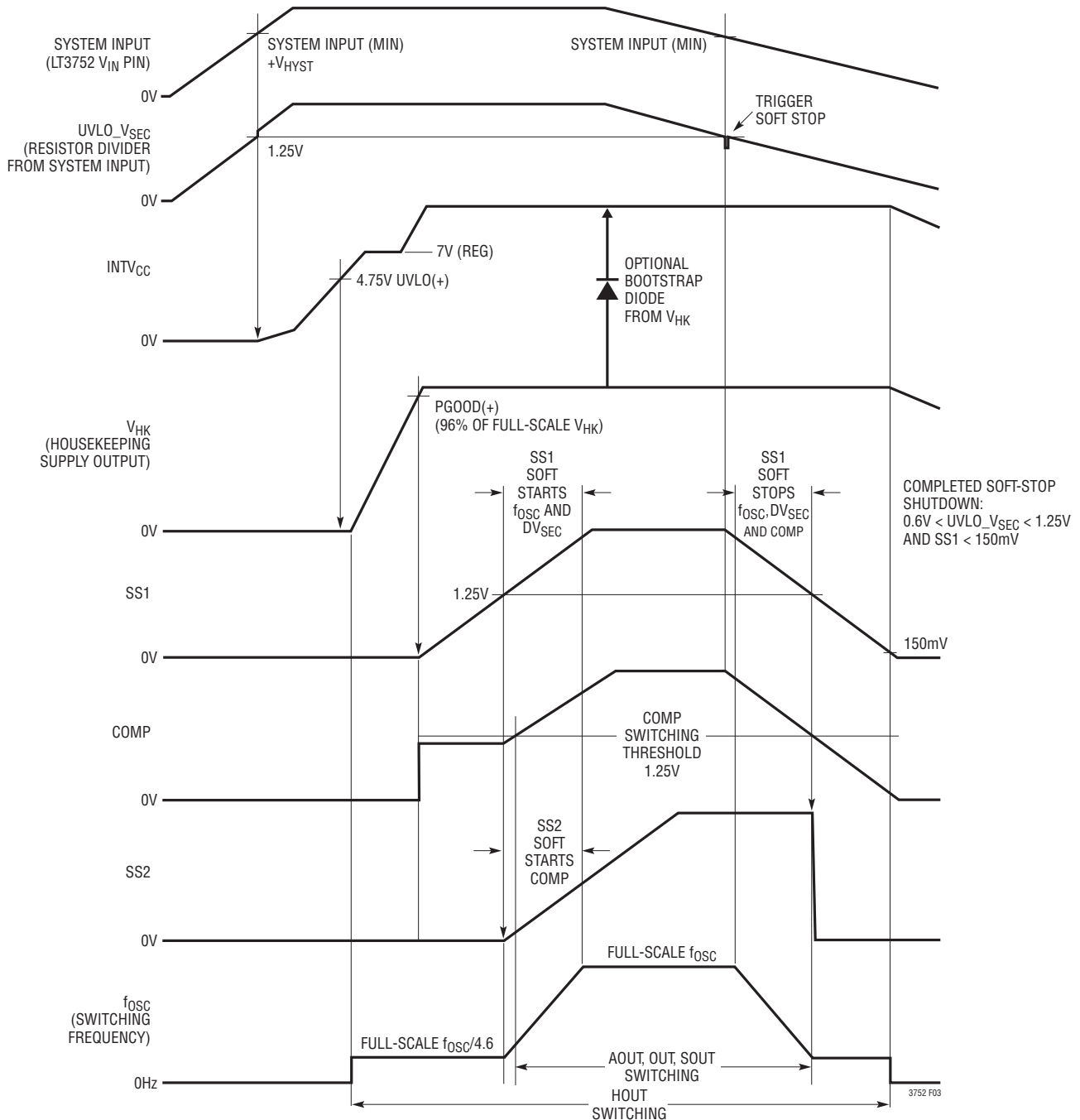


Figure 3. LT3752 Start-Up and Shutdown Timing Diagram

TIMING DIAGRAMS

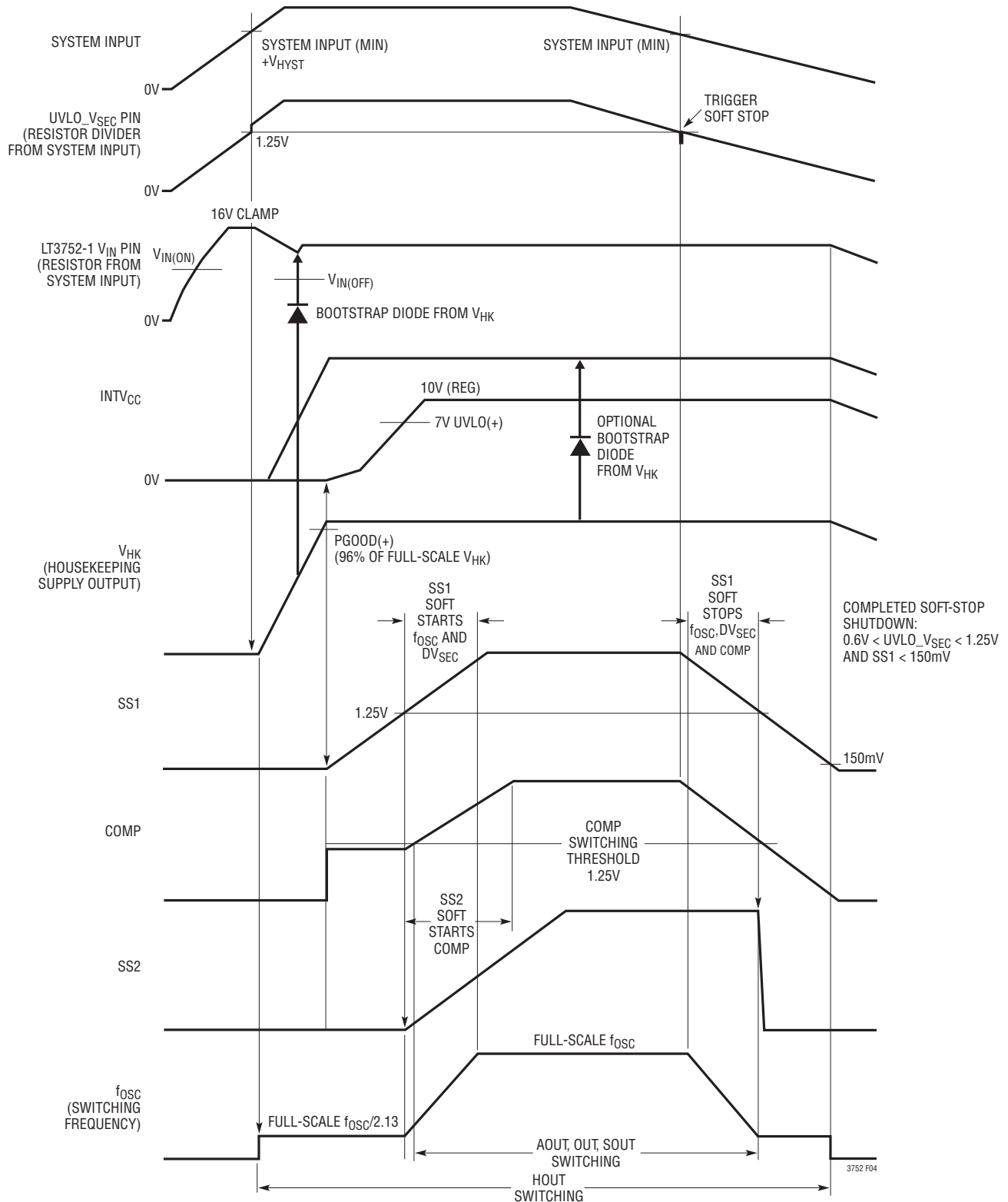


Figure 4. LT3752-1 Start-Up and Shutdown Timing Diagram

OPERATION

Introduction

The LT3752/LT3752-1 are primary side, current mode, PWM controllers optimized for use in a synchronous forward converter with active clamp reset. Combined with an integrated housekeeping controller, each IC provides a compact, versatile, and highly efficient solution. The LT3752 allows V_{IN} pin operation between 6.5V and 100V. For applications with system input voltages greater than 100V, the LT3752-1 allows RC start-up from input voltage levels limited only by external components. The LT3752 and LT3752-1 based forward converters are targeted for power levels up to 400W and are not intended for battery charger applications. For higher power levels the converter outputs can be stacked in series. Connecting UVLO_VSEC pins, OVLO pins, SS1 pins and SS2 pins together allows blocks to react simultaneously to all fault modes and conditions.

Each IC contains an accurate programmable volt-second clamp. When set above the natural duty cycle of the converter, it provides a duty cycle guardrail to limit primary switch reset voltage and prevent transformer saturation during load transients. The accuracy and excellent line regulation of the volt-second clamp provides V_{OUT} regulation for open-loop conditions such as no opto-coupler, reference or error amplifier on the secondary side.

For applications not requiring isolation but requiring high step-down ratios, each IC contains a voltage error amplifier to allow a very simple nonisolated, fully regulated synchronous forward converter.

The integrated housekeeping controller reduces the complexity and size of the main power transformer by avoiding the need for extra windings to create bias supplies. Secondary side ICs no longer require start-up circuitry and can operate even when output voltage is 0V.

A range of protection features include programmable overcurrent (OC) hiccup mode, programmable system input undervoltage lockout (UVLO), programmable system input overvoltage lockout (OVLO) and built-in thermal shutdown. Programmable slope compensation and switching frequency allow the use of a wide range of output inductor values and transformer sizes.

LT3752 Part Start-Up

LT3752 start-up is best described by referring to the Block Diagram and to the start-up waveforms in Figure 3. For part start-up, system input voltage must be high enough to drive the UVLO_VSEC pin above 1.25V and the V_{IN} pin must be greater than 6.5V. An internal linear regulator is activated and provides a 7V $INTV_{CC}$ supply for all gate drivers. The housekeeping controller starts up before the forward controller. An internal soft-start (HSS) ramps the housekeeping HCOMP pin to allow switching at the gate driver output HOUT to drive an external N-channel MOSFET. The housekeeping controller output voltage V_{HK} is regulated when the HFB pin reaches 1.0V. V_{HK} can be used to override $INTV_{CC}$ to reduce power in the part, increase efficiency and to optimize the $INTV_{CC}$ level. During start-up the housekeeping controller switches at the programmed switching frequency (f_{OSC}) folded back by 1/4.6. The SS1 pin of the forward controller is allowed to start charging when V_{HK} reaches 96% of its target value (PGOOD). When SS1 reaches 1.25V, the SS2 pin begins to charge, controlling COMP pin rise and the soft-start of output inductor peak current. The SS1 pin independently soft starts switching frequency and a volt-second clamp. As SS1 charges towards 2.6V the switching frequencies of both controllers remain equal, synchronized and soft started towards full-scale f_{OSC} .

If secondary side control already exists for soft starting the converter output voltage then the SS2 pin can still be used to control initial inductor peak current rise. Simply programming the primary side SS2 soft-start faster than the secondary side allows the secondary side to take over. If SS2 is not needed for soft-start control, its pull-down strength and voltage rating also allow it to drive the input of an opto-coupler connected to $INTV_{CC}$. This allows the option of communicating to the secondary side that switching has begun.

LT3752-1 Part Start-Up

The LT3752-1 start-up of housekeeping supply and forward converter are similar to the LT3752 except for a small change in architecture and V_{IN} pin level. LT3752-1 start-up is best described by referring to the Block Diagram and to

OPERATION

the start-up waveforms in Figure 4. The LT3752-1 starts up by using a high valued resistor from system input to charge up the input capacitor at the V_{IN} pin. If system input is already high enough to generate $UVLO_V_{SEC}$ above 1.25V, then the part turns on once V_{IN} pin charges past $V_{IN(ON)}$ (9.5V). If system input is not high enough to generate $UVLO_V_{SEC}$ above 1.25V, the V_{IN} pin charges towards system input until it reaches an internal 16V, 8mA clamp. The part turns on when system input becomes high enough to generate $UVLO_V_{SEC}$ above 1.25V. As the supply current of the part discharges the V_{IN} capacitor a bootstrap supply must be generated to prevent V_{IN} pin from falling below $V_{IN(OFF)}$ (7.6V).

The LT3752-1 uses the housekeeping controller to provide the bootstrap bias to the V_{IN} pin during RC start-up instead of waiting for the forward converter to also start. This method is more efficient, requires a smaller V_{IN} input capacitor

and avoids the need for an auxiliary winding in the main transformer. The part's low start-up current at the V_{IN} pin allows the use of a large start-up resistor to minimize power loss from system input. The V_{IN} capacitor value required for proper start-up is minimized by providing a large $V_{IN(ON)}-V_{IN(OFF)}$ hysteresis, a low $V_{IN} I_Q$ and a fast start-up time for the housekeeping controller. In contrast to the LT3752, the LT3752-1 housekeeping gate driver (HOUT) runs from the V_{IN} pin instead of $INTV_{CC}$. This avoids having to use current from the V_{IN} pin to charge the $INTV_{CC}$ capacitor during initial start-up. This means the regulated 10V $INTV_{CC}$ on the LT3752-1 does not wake up until the housekeeping supply is valid. Start-up from this point is similar to the LT3752. The housekeeping supply and forward converter switch together with a soft-started frequency and volt-second clamp. The forward converter peak inductor current is also soft started similar to the LT3752.

APPLICATIONS INFORMATION

Programming System Input Undervoltage Lockout (UVLO) Threshold and Hysteresis

The LT3752/LT3752-1 have an accurate 1.25V shutdown threshold at the UVLO_V_{SEC} pin. This threshold can be used in conjunction with an external resistor divider to define the falling undervoltage lockout threshold (UVLO(-)) for the converter's system input voltage (V_S) (Figure 5). A pin hysteresis current of 5μA allows programming of the UVLO(+) threshold.

$$V_S \text{ (UVLO(-)) [begin SOFT-STOP then shut down]} \\ = 1.25 \left[1 + \left(\frac{R1}{R2 + R3} \right) \right]$$

$$V_S \text{ (UVLO(+)) [begin SOFT-START]} \\ = V_S \text{ (UVLO(-))} + (5\mu\text{A} \cdot R1)$$

It is important to note that the part enters soft-stop when the UVLO_V_{SEC} pin falls back below 1.25V. During soft-stop the converter continues to switch as it folds back switching frequency, volt-second clamp and COMP pin voltage. See Soft-Stop in the Applications Information section. When the SS2 pin is finally discharged below its 150mV reset threshold both the housekeeping supply and forward converter are shut down.

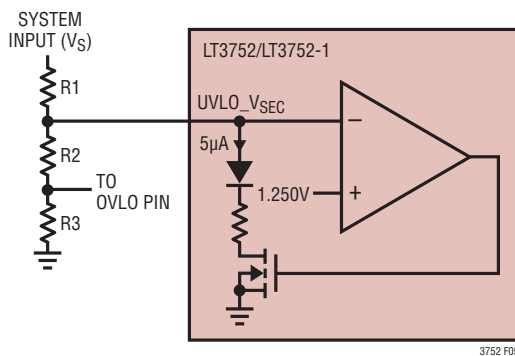


Figure 5. Programming Undervoltage Lockout (UVLO)

Soft-Stop Shutdown

Soft-stop shutdown (similar to system undervoltage) can be commanded by an external control signal. A MOSFET with a diode (or diodes) in series with the drain should be

used to pull down the UVLO_V_{SEC} pin below 1.25V but not below the micropower shutdown threshold of 0.6V(max). Typical V_{IN} quiescent current after soft-stop is 165μA.

Micropower Shutdown

If a micropower shutdown is required using an external control signal, an open-drain transistor can be directly connected to the UVLO_V_{SEC} pin. The LT3752/LT3752-1 have a micropower shutdown threshold of typically 0.4V at the UVLO_V_{SEC} pin. V_{IN} quiescent current in micropower shutdown is 20μA.

Programming System Input Overvoltage Lockout (OVLO) Threshold

The LT3752/LT3752-1 have an accurate 1.25V overvoltage shutdown threshold at the OVLO pin. This threshold can be used in conjunction with an external resistor divider to define the rising overvoltage lockout threshold (OVLO(+)) for the converter's system input voltage (V_S) (Figure 6). When OVLO(+) is reached, the part stops switching immediately and a hard stop discharges the SS1 and SS2 pins. The falling threshold OVLO(-) is fixed internally at 1.215V and allows the part to restart in soft-start mode. A single resistor divider can be used from system input supply (V_S) to define both the undervoltage and overvoltage thresholds for the system. Minimum value for R3 is 1k. If OVLO is unused, place a 10k resistor from OVLO pin to ground.

$$V_S \text{ OVLO(+)} \text{ [stop switching; HARD STOP]}$$

$$= 1.25 \left[1 + \left(\frac{R1 + R2}{R3} \right) \right]$$

$$V_S \text{ OVLO(-)} \text{ [begin SOFT-START]}$$

$$= V_S \text{ OVLO(+)} \cdot \frac{1.215}{1.25}$$

APPLICATIONS INFORMATION

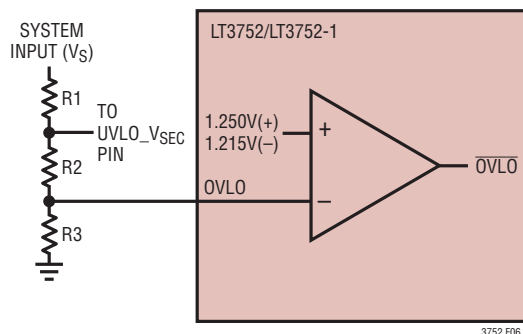


Figure 6. Programming Overvoltage Lockout (OVLO)

LT3752-1 Micropower Start-Up from High System Input Voltages

The LT3752-1 starts up from system input voltage levels limited only by external components (Figure 7). The low start-up current of the LT3752-1 allows a large start-up resistor (R_{START}) to be connected from system input voltage (V_S) to the V_{IN} pin.

When system input voltage is applied, the start-up capacitor (C_{START}) begins charging at the V_{IN} pin. Once the V_{IN} pin exceeds 9.5V (and $UVLO_V_{SEC} > 1.25V$) the housekeeping controller will start to switch and V_{IN} supply current will begin to discharge C_{START} . The C_{START} capacitor value should be chosen high enough to prevent the V_{IN} pin from falling below 7.6V before the housekeeping supply can provide a bootstrap bias to the V_{IN} pin. The LT3752-1 start-up architecture minimizes the value of C_{START} by activating only the house keeping controller for providing drive back to the V_{IN} pin. The forward controller only operates once the housekeeping supply is established. (If a bootstrap diode is used from the housekeeping supply back to $INTV_{CC}$, this only uses current from system input and not from the V_{IN} pin).

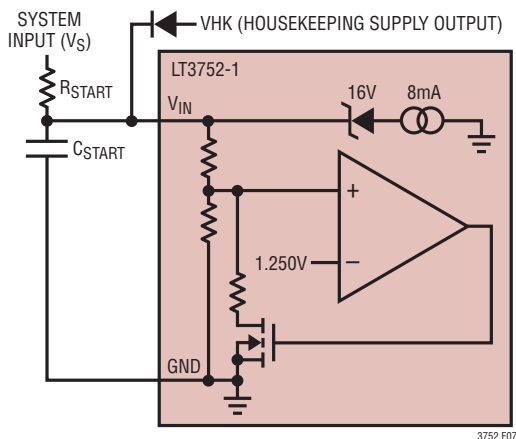


Figure 7. Micropower Start-Up from High System Input

The start-up capacitor can be calculated as:

$$C_{START(MIN)} = (I_{HKEEP} + I_{DRIVE})(MAX) \cdot \frac{t_{HSS(MAX)}}{V_{DROOP(MIN)}}$$

where:

I_{HKEEP} = Housekeeping I_Q (not switching)

$I_{DRIVE} = (f_{OSC}/2.13) \cdot Q_G$

f_{OSC} = full-scale controller switching frequency

Q_G = gate charge ($V_{GS} = V_{IN}$)(HOUT MOSFET)

t_{HSS} = housekeeping output voltage soft-start time

$V_{DROOP} = 16V(clamp) - V_{IN(OFF)}$ or $V_{IN(ONOFFHYST)}$

The start-up resistor can be calculated as:

$$R_{START(MAX)} = \frac{V_{S(MAX)} - V_{IN(ON)(MAX)}}{I_{START(MAX)} \cdot k}$$

where:

$V_{S(MAX)}$ = Maximum system input voltage

$V_{IN(ON)(MAX)}$ = Maximum V_{IN} pin turn on threshold

$I_{START(MAX)}$ = Maximum V_{IN} I_Q for part start-up

$k > 1.0$ reduces R_{START} and V_{IN} charge-up time

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Worst-case values should be used to calculate the C_{START} and R_{START} required to guarantee start-up and to turn on in the time required.

Example: (LT3752-1)

For $V_{S(MIN)} = 75V$, $V_{IN(ON)(MAX)} = 10.4V$

$I_{START(MAX)} = 265\mu A$, $I_{HKEEP(MAX)} = 4.6mA$

$Q_G = 8nC$ (at $V_{IN} = 10V$), $f_{OSC} = 150kHz$

$t_{HSS(MAX)} = 4ms$, $V_{DROOP(MIN)} = 1.61V$

$$C_{START(MIN)} = (4.6mA + 71kHz \cdot 8nC) \cdot \frac{4ms}{1.61V}$$

$$= 12.8\mu F \text{ (Choose } 14.7\mu F \text{)}$$

$$R_{START(MAX)} = \frac{75V - 10.4V}{265\mu A \cdot k} = 243k \text{ (for } k = 1.0 \text{)}$$

The $R_{START(MAX)}$ value should be chosen with higher k values until the charge-up time for C_{START} is acceptable. In most cases, C_{START} will be charged to the 16V clamp on the LT3752-1 V_{IN} pin before system input reaches its UVLO(+) threshold (Figure 4). This will allow an extra 5.6V for V_{DROOP} in the C_{START} equation, allowing a smaller C_{START} value and hence a faster start-up time.

The trade-off of lower R_{START} is greater power dissipation, given by:

$$P_{RSTART} = (V_S - V_{IN})^2 / R_{START}$$

for $R_{START} = 200k$, $V_{S(MAX)} = 150V$, $V_{IN} = 10V$ (back driven from housekeeping supply)

$$P_{RSTART} = (150 - 10)^2 / 200k = 98mW.$$

Programming Switching Frequency

The switching frequency for the housekeeping supply and the main forward converter are programmed using a resistor, R_T , connected from analog ground (Pin 18) to the RT pin. Table 1 shows typical f_{OSC} vs R_T resistor values. The value for R_T is given by:

$$R_T = 8.39 \cdot X \cdot (1 + Y)$$

where,

$$X = (10^9 / f_{OSC}) - 365$$

$$Y = (300kHz - f_{OSC}) / 10^7 \text{ (} f_{OSC} < 300kHz \text{)}$$

$$Y = (f_{OSC} - 300kHz) / 10^7 \text{ (} f_{OSC} > 300kHz \text{)}$$

Example: For $f_{OSC} = 200kHz$,

$$R_T = 8.39 \cdot 4635 \cdot (1 + 0.01) = 39.28k \text{ (choose } 39.2k \text{)}$$

The LT3752/LT3752-1 include frequency foldback at start-up (see Figures 3 and 4). In order to make sure that a SYNC input does not override frequency foldback during start-up, the SYNC function is ignored until SS1 pin reaches 2.2V. Both the housekeeping and forward controllers run synchronized to each other and in phase, with or without the SYNC input.

Table 1. R_T vs Switching Frequency (f_{OSC})

SWITCHING FREQUENCY (kHz)	R_T (k Ω)
100	82.5
150	53.6
200	39.2
250	30.9
300	24.9
350	21
400	18.2
450	15.8
500	14

Synchronizing to an External Clock

The LT3752 / LT3752-1 internal oscillator can be synchronized to an external clock at the SYNC pin. SYNC pin high level should exceed 1.8V for at least 100ns and SYNC pin low level should fall below 0.6V for at least 100ns. The SYNC pin frequency should be set equal to or higher than the typical frequency programmed by the RT pin. An f_{SYNC}/f_{OSC} ratio of x ($1.0 < x < 1.25$) will reduce the externally programmed slope compensation by a factor of $1.2x$. If required, the external resistor R_{ISLP} can be reprogrammed higher by a factor of $1.2x$. (see Current Sensing and Programmable Slope Compensation).

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The part injection locks the internal oscillator to every rising edge of the SYNC pin. If the SYNC input is removed at any time during normal operation the part will simply change switching frequency back to the oscillator frequency programmed by the R_T resistor. This injection lock method avoids the possible issues from a PLL method which can potentially cause a large drop in frequency if SYNC input is removed.

During soft-start the SYNC input is ignored until SS1 exceeds 2.2V. During soft-stop the SYNC input is completely ignored. If the SYNC input is to be used, recall that the programmable duty cycle clamp D_{VSEC} is dependent on the switching frequency of the part (see section Programming Duty Cycle Clamp). R_{IVSEC} should be reprogrammed by $1/x$ for an f_{SYNC}/f_{OSC} ratio of x .

INTV_{CC} Regulator Bypassing and Operation

The INTV_{CC} pin is the output of an internal linear regulator driven from V_{IN} and provides the supply for onboard gate drivers. The LT3752 INTV_{CC} provides a regulated 7V supply for gate drivers AOUT, SOUT, OUT and HOUT. The LT3752-1 INTV_{CC} provides a regulated 10V supply for gate drivers AOUT, SOUT and OUT. INTV_{CC} should be bypassed with a 4.7μF low ESR, X7R or X5R ceramic capacitor to power ground to ensure stability and to provide enough charge for the gate drivers.

The INTV_{CC} regulator has a minimum 35mA output current limit. This current limit should be considered when choosing the switching frequency and capacitance loading on each gate driver. Average current load on the INTV_{CC} pin for a single gate driver driving an external MOSFET is given as :

$$I_{INTVCC} = f_{OSC} \cdot Q_G$$

where:

f_{OSC} = controller switching frequency

Q_G = gate charge ($V_{GS} = INTV_{CC}$)

While the INTV_{CC} 50mA output current limit is sufficient for LT3752/LT3752-1 applications, efficiency and internal power dissipation should also be considered. INTV_{CC} can

be externally overdriven by the housekeeping supply to improve efficiency, remove power dissipation from within the IC and provide more than 35mA output current capability. Any overdrive level should exceed the regulated INTV_{CC} level but not exceed 16V.

In the case of a short-circuit fault from INTV_{CC} to ground, each IC reduces the INTV_{CC} output current limit to typically 23mA. The INTV_{CC} regulator has an undervoltage lockout rising threshold, UVLO(+), which prevents gate driver switching until INTV_{CC} reaches 4.75V (7V for LT3752-1) and maintains switching until INTV_{CC} falls below a UVLO(–) threshold of 4.6V (6.8V for LT3752-1).

For V_{IN} levels close to or below the INTV_{CC} regulated level, the INTV_{CC} linear regulator may enter dropout. The resulting lower INTV_{CC} level will still allow gate driver switching as long as INTV_{CC} remains above INTV_{CC} UVLO(–) levels. See the Typical Performance Characteristics section for INTV_{CC} performance vs V_{IN} and load current.

HOUSEKEEPING CONTROLLER

The LT3752/LT3752-1 include an internal constant frequency, current mode, PWM controller for creating a housekeeping supply (see the Block Diagram and Figure 8). Connected as a flyback converter with multiple outputs, the housekeeping supply is able to efficiently provide bias to both primary and secondary ICs. It eliminates the need to generate bias supplies from auxiliary windings in the main forward transformer, reducing the complexity, size and cost of the transformer.

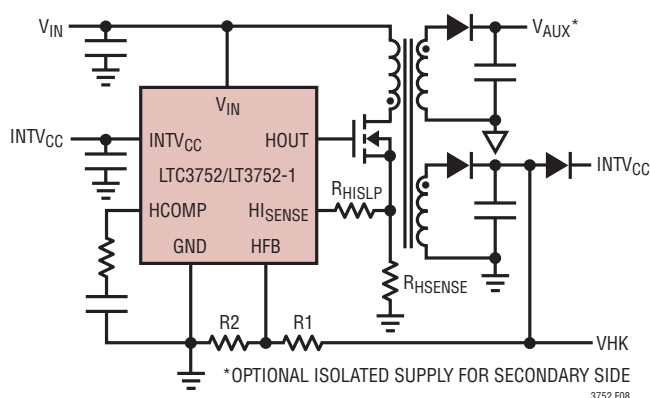


Figure 8. Housekeeping Supply

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Integrating the housekeeping controller saves cost and space and allows switching frequency to be inherently synchronized to the main forward converter.

The housekeeping supply can be used to overdrive the INTV_{CC} pin to take power outside of the part, improve efficiency, provide more drive current and optimize the INTV_{CC} level. It can also be used as a bootstrap bias to the V_{IN} pin as described in the section LT3752-1 Part Start-Up. The housekeeping supply also allows bias to any secondary side IC before the main forward converter starts switching. This removes the need for external start-up circuitry on the secondary side. Alternative methods involve powering secondary side ICs directly from the output voltage of the forward converter. This can cause issues depending on the minimum and maximum allowed input voltages for each IC.

Housekeeping: Operation

The LT3752/LT3752-1 housekeeping controller operation is best described by referring to the Block Diagram and Figure 8. The housekeeping controller uses a ±0.7A gate driver at HOUT to control an external N-channel MOSFET. When current in the primary winding of the flyback transformer exceeds a level commanded by HCOMP and sensed at the HI_{SENSE} pin, the duty cycle of the HOUT is terminated. Stored energy in the transformer is delivered to the output during the off time of HOUT. The housekeeping output voltage is programmed using a resistor divider to the HFB pin. A transconductance amplifier monitors the error signal between HFB pin and a 1.0V reference to control HCOMP level and hence peak switch current. A simple RC network from HCOMP pin to ground provides compensation. Overcurrent protection exists for the external switch when 98mV is sensed at the HI_{SENSE} pin. This causes a low power hiccup mode (repeated retry cycles' of shutdown followed by soft-start) until the overcurrent condition is removed.

Housekeeping: Soft-Start/Shutdown

During start-up of the LT3752/LT3752-1, the housekeeping controller has a built-in soft-start of approximately 2.2ms. The time will vary depending on the HCOMP level needed

to achieve regulation. The housekeeping controller is shut down and the internal soft-start capacitor is discharged for any of the following conditions (typical values):

- (1) UVLO_V_{SEC} < 1.25V (and SS1 < 0.15V) :Soft-Stop Shutdown
 - (2) UVLO_V_{SEC} < 0.4V :Micropower Shutdown
 - (3) OVLO > 1.250V :System Input OVLO
 - (4) HI_{SENSE} > 98mV :Housekeeping Overcurrent
 - (5) INTV_{CC} < X, > 16.5V :INTV_{CC} UVLO, OVLO
 - (6) T_J > 170°C :Thermal Shutdown
 - (7) V_{IN} < Y :V_{IN} Pin UVLO
- (X = 4.6V, Y = 5.5V for LT3752)
(X = 6.8V, Y = 7.6V for LT3752-1)

Housekeeping: Programming Output Voltage

The output voltage, V_{HK}, of the housekeeping controller is programmed using a resistor divider between V_{HK} and the HFB pin (Figure 8) using the equation:

$$V_{HK} = 1V \cdot \left(1 + \frac{R1}{R2}\right)$$

The HFB pin bias current is typically 85nA.

Housekeeping: Programming Cycle-by-Cycle Peak Inductor Current and Slope Compensation

The housekeeping controller limits cycle-by-cycle peak current in the external switch and primary winding of the flyback transformer by sensing voltage at a resistor (R_{HI_{SENSE}}) connected in the source of the external N-channel MOSFET (Figure 8). This sense voltage is compared to a sense threshold at the HI_{SENSE} pin, controlled by HCOMP with an upper limit of 79mV. Since there is only one sense line from the positive terminal of the sense resistor, any parasitic resistance in ground side will increase its effective value and reduce available peak switch current. For operation in continuous mode and above 50% duty cycle, required slope compensation can be programmed by adding a resistor R_{HISLP} in series with the HI_{SENSE} pin. A ramped current always flows out of the HI_{SENSE} pin. The current starts from 2μA at 0% duty cycle and ramps to 52μA at 100% duty cycle. Minimize capacitance on this pin.

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For a desired peak switch current, the value for R_{HSENSE} should be calculated using a 30% derated 79mV sense threshold with the effects of slope compensation included:

$$R_{HSENSE} = \frac{52.5\text{mV} - \Delta V_{HSLP}}{I_{LP(PEAK)}}$$

where:

$$\Delta V_{HSLP} = (2\mu\text{A} + D \cdot (62.5\mu\text{A})) \cdot R_{HISLP}$$

$I_{LP(PEAK)}$ = cycle-by-cycle peak current in primary winding

D = switch duty cycle

R_{HISLP} = slope compensation programming resistor

If operating in continuous mode above 50% duty cycle, a good starting value for R_{HISLP} is 499Ω which gives a 26mV total drop in current comparator threshold at 80% duty cycle. An f_{SYNC}/f_{OSC} ratio of x ($1.0V < x < 1.25$) will reduce the externally programmed slope compensation by a factor of 1.2x. If required, the external resistor R_{HISLP} can be reprogrammed higher by a factor of 1.2x.

Housekeeping: Adaptive Leading Edge Blanking

Blanking of the HL_{SENSE} signal on the leading edge of HOUT is adaptive to allow a wide range of MOSFETs. The blanking occurs from the start of HOUT rise and waits until HOUT has reached within 1V of its maximum level ($INTV_{CC}$ for LT3752, V_{IN} for LT3752-1) before adding an additional fixed 100ns of blanking.

Housekeeping: Overcurrent Hiccup Mode

To protect the housekeeping controller during a short-to-ground fault on the housekeeping output voltage, a 98mV fixed overcurrent threshold exists at the HL_{SENSE} pin to discharge the internal soft-start capacitor and enter a hiccup (retry) mode. This hiccup mode significantly reduces the average power in the external components compared to continued cycle-by-cycle switching at the 79mV threshold. Having already calculated the R_{HSENSE} resistor for peak cycle-by-cycle current, the typical

hiccup mode over current level in the switch and primary winding is given by:

$$I_{LP(OVERCURRENT)} = \frac{98\text{mV} - \Delta V_{HSLP}}{R_{HSENSE}}$$

where:

$$\Delta V_{HSLP} = (2\mu\text{A} + D \cdot (62.5\mu\text{A})) \cdot R_{HISLP}$$

D = switch duty cycle

R_{HISLP} = slope compensation programming resistor

R_{HSENSE} = current sense resistor

Housekeeping: Output Overvoltage and Power Good

The housekeeping controller monitors its supplies' rising output voltage V_{HK} via the HFB pin and determines power good (PGOOD(+)) when V_{HK} reaches 96% of its programmed value. 10μs after confirmation of PGOOD, the circuitry for the LT3752/LT3752-1 forward controller is activated.

The SS1 pin is allowed to begin charging and eventually allows the forward converter to start switching. If V_{HK} falls below 92% of its programmed level (PGOOD(-)), the SS1 pin is discharged and forward controller circuitry is disabled.

To limit housekeeping output overvoltage, V_{HK} , the housekeeping controller overrides its own regulation loop and immediately stops switching if its output voltage exceeds 20% of its programmed value. This is especially important when using the housekeeping supply to bias other ICs. The forward controller is still allowed to switch. The housekeeping controller returns to normal regulation loop control when its output voltage, V_{HK} , falls to less than 15% above its programmed value.

Housekeeping: Transformer Turns Ratio and Leakage Inductance

The external resistor divider used to set the output voltage of the housekeeping supply provides a relative freedom in selecting the transformer turns ratio to suit a given

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application. Simple integer turns ratios can be used which allow off-the-shelf transformers (see example circuits in the Typical Applications section). Turns ratios can be chosen on the basis of desired duty cycle. However, the input and output levels, turns ratio and flyback leakage spike must be considered for the breakdown rating of the MOSFET. Transformer leakage inductance causes a voltage spike to occur after the switch turns off. In some cases a snubber circuit will be required to limit this spike.

Housekeeping: Operating Without This Supply

The housekeeping supply is highly recommended for providing local bias voltages for both the primary and secondary sides (to improve efficiency, simplify the main transformer design and ensure all ICs are activated even for $V_{OUT} = 0V$). The LT3752 (not LT3752-1) housekeeping supply components can be omitted (not populated) if an extra winding already exists from the main transformer to create an auxiliary supply. Care must be taken that the auxiliary supply (for either the primary side or secondary side or both) does not affect proper operation. A resistor divider (Figure 8) should now be connected directly from $INTV_{CC}$ to supply the HFB pin with a ratio :

$$R1/R2 = 3$$

(Example : $R1 = 10k$, $R2 = 3.32k$).

This ratio ensures $HFB \gg 0.96V$ (typical PGOOD level to enable SS1 and the forward converter).

(a) At $INTV_{CC} = 4.75V$ (UVLO(+)), $HFB = 1.2V$.

(b) At $INTV_{CC} = 7V$ (Regulated), $HFB = 1.7V$.

(c) At $INTV_{CC} = 8V$ (Overdriven), $HFB = 2V$.

Care should be taken not to exceed $HFB = 3V$.

FORWARD CONTROLLER

The LT3752/LT3752-1 are primary side, current mode, PWM controllers optimized for use in a synchronous forward converter with active clamp reset. Each IC can

be used in a fully regulated forward converter application. In addition, they can still operate if damage occurs to the feedback path—no secondary side error amplifier or opto-coupler—by using an accurate, programmable volt-second clamp to regulate duty cycle inversely proportional to transformer input voltage.

Adaptive Leading Edge Blanking Plus Programmable Extended Blanking

The LT3752/LT3752-1 provide a $\pm 2A$ gate driver at the OUT pin to control an external N-channel MOSFET for main power delivery in the forward converter (Figure 10). During gate rise time and sometime thereafter, noise can be generated in the current sensing resistor connected to the source of the MOSFET. This noise can potentially cause a false trip of sensing comparators resulting in early switch turn off and in some cases re-soft-start of the system. To prevent this, LT3752/LT3752-1 provide adaptive leading edge blanking of both OC and I_{SENSE} signals to allow a wide range of MOSFET Q_G ratings. In addition, a resistor R_{TBLNK} connected from T_{BLNK} pin to analog ground (Pin 18) programs an extended blanking duration (Figure 9).

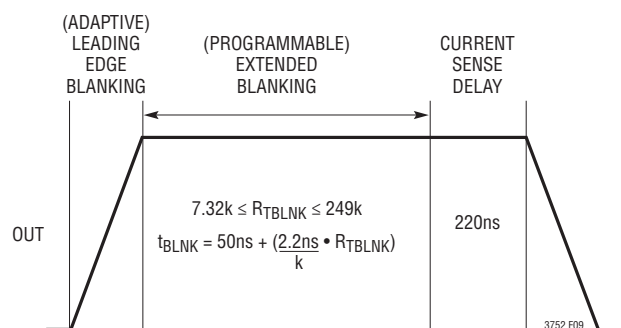


Figure 9. Adaptive Leading Edge Blanking Plus Programmable Extended Blanking

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Adaptive leading edge blanking occurs from the start of OUT rise and completes when OUT reaches within 1V of its maximum level ($INTV_{CC}$ for LT3752, V_{IN} for LT3752-1). An extended blanking then occurs which is programmable using the R_{TBI_NK} resistor given by:

$$t_{\text{BLNK}} = 50\text{ns} + \left(\frac{2.2\text{ns}}{k} \cdot R_{\text{TBLNK}} \right)$$

$$7.32k < R_{\text{TRUNK}} < 249k$$

Adaptive leading edge blanking minimizes the value required for R_{TBLNK} . Increasing R_{TBLNK} further than required increases M1 minimum on time (Figure 10).

In addition, the critical volt-second clamp (D_{VSEC}) is not blanked. Therefore, if D_{VSEC} decreases far enough (in soft start foldback and at maximum input voltage) M1 may turn off before blanking has completed. Since OC and I_{SENSEP} signals are only seen when M1 is on (and after blanking has completed), R_{TRINK} value should be limited by:

$$(2.2\text{ns/k})R_{\text{TBLNK}} < T_{\text{VSEC(MIN)}} - t_{\text{ADAPTIVE}} - 50\text{ns}$$

where,

$$T_{VSEC(MIN)} = 10^9 (D_{VSEC(MAX)} / (\text{fold.fosc}))$$

$$(\text{Input}_{(MIN)} / \text{Input}_{(MAX)})$$

fold = f_{OSC} and D_{VSEC} foldback ratio (for OUT pin)
(= 4 for LT3752 , = 2 for LT3752-1)

$$t_{\text{ADAPTIVE}} = \text{OUT pin rise time to } \text{INTV}_{\text{CC}} - 1\text{V}$$

Example: For Figure 20 circuit, $D_{VSEC(MAX)} = 0.77$, $Input_{(MIN)/(MAX)} = 17.4V/74V$, $fold = 4$, $t_{ADAPTIVE} = 23ns$ and $f_{OSC} = 240kHz$,

$$T_{VSEC(MIN)} = 10^9(0.77/(4 \cdot 2.4 \cdot 10^5)) \cdot 17.4/74 = 188ns$$

$$(2.2ns/1k)R_{TRINK} < 188 - 23 - 50$$

$R_{TBI\ NK} < 52.5k$ (Actual Circuit Uses 34k)

Current Sensing and Programmable Slope Compensation

The LT3752/LT3752-1 command cycle-by-cycle peak current in the external switch and primary winding of the forward transformer by sensing voltage across a resistor

connected in the source of the external n-channel MOSFET (Figure 10).

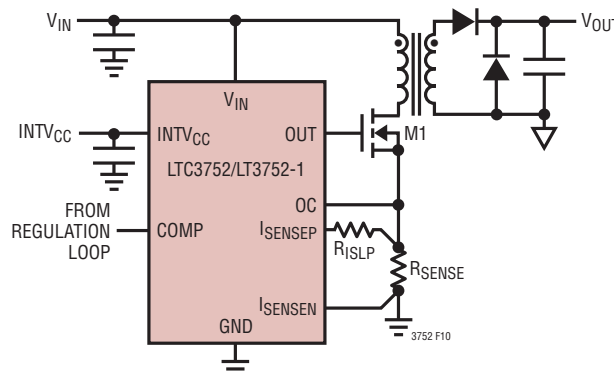


Figure 10. Current Sensing and Programmable Slope Compensation

The sense voltage across R_{SENSE} is compared to a sense threshold at the I_{SENSEP} pin, controlled by COMP pin level. Two sense inputs, I_{SENSEP} and I_{SENSEN} , are provided to allow a Kelvin connection to R_{SENSE} . For operation in continuous mode and above 50% duty cycle, required slope compensation can be programmed by adding a resistor, R_{ISLP} , in series with the I_{SENSEP} pin. A ramped current always flows out of the I_{SENSE} pin. The current starts from $2\mu A$ at 0% duty cycle and linearly ramps to $33\mu A$ at 80% duty cycle. A good starting value for R_{ISLP} is $1.5k\Omega$ which gives a 41mV total drop in current comparator threshold at 65% duty cycle.

The COMP pin commands an I_{SENSEP} threshold between 0mV and 220mV. The 220mV allows a large slope compensation voltage drop to exist in R_{ISLP} without effecting the programming of R_{SENSE} to set maximum operational currents in M1. An f_{SYNC}/f_{OSC} ratio of x ($1.0 < x < 1.25$) will reduce the externally programmed slope compensation by a factor of $1.2x$. If required, the external resistor R_{ISLP} can be reprogrammed higher by a factor of $1.2x$.

Overcurrent: Hiccup Mode

The LT3752/LT3752-1 use a precise 96mV sense threshold at the OC pin to detect excessive peak switch current (Figure 10). During an overload condition switching

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stops immediately and the SS1/SS2 pins are rapidly discharged. The absence of switching reduces the sense voltage at the OC pin, allowing SS1/SS2 pins to recharge and eventually attempt switching again. The part exists in this hiccup mode as long as the overcurrent condition exists. This protects the converter and reduces power dissipation in the components (see Hard Stop in the Applications Information section). The 96mV peak switch current threshold is independent of the voltage drop in R_{ISLP} used for slope compensation.

Output DC load current to trigger hiccup mode:

$$\text{LOAD(OVERCURRENT)} = \left(\frac{N_P}{N_S} \cdot \frac{96\text{mV}}{R_{\text{ISENSE}}} \right) - \left(1/2 I_{\text{RIPPLE(P-P)}} \right)$$

where:

N_P = forward transformer primary turns

N_S = forward transformer secondary turns

$I_{\text{RIPPLE(P-P)}}$ = Output inductor peak-to-peak ripple current

R_{ISENSE} should be programmed to allow maximum DC load current for the application plus enough margin during load transients to avoid overcurrent hiccup mode.

Programming Maximum Duty Cycle Clamp: D_{VSEC} (Volt-Second Clamp)

Unlike other converters which only provide a fixed maximum duty cycle clamp, the LT3752/LT3752-1 provide an accurate programmable maximum duty cycle clamp (D_{VSEC}) on the OUT pin which moves inversely with system input. D_{VSEC} provides a duty cycle guardrail to limit the volt-seconds-on product over the entire natural duty cycle range (Figures 11 and 12). This limits the drain voltage required for complete transformer reset.

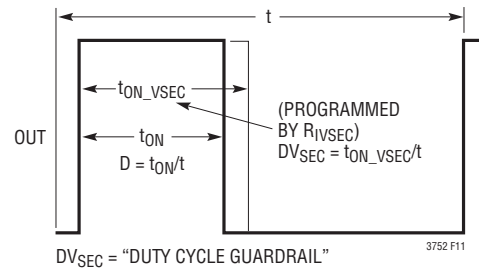


Figure 11. Volt-Second (D_{VSEC}) Clamp

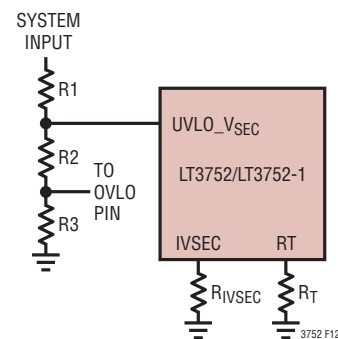


Figure 12. Programming D_{VSEC}

A resistor R_{IVSEC} from the IVSEC pin to analog ground (Pin 18) programs D_{VSEC} .

D_{VSEC} (OUT pin duty cycle clamp)

$$= 0.725 \cdot \frac{R_{\text{IVSEC}}}{51.1\text{k}} \cdot \frac{f_{\text{OSC}}}{300} \cdot \frac{1.25}{\text{UVLO_VSEC}}$$

where:

R_{IVSEC} = programming resistor at IVSEC pin

f_{OSC} = switching frequency (kHz)

UVLO_VSEC = resistor divided system input voltage

R_{IVSEC} can program any D_{VSEC} required at minimum system input. D_{VSEC} will then follow natural duty cycle as V_{IN} varies. Maximum programmable D_{VSEC} is typi-

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cally 0.75 but may be further limited by the transformer design and voltage ratings of components connected to the drain of the primary side power MOSFET (SWP). See voltage calculations in the LO side and HI side active clamp topologies sections.

If system input voltage falls below its UVLO threshold the part will enter soft-stop with continued switching. The LT3752/LT3752-1 include an intelligent circuit which prevents D_{VSEC} from continuing to rise as system input voltage falls (see Soft-Stop). Without this, too large a D_{VSEC} would require extremely high reset voltages on the SWP node to properly reset the transformer. The UVLO_ V_{SEC} pin maximum operational level is the lesser of $V_{IN} - 2V$ or 12.5V.

The LT3752/LT3752-1 volt-second clamp architecture is superior to an external RC network connected from system input to trip an internal comparator threshold. The RC method suffers from external capacitor error, part-to-part mismatch between the RC time constant and the IC's switching period, the error of the internal comparator threshold and the nonlinearity of charging at low input voltages. The LT3752/LT3752-1 use the R_{IVSEC} resistor to define the charge current for an internal timer capacitor to set an OUT pin maximum on-time, $t_{ON(VSEC)}$. The voltage across R_{IVSEC} follows UVLO_ V_{SEC} pin voltage (divided down from system input voltage). Hence, R_{IVSEC} current varies linearly with input supply. The LT3752/LT3752-1 also trim out internal timing capacitor and comparator threshold errors to optimize part-to-part matching between $t_{ON(VSEC)}$ and T.

D_{VSEC} Open Loop Control: No Opto-Coupler, Error Amplifier or Reference

The accuracy of the programmable volt-second clamp (D_{VSEC}) safely controls V_{OUT} if open loop conditions exist such as no opto-coupler, error amplifier or reference on the

secondary side. D_{VSEC} controls the output of the converter by controlling duty cycle inversely proportional to system input. If D_{VSEC} duty cycle guardrail is programmed X% above natural duty cycle, V_{OUT} will only increase by X% if a closed loop system breaks open. This volt-second clamp is operational over a 10:1 system input voltage range. See D_{VSEC} versus UVLO_ V_{SEC} pin voltage in the Typical Performance Characteristics section.

R_{IVSEC} : Open Pin Detection Provides Safety

The LT3752/LT3752-1 provide an open-detection safety feature for the R_{IVSEC} pin. If the R_{IVSEC} resistor goes open circuit the part immediately stops switching. This prevents the part from running without the volt-second clamp in place.

Transformer Reset: Active Clamp Technique

The LT3752/LT3752-1 include a $\pm 0.4A$ gate driver at the AOUT pin to allow the use of an active clamp transformer reset technique (Figures 13, 17). The active clamp method improves efficiency and reduces voltage stress on the main power switch, M1. By switching in the active clamp capacitor only when needed, the capacitor does not lose its charge during M1 on-time. By allowing the active clamp capacitor, C_{CL} , to store the average voltage required to reset the transformer, the main power switch sees lower drain voltage.

An imbalance of volt-seconds will cause magnetizing current to walk upwards or downwards until the active clamp capacitor is charged to the optimal voltage for proper transformer reset. The voltage rating of the capacitor will depend on whether the active clamp capacitor is actively switched to ground (Figure 13) or actively switched to

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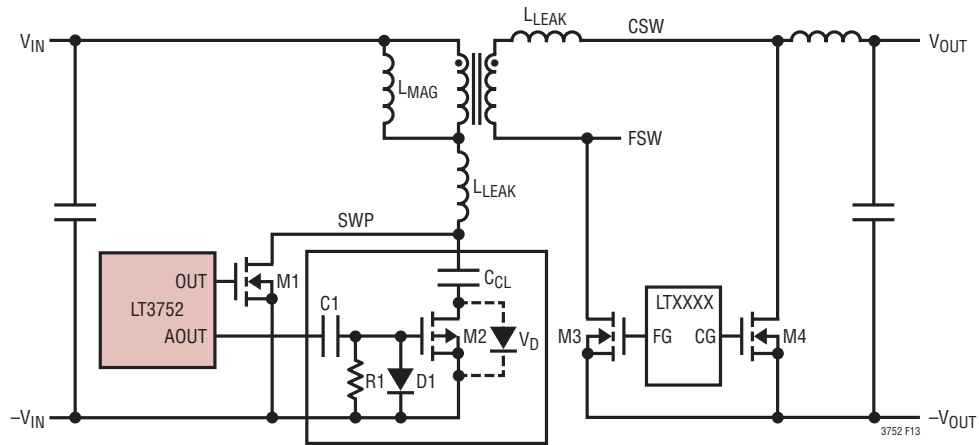


Figure 13. LO Side Active Clamp Topology

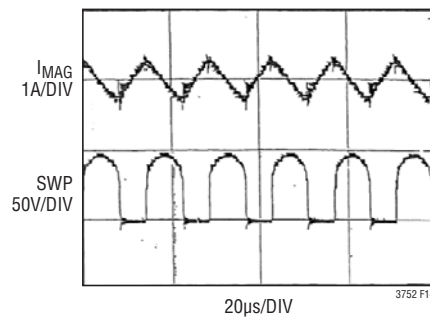


Figure 14. Active Clamp Reset: Magnetizing Current and M1 Drain Voltage

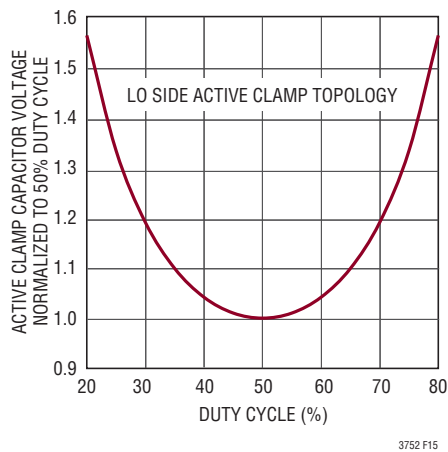


Figure 15. LO Side V_{CCL} vs Duty Cycle (Normalized to 50% Duty Cycle)

system input (Figure 17). In an active clamp reset topology, volt-second balance requires:

$$V_{IN} \cdot D = (SWP - V_{IN}) \cdot (1 - D)$$

where:

V_{IN} = Transformer input supply

$D = (V_{OUT}/V_{IN}) \cdot N$ = switch M1 duty cycle

V_{OUT} = Output voltage (including the voltage drop contribution of M4 catch diode during M1 off)

N = Transformer turns ratio = N_P/N_S

SWP = M1 drain voltage

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LO Side Active Clamp Topology (LT3752)

The steady-state active clamp capacitor voltage, V_{CCL} , required to reset the transformer in a LO side active clamp topology (Figure 13) can be approximated as the drain-to-source voltage (V_{DS}) of switch M1, given by:

V_{CCL} (LO side):

(a) Steady state: $V_{CCL} = SWP = V_{DS}$

$$= \left(\frac{1}{1-D} \right) \cdot V_{IN} = \frac{V_{IN}^2}{(V_{IN} - (V_{OUT} \cdot N))}$$

(b) Transient:

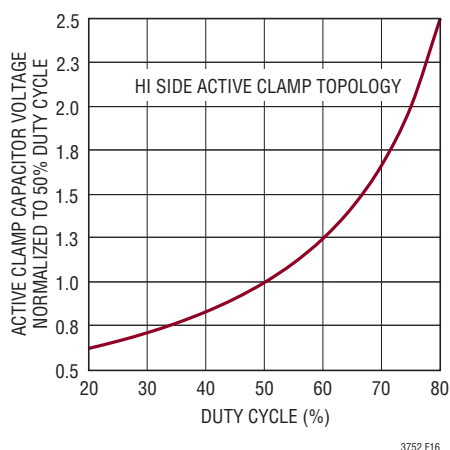


Figure 16. HI Side V_{CCL} vs Duty Cycle (Normalized to 50% Duty Cycle)

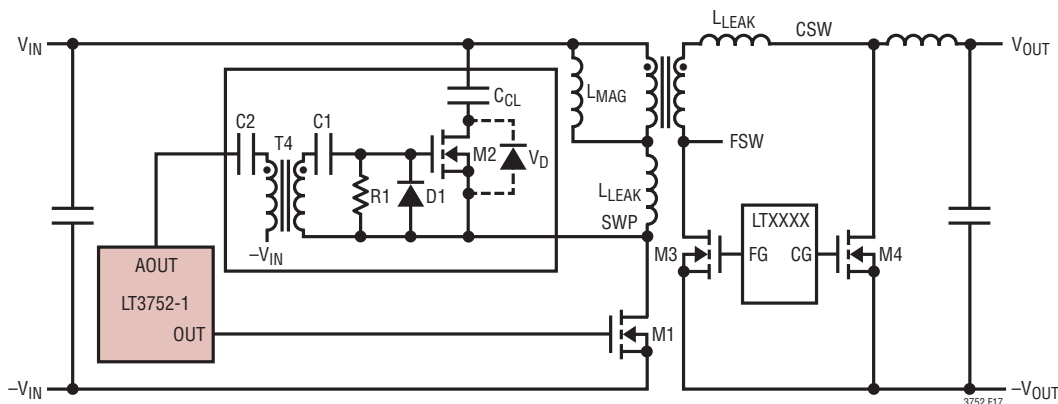


Figure 17. HI Side Active Clamp Topology

During load transients, duty cycle and hence V_{CCL} may increase. Replace D with D_{VSEC} in the equation above to calculate transient V_{CCL} values. See the previous section Programming Duty Cycle Clamp— D_{VSEC} . The D_{VSEC} guard-rail can be programmed as close as 5% higher than D but may require a larger margin to improve transient response.

As shown in Figure 15, the maximum steady-state value for V_{CCL} may occur at minimum or maximum input voltage. Hence V_{CCL} should be calculated at both input voltage levels and the largest of the two calculations used. M1 drain should be rated for a voltage greater than the above steady-state V_{DS} calculation due to tolerances in duty cycle, load transients, voltage ripple on C_{CL} and leakage inductance spikes. C_{CL} should be rated higher due to the effect of voltage coefficient on capacitance value. A typical choice for C_{CL} is a good quality X7R capacitor. M2 should have a V_{DS} rating greater than V_{CCL} since the bottom plate of C_{CL} is $-V_{CCL}$ during M1 on and M2 off. For high input voltage applications, the limited V_{DS} rating of available P-channel MOSFETs might require changing from a LO side to HI side active clamp topology.

For the LO side active clamp topology in steady state, during M1 on time, magnetizing current (I_{MAG}) increases from a negative value to a positive value (Figure 14). When M1 turns off, magnetizing current charges SWP until it reaches V_{CCL} plus the voltage drop of the M2 body diode. At this

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moment the active clamp capacitor is passively switched in to ground (due to the forward conduction of M2 body diode) and the drain voltage increases at a slower rate due to the loading of C_{CL} . SWP above V_{IN} causes I_{MAG} to reduce from a positive value towards zero ($dV_{SWP}/dT = 0$). As I_{MAG} becomes negative it begins to discharge the SWP node. Switching in M2 before I_{MAG} reverses, actively connects the bottom plate of C_{CL} to ground and allows SWP to be discharged slowly. The resulting SWP waveform during M1 off-time appears as a square wave with a superimposed sinusoidal peak representing ripple voltage on C_{CL} .

The switch M2 experiences near zero voltage switching (ZVS) since only the body diode voltage drop appears across it at switch turn on.

HI Side Active Clamp Topology (LT3752-1)

For high input voltage applications the V_{DS} rating of available P-channel MOSFETs might not be high enough to be used as the active clamp switch in the LO side active clamp topology (Figure 13). An N-channel approach using the HI side active clamp topology (Figure 17) should be used. This topology requires a gate drive transformer or a simple gate drive opto-coupler to drive the N-channel MOSFET (M2) for switching in the active clamp capacitor from SWP to V_{IN} . The M1 drain voltage calculation is the same as in the LO side active clamp case and M1 should be rated in a similar manner. The voltage across the clamp capacitor in the HI side architecture, however, is lower by V_{IN} since it is referenced to V_{IN} .

The steady-state active clamp capacitor voltage V_{CCL} to reset the transformer in a HI side active clamp topology can be approximated by:

V_{CCL} (HI side):

(a) Steady state: $V_{CCL} = V_{RESET} = V_{DS} - V_{IN}$

$$= \left(\frac{D}{1-D} \right) \cdot V_{IN} = V_{IN} \cdot V_{OUT} \cdot \frac{N}{V_{IN} - (V_{OUT} \cdot N)}$$

(b) Transient:

During load transients, duty cycle and hence V_{CCL} may increase. Replace D with D_{VSEC} in the equation above to calculate transient V_{CCL} values. D_{VSEC} guardrail can be programmed as close as 6% higher than D but may require a larger margin to improve transient response. See the previous section Programming Duty Cycle Clamp- D_{VSEC} .

C_{CL} should be rated for a voltage higher than the above steady-state calculation due to tolerances in duty cycle, load transients, voltage ripple on C_{CL} and the effect of voltage coefficient on capacitance value. A typical choice for C_{CL} is a good quality (X7R) capacitor. When using a gate drive transformer to provide control of the active clamp switch (M2), the external components C1, C2, R1, D1 and T4 are required. T4 size will increase for lower programmed switching frequencies due to a minimum volt-second requirement. Alternatively, a simple gate driver opto-coupler can be used as a switch to control M2, for a smaller solution size. The input supply capacitor for the gate drive opto-coupler is easily charged using the housekeeping supply of the LT3752-1. Common component values are shown in the Typical Applications section.

Active Clamp Capacitor Value and Voltage Ripple

The active clamp capacitor value should be chosen based on the amount of voltage ripple which can be tolerated by components attached to SWP. Lower C_{CL} values will create larger voltage ripple (increased drain voltage for the primary side power MOSFET) but will require less swing in magnetizing current to move the active clamp capacitor during duty cycle changes. Choosing too high a value for the active clamp capacitor (beyond what is needed to keep ripple voltage to an acceptable level) will require unnecessary additional flux swing during transient conditions. For systems with flux swing detection, too high a value for the active clamp capacitor will trigger the detection system early and degrade transient response.

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Another factor to consider is the resonance between C_{CL} and the magnetizing inductance (L_{MAG}) of the main transformer. An RC snubber (R_S , C_S) in parallel with C_{CL} will dampen the sinusoidal ringing and limit the peak voltages at the primary side MOSFET drain during input/load transients. Check circuit performance to determine if the snubber is required. Component values can be approximated as:

$$C_{CL} \text{ (active clamp capacitance)} = \frac{10}{L_{MAG}} \cdot \left(\frac{(1-D_{MIN})}{2 \cdot \pi \cdot f_{OSC}} \right)^2$$

where,

$$D_{MIN} = (V_{OUT}/V_{IN(MAX)}) \cdot N_P/N_S$$

and (if needed),

$$C_S \text{ (snubber capacitance)} = 6 \cdot C_{CL}$$

$$R_S \text{ (snubber resistance)} = (1/(1-D_{MAX})) \cdot \sqrt{(L_{MAG}/C_{CL})}$$

where,

$$D_{MAX} = (V_{OUT}/V_{IN(MIN)}) \cdot N_P/N_S$$

Check the voltage ripple on SWP during steady-state operation.

C_{CL} voltage ripple can be estimated as:

$$V_{CCL(RIPPLE)} = V_{CCL} \cdot (1-D)^2 / (8 \cdot C_{CL} \cdot L_{MAG} \cdot f_{OSC}^2)$$

where,

$$D = (V_{OUT}/V_{IN}) \cdot (N_P/N_S)$$

$$V_{CCL} = V_{IN}/(1-D) \text{ (Lo side active clamp topology)}$$

$$V_{CCL} = D \cdot V_{IN}/(1-D) \text{ (Hi side active clamp topology)}$$

Example : For $V_{IN} = 36V$, $V_{OUT} = 12V$, $N_P/N_S = 2$, $V_{CCL} = 108V$ (Lo side active clamp topology), $C_{CL} = 22nF$, $L_{MAG} = 100\mu H$, $f_{OSC} = 250kHz$, $V_{CCL(RIPPLE)} = 108(0.33)^2 / (8(22 \cdot 10^{-9})(10^{-4})(2.5 \cdot 10^4)^2) = 10.7V$

The transformer is typically chosen to operate at a maximum flux density that is low enough to avoid excessive core losses. This also allows enough headroom during input and load transients to move the active clamp capacitor at a fast enough rate to keep up with duty cycle changes.

Active Clamp MOSFET Selection

The selection of active clamp MOSFET is determined by the maximum levels expected for the drain voltage and drain current. The active clamp switch (M2) in either a lo side or hi side active clamp topology has the same BV_{dss} requirements as the main N-channel power MOSFET. The current requirements are divided into two categories :

(A) Drain Current

This is typically less than the main N-channel power MOSFET because the active clamp MOSFET sees only magnetizing current, estimated as :

$$\text{Peak } I_{MAG} \text{ (steady state)} = (1/2) \cdot (N_P/N_S) \cdot (V_{OUT}/L_{MAG}) \cdot (1/f_{OSC})$$

where,

L_{MAG} = main transformer's magnetizing inductance

Example (LT3752) : For $V_{OUT} = 12V$, $N_P/N_S = 2$, $f_{OSC} = 250kHz$ and $L_{MAG} = 100\mu H$, Peak $I_{MAG} = 0.48A$.

This value should be doubled for safety margin due to variations in L_{MAG} , f_{OSC} and transient conditions.

(B) Body Diode Current

The body diode will see reflected output current as a pulse every time the main N-channel power MOSFET turns off. This is due to residual energy stored in the transformer's leakage inductance. The body diode of the active clamp MOSFET should be rated to withstand a forward pulsed current of:

$$I_{D(MAX)} = (N_S/N_P) (I_{OUT(MAX)} + (I_{L(RIPPLE)}(P-P)/2))$$

where,

$$I_{L(RIPPLE)}(P-P) = \text{output inductor ripple current} = (V_{OUT}/(L_{OUT} \cdot f_{OSC})) \cdot (1 - (V_{OUT}/V_{IN})(N_P/N_S))$$

$$I_{OUT(MAX)} = \text{maximum output load current}$$

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Programming Active Clamp Switch Timing: AOUT to OUT (t_{AO}) and OUT to AOUT (t_{OA}) Delays

The timings t_{AO} and t_{OA} represent the delays between AOUT and OUT edges (Figures 1 and 2) and are programmed by a single resistor, R_{TAO} , connected from analog ground (Pin 18) to the T_{AO} pin. Once t_{AO} is programmed for the reasons given below, t_{OA} will be automatically generated.

Front-end timing t_{AO} (M2 off, M1 on)

= AOUT(edge)-to-OUT(rising)

$$= 50\text{ns} + 3.8\text{ns} \cdot \left(\frac{R_{TAO}}{1\text{k}} \right), 14.7\text{k} < R_{TAO} < 125\text{k}$$

In order to minimize turn-on transition loss in M1 the drain of M1 should be as low as possible before M1 turns on. To achieve this, AOUT should turn M2 off a delay of t_{AO} before OUT turns M1 on. This allows the main transformer's magnetizing current to discharge M1 drain voltage quickly towards V_{IN} before M1 turns on.

As SWP falls below V_{IN} , however, the rectifying diodes on the secondary side are typically active and clamp the SWP node close to V_{IN} . If enough leakage inductance exists, however, the clamping action on SWP by the secondary side will be delayed—potentially allowing the drain of M1 to be fully discharged to ground just before M1 turns on. Even with this delay due to the leakage inductance, L_{MAG} needs to be low enough to allow I_{MAG} to be negative enough to slew SWP down to ground before M1 turns on. If achievable, M1 will experience zero voltage switching (ZVS) for highest efficiency. As will be seen in a later section entitled Primary-Side Power MOSFET Selection, M1 transition loss is a significant contributor to M1 losses.

Back-end timing t_{OA} (M1 off, M2 on) is automatically generated

$$= \text{OUT(falling)-to-AOUT(edge)} = 0.9 \cdot t_{AO}$$

t_{OA} should be checked to ensure M2 is not turned on until M1 and M3 are turned off.

Programming Synchronous Rectifier Timing: SOUT to OUT (t_{SO}) and OUT to SOUT (t_{OS}) Delays

The LT3752/LT3752-1 include a $\pm 0.4\text{A}$ gate driver at the SOUT pin to send a control signal via a pulse transformer to the secondary side of the forward converter for synchronous rectification (see Figures 1 and 2). For the highest efficiency, M4 should be turned on whenever M1 is turned off. This suggests that SOUT should be a non-overlapping signal with OUT with very small non-overlap times. Inherent timing delays, however, which can vary from application to application, can exist between OUT to CSW and between SOUT to CG. Possible shoot-through can occur if both M1 and M4 are on at the same time, resulting in transformer and/or switch damage.

Front-end timing: t_{SO} (M4 off, M1 on)

= SOUT(falling)-to-OUT(rising) delay

$$= t_{SO} = t_{AO} - t_{AS}$$

$$= 3.8\text{ns} \cdot (R_{TAS} - R_{TAO})$$

where:

$$t_{AS} = 50\text{ns} + (3.8\text{ns} \cdot R_{TAS}/1\text{k}), 14.7\text{k} < R_{TAS} < 125\text{k},$$

$$t_{AO} = 50\text{ns} + (3.8\text{ns} \cdot R_{TAO}/1\text{k}), 14.7\text{k} < R_{TAO} < 125\text{k},$$

t_{SO} is defined by resistors R_{TAS} and R_{TAO} connected from analog ground (Pin 18) to their respective pins T_{AS} and T_{AO} . Each of these resistor defines a delay referenced to the AOUT edge at the start of each cycle. R_{TAO} was already programmed based on requirements defined in the previous section Programming AOUT to OUT Delay. R_{TAS} is then programmed as a delay from AOUT to SOUT to fulfill the equation above for t_{SO} . By choosing R_{TAS} less than or greater than R_{TAO} , the delay between SOUT falling and OUT rising can be programmed as positive or negative. While a positive delay can always be programmed for t_{SO} , the ability to program a negative delay allows for improved efficiency if OUT(rising)-to-CSW(rising) delay is larger than SOUT(falling)-to-CG(rising) delay.

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Back-end timing: t_{OS} (M1 off, M4 on)
 = OUT (falling)-to-SOUT (rising) delay
 $t_{OS} = 35\text{ns} + (2.2\text{ns} \cdot R_{TOS}/1\text{k})$, $7.32\text{k} < R_{TOS} < 249\text{k}$

The timing resistor, R_{TOS} , defines the OUT (falling)-to-SOUT (rising) delay. This pin allows programming of a positive delay, for applications which might have a large inherent delay from OUT fall to SW2 fall.

Soft-Start (SS1, SS2)

The LT3752/LT3752-1 use SS1 and SS2 pins for soft starting various parameters (Figures 3, 4 and 18). SS1 soft starts internal oscillator frequency and D_{VSEC} (maximum duty cycle clamp). SS2 soft starts COMP pin voltage to control output inductor peak current. Using separate SS1 and SS2 pins allows the soft-start ramp of oscillator frequency and D_{VSEC} to be independent of COMP pin soft-start. Typically SS1 capacitor (C_{SS1}) is chosen as $0.47\mu\text{F}$ and SS2 capacitor (C_{SS2}) is chosen as $0.1\mu\text{F}$. Soft-start charge currents are $11.5\mu\text{A}$ for SS1 and $21\mu\text{A}$ for SS2.

SS1 is allowed to start charging (soft-start) if all of the following conditions exist (typical values) :

- (1) $UVLO_V_{SEC} > 1.25\text{V}$: System input not in UVLO
 - (2) $OVLO < 1.215\text{V}$: System input not in OVLO
 - (3) $HFB > 0.96\text{V}$: Housekeeping supply valid
 - (4) $OC < 96\text{mV}$: No over current condition
 - (5) $X < INTV_{CC} < 16\text{V}$: $INTV_{CC}$ valid
 - (6) $T_J < 165^\circ\text{C}$: Junction temperature valid
 - (7) $V_{IN} > Y$: V_{IN} pin valid
- (X = 4.75V, Y = 5.8V for LT3752)
 (X = 7.0V, Y = 9.5V for LT3752-1)

SS1 = 0V to 1.25V (no switching). This is the SS1 range for no switching for the forward converter. SS2 = 0V.

SS1 > 1.25V allows SS2 to begin charging from 0V.

SS1 = 1.25V to 2.45V (soft-start f_{OSC} , D_{VSEC}). This is the SS1 range for soft-starting f_{OSC} and D_{VSEC} folded back from 22% (50% for LT3752-1) to 100% of their programmed levels. Fold back of f_{OSC} and D_{VSEC} reduces effective minimum duty cycle for the primary side MOSFET. This allows inductor current to be controlled at low output voltages during start-up.

SS1 ramp rate is chosen slow enough to ensure f_{OSC} and D_{VSEC} foldback lasts long enough for the converter to take control of inductor current at low output voltages. In addition, slower SS1 ramp rate increases the non-switching period during an output short to ground fault (over current hiccup mode) to reduce average power dissipation (see Hard-Stop).

SS2 = 0V to 1.6V (soft-start COMP pin). This is the SS2 range for soft-starting COMP pin from approximately 1V to 2.6V.

SS2 ramp rate is chosen fast enough to allow a (slower) soft-start control of COMP pin from a secondary side opto-coupler controller.

SS1 soft-start non-switching period (0V to 1.25V)
 $= 1.25\text{V} \cdot C_{SS1}/11.5\mu\text{A}$

SS1 soft-start f_{OSC} , D_{VSEC} period (1.25V to 2.45V)
 $= 1.2\text{V} \cdot C_{SS1}/11.5\mu\text{A}$

SS2 soft-start COMP period (0V to 1.6V) = $1.6\text{V} \cdot C_{SS2}/21\mu\text{A}$

Soft-Stop (SS1)

The LT3752/LT3752-1 gradually discharge the SS1 pin (soft-stop) when a system input UVLO occurs or when an external soft-stop shutdown command occurs ($0.4\text{V} < UVLO_V_{SEC} < 1.25\text{V}$). During SS1 soft-stop the converter continues to switch, folding back f_{OSC} , D_{VSEC} and COMP pin voltage (Figures 3, 4 and 18). Soft-stop discharge current is $10.5\mu\text{A}$ for SS1. Soft-stop provides:

- (1) Active control of the secondary winding during output discharge for clean shutdown in self-driven applications.
- (2) Controlled discharge of the active clamp capacitor to minimize magnetizing current swing during restart.

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SS1: 2.45V to 1.25V (soft-stop f_{OSC} , D_{VSEC} , COMP). This is the SS1 range for soft-stop folding back of:

- (1) f_{OSC} and D_{VSEC} from 100% to 22% (50% for LT3752-1) of their programmed levels.
- (2) COMP pin (100% to 0% of commanded peak current).

SS1 soft-stop f_{OSC} , D_{VSEC} , COMP period (2.45V to 1.25V)
 $= 1.2V \cdot C_{SS1}/10.5\mu A$

SS1 < 1.25V. Forward converter stops switching and SS2 pin is discharged to 0V using 2.8mA.

SS1 = 1.25V to 0V: When SS1 falls below 0.15V the internal SS1 latch is reset. If all faults are removed, SS1 begins charging again. If faults still remain, SS1 discharges to 0V.

SS1 soft-stop non-switching period (1.25V to 0V)
 $= 1.25V \cdot C_{SS1}/10.5\mu A$

D_{VSEC} rises as system input voltage falls in order to provide a maximum duty cycle guardrail (volt-second clamp). When system input falls below its UVLO threshold, however, this triggers a soft-stop with the converter continuing to switch. It is important that D_{VSEC} no longer increases even though system input voltage may still be falling. The LT3752/LT3752-1 achieve an upper clamp on D_{VSEC} by clamping the minimum level for the I_{VSEC} pin to 1.25V. As SS1 pin discharges during soft-stop it folds back D_{VSEC} . As D_{VSEC} falls below the natural duty cycle of the converter, the converter loop follows D_{VSEC} . If the system input voltage rises (I_{VSEC} pin rises) during soft-stop the volt-second clamp circuit further reduces D_{VSEC} . The I.C. chooses the lowest D_{VSEC} commanded by either the I_{VSEC} pin or the SS1 soft-stop function.

Hard-Stop (SS1, SS2)

Switching immediately stops and both SS1 and SS2 pins are rapidly discharged (Figure 18. Hard-Stop) if any of the following faults occur (typical values):

- (1) $UVLO_V_{SEC} < 0.4V$: Micropower shutdown
- (2) $OVLO > 1.250V$: System input OVLO

(3) $HFB < 0.92V$: Housekeeping supply UVLO

(4) $OC > 96mV$: Over current condition

(5) $INTV_{CC} < X(UVLO)$, $> 16.5V$ (OVLO)

(6) $T_J > 170^\circ C$: Thermal shutdown

(7) $V_{IN} < Y$: V_{IN} pin UVLO

(X = 4.6V, Y = 5.5V for LT3752)

(X = 6.8V, Y = 7.6V for LT3752-1)

Switching stops immediately for any of the faults listed above. When SS1 discharges below 0.15V it begins charging again if all faults have been removed. For an over current fault triggered by $OC > 96mV$, the disable of switching will cause the OC pin voltage to fall back below 96mV. This will allow SS1 and SS2 to recharge and eventually attempt switching again. If the over current condition still exists, OC pin will exceed 96mV again and the discharge/charge cycle of SS1 and SS2 will repeat in a hiccup mode. The non-switching dead time period during hiccup mode reduces the average power seen by the converter in an over current fault condition. The dead time is dominated by SS1 recharging from 0.15V to 1.25V.

Non-switching period in over current (hiccup mode):
 $= 1.1V \cdot C_{SS1}/11.5\mu A$

OUT, AOUT, SOUT Pulse-Skipping Mode

During load steps, initial soft-start, end of soft-stop or light load operation (if the forward converter is designed to operate in DCM), the loop may require pulse skipping on the OUT pin. This occurs when the COMP pin falls below its switching threshold. If the COMP pin falls below its switching threshold while OUT is turned on, the LT3752/LT3752-1 will immediately turn OUT off; both AOUT and SOUT will complete their normal signal timings referenced from the OUT falling edge. If the COMP pin remains below its switching threshold at the start of the next switching cycle, the LT3752/LT3752-1 will skip the next OUT pulse and therefore also skip AOUT and SOUT pulses. For AOUT control, this prevents the active clamp capacitor from be-

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HARD STOP (FAULTS)	SOFT-START (WHEN ALL CONDITIONS SATISFIED)	SOFT-STOP ($0.4V < UVLO_V_{SEC} < 1.25V$)
(1) $UVLO_V_{SEC} < 0.4V$ (2) $OVLO > 1.25V$ (3) $HFB < 0.92V$ (4) $OC > 96mV$ (5) $INTV_{CC} < X, > 16.5V$ (6) $T_J > 170^{\circ}C$ (7) $V_{IN} < Y$ (X = 4.6V, Y = 5.5V: LT3752) (X = 6.8V, Y = 7.6V: LT3752-1)	(1) $UVLO_V_{SEC} > 1.25V$ (2) $OVLO < 1.215V$ (3) $HFB > 0.96V$ (4) $OC < 96mV$ (5) $X < INTV_{CC} < 16V$ (6) $T_J < 165^{\circ}C$ (7) $V_{IN} > Y$ (X = 4.75V, Y = 5.8V: LT3752) (Y = 7.0V, Y = 9.5V: LT3752-1)	(1) EXTERNAL SOFT-STOP SHUTDOWN (2) SYSTEM INPUT UVLO

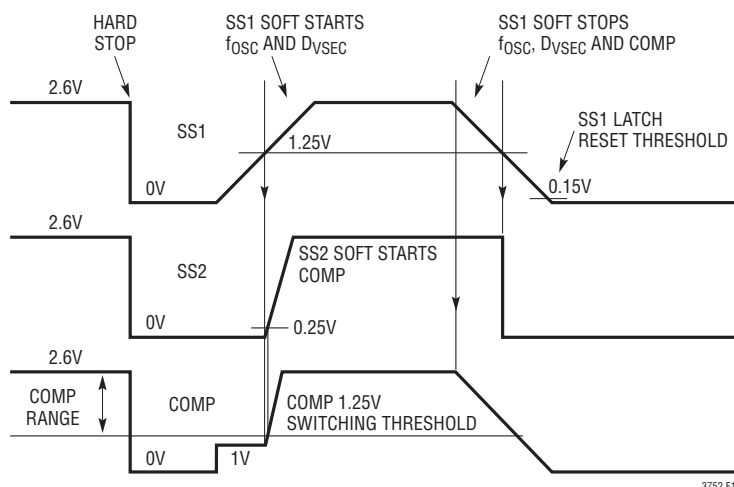


Figure 18. SS1, SS2 and COMP Pin Voltages During Faults, Soft-Start and Soft-Stop

ing accidentally discharged during missing OUT pulses and/or causing reverse saturation of the transformer. For SOUT control, this prevents the secondary side synchronous rectifier controller from incorrectly switching between forward FET and synchronous FET conduction. The LT3752/LT3752-1 correctly re-establish the required AOUT, SOUT control signals if the OUT signal is required for the next cycle.

AOUT Timeout

During converter start-up in soft-start, the switching frequency and maximum duty cycle clamp D_{VSEC} are both folded back. While this correctly reduces the effective minimum on time of the OUT pin (to allow control of inductor current for very low output voltages during start-up), this means the AOUT pin on time duration can be large.

In order to ensure the active clamp switch controlled by AOUT does not stay on too long, the LT3752/LT3752-1 have an internal $15\mu s$ timeout to turn off the AOUT signal. This prevents the active clamp capacitor from being connected across the transformer primary winding long enough to create reverse saturation.

Main Transformer Selection

The LT3752/LT3752-1 simplify the design of the main transformer and output inductor by removing the need for any auxiliary windings. Any bootstrap supplies required for the primary side or bias supplies required for the secondary side can all be provided by the housekeeping DC/DC controller included in the LT3752/LT3752-1. (see Housekeeping Controller in the Applications Information Section).

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The selection of the main transformer will depend on the applications requirements : isolation voltage, power level, maximum volt-seconds, turns ratio, component size, power losses and switching frequency.

Transformer construction using the planar winding technology is typically chosen for minimizing leakage inductance and reducing component height. Transformer core type is usually a ferrite material for high frequency applications.

Find a family of transformers that meet both the isolation and power level requirements of the application. The next step is to find a transformer within that family which is suitable for the application. The subsequent thought process for the transformer design will include :

- (1) Secondary turns (N_S), core losses, temperature rise, flux density, switching frequency
- (2) Primary turns (N_P), maximum duty cycle and reset voltages
- (3) Copper losses

The expression for secondary turns (N_S) is given by,

$$N_S = 10^8 V_{OUT} / (f_{OSC} \cdot A_C \cdot B_M)$$

where,

A_C = cross-sectional area of the core in cm^2

B_M = maximum AC flux density desired

For flux density, choose a level which achieves an acceptable level of core loss/temperature rise at a given switching frequency. The transformer data sheet will provide curves of core loss versus flux density at various switching frequencies. The data sheet will also provide temperature rise versus core loss. While choosing a value for B_M to avoid excessive core losses will usually allow enough headroom for flux swing during input / load transients, still make sure to stay well below the saturation flux density of the transformer core. If needed, increasing N_S will reduce flux

density. After calculating N_S , the number of primary turns (N_P) can be calculated from,

$$N_P = N_S \cdot D_{MAX} V_{IN(MIN)} / V_{OUT}$$

where,

$V_{IN(MIN)}$ = minimum system input voltage

D_{MAX} = maximum switch duty cycle at $V_{IN(MIN)}$ (typically chosen between 0.6 and 0.7)

At minimum input voltage the converter will run at a maximum duty cycle D_{MAX} . A higher transformer turns ratio (N_P/N_S) will create a higher D_{MAX} but it will also require higher voltages at the drain of the primary side switch to reset the transformer (see previous sections Lo side Active Clamp Topology and Hi side Active Clamp Topology). D_{MAX} values are typically chosen between 0.6 and 0.7. Even for a given D_{MAX} value, the loop must also provide protection against duty cycles that may excessively exceed D_{MAX} during transients or faults. While most converters only provide a fixed duty cycle clamp, the LT3752/LT3752-1 provide a programmable maximum duty cycle clamp D_{VSEC} that also moves inversely with input voltage.

The resulting function is that of a programmable volt-second clamp. This allows the user to choose a transformer turns ratio for D_{MAX} and then customize a maximum duty cycle clamp D_{VSEC} above D_{MAX} for safety. D_{VSEC} then follows the natural duty cycle of the converter as a safety guardrail (see previous section Programming Duty Cycle Clamp).

After deciding on the particular transformer and turns ratio, the copper losses can then be approximated by,

$$P_{CU} = D \cdot I(\text{Load})_{(MAX)}^2 (R_{SEC} + (N_S/N_P)^2 R_{PRI})$$

where,

D = switch duty cycle (choose nominal 0.5)

$I(\text{Load})_{(MAX)}$ = maximum load current

APPLICATIONS INFORMATION

R_{PRI} = primary winding resistance

R_{SEC} = secondary winding resistance

If there is a large difference between the core losses and the copper losses then the number of secondary turns can be adjusted to achieve a more suitable balance. The number of primary turns should then be recalculated to maintain the desired turns ratio.

Primary-Side Power MOSFET Selection

The selection of the primary-side N-channel power MOSFET M1 is determined by the maximum levels expected for the drain voltage and drain current. In addition, the power losses due to conduction losses, gate driver losses and transition losses will lead to a fine tuning of the MOSFET selection. If power losses are high enough to cause an unacceptable temperature rise in the MOSFET then several MOSFETs may be required to be connected in parallel.

The maximum drain voltage expected for the MOSFET M1 follows from the equations previously stated in the active clamp topology sections:

$$V_{DS}(M1) = V_{IN}^2 / (V_{IN} - (V_{OUT} \cdot N))$$

The MOSFET should be selected with a BV_{DSS} rating approximately 20% greater than the above steady state V_{DS} calculation due to tolerances in duty cycle, load transients, voltage ripple on C_{CL} and leakage inductance spikes. A MOSFET with the lowest possible voltage rating for the application should be selected to minimize switch on resistance for improved efficiency. In addition, the MOSFET should be selected with the lowest gate charge to further minimize losses.

MOSFET M1 losses at maximum output current can be approximated as :

$$P_{M1} = P_{CONDUCTION} + P_{GATEDRIVER} + P_{TRANSITION}$$

$$(i) P_{CONDUCTION} = (N_P/N_S) \cdot (V_{OUT}/V_{IN}) \cdot (N_S/N_P \cdot I_{OUT(MAX)})^2 \cdot R_{DS(ON)}$$

Note: The on resistance of the MOSFET, $R_{DS(ON)}$, increases with the MOSFET's junction temperature. $R_{DS(ON)}$ should therefore be recalculated once junction tem-

perature is known. A final value for $R_{DS(ON)}$ and therefore $P_{CONDUCTION}$ can be achieved from a few iterations.

$$(ii) P_{GATEDRIVER} = (Q_G \cdot INTV_{CC} \cdot f_{OSC})$$

where,

$$Q_G = \text{gate charge } (V_{GS} = INTV_{CC})$$

$$(iii) P_{TRANSITION} = P_{TURN_OFF} + P_{TURN_ON} (\approx 0 \text{ if ZVS})$$

$$(a) P_{TURN_OFF} = (1/2) I_{OUT(MAX)} (N_S/N_P) (V_{IN}/1-D) (Q_{GD}/I_{GATE}) \cdot f_{OSC}$$

where,

$$Q_{GD} = \text{gate to drain charge}$$

$$I_{GATE} = 2A \text{ source/sink for OUT pin gate driver}$$

$$(b) P_{TURN_ON} = (1/2) I_{OUT(MAX)} (N_S/N_P) (V_{DS}) (Q_{GD}/I_{GATE}) \cdot f_{OSC}$$

where,

$$V_{DS} = \text{M1 drain voltage at the beginning of M1 turn on}$$

$$V_{DS} \text{ typically sits between } V_{IN} \text{ and } 0V \text{ (ZVS)}$$

During programmable timing t_{AO} , negative I_{MAG} discharges M1 drain SWP towards V_{IN} (Figure 1). ZVS is achieved if enough leakage inductance exists—to delay the secondary side from clamping M1 drain to V_{IN} —and if enough energy is stored in L_{MAG} to discharge SWP to 0V during that delay. (see Programming Active Clamp Switch Timing: AOUT to OUT (t_{AO})).

Synchronous Control (SOUT)

The LT3752 / LT3752-1 use the SOUT pin to communicate synchronous control information to the secondary side synchronous rectifier controller (Figure 19). The isolating transformer (T_{SYNC}), coupling capacitor (C_{SYNC}) and resistive load (R_{SYNC}) allow the ground referenced SOUT signal to generate positive and negative signals required at the SYNC input of the secondary side synchronous rectifier controller. For the typical LT3752/LT3752-1 applications operating with an LT8311, C_{SYNC} is 220pF, R_{SYNC} is 560Ω and T_{SYNC} is typically a PULSE PE-68386NL.

APPLICATIONS INFORMATION

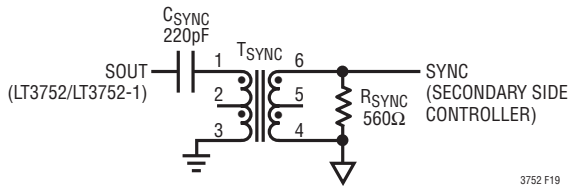


Figure 19. SOUT Pulse Transformer

Typically choose C_{SYNC} between 220pF and 1nF. R_{SYNC} should then be chosen to obey :

$$(1) SOUT_{MAX}/100mA \leq R_{SYNC} \leq \sqrt{L_{MAG}/C_{SYNC}}$$

where,

$$SOUT_{MAX} = INTV_{CC}$$

$$L_{MAG} = T_{SYNC}'s \text{ magnetizing inductance}$$

$$100mA = SOUT \text{ gate driver minimum source current}$$

and

$$(2) R_{SYNC} \cdot C_{SYNC} \geq (-1) \cdot Y / (\ln(Z/SOUT_{MAX}))$$

where,

$$Y = SYNC \text{ minimum pulse duration (50ns; LT8311)}$$

$$Z = |SYNC \text{ level to achieve } Y| (\pm 2V; LT8311)$$

Even though the LT3752/LT3752-1 $INTV_{CC}$ pin is allowed to be over driven by as much as 15.4V using the house-keeping supply, $SOUT_{MAX}$ level should be designed to not cause T_{SYNC} output to exceed the maximum ratings of the LT8311's SYNC pin.

Cost/Space reduction : If discontinuous conduction mode (DCM) operation is acceptable at light load, the LT8311 has a preactive mode which controls the synchronous MOSFETs without T_{SYNC} , C_{SYNC} , R_{SYNC} or the LT3752/LT3752-1 timing resistors R_{TAS} , R_{TOS} (leave open).

Output Inductor Value

The choice of output inductor value L_{OUT} will depend on the amount of allowable ripple current. The inductor ripple current is given by:

$$I_{L(RIPPLE)(P-P)} = \Delta I_L = (V_{OUT}/(L_{OUT} \cdot f_{OSC})) \cdot (1 - (V_{OUT}/V_{IN})(N_P/N_S))$$

The LT3752/LT3752-1 allow very large ΔI_L values (low L_{OUT} values) without the worry of insufficient slope compensation—by allowing slope compensation to be programmed with an external resistor in series with the I_{SENSE} pin (see Current Sensing and Programmable Slope Compensation).

Larger ΔI_L will allow lower L_{OUT} , reducing component size, but will also cause higher output voltage ripple and core losses. For LT3752/LT3752-1 applications, ΔI_L is typically chosen to be 40% of $I_{OUT(MAX)}$.

Output Capacitor Selection

The choice of output capacitor value is dependent on output voltage ripple requirements given by :

$$\Delta V_{OUT} \approx \Delta I_L (ESR + (1/(8 \cdot f_{OSC} \cdot C_{OUT})))$$

where,

$$\Delta I_L = \text{output inductor ripple current } I_{L(RIPPLE)(P-P)}$$

$$ESR = \text{effective series resistance (of } C_{OUT})$$

$$f_{OSC} = \text{switching frequency}$$

$$C_{OUT} = \text{output capacitance}$$

This gives:

$$C_{OUT} = \Delta I_L / (8 \cdot f_{OSC} \cdot (\Delta V_{OUT} - \Delta I_L \cdot ESR))$$

Typically C_{OUT} is made up of a low ESR ceramic capacitor(s) to minimize ΔV_{OUT} . Additional bulk capacitance is added in the form of electrolytic capacitors to minimize output voltage excursions during load steps.

Input Capacitor Selection

The active clamp forward converter demands pulses of current from the input due to primary winding current and magnetizing current. The input capacitor is required to provide high frequency filtering to achieve an input voltage as close as possible to a pure DC source with low ripple voltage. For low impedance input sources and medium to low voltage input levels, a simple ceramic capacitor with low ESR should suffice. It should be rated to operate at a worst case RMS input current of :

$$I_{CIN(RMS)} = (N_S/N_P) I_{OUT(MAX)}/2$$

APPLICATIONS INFORMATION

A small 1 μ F bypass capacitor should also be placed close to the IC between V_{IN} and GND.

As input voltage levels increase, any use of bulk capacitance to minimize input ripple can impact on solution size and cost. In addition, inputs with higher source impedance will cause an increase in voltage ripple. In these applications it is recommended to include an LC input filter. The output impedance of the input filter should remain below the negative input impedance of the DC/DC forward converter.

PCB Layout / Thermal Guidelines

For proper operation, PCB layout must be given special attention. Critical programming signals must be able to co-exist with high dv/dt signals. Compact layout can be achieved but not at the cost of poor thermal management. The following guidelines should be followed to approach optimal performance.

1. Ensure that a local bypass capacitor is used (and placed as close as possible) between V_{IN} and GND for the controller IC(s).
2. The critical programming resistors for timing (pins T_{AO} , T_{AS} , T_{OS} , T_{BLNK} , $IVSEC$ and RT) must use short traces to each pin. Each resistor should also use a short trace to connect to a single ground bus specifically connected to pin 18 of the IC (GND).
3. The current sense resistor for the forward converter must use short Kelvin connections to the I_{SENSEP} and I_{SENSEN} pins. The current sense resistor for the housekeeping supply should have its ground connection as close as possible to the power ground (PGND) pin 38.
4. High dv/dt lines should be kept away from all timing resistors, current sense inputs, HCOMP/COMP pins, UVLO_VSEC/OVLO pins and both HFB and FB feedback traces.
5. Gate driver traces (HOUT, AOUT, SOUT, OUT) should be kept as short as possible.
6. When working with high power components, multiple parallel components are the best method for spreading out power dissipation and minimizing temperature rise. In particular, multiple copper layers connected by vias should be used to sink heat away from each power MOSFET.
7. Keep high switching current PGND paths away from signal ground. Also minimize trace lengths for those high current switching paths to minimize parasitic inductance.

APPLICATIONS INFORMATION

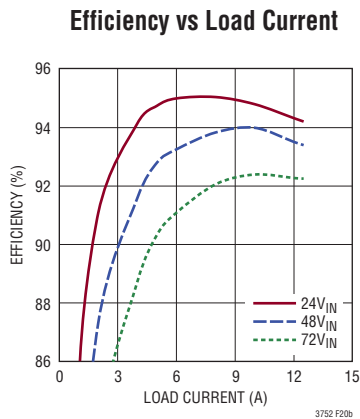
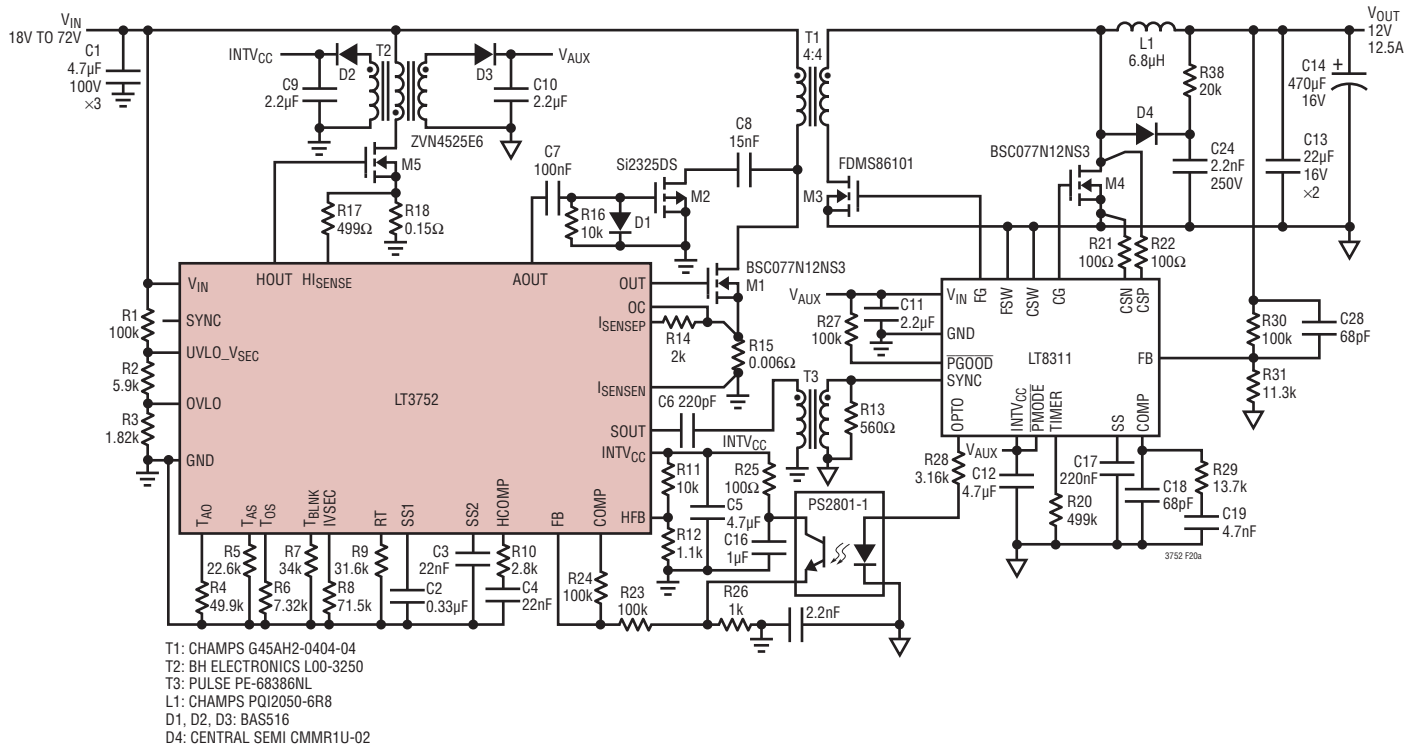
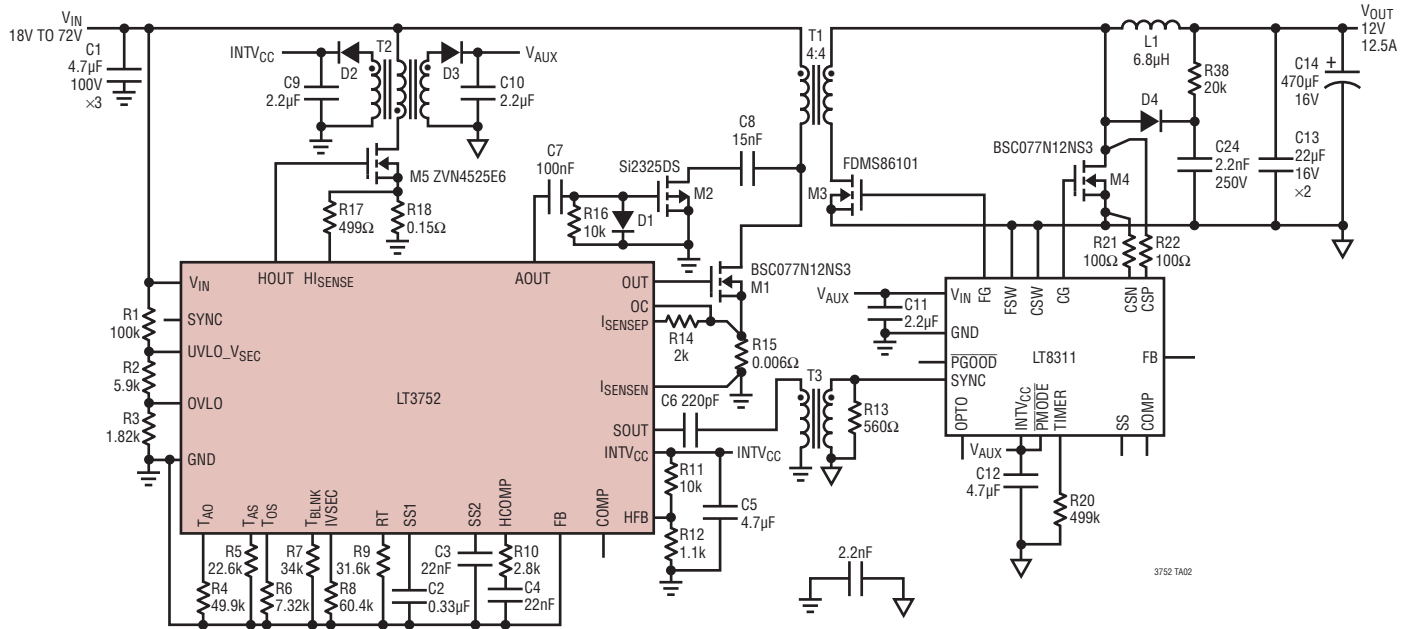


Figure 20. 18V to 72V, 12V/12.5A, 150W Active Clamp Isolated Forward Converter

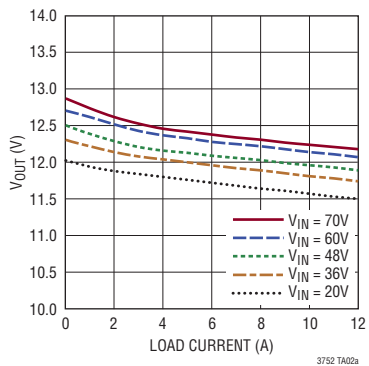
TYPICAL APPLICATIONS

18V to 72V, 12V/12.5A, 150W No-Opto, Active Clamp Isolated Forward Converter

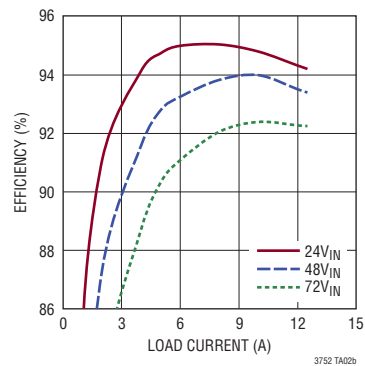


T1: CHAMPS G45AH2-0404-04
 T2: BH ELECTRONICS L00-3250
 T3: PULSE PE-68386NL
 L1: CHAMPS PQI2050-6R8
 D1, D2, D3: BAS516
 D4: CENTRAL SEMI CMMR1U-02

V_{OUT} vs Load Current (No-Opto)

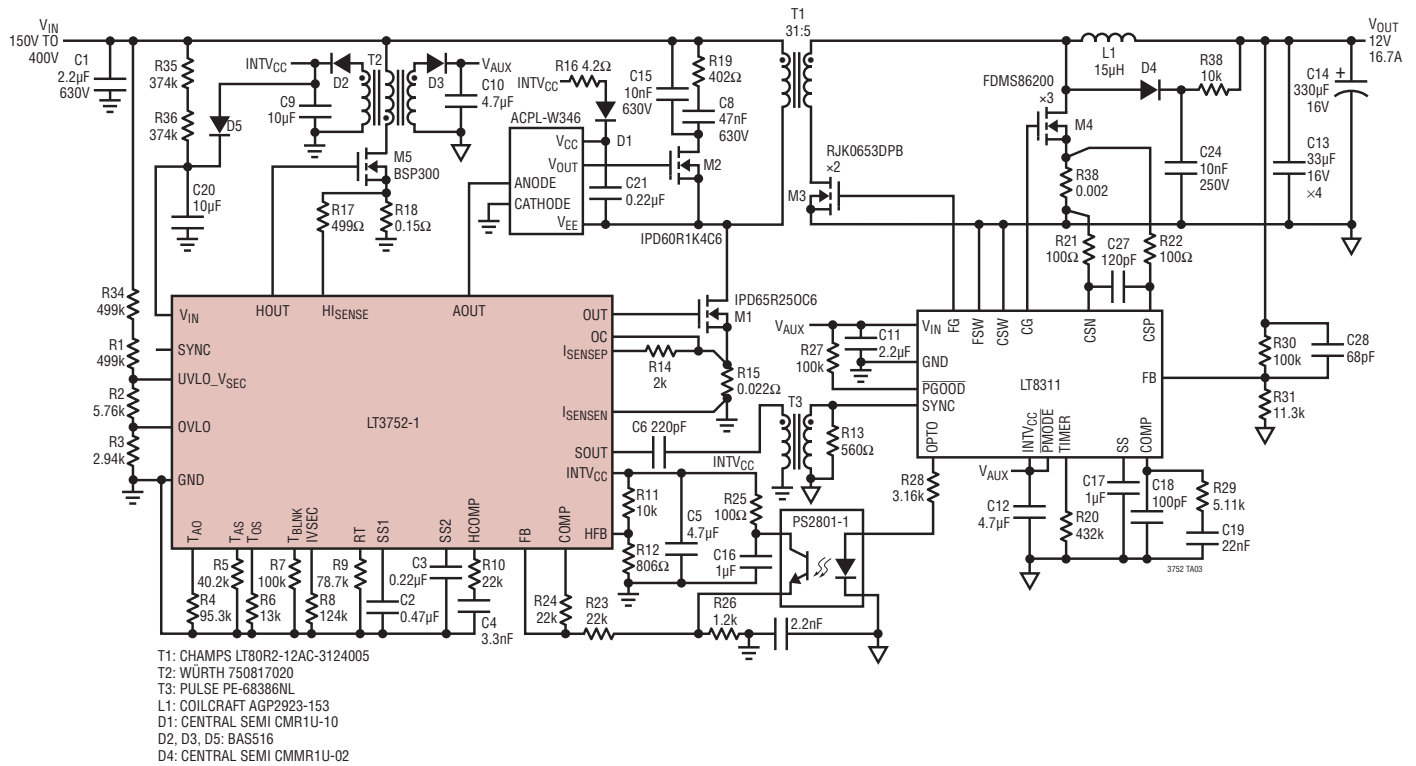


Efficiency vs Load Current

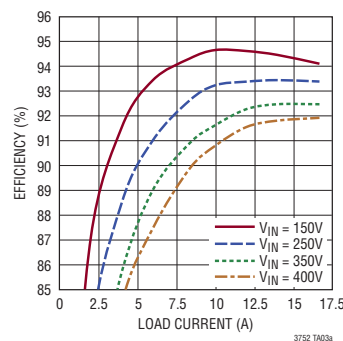


TYPICAL APPLICATIONS

150V to 400V, 12V/16.7A, 200W Active Clamp Isolated Forward Converter



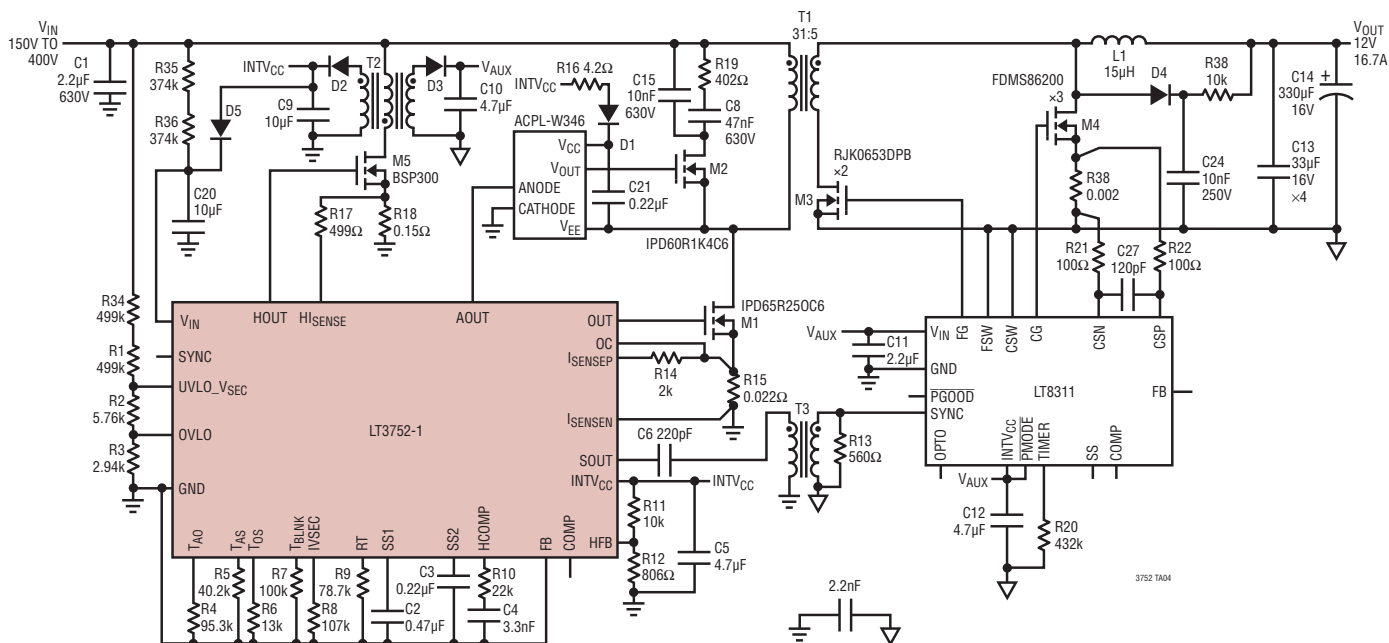
Efficiency vs Load Current



LT3752/LT3752-1

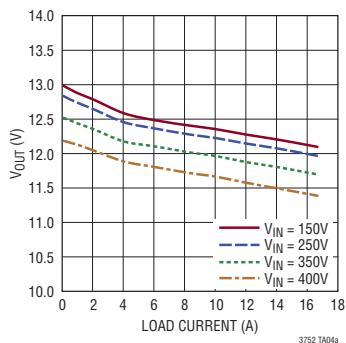
TYPICAL APPLICATIONS

150V to 400V, 12V/16.7A, 200W No-Opto, Active Clamp Isolated Forward Converter

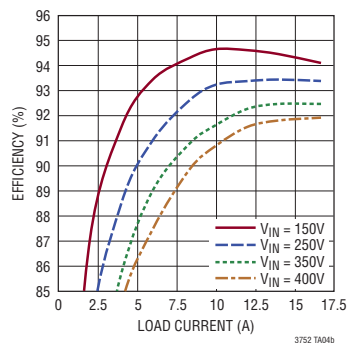


T1: CHAMPS LT80R2-12AC-3124005
 T2: WÜRTH 750817020
 T3: PULSE PE-68386NL
 L1: COILCRAFT AGP2923-153
 D1: CENTRAL SEMI CMR1U-10
 D2, D3, D5: BAS516
 D4: CENTRAL SEMI CMMR1U-02

V_{OUT} vs Load Current (No-Opto)

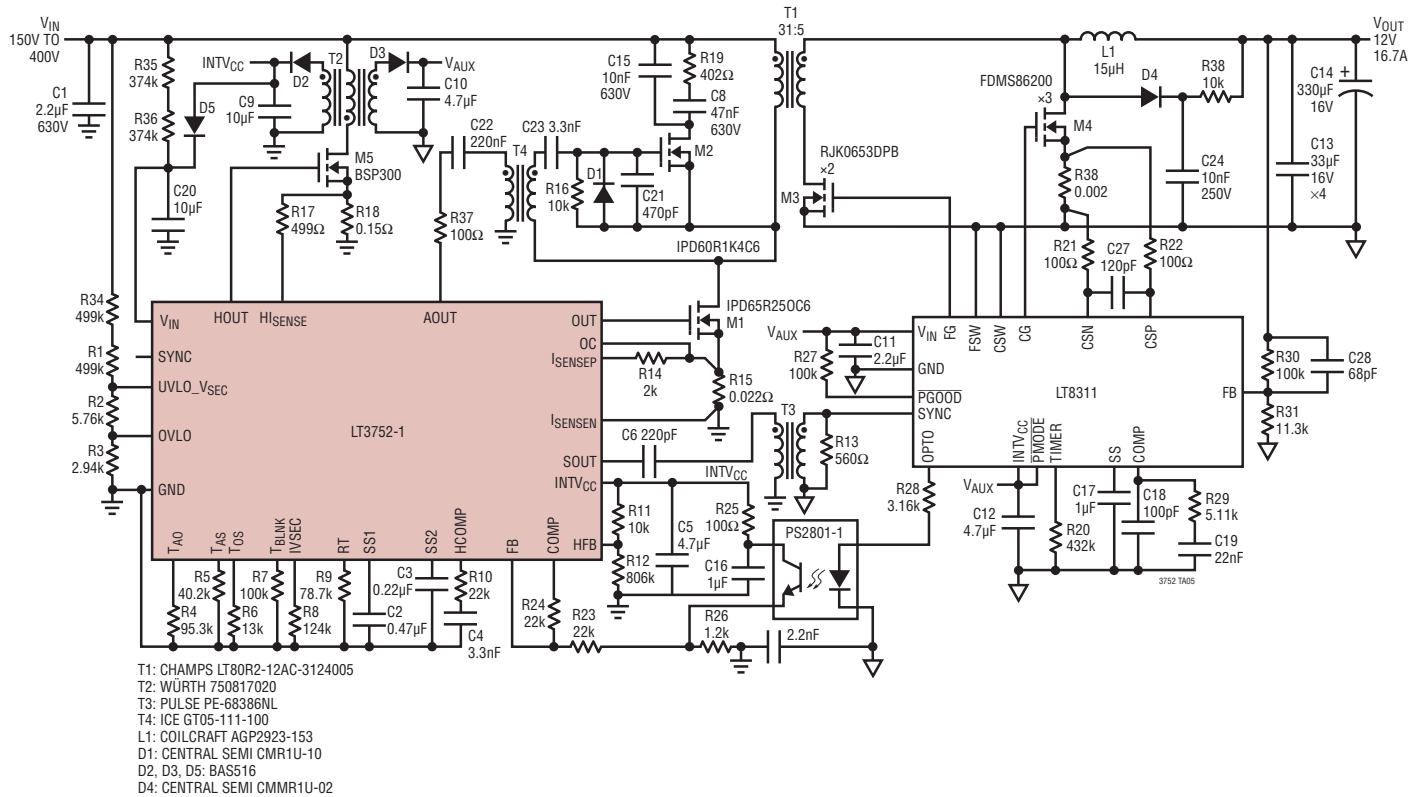


Efficiency vs Load Current

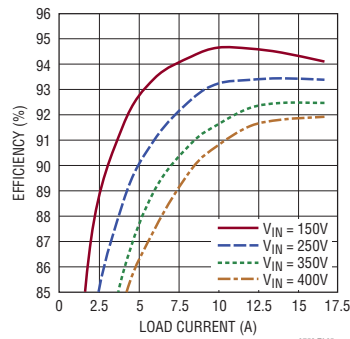


TYPICAL APPLICATIONS

150V to 400V, 12V/16.7A, 200W, Active Clamp Isolated Forward Converter (Using Gate Drive Transformer for High Side Active Clamp)

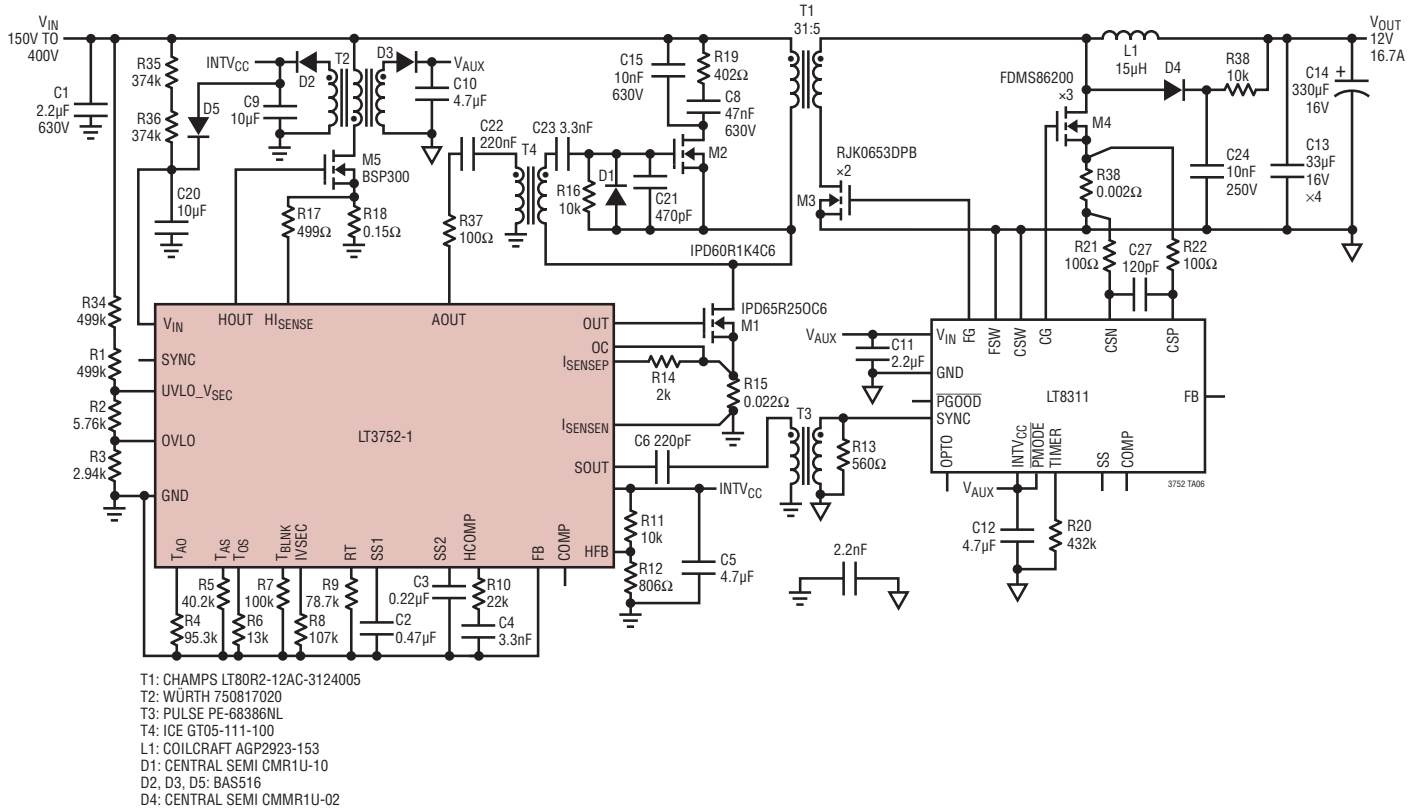


Efficiency vs Load Current

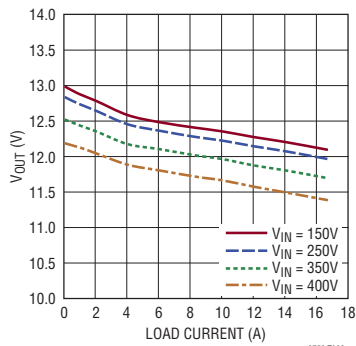


TYPICAL APPLICATIONS

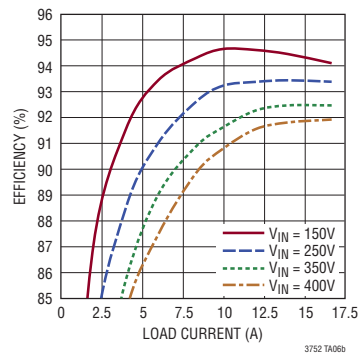
150V to 400V, 12V/16.7A 200W, No-Opto, Active Clamp Isolated Forward Converter (Using Gate Drive Transformer for High Side Active Clamp)



V_{OUT} vs Load Current (No-Opto)

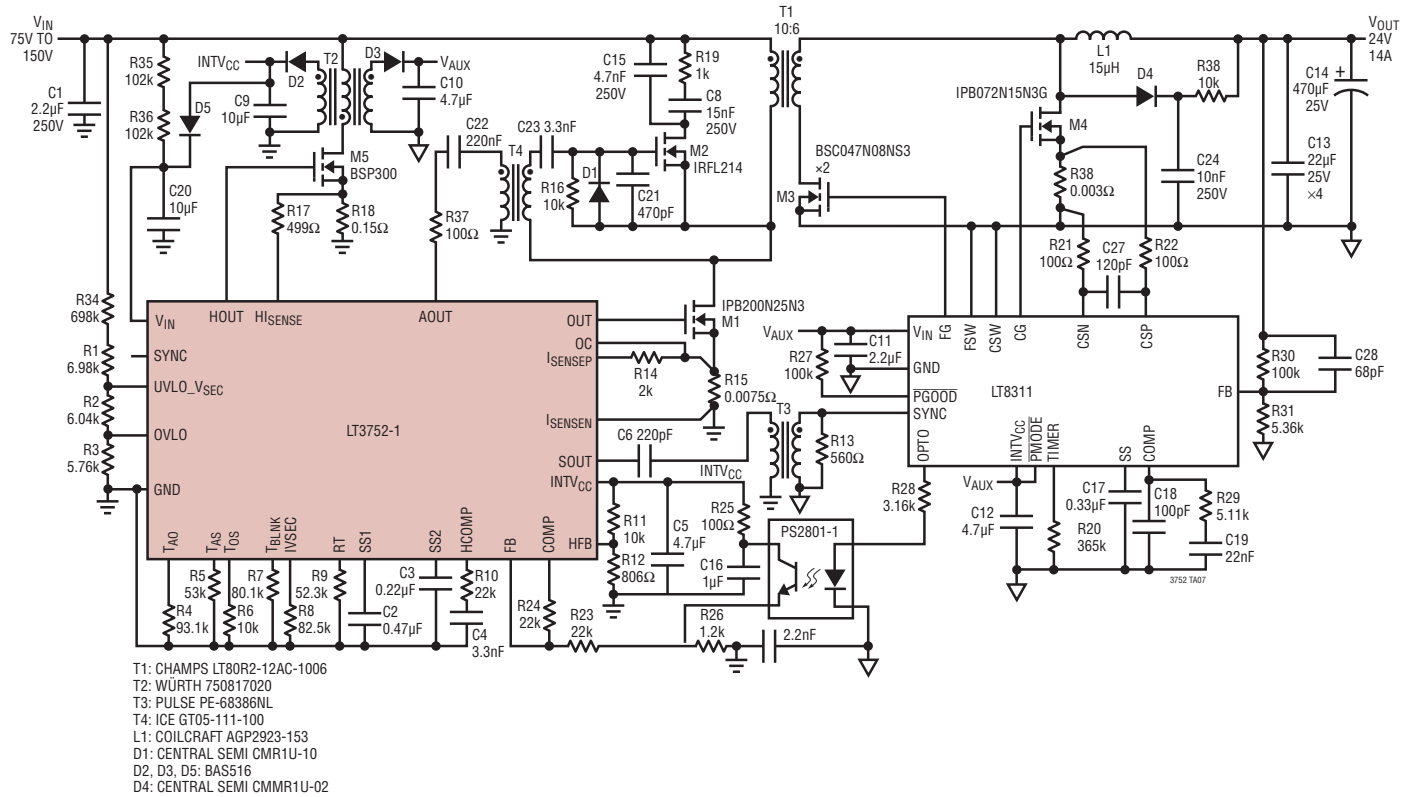


Efficiency vs Load Current

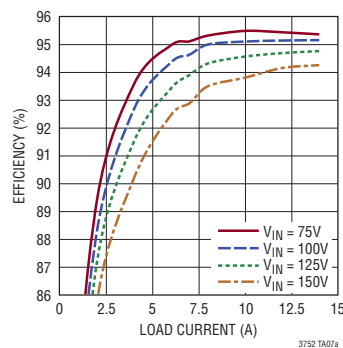


TYPICAL APPLICATIONS

75V to 150V, 24V/14A 340W Active Clamp Isolated Forward Converter (Using Gate Drive Transformer for High Side Active Clamp)



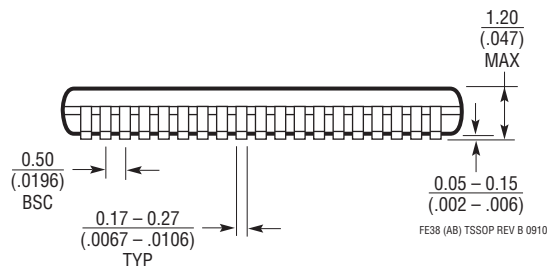
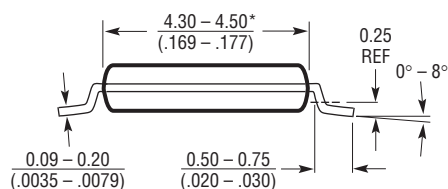
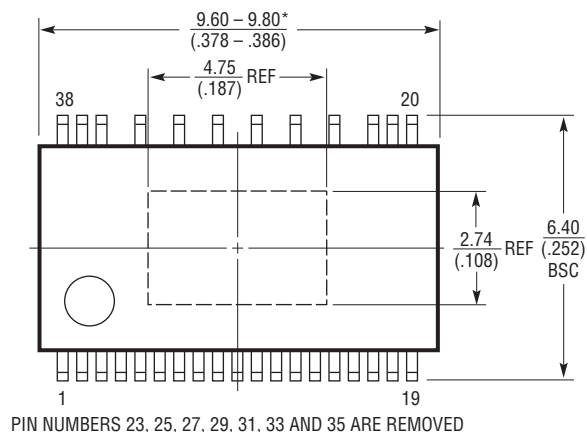
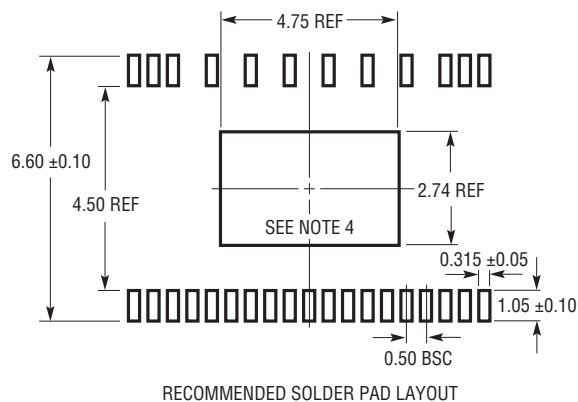
Efficiency vs Load Current



PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

FE Package
Package Variation: FE38 (31)
38-Lead Plastic TSSOP (4.4mm)
 (Reference LTC DWG # 05-08-1665 Rev B)
Exposed Pad Variation AB



NOTE:

1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE

4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

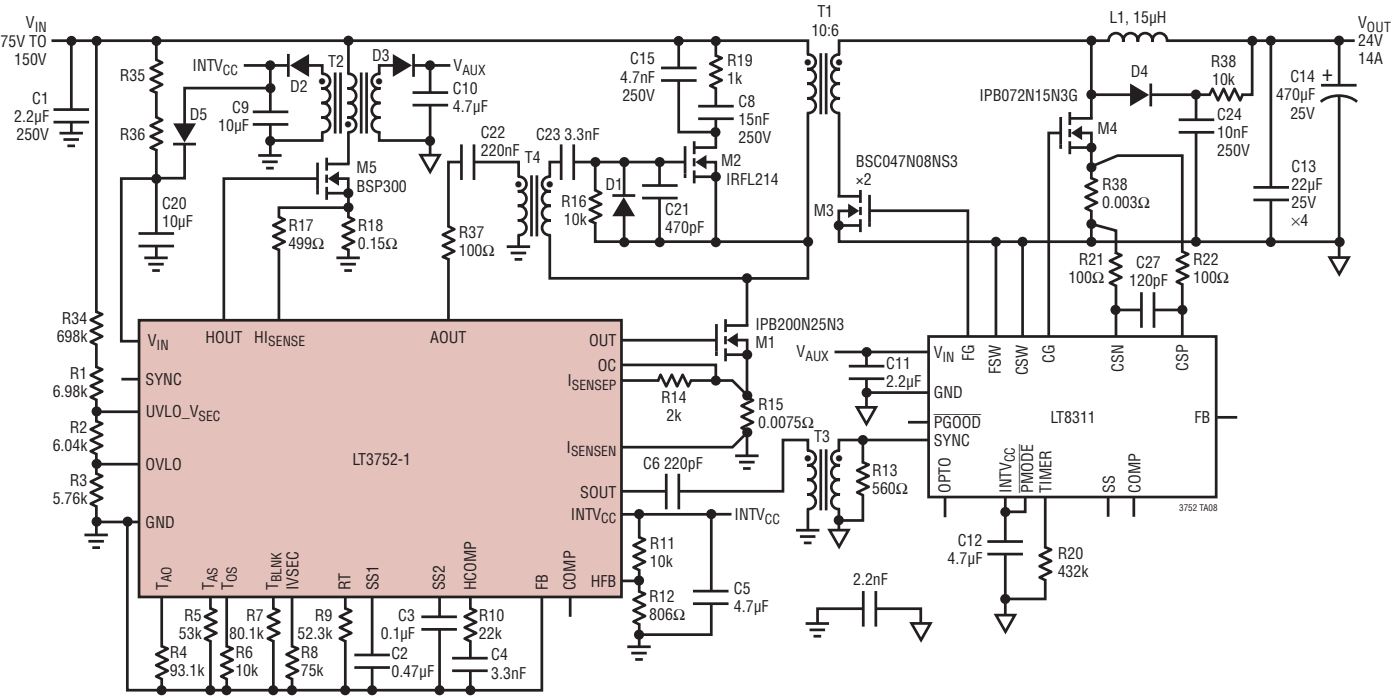
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/14	Minor typographical changes throughout data sheet.	All
B	07/15	Changed Absolute Maximum SS2 rating to 16V.	3
		Changed Absolute Maximum SS1 rating to 3V.	3
		Changed Output Low Level in Shutdown conditions to $INTV_{CC} = 3V$.	3
		Changed AOUT Rise and Fall Times.	5
		Changed SOUT Rise and Fall Times.	6
		Changed SS2 Discharge Current conditions to $SS2 = 2.5V$.	6
		Changed SS2 Charge Current conditions to $SS2 = 1.5V$.	6
		Changed HOUT Rise and Fall Times.	7

LT3752/LT3752-1

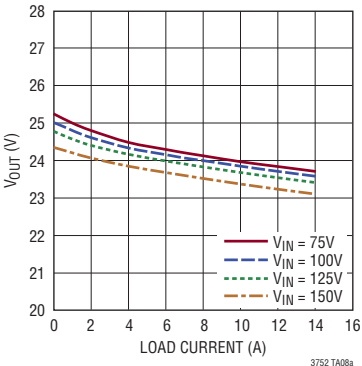
TYPICAL APPLICATION

75V to 150V, 24V/14A 340W No-Opto, Active Clamp Isolated Forward Converter

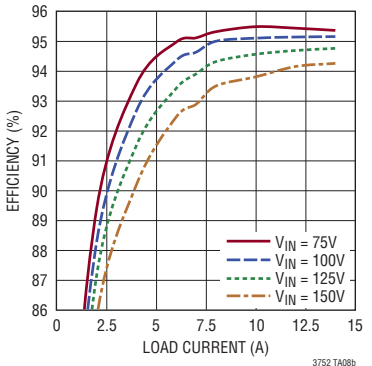


T1: CHAMPS LT80R2-12AC-1006
T2: WÜRTH 750817020
T3: PULSE PE-68386NL
T4: ICE GT05-111-100
L1: COILCRAFT AGP2923-153
D1: CENTRAL SEMI CMR1U-10
D2, D3, D5: BAS516
D4: CENTRAL SEMI CMMR1U-02

V_{OUT} vs Load Current (No-Opto)



Efficiency vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8311	Preactive Secondary Synchronous and Opto Control for Forward Converters	Optimized for Use with Primary-Side LT3752/-1, LT3753 and LT8310 Controllers
LTC3765/LTC3766	Synchronous No-Opto Forward Controller Chip Set with Active Clamp Reset	Direct Flux Limit, Supports Self Starting Secondary Forward Control
LTC3722/LTC3722-2	Synchronous Full Bridge Controllers	Adaptive or Manual Delay Control for Zero Voltage Switching, Adjustable Synchronous Rectification Timing
LT3748	100V Isolated Flyback Controller	5V ≤ V _{IN} ≤ 100V, No Opto Flyback, MSOP-16 with High Voltage Spacing
LT3798	Off-Line Isolated No-Opto Flyback Controller with Active PFC	V _{IN} and V _{OUT} Limited Only by External Components