19-0732; Rev 2; 12/10

EVALUATION KIT AVAILABLE

Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

MAX8662/MAX8663

General Description

The MAX8662/MAX8663 power-management ICs (PMICs) are efficient, compact devices suitable for smart cellular phones, PDAs, Internet appliances, and other portable devices. They integrate two synchronous buck regulators, a boost regulator driving two to seven white LEDs, four low-dropout linear regulators (LDOs), and a linear charger for a single-cell Li-ion (Li+) battery.

Maxim's Smart Power Selector™ (SPS) safely distributes power between an external power source (AC adapter, auto adapter, or USB source), battery, and the system load. When system load peaks exceed the external source capability, the battery supplies supplemental current. When system load requirements are small, residual power from the external power source charges the battery. A thermal-limiting circuit limits battery-charge rate and external power-source current to prevent overheating. The PMIC also allows the system to operate with no battery or a discharged battery.

The MAX8662 is available in a 6mm x 6mm, 48-pin TQFN package, while the MAX8663, without the LED driver, is available in a 5mm x 5mm, 40-pin TQFN package.

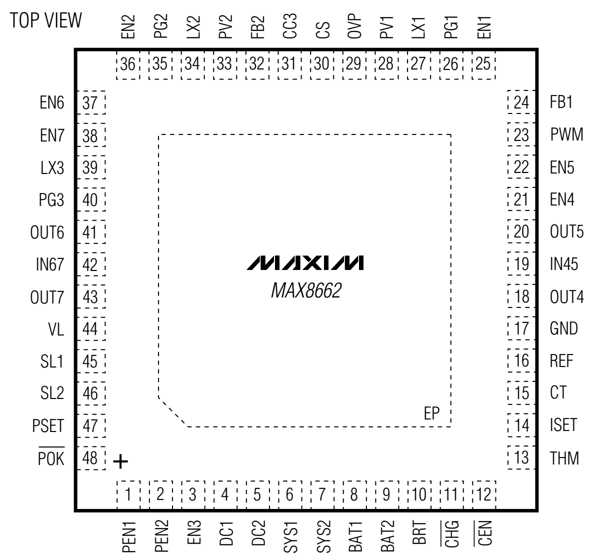
Applications

Smart Phones and PDAs

MP3 and Portable Media Players

Palmtop and Wireless Handhelds

Pin Configurations



TQFN
(6mm x 6mm)

Pin Configurations continued at end of data sheet.

Features

- ♦ **Two 95%-Efficient 1MHz Buck Regulators**
  - **Main Regulator: 0.98V to V_{IN} at 1200mA**
  - **Core Regulator: 0.98V to V_{IN} at 900mA**
- ♦ **1MHz Boost WLED Driver**
  - **Drives Up to 7 White LEDs at 30mA (max)**
  - **PWM and Analog Dimming Control**
- ♦ **Four Low-Dropout Linear Regulators**
  - **1.7V to 5.5V Input Range**
  - **15µA Quiescent Current**
- ♦ **Single-Cell Li+ Charger**
  - **Adapter or USB Input**
  - **Thermal-Overload Protection**
- ♦ **Smart Power Selector (SPS)**
  - **AC Adapter/USB or Battery Source**
  - **Charger-Current and System-Load Sharing**

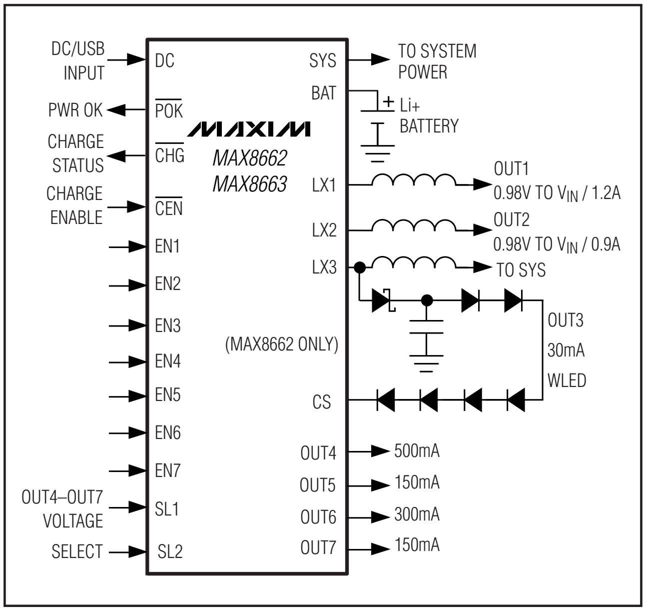
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8662ETM+	-40°C to +85°C	48 TQFN-EP* 6mm x 6mm x 0.8mm
MAX8663ETL+	-40°C to +85°C	40 TQFN-EP* 5mm x 5mm x 0.8mm

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

LX3 to GND ....-0.3V to +33V
DC_ to GND.....................................-0.3V to +9V
BAT_, $\overline{CEN}$, $\overline{CHG}$, EN_, PEN_, $\overline{POK}$, PV_, PWM,
SYS_, LX1, CS, LX2 to GND ....-0.3V to +6V
VL to GND ....-0.3V to +4V
BRT, CC3, FB_, IN45, IN67, OVP, REF,
SL_ to GND ....-0.3V to (V_{SYS} + 0.3V)
CT, ISET, PSET, THM to GND ....-0.3V to (V_{VL} + 0.3V)
OUT4, OUT5 to GND........................-0.3V to (V_{IN45} + 0.3V)
OUT6, OUT7 to GND........................-0.3V to (V_{IN67} + 0.3V)
PG_ to GND......................................-0.3V to +0.3V
BAT1 + BAT2 Continuous Current 3A
SYS1 + SYS2 Continuous Current (2 pins) 3A
LX_ Continuous Current 1.5A
Continuous Power Dissipation (T_A = +70°C)
40-Pin 5mm x 5mm TQFN
(derate 35.7mW/°C above +70°C)
(multilayer board)...2857mW
48-Pin 6mm x 6mm TQFN
(derate 37mW/°C above +70°C) (multilayer board)...2963mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature Range ....-40°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Input Limiter and Battery Charger)

(V_{DC} = 5V, V_{BAT} = 4V, $V_{\overline{CEN}}$ = 0V, $V_{PEN\_}$ = 5V, R_{PSET} = 3kΩ, R_{ISET} = 3.15kΩ, C_{CT} = 0.068µF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT LIMITER							
DC Operating Range	V_{DC}	(Note 2)		4.1		8.0	V
DC Undervoltage Threshold	V_{DC_L}	V_{DC} rising, 500mV hysteresis		3.9	4.0	4.1	V
DC Overvoltage Threshold	V_{DC_H}	V_{DC} rising, 100mV hysteresis		6.6	6.9	7.2	V
DC Supply Current		I_{SYS} = I_{BAT} = 0mA, $V_{\overline{CEN}}$ = 0V			1.5		mA
		I_{SYS} = I_{BAT} = 0mA, $V_{\overline{CEN}}$ = 5V			0.9		
DC Shutdown Current		V_{DC} = 5V, $V_{\overline{CEN}}$ = 5V, V_{PEN1} = V_{PEN2} = 0V (USB suspend mode)			110	180	µA
DC-to-SYS Dropout On-Resistance	R_{DC_SYS}	V_{DC} = 5V, I_{SYS} = 400mA, $V_{\overline{CEN}}$ = 5V			0.1	0.2	Ω
DC-to-BAT Dropout Threshold	$V_{DR\_DC\_BAT}$	When V_{SYS} regulation and charging stops, V_{DC} falling, 150mV hysteresis		20	50	85	mV
VL Voltage	V_{VL}	I_{VL} = 0 to 10mA		3.1	3.3	3.5	V
SYS Regulation Voltage	V_{SYS_REG}	V_{DC} = 5.8V, I_{SYS} = 1mA, $V_{\overline{CEN}}$ = 5V		5.2	5.3	5.4	V
DC Input Current Limit	I_{DC_LIM}	V_{DC} = 5V, V_{SYS} = 4.0V	V_{PEN1} = 5V, V_{PEN2} = 5V, R_{PSET} = 1.5kΩ	1800	2000	2200	mA
			V_{PEN1} = 5V, V_{PEN2} = 5V, R_{PSET} = 3kΩ	900	1000	1100	
			V_{PEN1} = 5V, V_{PEN2} = 5V, R_{PSET} = 6kΩ	450	500	550	
			V_{PEN1} = 0V, V_{PEN2} = 5V (500mA USB mode)	450	475	500	
			V_{PEN1} = V_{PEN2} = 0V (100mA USB mode)	80	90	100	
PSET Resistance Range	R_{PSET}	Guaranteed by SYS current limit		1.5		6.0	kΩ
Input Limiter Soft-Start Time	$T_{SS\_DC\_SYS}$	Current-limit ramp time			1.5		ms

ELECTRICAL CHARACTERISTICS (Input Limiter and Battery Charger) (continued)

(V_{DC} = 5V, V_{BAT} = 4V, $V_{\overline{CEN}}$ = 0V, $V_{PEN\_}$ = 5V, R_{PSET} = 3kΩ, R_{ISET} = 3.15kΩ, C_{CT} = 0.068µF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BATTERY CHARGER							
BAT-to-SYS On-Resistance	R_{BAT_REG}	V_{DC} = 0V, V_{BAT} = 4.2V, I_{SYS} = 1A			40	80	mΩ
BAT-to-SYS Reverse Regulation Voltage		V_{DC} = 5V, V_{PEN1} = V_{PEN2} = 0V (USB 100mA mode), I_{SYS} = 200mA (BAT to SYS voltage drop during SYS overload)		50	100	150	mV
BAT Regulation Voltage	V_{BAT_REG}	I_{BAT} = 0mA	T_A = +25°C	4.179	4.200	4.221	V
			T_A = -40°C to +85°C	4.158	4.200	4.242	
BAT Recharge Threshold		BAT voltage drop to restart charging		-140	-100	-60	mV
BAT Fast-Charge Current		I_{SYS} = 0mA, R_{PSET} = 1.5kΩ, V_{PEN1} = V_{PEN2} = 5V	R_{ISET} = 1.89kΩ		1250		mA
			R_{ISET} = 3.15kΩ	675	750	825	
			R_{ISET} = 7.87kΩ		300		
BAT Prequalification Current		V_{BAT} = 2.5V, R_{ISET} = 3.15kΩ (prequalification current is 10% of fast-charge current)			75		mA
ISET Resistance Range	R_{ISET}	Guaranteed by BAT charging current (1.5A to 300mA)		1.57		7.87	kΩ
V_{ISET}-to-I_{BAT} Ratio		R_{ISET} = 3.15kΩ (ISET output voltage to actual charge-current ratio)			2		V/A
Charger Soft-Start Time	t_{SS_CHG}	Charge-current ramp time			1.5		ms
BAT Prequalification Threshold		V_{BAT} rising, 180mV hysteresis		2.9	3.0	3.1	V
BAT Leakage Current		V_{BAT} = 4.2V, outputs disabled	V_{DC} = 0V		0.01	5	µA
			V_{DC} = $V_{\overline{CEN}}$ = 5V		0.01	5	
$\overline{CHG}$ and Top-Off Threshold		I_{BAT} where $\overline{CHG}$ goes high, and top-off timer; I_{BAT} falling (7.5% of fast-charge current)	R_{ISET} = 3.15kΩ		56.25		mA
Timer-Suspend Threshold		I_{BAT} falling (Note 3)		250	300	350	mV
Timer Accuracy		C_{CT} = 0.068µF		-20		+20	%
Prequalification Time	$t_{PREQUAL}$	From $\overline{CEN}$ high to end of prequalification charge, V_{BAT} = 2.5V, C_{CT} = 0.068µF			30		Min
Charge Time	$t_{FST-CHG}$	From $\overline{CEN}$ high to end of fast charge, C_{CT} = 0.068µF			300		Min
Top-Off Time	$t_{TOP-OFF}$	From $\overline{CHG}$ high to end of fast charge, C_{CT} = 0.068µF			30		Min
Charger Thermal-Limit Temperature		(Note 4)			100		°C
Charger Thermal-Limit Gain		R_{PSET} = 3kΩ			50		mA/°C

Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

ELECTRICAL CHARACTERISTICS (Input Limiter and Battery Charger) (continued)

(V_{DC} = 5V, V_{BAT} = 4V, $V_{\overline{CEN}}$ = 0V, $V_{PEN\_}$ = 5V, R_{PSET} = 3kΩ, R_{ISET} = 3.15kΩ, C_{CT} = 0.068µF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMISTOR INPUT (THM)						
THM Internal Pullup Resistance				10		kΩ
THM Resistance Threshold, Hot		Resistance falling (1% hysteresis)	3.73	3.97	4.21	kΩ
THM Resistance Threshold, Cold		Resistance rising (1% hysteresis)	26.98	28.7	30.42	kΩ
THM Resistance Threshold, Disabled		Resistance falling	270	300	330	Ω
LOGIC I/O ($\overline{POK}$, $\overline{CHG}$, PEN_, EN_, PWM, $\overline{CEN}$)						
Input Logic-High Level			1.3			V
Input Logic-Low Level					0.4	V
Logic Input-Leakage Current		V_{LOGIC} = 0V to 5.5V, T_A = +25°C	-1	+0.001	+1	µA
		V_{LOGIC} = 5.5V, T_A = +85°C		0.01		
Logic Output-Voltage Low		I_{SINK} = 1mA		10	100	mV
Logic Output-High Leakage Current		V_{LOGIC} = 5.5V, T_A = +25°C		0.001	1	µA
		V_{LOGIC} = 5.5V, T_A = +85°C		0.01		

ELECTRICAL CHARACTERISTICS (Output Regulator)

($V_{SYS\_}$ = $V_{PV\_}$ = V_{IN45} = V_{IN67} = 4.0V, V_{BRT} = 1.25V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM						
SYS Operating Range	V_{SYS}		2.6		5.5	V
SYS Undervoltage Threshold	V_{UVLO_SYS}	V_{SYS} rising, 100mV hysteresis	2.4	2.5	2.6	V
SYS Bias Current Additional Regulator Supply Current		Extra supply current when at least one output is on		35	70	µA
		Not including SYS bias current: OUT1 on, V_{PWM} = 0V		16	35	µA
		Not including SYS bias current: OUT2 on, V_{PWM} = 0V		16	35	µA
		Not including SYS bias current: OUT3 on		1	2	mA
		Not including SYS bias current: OUT4 on (current into IN45)		20	30	µA
		Not including SYS bias current: OUT5 on (current into IN45)		16	25	µA
		Not including SYS bias current: OUT6 on (current into IN67)		17	27	µA
		Not including SYS bias current: OUT7 on (current in IN67)		16	25	µA
Internal Oscillator Frequency		PWM frequency of OUT1, OUT2, and OUT3	0.9	1.0	1.1	MHz
BUCK REGULATOR 1						
Supply Current		I_{SYS} + I_{PV1}, no load, not including SYS bias current, V_{PWM} = 0V		16	35	µA
		I_{SYS} + I_{PV1}, no load, not including SYS bias current, V_{PWM} = 5V		2.9		mA
Output Voltage Range	V_{OUT1}	Guaranteed by FB accuracy	0.98		3.30	V
Maximum Output Current	I_{OUT1}		1200			mA

ELECTRICAL CHARACTERISTICS (Output Regulator) (continued)

($V_{SYS\_} = V_{PV\_} = V_{IN45} = V_{IN67}$ = 4.0V, V_{BRT} = 1.25V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FB Regulation Accuracy		From V_{FB1} = 0.98V, I_{OUT1} = 0 to 1200mA, V_{OUT1} = 0.98V to 3.3V		-3		+3	%
FB1 Input Leakage Current					0.01	0.10	µA
pMOS On-Resistance		I_{LX1} = 100mA	V_{PV1} = 3.3V		0.12	0.24	Ω
			V_{PV1} = 2.6V		0.15		
nMOS On-Resistance		I_{LX1} = 100mA	V_{PV1} = 3.3V		0.2	0.4	Ω
			V_{PV1} = 2.6V		0.3		
pMOS Current Limit				1.4	1.8	2.2	A
Skip Mode Transition Current					90		mA
nMOS Zero-Cross Current					25		mA
LX Leakage		V_{EN1} = 0V, V_{SYS} = 5.5V, T_A = +25°C	$V_{LX1} = V_{PV1}$ = 5.5V		0.01	1.00	µA
			V_{LX1} = 0V, V_{PV1} = 5.5V	-5.00	-0.01		
Soft-Start Time					400		µs
BUCK REGULATOR 2							
Supply Current		$I_{SYS} + I_{PV2}$, no load, not including SYS bias current	V_{PWM} = 0V		16	35	µA
			V_{PWM} = 5V		2.1		mA
Output Voltage Range		Guaranteed by FB accuracy		0.98		3.30	V
Maximum Output Current				900			mA
FB Regulation Accuracy		From V_{FB2} = 0.98V, I_{OUT2} = 0 to 600mA, V_{OUT2} = 0.98V to 3.3V		-3		+3	%
FB2 Input Leakage Current					0.01	0.10	µA
pMOS On-Resistance		I_{LX2} = 100mA	V_{PV2} = 3.3V		0.2	0.4	Ω
			V_{PV2} = 2.6V		0.3		
nMOS On- Resistance		I_{LX2} = 100mA	V_{PV2} = 3.3V		0.2	0.4	Ω
			V_{PV2} = 2.6V		0.3		
pMOS Current Limit				1.07	1.30	1.55	A
Skip Mode Transition Current					90		mA
nMOS Zero-Cross Current					25		mA
LX Leakage		V_{EN2} = 0V, V_{SYS} = 5.5V, T_A = +25°C	$V_{LX2} = V_{PV2}$ = 5.5V		0.01	1.00	µA
			V_{LX2} = 0V, V_{PV2} = 5.5V	-5.00	-0.01		
Soft-Start Time					400		µs
BOOST REGULATOR FOR LED DRIVER							
Supply Current		At SYS, no load, not including SYS bias current	Switching		1		mA
Output Range	V_{OUT3}			V_{SYS}		30	V
Minimum Duty Cycle	D_{MIN}				10		%
Maximum Duty Cycle	D_{MAX}			90	92		%
CS Regulation Voltage	V_{CS}			0.29	0.32	0.35	V
OVP Regulation Voltage		Duty = 90%, I_{LX3} = 0mA		1.225	1.250	1.275	V
OVP Sink Current				19.2	20.0	20.8	µA
OVP Soft-Start Period		Time for I_{OVP} to ramp from 0 to 20µA (Note 5)			1.25		ms

Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

ELECTRICAL CHARACTERISTICS (Output Regulator) (continued)

($V_{SYS\_} = V_{PV\_} = V_{IN45} = V_{IN67}$ = 4.0V, V_{BRT} = 1.25V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVP Leakage Current		V_{EN3} = 0V, $V_{OVP} = V_{SYS}$ = 5.5V	T_A = +25°C		0.01	1	µA
			T_A = +85°C		0.1		
nMOS On-Resistance		I_{LX3} = 100mA			0.6	1.2	Ω
nMOS Off-Leakage Current		V_{LX3} = 30V	T_A = +25°C		0.01	5.00	µA
			T_A = +85°C		0.1		
nMOS Current Limit				500	620	900	mA
LED DRIVER							
BRT Input Range	V_{BRT}	I_{CS} = 0 to 30mA		0		1.5	V
REF Voltage	V_{REF}	I_{REF} = 0mA		1.45	1.50	1.55	V
BRT Input Current		V_{BRT} = 0 to 1.5V	T_A = +25°C	-1	-0.01	+1	µA
			T_A = +85°C		0.1		
CS Sink Current		V_{CS} = 0.2V	V_{BRT} = 1.5V	28	30	32	mA
			V_{BRT} = 50mV	0.4	0.8	1.2	
CS Current-Source Line Regulation		V_{SYS} = 2.7V to 5.5V			0.1		%/V
PWM DIMMING							
EN3 DC Turn-On Delay		From V_{EN3} = high to LED on		1.5	2.0	2.5	ms
EN3 Shutdown Delay		From V_{EN3} = low to LED off		1.5	2.0	2.5	ms
PWM Dimming Capture Period		Time between rising edges on EN3 for PWM dimming to become active	Maximum	1.5	2.0		ms
			Minimum		8	10	µs
PWM Dimming Pulse-Width Resolution		Resolution of high or low-pulse width on EN3 for dimming change			0.5		µs
LINEAR REGULATORS							
IN45, IN67 Operating Range	V_{IN45}			1.7		5.5	V
IN45, IN67 Undervoltage Threshold	$V_{UVLO-IN45}$	V_{IN45} rising, 100mV hysteresis		1.5	1.6	1.7	V
Output Noise		f = 100Hz to 100kHz			200		$µV_{RMS}$
PSRR		f = 100kHz			30		dB
Shutdown Supply Current		$V_{EN4} = V_{EN5}$ = 0V, T_A = +25°C			0.001	1	µA
Soft-Start Ramp Time		V_{OUT4} to 90% of final value			34		V/ms
Output Discharge Resistance in Shutdown		V_{EN4} = 0V		0.5	1.0	2.0	kΩ
LINEAR REGULATOR 4 (LDO4)							
Supply Current		At IN45, V_{EN5} = 0V	I_{OUT4} = 0A		20	30	µA
Voltage Accuracy		I_{OUT4} = 0 to 500mA, $V_{IN45} = V_{OUT4}$ + 0.3V to 5.5V with 1.7V (min)		-1.5		+1.5	%
Minimum Output Capacitor	C_{OUT4}	Guaranteed stability, ESR < 0.05Ω		3.76			µF
Dropout Resistance		IN45 to OUT4			0.2	0.4	Ω
Current Limit		V_{OUT4} = 0V		500	700		mA

ELECTRICAL CHARACTERISTICS (OUTPUT REGULATOR) (continued)

($V_{SYS\_} = V_{PV\_} = V_{IN45} = V_{IN67}$ = 4.0V, V_{BRT} = 1.25V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATOR 5 (LDO5)							
Supply Current		At IN45, V_{EN4} = 0V	I_{OUT5} = 0A		16	25	µA
Voltage Accuracy		I_{OUT5} = 0 to 150mA, $V_{IN45} = V_{OUT5}$ + 0.3V to 5.5V with 1.7V (min)		-1.5		+1.5	%
Minimum Output Capacitor	C_{OUT5}	Guaranteed stability, ESR < 0.05Ω		0.8			µF
Dropout Resistance		IN45 to OUT5			0.6	1.2	Ω
Current Limit		V_{OUT5} = 0V		150	210		mA
LINEAR REGULATOR 6 (LDO6)							
Supply Current		At IN67, $V_{EN6} = V_{SYS}$, V_{EN7} = 0V	I_{OUT6} = 0A		17	27	µA
Voltage Accuracy		I_{OUT6} = 0 to 300mA, $V_{IN67} = V_{OUT6}$ + 0.3V to 5.5V		-1.5		+1.5	%
Minimum Output Capacitor	C_{OUT6}	Guaranteed stability, ESR < 0.05Ω		1.76			µF
Dropout Resistance		IN67 to OUT6			0.35	0.60	Ω
Current Limit		V_{OUT6} = 0V		300	420		mA
LINEAR REGULATOR 7 (LDO7)							
Supply Current		At IN67, V_{EN6} = 0V, $V_{EN7} = V_{SYS}$	I_{OUT7} = 0A		16	25	µA
Voltage Accuracy		I_{OUT7} = 0 to 150mA, $V_{IN67} = V_{OUT7}$ + 0.3V to 5.5V with 1.7V (min)		-1.5		+1.5	%
Minimum Output Capacitor	C_{OUT7}	Guaranteed stability, ESR < 0.05Ω		0.8			µF
Dropout Resistance		IN67 to OUT6			0.6	1.2	Ω
Current Limit		V_{OUT7} = 0V		150	210		mA
THERMAL SHUTDOWN							
Thermal-Shutdown Temperature		T_J rising			165		°C
Thermal-Shutdown Hysteresis					15		°C

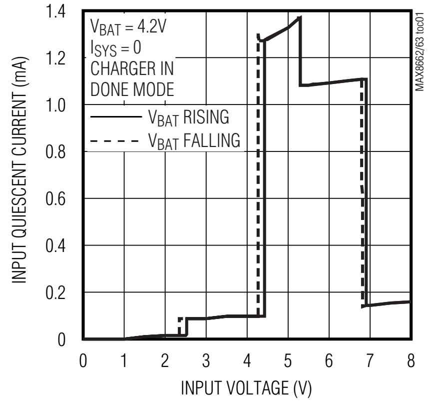
Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.
Note 2: Input withstand voltage. Not designed to operate above V_{DC} = 6.5V due to thermal-dissipation issues.
Note 3: ISET voltage when CT timer stops. Occurs only when in constant-current mode. Translates to 20% of fast-charge current.
Note 4: Temperature at which the input current limit begins to reduce.
Note 5: The WLED driver's sink current ramp time is a function of the external compensation at CC3. With a compensation of 1kΩ in series with 0.22µF and a target sink current of 30mA, the WLED boost's output voltage ramps up in 1.25ms, but the WLED sink current of 30mA settles in 12ms. See the OUT3 Enable and Disable Response graph in the *Typical Operating Characteristics* section for more information.

Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

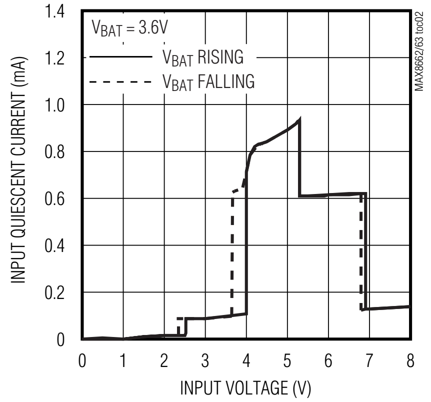
Typical Operating Characteristics

(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

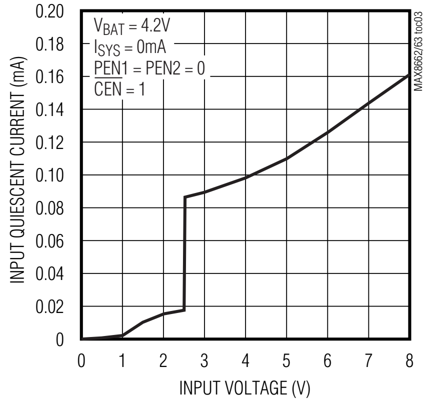
INPUT QUIESCENT CURRENT vs. INPUT VOLTAGE (CHARGER ENABLED)



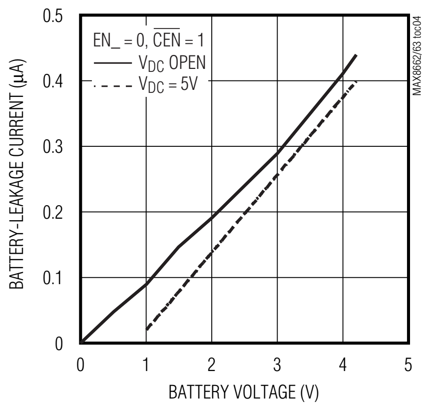
INPUT QUIESCENT CURRENT vs. INPUT VOLTAGE (CHARGER DISABLED)



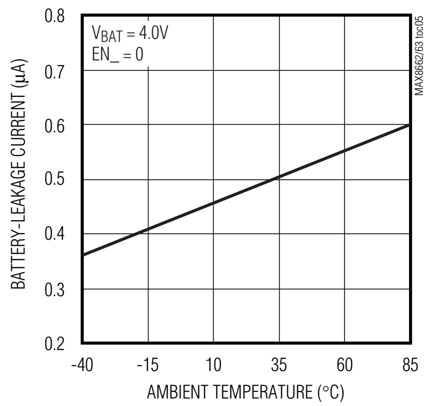
INPUT QUIESCENT CURRENT vs. INPUT VOLTAGE (SUSPEND)



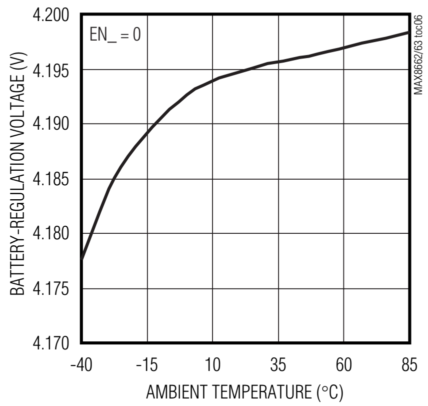
BATTERY-LEAKAGE CURRENT vs. BATTERY VOLTAGE



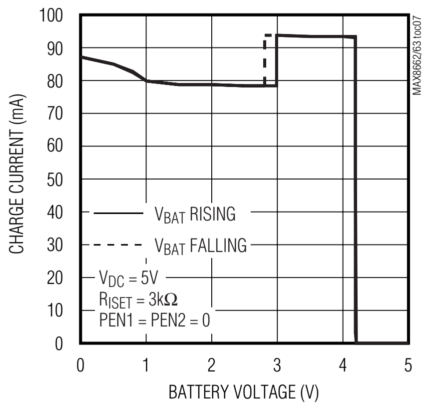
BATTERY-LEAKAGE CURRENT vs. TEMPERATURE (INPUT DISCONNECTED)



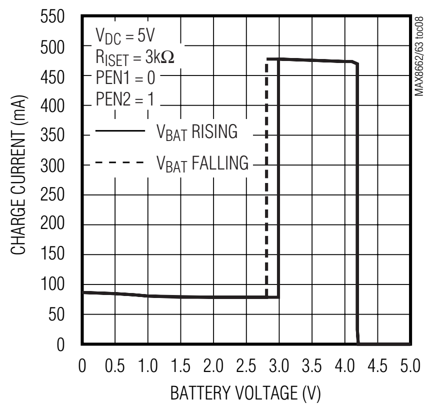
BATTERY-REGULATION VOLTAGE vs. TEMPERATURE



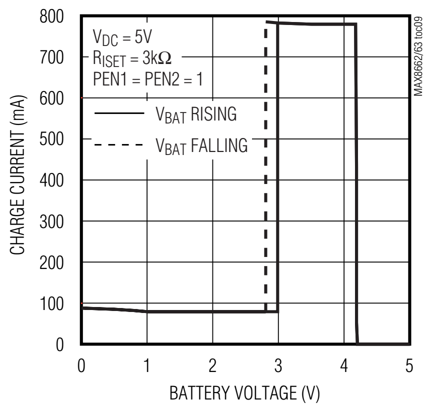
CHARGE CURRENT vs. BATTERY VOLTAGE (100mA USB)



CHARGE CURRENT vs. BATTERY VOLTAGE (500mA USB)



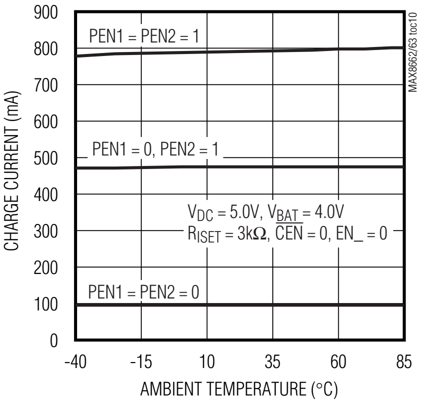
CHARGE CURRENT vs. BATTERY VOLTAGE (AC ADAPTER)



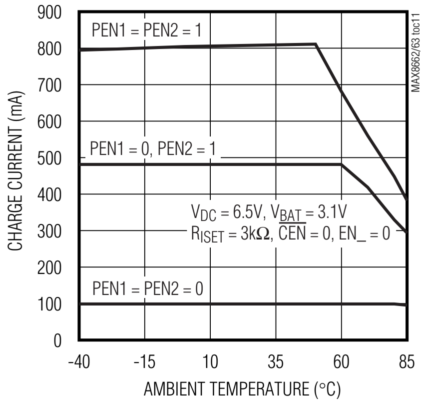
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10μF, C_{OUT2} = 2 x 10μF, C_{OUT3} = 0.1μF, C_{OUT4} = 4.7μF, C_{OUT5} = 1μF, C_{OUT6} = 2.2μF, C_{OUT7} = 1μF, CT = 0.068μF, C_{REF} = C_{VL} = 0.1μF, R_{THM} = 10kΩ, L1 = 3.3μH, L2 = 4.7μH, L3 = 22μH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

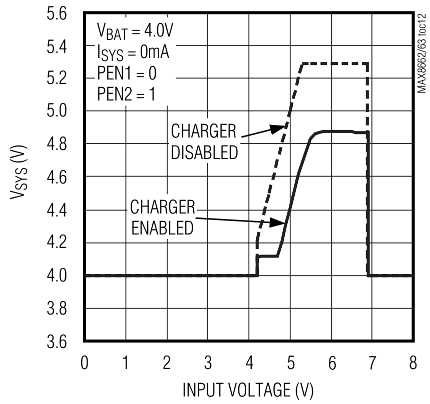
CHARGE CURRENT vs. AMBIENT TEMPERATURE (LOW IC POWER DISSIPATION)



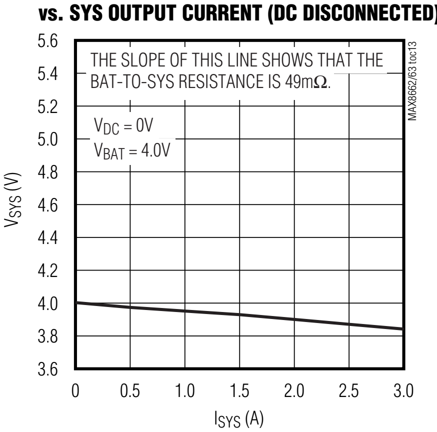
CHARGE CURRENT vs. AMBIENT TEMPERATURE (HIGH IC POWER DISSIPATION)



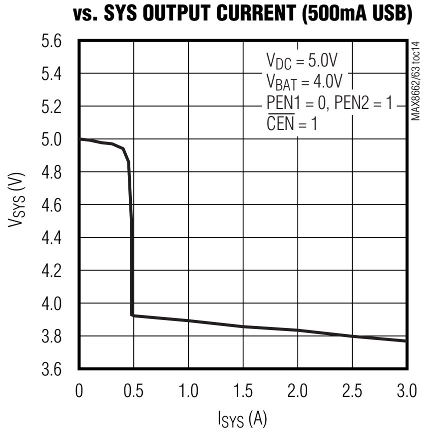
SYS OUTPUT VOLTAGE vs. INPUT VOLTAGE



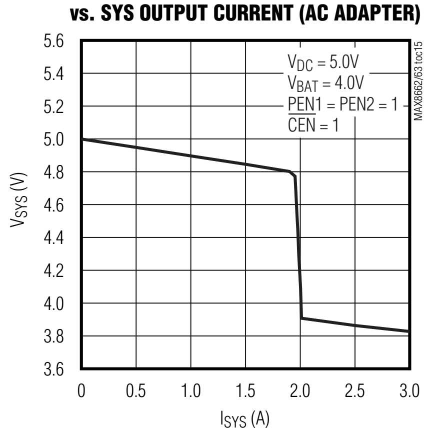
SYS OUTPUT VOLTAGE vs. SYS OUTPUT CURRENT (DC DISCONNECTED)



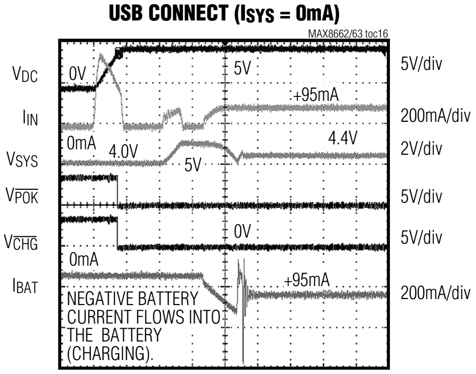
SYS OUTPUT VOLTAGE vs. SYS OUTPUT CURRENT (500mA USB)



SYS OUTPUT VOLTAGE vs. SYS OUTPUT CURRENT (AC ADAPTER)



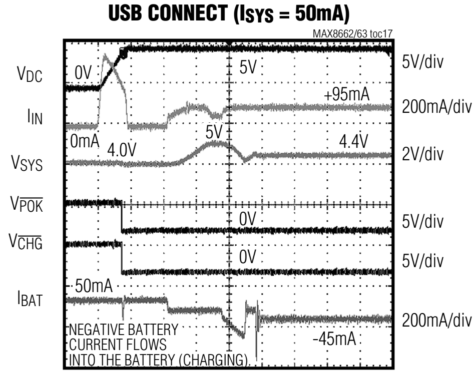
USB CONNECT (I_{SYS} = 0mA)



200μs/div

PEN1 = PEN2 = 0, $\overline{CEN}$ = 0,
V_{BAT} = 4.0V, I_{SYS} = 0mA, EN_ = 1

USB CONNECT (I_{SYS} = 50mA)



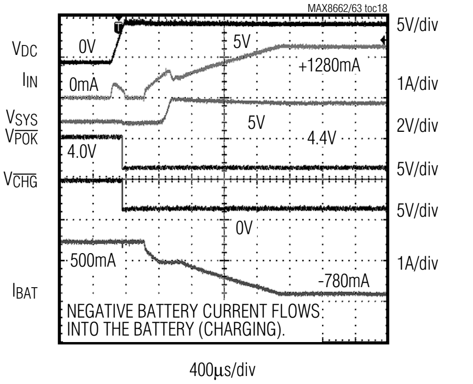
200μs/div

PEN1 = PEN2 = 0, $\overline{CEN}$ = 0,
V_{BAT} = 4.0V, I_{SYS} = 50mA, EN_ = 1

Typical Operating Characteristics (continued)

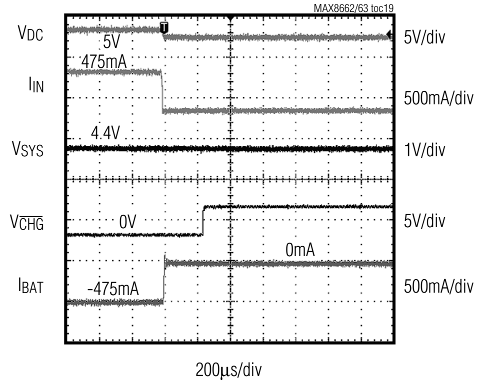
(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

AC ADAPTER CONNECT (I_{SYS} = 500mA)



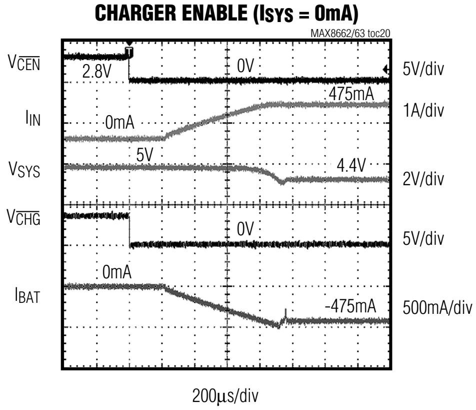
PEN1 = PEN2 = 1, $\overline{CEN}$ = 0,
V_{BAT} = 4.0V, I_{SYS} = 500mA, EN_ = 1

USB DISCONNECTED (500mA USB)



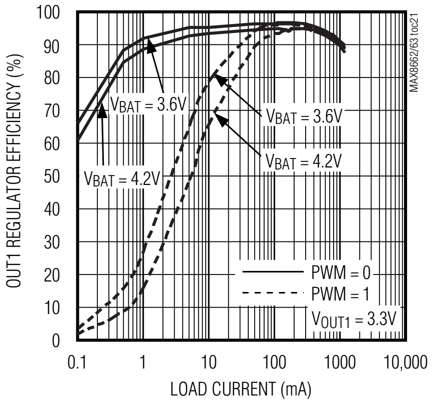
PEN1 = 0, PEN2 = 1, $\overline{CEN}$ = 0,
V_{BAT} = 4.0V, I_{SYS} = 0mA

CHARGER ENABLE (I_{SYS} = 0mA)

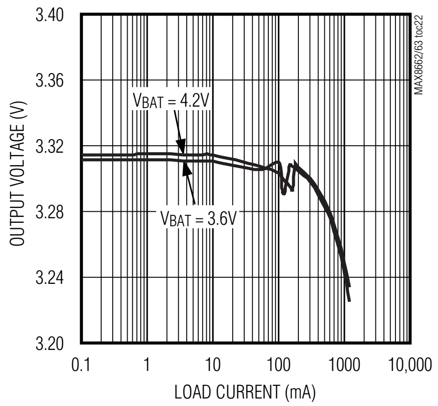


PEN1 = 0, PEN2 = 1, V_{BAT} = 4.0V, I_{SYS} = 0mA, EN_ = 1

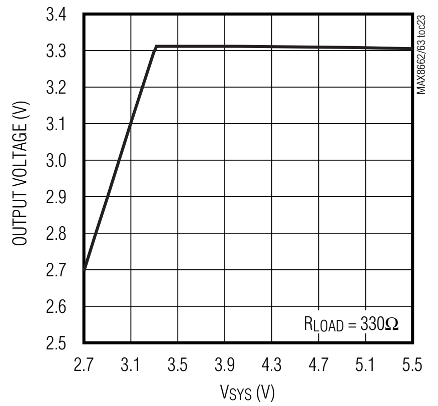
OUT1 REGULATOR EFFICIENCY vs. LOAD CURRENT



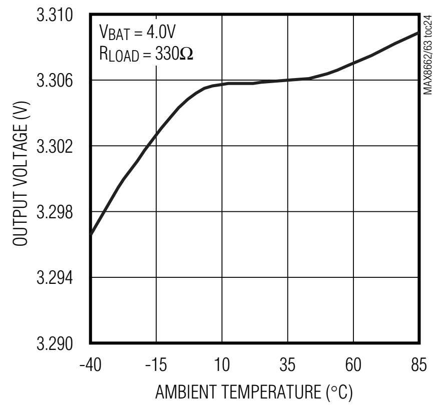
OUT1 REGULATOR LOAD REGULATION



OUT1 REGULATOR LINE REGULATION



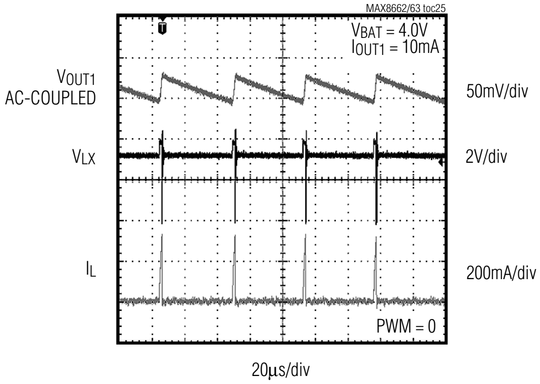
OUT1 VOLTAGE vs. TEMPERATURE



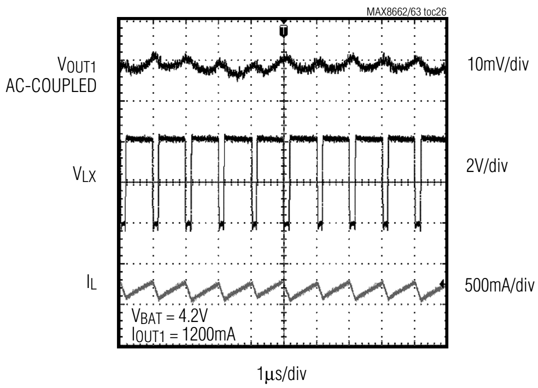
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

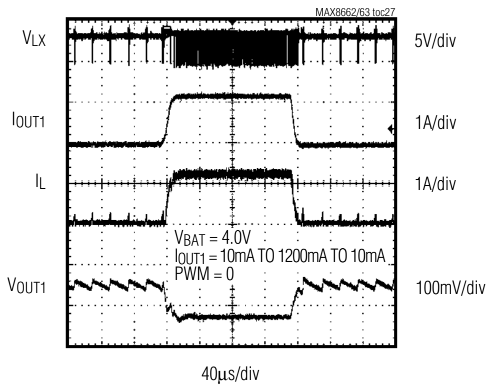
OUT1 REGULATOR LIGHT-LOAD SWITCHING WAVEFORMS



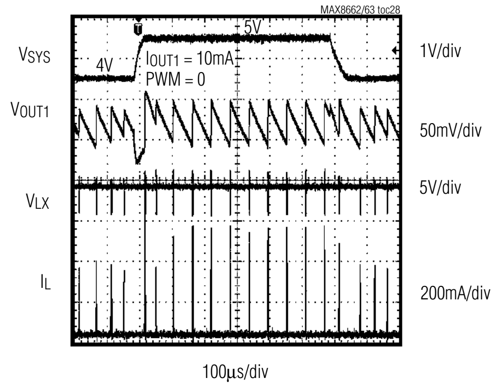
OUT1 REGULATOR HEAVY-LOAD SWITCHING WAVEFORMS



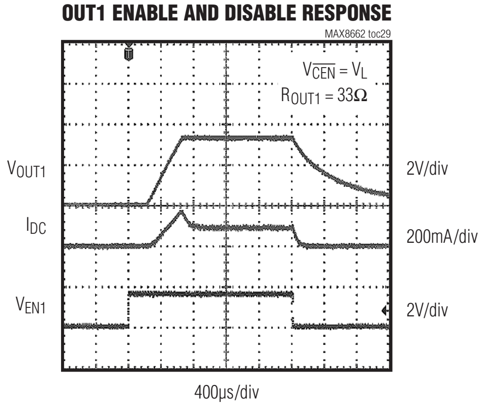
OUT1 REGULATOR LOAD-TRANSIENT RESPONSE



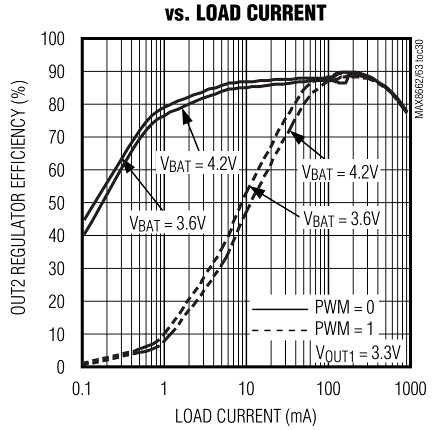
OUT1 REGULATOR LINE-TRANSIENT RESPONSE



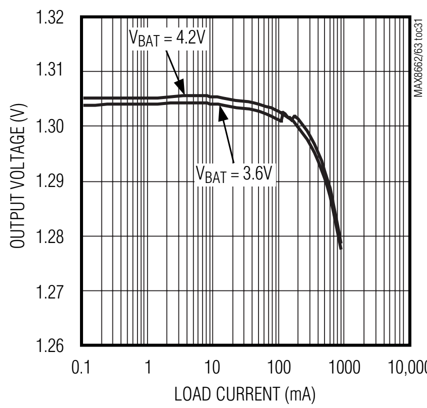
OUT1 ENABLE AND DISABLE RESPONSE



OUT2 REGULATOR EFFICIENCY vs. LOAD CURRENT



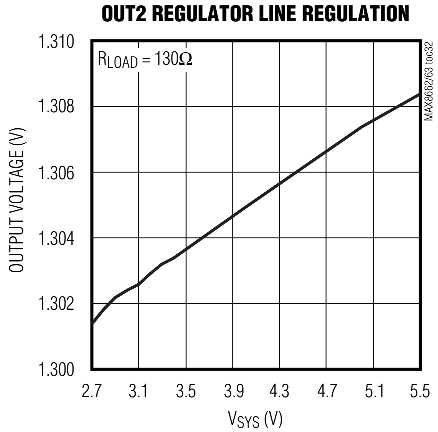
OUT2 REGULATOR LOAD REGULATION

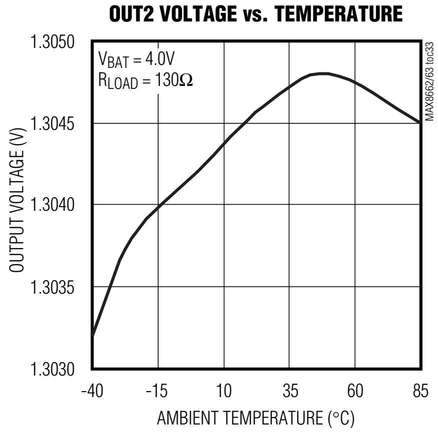


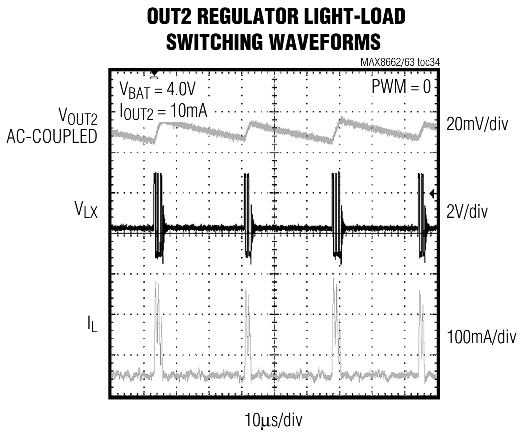
Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

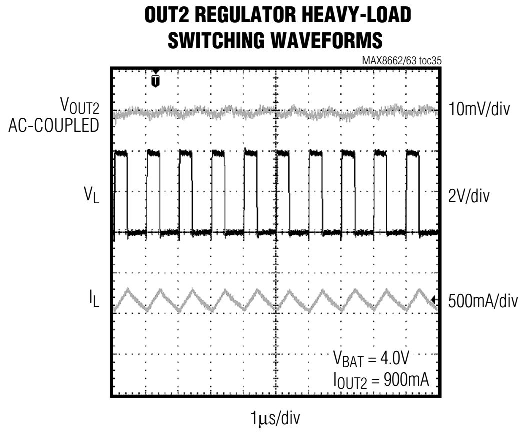
Typical Operating Characteristics (continued)

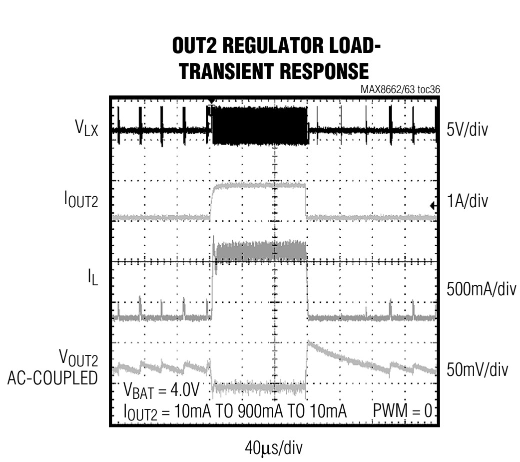
(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

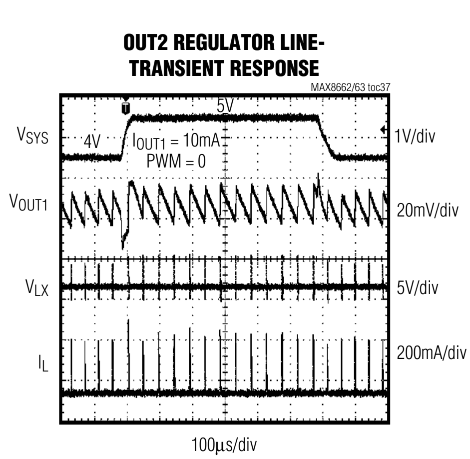








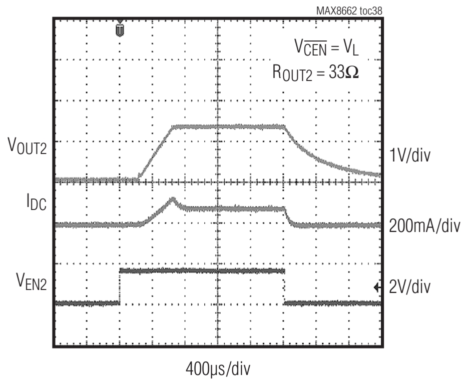




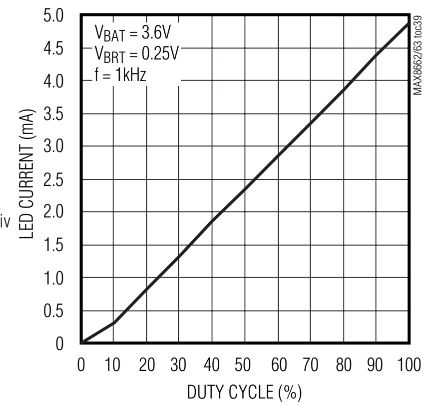
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

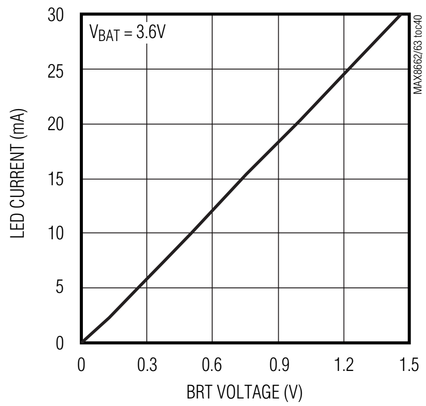
OUT2 ENABLE AND DISABLE RESPONSE



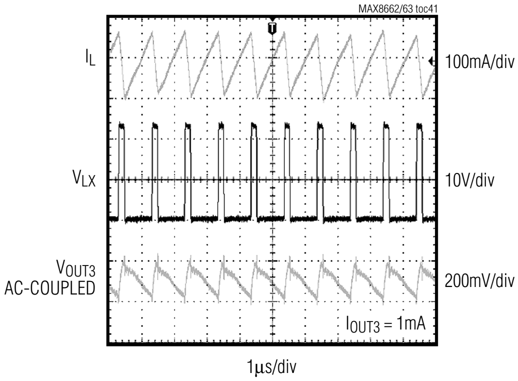
LED CURRENT vs. PWM DIMMING DUTY CYCLE



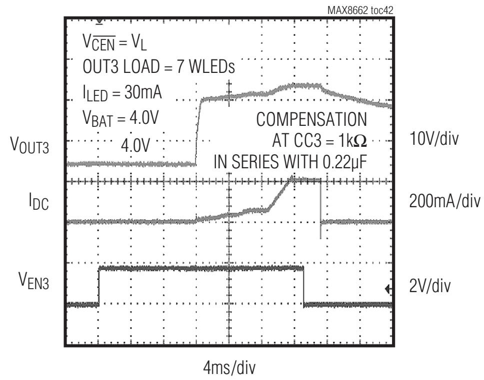
LED CURRENT vs. BRT VOLTAGE



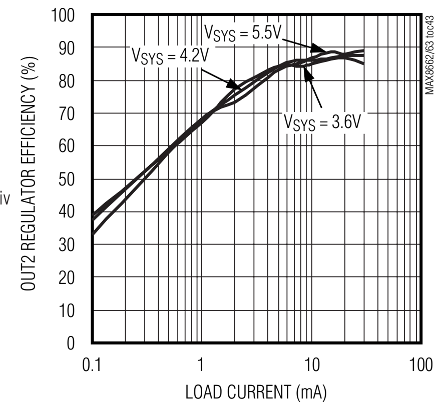
OUT3 SWITCHING WAVEFORMS



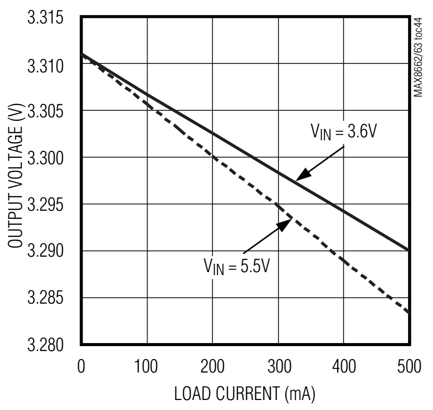
OUT3 ENABLE AND DISABLE RESPONSE



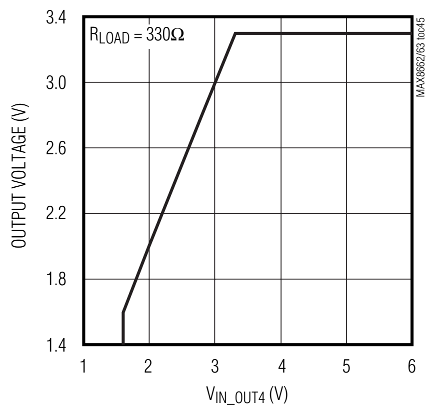
OUT3 REGULATOR EFFICIENCY vs. LOAD CURRENT



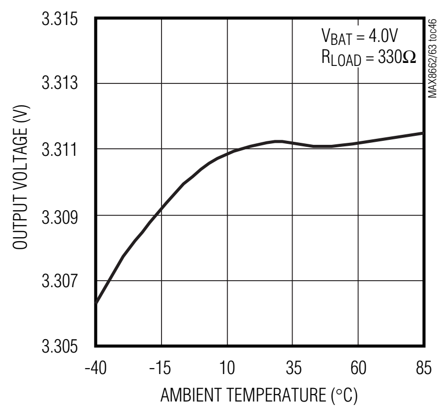
OUT4 REGULATOR LOAD REGULATION



OUT4 REGULATOR LINE REGULATION



OUT4 VOLTAGE vs. TEMPERATURE

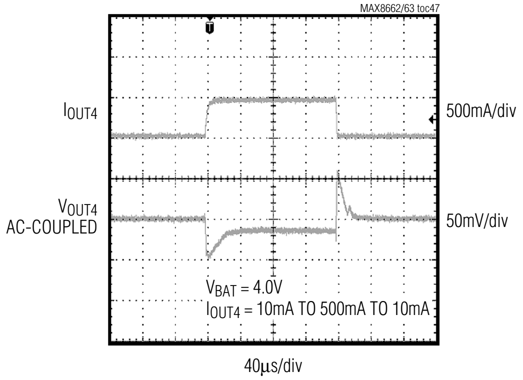


Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

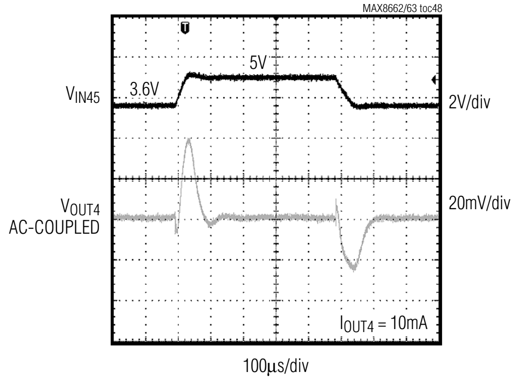
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

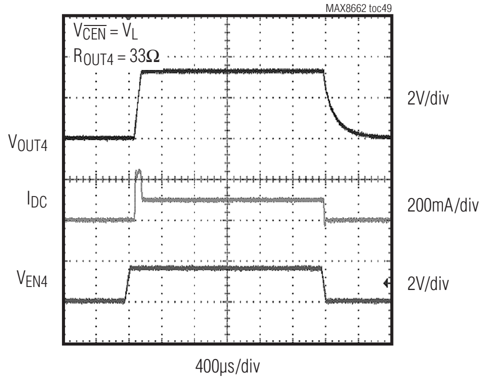
OUT4 REGULATOR LOAD-TRANSIENT RESPONSE



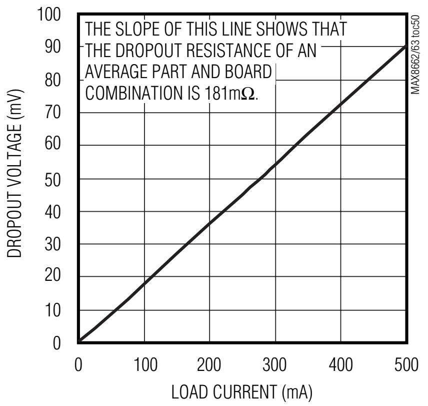
OUT4 REGULATOR LINE-TRANSIENT RESPONSE



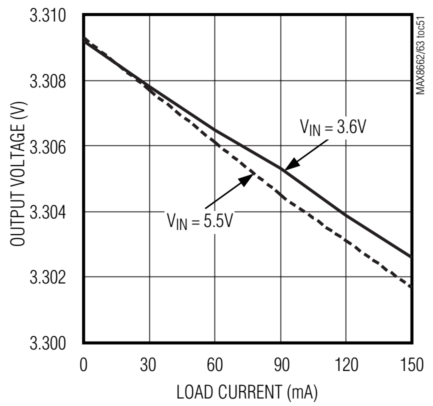
OUT4 ENABLE AND DISABLE RESPONSE



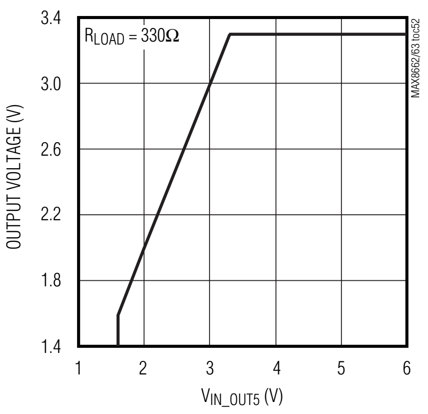
OUT4 REGULATOR DROPOUT VOLTAGE vs. LOAD CURRENT



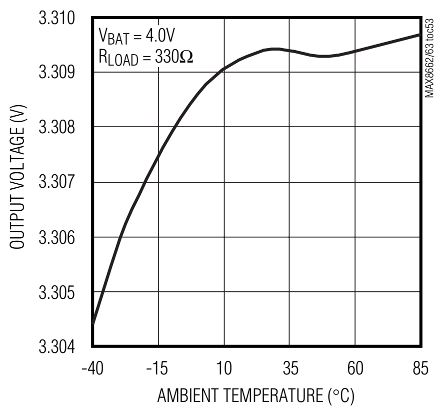
OUT5 REGULATOR LOAD REGULATION



OUT5 REGULATOR LINE REGULATION



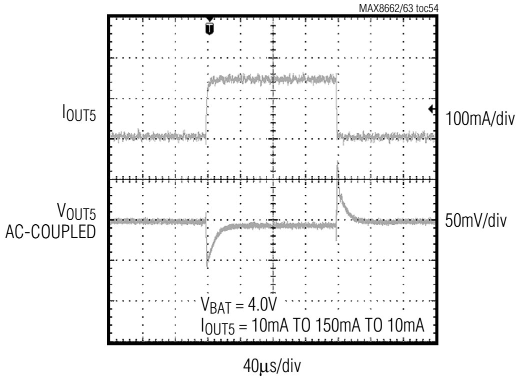
OUT5 VOLTAGE vs. TEMPERATURE



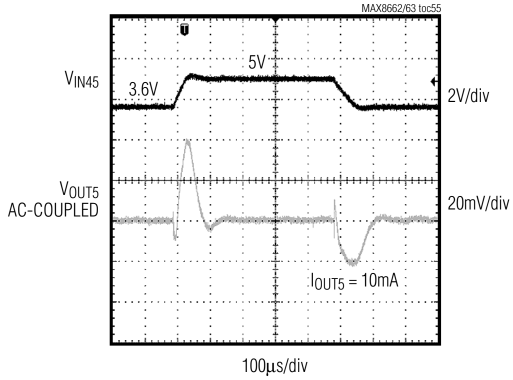
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

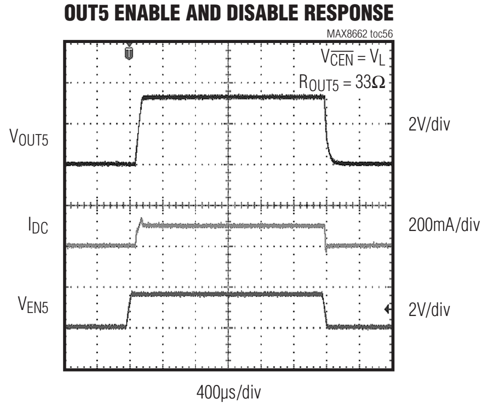
OUT5 REGULATOR LOAD-TRANSIENT RESPONSE



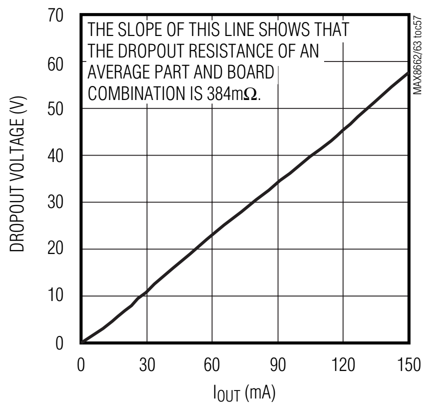
OUT5 REGULATOR LINE-TRANSIENT RESPONSE



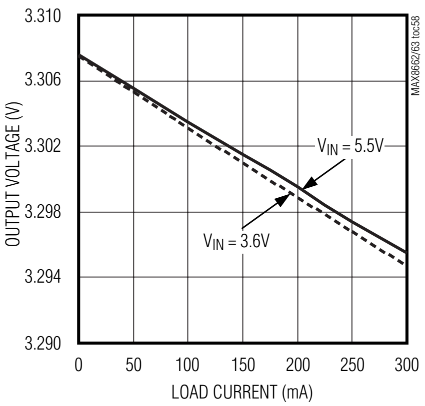
OUT5 ENABLE AND DISABLE RESPONSE



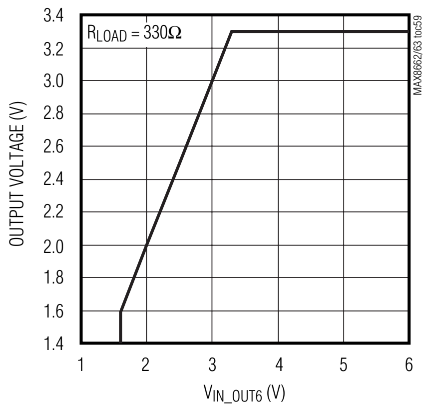
OUT5 REGULATOR DROPOUT VOLTAGE vs. LOAD CURRENT



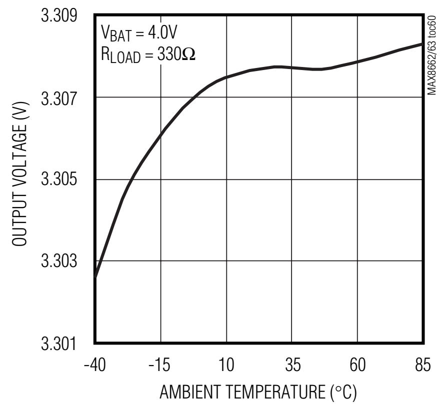
OUT6 REGULATOR LOAD REGULATION



OUT6 REGULATOR LINE REGULATION



OUT6 VOLTAGE vs. TEMPERATURE

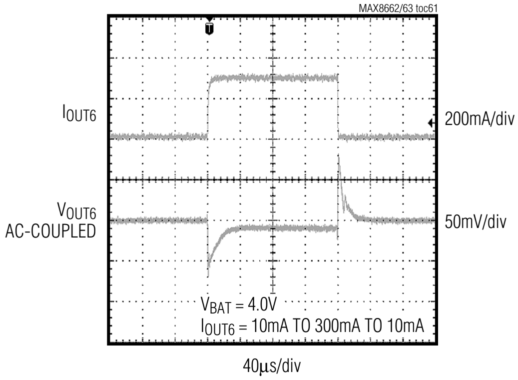


Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

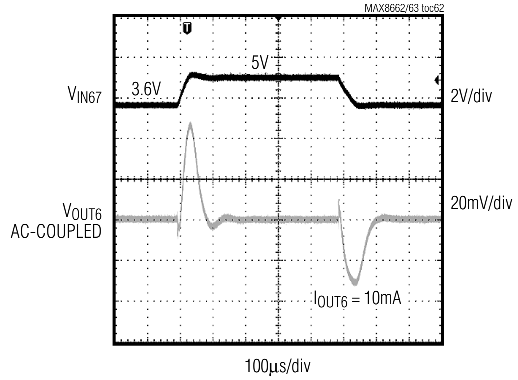
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

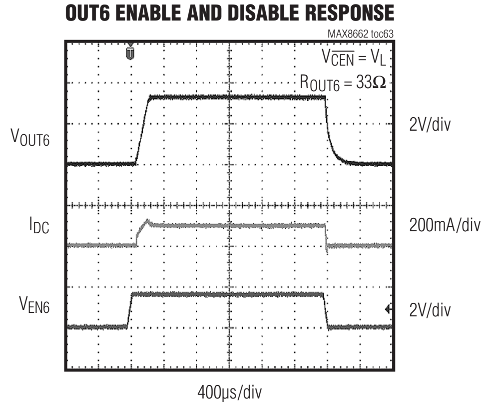
OUT6 REGULATOR LOAD-TRANSIENT RESPONSE



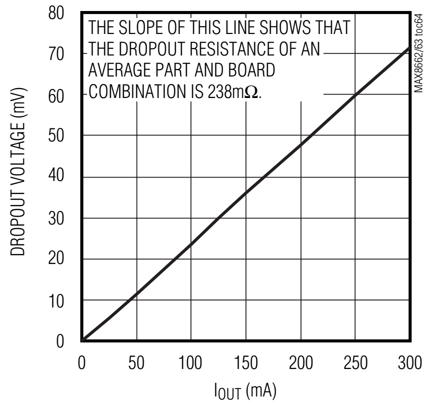
OUT6 REGULATOR LINE-TRANSIENT RESPONSE



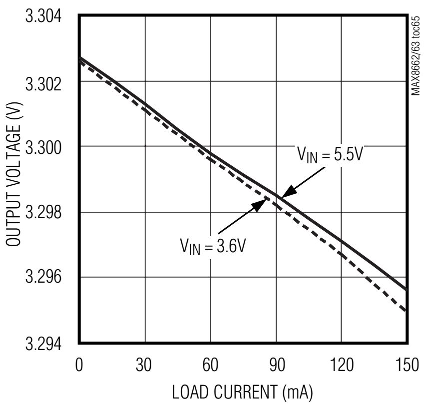
OUT6 ENABLE AND DISABLE RESPONSE



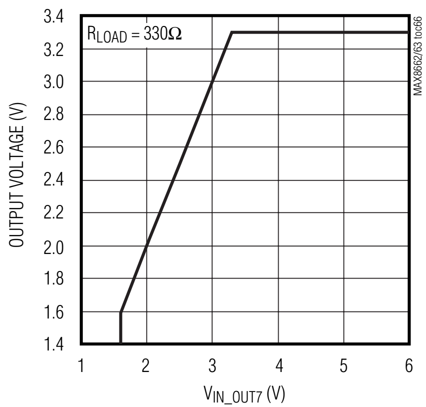
OUT6 REGULATOR DROPOUT VOLTAGE vs. LOAD CURRENT



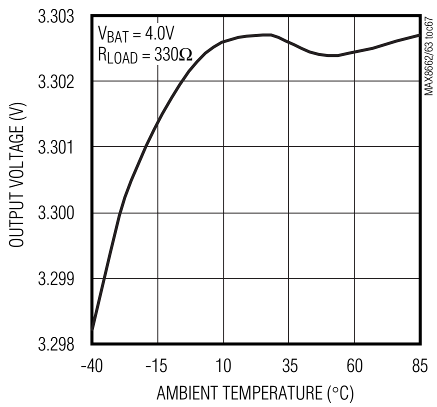
OUT7 REGULATOR LOAD REGULATION



OUT7 REGULATOR LINE REGULATION



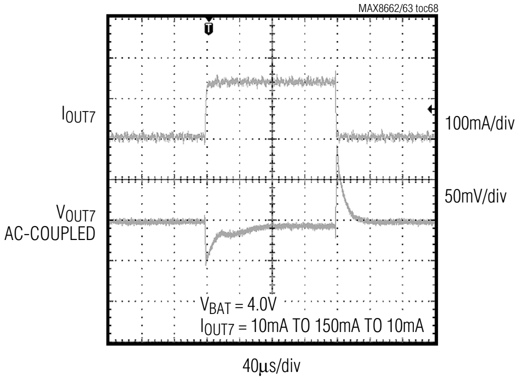
OUT7 VOLTAGE vs. TEMPERATURE



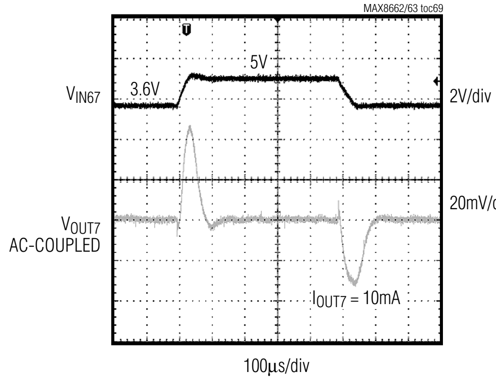
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DC} = 5V, R_{PSET} = 1.5kΩ, R_{ISET} = 3kΩ, V_{OUT1} = 3.3V, V_{OUT2} = 1.3V, SL1 = SL2 = open, $V_{\overline{CEN}}$ = 0V, V_{PEN1} = V_{PEN2} = 5V, C_{OUT1} = 2 x 10µF, C_{OUT2} = 2 x 10µF, C_{OUT3} = 0.1µF, C_{OUT4} = 4.7µF, C_{OUT5} = 1µF, C_{OUT6} = 2.2µF, C_{OUT7} = 1µF, CT = 0.068µF, C_{REF} = C_{VL} = 0.1µF, R_{THM} = 10kΩ, L1 = 3.3µH, L2 = 4.7µH, L3 = 22µH, V_{GND} = V_{PG1} = V_{PG2} = V_{PG3} = 0V, T_A = +25°C, unless otherwise noted.)

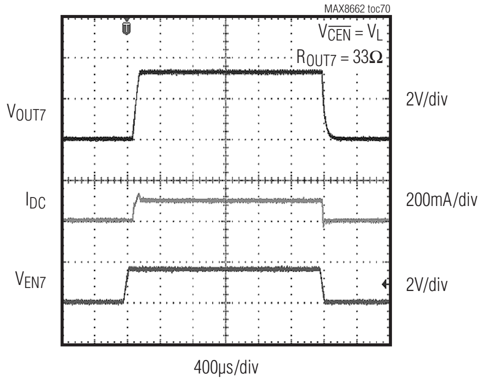
OUT7 REGULATOR LOAD-TRANSIENT RESPONSE



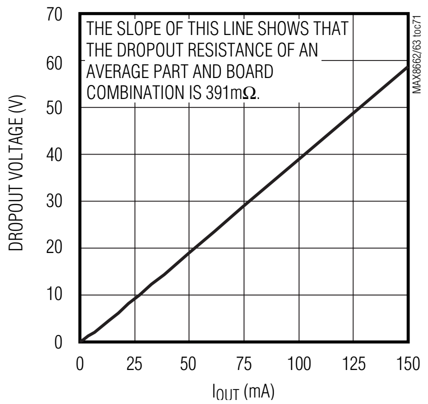
OUT7 REGULATOR LINE-TRANSIENT RESPONSE



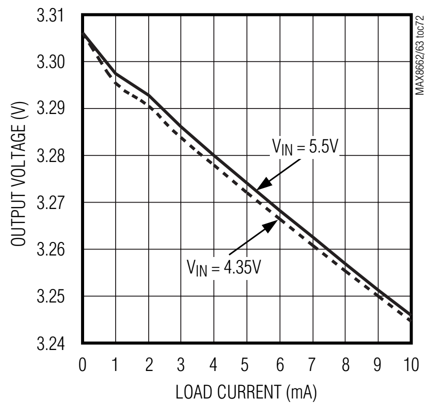
OUT7 ENABLE AND DISABLE RESPONSE



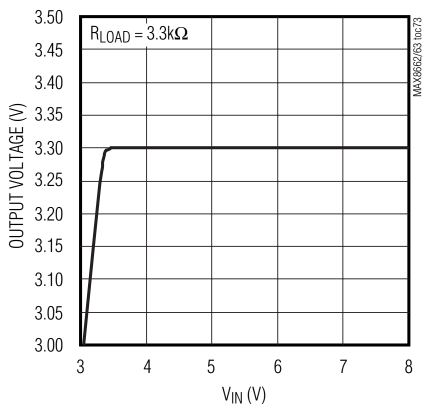
OUT7 REGULATOR DROPOUT VOLTAGE vs. LOAD CURRENT



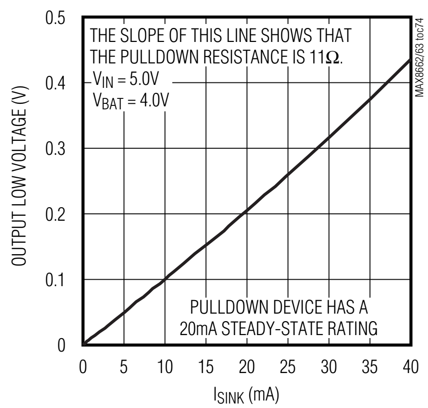
VL REGULATOR LOAD REGULATION



VL REGULATOR LINE REGULATION



OPEN-DRAIN OUTPUT VOLTAGE LOW vs. SINK CURRENT



Pin Description

PIN MAX8662	PIN MAX8663	NAME	FUNCTION
1	1	PEN1	Input Limiter-Control Input 1. Used with $\overline{CEN}$ and PEN2 to set the DC current limit to 95mA, 475mA, a resistor programmable level up to 2A, or to turn off the input limiter (see Table 1).
2	2	PEN2	Input Limiter-Control Input 2. Used with $\overline{CEN}$ and PEN1 to set the DC current limit to 95mA, 475mA, a resistor programmable level up to 2A, or to turn off the input limiter (see Table 1).
3	—	EN3	Enable Input and PWM Dimming Input for Regulator 3 White LED Boost. Drive high to enable. Drive low for more than 2ms to turn off. For PWM-controlled dimming, drive EN3 with a PWM switching input with a frequency of 1kHz to 100kHz.
4, 5	3, 4	DC1, DC2	DC Input Source. Connect to an AC adapter or USB source. DC1 and DC2 are internally connected.
6, 7	5, 6	SYS1, SYS2	System Supply Voltage. The SYS output supplies power to all regulators. With no external power, SYS1 and SYS2 connect to BAT through an internal 40mΩ switch. When a valid voltage is present at DC_, SYS_ connects to DC_ but is limited to 5.3V. SYS1 and SYS2 are internally connected.
8, 9	7, 8	BAT1, BAT2	Battery Connections. Connect to a single-cell Li+ battery. The battery is charged from SYS_ when a valid source is present at DC. BAT_ drives SYS_ when DC is not valid. BAT1 and BAT2 are internally connected.
10	—	BRT	LED Analog Brightness Control Input. Connect BRT to a voltage from 50mV to 1.5V to set I_{CS} from 1mA to 30mA. Connect BRT to the center of a resistor-divider connected between REF and GND to set a fixed brightness when analog dimming is not required.
11	9	$\overline{CHG}$	Charger Status Output. $\overline{CHG}$ is an open-drain nMOS that pulls low when the charger is in fast charge or prequalification modes. $\overline{CHG}$ goes high impedance when the charger is in top-off mode or disabled.
12	10	$\overline{CEN}$	Charger Enable Input. Drive $\overline{CEN}$ low to enable the charger when a valid source is connected at DC. Drive $\overline{CEN}$ high to disable charging. Drive $\overline{CEN}$ high and PEN2 low to enter USB suspend mode.
13	11	THM	Thermistor Input. Connect a 10kΩ negative temperature coefficient (NTC) thermistor from THM to GND. Charging is suspended when the temperature is beyond the hot or cold limits. Connect THM to GND to disable the thermistor functionality.
14	12	ISET	Charge Rate-Set Input. Connect a resistor from ISET to GND to set the fast-charge current from 300mA to 1.25A. The prequalification charge current and top-off threshold are set to 10% and 7.5% of fast-charge current, respectively.
15	13	CT	Charge Timer-Programming Pin. Connect a capacitor from CT to GND to set the length of time required to trigger a fault condition in fast-charge or prequalification mode and to determine the time the charger remains in top-off mode. Connect CT to GND to disable timers.
16	—	REF	Reference Voltage. Provides 1.5V output when EN3 is high. An internal discharge resistance pulls REF to 0V when EN3 is low.
17	14	GND	Ground. Low-noise ground connection.
18	15	OUT4	Linear Regulator 4 Output. Delivers up to 500mA at an output voltage determined by SL1 and SL2. Connect a 4.7µF ceramic capacitor from OUT4 to GND. Increase the value to 10µF if V_{OUT4} < 1.5V.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8662	MAX8663		
19	16	IN45	Input Supply for Linear Regulators 4 and 5. Connect IN45 to a supply voltage between 1.7V and V_{SYS}. Connect at least a 1µF ceramic capacitor from IN45 to GND.
20	17	OUT5	Linear Regulator 5 Output. Delivers up to 150mA at an output voltage determined by SL1 and SL2. Connect a 1µF ceramic capacitor from OUT5 to GND. Increase the value to 2.2µF if V_{OUT5} < 1.5V.
21	18	EN4	Enable Input for Linear Regulator 4. Drive high to enable.
22	19	EN5	Enable Input for Linear Regulator 5. Drive high to enable.
23	20	PWM	PWM/Skip-Mode Selector. Drive PWM high to force step-down regulators 1 and 2 to operate in 1MHz forced-PWM mode. Drive PWM low, or connect to GND to allow regulators 1 and 2 to enter skip mode at light loads.
24	21	FB1	Feedback Input for Buck Regulator 1. Connect FB1 to the center of a resistor-divider connected between OUT1 and GND to set the output voltage between 0.98V and 3.3V.
25	22	EN1	Enable Input for Buck Regulator 1. Drive high to enable.
26	23	PG1	Power Ground for Buck Regulator 1. GND, PG1, PG2, and PG3 must be connected together externally.
27	24	LX1	Buck Regulator 1 Inductor Connection Node. Connect an inductor from LX1 to the output of regulator 1.
28	25	PV1	Power Input for Buck Regulator 1. Connect PV1 to SYS and decouple with a 10µF or greater low-ESR capacitor to GND. PV1, PV2, and SYS must be connected together externally.
29	—	OVP	LED Boost Overvoltage Input. Connect a resistor from OVP to the boost output to set the maximum output voltage and to initiate soft-start when EN3 goes high. An internal 20µA pulldown current from OVP to GND determines the maximum boost voltage. The internal current is disconnected when EN3 is low. OVP is diode clamped to SYS_.
30	—	CS	LED Current Source. Sinks from 1mA to 30mA depending on the voltage at BRT and the PWM signal at EN3. Driving EN3 low for more than 2ms turns off the current source. V_{CS} is regulated to 0.32V.
31	—	CC3	Compensation Input for LED Boost Regulator 3. See the *Boost Converter with White LED Driver (OUT3, MAX8662 Only)* section.
32	26	FB2	Feedback Input for Buck Regulator 2. Connect FB2 to the center of a resistor-divider connected between OUT2 and GND to set the output voltage between 0.98V and 3.3V.
33	27	PV2	Power Input for Buck Regulator 2. Connect PV2 to SYS and decouple with a 10µF or greater low-ESR capacitor to GND. PV1, PV2, and SYS must be connected together externally.
34	28	LX2	Buck Regulator 2 Inductor Connection Node. Connect an inductor from LX2 to the output of regulator 2.
35	29	PG2	Power Ground for Buck Regulator 2. GND, PG1, PG2, and PG3 must be connected together externally.
36	30	EN2	Enable Input for Buck Regulator 2. Drive high to enable.
37	31	EN6	Enable Input for Linear Regulator 6. Drive high to enable.
38	32	EN7	Enable Input for Linear Regulator 7. Drive high to enable.
39	—	LX3	Boost Regulator 3 Inductor Connection Node. Connect an inductor from LX3 to SYS_.

Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8662	MAX8663		
40	—	PG3	Power Ground for Boost Regulator 3. GND, PG1, PG2, and PG3 must be connected together externally.
41	33	OUT6	Linear Regulator 6 Output. Delivers up to 300mA at an output voltage determined by SL1 and SL2. Connect a 2.2µF ceramic capacitor from OUT6 to GND. Increase the value to 4.7µF if V_{OUT6} < 1.5V.
42	34	IN67	Input Supply for Linear Regulators 6 and 7. Connect IN67 to a supply voltage of 1.7V to V_{SYS}. Connect at least a 1µF ceramic capacitor from IN67 to GND.
43	35	OUT7	Linear Regulator 7 Output. Delivers up to 150mA at an output voltage determined by SL1 and SL2. Connect a 1µF ceramic capacitor from OUT7 to GND. Increase the value to 2.2µF if V_{OUT7} < 1.5V.
44	36	VL	Input Limiter and Charger Logic Supply. Provides 3.3V when a valid input voltage is present at DC. Connect a 0.1µF capacitor from VL to GND. VL is capable of providing up to 10mA to an external load when DC is valid.
45	37	SL1	Output-Voltage Select Inputs 1 and 2 for Linear Regulators. Leave disconnected, or connect to GND or SYS to set to one of three states. SL1 and SL2 set the output voltage of OUT4, OUT5, OUT6, and OUT7 to one of nine combinations. See Table 3.
46	38	SL2	
47	39	PSET	Input Current-Limit Set Input. Connect a resistor (R_{PSET}) from PSET to ground to program the DC input current limit from 500mA to 2A.
48	40	$\overline{POK}$	Power-Ok Output. $\overline{POK}$ is an open-drain nMOS output that pulls low when a valid input is detected at DC. This output is not affected by the states of PEN1, PEN2, or $\overline{CEN}$.
—	—	EP	Exposed Paddle. Connect the exposed paddle to ground. Connecting the exposed paddle to ground does not remove the requirement for proper ground connections to GND, PG1, PG2, and PG3. The exposed paddle is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

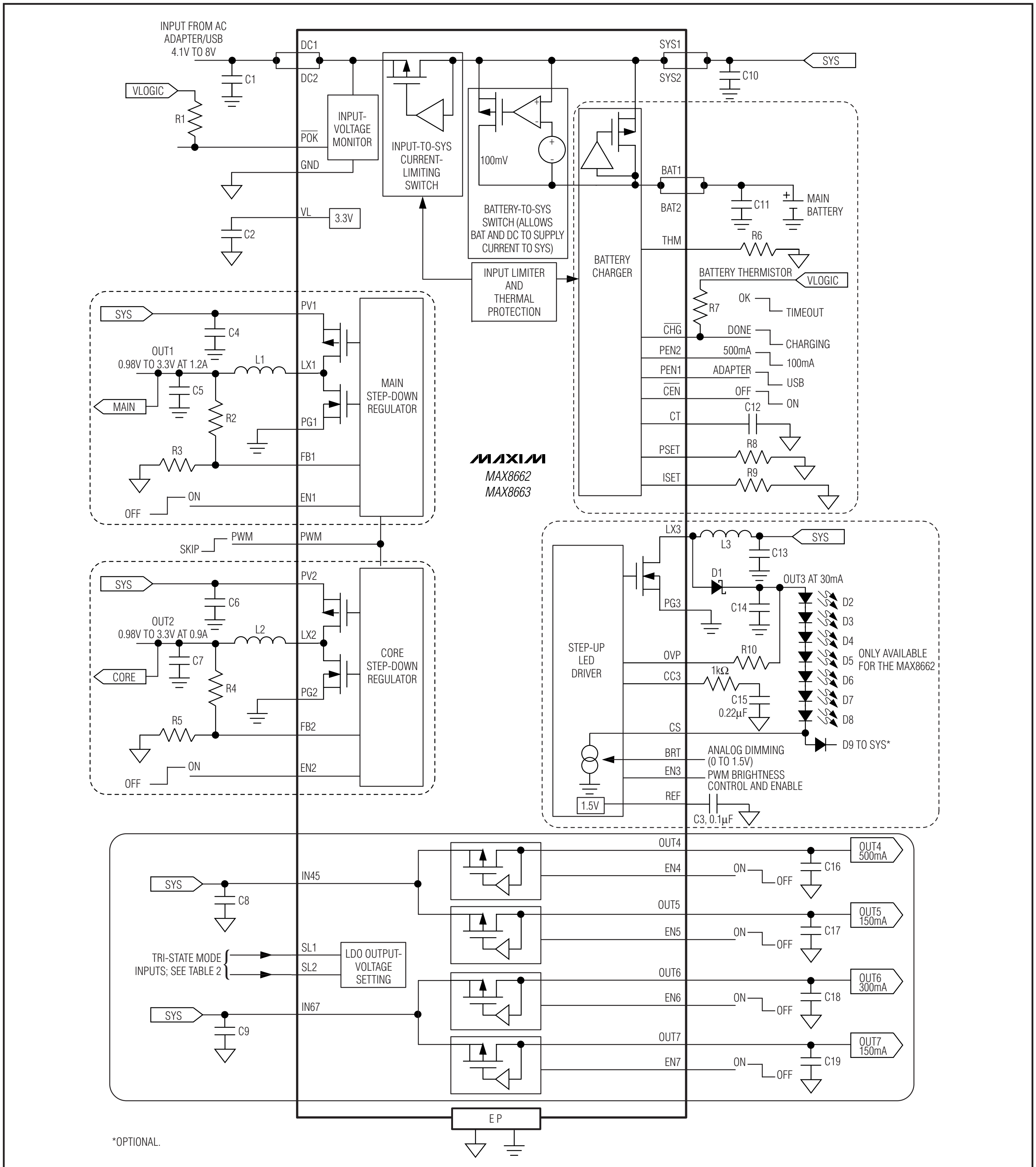


Figure 1. Block Diagram and Application Circuit

Detailed Description

The MAX8662/MAX8663 highly integrated PMICs are designed for use in smart cellular phones, PDAs, Internet appliances, and other portable devices. They integrate two synchronous buck regulators, a boost regulator driving two to seven white LEDs (MAX8662 only), four low dropout (LDO) linear regulators, and a linear charger for a single-cell Li+ battery. Figure 1 is the block diagram and application circuit.

SPS circuitry offers flexible power distribution between an AC adapter or USB source, battery, and system load, and makes the best use of available power from the AC adapter/USB input. The battery is charged with any available power not used by the system load. If a system load peak exceeds the current limit, supplemental current is taken from the battery. Thermal limiting prevents overheating by reducing power drawn from the input source.

Two step-down DC-DC converters achieve excellent light-load efficiency and have on-chip soft-start circuitry; 1MHz switching frequency allows for small external components. Four LDO linear regulators feature low quiescent current and operate from inputs as low as 1.7V. This allows the LDOs to operate from the step-down output voltage to improve efficiency. The white LED driver features easy adjustment of LED brightness and open-LED overvoltage protection. A 1-cell Li+ charger has programmable charge current up to 1.25A and a charge timer.

Smart Power Selector (SPS)

SPS seamlessly distributes power between the external input, the battery, and the system load (Figure 2). The basic functions of SPS are:

- With both the external power supply and battery connected:
  - a) When the system load requirements exceed the capacity of the external power input, the battery supplies supplemental current to the load.
  - b) When the system load requirements are less than the capacity of the external power input, the battery is charged with residual power from the input.
- When the battery is connected and there is no external power input, the system is powered from the battery.
- When an external power input is connected and there is no battery, the system is powered from the external power input.

A thermal-limiting circuit reduces battery-charge rate and external power-source current to prevent overheating.

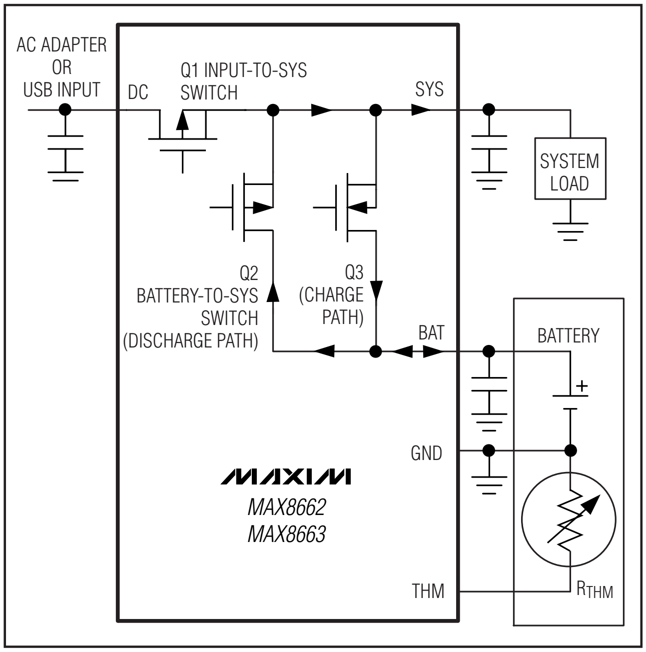


Figure 2. Smart Power Selector Block Diagram

Input Limiter

All regulated outputs (OUT1–OUT7) derive their power from the SYS output. With an AC adapter or USB source connected at DC, the input limiter distributes power from the external power source to the system load and battery charger. In addition to the input limiter's primary function of passing the DC power source to the system and charger loads at SYS, it performs several additional functions to optimize use of available power:

- **Input Voltage Limiting:** If the voltage at DC rises, SYS limits to 5.3V, preventing an overvoltage of the system load. A DC voltage greater than 6.9V is considered invalid and the input limiter disconnects the DC input entirely. The withstand voltage at DC is guaranteed to be at least 9V. A DC input is also invalid if it is less than BAT, or less than the DC undervoltage threshold of 3.5V (falling). With an invalid DC input voltage, SYS connects to BAT through a 40mΩ switch.
- **Input Overcurrent Protection:** The current at DC is limited to prevent input overload. This current limit is automatically adjusted to match the capabilities of source, whether it is a 100mA or 500mA USB source, or an AC adapter. When the load exceeds the input current limit, SYS drops to 100mV below BAT and supplemental load current is provided by the battery.

- **Thermal Limiting:** The input limiter includes a thermal-limiting circuit that reduces the current drawn from DC when the IC junction temperature increases beyond +100°C in an attempt to prevent further heating. The current limit is be reduced by 5%/°C for temperatures above +100°C, dropping to 0mA at +120°C. Due to the adaptive nature of the charging circuitry, the charger current reduces to 0mA before the system load is affected by thermal limiting.
- **Adaptive Battery Charging:** While the system is powered from DC, the charger can also draw power from SYS to charge the battery. If the charger load plus system load exceeds the current capability of the input source, an adaptive charger control loop reduces charge current to prevent the SYS voltage from collapsing. Maintaining a higher SYS voltage improves efficiency and reduces power dissipation in the input limiter by running the switching regulators at lower current.

Figure 3 shows the SYS voltage and its relationship to DC and BAT under three conditions:

a) Charger is off and SYS is driven from DC.

b) Charger is on and adaptive charger control is limiting charge current.

c) The load at SYS is greater than the available input current.

The adaptive battery-charger circuit reduces charging current when the SYS voltage drops 550mV below DC. For example, if DC is at 5V, the charge current reduces to prevent SYS from dropping below 4.45V. When DC is greater than 5.55V, the adaptive charging circuitry reduces charging current when SYS drops 300mV below the 5.3V SYS regulation point (5.0V). Finally, the circuit prevents itself from pulling SYS down to within 100mV of BAT.

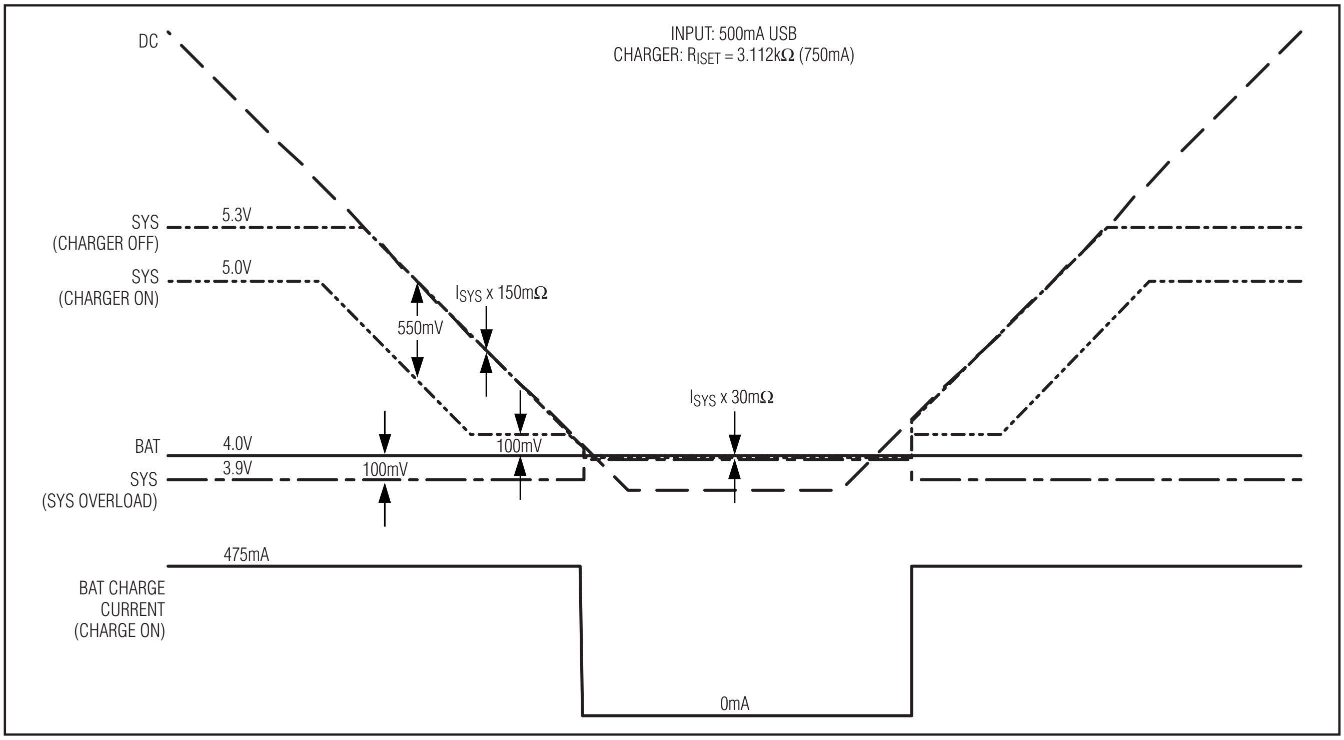


Figure 3. SYS Voltage and Charge Current vs. DC and BAT Voltage

Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

DC Input Current-Limit Selection (PEN1/PEN2)

The input current limit can be set to a variety of values as shown in Table 1. When the PEN1 input is low, a USB source is expected at DC and the current limit is set to either 95mA or 475mA by PEN2.

When PEN1 is high, an AC adapter is expected at DC and the current limit is set based on a programming resistor at PSET. The DC input current limit is calculated from:

$$I_{DC\_LIM} = 2000 \times (1.5 / R_{PSET})$$

An exception is when the battery charger is disabled ($\overline{\text{CEN}}$ high) with PEN2 low, where the MAX8662/MAX8663 enter USB suspend mode.

Power-OK Output ($\overline{\text{POK}}$)

$\overline{\text{POK}}$ is an active-low open-drain output indicating DC status. When the voltage at DC is between the undervoltage and the overvoltage thresholds, and is greater than the BAT voltage, $\overline{\text{POK}}$ pulls low to indicate that input power is OK. Otherwise, $\overline{\text{POK}}$ is high impedance. $\overline{\text{POK}}$ is not affected by the states of PEN1, PEN2, or $\overline{\text{CEN}}$. $\overline{\text{POK}}$ remains active in thermal overload.

Battery Charger

The battery charger state diagram is illustrated in Figure 4.

With a valid AC adapter/USB voltage present, the battery charger initiates a charge cycle when the charger

Table 1. DC Input Current and Charger Current-Limit Select

$\overline{\text{CEN}}$	PEN1	PEN2	DC INPUT CURRENT LIMIT	EXPECTED INPUT TYPE	CHARGER CURRENT LIMIT**
0	0	0	95mA	100mA USB	$1556(1.5V / R_{ISET})$
0	0	1	475mA	500mA USB	$1556(1.5V / R_{ISET})$
0	1	X*	$2000(1.5V / R_{PSET})$	AC adapter	$1556(1.5V / R_{ISET})$
1	X*	0	Off	USB suspend	Off
1	0	1	475mA	500mA USB	Off
1	1	1	$2000(1.5V / R_{PSET})$	AC adapter	Off

**X = Don't care.* ***The maximum charge will not exceed the DC Input current.*

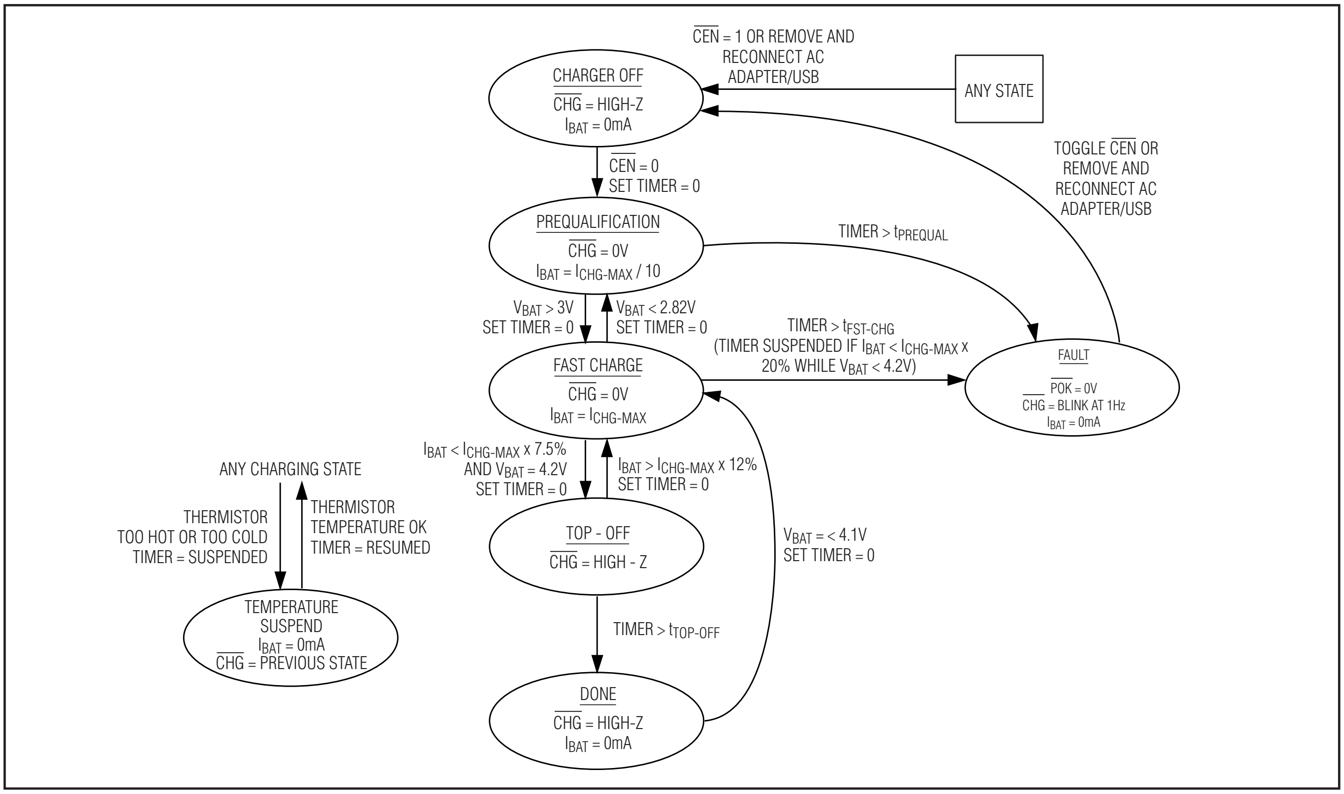


Figure 4. Charger State Diagram

is enabled. It first detects the battery voltage. If the battery voltage is less than the BAT prequalification threshold (3.0V), the charger enters prequalification mode in which the battery charges at 10% of the maximum fast-charge current. This slow charge ensures that the battery is not damaged by fast-charge current while deeply discharged. Once the battery voltage rises to 3.0V, the charger transitions to fast-charge mode and applies the maximum charge current. As charging continues, the battery voltage rises until it reaches the battery regulation voltage (4.2V) where charge current starts tapering down. When charge current decreases to 7.5% of fast-charge current, the charger enters top-off mode. Top-off charging continues for 30min, then all charging stops. If the battery voltage subsequently drops below the 4.1V recharge threshold, charging restarts and the timers reset.

Charge Current

ISET adjusts the MAX8662/MAX8663 charging current to match the capacity of the battery. A resistor from ISET to ground sets the maximum fast-charge current, the charge current in prequal, and the charge-current threshold below which the battery is considered completely charged. Calculate these thresholds as follows:

$$I_{CHG\text{-}MAX} = 1556 \times 1.5V / R_{ISET}$$

$$I_{PRE\text{-}QUAL} = 10\% \times I_{CHG\text{-}MAX}$$

$$I_{TOP\text{-}OFF} = 7.5\% \times I_{CHG\text{-}MAX}$$

Determine the $I_{CHG\text{-}MAX}$ value by considering the characteristics of the battery, and not the capabilities of the expected AC adapter/USB charging input, the system load, or thermal limitations of the PCB. The MAX8662/MAX8663 automatically adjust the charging algorithm to accommodate these factors.

In addition to setting the charge current, ISET also provides a means to monitor battery-charge current. The output voltage of the ISET pin tracks the charge current delivered to the battery, and can be used to monitor the charge rate, as shown in Figure 5. A 1.5V output indicates the battery is being charged at the maximum set fast-charge current; 0V indicates no charging. This voltage is also used by the charger control circuitry to set and monitor the battery current. Avoid adding more than 10pF capacitance directly to the ISET pin. If filtering of the charge-current monitor is necessary, add a resistor of 100kΩ or more between ISET and the filter capacitor to preserve charger stability.

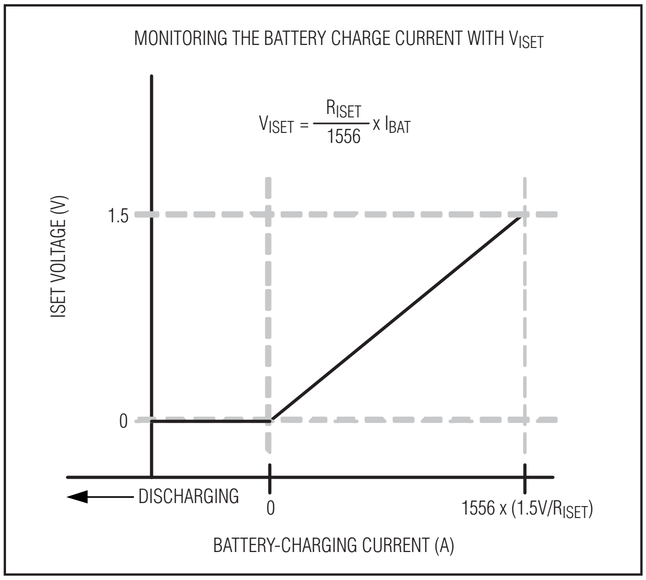


Figure 5. Monitoring the Battery Charge Current with ISET Output Voltage

Charge Timer

As shown in Figure 3, the MAX8662/MAX8663 feature a fault timer for safe charging. If prequalification charging or fast charging does not complete within the time limits, which are programmed by the timer capacitor at CT, the charger stops charging and issues a timeout fault. Charging can be resumed by either toggling $\overline{\text{CEN}}$ or cycling the DC input voltage.

The MAX8662/MAX8663 support values of C_{CT} from 0.01µF to 1µF:

$$t_{PREQUAL} = 30\text{min} \times \frac{C_{CT}}{0.068\mu F}$$

$$t_{FST-CHG} = 300\text{min} \times \frac{C_{CT}}{0.068\mu F}$$

When the charger exits fast-charge mode, $\overline{\text{CHG}}$ goes high impedance and top-off mode is entered. Top-off time is also determined by the capacitance at CT:

$$t_{TOP-OFF} = 300\text{min} \times \frac{C_{CT}}{0.068\mu F}$$

In fast-charge mode, the fault timer is suspended when the charge current is limited, by input or thermal limiting, to less than 20% of $I_{CHG\text{-}MAX}$.

Connect CT to GND to disable the prequalification and fast-charge timers, allowing the battery to charge indefinitely in top-off mode, or if other system timers are to be used to control charging.

Charge-Enable Input ($\overline{CEN}$)

Driving $\overline{CEN}$ high disables the battery charger. Driving $\overline{CEN}$ low enables the charger when a valid source is connected at DC. $\overline{CEN}$ does not affect the input limit current, except that driving $\overline{CEN}$ high and $\overline{PEN2}$ low activates USB suspend mode.

In many systems, there is no need for the system controller (typically a microprocessor) to disable the charger because the SPS circuitry independently manages charging and adapter/battery power hand-off. In these situations, $\overline{CEN}$ can be connected to ground.

Charge Status Output ($\overline{CHG}$)

$\overline{CHG}$ is an open-drain output that indicates charger status. $\overline{CHG}$ is low when the battery charger is in prequalification or fast-charge mode. It is high impedance when the charger is done, in top-off, or disabled.

The charger faults if the charging timer expires in prequalification or fast charge. In this state, $\overline{CHG}$ pulses at 1Hz to indicate that a fault occurred.

Battery Charger Thermistor Input (THM)

Battery or ambient temperature can be monitored with a negative temperature coefficient (NTC) thermistor. Charging is allowed when the thermistor temperature is within the allowable range.

The charger enters a temperature suspend state when the thermistor resistance falls below 3.97kΩ (too hot) or rises above 28.7kΩ (too cold). This corresponds to a 0 to +50°C range when using a 10kΩ NTC thermistor with a beta of 3500. The relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R25 \times e^{\left\{\beta\left(\frac{1}{T+273} - \frac{1}{298}\right)\right\}}$$

where:

R_T = The resistance in ohms of the thermistor at temperature T in Celsius

R25 = The resistance in ohms of the thermistor at +25°C

ß = The material constant of the thermistor, which typically ranges from 3000K to 5000K

T = The temperature of the thermistor in °C

Table 2 shows temperature limits for different thermistor material constants.

Some designs may prefer other trip temperatures. This can usually be accommodated by connecting a resistor in series and/or in parallel with the thermistor and/or using a thermistor with different ß. For example, a +45°C hot threshold and 0°C cold threshold can be realized by using a thermistor with a ß of 4250 and connecting 120kΩ in parallel. Since the thermistor resistance near 0°C is much higher than it is near +50°C, a large parallel resistance lowers the cold threshold, while only slightly lowering the hot threshold. Conversely, a small series resistance raises the cold threshold, while only slightly raising the hot threshold.

The charger timer pauses when the thermistor resistance goes out of range: charging stops and the timer counters hold their state. When the temperature comes back into range, charging resumes and the counters continue from where they left off. Connecting THM to GND disables the thermistor function.

Table 2. Fault Temperatures for Different Thermistors

THERMISTOR ß (K)	3000 (K)	3250 (K)	3500 (K)	3750 (K)	4250 (K)
Resistance at +25°C (kΩ)	10	10	10	10	10
Resistance at +50°C (kΩ)	4.59	4.30	4.03	3.78	3316
Resistance at 0°C (kΩ)	25.14	27.15	29.32	31.66	36.91
Nominal Hot Trip Temperature (°C)	55	53	50	49	46
Nominal Cold Trip Temperature (°C)	-3	-1	0	2	4.5

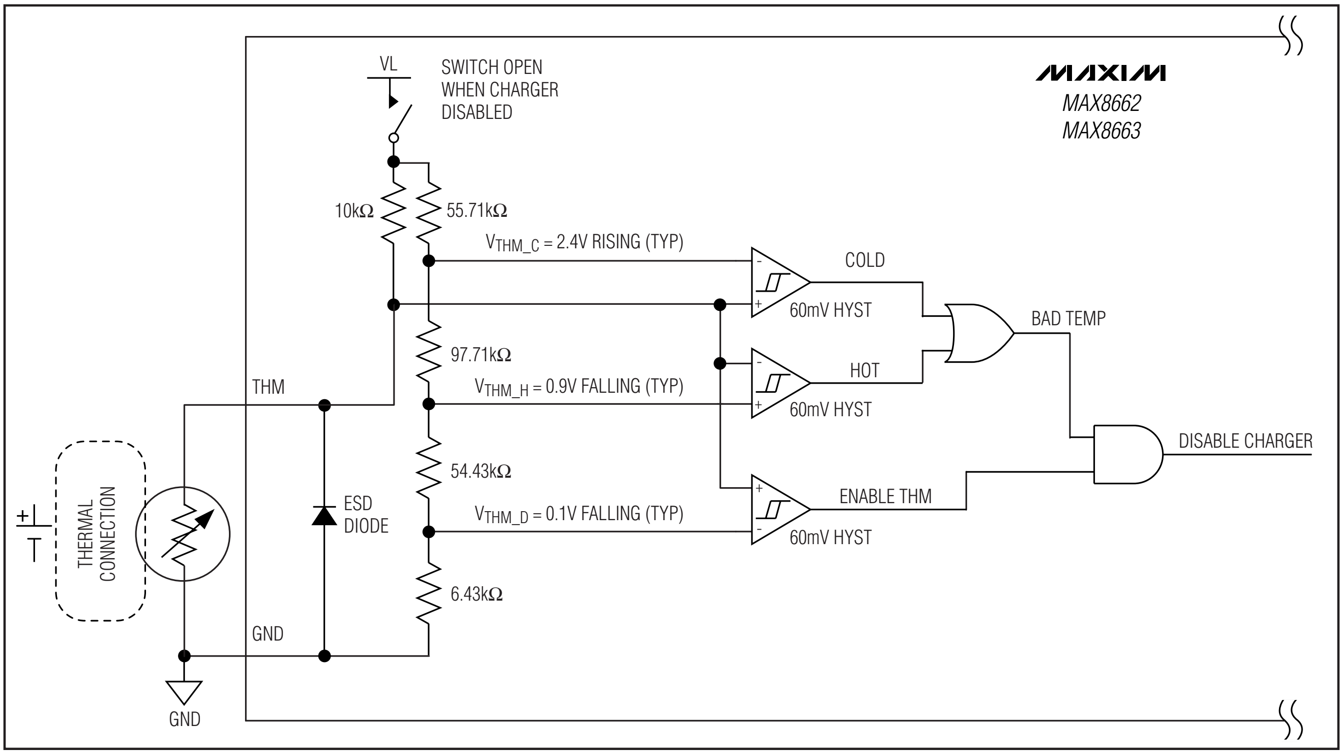


Figure 6. Thermistor Input

Figure 6 shows a simplified version of the THM input. Ensure that the physical size of the thermistor is such that the circuit of Figure 6 does not cause self-heating.

Step-Down DC-DC Converters (OUT1 and OUT2)

OUT1 and OUT2 are high-efficiency, 1MHz, current-mode step-down converters with adjustable output voltage. The OUT1 regulator outputs 0.98V to V_{IN} at up to 1200mA while OUT2 outputs 0.98V to V_{IN} at up to 900mA.

OUT1 and OUT2 have individual enable inputs. When enabled, the OUT1 and OUT2 gradually ramp the output voltage over a 400µs soft-start time. This soft-start eliminates input inrush current spikes.

OUT1 and OUT2 can operate at a 100% duty cycle, which allows the regulators to maintain regulation at the lowest possible battery voltage. The OUT1 dropout voltage is 72mV with a 600mA load and the OUT2 dropout voltage is 90mV with a 450mA load (does not include inductor resistance). During 100% duty-cycle operation, the high-side p-channel MOSFET turns on continuously, connecting the input to the output through the inductor.

Step-Down Converter Operating Modes

OUT1 and OUT2 can operate in either auto-PWM mode (PWM low) or forced-PWM mode (PWM high). In auto-PWM mode, OUT1 and OUT2 enter skip mode when the load current drops below a predetermined level. In skip mode, the regulator skips cycles when they are not needed, which greatly decreases quiescent current and improves efficiency at light loads. In forced-PWM mode, the converters operate with a constant 1MHz switching frequency regardless of output load. Output voltage is regulated by modulating the switching duty cycle. Forced-PWM mode is preferred for low-noise systems, where switching harmonics can occur only at multiples of the constant-switching frequency and are easily filtered; however, regulator operating current is greater and light-load efficiency is reduced.

Synchronous Rectification

Internal n-channel synchronous rectifiers eliminate the need for external Schottky diodes and improve efficiency. The synchronous rectifier turns on during the second half of each switching cycle. During this time, the voltage across the inductor is reversed, and the inductor current ramps down. In PWM mode, the synchronous rectifier turns off at the end of the switching cycle. In

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skip mode, the synchronous rectifier turns off when the inductor current falls below the n-channel zero-crossing threshold or at the end of the switching cycle, whichever occurs first.

Setting OUT1 and OUT2 Output Voltage

Select an output voltage for OUT1 between 0.98V and V_{IN} by connecting FB1 to the center of a resistive voltage-divider between OUT1 and GND. Choose R3 (Figure 1) for a reasonable bias current in the resistive divider; choose R3 to be between 100kΩ and 200kΩ. Then, R2 (Figure 1) is given by:

$$R2 = R3 ((V_{OUT1}/V_{FB}) - 1)$$

where V_{FB} = 0.98V. For OUT2, R4 and R5 are calculated using:

$$R4 = R5 ((V_{OUT2}/V_{FB}) - 1)$$

OUT1 and OUT2 Inductors

3.3µH and 4.7µH inductors are recommended for the OUT1 and OUT2 step-down converters. Ensure that the inductor saturation current rating exceeds the peak inductor current, and the rated maximum DC inductor current exceeds the maximum output current. For lower load currents, the inductor current rating may be reduced. For most applications, use an inductor with a current rating 1.25 times the maximum required output current. For maximum efficiency, the inductor's DC resistance should be as low as possible. See Table 4 for component examples.

Boost Converter with White LED Driver (OUT3, MAX8662 Only)

The MAX8662 contains a boost converter, OUT3, which drives up to seven white LEDs in series at up to 30mA. The boost converter regulates its output voltage to maintain the bottom of the LED stack at 320mV. A 1MHz switching rate allows for a small inductor and small input and output capacitors, while also minimizing input and output ripple.

Reference Voltage

REF is a 1.5V regulated output that is available to drive the BRT input when the boost converter is enabled. This voltage can be used to control LED brightness by driving BRT through a resistor-divider.

Boost Overvoltage Protection (OVP)

OVP limits the maximum voltage of the boost output for protection against overvoltage due to open or disconnected LEDs. An external resistor between OUT3 and OVP, with an internal 20µA pulldown current from OVP to GND, sets the maximum boost output to:

$$V_{BOOST\_MAX} = (R_{OVP} \times 20\mu A) + 1.25V$$

For example, with R_{OVP} = 1.2MΩ, the OUT3 maximum voltage is set at 25.25V. The OVP circuit also provides soft-start to reduce inrush current by ramping the internal pulldown current from 0 to 20µA over 1.25ms at startup. The 20µA internal current is disconnected when EN3 goes low.

OUT3 can also be used as a voltage-output boost by setting R_{OVP} for the desired output voltage. When doing this, the output filter capacitor must be at least 1µF, and the compensation network should be a 0.01µF capacitor in series with a 10kΩ resistor from CC3 to ground.

Brightness Control (Voltage or PWM)

LED current is set by the voltage at BRT. The V_{BRT} range for adjusting output current from 1mA to 30mA is 50mV to 1.5V. Connecting BRT to a 1.5V reference voltage (such as REF) sets LED current to 30mA.

The EN3 input can also be driven by a logic-level PWM brightness control signal, such as that supplied by a microcontroller. The allowed PWM frequency range is from 1kHz to 100kHz. A 100% duty cycle corresponds to full current set by the BRT pin. The MAX8662 digitally decodes the PWM brightness signal and eliminates PWM ripple found in more common PWM brightness controls. As a result, no external filtering is needed to prevent intensity ripple at the PWM rate.

In order to properly distinguish between a DC or PWM control signal, the MAX8662 delays turn-on from the rising edge of EN3, and turn-off from the falling edge of EN3, by 2ms. If there are no more transitions in the EN3 signal after 2ms, EN3 assumes the control signal is DC and sets LED brightness based on the DC level. If two rising edges occur within 2ms, the circuit assumes the control is PWM and sets brightness based on the duty cycle.

OUT3 Inductor

For the white LED driver, OUT3, a 22µH inductor is recommended for most applications. For best efficiency, the inductor's DC resistance should also be as low as possible. See Table 4 for component examples.

OUT3 Compensation

An RC compensation network from CC3 to GND and an output capacitor (C14 of Figure 1) ensure boost converter stability. For WLED applications, connect a 0.22µF ceramic capacitor in series with a 1kΩ resistor from CC3 to GND and use a 0.1µF output capacitor. For fixed output voltage applications such as OLED, connect a 0.01µF ceramic capacitor in series with a 10kΩ resistor from CC3 to GND and use a 1µF capacitor. These components for fixed output voltage applications improve the load transient performance of the boost converter. The trade-off for this improved load transient performance is the larger (1µF) high-voltage (30V) output capacitor.

The RC compensation network from CC3 to GND affects the WLED driver's sink current ramp time. As shown in the *OUT3 Enable and Disable Response* graph in the *Typical Operating Characteristics* section, the OUT3 voltage ramps up in 1.25ms, but the WLED sink current of 30mA settles in 12ms. This 12ms is associated with the compensation of 1kΩ in series with 0.22µF. Smaller RC time constants reduce the WLED sink current ramp time.

OUT3 Diode Selection

The MAX8662 boost converter's high-switching frequency demands a high-speed rectification diode (D1) for optimum efficiency. A Schottky diode is recommended due to its fast recovery time and low forward-voltage drop. Ensure the diode's peak current rating exceeds the peak inductor current. In addition, the diode's reverse breakdown voltage must exceed V_{OUT3}. See Table 4 for component examples.

Linear Regulators (OUT4, OUT5, OUT6, and OUT7)

The MAX8662/MAX8663 contain four low-dropout, low-quiescent current, low-operating voltage linear regulators. The maximum output currents for OUT4, OUT5, OUT6, and OUT7 are 500mA, 150mA, 300mA, and 150mA, respectively. Each regulator has its own enable input. When enabled, a linear regulator soft-starts by ramping the outputs at 34V/ms. This limits inrush current when the regulators are enabled.

The LDO output voltages, OUT4, OUT5, OUT6, and OUT7 are pin programmable by SL1 and SL2 (Table 3). SL1 and SL2 are intended to be hardwired and cannot be driven by active logic. Changes to SL1 and SL2 after power-up are ignored.

VL Linear Regulator

VL is the output of a 3.3V linear regulator that powers the on-chip input limiter and charger control circuitry. VL is powered from DC and can provide up to 10mA when a DC source is present. Bypass VL to GND with a 0.1µF capacitor.

Regulator Enable Inputs (EN_)

The OUT1–OUT7 regulators have individual enable inputs. Drive EN_ high to initiate soft-start and enable OUT_. Drive EN_ low to disable OUT_. When disabled, each regulator (OUT1–OUT7) switches in an active pulldown resistor to discharge the output.

Soft-Start/Inrush Current

The MAX8662/MAX8663 implement soft-start on many levels to control inrush current and avoid collapsing source supply voltages. The input-voltage limit and battery charger have a 1.5ms soft-start time. All regulators also implement soft-start. White LED driver soft-start is accomplished by ramping the OVP current from 0 to 20µA in 1.25ms. During soft-start, the PWM controller forces 0% switching duty cycle to avoid an input current surge at turn-on.

Undervoltage and Overvoltage Lockout

DC UVLO

When the DC voltage is below the DC undervoltage threshold (V_{UVLO_DC}, typically 3.5V falling), the MAX8662/MAX8663 enter DC undervoltage lockout (DC UVLO). DC UVLO forces the power management circuits to a known dormant state until the DC voltage is high enough to allow the device to make accurate decisions. In DC UVLO, Q1 is open (Figure 2), the charger is disabled, $\overline{POK}$ is high-Z, and $\overline{CHG}$ is high-Z. The system load switch, Q2 (Figure 2) is closed in DC UVLO, allowing the battery to power the SYS node. All regulators are allowed to operate from the battery in DC UVLO.

Table 3. SL1 and SL2, Output Voltage Selection

CONNECT SL_ TO:		LINEAR REGULATOR OUTPUT VOLTAGES			
SL1	SL2	OUT4 (V)	OUT5 (V)	OUT6 (V)	OUT7 (V)
Open circuit	Open circuit	3.3	3.3	3.3	3.3
Ground	Open circuit	3.3	2.85	1.85	1.85
SYS	Open circuit	2.85	2.85	1.85	1.85
Open circuit	Ground	3.3	2.85	2.85	1.85
Ground	Ground	2.5	3.3	1.5	1.5
SYS	Ground	2.5	3.3	1.5	1.3
Open circuit	SYS	1.2	1.8	1.1	1.3
Ground	SYS	3.3	2.85	1.5	1.5
SYS	SYS	1.8	2.5	3.3	2.85

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DC OVLO

When the DC voltage is above the DC overvoltage threshold (V_{OVLO_DC}, typically 6.9V), the MAX8662/MAX8663 enter DC overvoltage lockout (DC OVLO). DC OVLO mode protects the MAX8662/MAX8663 and downstream circuitry from high-voltage stress up to 9V. In DC OVLO, VL is on, Q1 (Figure 2) is open, the charger is disabled, $\overline{POK}$ is high-Z, and $\overline{CHG}$ is high-Z. The system load switch Q2 (Figure 2) is closed in DC OVLO, allowing the battery to power SYS. All regulators are allowed to operate from the battery in DC OVLO.

SYS UVLO

When the SYS voltage falls below the SYS undervoltage threshold (V_{UVLO_SYS}, typically 2.4V falling), the MAX8662/MAX8663 enter SYS undervoltage lockout (SYS UVLO). SYS UVLO forces all regulators off. All regulators assume the states determined by the corresponding enable input (EN_) when the SYS voltage rises above V_{UVLO_SYS}.

Input-Limiter Thermal Limiting

The MAX8662/MAX8663 reduce input-limiter current by 5%/°C when its die temperature exceeds +100°C. The system load (SYS) has priority over charger current, so input current is first reduced by lowering charge current. If the junction temperature still reaches +120°C in spite of charge-current reduction, no current is drawn from DC, the battery supplies the entire system load, and SYS is regulated at 100mV below BAT. Note that this on-chip thermal-limiting circuitry is not related to, and operates independently from, the thermistor input.

Regulator Thermal-Overload Shutdown

The MAX8662/MAX8663 disable all charger, SYS, and regulator outputs (except VL) if the junction temperature rises above +165°C, allowing the device to cool. When the junction temperature cools by approximately 15°C, resume the state they held prior to thermal overload. Note that this on-chip thermal-protection circuitry is not related to, and operates independently from, the thermistor input. Also note that thermal-overload shutdown is a fail-safe mechanism. Proper thermal design should ensure that the junction temperature of the MAX8662/MAX8663 never exceeds the absolute maximum rating of +150°C.

Applications Information

Step-Down Converters (OUT1 and OUT2)

Capacitor Selection

The input capacitor in a DC-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than the input source's output impedance so that high-frequency switching currents do not pass through the input source. The DC-DC converter output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are highly recommended for both input and output capacitors due to their small size, low ESR, and small temperature coefficients.

See Table 4 for example OUT1/OUT2 input and output capacitors and manufacturers.

Table 4. External Components List (See Figure 1)

COMPONENT	FUNCTION	PART
C1	Input filter capacitor	4.7µF ±10%, 16V X5R ceramic capacitor Murata GRM188R61C105KA93B or Taiyo Yuden EMK107 BJ105KA
C2, C3	VL filter capacitor	0.1µF ±10%, 10V X5R ceramic capacitor (0402) Murata GRM 155R61A104KA01 or TDK C1005X5R1A104K
C4, C6	Buck input bypass capacitors	4.7µF ±10%, 6.3V X5R ceramic capacitors (0603) Mutara GRM188R60J475KE
C5, C7	Step-down output filter capacitors	2 x 10µF ±10%, 6.3V X5R ceramic capacitors (0805) Murata GRM219R60J106KE19
C8, C9	Linear regulator input filter capacitors	1.0µF ±10%, 16V X5R ceramic capacitors (0603) Murata GRM188R61C105KA93B or Taiyo Yuden EMK107 BJ105KA
C10	SYS output bypass capacitor	10µF ±10%, 6.3V X5R ceramic capacitor
C11	Battery bypass capacitor	4.7µF ±10%, 6.3V X5R ceramic capacitor
C12	Charger timing capacitor	0.068µF ±10%, 10V X5R ceramic capacitor (0402) TDK C1005X5R1A683K

Table 4. External Components List (See Figure 1) (continued)

COMPONENT	FUNCTION	PART
C13	Boost input bypass capacitor	1.0µF ±10%, 16V X5R ceramic capacitor (0603) Murata GRM188R61C105KA93B or Taiyo Yuden EMK107BJ105KA
C14	Step-up output filter capacitor	0.1µF ±10%, 50V X7R ceramic capacitor (0603) Murata GRM188R71H104KA93 or Taiyo Yuden UMK107BJ104KA
C15	Step-up compensation capacitor	0.22µF ±10%, 10V X5R ceramic capacitor (0402) Murata GRM155R61A224KE19
C16	Linear regulator output filter capacitor	4.7µF ±10%, 6.3V X5R ceramic capacitor (0603) Murata GRM188R60J475KE19
C17, C19	Linear regulator output filter capacitors	1.0µF ±10%, 6.3V X5R ceramic capacitors (0603) Murata GRM188R60J105KA01
C18	Linear regulator output filter capacitor	2.2µF ±10%, 6.3V X5R ceramic capacitor (0603) Murata GRM185R60J225KE26
D1	Boost rectifier	200mA, 30V Schottky diode (SOD-323) Central CMDSH2-3
D2–D8	Display backlighting	30mA surface-mount white LEDs Nichia NSCW215T
D9	CS clamp	100mA silicon signal diode Central CMOD4448
L1	OUT1 step-down inductor	3.3µH inductor TOKO DE2818C 1072AS-3R3M, 1.6A, 50mΩ
L2	OUT2 step-down inductor	4.7µH inductor TOKO DE2818C 1072AS-4R7M, 1.3A, 70mΩ
L3	OUT3 step-up inductor	22µH inductor Murata LQH32CN220K53, 250mA, 0.71Ω DCR (3.2mm x 2.5mm x 1.55mm) or TDK VLF3012AT-220MR33, 330mA, 0.76Ω DCR (2.8mm x 2.6mm x 1.2mm)
R1, R7	Logic output pullup resistors	100kΩ
R2–R5	Step-down feedback resistors	R3 and R5 are 200kΩ ±0.1%; R2 and R4 depend on output voltage (±0.1%)
R6	Negative TC thermistor	Phillips NTC thermistor P/N 2322-640-63103 10kΩ ±5% at +25°C
R8	Input current-limit programming resistor	1.5kΩ ±1%, for 2A limit
R9	Fast charge-current programming resistor	3kΩ ±1%, for 777mA charging
R10	Step-up overvoltage feedback resistor	1.2MΩ ±1%, for 25V max output

Power Dissipation

The MAX8662/MAX8663 have a thermal-limiting circuitry, as well as a shutdown feature to protect the IC from damage when the die temperature rises. To allow the maximum charging current and load current on each regulator, and to prevent thermal overload, it is important to ensure that the heat generated by the MAX8662/MAX8663 is dissipated into the PCB. The package's exposed paddle must be soldered to the PCB, with multiple vias tightly packed under the exposed paddle to ensure optimum thermal contact to the ground plane.

Table 5 shows the thermal characteristics of the MAX8662/MAX8663 packages. For example, the junction-to-case thermal resistance (θ_{JC}) of the MAX8663 is 1.7°C/W. When properly mounted on a multilayer PCB, the junction-to-ambient thermal resistance (θ_{JA}) is typically 28°C/W.

PCB Layout and Routing

High switching frequencies and relatively large peak currents make the PCB layout a very important aspect of design. Good design minimizes ground bounce, excessive EMI on the feedback paths, and voltage gradients in the ground plane, which can result in instability or regulation errors.

A separate low-noise analog ground plane containing the reference, linear regulator, signal ground, and GND must connect to the power-ground plane at only one point to minimize the effects of power-ground currents. PG_, DC power, and battery grounds must connect directly to the power-ground plane. Connect GND to the exposed paddle directly under the IC. Use multiple tightly spaced vias to the ground plane under the exposed paddle to help cool the IC.

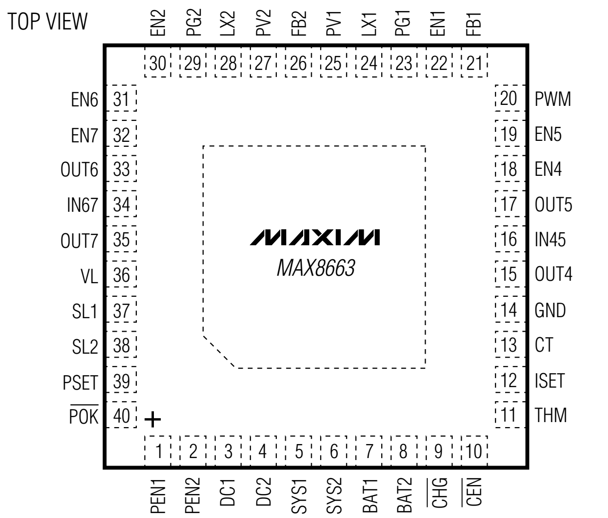
Position input capacitors from DC, SYS, BAT, PV1, and PV2 to the power-ground plane as close as possible to the IC. Connect input capacitors and output capacitors from inputs of linear regulators to low-noise analog ground as close as possible to the IC. Connect the inductors, output capacitors, and feedback resistors as close to the IC as possible and keep the traces short, direct, and wide.

Refer to the MAX8662/MAX8663 evaluation kit for a suitable PCB layout example.

Table 5. MAX8662/MAX8663 Package Thermal Characteristics

	48-PIN THIN QFN (6mm x 6mm)		40-PIN THIN QFN (5mm x 5mm)	
	SINGLE-LAYER PCB	**MULTILAYER PCB**	**SINGLE-LAYER PCB**	**MULTILAYER PCB**
CONTINUOUS POWER DISSIPATION	2105.3mW Derate 26.3mW/°C above +70°C	2963.0mW Derate 37.0mW/°C above +70°C	1777.8mW Derate 22.2mW/°C above +70°C	2857.1mW Derate 35.7mW/°C above +70°C
θ_{JA}	38°C/W	27°C/W	45°C/W	28°C/W
θ_{JC}	1.4°C/W	1.4°C/W	1.7°C/W	1.7°C/W

Pin Configurations (continued)



TQFN
(5mm x 5mm)

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4866-1	**21-0141**	**90-0057**
40 TQFN-EP	T4055-1	**21-0140**	**90-0016**

Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/07	Initial release	—
1	12/08	Updated Figure 1	21
2	12/10	Updated *Electrical Characteristics* table, TOCs 29, 38, 42, 49, 56, 63, and 70, Figures 3, 4, 5, and 6, *OUT3 Compensation* section	5, 6, 7, 11, 13–17, 23, 24, 25, 27, 28, 29