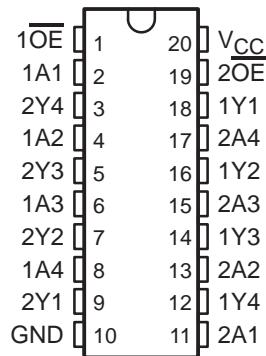


- Operates From 2.7 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.9 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



### description/ordering information

This octal buffer/line driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCZ244A is organized as two 4-bit line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 20	SN74LVCZ244AN	SN74LVCZ244AN
	SOIC – DW	Tube of 25	SN74LVCZ244ADW	LVCZ244A
		Reel of 2000	SN74LVCZ244ADWR	
	SOP – NS	Reel of 2000	SN74LVCZ244ANSR	LVCZ244A
	SSOP – DB	Reel of 2000	SN74LVCZ244ADBR	CV244A
	TSSOP – PW	Tube of 70	SN74LVCZ244APW	CV244A
		Reel of 2000	SN74LVCZ244APWR	
		Reel of 250	SN74LVCZ244APWT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74LVCZ244A

## OCTAL BUFFER/DRIVER

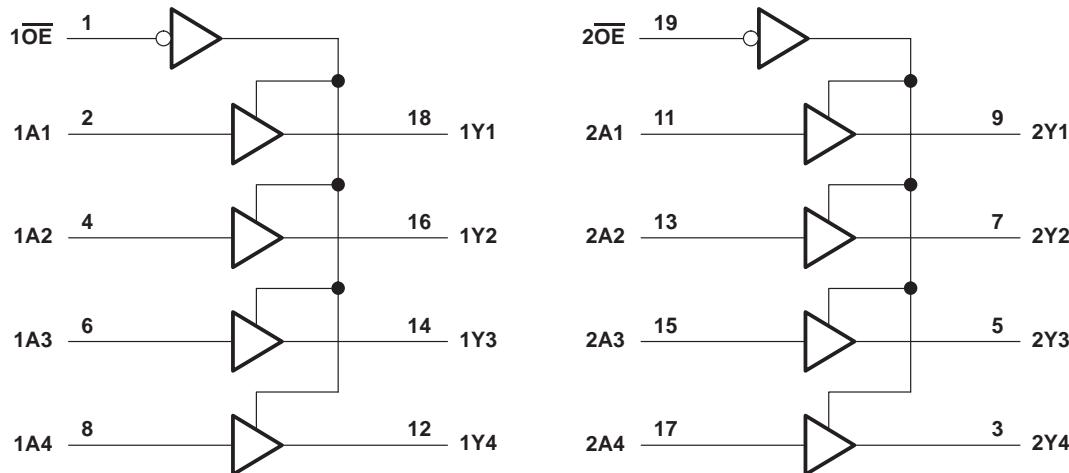
### WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
PW package .....	83°C/W
Storage temperature range, $T_{STG}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

**recommended operating conditions (see Note 4)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3-state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2.7\text{ V}$		-12	mA
		$V_{CC} = 3\text{ V}$		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7\text{ V}$		12	mA
		$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			6	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		150		$\mu\text{s/V}$
$T_A$	Operating free-air temperature		-40	85	$^{\circ}\text{C}$

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>†</sup>	MAX	UNIT
$V_{OH}$	$I_{OH} = -100\text{ }\mu\text{A}$	2.7 V to 3.6 V	$V_{CC}-0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
	$I_{OH} = -24\text{ mA}$	3 V	2.4			
$V_{OL}$	$I_{OL} = 100\text{ }\mu\text{A}$	2.7 V to 3.6 V		0.2		V
	$I_{OL} = 12\text{ mA}$	2.7 V		0.4		
	$I_{OL} = 24\text{ mA}$	3 V		0.55		
$I_I$	$V_I = 0$ to 5.5 V	3.6 V		$\pm 5$	$\mu\text{A}$	
$I_{off}$	$V_O = 0$ to 5.5 V	0		$\pm 5$	$\mu\text{A}$	
$I_{OZ}$	$V_O = 0$ to 5.5 V	3.6 V		$\pm 5$	$\mu\text{A}$	
$I_{OZPU}$	$V_O = 0.5\text{ V to }2.5\text{ V}, \overline{OE} = \text{don't care}$	0 to 1.5 V		$\pm 5$	$\mu\text{A}$	
$I_{OZPD}$	$V_O = 0.5\text{ V to }2.5\text{ V}, \overline{OE} = \text{don't care}$	1.5 V to 0		$\pm 5$	$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}$ or GND	3.6 V		100		$\mu\text{A}$
	$3.6\text{ V} \leq V_I \leq 5.5\text{ V}^{\ddagger}$			100		
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND	2.7 V to 3.6 V		100	$\mu\text{A}$	
$C_I$	$V_I = V_{CC}$ or GND	3.3 V		3.5	pF	
$C_O$	$V_O = V_{CC}$ or GND	3.3 V		5.5	pF	

<sup>†</sup>All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup>This applies in the disabled state only.

**SN74LVCZ244A**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	6.9	1.5	5.9	ns	
t <sub>en</sub>	OE	A or B	8.6	1.5	7.6	ns	
t <sub>dis</sub>	OE	A or B	6.8	1.5	6.5	ns	

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 3.3 V		UNIT
		TYP		
C <sub>pd</sub> Power dissipation capacitance per buffer/driver	Outputs enabled	40		pF
	Outputs disabled	3		

PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 2.7\text{ V AND }3.3\text{ V} \pm 0.3\text{ V}$

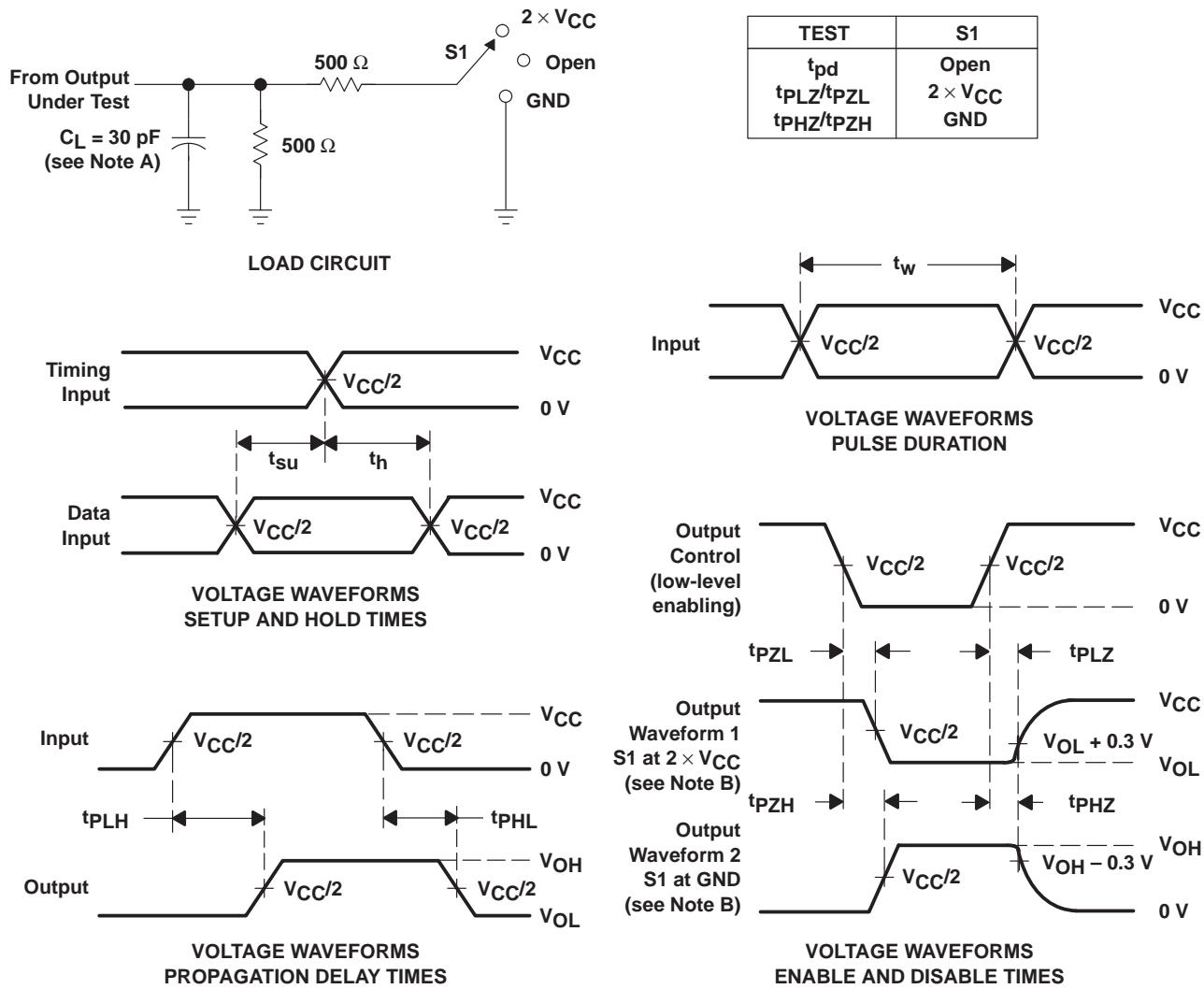


Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVCZ244ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ADB RG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LVCZ244ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LVCZ244ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ244APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

**(2) Eco Plan** - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

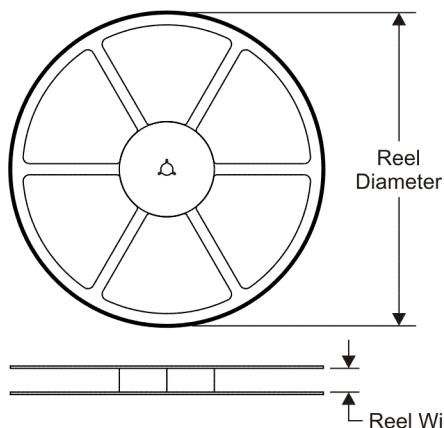
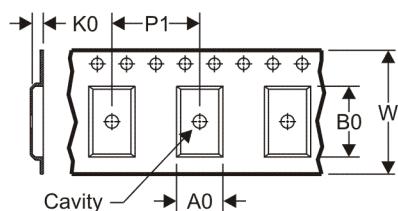
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

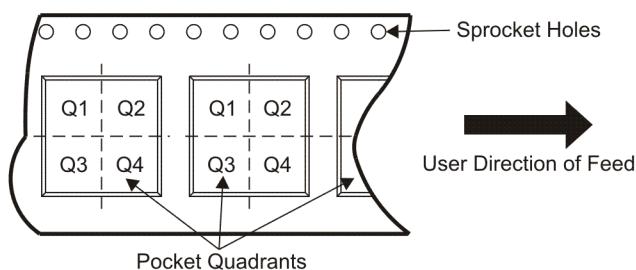
**(3) MSL, Peak Temp.** -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


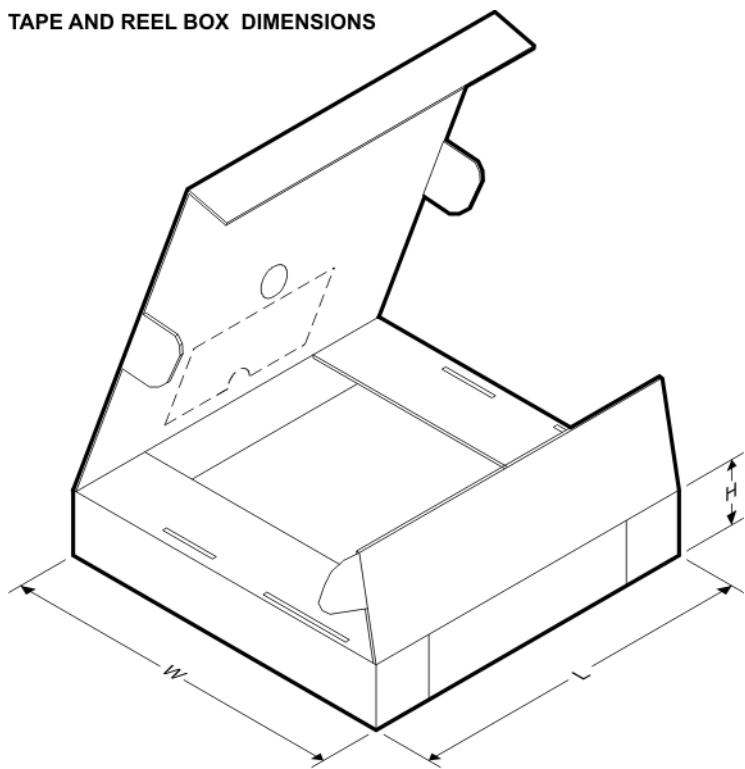
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCZ244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCZ244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVCZ244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



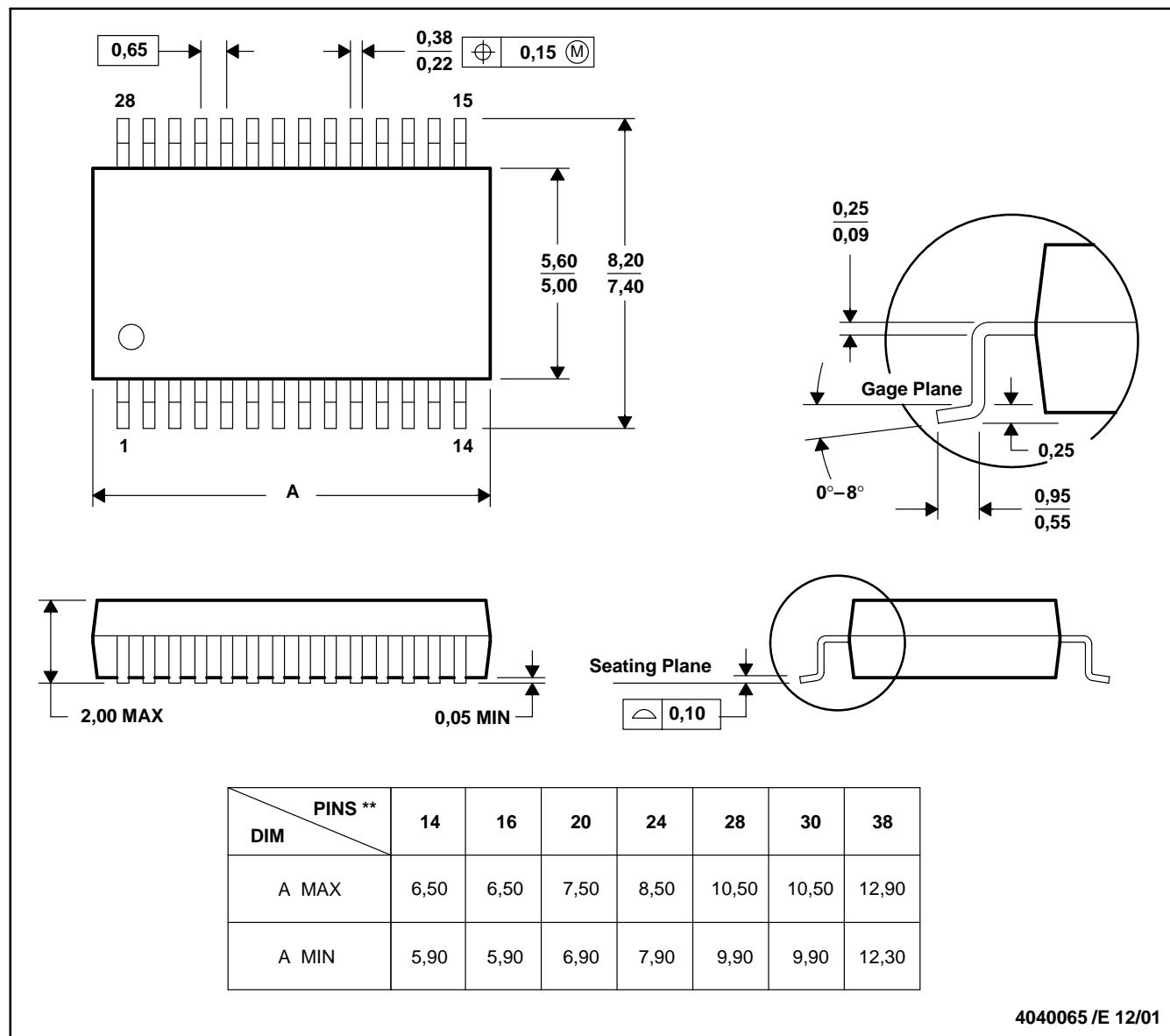
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCZ244ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LVCZ244ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LVCZ244APWR	TSSOP	PW	20	2000	346.0	346.0	33.0

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



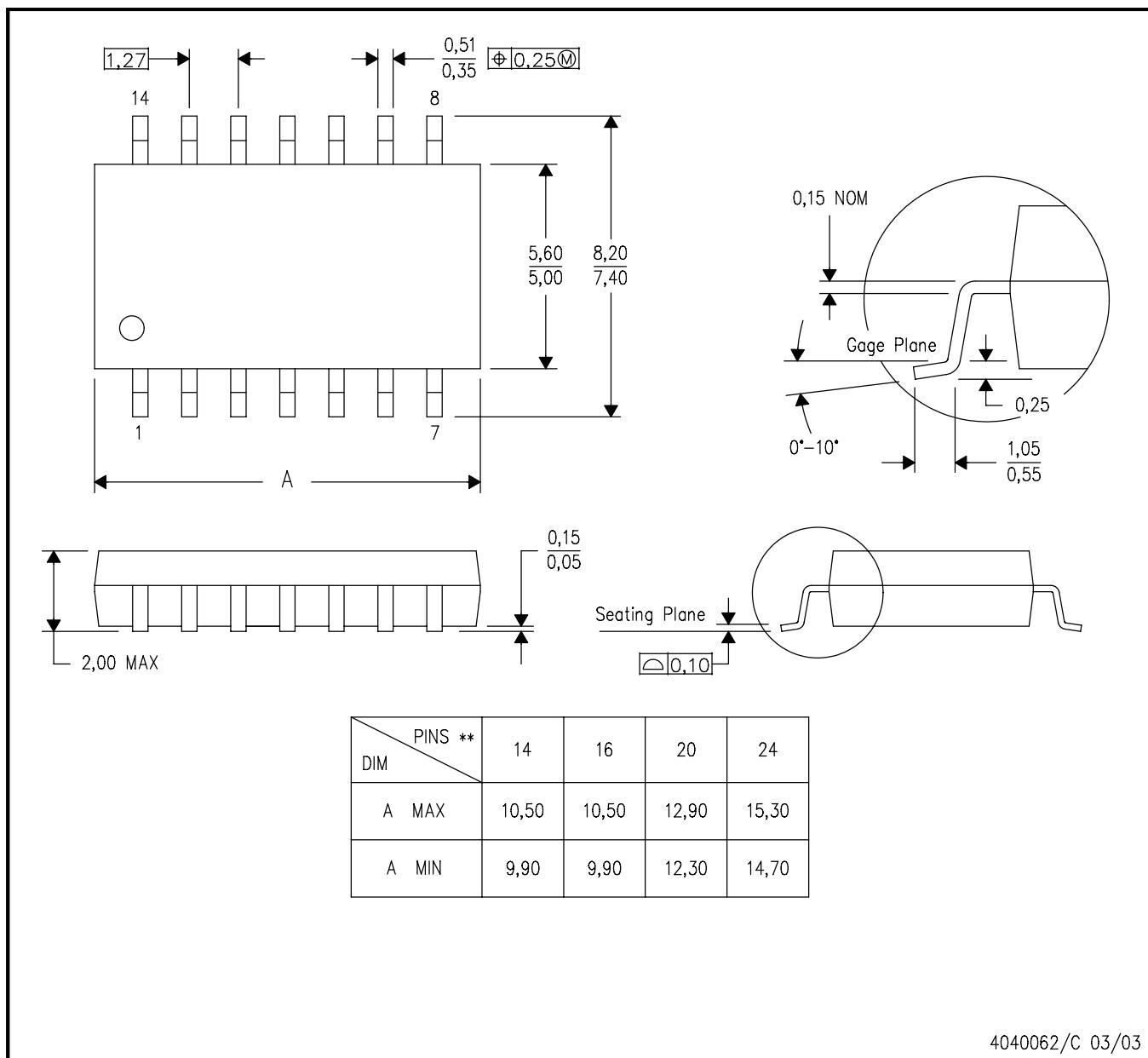
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



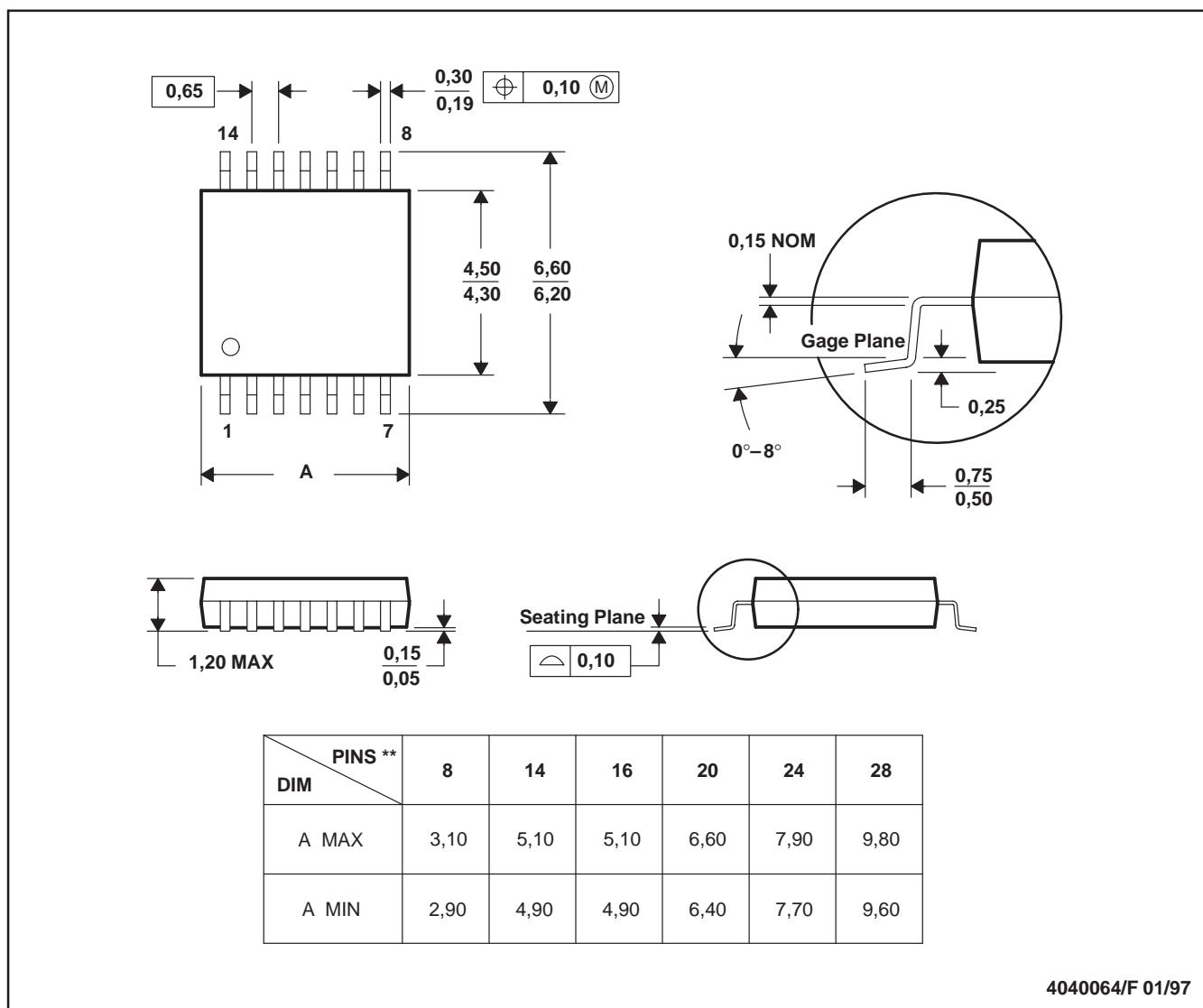
4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

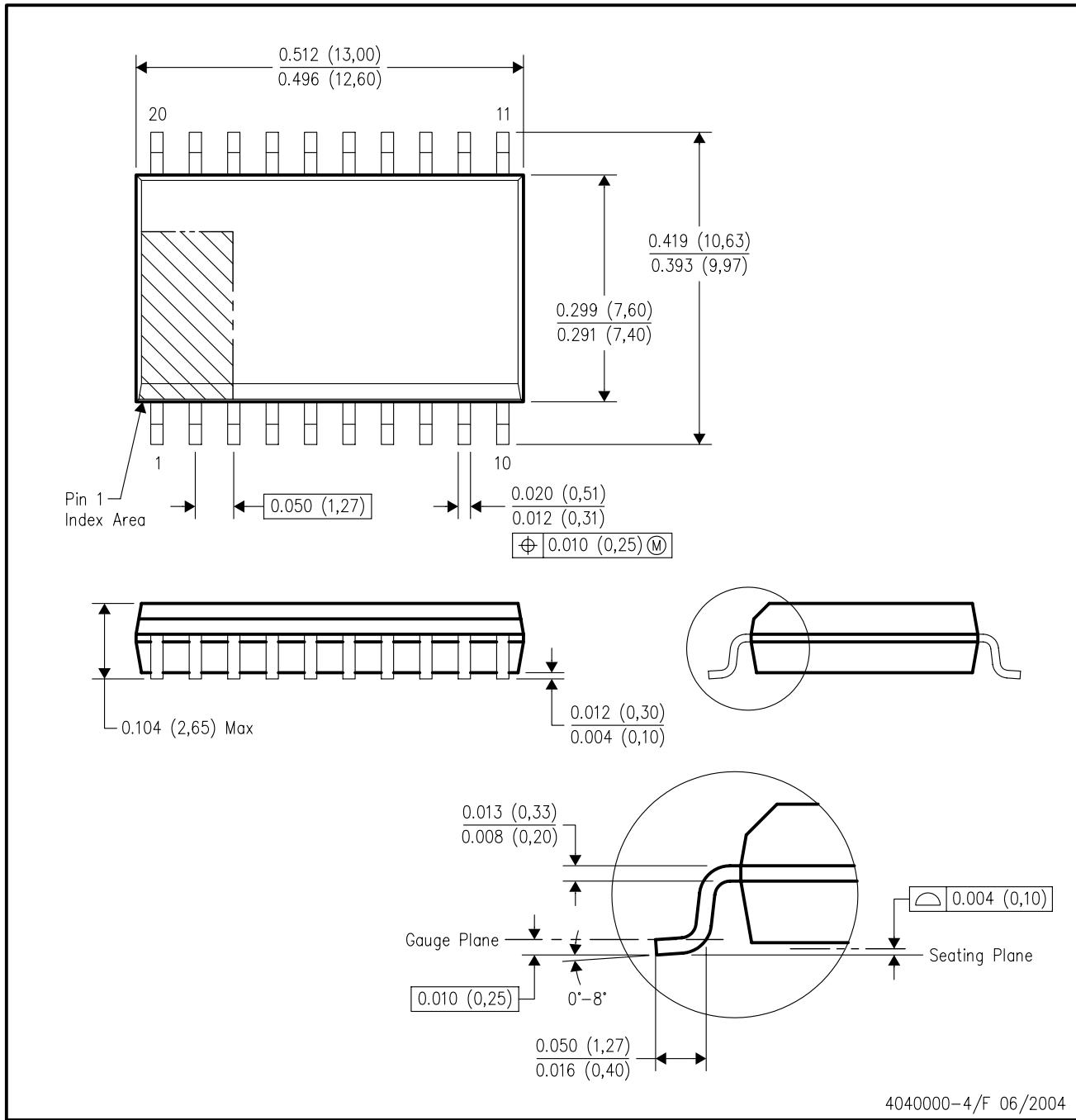


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



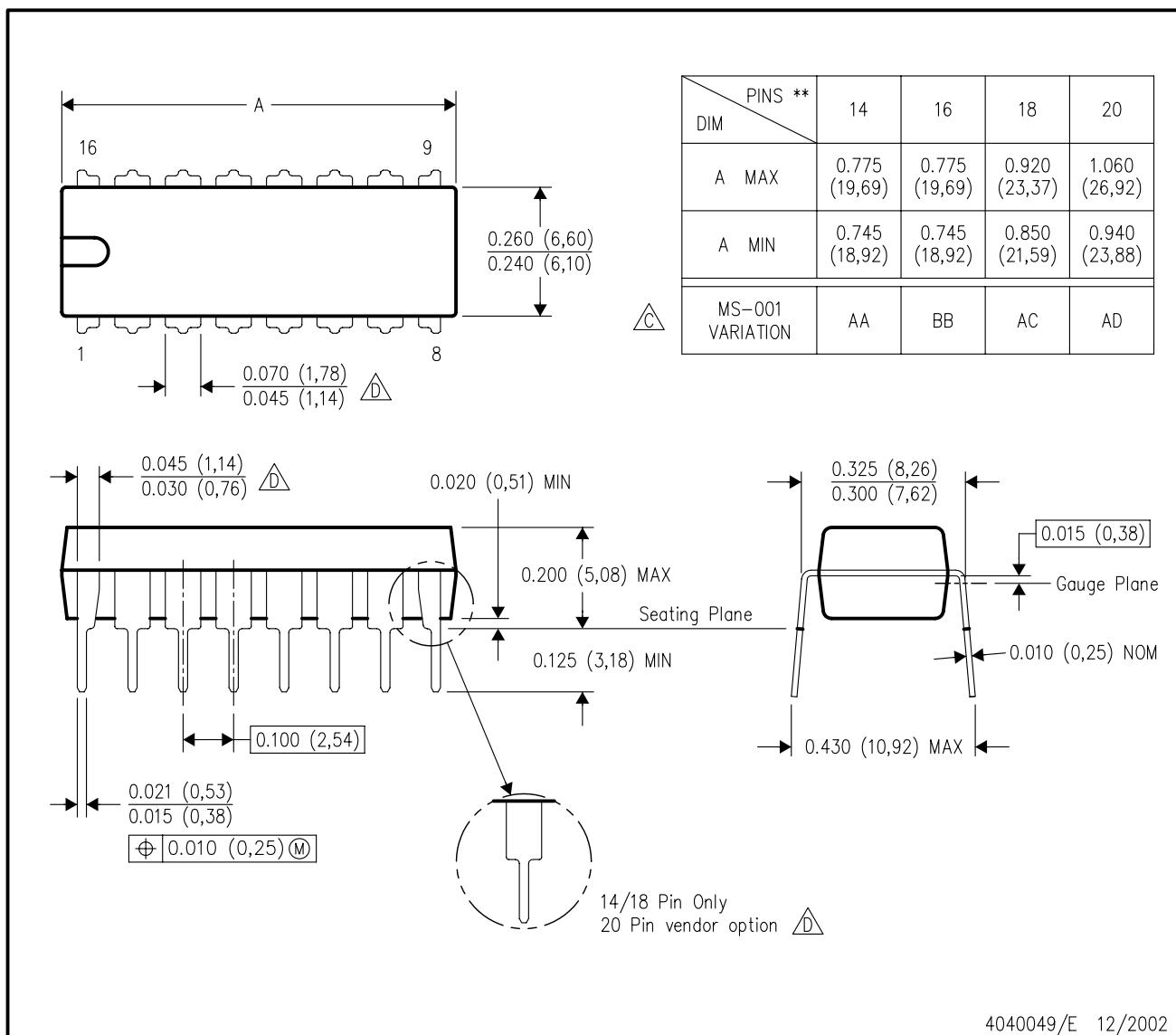
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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