ISL6522

Buck and Synchronous Rectifier Pulse-Width Modulator (PWM) Controller

FN9030
Rev 8.00
Mar 10, 2006

The ISL6522 provides complete control and protection for a DC-DC converter optimized for high-performance micro-processor applications. It is designed to drive two N-Channel MOSFETs in a synchronous rectified buck topology. The ISL6522 integrates all of the control, output adjustment, monitoring and protection functions into a single package.

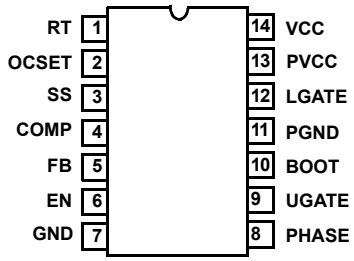
The output voltage of the converter can be precisely regulated to as low as 0.8V, with a maximum tolerance of ±1% over temperature and line voltage variations.

The ISL6522 provides simple, single feedback loop, voltage-mode control with fast transient response. It includes a 200kHz free-running triangle-wave oscillator that is adjustable from below 50kHz to over 1MHz. The error amplifier features a 15MHz gain-bandwidth product and 6V/µs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty ratio ranges from 0–100%.

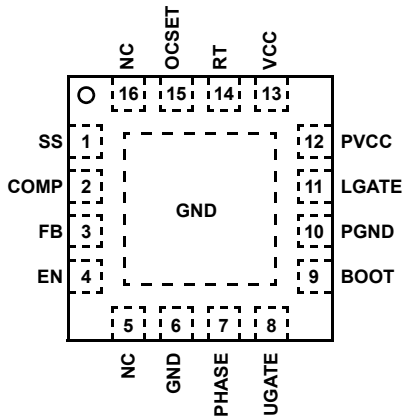
The ISL6522 protects against overcurrent conditions by inhibiting PWM operation. The ISL6522 monitors the current by using the $r_{DS(ON)}$ of the upper MOSFET which eliminates the need for a current sensing resistor.

Pinouts

SOIC, TSSOP
TOP VIEW



QFN
TOP VIEW



Features

- Drives two N-Channel MOSFETs
- Operates from +5V or +12V input
- Simple single-loop control design
  - Voltage-mode PWM control
- Fast transient response
  - High-bandwidth error amplifier
  - Full 0–100% duty ratio
- Excellent output voltage regulation
  - 0.8V internal reference
  - ±1% over line voltage and temperature
- Overcurrent fault monitor
  - Does not require extra current sensing element
  - Uses MOSFETs $r_{DS(ON)}$
- Converter can source and sink current
- Small converter size
  - Constant frequency operation
  - 200kHz free-running oscillator programmable from 50kHz to over 1MHz
- 14-lead SOIC and TSSOP package and 16-lead 5x5mm QFN Package
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads-Product Outline.
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
- Pb-free plus anneal available (RoHS compliant)

Applications

- Power supply for Pentium®, Pentium Pro, PowerPC® and AlphaPC™ microprocessors
- High-power 5V to 3.xV DC-DC regulators
- Low-voltage distributed power supplies

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6522CB	ISL6522CB	0 to 70	14 Ld SOIC	M14.15
ISL6522CBZ (Note)	6522CBZ	0 to 70	14 Ld SOIC (Pb-free)	M14.15
ISL6522CBZA (Note)	6522CBZ	0 to 70	14 Ld SOIC (Pb-free)	M14.15
ISL6522IB	ISL6522IB	-40 to 85	14 Ld SOIC	M14.15
ISL6522IBZ (Note)	6522IBZ	-40 to 85	14 Ld SOIC (Pb-free)	M14.15
ISL6522CV	ISL6522CV	0 to 70	14 Ld TSSOP	M14.173
ISL6522CVZ (Note)	ISL6522CVZ	0 to 70	14 Ld TSSOP (Pb-free)	M14.173
ISL6522IV	ISL6522IV	-40 to 85	14 Ld TSSOP	M14.173
ISL6522IVZ (Note)	ISL6522IVZ	-40 to 85	14 Ld TSSOP (Pb-free)	M14.173

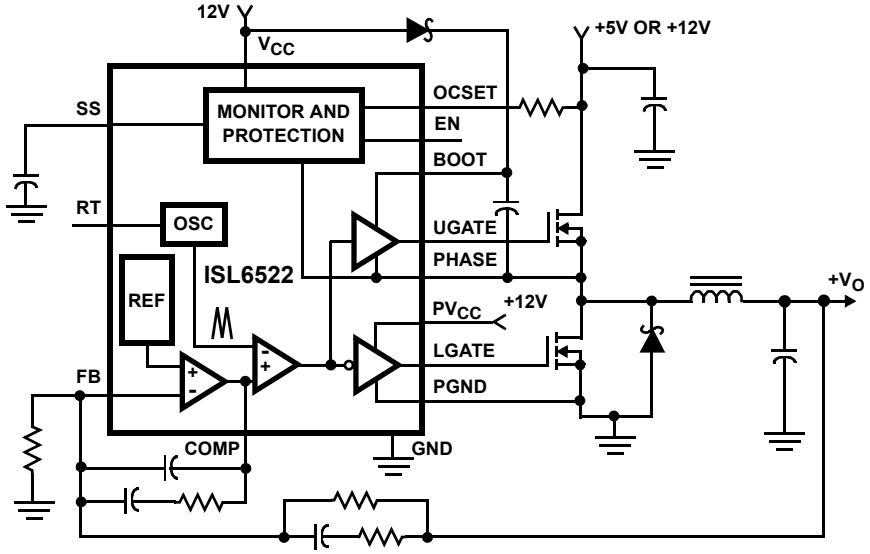
Ordering Information (Continued)

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6522CR	ISL6522CR	0 to 70	16 Ld 5x5 QFN	L16.5x5B
ISL6522CRZ (Note)	ISL6522CRZ	0 to 70	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6522IR	ISL6522IR	-40 to 85	16 Ld 5x5 QFN	L16.5x5B
ISL6522IRZ (Note)	ISL6522IRZ	-40 to 85	16 Ld 5x5 QFN (Pb-free)	L16.5x5B

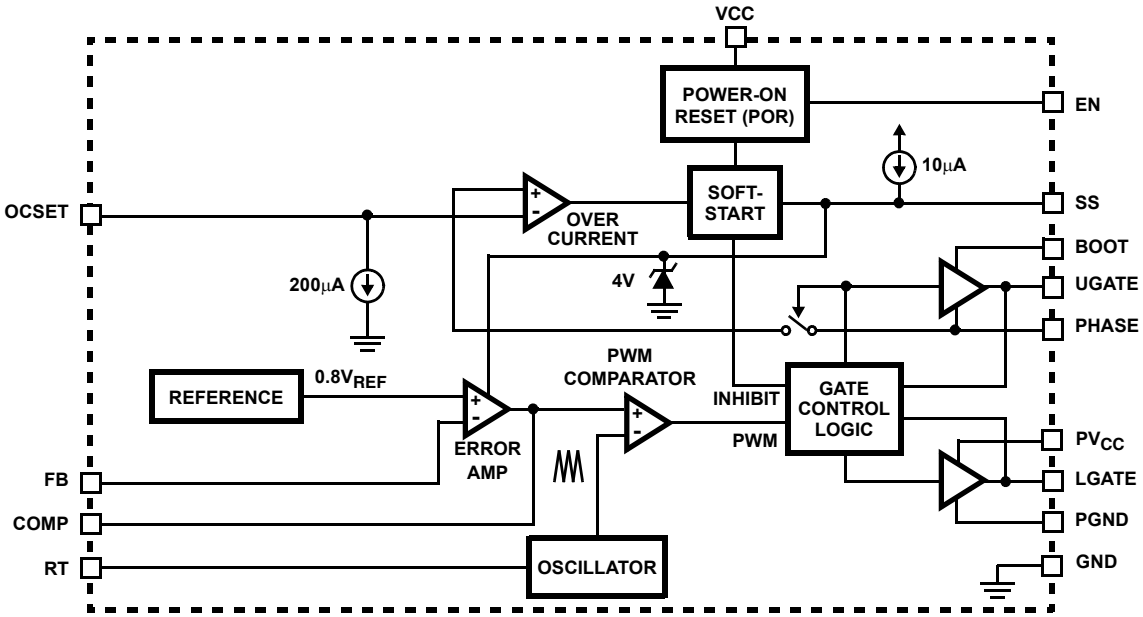
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Add “-T” for tape and reel.

Typical Application



Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +15.0V
Boot Voltage, V_{BOOT} - V_{PHASE} . . . . . +15.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . +12V ±10%
Ambient Temperature Range, ISL6522C. . . . . 0°C to 70°C
Ambient Temperature Range, ISL6522I. . . . . -40°C to 85°C
Junction Temperature Range, ISL6522C. . . . . 0°C to 125°C
Junction Temperature Range, ISL6522I . . . . . -40°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	67	n/a
TSSOP Package (Note 1)	95	n/a
QFN Package (Notes 2, 3).	36	5

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a highs effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. SeeTech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY CURRENT						
Nominal Supply	I_{CC}	EN = V_{CC}; UGATE and LGATE Open	-	5	-	mA
Shutdown Supply		EN = 0V	-	50	100	µA
POWER-ON RESET						
Rising V_{CC} Threshold		V_{OCSET} = 4.5VDC	-	-	10.4	V
Falling V_{CC} Threshold		V_{OCSET} = 4.5VDC	8.1	-	-	V
Enable-Input Threshold Voltage		ISL6522C, V_{OCSET} = 4.5VDC	0.8	-	2.0	V
		ISL6522I, V_{OCSET} = 4.5VDC	0.8	-	2.1	V
Rising V_{OCSET} Threshold			-	1.27	-	V
OSCILLATOR						
Free Running Frequency		ISL6522C, R_T = OPEN, V_{CC} = 12	175	200	230	kHz
		ISL6522I, R_T = OPEN, V_{CC} = 12	160	200	230	
Total Variation		6kΩ < R_T to GND < 200kΩ	-20	-	+20	%
Ramp Amplitude	ΔV_{OSC}	R_T = OPEN	-	1.9	-	V_{P-P}
REFERENCE						
Reference Voltage Tolerance	V_{REF}	Commercial	-1	-	1	%
		Industrial	-2	-	+1	%
Reference Voltage			-	0.800	-	V
ERROR AMPLIFIER						
DC Gain			-	88	-	dB
Gain-Bandwidth Product	GBW		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	V/µs
GATE DRIVERS						
Upper Gate Source	I_{UGATE}	V_{BOOT} - V_{PHASE} = 12V, V_{UGATE} = 6V	350	500	-	mA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Upper Gate Sink	R_{UGATE}	ISL6522C, I_{LGATE} = 0.3A	-	5.5	10	Ω
		ISL6522I, I_{LGATE} = 0.3A	-	5.5	7.2	Ω
Lower Gate Source	I_{LGATE}	V_{CC} = 12V, V_{LGATE} = 6V	300	450	-	mA
Lower Gate Sink	R_{LGATE}	ISL6522C, I_{LGATE} = 0.3A	-	3.5	6.5	Ω
		ISL6522I, I_{LGATE} = 0.3A	-	3.5	4.5	Ω
PROTECTION						
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5VDC	170	200	230	µA
Soft-Start Current	I_{SS}		-	10	-	µA

Typical Performance Curves

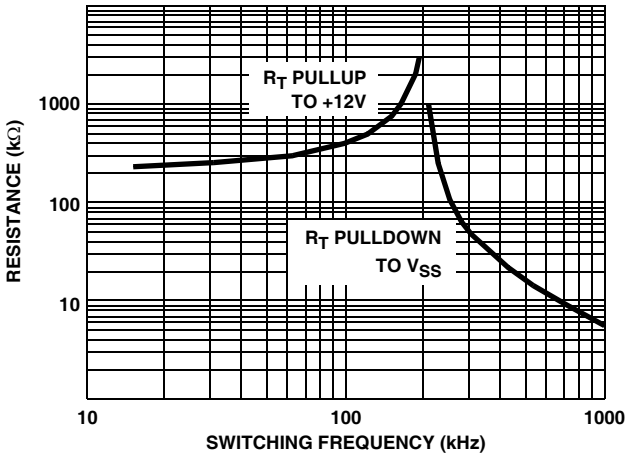


FIGURE 1. R_T RESISTANCE vs FREQUENCY

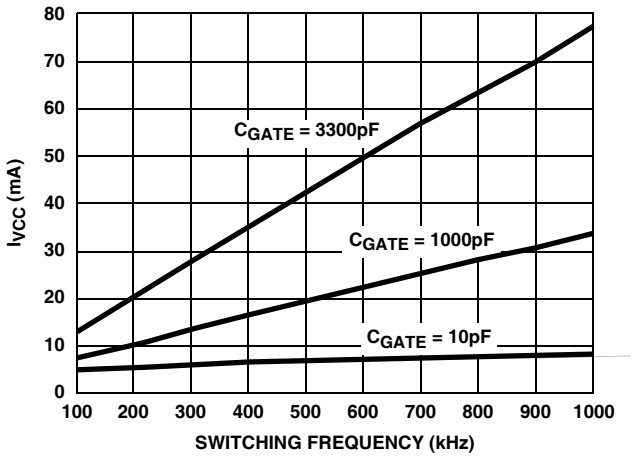
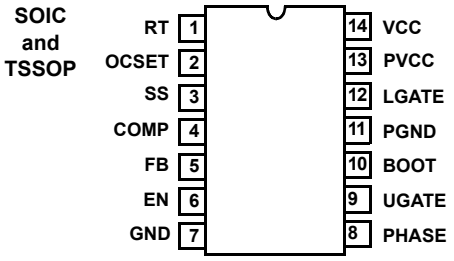
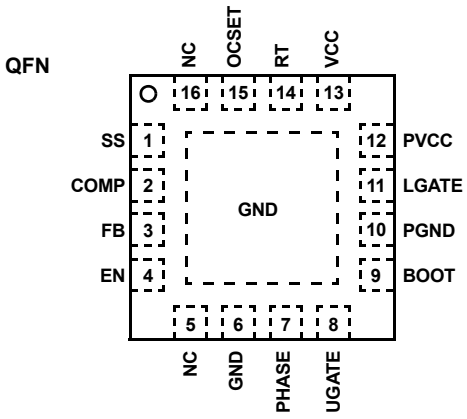


FIGURE 2. BIAS SUPPLY CURRENT vs FREQUENCY

Functional Pin Descriptions





RT

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$Fs \approx 200kHz + \frac{5 \bullet 10^6}{R_T} \quad (R_T \text{ to GND})$$

Conversely, connecting a pull-up resistor (R_T) from this pin to V_{CC} reduces the switching frequency according to the following equation:

$$Fs \approx 200kHz - \frac{4 \bullet 10^7}{R_T} \quad (R_T \text{ to 12V})$$

OCSET

Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 200µA current source (I_{OCS}), and the upper MOSFET on-resistance ($r_{DS(ON)}$) set the converter overcurrent (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{r_{DS(ON)}}$$

An overcurrent trip cycles the soft-start function.

SS

Connect a capacitor from this pin to ground. This capacitor, along with an internal 10µA current source, sets the soft-start interval of the converter.

COMP and FB

COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.

EN

This pin is the open-collector enable pin. Pull this pin below 1V to disable the converter. In shutdown, the soft-start pin is discharged and the UGATE and LGATE pins are held low.

GND

Signal ground for the IC. All voltage levels are measured with respect to this pin.

PHASE

Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for overcurrent protection. This pin also provides the return path for the upper gate drive.

UGATE

Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the upper MOSFET. This pin is also monitored by the adaptive shoot through protection circuitry to determine when the upper MOSFET has turned off.

BOOT

This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.

PGND

This is the power ground connection. Tie the lower MOSFET source to this pin.

LGATE

Connect LGATE to the lower MOSFET gate. This pin provides the gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot through protection circuitry to determine when the lower MOSFET has turned off.

PVCC

Provide a bias supply for the lower gate drive to this pin.

VCC

Provide a 12V bias supply for the chip to this pin.

Functional Description

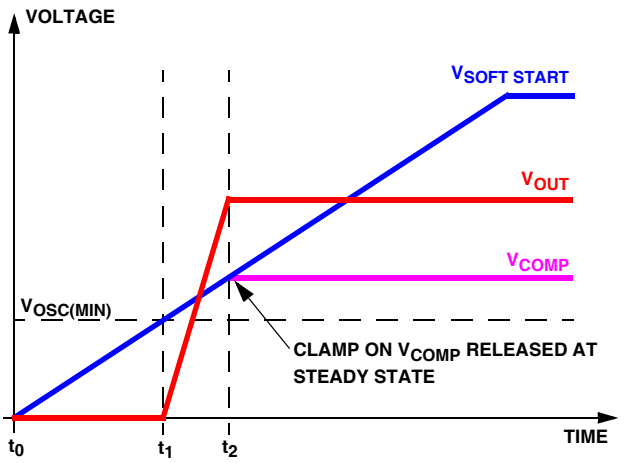
Initialization

The ISL6522 automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages and the enable (EN) pin. The POR monitors the bias voltage at the VCC pin and the input voltage (V_{IN}) on the OCSET pin. The level on OCSET is equal to V_{IN} Less a fixed voltage drop (see overcurrent protection). With the EN pin held to V_{CC}, the POR function initiates soft-start operation after both input supply voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and V_{CC} are equivalent and the +12V power source must exceed the rising V_{CC} threshold before POR initiates operation.

The POR function inhibits operation with the chip disabled (EN pin low). With both input supplies above their POR thresholds, transitioning the EN pin high initiates a soft-start interval.

Soft-Start

The POR function initiates the soft-start sequence. An internal 10µA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. Soft-start clamps the error amplifier output (COMP pin) to the SS pin voltage. Figure 3 shows the soft-start interval. At t_1 in Figure 3, the SS and COMP voltages reach the valley of the oscillator's triangle wave. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). This interval of increasing pulse width continues to t2, at which point the output is in regulation and the clamp on the COMP pin is released. This method provides a rapid and controlled output voltage rise.



$$t_1 = \frac{C_{SS}}{I_{SS}} \cdot V_{OSC(MIN)}$$

$$t_{SoftStart} = t_2 - t_1 = \frac{C_{SS}}{I_{SS}} \cdot \frac{V_{OUT_{SteadyState}}}{V_{IN}} \cdot \Delta V_{OSC}$$

Where: C_{SS} = Soft Start Capacitor
I_{SS} = Soft Start Current = 10µA
$V_{OSC(MIN)}$ = Bottom of Oscillator = 1.35V
V_{IN} = Input Voltage
ΔV_{OSC} = Peak to Peak Oscillator Voltage = 1.9V
$V_{OUTSteadyState}$ = Steady State Output Voltage

FIGURE 3. SOFT-START INTERVAL

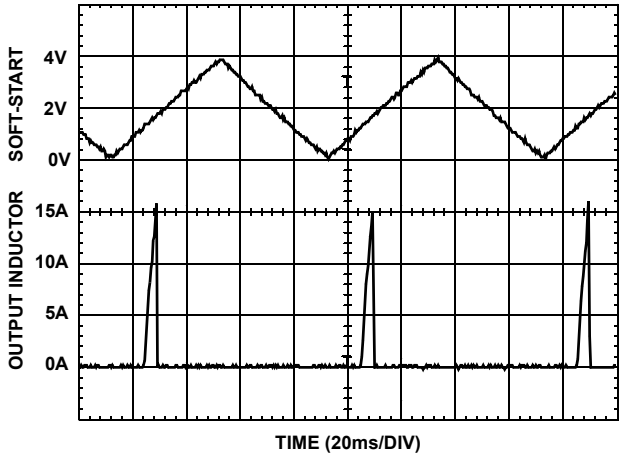


FIGURE 4. OVERCURRENT OPERATION

Overcurrent Protection

The overcurrent function protects the converter from a shorted output by using the upper MOSFETs on-resistance, $r_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The overcurrent function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the overcurrent trip level. An internal 200µA (typical) current sink develops a voltage across R_{OCSET} that is reference to V_{IN}. When the voltage across the upper MOSFET (also referenced to V_{IN}) exceeds the voltage across R_{OCSET}, the overcurrent function initiates a soft-start sequence. The soft-start function discharges C_{SS} with a 10µA current sink and inhibits PWM operation. The soft-start function recharges C_{SS}, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging C_{SS}, the soft-start function inhibits PWM operation while fully charging C_{SS} to 4V to complete its cycle. Figure 4 shows this operation with an overload condition. Note that the inductor current increases to over 15A during the C_{SS} charging interval and causes an overcurrent trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 4 is 2.5W.

The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \bullet R_{OCSET}}{r_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source (200µA is typical). The OC trip point varies mainly due to the MOSFETs $r_{DS(ON)}$ variations. To avoid overcurrent tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

The maximum $r_{DS(ON)}$ at the highest junction temperature.

1. The minimum I_{OCSET} from the specification table.
2. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled *Output Inductor Selection*.

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Current Sinking

The ISL6522 incorporates a MOSFET shoot-through protection method which allows a converter to sink current as well as source current. Care should be exercised when designing a converter with the ISL6522 when it is known that the converter may sink current.

When the converter is sinking current, it is behaving as a boost converter that is regulating its input voltage. This means that the converter is boosting current into the V_{IN} rail, the voltage that is being down-converted. If there is nowhere for this current to go, such as to other distributed loads on the V_{IN} rail, through a voltage limiting protection device, or other methods, the capacitance on the V_{IN} bus will absorb the current. This situation will cause the voltage level of the V_{IN} rail to increase. If the voltage level of the rail is boosted to a level that exceeds the maximum voltage rating of the MOSFETs or the input capacitors, damage may occur to these parts. If the bias voltage for the ISL6522 comes from the V_{IN} rail, then the

maximum voltage rating of the ISL6522 may be exceeded and the IC will experience a catastrophic failure and the converter will no longer be operational. Ensuring that there is a path for the current to follow other than the capacitance on the rail will prevent these failure modes.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

Figure 5 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 6 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the ISL6522 within three inches of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the ISL6522 must be sized to handle up to 1A peak current.

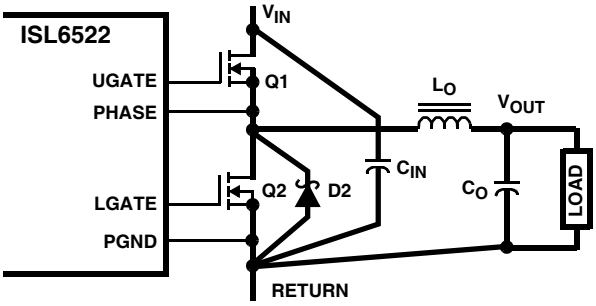


FIGURE 5. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 6 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor, C_{SS} close to the SS pin because the internal current source is only 10µA. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

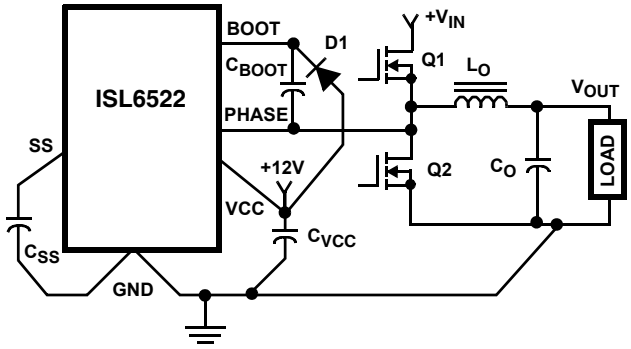


FIGURE 6. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Feedback Compensation

Figure 7 highlights the voltage-mode control loop for a synchronous rectified buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level. The error amplifier (error amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

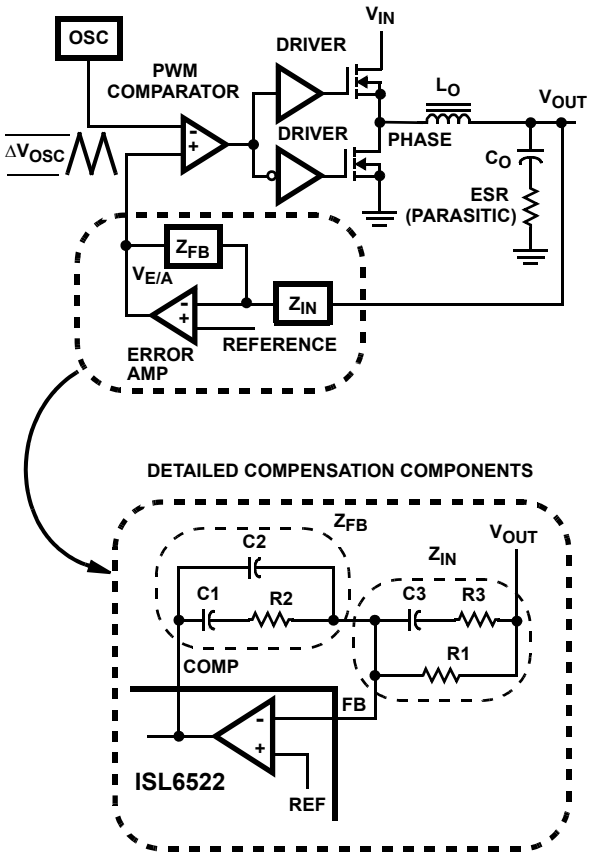


FIGURE 7. VOLTAGE - MODE BUCK CONVERTER COMPENSATION DESIGN

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \qquad F_{ESR} = \frac{1}{2\pi \bullet (ESR \bullet C_O)}$$

The compensation network consists of the error amplifier (internal to the ISL6522) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 8. Use these guidelines for locating the poles and zeros of the compensation network:

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \qquad F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \qquad F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3}$$

1. Pick Gain (R2/R1) for desired converter bandwidth
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC})
3. Place 2ND Zero at Filter's Double Pole
4. Place 1ST Pole at the ESR Zero
5. Place 2ND Pole at Half the Switching Frequency
6. Check Gain against Error Amplifier's Open-Loop Gain
7. Estimate Phase Margin - Repeat if Necessary

Figure 8 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual modulator gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 8. Using the above guidelines should give a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The closed loop gain is constructed on the log-log graph of Figure 8 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

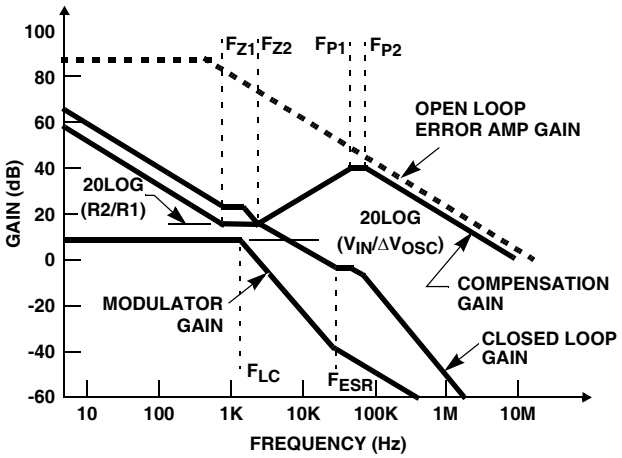


FIGURE 8. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by

the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium-Pro be composed of at least forty (40) 1.0µF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6522 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through-hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The ISL6522 requires two N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower

switch realizes most of the switching losses when the converter is sinking current (see the equations below).

Losses while Sourcing Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Losses while Sinking Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

Where: D is the duty cycle = V_{OUT} / V_{IN},
t_{SW} is the switching interval, and
F_S is the switching frequency.

These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6522 and do not heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Standard-gate MOSFETs are normally recommended for use with the ISL6522. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFETs absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 9 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT} develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle to a voltage of V_{CC} less the boot diode drop (V_D) when the lower MOSFET, Q2 turns on. A logic-level MOSFET can only be used for Q1 if the MOSFETs absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}. For Q2, a logic-level MOSFET can be used if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to PVCC.

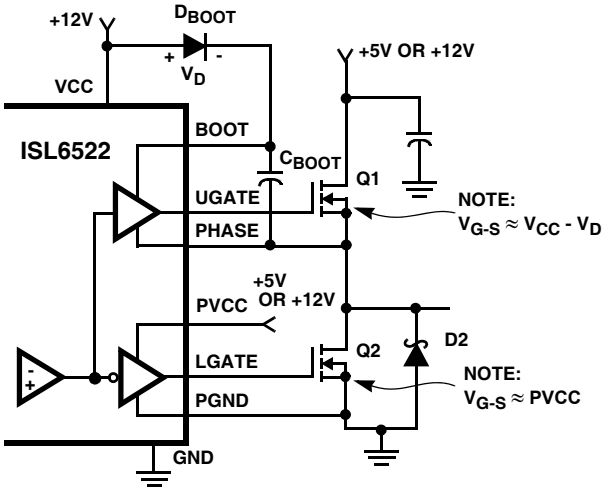


FIGURE 9. UPPER GATE DRIVE - BOOTSTRAP OPTION

Figure 10 shows the upper gate drive supplied by a direct connection to V_{CC}. This option should only be used in converter systems where the main input voltage is $+5V_{DC}$ or less. The peak upper gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and $+12V_{DC}$ for the bias, the gate-to-source voltage of Q1 is 7V. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to PV_{CC}.

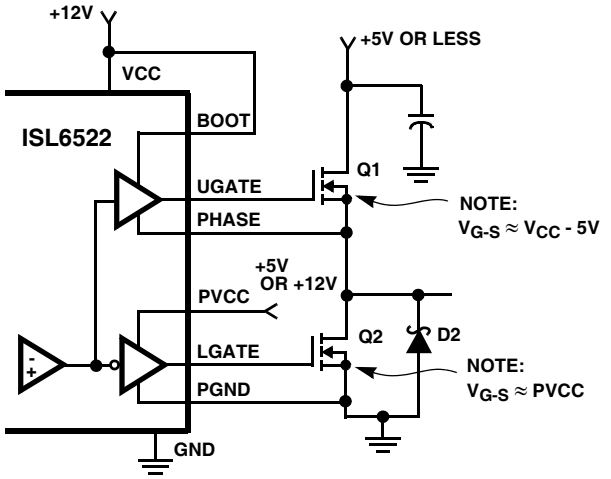


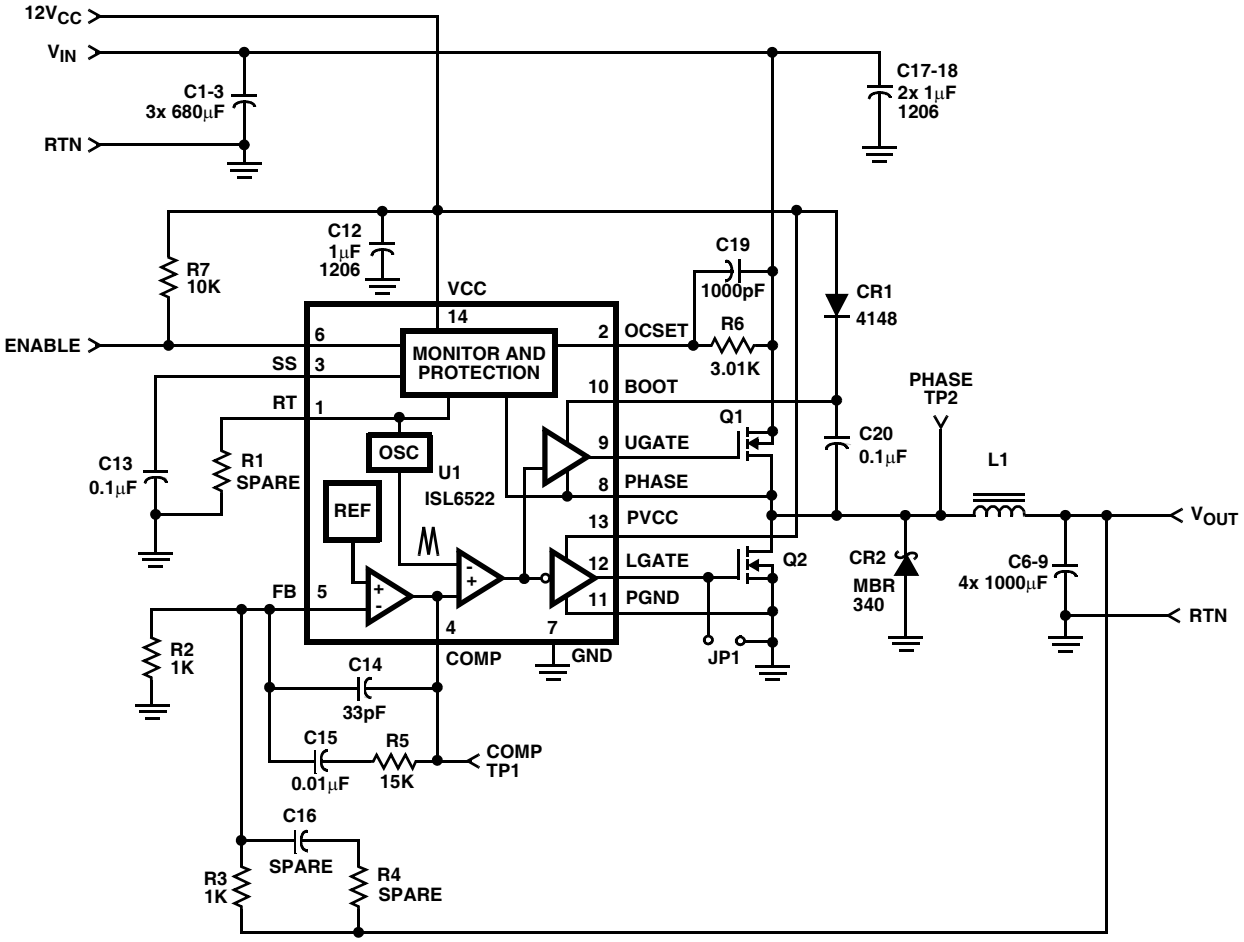
FIGURE 10. UPPER GATE DRIVE - DIRECT V_{CC} DRIVE OPTION

Schottky Selection

Rectifier D2 is a clamp that catches the negative inductor swing during the dead time between turning off the lower MOSFET and turning on the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency will drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

ISL6522 DC-DC Converter Application Circuit

Figure 11 shows a DC-DC converter circuit for a microprocessor application, originally designed to employ the HIP6006 controller. Given the similarities between the HIP6006 and ISL6522 controllers, the circuit can be implemented using the ISL6522 controller without any modifications. Detailed information on the circuit, including a complete bill of materials and circuit board description, can be found in Application Note AN9722. See Intersil's home page on the web: http://www.intersil.com.



Component Selection Notes:

C1-C3 - Three each 680µF 25W VDC, Sanyo MV-GX or equivalent.

C6-C9 - Four each 1000µF 6.3W VDC, Sanyo MV-GX or equivalent.

L1 - Core: micrometals T50-52B; winding: ten turns of 17AWG.

CR1 - 1N4148 or equivalent.

CR2 - 3A, 40V Schottky, Motorola MBR340 or equivalent.

Q1, Q2 - Fairchild MOSFET; RFP25N05

FIGURE 11. DC-DC CONVERTER APPLICATION CIRCUIT

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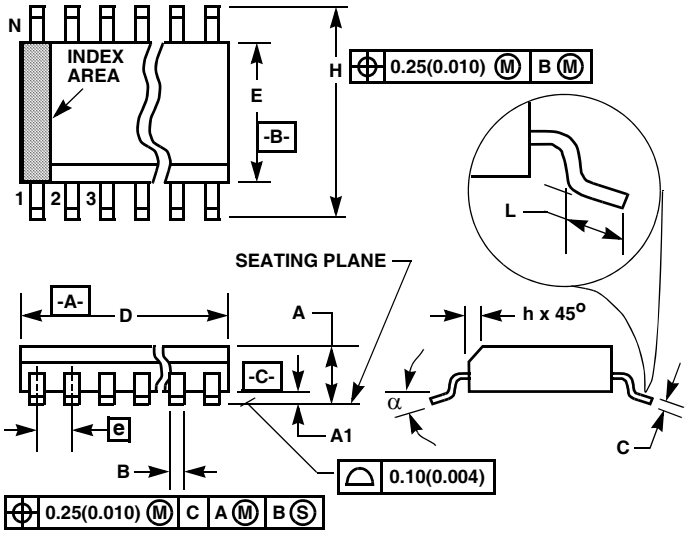
Small Outline Plastic Packages (SOIC)



NOTES:

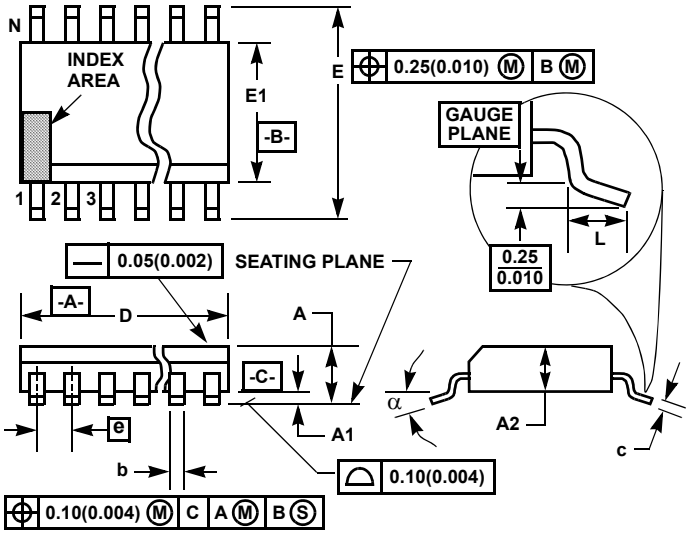
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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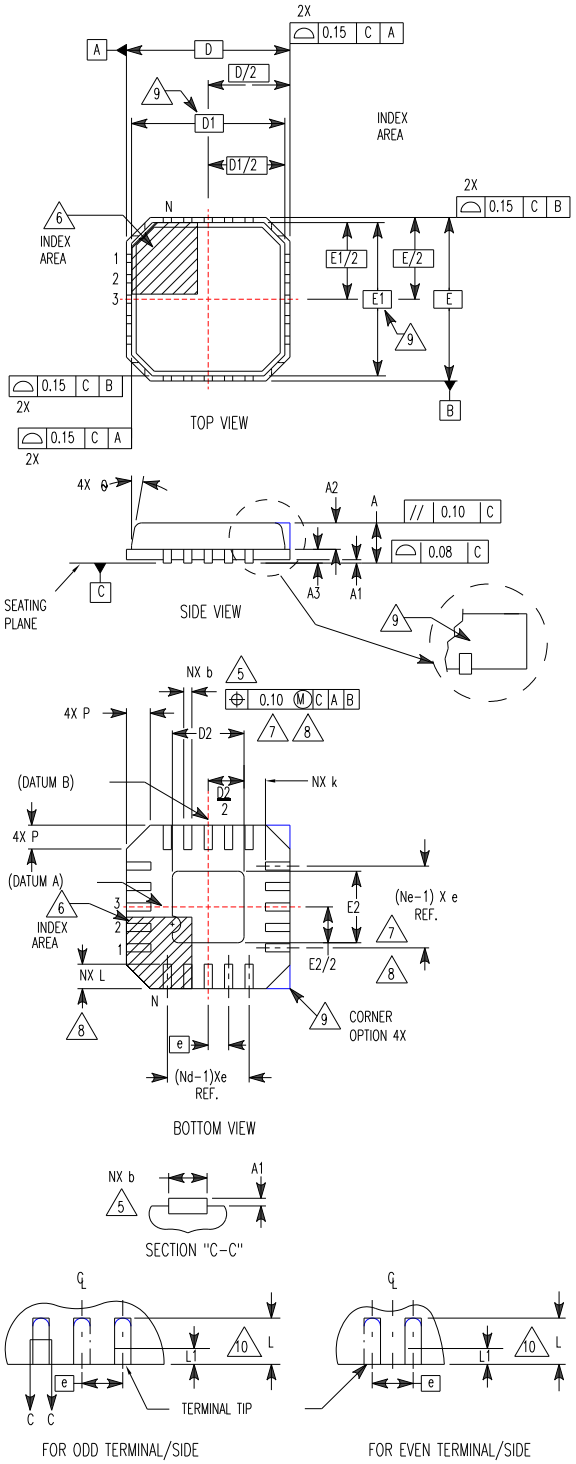
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.5x5B

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHB ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.40	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.