78Q8430 10/100 Ethernet MAC and PHY

Simplifying System Integration™

DATA SHEET

March 2009

DESCRIPTION

The Teridian 78Q8430 is a 10/100 Fast Ethernet controller supporting multi-media offload. The device is optimized for host processor offloading and throughput enhancements for demanding multi-media applications found in Set Top Box, IP Video and Broadband Media Appliance applications. The 78Q8430 seamlessly interfaces to non-PCI processors through a simplified pseudo SRAM-like Host Bus Interface supporting 32/16/8 bit data bus widths. Supported features include IEEE802.3x flow control and full IEEE802.3 and 802.3u standards compliance.

Supporting 10Base-T and 100Base-TX, the transceiver provides Auto MDI-X cable cross-over correction, AUTO Negotiation, Link Configuration and full/half duplex support with full duplex flow control. The line interface requires only a dual 1:1 isolation transformer. Numerous packet processing and IP address resolution control functions are incorporated, including an extensive set of Error Monitoring, Reporting and Troubleshooting features. The 78Q8430 provides optimal 10/100 Ethernet connectivity in demanding video streaming and mixed-media applications.

BENEFITS

- Support for IEEE-802.3, IEEE-802.3u and IEEE-802.3-2000 Annex 31.B
- Low host CPU utilization/overhead with minimal software driver overhead and small driver memory space requirements
- Improved packet processing, low latency and low host CPU utilization
- Highest performance streaming Video over IP
- Optimized performance in mixed media application such as video, data and voice
- Ease of use, faster development cycles, high throughput
- Optimized power conservation with automatic turn on when needed
- Reduced host CPU utilization and overhead
- Improved packet processing
- Optimized performance in mixed media applications

FEATURES

- Single chip 10Base-T/100Base-TX IEEE-802.3 compliant MAC and PHY
  - Adaptive 32 kB SRAM FIFO memory allocation between Tx and Rx paths
  - Queue independent user settable water marks
  - Per queue status indication
- Address Resolution Controller (ARC)
  - Multiple perfect address filtering: 8 default (max 12)
  - Wildcard address filtering, individual, multicast and broadcast address recognition and filtering
  - Positive/negative filtering and promiscuous mode
- 64 kB JUMBO packet support
- QoS: 4 Transmit priority levels
- Non-PCI pseudo-SRAM Host Bus Interface
  - 8-bit, 16-bit and 32-bit bus width
  - Big/little endian support for 16-bit/32-bit bus widths
  - Asynchronous (100 MHz) and synchronous (50 MHz) bus clock support
- Low power and flexible power supply management
  - Power down/save
  - Wake on LAN (Magic Packet™, OnNow packet)
  - Link status change
- Traffic Offload Engine Functionality
  - Transfer frame: APF & ICMP Echo
  - IP Firewall configuration: drop frames on source IP address
  - IP Checksum
- Available in an industrial temperature range (-40 °C to +85 °C)
- RoHS compliant (6/6) lead-free package

APPLICATIONS

- Satellite, cable and IPTV Set Top Boxes
- Multi Media Residential Gateways
- High Definition 1080p/1080i DTVs
- IP-PVR and video distribution systems
- Digital Video Recorders/Players
- Routers and IADs
- Video over IP system, IP-PBX
- IP Security Cameras / PVRs
- Low latency industrial automation

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1 Introduction

The Teridian 78Q8430 is a single chip 10Base-T/100Base-TX capable Fast Ethernet Media Access Controller (MAC) and Physical Layer (PHY) transceiver. The device is optimized for video applications, such as the Set Top Box (STB), and easily interfaces to available STB core processors, such as the STi5100, STi5516, STi5514, ARM™ and Intel® based processors. The 78Q8430 is compliant with applicable IEEE-802.3 standards. MAC and PHY configuration and status registers are provided as specified by IEEE-802.3u.

The 78Q8430 operates over Category-5 Unshielded Twisted Pair (Cat-5 UTP) cabling in 100Base-TX applications and over Cat-3 UTP in 10Base-T applications requiring only a dual 1:1 isolation transformer interface to the copper media.

The Ethernet MAC section makes use of a 32 kB deep on-chip SRAM FIFO packet memory to adaptively buffer transmit and receive data. SRAM memory can be dynamically allocated to either the transmit queues or the receive queues as required to optimize throughput.

The host processor accesses the FIFO(s) using a simple asynchronous pseudo-SRAM like host bus interface. A 32 bit wide bus is provided; the bus width can be pin-configured for 8-bit, 16-bit or 32-bit bus width at boot-up. Big endian, little endian and mixed endian options are available in 32-bit operation; little endian is available for 16-bit operation. Different End-in variations are supported through internal circuitry with minimal user intervention required.

The MAC interface logic may assert MEMWAIT during bus transactions, requesting wait states from the host while critical internal data transfer completes. The MAC provides both half duplex and full duplex operation, as well as support for full duplex flow control. Complete, portable device drivers for Linux®, OS20 and VxWorks® are available.

The 78Q8430 operates from a single 3.3 V supply. Power down modes and power saving modes are available. The 78Q8430 defaults to use an on-chip crystal oscillator. In this mode, a 25 MHz reference crystal is connected between the XTLP and XTLN pins. Alternatively, an externally generated 25 MHz clock can be connected to the XTLP pin. The chip will automatically configure itself to use the external clock. In this mode of operation, a crystal is not required.

1.1 Systems Applications

Figure **1** presents an overview of the 78Q8430 in a block diagram.

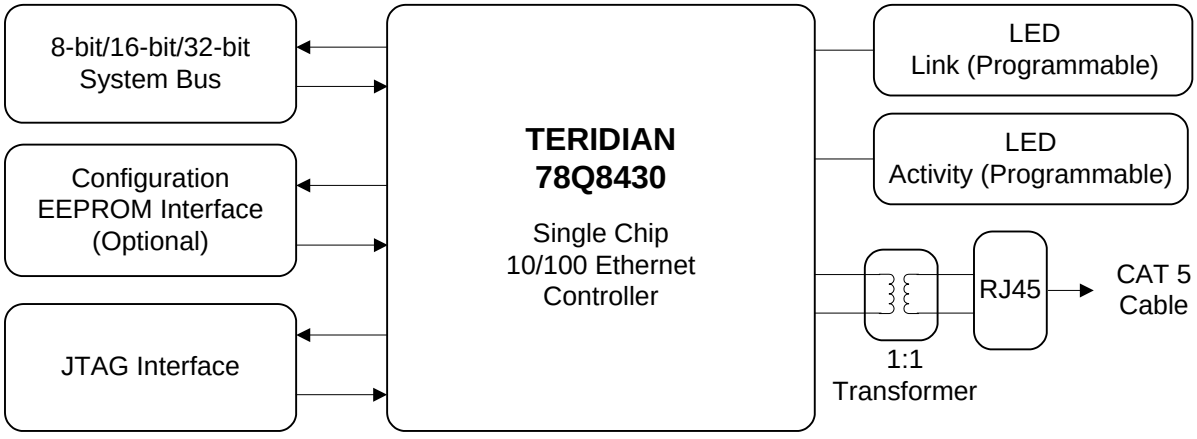


Figure 1: 78Q8430 Block Diagram

1.2 System Level Application Information

This section provides an overview of system level applications in some typical high-volume consumer equipment.

1.2.1 Set Top Box Application

Figure 2 shows a typical application diagram for a set top box.

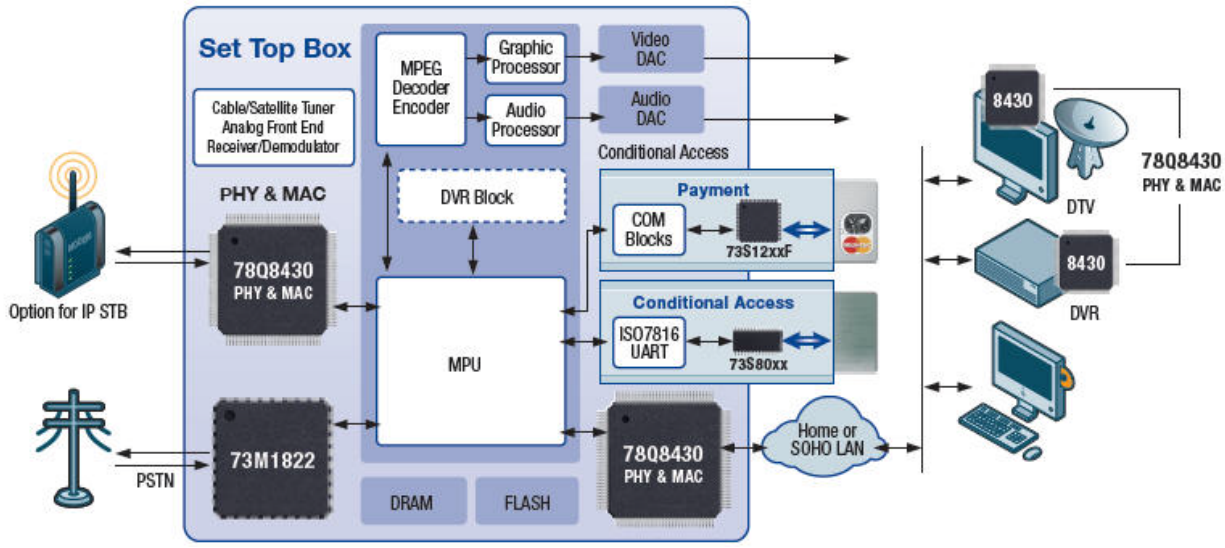


Figure 2: Set Top Box Diagram

1.2.2 IP Security Application

Figure 3 shows a typical application diagram for an IPTV security camera application.

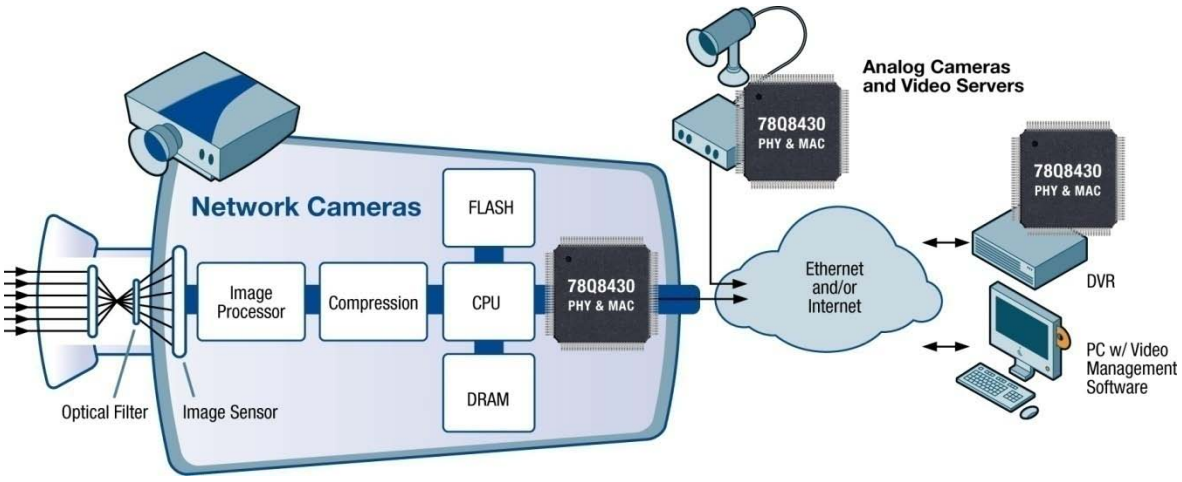


Figure 3: Network Cameras Diagram

1.2.3 IP PBX Application

Figure 4 shows a typical application diagram for an IP PBX application.

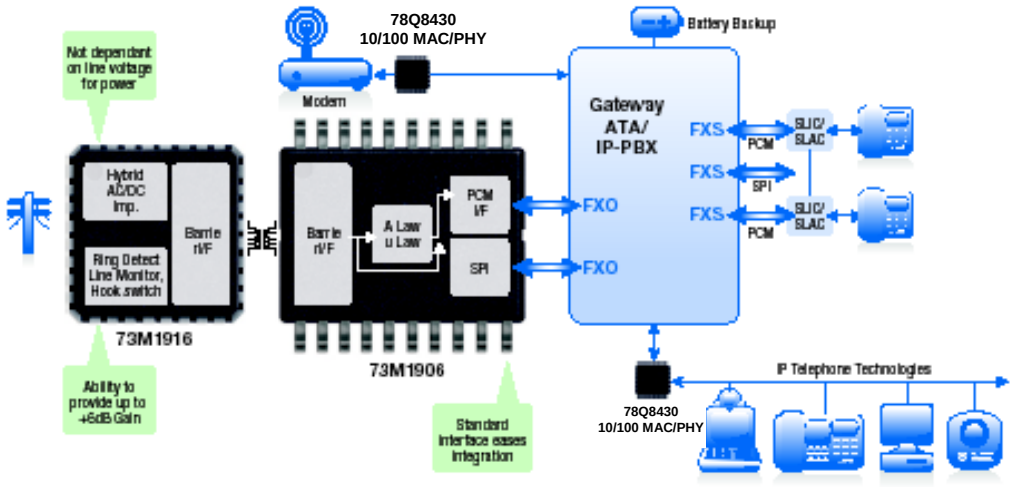


Figure 4: Typical FXO VoIP Application

1.3 Overview

The 78Q8430 is divided into four sections, as shown in Figure 5.

- Generic Bus Interface (GBI) Control Layer
- Queue Memory Layer
- Ethernet Media Access Control (MAC) Layer
- Ethernet Physical (PHY) Layer

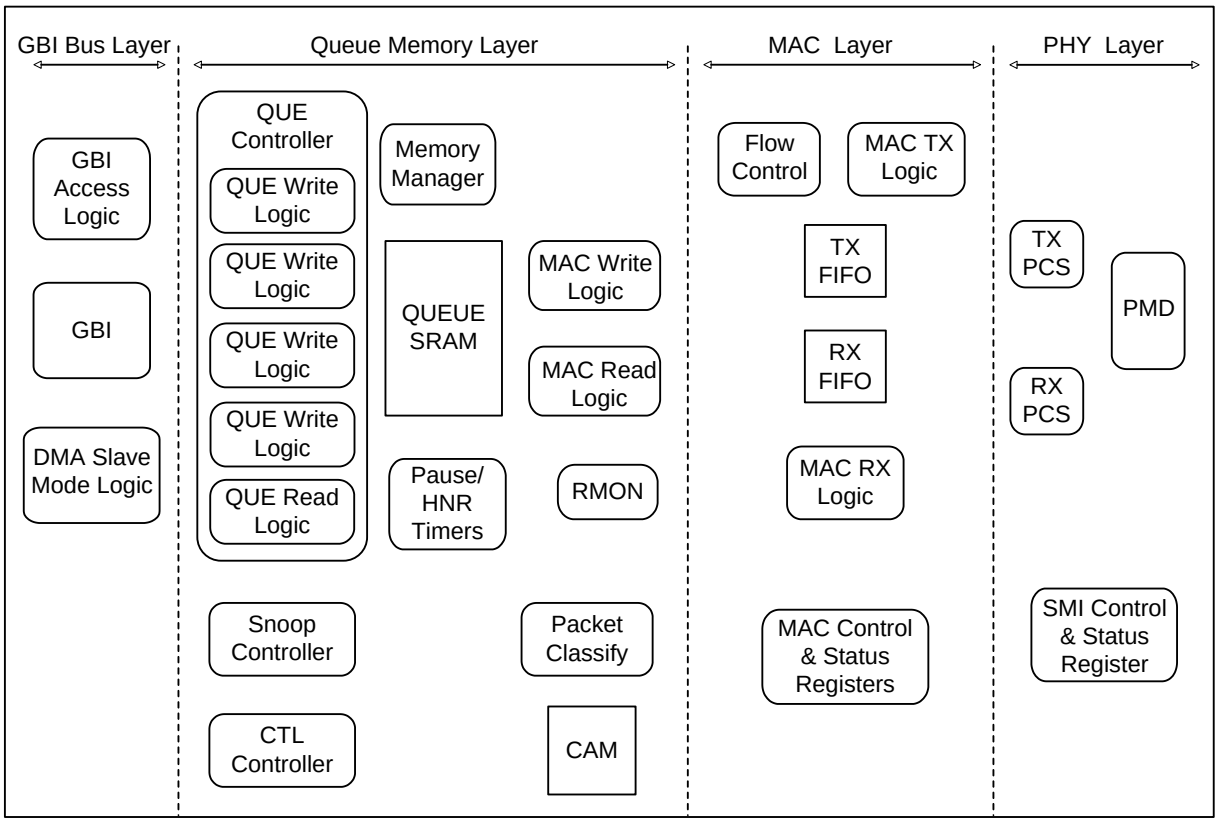


Figure 5: Device Block Diagram

1.4 Application Environments

This section provides an overview of the application environments such as the STMicroelectronics and Embest ARM9™ processors, for which the 78Q8430 provides a seamless interface. Figure 6 shows a simple application diagram for a design using the GBI based 10/100-Mbps Ethernet Controller. By providing a direct connection to the GBI bus, applications requiring Ethernet network access can be realized with a high degree of integration. The figure shows the processor and the Ethernet controller with connected address and data buses. This connection can be either on the motherboard, or via an expansion module. The GBI Controller controls the address and data and the system control signals.

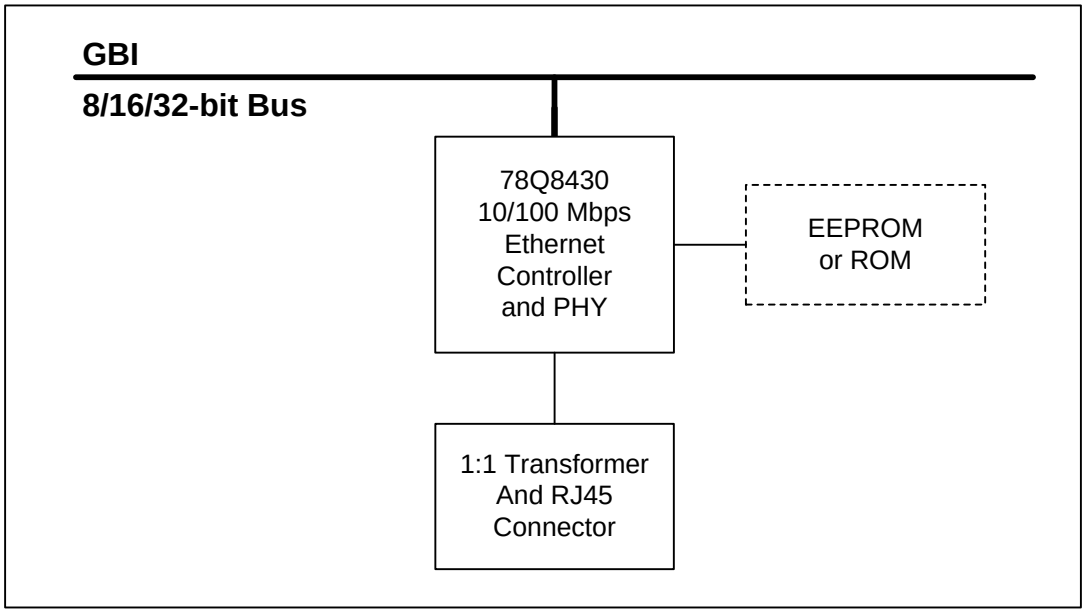


Figure 6: GBI Bus Block Diagram

Figure 6 shows the components that are likely to be used with the 10/100-Mbps Ethernet Controller. The integrated PHY is designed to directly connect to an integrated 1:1 transformer and RJ-45 connector, thereby providing a minimum parts solution.

1.5 Supply Voltages

The 78Q8430 requires a single 3.3 V (+/-5%) supply voltage. No external components are required to generate on-chip bias voltages and currents. High accuracy is maintained through a closed-loop trimmed biasing network. On-chip power converters generate 1.8 V power for core digital logic and memory blocks. The voltage regulator is not affected by the power-down mode.

1.6 Power Management

The 78Q8430 supports both normal and power-saving modes. When the GBI bus is active, it can be in normal mode or Power Management low-power modes.

2 Pinout

The 78Q8430 is available in a 14x14 mm 100-pin LQFP package.

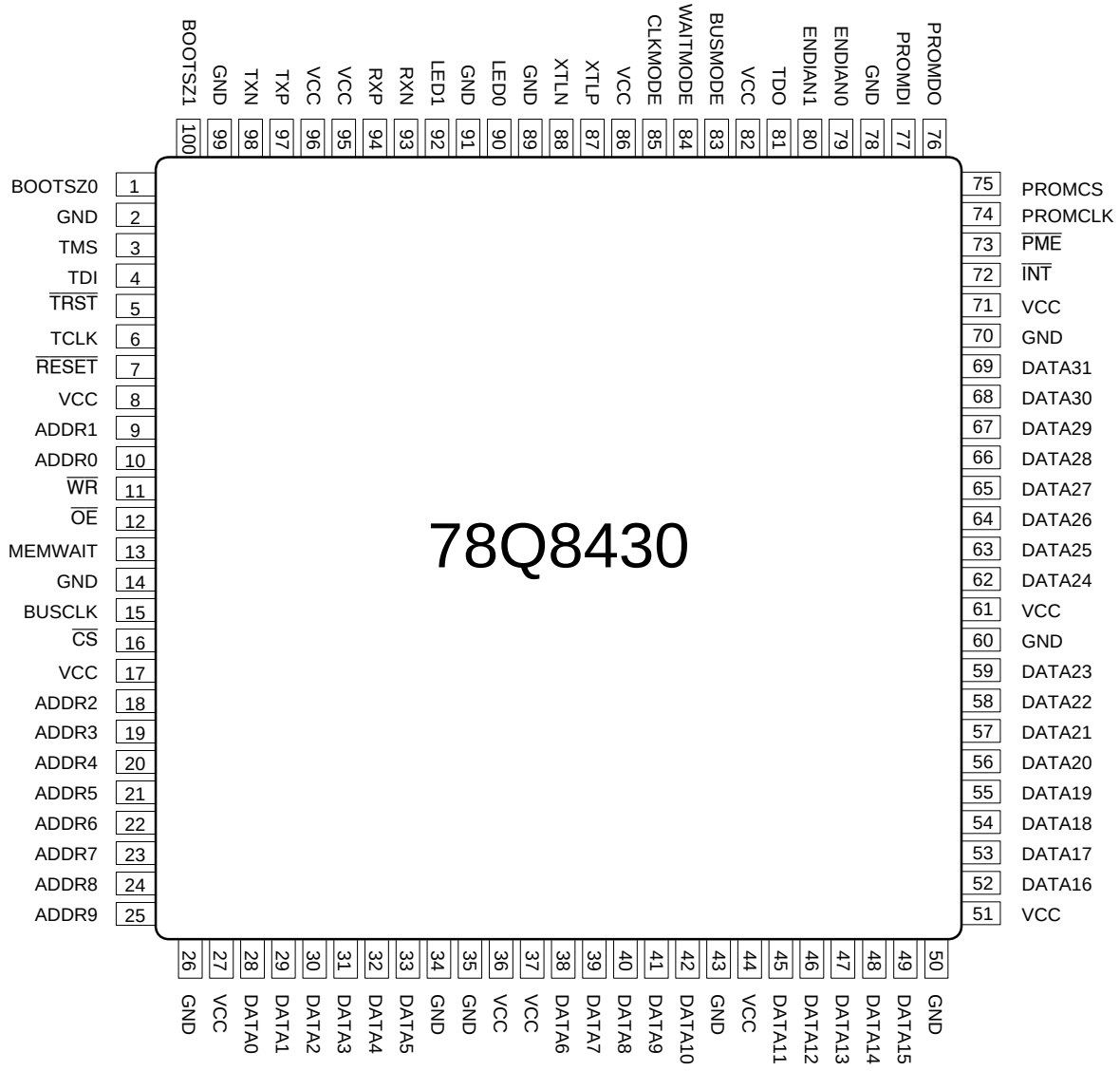


Figure 7: Pinout

3 Pin Description

3.1 Pin Legend

Table 1 lists the different pin types found on the 78Q8430 device. The Type field of the pin description tables refers to one of these types.

Table 1: Pin Legend

Type	Description
A	Analog
IU	TTL-level Input, with Pull-up
IS	TTL-level Input, with Schmitt Trigger
O	TTL-level Output
OD	TTL-level Output (Open Drain)
S	Supply
I	TTL-level Input
ID	TTL-level Input, with Pull-down
B	TTL-level Bidirectional Pin
OZ	TTL-level Output (Tristate)
G	Ground

3.2 Pin Descriptions

The pin descriptions in the following tables are grouped by interface. A pin number, type specification per Table 2 and a functional description is provided for each pin on the 78Q8430 device.

3.2.1 Clock Pins

Table 2: Clock Pin Descriptions

Signal	Pin Number	Type	Description
XTLP	87	A	**Crystal Positive/Negative** To use the internal oscillator, connect a 25 MHz crystal across XTLP and XTLN. To use of an external clock, XTLN is grounded and XTLP is driven with a 25 MHz clock. Provides timing reference for all media dependant interface operations. An internal PLL is used to multiply this clock by four for use as the main system clock in internal clock mode.
XTLN	88		
BUSCLK	15	I	**Peripheral Clock** The source for the main system clock in external clock mode. In synchronous bus mode, all host bus signals are assumed to be synchronous to this clock.

3.2.2 Media Dependent Interface (MDI) Pins

Table 3: MDI Pin Descriptions

Signal	Pin Number	Type	Description
TXP	97	A	**Transmit Output Positive/Negative** Transmitter outputs for both 10BASE-T and 100BASE-TX. MDI-X Mode: Receive Input Positive/Negative Receiver inputs for both 10BASE-T and 100BASE-TX.
TXN	98	A	
RXP	94	A	**Receive Input Positive/Negative** Receiver inputs for both 10BASE-T and 100BASE-TX. MDI-X Mode: Transmit Output Positive/Negative Transmitter outputs for both 10BASE-T and 100BASE- TX.
RXN	93	A	

3.2.3 LED Display (PHY) Pins

The LED pins use standard logic drivers. They output a logic low when the LED is meant to be on and are tri-state when it is meant to be off. The LED cathode should be connected to the output pin and a series resistor from the power supply connected to the LED anode.

Table 4: LED Pin Descriptions

Signal	Pin Number	Type	Description
LED0	90	OZ	**PHY display LED0 (Link OK)** The default for LED0 is Link OK (LED is on for link established).
LED1	92	OZ	**PHY display LED1 (Activity)** The default for LED1 is Link Activity (LED blinks for Rx or Tx data transferred).

3.2.4 EEPROM Pins

Table 5: **EEPROM Interface Pin Descriptions**

Signal	Pin Number	Type	Description
PROM_CS	75	O	**EEPROM Chip Select** Used to frame transmissions to and from an external EEPROM.
PROM_CLK	74	O	**EEPROM Clock** Clock for transmitting to and from an external EEPROM/ROM. This is compatible with the slowest commercial parts, which specify a maximum frequency of 1 MHz.
PROM_DI	77	I	**EEPROM Data In** Data line for transmitting from the external EEPROM to the controller. Must be high with no EEPROM present.
PROM_DO	76	OZ	**EEPROM Data Out** Transfers data from the controller to an external EEPROM/ROM.

3.2.5 GBI Data Pins

Table 6: GBI Data Pin Descriptions

Signal	Pin Number	Type	Description
DATA31	69	B	**Data Bus DATA[31:0]** Bi-directional host bus data. The BOOTSZ pins determine how many of these are actually used. The $\overline{OE}$ input will disable the output drivers to prevent bus collisions.
DATA30	68		
DATA29	67		
DATA28	66		
DATA27	65		
DATA26	64		
DATA25	63		
DATA24	62		
DATA23	59		
DATA22	58		
DATA21	57		
DATA20	56		
DATA19	55		
DATA18	54		
DATA17	53		
DATA16	52		
DATA15	49		
DATA14	48		
DATA13	47		
DATA12	46		
DATA11	45		
DATA10	42		
DATA9	41		
DATA8	40		
DATA7	39		
DATA6	38		
DATA5	33		
DATA4	32		
DATA3	31		
DATA2	30		
DATA1	29		
DATA0	28		

3.2.6 GBI Address Pins

Table 7: GBI Address Pin Descriptions

Signal	Pin Number	Type	Description
ADDR9	25	I	**Address Bus** The address lines are required to be stable for the entire duration of a $\overline{CS}$ cycle. In synchronous bus mode, the address pins are sampled on the first rising edge of BUSCLK that $\overline{CS}$ is asserted low. In asynchronous bus mode, the address pins are sampled as soon as the falling edge of $\overline{CS}$ is synchronized to the internal system clock. In 32-bit bus mode, ADDR[1:0] are ignored. In 16-bit bus mode, ADDR[0] is ignored. In 8-bit bus mode, all ADDR bits are used to reference a register byte.
ADDR8	24	I	
ADDR7	23	I	
ADDR6	22	I	
ADDR5	21	I	
ADDR4	20	I	
ADDR3	19	I	
ADDR2	18	I	
ADDR1	9	I	
ADDR0	10	I	

3.2.7 GBI Control Pins

Table 8: GBI Control Pin Descriptions

Signal	Pin Number	Type	Description
$\overline{RESET}$	7	I	**Reset (active low)** Referred to as hardware reset. Causes all 78Q8430 outputs to enter a high-impedance state, stops all current operations and initializes registers.
$\overline{CS}$	16	I	**Chip Select (active low)** The Processor asserts this signal to initiate a read or write operation.
$\overline{WR}$	11	I	**Write Enable (active low)** The Processor asserts $\overline{WR}$ to indicate a write operation.
OE	12	I	**Output Enable (active low)** The Processor asserts $\overline{OE}$ to enable the 78Q8430 data drivers during a read cycle.
MEMWAIT	13	OZ	**Memory Wait** During a bus cycle the 78Q8430 asserts MEMWAIT to indicate that it is not ready to drive or receive valid data on the DATA lines. The polarity is dependent on the WAITMODE pin. When WAITMODE is high then the pin is asserted high; when WAITMODE is low then the pin is asserted low.
$\overline{INT}$	72	OD	**Interrupt (active low)** The 78Q8430 asserts the $\overline{INT}$ signal low when it detects an interrupt event.
$\overline{PME}$	73	OD	**Power Management Event (active low)** The 78Q8430 asserts the $\overline{PME}$ signal low when it detects a wake-up event.

3.2.8 Mode Pins

Table 9: Chip Mode Pin Descriptions

Signal	Pin Number	Type	Description
BUSMODE	83	I	**BUSMODE, CLKMODE, WAITMODE Configuration** 0,0,0 = Sync bus, ext. system clock, memwait act low 0,0,1 = Sync bus, ext. system clock, memwait act high 0,1,0 = Reserved 0,1,1 = Reserved 1,0,0 = Async bus, ext. system clock, memwait act low 1,0,1 = Async bus, ext. system clock, memwait act high 1,1,0 = Async bus, int. system clock, memwait act low 1,1,1 = Async bus, int. system clock, memwait act high
CLKMODE	85	I	
WAITMODE	84	I	
ENDIAN0	79	I	**Data Bus Endian Select** 0,0 = Big endian (MSB at high bit positions) 0,1 = Bytes are little endian inside 16-bit words 1,0 = Word endian (MSW at low bit positions) 1,1 = Little endian (MSB at low bit positions)
ENDIAN1	80	I	
BOOTSZ1	100	I	**GBI Bus Size** BOOTSZ[1:0]: is strapped to indicate the GBI bus size: 00 = Bus is 32 bits wide 01 = Bus is 16 bits wide. Only DATA[15:0] are used. 10 = Bus is 8 bits wide. Only DATA[7:0] are used. 11 = Reserved
BOOTSZ0	1	I	

Notes:

1. The internal PHY should never be powered down when the internal system clock is selected by the CLKMODE pin (CLKMODE=1)
2. There is no external visibility for the system clock when the internal clock mode is selected. The GBI interface must therefore always be used in asynchronous bus mode.

3.2.9 JTAG Pins

Table 10: JTAG Pin Descriptions

Signal	Pin Number	Type	Description
$\overline{\text{TRST}}$	5	I	**Test Reset (active low)** System provided reset for JTAG logic.
TCLK	6	I	**Test Clock** System provided clock for JTAG logic.
TMS	3	IU	**Test Mode Select** Enables JTAG boundary scan using serial in/serial out ports. Sampled on rising edge of TCLK.
TDI	4	IU	**Test Data In** Serial input port for clocking in test data to be shifted to the output at the end of the boundary scan chain (TDO).
TDO	81	O	**Test Data Out** Serial output port for clocking out test data shifted from the input at the beginning of the boundary scan chain (TDI).

3.2.10 Power Pins

Table 11: Power Pin Descriptions

Signal	Pin Number	Type	Description
VCCA	86 95 96	S	3.3 V supply for the analog transmit section.
VCC	8 17 27 36-37 44 51 61 71 82	S	3.3 V supply for the digital logic section.
GND	2 14 26 34-35 43 50 60 70 78 89 91 99	G	Common ground return.

4 Electrical Specification

4.1 Absolute Maximum Ratings

Operation above the maximum rating may permanently damage the device.

Table 12: Absolute Maximum Ratings

Parameter	Rating
DC Supply Voltage (V_{CC})	-0.5 to 4.0 VDC
Storage Temperature	-65 to 150 °C
Pin Voltage (except TXOP/N and RXIP/N)	-0.3 to (V_{CC}+0.6) VDC
Pin Voltage (TXOP/N and RXIP/N only)	-0.3 to (V_{CC}+1.4) VDC
Pin Current	± 120 mA

4.2 Recommended Operation Conditions

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges.

Table 13: Recommended Operating Conditions

Parameter	Rating
DC Voltage Supply (V_{CC})	3.3 ± 0.17 VDC
Ambient Operating Temperature (T_{AMB})	-40 to +85 °C

4.3 DC Characteristics

Table 14: DC Characteristics

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Supply Current	I_{CC}	V_{CC} = 3.3 V Auto-Negotiation 10BT (Idle) 10BT (Normal Activity) 100BTX	–	– 124 110 230 165	– 150 140 250 190	– mA
Supply Current	I_{CC}	Power-down mode	–	14	45	mA

4.4 Digital I/O Characteristics

Table 15: Digital I/O Characteristics

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Input Voltage Low	V_{IL}		–	–	0.8	V
Input Voltage High	V_{IH}		2.0	–	–	V
Input Current	I_{IL}, I_{IH}		-1	–	1	µA
Input Capacitance	C_{IN}		–	8	–	pF
Output Voltage Low	V_{OL}	I_{OL} = 8 mA	–	–	0.4	V
Output Voltage High**	V_{OH}	I_{OH} = -8 mA	2.4	–	–	V
Output Transition Time	T_T	C_L = 20 pF I_{OH} = -8 ma (H to Z)	–	–	6	ns
Tri-state Output Leakage Current*	I_Z	Type tri-state only	-1	–	1	µA

**PMEB and INTB are active low outputs requiring external pull-up resistors. V_{OH} for these outputs is not specified.

4.5 Analog Electrical Characteristics

4.5.1 100Base-TX Transmitter

Table 16: MII 100Base-TX Transmit Timing

Parameter	Conditions	Min	Nom	Max	Unit
Peak Output Amplitude ($\|V_P+\|$, $\|V_P-\|$) (see note below)	Best-fit over 14 bit times; 0.4 dB Transformer loss	950	–	1050	mVpk
Output Amplitude Symmetry	$\|V_P +\|$ $\|V_P -\|$	0.98	–	1.02	
Output Overshoot	Percent of V_P+, V_P-	–	–	5	%
Rise/Fall time (t_R, t_F)	10-90% of V_P+, V_P-	3	–	5	ns
Rise/Fall time Imbalance	$\|t_R - t_F\|$	–	–	500	ps
Duty Cycle Distortion	Deviation from best-fit time-grid; 010101... Sequence	–	–	±250	ps
Jitter	Scrambled Idle, Internal Oscillator Mode	–	–	1.4	ns

Note: Measured at the line side of the transformer. Test Condition: Transformer P/N: TLA-6T103. Line Termination: 100 Ω±1%

4.5.2 100Base-TX Transmitter (Informative)

Table 17: MII 100Base-TX Transmitter (Informative)

Parameter	Conditions	Min	Max	Unit
Return Loss	2 < f < 30 MHz 30 < f < 60 MHz 60 < f < 80 MHz	16 $16 - 20\log\left(\frac{f}{30MHz}\right)$ 10	–	dB
Open-Circuit Inductance	-8 < I_{IN} < 8 mA	350	–	µH

Note: The specifications in the preceding table are included for information only. They are mainly a function of the external transformer and termination resistors used for measurements.

4.5.3 100Base-TX Receiver

Table 18: MII 100Base-TX Receiver Timing

Parameter	Conditions	Min	Nom	Max	Unit
Signal Detect Assertion Threshold		600	700	800	mVppd
Signal Detect De-assertion Threshold		300	350	400	mVppd
Differential Input Resistance		–	20	–	kΩ
Jitter Tolerance (pk-pk)		4	–	–	ns
Baseline Wander Tracking		-75	–	+75	%
Signal Detect Assertion Time	Not tested	–	–	1000	µs
Signal Detect De-assertion Time	Not tested	–	–	4	µs

4.5.4 10Base-T Transmitter

Table 19: MII 10Base-T Transmitter Timing

Parameter	Conditions	Min	Nom	Max	Unit
Peak Differential Output Signal (see note below)	All data patterns	2.2	–	2.8	V
Harmonic Content (dB below fundamental)	Any harmonic All ones data Not tested	27	–	–	dB
Link Pulse Width		–	100	–	ns
Start-of-Idle Pulse Width	Last bit 0 Last bit 1	– –	300 350	– –	ns ns

Note: The Manchester-encoded data pulses, the link pulse and the start-of-idle pulse are tested against the templates and using the procedures found in Clause 14 of IEEE 802.3. Measured at the line side of the transformer. Test Condition: Transformer P/N: TLA-6T103. Line Termination: 100 Ω±1%

4.5.5 10Base-T Transmitter (Informative)

Table 20: MII 10Base-T Transmitter (Informative)

Parameter	Conditions	Min	Nom	Max	Unit
Output Return Loss		15	–	–	dB
Output Impedance Balance	1 MHz < freq < 20 MHz	$29 - 17\log\left(\frac{f}{10}\right)$	–	–	dB
Peak Common-mode Output Voltage		–	–	50	mV
Common-mode Rejection	15 V_{PK}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.	–	–	100	mV
Common-mode Rejection Jitter	15 V_{PK}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.	–	–	1	ns

Note: The specifications in the preceding table are included for information only. They are mainly a function of the external transformer and termination resistors used for measurements

4.5.6 10Base-T Receiver

Table 21: MII 10Base-T Receive Timing

Parameter	Conditions	Min	Nom	Max	Unit
DLL Phase Acquisition Time		–	10	–	BT
Jitter Tolerance (pk-pk)		30	–	–	ns
Input Squelched Threshold		500	600	700	mVppd
Input Unsquelched Threshold		275	350	425	mVppd
Differential Input Resistance		–	20	–	kΩ
Bit Error Ratio		–	10^{-10}	–	
Common-mode Rejection	Square wave 0 < f < 500 kHz Not tested	25	–	–	V

5 Host Interface Timing Specification

5.1 Host Interface

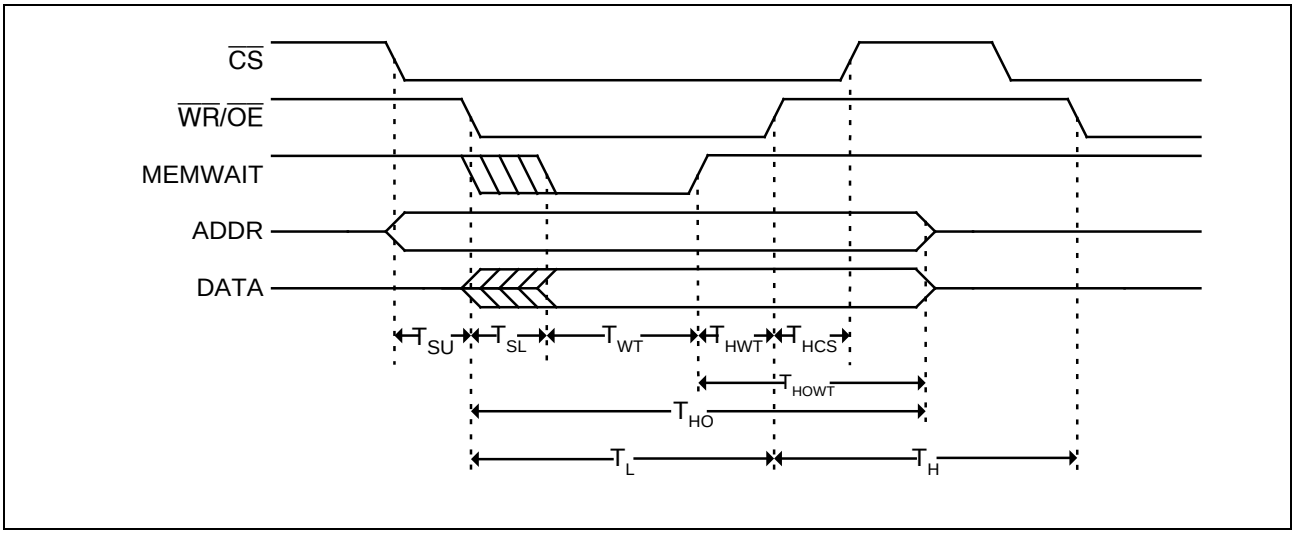


Figure 8: Host Interface Timing Diagram

Name	Description	Requirement	Min	Max
T_{SU}	$\overline{CS}$ and ADDR setup time	$\overline{CS}$ and ADDR must be stable on or before the falling edge of $\overline{WR}/\overline{OE}$.	0 ns	–
T_{SL}	Output settling time	The maximum amount of time that it will take the MEMWAIT, or DATA when there is no MEMWAIT, outputs to become stable after the falling edge of $\overline{WR}/\overline{OE}$.	–	13.7 ns
T_{WT}	Maximum wait time	The maximum amount of time that the MEMWAIT output will held asserted.	–	17 ck
T_{HWT}	Wait hold time	The minimum amount of time that the $\overline{WR}/\overline{OE}$ input must be held past the de-assertion of MEMWAIT.	10 ns	–
T_{HCS}	$\overline{CS}$ hold time	The $\overline{CS}$ input must be stable low for the entire duration of the $\overline{WR}/\overline{OE}$ low cycle.	0 ns	–
T_{HO}	ADDR and DATA hold time	The ADDR and DATA inputs must be stable for no less than this amount of time after the falling edge of $\overline{WR}$.	2.5 ck	–
T_L	$\overline{WR}/\overline{OE}$ min low pulse	The minimum amount of time that the $\overline{WR}/\overline{OE}$ inputs must be held low.	2 ck	–
T_H	$\overline{WR}/\overline{OE}$ min high pulse	The minimum amount of time that the $\overline{WR}/\overline{OE}$ inputs must be held high.	2 ck	–

Note: On read cycles when MEMWAIT is asserted the DATA outputs will be valid before the de-assertion of MEMWAIT.

5.1.1 Synchronous Mode Timing

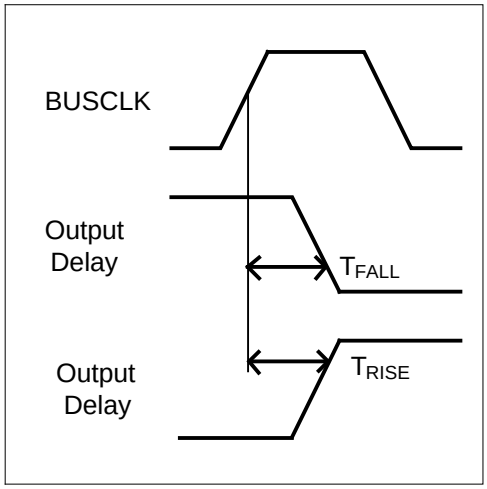


Figure 9: Host Bus Output Timing Diagram

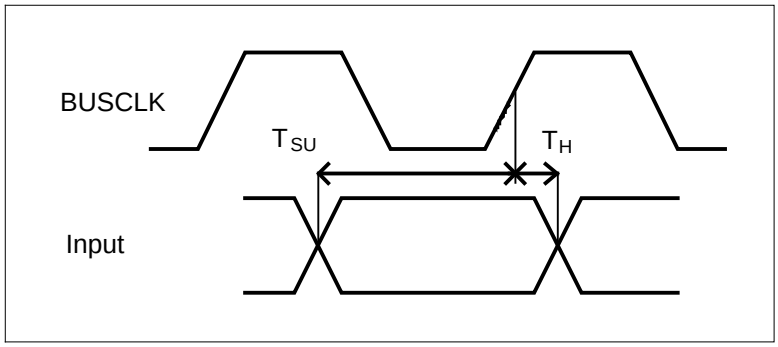


Figure 10: Host Bus Input Timing Diagram

Parameter	Symbol	Min	Nom	Max	Unit
Input Setup Time	T_{SU}	6	–	–	ns
Input Hold Time	T_{H}	6	–	–	ns
Output Fall Delay	T_{FALL}	–	–	8	ns
Output Rise Delay	T_{RISE}	–	–	8	ns
CSB min low	P_{WL}	1	–	–	clk
CSB min high	P_{WH}	2	–	–	clk

5.1.2 Bus Clock Timing

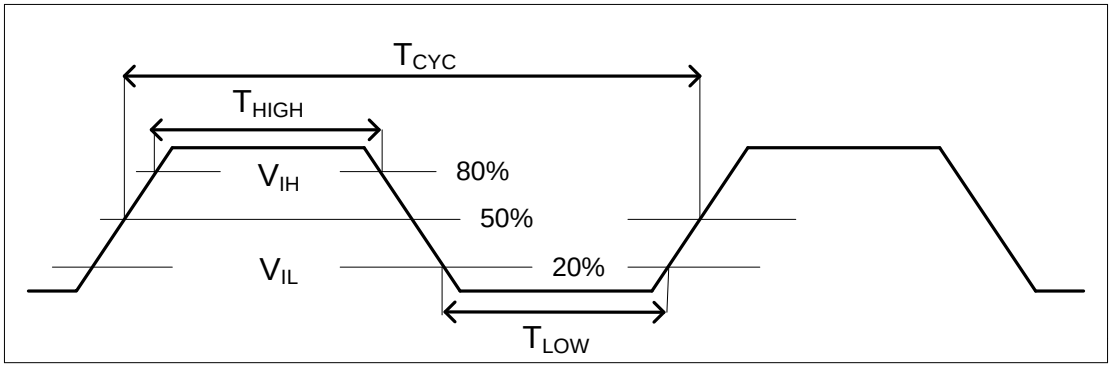


Figure 11: Bus Clock Timing

Parameter	Symbol	Sync 50		Async 100		Units
		Min	Max	Min	Max	
BUSCLK Cycle Time	T_{CYC}	20	–	10	–	ns
BUSCLK Frequency	–	–	50	–	100	MHz
BUSCLK High Time	T_{HIGH}	8	–	3	–	ns
BUSCLK Low Time	T_{LOW}	8	–	3	–	ns
BUSCLK Slew Rate	–	1	3	1	3	V/ns

5.1.3 Reset Timing

Parameter	Symbol	Min	Nom	Max	Units
RESETB Minimum Duration	T_{RESET}	1	–	–	clocks

6 Functional Description

6.1 Internal Block Diagrams

6.1.1 Internal Digital Block

Figure 12 presents an overview of the functional layers of the 78Q8430. On the left side are the signals, which connect to the GBI bus. On the upper and middle right, the blocks that implement the MAC side of the MII are shown. These blocks are connected to the embedded PHY. On the lower right, connections to the EEPROM are shown.

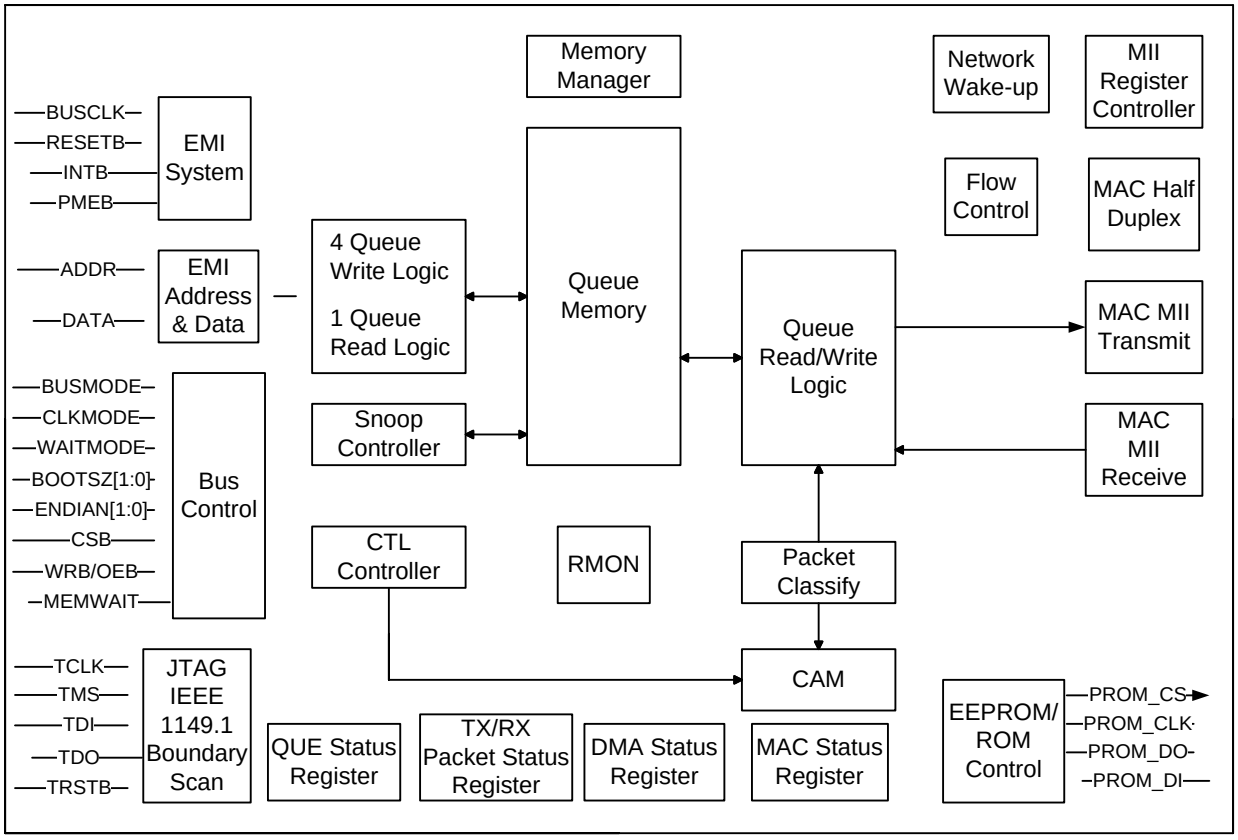


Figure 12: Internal Digital Block Diagram

6.1.2 Internal PHY

Figure 13 shows the functional blocks of the internal 78Q8430 PHY. The signals shown on the left side are the internal MII signals to the MAC. These signals are multiplexed with their respective external pins for use with an external PHY device. The 78Q8430 is not a two-port device. Only one PHY interface can be operational.

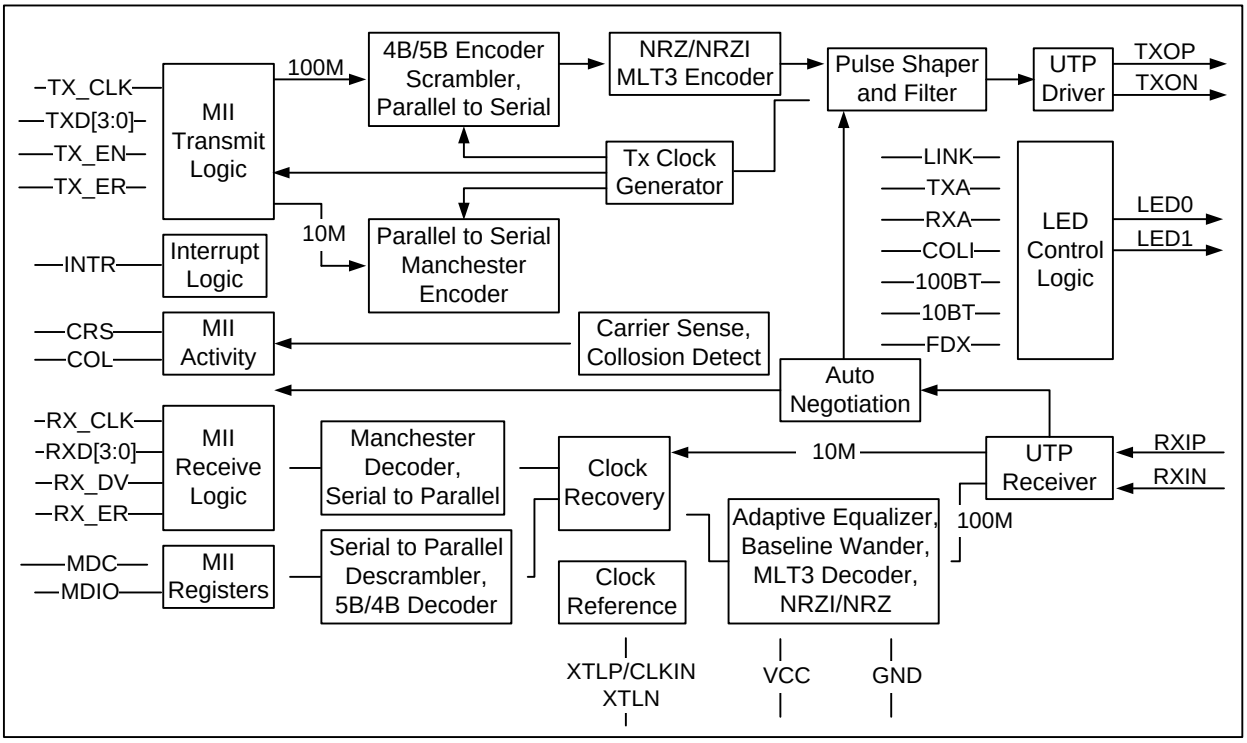


Figure 13: Internal PHY Block Diagram

On the right side are the signals, which connect to the status LEDs and a 1:1 isolation transformer before connecting to an RJ-45 connector, or equivalent media components.

6.2 Data Queuing

Ethernet frame data in the 78Q8430 is managed in queuing structures called QUEs. The host bus address space allocated for QUEs has enough space for eight, while the 78Q8430 circuit only implements five. QUEs are identified numerically, QUE0 through QUE7, based on the registers in the QUE register space that are used to access them. QUE1, QUE6 and QUE7 are unimplemented and reserved for future use.

A QUE allocates main buffer memory as needed and stores discrete frames as they are written into the QUE. The QUE then reads back frames in the same order that they were written and frees the main buffer memory. A QUE can contain a maximum of 125 frames at any one time. If a QUE is unable to allocate main buffer memory when writing a frame, the frame will be partially added to the QUE as a truncated frame. If a QUE is unable to allocate main buffer memory to start a frame, the entire frame is dropped.

The QUEs are divided into two categories: receive QUEs, that store received frame data and transmit QUEs, that store transmit frame data. Frames are written to a receive QUE by the MAC and read out by the host. Frames are written to a transmit QUE by the host and read out by the MAC. QUE0 and QUE1 are receive QUEs (only QUE0 is implemented), and QUE2 through QUE7 are transmit QUEs (QUE2 through QUE5 are implemented). Writing to the *Transmit Data Register* (TDR) for a receive QUE or reading from the *Read Data Register* (RDR) for a transmit QUE is not supported and the result is undefined in this specification.

The transmit QUEs are further divided into standard QUEs, as described above, and static QUEs. Static QUEs differ from the standard QUEs in that they can only contain a single frame, and that frame must be 252 bytes or less in total size. Unlike standard QUEs, static QUEs do not remove a frame when it is read from the QUE. Once a frame is written to a static QUE, it can be read out any number of times and the static QUE will always read out the same one frame. If a second frame is written to a static QUE then it will replace the first as the one frame contained in the QUE.

The purpose of a static transmit QUE is to allow the host to configure a frame that will need to be transmitted multiple times or transmitted at a later time without any interaction with the host. Transmit QUE2 and QUE5 are static QUEs. Transmit QUE2 is best suited for MAC control pause frames as it can be triggered to transmit by a main buffer watermark. Transmit QUE5 is best suited to *Host Not Responding* (HNR) frames as it can be triggered to transmit by a host interrupt timeout.

When the MAC transmitter is idle and ready to transmit a frame, it determines which QUE to read from on a priority basis. The lowest numbered QUE containing data that needs to be transmitted is selected by the MAC, which means when more than one transmit QUE is ready, the one with the lowest number always gets priority.

6.3 Host Interface

6.3.1 Reading Receive Data

The status of the frame at the top of the receive FIFO can be obtained by reading the *Receive Packet Status Register* (RPSR). The 16 LSBs of the RPSR contain a count of the total number of bytes that have entered the receive FIFO for this frame. A value of zero means that there are no new frames in the receive FIFO. As frame bytes enter the FIFO, the count value is incremented. However, the count value does not decrease the bytes read out of the read FIFO such that the final value will always be the final frame size.

The MSB of the RPSR is the DONE bit. Once the last byte in the frame has entered the receive FIFO, the DONE bit is set indicating that the count value contained in the total bytes field now contains the final size in bytes of the frame and the error status and classification fields now contain the final frame status. When the DONE bit is asserted, this also indicates that the status for this frame has been removed from the receive status FIFO and future reads of the RPSR will refer to the next frame in the receive FIFO, even if all of the data for the current frame has not been retrieved.

The frame data is read from the receive FIFO 32 bits at a time by successive reads to the *Receive Data Register* (RDR). If the frame length is not an even multiple of 4 bytes then the final read of the RPDR register for that frame will be padded with zeros.

6.3.2 Writing Transmit Data

A transmit QUE is initialized by writing to its *Packet Control Word Register* (PCWR). This will assign an ID to the frame and select various transmission options. The frame size must then be set by writing to the QUE *Packet Size Register* (PSZR). Transmit data is then written to the transmit FIFO 32 bits at a time via successive writes to the *Transmit Data Register* (TDR).

If more bytes are written to the TDR than indicated n the PSZR, the excess bytes are ignored. Writes to the TDR past the end of the frame, however, will trigger a transmit FIFO overrun interrupt condition. Similarly, if a new frame is initialized by a write to the PCWR before the frame length counter is expired, a transmit FIFO under-run interrupt condition will result and the previous frame will be aborted. If there is any question, the PSZR can be queried for the remaining number of bytes expected in the previous frame before a new frame is initialized.

In the event that the host wishes to terminate a frame early without triggering an under-run interrupt and aborting the frame, or if the size of the frame is not initially known, the PSZR can be rewritten at any time before the end of the frame's transmission. As an example, no matter what the current value of the PSZR is, if it is written with a value of one then the next write to the TDR will add one byte to the completed frame. Conversely, if the frame byte counter is about to expire then writing a larger value to the PSZR will extend the frame. It is an error to write a value of zero to the PSZR and the circuit behavior in this case is undefined.

As each frame egresses the transmit FIFO, its status is placed in the transmit status FIFO. Transmit frame status is recovered by reading the *Transmit Packet Status Register* (TPSR). The Packet ID field from the PCWR is also placed in the TPSR such that the status can be associated with the exact frame to which it belongs.

6.3.2.1 Using the Setup Transmit Data Register

The *Setup Transmit Data Register* (STDR) can be used to control the way in which 32-bit data words are transferred to the transmit FIFO. The STDR can be changed on a word-by-word basis to change the network endianness or buffer-byte-alignment, or the STDR can be used to setup the transfer of an entire buffer of transmit data. A new frame must be initialized by a write to the PCWR before the STDR is setup for transferring frame data to the QUE.

The Count field of the STDR contains one less than the number of writes to the TDR that will be needed to complete the transfer of the buffer. The Start Offset field contains the number of bytes in the first write to the TDR to ignore. The End Offset field contains the number of bytes in the last write (when the Count field is equal to zero) to ignore.

Table 22: Transmit Data Buffer Example

	32-bit Write Data			
Transmit Order:	**Byte-1**	**Byte-2**	**Byte-3**	**Byte-4**
Start Offset = 2	X	X	B1	B2
	B3	B4	B5	B6
Count decrements for each write	…	…	…	…
	…	…	…	…
	B_{N-4}	B_{N-3}	B_{N-2}	B_{N-1}
End Offset = 3	B_N	X	X	X

Notes:

1. The End Offset will continue to be applied as long as the COUNT field of the STDR contains zero. If a non-zero End Offset is used, it must be cleared at the end of the block transfer.

2. The COUNT field must expire before the PSZR expires. Frames that are entirely contained within one block should not use the End Offset. Instead, use the PSZR to clip the last write to the TDR.

The Endian field of the STDR is used to set the transmit order of the data written on the bus, or how host bus write data bytes are mapped to transmit buffer bytes. If the Endian bit is set then the most significant byte of the host bus as defined by the logical endianness, is mapped to the first transmitted byte in the buffer, otherwise, the least significant byte is mapped to the first transmitted byte.

6.3.2.2 Preloading Transmit Data

A transmit QUE signals the MAC transmitter that it is ready to transmit by asserting the *QUE Data Ready* bit (QDR) in its *QUE Status Register* (QSR). The default behavior of the QDR for a transmit QUE is to assert anytime the QUE contains any data. This means that a transmit QUE can potentially begin transmitting as soon as the first BLOCK is added to the QUE. Once the QUE begins transmitting, data for the packet being transmitted must be added to the QUE faster than the transmitter removes it or a TX FIFO under-run condition will eventually abort the packet (see TPSR).

In the event that interrupt latency, host bus performance, or other issues may prevent the host from loading data into the QUE faster than it is removed by the MAC, the QSR can be used to modify the QDR behavior and prevent an under-run condition on the QUE. Bits 25 and 24 of the QSR are the Mode field. The default setting for the Mode field is 00b. In this mode the QDR bit is set anytime the QUE contains at least one BLOCK. In this mode, the host must be diligent in keeping the QUE populated with data to avoid a TX FIFO under-run condition in the MAC.

If the Mode setting is 01b then the QDR bit for the QUE is set only when the number of BLOCKs in the QUE is above the value indicated by the Threshold field. This will allow the host to fill the QUE up to the threshold level at its leisure without risk of a TX FIFO under-run. The drawback to this mode is that a small packet that uses fewer than the threshold number of BLOCKs will be stranded in the QUE until more data is added to the QUE to bring the total number of BLOCKs up and over the threshold.

If small packets are a problem, then the Mode setting of 10b can be used. In this mode, the QDR bit for the QUE is set only when there is an EOF in the QUE, or in other words, the QUE contains at least one entire frame. In this mode, TX FIFO under-runs are not possible since the QUE will not begin to transmit until it contains the entire frame. The draw-back to this mode is with very large frames. If a frame is too large to fit into the QUE all at one time then it will never begin transmitting and the QUE will be stalled. If both small and large packets are to be handled then a Mode setting of 11b should be used. In this mode, the QDR bit for the QUE is set anytime there is an EOF in the QUE or the number of BLOCKs in the QUE is above the threshold. In this way, large packets can preload a fixed number of BLOCKs while small packets are guaranteed to transmit.

To facilitate the handling of very large packets by a fast host, an interrupt that is tied to the QSR Threshold is provided. To make use of this, the host sets the Threshold field based on the interrupt latency. The host then preloads the QUE with some number of BLOCKs. As soon as the total number of blocks left in the QUE falls below the Threshold, an interrupt is generated. In response to the interrupt the host writes more data to the QUE to put the number back above the threshold. The host can then go on to other tasks until the next interrupt. This cycle is repeated until the frame is completed.

6.3.3 DMA Slave Mode Access

Reading or writing large amounts of data into and out of a single QUE involves accessing the same RDR or TDR register repeatedly. A DMA Slave Mode is implemented to facilitate this activity and reduce overhead on the host side. While in DMA Slave Mode, the address bus on the host interface is ignored and all access is assumed to be to the programmed address until DMA mode is terminated. In this way the host can use a DMA engine or block transfer facility to write or read QUE data without regard to the addresses generated.

DMA Slave Mode is controlled by the *DMA Register* (DMA) at address 0x100.

To read data from a QUE using DMA Slave Mode, the host writes the address of the RDR for the desired QUE into bits nine through zero and sets bit 17, the Read Mode bit, in the DMA register at address 0x100. The host then starts the DMA transfer and all read access to the host interface will go to the programmed RDR address. When the DMA transfer is complete, the DMA Mode is terminated by writing a zero to bit 17 of the *DMA Register* (DMA).

To write data to a QUE using DMA Slave Mode, the host writes the address of the TDR for the desired QUE into bits nine through zero and sets bit 16, the Write Mode bit, in the *DMA Register*. The host then starts the DMA transfer and all write access to the host interface will go to the programmed TDR address. When the DMA transfer is complete, reading the cleared Write Mode bit from the *DMA Register* terminates the DMA Mode.

DMA Slave Mode does not have any effect on other operations of the interface such that, for example, the ENDIAN settings, STDR settings, etc. are all in effect during a DMA Mode transfer. During a DMA mode transfer, the actual register address of the host bus access is ignored. This means that using DMA Slave Mode to transfer data out of order is not supported. Data words must always be written to a transmit QUE in the desired transmit order and are always read from a receive QUE in received order.

6.4 Snoop Mode Access

The Snoop Interface provides a means by which QUE data can be inspected and modified in situ**,** leaving the state of the QUE unchanged. The Snoop Interface works by presenting the contents of a specific BLOCK of QUE memory at the SNOOP address space 0x300-0x3FF. The *Snoop Control Register* (SNCR) is used to set which BLOCK of QUE memory is mapped into the SNOOP address space.

For example, an application that wishes to inspect or modify the contents of the first frame in the receive QUE, QUE0, first reads the value of the FIRST BLOCK in QUE0 from its *QFLR Register* (QFLR). The pointer to the FIRST BLOCK in QUE0 is then written to the SNCR register. Now that the *SNCR Register* has programmed the SNOOP interface to point to the FIRST BLOCK for QUE0, accessing registers in the address space from 0x300 to 0x3FF will be directly accessing the data for the first frame contained in QUE0.

Snooping the contents of a frame before it is read out of the receive QUE can be useful if additional inspection of the frame is needed, beyond what is provided by classification, to determine the disposition of a received frame. It can also be used, in conjunction with the QUE transfer feature, to minimize host bus overhead in responding to simple ARP or ICMP requests. In this case, the host can use the Snoop Interface to modify a received ARP or ICMP request and convert it into the appropriate response, while the frame is still resident in the receive QUE. The QUE Transfer feature is then used to transfer the response directly to a TX QUE and transmit it back to the source without having to read the entire frame into host memory.

6.5 Water Marking

The Timers module (see Section 6.8) monitors the number of free memory blocks in the system input. There are three watermarks (Interrupt, PAUSE and Headroom), accessed via the *Water Mark Values Register* (WMVR), which can be used to manage memory usage based on the size of the free memory pool.

6.5.1 Interrupt Watermark

When the number of free BLOCKs falls below the interrupt threshold, the WATER MARK interrupt in the HIR is triggered. An interrupt threshold setting of zero disables this feature.

6.5.2 PAUSE Watermark

When the number of free BLOCKs falls below the pause threshold, the QDR bit for the PAUSE QUE triggers the transmission of the pause frame. A pause threshold setting of zero disables this feature.

6.5.3 Headroom Watermark

When the number of free BLOCKs falls below the headroom threshold then the MAC receiver is halted causing the MAC to drop any frames received after completion of the current frame. This condition is cleared once the number of free BLOCKs rises back above the threshold. This prevents a saturated receiver from consuming all free memory thereby locking out the local transmitter. A headroom setting of zero disables this feature.

6.6 Counters

A block of hardware counters is implemented to allow monitoring transmit and receive statistics. These counters are accessed and managed by using the *Count Data Register* (CDR), the *Counter Control Register* (CCR) and the *Counter Management Register* (CMR).

6.6.1 Summary of Counters

Table 23 provides a summary of all counters by address. Counters at addresses 0x00 through 0x0E are transmit counters. Counters at addresses 0x0F through 0x27 are receive counters.

Table 23: Counter Summary

Counter Address	Counter Description
0x00	Transmitted Packets, 0 Collisions, not deferred or excessive deferred
0x01	Transmitted Packets, 1 Collision
0x02	Transmitted Packets, 2-15 Collisions
0x03	Excessive Collisions
0x04	Deferred transmissions
0x05	Late Collisions
0x06	MAC errors (TX under-run or transmit halted)
0x07	Lost carrier sense errors
0x08	Excessive deferrals
0x09	Total packets transmitted
0x0A	Multicast packets

Counter Address	Counter Description
0x0B	Broadcast packets
0x0C	SQE errors
0x0D	Pause packets transmitted
0x0E	Transmitted bytes
0x0F	Received packets, 63 bytes or less
0x10	Received packets, 64 bytes
0x11	Received packets, 65 to 127 bytes
0x12	Received packets, 128 to 255 bytes
0x13	Received packets, 256 to 511 bytes
0x14	Received packets, 512 to 1023 bytes
0x15	Received packets, 1024 to 1518 (1522 for VLAN tag) bytes
0x16	Received packets, 1519 bytes or more (1523 or more for VLAN tag) bytes
0x17	CRC error and no alignment error
0x18	Alignment errors
0x19	Fragment errors (less than 64 bytes with CRC or alignment error)
0x1A	Jabbers (greater than 1518 or 1522 and CRC or alignment error)
0x1B	MAC errors
0x1C	Dropped packets
0x1D	Classification dropped packet
0x1E	Total received packets with no errors
0x1F	Total received multicast packets with no errors
0x20	Total received broadcast packets with no errors
0x21	Range errors (length field <= 1500 and received data <= 1500 and not control packet and length field does not match data bytes received and unpadded packet and no CRC/alignment errors
0x22	Out of range count (length field > 1500 and not control packet 8808)
0x23	Total received VLAN packets with no errors
0x24	Total received Pause packets with no errors
0x25	Total received Control packets with no errors
0x26	Total received bytes with no errors
0x27	Total received bytes with errors but not jabber nor fragment

6.6.2 Reading and Setting Counter Values

Before any counters can be accessed, the CCR value must be set appropriately. Bits 0 to 5 of the CCR are the Address field. These bits must contain the address of the first counter to be accessed. Bit eight of the CCR is the Access Mode bit. When the Access Mode bit is clear, the access mode is read. When the Access Mode bit is set, the access mode is write. Bit nine of the CCR is the Clear on Read bit. The Clear on Read bit is only relevant when the access mode is read. When the Clear on Read bit is set, then the counter values are automatically reset to zero after the counter value is read. If a countable event occurs at the same time as the reset, then the counter value is reset to one such that no countable events are missed. Bit ten of the CCR must always be set.

Once the CCR has been configured for the desired counter access, the CDR is used to gain access to the actual counter values. When the CCR Access Mode bit is cleared for read, only read access to the CDR is allowed, and a read of the CDR will return the value of the counter specified by the CCR Address field. When the CCR Access Mode bit is set to write, only write access to the CDR is allowed, and the value written to the CDR will be written to the counter at the address specified by the CCR Address field. The CCR Address field value is automatically incremented after each read or write access to the CDR allowing many counters to be accessed through repeated reads or writes on the CDR without the need to reconfigure the CCR each time. When writing a value to a counter, if a countable event occurs at the

same time then the actual value placed into the counter is the CDR value plus one to prevent the loss of any countable events.

6.6.3 Precision Counting

Applications that require a high degree of temporal precision across all the counters can use the CMR for this purpose.

Bit two of the CMR is the Freeze bit. The Freeze bit can be used when the values of many or all counters must be known at an exact point in time. Setting the Freeze bit in the CMR will cause all counters to stop counting at that moment. Any countable events that occur after the Freeze bit is set are stored in an event FIFO. After the application has set the CMR Freeze bit, it should read all the counter values as quickly as possible. The event FIFOs are deep enough to hold off countable events for up to 28 microseconds assuming minimum sized frames are ingressing and or egressing at full 100 Mbps data rate, or 280 microseconds for 10 Mbps. When the application has finished reading the counter values, it should clear the CMR Freeze bit. All of the events stored in the FIFOs will be counted at that time. If any event FIFO fills before the application has cleared the CMR Freeze bit, then the hardware will auto-clear the freeze condition and count all events in the event FIFOs. To check for this condition, the application can query the CMR Freeze bit before clearing it. If it is already clear then the freeze condition had to be cleared by hardware in order to avoid losing any counts. In this case, not all of the counters read are guaranteed to be at their frozen value.

In the case that the application wants to start all the counters counting at the same time, the CMR provides a Clear Receive bit and a Clear Transmit bit. These bits are write only, they will always read back zero. When one is set, it causes all the read or write counters to be reset to zero at exactly the same time.

6.6.4 Rollover Interrupts

For applications that only need a much more coarse counter treatment, rollover interrupts are provided for each counter. The counter rollover interrupts can be individually enabled or disabled for each counter. In some cases it may be desirable to preload a counter with a nonzero value to set how many counts, it will take to roll the counter and trigger an interrupt.

The rollover indication for transmit counters zero through fourteen are bits zero through fourteen of the TRIR respectively. The rollover indication for receive counters fifteen through thirty-nine are bits zero through twenty-four of the RRIR respectively.

Each transmit and receive rollover bit can be individually enabled or disabled in terms of triggering a host interrupt. When a rollover bit is set then the RMON bit of the HIR will be set unless the mask bit corresponding to the rollover bit is clear. The RMON bit of the HIR will, in turn, trigger a host interrupt when its corresponding mask bit is set.

6.7 Packet Classification

The packet classification engine is comprised of a content addressable memory (CAM) linked to control logic (WCS), which is responsible for acting on the CAM result and generating the next CAM reference word. The WCS applies the first byte of packet data to the CAM using a previous hit value of zero. The resulting CAM address is then used to index a control word for the control logic to process. The control logic then uses the control word along with the CAM address and the next packet byte to generate another reference word to apply to the CAM. This process iterates until the packet is done or the control word calls for completion. The final classification result is the address of the last CAM hit.

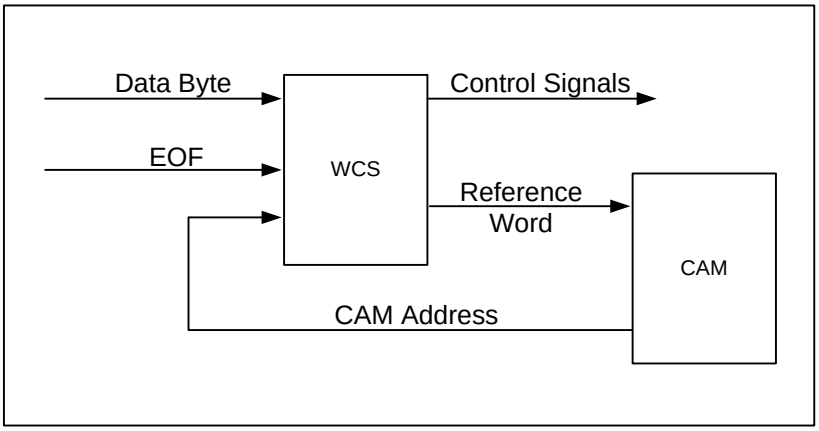


Figure 14: Classification Architecture

The CAM is a 128-word by 15-bit wide content addressable memory. When a reference data word is applied to the CAM, the result is the highest numbered address that contains a data word that matches the reference. Each data word contained in the CAM also contains 15 mask bits that conditionally disable individual data bits from preventing a match. Address 0 is reserved and can never match such that no reference data can ever result in a CAM address of zero. Address 1 is also reserved and always matches such that a reference word that does not match any entry in the CAM will give a result of one. Associated with each CAM entry is a control word. When a reference data word is presented to the CAM and an address results, the control word associated with that address is passed to the control logic that determines the next action taken by the packet classifier.

The control logic can execute any of the following actions:

- Set the most significant byte of the pause counter.
- Set the least significant byte of the pause counter.
- Start the pause timer.
- Cause the packet to be dropped.
- Wake the host from power down mode (starts the HNR timer).
- Interrupt the host.
- Manipulate the classification result reported in the RPSR.
- Identify multicast/broadcast frames for RMON statistics.
- Identify the Len/Type field for frame size checking.
- Identify the IP header for checksum checking.

To facilitate classification, the control logic contains a general purpose 8-bit register, ‘X’ and a 5-bit counter, ‘C’. The ‘X’ register can be used to store a packet byte or a CAM result for later use. The counter can be used as a loop index to iterate a set of rules a fixed number of times. The TOC action is used to set the counter and the DEC action is used to decrement the counter. When a DEC action causes the counter to expire, the loop is broken by decrementing the actual CAM address of the rule that executed the DEC action for the purposes of the next CAM reference word. To prevent ambiguity, the rule immediately below a rule that uses the DEC action should generally not be used.

Additionally, the control logic is responsible for generating the next 15-bit CAM match word by concatenating the next 8-bit packet data byte or the ‘X’ register value with the 7-bit address of the current CAM match. At the beginning of the packet, the previous CAM match is initialized to zero as is the control logic ‘X’ register. The CAM address of zero is reserved and will never result from a CAM match such that the first data byte in the frame is guaranteed to be the only byte that is accompanied by a zero value for the previous hit. In other words, a CAM rule with a specified value for the previous hit of zero will only match the first byte of the frame.

6.7.1 Address Filtering

The 78Q8430 CAM is loaded upon reset with a set of default rules for users who only want to use the address filter feature (see Section 6.7.4). The following rules are intended as a template to provide address-filtering functionality. They support four multicast and eight unicast address filters. The last unicast address filter rule is configured by default as a promiscuous mode rule such that the address-filter is in promiscuous mode right out of reset.

6.7.1.1 Promiscuous Mode Off

In promiscuous mode, all addresses are passed on to the host driver. This means that, as long as promiscuous mode is enabled, none of the other address filters are effective. Promiscuous mode must therefore be disabled before any address filtering can happen. The following procedure should be used to deactivate promiscuous mode:

STEP 1. Change the Match Control field of rule 0x30 from MD to DROP. This will cause any frame with an address that does not match any other address filter to be dropped.

6.7.1.2 Promiscuous Mode On

The promiscuous mode filter is a filter with all address bits masked as wildcard bits such that any address will match. Turning promiscuous mode on and off is the same as changing the promiscuous mode filter from a positive filter to a negative filter (see Section 6.7.1.5). The following procedure should be used to activate promiscuous mode:

STEP 1. Change the Match Control field of rule 0x30 from DROP to MD. This will cause all frames to pass the address filters.

6.7.1.3 Unicast Address Filters

The default CAM rule set supports eight unicast address filters. The first, unicast filter #0, is the promiscuous mode filter and is reserved for that purpose. The remaining seven are general use. Each filter has two components, the 48-bit address that it matches and a mask that defines which bits of the address are relevant and which bits are wildcards. Each byte of each address filter has a rule assigned to it. The following table summarizes the association of unicast filter bytes and CAM rules.

Table 24: CAM Rules Associated with Unicast Filter Bytes

	Byte [0]	Byte [1]	Byte [2]	Byte [3]	Byte [4]	Byte [5]
U/C Filter #7	0x77	0x6F	0x5F	0x57	0x47	0x37
U/C Filter #6	0x76	0x6E	0x5E	0x56	0x46	0x36
U/C Filter #5	0x75	0x6D	0x5D	0x55	0x45	0x35
U/C Filter #4	0x74	0x6C	0x5C	0x54	0x44	0x34
U/C Filter #3	0x73	0x6B	0x5B	0x53	0x43	0x33
U/C Filter #2	0x72	0x6A	0x5A	0x52	0x42	0x32
U/C Filter #1	0x71	0x69	0x59	0x51	0x41	0x31

Note: Bytes are in network transmit order starting with Byte [0].

For an arbitrary unicast filter number *N*, the following procedure should be used to set the address and mask values:

STEP 1. Write address and mask byte [0] to the CAM. CAM rule 0x70+*N* should be written as shown in the following table:

Reg.	Field	Value to write
CAR	ADDR	0x70+*N*
RMR	Data Match	Value of MAC address byte [0]
	Data Mask	Value of mask byte [0] from the Wild Card setting (0xFF is for a perfect match)
	Previous Hit Match	0x00 to disable the filter
	Previous Hit Mask	0x00
RCR	Byte Offset	Retain default: 0x00
	Interrupt	Retain default: 0
	Control Logic Action	Retain default: NOP
	Match Control	Retain default: MD

STEP 2. Write address and mask byte [1] through byte [4] to the CAM. For each byte the CAM rule indicated by Table 24 based on the filter number, N, and byte number should be written as follows.

Reg.	Field	Value to write			
CAR	ADDR	byte [1]: 0x68+*N*	byte [2]: 0x58+*N*	byte [3]: 0x50+*N*	byte [4]: 0x40+*N*
RMR	Data Match	Value of MAC address byte [1] … byte [4]			
	Data Mask	Value of mask byte [1] . . . byte [4]			
	Previous Hit Match	Value of the CAM rule used by the previous byte			
	Previous Hit Mask	0x7F			
RCR	Byte Offset	Retain default: 0x00			
	Interrupt	Retain default: 0			
	Control Logic Action	Retain default: NOP			
	Match Control	Retain default: MD			

Unlike the settings for byte [0], the Previous Hit Mask field is set to 0x7F and the Previous Hit Match field is always set to the value of the CAM rule used by the previous byte. As an example, the Previous Hit Mask fields for filter #1 would be 0x71, 0x69, 0x59 and 0x51, for byte [1] through byte [4] respectively.

STEP 3. Write address and mask byte [5] to the CAM. CAM rule 0x30+*N* should be written as follows.

Reg.	Field	Value to write
CAR	ADDR	0x30+*N*
RMR	Data Match	Value of MAC address byte [5]
	Data Mask	Value of mask byte [5]
	Previous Hit Match	Set to the CAM rule that was used for byte [4] (0x40+*N*).
	Previous Hit Mask	0x7F
RCR	Byte Offset	Retain default: 0x00
	Interrupt	Retain default: 0
	Control Logic Action	Set to TAX
	Match Control	Retain default: MD

STEP 4. Enable the filter. The unicast address filter is enabled by setting the Previous Hit Mask field of the CAM rule for byte [0] to 0x7F. This step must be done last to prevent an ingressing frame from matching a partial set of filter rules. All the rules for a filter must be in place before enabling the filter.

An address filter can be simply activated/deactivated by toggling the value of the Previous Hit Mask field for the byte [0] CAM rule between 0x7F and 0x00 respectively. The promiscuous mode filter, filter #0, should not be deactivated in this way.

It is important that STEP 1 deactivates the filter so that no frames are filtered using a partial filter setting before all relevant rules are written. Step 4 reactivates the filter once the new settings are in place.

6.7.1.4 Multicast Address Filters

The default CAM rule set supports four multicast address filters. The first, multicast filter #0, serves the same purpose as the promiscuous mode filter except it applies only to multicast addresses. The last, multicast filter #3, is the broadcast filter and is reserved for that purpose. The second, multicast filter #1, is the PAUSE filter and is setup by default to match the PAUSE address. Multicast filter #2 is unused by default and available for general use. Each filter has two components, the 48-bit address that it matches and a mask that defines which bits of the address are relevant and which bits are wildcards. Each byte of each address filter has a CAM rule assigned to it. Table 25 summarizes the association of multicast filter bytes and CAM rules.

Table 25: CAM Rules Associated with Multicast Filter Bytes

	Byte [0]	Byte [1]	Byte [2]	Byte [3]	Byte [4]	Byte [5]
M/C Filter #3	0x7F	0x67	0x63	0x4F	0x4B	0x3F
M/C Filter #2	0x7E	0x66	0x62	0x4E	0x4A	0x3E
M/C Filter #1	0x7D	0x65	0x61	0x4D	0x49	0x3D

Note: Bytes are in network transmit order starting with Byte [0].

For an arbitrary multicast filter number *N*, the following procedure should be used to set the address and mask values:

STEP 1. Write address and mask byte [0] to CAM rule 0x7C+*N* as follows.

Reg.	Field	Value to write
CAR	ADDR	0x7C+*N*
RMR	Data Match	Value of MAC address byte [0][1]
	Data Mask	Value of mask byte [0][1]
	Previous Hit Match	0x00 to disable the filter
	Previous Hit Mask	0x00
RCR	Byte Offset	Retain default: 0x00
	Interrupt	Retain default: 0
	Control Logic Action	SETMC
	Match Control	Retain default: MD

[1]The LSB of both address byte [0] and mask byte [0] must be set for multicast address filters. If the LSBs are not set then the address is not multicast and belongs in the unicast filter set.

STEP 2. Write address and mask byte [1] through byte [4] to the CAM. For each byte the CAM rule indicated by table 5.7.2 based on the filter number and byte number should be written as follows.

Reg.	Field	Value to write			
CAR	ADDR	byte [1]: 0x64+*N*	byte [2]: 0x60+*N*	byte [3]: 0x4C+*N*	byte [4]: 0x48+*N*
RMR	Data Match	Value of MAC address byte [1] … byte [4]			
	Data Mask	Value of mask byte [1] . . . byte [4]			
	Previous Hit Match	Value of the CAM rule used by the previous byte [1]			
	Previous Hit Mask	0x7F			
RCR	Byte Offset	Retain default: 0x00			
	Interrupt	Retain default: 0			
	Control Logic Action	Retain default: NOP [2]			
	Match Control	Retain default: MD			

[1]As an example, the Previous Hit Match fields for filter #1 would be 0x7D, 0x65, 0x61 and 0x4D, for byte [1] through byte [4] respectively.

[2]An exception is byte [4] of the broadcast filter. Multicast filter #3, byte [4] should have the Control Logic Action field set to TAX.

STEP 3. Write address and mask byte [5] to CAM rule 0x3C+*N* as follows.

Reg.	Field	Value to write
CAR	ADDR	0x3C+*N*
RMR	Data Match	Value of MAC address byte [5]
	Data Mask	Value of mask byte [5]
	Previous Hit Match	Set to the CAM rule that was used for byte [4] (0x48+*N*).
	Previous Hit Mask	0x7F
RCR	Byte Offset	Retain default: 0x00
	Interrupt	Retain default: 0
	Control Logic Action	Set to TAX[1]
	Match Control	Retain default: MD

[1]**Exception**: Multicast filter #3, byte [5] should have the Action field set to SETBC.

STEP 4. Enable the filter. The multicast address filter is enabled by setting the Previous Hit Mask field of the CAM rule for byte [0] to 0x7F. This step must be done last to prevent an ingressing frame from matching a partial set of filter rules. All the rules for a filter must be in place before enabling the filter.

A Multicast address filter can be simply activated/deactivated by toggling the value of the Previous Hit Mask field for the byte [0] CAM rule between 0x7F and 0x00 respectively. Multicast filter #0 should not be deactivated in this way.

It is important that STEP 1 deactivates the filter so that no frames are filtered using a partial filter setting before all relevant rules are written. STEP 4 reactivates the filter once the new settings are in place.

6.7.1.5 Negative Address Filters

Any address filter, either multicast or unicast, can be set as either a positive or negative filter. A positive filter is a filter that passes frames with a source MAC address that matches the filter. A negative filter is a filter that blocks frames with a source MAC address that matches the filter. By default, all filters are positive acting. The following procedure is used to change a filter to negative action:

STEP 1. Change the Match Control field for the CAM rule for byte [5] from MD to DROP.

To change a filter back to a positive acting filter, change the same Match Control field back to MD.

6.7.2 Configuring the CAM

The CAM rules are accessed indirectly one at a time via the *CAM Address Register* (CAR). The contents of the rule whose number is indicated by the CAR are available for read and write via the *Rule Match Register* (RMR) and the *Rule Control Register* (RCR). The RMR contains a template that the CAM reference word must match in order to trigger the rule, and the RCR contains the control word that is passed to the control logic when the rule is triggered.

6.7.2.1 Rule Match Register

The RMR contains four fields that control when a rule is triggered: Previous Hit Match and Previous Hit Mask, Data Match and Data Mask. The mask fields are used to determine which bits in their respective match field are required to make a match and which bits are ignored. A mask bit value of one means that the corresponding match bit must be exactly equal to the same bit in the CAM reference word to trigger the rule. Inversely, a mask bit value of zero means that the corresponding bit in the CAM reference word is ignored. A special case is that all previous hit mask bits are zero. In this case, the rule is deactivated and can never be triggered.

6.7.2.2 Rule Control Register

The RCR contains four fields that control the actions taken by the control logic when the rule is triggered: Byte Offset, Interrupt, Action and Match Control fields.

RCR Byte Offset

The Byte Offset field is generally used to skip over bytes in the frame that are not relevant to the current classification. When the Byte Offset is non-zero then the classification will skip the number of bytes indicated. The exception is when the TOC action is used, in which case, the value of the Byte Offset field is used to initialize the control logic counter and no offset is applied.

An offset value of 0x3F will skip just the right number of bytes to jump over the current IPv4 header.

RCR Interrupt

When the Interrupt bit in the RCR for a given rule is set, then the triggering of the rule will cause an HIR classification interrupt.

Control Logic Action

The value of the control logic Action field in the RCR determines the action that will be taken by the control logic when the rule is triggered.

Table 26: Control Logic Actions

Hex Value	Binary Value	Name	Action Taken
0x0	00000b	NOP	No action taken.
0x2	00010b	PAUSE	Start the local pause timer.
0x4	00100b	WAKE	Send a wake-up signal to the host and start the HNR timer.
0x6	00110b	IPCK	Start the IP header checksum check and the IP header counter.
0x7	00111b	TIPO	Transfer IP header counter to offset.
0x8	01000b	TDX	‘X’ is assigned the value of the frame data.
0xA	01010b	TAX	‘X’ is assigned the value of the current rule number.
0xC	01100b	TAXH	The high-order nibble of ‘X’ is assigned the value of the low-order nibble of the current rule number.
0xD	01110b	TAXL	The low-order nibble of ‘X’ is assigned the value of the low-order nibble of the current rule number.
0x10	10000b	TXA	The classification result is assigned the value of ‘X’.
0x12	10010b	TLXA	The low-order nibble of the classification result is assigned the value of the low-order nibble of ‘X’.

Hex Value	Binary Value	Name	Action Taken
0x14	10100b	THXA	The high-order nibble of the classification result is assigned the value of the high-order nibble value of 'X'.
0x15	10101b	SETMC	Mark the frame as multicast for Rx statistics purposes.
0x16	10110b	VLAN	Mark the frame as VLAN tagged for length checking and statistics.
0x17	10111b	SETBC	Mark the frame as broadcast for Rx statistics purposes.
0x18	11000b	TOC	The control logic counter value is initialized to the value contained in the Byte Offset field. No offset is applied.
0x1A	11010b	DEC	The control logic counter value is decremented. If the counter has reached zero then the control logic will decrement the previous hit value used to generate the next CAM reference word by one.
0x1B	11011b	MCTL	Classify the frame as a MAC control frame. This also sets the Len/Type LSB.
0x1C	11100b	TDPH	The pause counter most significant byte is set from the frame data.
0x1D	11101b	TDLTH	The Len/Type most significant byte is set from the frame data.
0x1E	11110b	TDPL	The pause counter least significant byte is set from the frame data.
0x1F	11111b	TDLTL	The Len/Type least significant byte is set from the frame data.

RCR Match Control

The value of the Match Control field will determine how the control logic generates the next CAM reference word.

Table 27: RCR Match Control

Value	Name	Action Taken
00b	DONE	No more CAM reference words are generated. No further classification is done for the current frame.
10b	MD	The next frame data is used to generate the next CAM reference word.
01b	MX	The 'X' value is used in place of the frame data to generate the next CAM reference word.
11b	DROP	Drop the frame. If this is executed within the first 128 bytes of the frame then the entire frame is dropped from the QUE. No more CAM reference words are generated.

6.7.3 Frame Format

The following table shows the format of an Ethernet frame. The fields are in the order that the classification engine sees them, from left to right. The byte count for each field is specified on the bottom row of the table.

Table 28: Ethernet Frame for Classification

Destination Address	Source Address	Len/Typ		LLC Data		CRC (FCS)			
		Hi	Lo	User	Pad	MSB			LSB
6 Bytes	6 Bytes	1B	1B	0-1500B	46-0B	4 Bytes			

If the Len/Type field contains a 16-bit value that is less than 0x0600, the field is interpreted as a length field that specifies the number of bytes in the User field. If the value is greater than or equal to 0x0600, the type interpretation is to be used.

6.7.4 Default CAM Rule Summary

This section provides the default rules that the 78Q8430B CAM is loaded with on reset.

6.7.4.1 Destination Address

Table 29 contains the rules processing destination address, which also includes the pause packet and promiscuous mode.

Table 29: Process Destination Address Rules

Rule#	PrevHit	PH-Mask	Data	D-Mask	Next	Offset	Action	Interrupt	Comment
0x7F	0x00	0x7F	0xFF	0xFF	MD	0x00	SETMC	0	
0x7E	0x00	0x00	0x00	0x00	MD	0x00	SETMC	0	
0x7D	0x00	0x7F	0x01	0xFF	MD	0x00	SETMC	0	
0x7C	0x00	0x7F	0x01	0x01	MD	0x00	SETMC	0	
0x7B	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	Not used
0x7A	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	Not used
0x79	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	Not used
0x78	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	Not used
0x77	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	
0x76	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	
0x75	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	
0x74	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	
0x73	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	
0x72	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	
0x71	0x00	0x00	0x00	0x00	MD	0x00	NOP	0	
0x70	0x00	0x7F	0x00	0x00	MD	0x00	NOP	0	
0x6F	0x77	0x00	0x00	0x00	MD	0x00	NOP	0	
0x6E	0x76	0x00	0x00	0x00	MD	0x00	NOP	0	
0x6D	0x75	0x00	0x00	0x00	MD	0x00	NOP	0	
0x6C	0x74	0x00	0x00	0x00	MD	0x00	NOP	0	
0x6B	0x73	0x00	0x00	0x00	MD	0x00	NOP	0	
0x6A	0x72	0x00	0x00	0x00	MD	0x00	NOP	0	
0x69	0x71	0x00	0x00	0x00	MD	0x00	NOP	0	
0x68	0x70	0x78	0x00	0x00	MD	0x00	NOP	0	
0x67	0x7F	0x7F	0xFF	0xFF	MD	0x00	NOP	0	
0x66	0x7E	0x00	0x00	0x00	MD	0x00	NOP	0	
0x65	0x7D	0x7F	0x80	0xFF	MD	0x00	NOP	0	
0x64	0x7C	0x7C	0x00	0x00	MD	0x00	NOP	0	
0x63	0x67	0x7F	0xFF	0xFF	MD	0x00	NOP	0	
0x62	0x66	0x00	0x00	0x00	MD	0x00	NOP	0	
0x61	0x65	0x7F	0xC2	0xFF	MD	0x00	NOP	0	
0x60	0x64	0x7C	0x00	0x00	MD	0x00	NOP	0	
0x5F	0x6F	0x00	0x00	0x00	MD	0x00	NOP	0	
0x5E	0x6E	0x00	0x00	0x00	MD	0x00	NOP	0	
0x5D	0x6D	0x00	0x00	0x00	MD	0x00	NOP	0	
0x5C	0x6C	0x00	0x00	0x00	MD	0x00	NOP	0	
0x5B	0x6B	0x00	0x00	0x00	MD	0x00	NOP	0	
0x5A	0x6A	0x00	0x00	0x00	MD	0x00	NOP	0	
0x59	0x69	0x00	0x00	0x00	MD	0x00	NOP	0	
0x58	0x68	0x78	0x00	0x00	MD	0x00	NOP	0	

Rule#	PrevHit	PH-Mask	Data	D-Mask	Next	Offset	Action	Interrupt	Comment
0x57	0x5F	0x00	0x00	0x00	MD	0x00	NOP	0	
0x56	0x5E	0x00	0x00	0x00	MD	0x00	NOP	0	
0x55	0x5D	0x00	0x00	0x00	MD	0x00	NOP	0	
0x54	0x5C	0x00	0x00	0x00	MD	0x00	NOP	0	
0x53	0x5B	0x00	0x00	0x00	MD	0x00	NOP	0	
0x52	0x5A	0x00	0x00	0x00	MD	0x00	NOP	0	
0x51	0x59	0x00	0x00	0x00	MD	0x00	NOP	0	
0x50	0x58	0x78	0x00	0x00	MD	0x00	NOP	0	
0x4F	0x63	0x7F	0xFF	0xFF	MD	0x00	NOP	0	
0x4E	0x62	0x00	0x00	0x00	MD	0x00	NOP	0	
0x4D	0x61	0x7F	0x00	0xFF	MD	0x00	NOP	0	
0x4C	0x60	0x7C	0x00	0x00	MD	0x00	NOP	0	
0x4B	0x4F	0x7F	0xFF	0xFF	MD	0x00	TAX	0	
0x4A	0x4E	0x00	0x00	0x00	MD	0x00	NOP	0	
0x49	0x4D	0x7F	0x00	0xFF	MD	0x00	NOP	0	
0x48	0x4C	0x7C	0x00	0x00	MD	0x00	NOP	0	
0x47	0x57	0x00	0x00	0x00	MD	0x00	NOP	0	
0x46	0x56	0x00	0x00	0x00	MD	0x00	NOP	0	
0x45	0x55	0x00	0x00	0x00	MD	0x00	NOP	0	
0x44	0x54	0x00	0x00	0x00	MD	0x00	NOP	0	
0x43	0x53	0x00	0x00	0x00	MD	0x00	NOP	0	
0x42	0x52	0x00	0x00	0x00	MD	0x00	NOP	0	
0x41	0x51	0x00	0x00	0x00	MD	0x00	NOP	0	
0x40	0x50	0x78	0x00	0x00	MD	0x00	NOP	0	
0x3F	0x4B	0x7F	0xFF	0xFF	MD	0x00	SETBC	0	BC
0x3E	0x4A	0x00	0x00	0x00	MD	0x00	TAX	0	
0x3D	0x49	0x7F	0x01	0xFF	MD	0x00	TAX	0	PAUSE
0x3C	0x48	0x7C	0x00	0x00	MD	0x00	TAX	0	MC
0x3B	0x00	0x00	0x00	0x00	MD	0x00	TAX	0	Not used
0x3A	0x00	0x00	0x00	0x00	MD	0x00	TAX	0	Not used
0x39	0x00	0x00	0x00	0x00	MD	0x00	TAX	0	Not used
0x38	0x00	0x00	0x00	0x00	MD	0x00	TAX	0	Not used
0x37	0x47	0x00	0x00	0x00	MD	0x00	TAX	0	
0x36	0x46	0x00	0x00	0x00	MD	0x00	TAX	0	
0x35	0x45	0x00	0x00	0x00	MD	0x00	TAX	0	
0x34	0x44	0x00	0x00	0x00	MD	0x00	TAX	0	
0x33	0x43	0x00	0x00	0x00	MD	0x00	TAX	0	
0x32	0x42	0x00	0x00	0x00	MD	0x00	TAX	0	
0x31	0x41	0x00	0x00	0x00	MD	0x00	TAX	0	
0x30	0x40	0x78	0x00	0x00	MD	0x00	TAX	0	promiscuous

6.7.4.2 Source Address Filtering

Source address filtering can be used to drop frames with a specific address while passing all others. Table 30 contains the rules on processing source address.

Table 30: Process Source Address Rules

Rule#	PrevHit	PH-Mask	Data	D-Mask	Next	Offset	Action	Interrupt	Comment
0x2F	0x30	0x70	0x01	0x01	DROP	0x00	NOP	0	MC drop
0x2E	0x30	0x70	0x00	0x00	MD	0x05	NOP	0	pass other

6.7.4.3 Length/Type Field, MAC Control Frames and IP Header Checksum

Table 31 contains the rules on processing length/type, MAC control frames and start IP header checksum check.

Table 31: Process Length/Type, MAC Control Frames and Start IP Header Checksum Rules

Rule#	PrevHit	PH-Mask	Data	D-Mask	Next	Offset	Action	Interrupt	Comment
0x2D	0x2B	0x7F	0x00	0xFF	MD	0x02	VLAN	0	
0x2C	0x00	0x00	0x00	0x00	DONE	0x00	NOP	0	
0x2B	0x2E	0x7F	0x81	0xFF	MD	0x00	TDLTH	0	
0x2A	0x2B	0x7F	0x00	0x00	DONE	0x00	TDLTL	0	
0x29	0x2F	0x7C	0x88	0xFF	MD	0x00	TDLTH	0	
0x28	0x29	0x7F	0x08	0xFF	MD	0x00	MCTL	0	
0x27	0x29	0x7F	0x00	0x00	DONE	0x00	TDLTL	0	
0x26	0x2F	0x7C	0x00	0x00	MD	0x00	TDLTH	0	
0x25	0x26	0x7F	0x00	0x00	MD	0x00	TDLTL	0	
0x24	0x25	0x7F	0x40	0xF0	MD	0x00	IPCK	0	
0x23	0x24	0x7E	0x00	0x00	MD	0x3F	TXA	0	
0x22	0x28	0x7F	0x00	0xFF	MD	0x00	NOP	0	
0x21	0x28	0x7F	0x00	0x00	DONE	0x00	NOP	0	
0x20	0x22	0x7F	0x01	0xFF	MD	0x00	NOP	0	MCTL pause
0x1F	0x22	0x7F	0x00	0x00	DONE	0x00	NOP	0	MCTL other
0x1E	0x20	0x7F	0x00	0x00	MD	0x00	TDPH	0	
0x1D	0x1E	0x7F	0x00	0x00	MX	0x00	TDPL	0	
0x1C	0x1D	0x7F	0x3D	0xFF	DONE	0x00	PAUSE	0	
0x1B	0x1D	0x7F	0x00	0x00	DONE	0x00	NOP	0	MCTL pause with bad SRC

6.7.4.4 Wake on LAN

The packet classification engine can use the WAKE action to signal the host to come out of power down mode. This is used to implement the Wake-On-LAN feature.

The *Power Management Control and Status Register* (PMCSR) is used to control the hardware response to a WAKE action. **If the PS field of the PMCSR is zero then all WAKE actions are ignored. The WAKE action is only honored if the part is currently in a power down mode as determined by the PS field.** If the PME_ENB bit in the PMCSR is set then a valid WAKE action will trigger the assertion of the PMEB primary output. If the PME_ENB bit is clear then a valid WAKE action will only result in the normal HIR WAKE interrupt.

When the host is notified of a valid WAKE event, either by the assertion of the PMEB primary output or assertion of INTB via the WAKE HIR interrupt, the rule that triggered the event can be read from the *Wake Up Status Register* (WUSR). A valid WAKE event will also start the Host Not Responding (HNR) timer. When the host is notified of a WAKE event, it must clear the event by setting the PME bit in the

PMCSR. This action will clear the WAKE event and clear the WAKE bit in the HIR and the PMEB primary output, if it was enabled. If the HNR timer expires before the host clears the WAKE event then the QDR bit for QUE5 is set triggering the transmission of the HNR frame contained in QUE5. The length of the HNR timer is determined by the value contained in the Host Not Responding Count Register (HNRCR).

When configuring for Wake On LAN, the host should set the HNRCR with a value based on the longest anticipated interrupt service latency.

OnNow Packets

The OnNow specification states that an OnNow compliant node must be able to wake up upon the reception of a frame that matches a reference frame with a byte mask applied. Table 32 contains the rules on processing OnNow packets.

Table 32: Process Rules for OnNow Packet

Rule#	PrevHit	PH-Mask	Data	D-Mask	Next	Offset	Action	Interrupt	Comment
0x15	0x23	0x7F	0x54	0xFF	MD	0x00	NOP	0	
0x14	0x15	0x7F	0x00	0x00	MD	0x02	NOP	0	
0x13	0x14	0x7F	0x04	0xFF	MD	0x00	NOP	0	
0x12	0x13	0x7F	0x05	0xFF	MD	0x00	NOP	0	
0x11	0x12	0x7F	0x06	0xFF	MD	0x00	NOP	0	
0x10	0x11	0x7F	0x07	0xFF	DONE	0x00	WAKE	0	

Magic Packets

A magic packet is defined to be a frame that contains a specific sequence of bytes anywhere in its USER field. Table 33 contains the rules on checking for the sequence in a frame and waking the host if it finds a magic packet.

Table 33: Process Rules for Magic Packet

Rule#	PrevHit	PH-Mask	Data	D-Mask	Next	Offset	Action	Interrupt	Comment
0x0F	0x25	0x7F	0xFF	0xFF	MD	0x05	TOC	0	Bare Ethernet
0x0E	0x23	0x7F	0xFF	0xFF	MD	0x05	TOC	0	IP payload
0x0D	0x01	0x7F	0xFF	0xFF	MD	0x05	TOC	0	offset payload
0x0C	0x0F	0x7C	0xFF	0xFF	MD	0x00	DEC	0	
0x0B	0x0B	0x7F	0xFF	0xFF	MD	0x00	NOP	0	
0x0A	0x00	0x00	0x00	0x00	DONE	0x00	NOP	0	
0x09	0x0B	0x7F	0x10	0xFF	MD	0x0F	TOC	0	
0x08	0x03	0x7F	0x10	0xFF	MD	0x00	NOP	0	
0x07	0x08	0x7E	0x20	0xFF	MD	0x00	NOP	0	
0x06	0x07	0x7F	0x30	0xFF	MD	0x00	NOP	0	
0x05	0x06	0x7F	0x40	0xFF	MD	0x00	NOP	0	
0x04	0x05	0x7F	0x50	0xFF	MD	0x00	NOP	0	
0x03	0x04	0x7F	0x60	0xFF	MD	0x00	DEC	0	
0x02	0x02	0x7F	0x00	0x00	DONE	0x00	WAKE	0	

6.8 Timers

The Timers block implements several timers used within the system. Watermarking for main memory is also handled in this block as it relates to the PAUSE operation.

6.8.1 PAUSE Timer

The PAUSE timer is used to implement the MAC Control PAUSE operation described in Annex 31B of IEEE STD 802.3-2002. It consists of a 16-bit counter that determines the duration of the pause state. The host can also trigger a local pause state via the Start Pause bit of the PDCR.

6.8.2 HNR Timer

The Host Not Responding timer is used to notify remote nodes that have requested a Wake-On-LAN that the local host is not responding to the request. The host, knowing about how long it should take to wake, sets the value for how long to wait after a wake request for the host to clear the interrupt before a timeout triggers the transmission of a Host Not Responding packet. This value is set in the *Host Not Responding Count Register* (HNRCR).

The host can determine the wake status by reading the *Power Management Control and Status Register* (PMCSR). The default state is clear.

The HNR counter is decremented on every system clock that it has a non-zero value.

6.8.3 Interrupt Delay Timer

The Interrupt Delay Timer is used to delay the received data interrupt to the host. The host determines how long the delay should be by writing a value to the *Interrupt Delay Count Register* (IDCR).

As noted above, the interrupt timer is using MAC receive byte times as its unit of time. The value written to the IDCR can therefore be thought of as the maximum number of bytes that could possibly be received between the time the first data was added to the QUE and when the received data interrupt is actually triggered.

6.9 EEPROM Controller

The PROM controller provides logic for reading and writing an optional external EEPROM or ROM device. The external devices supported are the MicroChip 93LC46B and the National NM93C46. Timing compatible devices, smaller devices and read-only equivalent devices are also supported.

The basic sequences of events in accessing an external EEPROM or serial ROM are:

- System software reads the busy bit to ensure the EEPROM controller is not busy.
- On a write, the data should be written into the data register before setting the control register.
- Software writes the address and the read/write flag and sets the busy bit.
- The controller completes the operation and clears the busy bit.
- On a read, when system software detects the busy bit is cleared, it can read the data register.

6.10 Ethernet MAC

The MAC consists of a transmit block, a receive block, a control register, a flow control block and a serial controller for station management communications to the PHY and the optional external EEPROM/ROM. The MAC also has a loop back circuit.

6.10.1 MAC Transmit Block

The MAC transmit block moves the outgoing data from the MAC transmit FIFO, encapsulates it and passes it on to the MII interface logic in the PHY. The transmit block has circuits for generating preamble and jam bytes, pad bytes, the CRC value and error extension. The transmit block also has a timer for the back-off delay after a collision and a timer for the inter-packet gap after transmission.

6.10.2 MAC Receive Block

The receive block receives frames from the PHY via the MII interface. It strips the preamble and SOF and passes the remainder of the received frame data and error information to the MAC receive FIFO. The MAC receiver passes all frames received, including error frames and collisions. Dropping of error frames is handled by the receive producer in the QUE logic.

6.10.3 MAC Control Register

The *MAC Control Register* (MCR) provides controls for network operation, including:

- Enable and disable transmit and receive circuit, including requests to halt at end of current packet.
- Enable and disable full duplex operation and loopback modes.
- Enable and disable various MAC features like excessive-deferral detection, SQE and CRC checking.

6.10.4 Transmitting a Frame

To transmit a frame, the transmit enable bit in the MCR must be set and the transmit halt request bit must be clear. The MAC does not signal the DMA engine to transfer bytes to the MAC transmit FIFO. The QUE transmit controller controls the transfer of bytes to the MAC transmit FIFO.

The MAC transmit block then starts transmitting the data in the FIFO, but will retain the first 64 bytes until it has acquired the net. At that time, the MAC transmit block will request more data and transmit it until the QUE transmit controller signals the end of the frame to be transmitted. The MAC transmit block generates pad bytes, if needed, appends the calculated CRC to the end of the packet if requested and transmission stops. It sets the completion bit in the *Transmit Packet Status Register* (TPSR), signaling the end of a transmission, which may in turn cause an interrupt. If the QUE transmit controller indicates an error then the MAC transmit block will transmit an MII error status and abort the frame.

The MAC transmit block does not begin transmission until the number of bytes indicated by the preload field of the PCWR are in the MAC transmit FIFO. This is to give the IP header checksum generator a head start in generating the checksum. This may be needed since the checksum is in the middle of the IP header but cannot be known until the entire header is summed. The results are undefined if the header checksum is inserted into the frame after the checksum has already been transmitted.

6.10.5 IEEE 802.3 Transmit Protocols

6.10.5.1 Interpacket Gap Timing

In half duplex mode, the gap state machine is responsible for counting the 96 bit times from the de-assertion of the carrier sense signal, which is the inter-record gap. It breaks the 96 bit times for inter-record gap into the first 64 bits and the last 32 bits, in order to precisely control the appropriate times for beginning transmission. If there is any traffic within the first 64-bit times, it resets the counter and resumes counting from zero. If there is any traffic within the last 32 bits, it continues counting and signals the end at 96 bit times. In full duplex mode, the gap state machine starts counting at the end of transmission and signals the end at 96 bit times (12 byte times).

6.10.5.2 Collision Processing and Back-off

If the main transmit state machine detects a collision, it starts the back-off state machine counters and waits for the end of the back-off slot, before retransmitting the collision causing packet again. Each back-off slot is a multiple (including zero) of 512 bit times. Each time there is a collision for the same packet, the back-off state machine increments an internal attempt counter. A pseudo-random number generator outputs a random number by selecting a subset of the value of the generator. The subset grows by one bit for each subsequent attempt. This implements the equation:

$$0 < r < 2\ k,\ k = \min.\ (n, 10)$$

where r is the number of slot times that the MAC has to wait in case of a collision, and n is the number of attempts. For example, after the first collision, n is 1 and r is a random number between 0 and 1. The pseudo-random-number generator in this case is one-bit wide and gives a random number of either 0 or

1. After the second attempt, r is a random number between 0 and 3; the state machine looks at the two least significant bits of the generator (n = 2) which gives a value between 0 and 3.

In order to improve the statistical independence between two MACs using the same pseudo-random number generator, the MAC uses values from the CRC of previous successfully transmitted packets to modify the basic random number sequence.

6.10.6 Transmit Operation

If there is data to be transferred, the inter-packet gap is OK and the MII is ready (there are no collisions and the device is either in full duplex mode or there is no CRS), then the MAC transmit block transmits the preamble followed by the SFD. After the transmission of the preamble and the SFD, it transmits 64 bytes of data regardless of the packet length, unless short transmission is enabled. This means that if the packet is less than 64 bytes, it will pad the LLC data field with zeroes, unless NoPad is enabled. At the end of the packet, it appends the CRC, unless NoCRC generation is enabled. If there is any collision during the first 64 bytes (8 bytes of preamble and SFD and 56 bytes of the frame), it stops the transmission and transmits a jam pattern (32 bits of all ones). It increments the collision attempt counter, returns control to the back-off state machine and retransmits the packet when the back-off time has elapsed and the gap time is OK.

If there is a collision after the first 64 bytes, it is reported as a late collision and the packet is terminated with an error indication. The 78Q8430 does not retry late collisions.

If there are no collisions, the MAC transmit block transmits the rest of the packet and at this time (after the first 64 bytes have been transmitted without collisions), it allows the DMA engine to overwrite this packet. After transmitting the first 64 bytes, it transmits the rest of the packet and appends the CRC to the end. FIFO under-run or more than 16 collisions will cause the state machine to abort the packet (no retry) and prepare for the next packet in the queue.

In case of any transmission errors, the MAC transmit block sets the appropriate error bit in the TPSR and sends a bad TX signal to the interrupt controller.

6.10.7 Receiving a Frame

To receive a frame, the receive enable bit in the MCR must be set and the receive halt bit must be clear. The MAC receive block, when enabled, constantly monitors a data stream coming from the integrated PHY. If the MAC is in loop back mode, the data stream will be going to the MAC transmit block via internal connections.

The MAC receive block receives zero to seven bytes of preamble, followed by the Start Frame Delimiter (SFD). The MAC receive block checks that the first data received is preamble and looks for the SFD in the first eight bytes. If the SFD is not the first non-preamble byte, it treats the packet as a fragment and discards it. When it has received a full byte, the MAC receive block stores the byte and several status bits in the MAC receive FIFO which then signals that data is present. It receives subsequent bytes and stores them and their status in the FIFO. If, during the frame reception, the receive FIFO overflows, or the PHY asserts mii_rx_er, or the frame ends on an odd nibble, the MAC receive block sets the corresponding status bit for the byte in the FIFO.

The QUE receive controller reads bytes from the MAC receive FIFO, combines them into four-byte words, checks the CRC, optionally drops the padding and/or CRC field and moves the data into the receive QUE. The QUE receive controller will never take bytes from the FIFO on two consecutive clocks. The status bits from the receive FIFO are held by the QUE receive controller for the receive status FIFO until the EOF status bit from the FIFO is true, at which time the final status is added to the status FIFO and the held status bits are all cleared in preparation for the next frame. The QUE receive controller will signal the receive producer to drop a frame if there is no room in the status FIFO when the frame arrives. This makes sure that there is a one-to-one relation between frames in the QUE and status words in the status FIFO.

6.10.8 Strip Padding/FCS

The strip-padding feature will remove any padding from 64-byte frames. The strip-padding feature will also remove excess padding from frames up to 127 bytes in total length. Frames that are 128 bytes or larger will never have any padding stripped. Padded frames that have their padding removed by the strip-padding feature will also have their FCS field removed, even if the strip CRC feature is not enabled. If the strip-padding feature is enabled but the strip CRC feature is not, then frames received that have no padding removed will still have their FCS field, but frames that have padding removed will not. The CRC is always checked even if it is removed by the strip padding feature and not the strip CRC feature. The strip CRC feature will always remove the FCS field from all received frames.

The packet classification block snoops data bytes as they are popped from the receive FIFO by the QUE receive controller. If the classifier determines that a frame is to be dropped, the frame error bit to the receive producer is set and, assuming the first BLOCK of the frame has not been added, the frame is dumped before it is appended to the QUE. If the classification block determines that a frame is to be dropped after one or more BLOCKs have been added to the QUE then the frame is truncated at that point and the remainder of the frame is dropped.

6.11 MAC Error Reporting

Errors reported by the MAC are communicated back to the host on a frame-by-frame basis through the Transmit Status FIFO and Receive Status FIFO.

6.11.1 MAC Transmit Errors

6.11.1.1 Transmit FIFO Underrun Error

The 80-byte MAC transmit FIFO is capable of handling a worst-case QUE latency of 1.28 µs (128 bit times, or 16 byte times) because 64 bytes are retained for possible retransmission after a collision. The QUE transmit controller has higher bandwidth than the 100 Mb PHY such that a MAC transmit FIFO under-run usually indicates a host bus latency problem. See Section 6.3.2.2 for a discussion on how to mitigate this situation.

In the event that the transmit FIFO does under-run, the MAC aborts the transmission, sets the Underrun bit in the transmit status and discards the remainder of the frame when it finally does arrive.

6.11.1.2 Lost Carrier Error

In half duplex mode, Carrier Sense (CRS) is monitored from the beginning of the Start Frame Delimiter (SFD) to the last byte transmitted. A lost carrier condition indicates that CRS was never present or was dropped during transmission (a possible network problem), but transmission is not aborted. Lost carrier error is disabled during loop back mode. During full duplex operation, CRS is not passed to the transmit block and lost carrier will not be asserted. Lost carrier sets the Carrier bit in the *Transmit Packet Status Register* (TPSR).

6.11.1.3 Excessive Collision Error

In half duplex mode, whenever the MAC encounters a collision during transmit, it will back off, update the collision counter and try again later. When the counter equals 16 (16 attempts all resulted in a collision) transmission is aborted. Excessive collisions probably indicate a network problem. Excessive collision sets the Excessive Collision bit in the *Transmit Packet Status Register* (TPSR).

6.11.1.4 Late Collision Error (Transmit Out-Of-Window Collision)

In a correctly configured and operating network, the controller sees a collision (if there is one) within the first 64 bytes of data being transmitted. If a collision occurs after this time a possible network problem is detected. Late collision sets the Late Collision bit in the *Transmit Packet Status Register* (TPSR) and transmission of the packet is aborted, i.e. late collisions are not retried.

6.11.1.5 Signal Quality Error

In 10 Mbps mode, the MAC checks for a “heartbeat” at the end of a transmitted packet. This is a short Collision signal within the first 40 bit times after end of transmission. Signal Quality Error sets the No Heart Beat bit in the *Transmit Packet Status Register (TPSR)*.

6.11.1.6 Deferral

In half duplex mode, during any attempt to send a packet, the MAC may have to defer the transmission because of a pre-occupied network. This is not an error, but is used as a network activity indicator, but only when collisions do not occur. Deferral sets the Deferral bit of the *Transmit Packet Status Register (TPSR)*.

6.11.1.7 Excessive Deferral

In half duplex operation, the MAC will defer transmission of frames when there is network activity. If the deferral time is longer than two maximum sized frame times (2.4288 ms for 10-Mbps operation or 0.24288 ms for 100-Mbps operation) then the Excessive Deferral bit of the *Transmit Packet Status Register (TPSR)* is set. If the Tx Enable bit of the *MCR Register (MCR)* is clear, then the transmission is aborted. Excessive deferral indicates a possible network problem.

6.11.2 MAC Receive Errors

6.11.2.1 Alignment Error

At the end of reception, the MAC receive block checks that the incoming packet has been correctly framed on an 8-bit boundary. If it is not and the CRC is invalid, data has been disrupted through the network and the MAC receive block reports an alignment error. A CRC error is also reported. The Dangling Byte bit and the CRC bit are set in the *Receive Packet Status Register* (RPSR).

6.11.2.2 CRC Error

At the end of reception, the MAC receive block checks the CRC for validity and reports a CRC error if it is invalid.

6.11.2.3 Overflow Error

During reception, incoming data is put into the MAC receive FIFO before it is transferred to the QUE receive controller. If the MAC receive FIFO fills up because of excessive system latency or other reasons, the MAC receive block sets the Overflow Error of the *Receive Packet Status Register* (RPSR) and the remaining frame is dropped.

6.11.2.4 Length Error

The MAC receive block checks the length of the incoming packet at the end of reception based on the value of the Len/Type field of the frame. If the length is specified in the Len/Type field and the frame is longer than the maximum frame size of 1518 bytes, (1522 for VLAN tagged packets), the MAC receive block reports a length error, unless long frame mode is enabled. The MAC will also flag as an error a MAC control frame that is not exactly 64 bytes in length.

6.11.2.5 MII Error

The PHY informs the MAC if it detects a media error (such as coding violation) by asserting RX_ER. When the PHY asserts RX_ER, the MAC sets the MII error bit in the *Receive Packet Status Register* (RPSR).

6.12 PHY Operations

6.12.1 Automatic MDI/MDIX Cable Crossover Configuration

The transmitter and receiver contain logic and mux to detect and correct for cross over cabling errors. The implementation is fully compliant with IEEE 802.3 specifications, ensuring interoperation with other PHYs, which may or may not implement automatic MDI/MDI-X configuration. The automatic MDI/MDI-X state machine facilitates switching TXN and TXP pins with the RXN and RXP pins, prior to the auto-negotiation mode of operation. The correct polarization of the crossover circuit is determined by an algorithm that controls the switching function. Use of an 11-bit *Linear Feedback Shift Register* (LFSR) creates a pseudo-random sequence to determine the MDI configuration. Upon making the selection to either MDI or MDI-X, the 78Q8430 waits for a specified amount of time while evaluating its receive channel to determine whether the other end of the link is sending link pulses or 10BASE-T or 100BASE-TX data. If link pulses or data are detected, the 78Q8430 remains in that configuration. If link pulses or data are not detected, it increments it's LFSR and makes a decision to switch based on the value of the next bit. The state machine does not move from one state to another while link pulses are being transmitted.

6.12.2 100Base-TX Transmit

The 78Q8430 PHY contains all of the necessary circuitry to convert the transmit MII signaling from a MAC to an IEEE-802.3 compliant data-stream driving Cat-5 UTP cabling. The internal PCS interface maps 4-bit nibbles from the MII to 5-bit code groups as defined in Table 24-1 of IEEE-802.3. The 5-bit code groups are then scrambled and converted to a serial stream before being sent to the MLT-3 pulse shaping circuitry and line driver. The pulse-shaper uses current modulation to produce the desired output waveform. Controlled rise/fall time in the MLT-3 signal is achieved using an accurately controlled voltage ramp generator. The line driver requires an external 1:1 isolation transformer to interface with the line media. The center-tap of the primary side of the transformer connects to the 3.3 V supply.

6.12.3 100Base-TX Receive

The 78Q8430 PHY receives a 125 MBaud MLT-3 signal through a 1:1 transformer. The signal then goes through a combination of adaptive offset adjustment (baseline wander correction) and adaptive equalization. The effect of these circuits is to sense the amount of dispersion and attenuation caused by the cable and transformer and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The 78Q8430 PHY can compensate for cable loss of up to 10dB at 16 MHz. This loss is represented as test_chan_5 in Annex A of the ANSI X3.263:1995 specification and corresponds to approximately 140 m of CAT-5 UTP cabling. The equalized MLT-3 data signal is bi-directionally sliced and the resulting bit-stream is presented to the CDR where it is re-timed and decoded to NRZ format. The retimed serial data is converted to parallel, then de-scrambled and aligned into 5 bit code groups. The receive PCS interface maps these code groups to 4 bit data for the internal MII as outlined in Clause 24 of IEEE-802.3.

6.12.4 10Base-T Transmit

The 78Q8430 PHY takes 4-bit parallel NRZ data via the MII interface and passes it through a parallel to serial converter. The data is then passed through a Manchester encoder, pre-emphasis pulse-shaper, media filter and finally to the twisted-pair line driver. The pulse shaper and filter ensures the output waveforms meet the output voltage template and spectral content requirements detailed in Clause 14 of IEEE-802.3. Interface to the twisted pair media is through a center-tapped 1:1 transformer. No external filtering is required. During auto-negotiation and 10BASE-T idle periods, link pulses are transmitted. The 78Q8430 PHY employs an on board timer to prevent the MAC from capturing a network through excessively long transmissions. When this timer is exceeded the chip enters the jabber state and transmission is disabled. The jabber state is exited after the MII goes idle for 500 ms ± 250 ms.

6.12.5 10Base-T Receive

The 78Q8430 PHY receives Manchester encoded 10BASE-T data through the twisted pair inputs and re-establishes logic levels through a slicer with a smart squelch function. The slicer automatically adjusts its level after valid data with the appropriate levels are detected. Data is passed on to the CDR where the clock is recovered and data is re-timed and passed through a Manchester decoder. From here, data enter the serial to parallel converter for transmission to the MAC via the media independent interface. Interface to the twisted pair media is through a 1:1 transformer. Polarity information is detected and corrected in internal circuitry.

6.12.6 SQE Test

The 78Q8430 PHY supports the signal quality error (SQE) function detailed in IEEE-802.3. At an interval of 1µs after each negative transition of the TXEN pin in 10BASE-T mode, the COL pin will go high for a period of 1µs. SQE is not signaled if a collision is detected during transmission. This function can be disabled through register bit MR16.11.

6.12.7 Polarity Correction

The 78Q8430 PHY is capable of either automatic or manual polarity reversal for 10BASE-T and auto-negotiation. These features are controlled by the PHY management register MR16, bits APOL and RVSPOL. The default is automatic mode, where APOL is negated and RVSPOL indicates if the detection circuitry has inverted the input signal. To enter manual mode, APOL needs to be asserted and then RVSPOL will control the signal polarity.

6.12.8 Natural Loopback

The natural loop back function can be enabled by setting register bit MR16.10. With natural loop back enabled, whenever the 78Q8430 PHY is transmitting and not receiving on the twisted pair media (10BASE-T Half Duplex mode), data on the TXD pins is looped back onto the RXD pins. During a collision, data from the RXI pins is routed to the RXD pins.

6.12.9 Auto-Negotiation

The 78Q8430 PHY supports the auto-negotiation functions of Clause 28 of IEEE-802.3. This function can be controlled via register settings. The auto-negotiation function defaults to on and bit MR0[12], ANEGEN, is high after reset. Software can disable the auto-negotiation function by writing to bit MR0[12].

The contents of register MR4 are sent to the PHY's link partner during auto-negotiation, coded in fast link pulses. Bits MR4.8:5 reflect the state of the TECH[2:0] bits after reset. If TECH[2:0] = 111b, then all 4 bits are high. If TECH[2:0] = 001b, then only bit 5 is high. After reset, software can change any of these bits from a 1 to a 0.

With auto-negotiation enabled, the 78Q8430 PHY will start sending fast link pulses at power on, loss of link or a command to restart. At the same time, it will look for either 10BASE-T idle, 100BASE-TX idle or fast link pulses from its link partner. If either idle pattern is detected, the 78Q8430 PHY configures itself in half- duplex mode at the appropriate speed. If it detects fast link pulses, it decodes and analyzes the link code transmitted by the link partner. When three identical link code words are received (ignoring the acknowledge bit), the link code word is stored in register 5. Upon receiving three more identical link code words, with the acknowledge bit set, the 78Q8430 PHY configures itself to the highest priority technology common to the two link partners. The technology priorities are, in descending order:

- 100BASE-TX, Full Duplex.
- 100BASE-TX, Half Duplex.
- 10BASE-T, Full Duplex.
- 10BASE-T, Half Duplex.

Once auto-negotiation is complete, register bits MR18[11:10] will reflect the actual speed and duplex that was chosen. If auto-negotiation fails to establish a link for any reason, register bit MR18[12] will reflect this and auto negotiation will restart from the beginning. Writing a one to bit MR0[9], RANEG, will also cause auto negotiation to restart.

6.12.10 LED Indicators

Two LED pins can be used to indicate various states of operation of the 78Q8430 PHY. The default configuration uses LED0 to indicate the link is up and LED1 to indicate either RX or TX activity. LED0 and LED1 may be redefined via MR23. There is no direct hardware for controlling the MAC from the PHY LED status, therefore software drivers must obtain the DUPLEX and SPEED parameters from the PHY register MR18[11:10] and configure the MAC accordingly.

6.12.11 PHY Interrupts

The 78Q8430 PHY has an Interrupt signal that is asserted whenever any of the eight interrupt bits of MR17[7:0] are set. The PHY bit in the *Host Interrupt Register* (HIR) is set to indicate and interrupt from the PHY. Individual PHY interrupt conditions can be enabled via MR17, bits 15:8, the PHY Interrupt Enable bits. PHY interrupt bits are cleared when MR17 is read.

6.12.12 Internal Clock PLL

When the internal clock mode is selected by the CLKMODE pin, the 100 MHz system clock is provided by a PLL inside the PHY. This PLL multiplies the frequency of the 25 MHz PLL crystal oscillator up to the 100 MHz needed to run the system clock.

When the PHY is powered down, the PLL used to generate the internal system clock is also powered down and ceases to function. For this reason, the internal PHY should never be powered down when the internal system clock is selected by the CLKMODE pin.

There is no external visibility for the system clock when the internal clock mode is selected. The GBI interface must therefore always be used in asynchronous bus mode when the internal clock mode is used.

7 Register Descriptions

7.1 Register Overview

The 78Q8430 has 10 address bits for a total address space of 1024 bytes. This address space is divided into four 256-location blocks: QUE, CTL, Reserved and SNOOP.

The QUE section contains registers used to control transmit and receive queues. Each queue is allocated eight 32-bit registers for a maximum of eight queues supported.

The CTL section contains control registers used to control the behavior of 78Q8430.

A block of 256 addresses is reserved for future use.

The SNOOP section is mapped to cache memory via the *Snoop Control Register.*

Address Range	Group
0x000 … 0x0FF	QUE
0x100 … 0x1FF	CTL
0x200 … 0x2FF	Reserved
0x300 … 0x3FF	SNOOP

7.2 QUE Register Overview

Address Range	QUE #	Symbol	Name
0x000-0x01C	QUE 0		
	0x00	PCWR	Packet Control Word Register
	0x04	PSZR	Packet Size Register
	0x08	STDR	Setup Transmit Data Register
	0x0C	TDR	Transmit Data Register
	0x10	RDR	Receive Data Register
	0x14	Reserved	
	0x18	QFLR	QUE First/Last pointers.
	0x1C	QSR	QUE Status Register
0x020-0x03F	QUE 1		
	…		QUE 1 Registers
0x040-0x05F	QUE 2		
	…		QUE 2 Registers
0x060-0x07F	QUE 3		
	…		QUE 3 Registers
0x080-0x09F	QUE 4		
	…		QUE 4 Registers
0x0A0-0x0BF	QUE 5		
	…		QUE 5 Registers
0x0C0-0x0DF	QUE 6		
	…		QUE 6 Registers
0x0E0-0x0FF	QUE 7		
	…		QUE 7 Registers

7.3 CTL Register Overview

Address	Symbol	Page	Name
0x100	DMA	59	DMA Slave Mode Control and Status
0x104	RPSR	59	Receive Packet Status FIFO
0x108	TPSR	59	Transmit Packet Status FIFO
0x10C	TPROS	60	Transmit Producer Status
0x110	RPROS	60	Receive Producer Status
0x114	Reserved		
0x118	GBI_ID	61	Part ID Register
0x11C	GBI_CS	61	Configuration Register
0x120	Reserved		
0x124	Reserved		
0x128	RTTR	61	Receive to Transmit Transfer Register
0x12C	FDR	61	Frame Disposition Register
0x130	RFBSR	61	Receive FIRST BLOCK Status Register
0x134	RDSR	62	Receive Data Status Register
0x138	BCR	62	BIST Control Register
0x13C	BBDR	63	BIST Bypass Mode Data Register
0x140	MDDAR	63	Station Management Data Register
0x144	MDCAR	63	Station Management Control and Address Register
0x148	PRDR	63	PROM Data
0x14C	PRCR	64	PROM Control
0x150	Reserved		
0x154	MCR	64	MAC Control Register
0x158	Reserved		
0x15C	Reserved		
0x160	Reserved		
0x164	CDR	65	Count Data Register
0x168	CCR	65	Count Control Register
0x16C	CMR	66	Count Management Register
0x170	SNCR	66	Snoop Control Register
0x174 - 0x17C	Reserved		
0x180	IDCR	66	Interrupt Delay Count Register
0x184	PDCR	66	Pause Delay Count Register
0x188	HNRCR	67	Host Not Responding Count Register
0x18C	WUSR	67	Wake Up Status Register
0x190	WMVR	67	Water Mark Values Register
0x194	Reserved		
0x198	PMCAP	67	Power Management Capabilities
0x19C	PMCSR	68	Power Management Control and Status
0x1A0	CAR	68	Address of CAM rule being accessed
0x1A4	RMR	69	Rule Match Register
0x1A8	RCR	69	Rule Control Register
0x1AC	Reserved		

Address	Symbol	Page	Name
0x1B0	Reserved		
0x1B4	Reserved		
0x1B8	Reserved		
0x1BC	Reserved		
0x1C0	QSIR	70	QUE Status Interrupt Register
0x1C4	QSMR	70	QUE Status Mask Register
0x1C8	OUIR	71	Overflow/Underrun Interrupt Register
0x1CC	OUMR	71	Overflow/Underrun Mask Register
0x1D0	TRIR	71	Transmit RMON Interrupt Register
0x1D4	TRMR	72	Transmit RMON Mask Register
0x1D8	RRIR	72	Receive RMON Interrupt Register
0x1DC	RRMR	72	Receive RMON Mask Register
0x1E0	Reserved		
0x1E4	Reserved		
0x1E8	HIR	72	Host Interrupt Register
0x1EC	HIMR	73	Host Interrupt Mask Register
0x1F0	Reserved		
0x1F4	Reserved		
0x1F8	Reserved		
0x1FC	Reserved		

7.4 Snoop Address Space Overview

0x300-0x3FF	SNOOP	Accessing data in this address space will be mapped to the contents of the buffer memory BLOCK indicated by the SNCR.

7.5 QUE Registers

7.5.1 Packet Control Word Register

Name: **PCWR** Reset Val: **0x0000_0000** Block: **QUE** Address: **0x000**

Bits	Type	Default	Description
31:30	X		Reserved
29:25	WO	N/A	**Preload** The number of bytes to pre-load into the MAC TX FIFO before the frame begins transmission to the PHY. This may need to be non-zero for large IP headers that want to have the checksum inserted to ensure the checksum is not transmitted before the end of the header is loaded.
24:16	WO	N/A	**Packet ID** The 9-bit ID value used to identify this packet in the TX status FIFO.
15:10	WO	N/A	**IP Header Offset** Offset in bytes to the IP header in this frame. If this value is non-zero then the IP header checksum will be corrected.
9	WO	N/A	**Append CRC** When set, the transmitter shall append the correct CRC checksum to the end of the frame.
8	WO	N/A	**Fix CRC** When set, the transmitter shall correct the existing CRC checksum on the end of the packet.
7	X		Reserved
6	WO	N/A	**Disable Padding** For small packets (<64 Bytes).
5	WO	N/A	**Late Notify** Interrupt on completion.
4	WO	N/A	**Early Notify** Interrupt at beginning of transmission.
3	WO	N/A	Interrupt on excessive collisions.
2	WO	N/A	Disable deferral timeout.
1	WO	N/A	Enable fast back-off timer.
0	X		Reserved

7.5.2 Packet Size Register

Name: **PSZR** Reset Val: **0x0000_0000** Block: **QUE** Address: **0x004**

Bits	Type	Default	Description
31:16	X		Reserved
15:0	RW	0000	**Packet Size** The size, in bytes, of the packet that will be added to the QUE.

7.5.3 Setup Transmit Data Register

Name: **STDR** Reset Val: **0x0000_0000** Block: **QUE** Address: **0x008**

Bits	Type	Default	Description
31:25	X		Reserved
24	RW		**Endian** The network transmit byte order. Set = big endian (Most significant byte transmit first) Clear = little endian (Least significant byte transmit first)
23:20	X		Reserved
19:18	RW	00	**Start Offset** The number of bytes to ignore on the first data word written for this buffer. This byte mask is applied any time the Count value is non-zero. After each time it is applied, however, it is reset to zero such that it is really only applied on the first write.
17:16	RW	00	**End Offset** The number of bytes to ignore on the last data word written for this buffer. This byte mask is applied any time the Count value is zero. Unlike the Start Offset, the End Offset is not self clearing. This means that the End Offset will be applied to all writes to the QUE once the Count value reaches zero, unless the host clears the End Offset. The remainder of PSZR will override the End Offset when a write occurs and the PSZR value is less than four.
15:14	X		Reserved
13:0	RW	0000	**Count** The total number of writes needed to complete the buffer minus one. This counter decrements on each write operation to the QUE. This counter decrements on each write operation to the QUE until it reaches zero. The Count value will remain zero until the next host write. The value written here must be one less than the number of writes in the buffer so that the Count value will equal zero on the last write and cause the End Offset to be applied.

Note: The PCWR and PSZR must be set before writing to the STDR.

7.5.4 Transmit Data Register

Name: **TDR** Reset Val: **0x0000_0000** Block: **QUE** Address: **0x00C**

Bits	Type	Default	Description
31:0	WO	N/A	**Packet Data to Add to the QUE** Data written to this register is added to the QUE to which the register belongs.

7.5.5 Receive Data Register

Name: **RDR** Reset Val: **0x0000_0000** Block: **QUE** Address: **0x010**

Bits	Type	Default	Description
1:0	RO	N/A	**Packet Data Read from the QUE** Data read from this register is shifted out of the QUE to which the register belongs. The RPSR should be consulted to make sure data is available before reading this register.

7.5.6 QUE First/Last Register

Name: **QFLR** Reset Val: **0x0000_0000** Block: **QUE** Address: **0x018**

Bits	Type	Default	Description
31:23	X		Reserved
22:16	RW	0x00	**Last** The value of the Last pointer for this QUE.
15:7	X		Reserved
6:0	RW	0x00	**First** The value of the First pointer for this QUE.

Note: The default values will vary for static QUEs 2 and 5.

7.5.7 QUE Status Register

Name: **QSR** Reset Val: **0x0000_0000** Block: **QUE** Address: **0x01C**

Bits	Type	Default	Description
31	RW	0	**QDR** QUE data is ready.
30	RW	0	**Pause Mask** When set, pause mode has no effect on the QDR bit for this QUE. The default behavior when clear is to disallow the setting of the QDR bit in pause mode.
29:26	X		Reserved
25:24	RW	00	**Mode** The current QSR value for the QDR mode. 00 = QDR set when First is not 0 01 = QDR set when above is set. 10 = QDR set when LEOP is not zero. 11 = QDR set when above is set or LEOP is not 0.
23:19	X		Reserved
18	RO	0	**EOP** The QUE contains at least one EOP.
17	RO	0	**Above** The Count value is above the threshold.
16	RO	0	**Below** The Count value is below the threshold.
15	X		Reserved
14:8	RW	0x00	**Threshold** The number to compare to Count to determine the above and below bits.
7	X		Reserved
6:0	RO	0x00	**Count** The total number of BLOCKs assigned to this QUE.

Note: Only bits 31 and 30 are valid for static QUEs 2 and 5.

7.6 CTL Registers

7.6.1 DMA Control and Status Register

Name: **DMA** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x100**

Bits	Type	Default	Description
31:18	X	0	Reserved
17	RW	0	**Read Mode** Once this bit is set the host interface will be in DMA read mode until the bit is cleared by a write to this register.
16	RW	0	**Write Mode** Once this bit is set the host interface will be in DMA write mode until the bit is cleared by a read to this register.
15:10	X	0	Reserved
9:0	RW	0	**Address** The location of the register to direct DMA access to.

7.6.2 Receive Packet Status Register

Name: **RPSR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x104**

Bits	Type	Default	Description
31	RO	0	**Done** When not set the packet is still in the process of ingressing the QUE.
30	RO	0	**Length Error** The packet length was not correct.
29	RO	0	**Truncated** The packet was truncated and is incomplete.
28	RO	0	**Collision** The packet suffered a collision and is incomplete.
27	RO	0	**MII Error**
26	RO	0	**Dangling Byte** The received packet length was not an integer number of bytes.
25	RO	0	**CRC** Ethernet CRC checksum error.
24	RO	0	**Checksum** IP Header checksum error.
23:16	RO	0	**Classification** The packet classification results.
15:0	RO	0	**Count** The total number of bytes currently in the QUE for this packet. When the Done bit is set, this represents the actual packet size.

7.6.3 Transmit Packet Status Register

Name: **TPSR** Reset Val: **0x0E00_0000** Block: **CTL** Address: **0x108**

Bits	Type	Default	Description
31	RO	0	**Done** When not set, the frame is still in transmission. When set, the content is egressing the QUE.
30	RO	0	**Halted** The packet was halted.
29	RO	0	**Truncated** The packet was truncated and is incomplete.

Name: **TPSR** Reset Val: **0x0E00_0000** Block: **CTL** Address: **0x108**

Bits	Type	Default	Description
28	RO	0	**Carrier** Loss of carrier during transmission.
27:25	RO	7	**QUE** The number of the QUE that was the source for this packet.
24:16	RO	0	**Packet ID** The packet ID that was assigned to this packet by the PCWR when it was loaded into the QUE.
15:13	X		Reserved
12	RO	0	**No Heart Beat** No heartbeat was detected at the end of transmission.
11	RO	0	**Excessive Deferrals**
10	RO	0	**Deferred**
9	RO	0	**Late Collision**
8	RO	0	**Excessive Collisions**
7:4	X		Reserved
3:0	RO	0	**Collision Count** The number of collisions experienced by this packet.

Note: When the Done bit is not set, the Collision Count field may not be correct. In this case, a non-zero value does indicate that the frame currently being transmitted has experienced at least one collision, but the actual count value may not be correct until the Done bit is set.

7.6.4 Transmit Producer Status

Name: **TPROS** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x10C**

Bits	Type	Default	Description
31:8	X		Reserved
7	RO	0	**QUE7:** QUE is dropping a packet.
6	RO	0	**QUE6:** QUE is dropping a packet.
5	RO	0	**QUE5:** QUE is dropping a packet.
4	RO	0	**QUE4:** QUE is dropping a packet.
3	RO	0	**QUE3:** QUE is dropping a packet.
2	RO	0	**QUE2:** QUE is dropping a packet.
1	RO	0	**QUE1:** QUE is dropping a packet.
0	RO	0	**QUE0:** QUE is dropping a packet.

7.6.5 Receive Producer Status

Name: **RPROS** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x110**

Bits	Type	Default	Description
31:8	X		Reserved
7	RO	0	**QUE7:** QUE is dropping a packet.
6	RO	0	**QUE6:** QUE is dropping a packet.
5	RO	0	**QUE5:** QUE is dropping a packet.
4	RO	0	**QUE4:** QUE is dropping a packet.
3	RO	0	**QUE3:** QUE is dropping a packet.
2	RO	0	**QUE2:** QUE is dropping a packet.
1	RO	0	**QUE1:** QUE is dropping a packet.
0	RO	0	**QUE0:** QUE is dropping a packet.

7.6.6 Revision ID

Name: **ID** Reset Val: **0x8430_0102** Block: **CTL** Address: **0x118**

Bits	Type	Default	Description
31:16	RO	8430	**Prod ID** Indicates the product number.
15:8	RO	2	**Ver ID** Indicates the product version number.
7:0	RO	1	**Rev ID** Indicates the silicon revision number.

7.6.7 Configuration

Name: **GBI_CS** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x11C**

Bits	Type	Default	Description
31:5	X		Reserved
4:0	RO	0	**CONF** The current status of the configuration pins.

7.6.8 Receive to Transmit Transfer Register

Name: **RTTR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x128**

Bits	Type	Default	Description
31:1	X		Reserved
0	RW	0	**Transfer** Writing a one to this bit signals the QUE logic to transfer the QUE0 FIRST BLOCK to QUE3. The QUE logic clears the bit when the operation is complete.

7.6.9 Frame Disposition Register

Name: **FDR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x12C**

Bits	Type	Default	Description
31:1			Reserved
0	W		**Drop Rx Frame** Writing a 1 to this bit causes the Rx consumer to drop the current frame entirely from the QUE.

7.6.10 Receive FIRST BLOCK Status Register

Name: **RFBSR** Reset Val: **0x0002_0000** Block: **CTL** Address: **0x130**

Bits	Type	Default	Description
31:18			Reserved
17	R	1	**EOF** The FIRST BLOCK is the end of its frame.
16	R	0	**ERR** The FIRST BLOCK is the end of a truncated frame.
15			Reserved
14:8	R	00	**Next** The BLOCK that is next in QUE0 after the current FIRST BLOCK.
7:0	R	00	**Used** The number of valid bytes in the FIRST BLOCK for QUE0.

7.6.11 Receive Data Status Register

Name: **RDSR** Reset Val: **0x0001_0000** Block: **CTL** Address: **0x134**

Bits	Type	Default	Description
31:25			Reserved
24	R	0	**EOF** When set this bit indicates that the next data word read from QUE0 will be the end of its frame.
23:17			Reserved
16	R	1	**QUE0 Empty** When set this bit indicates that QUE0 contains no data.
15:2			Reserved
1:0	R	00b	**QUE0 Data Size** The number of valid bytes in the next data word read from QUE0.

7.6.12 BIST Control Register

Name: **BCR** Reset Val: **0x2010_0000** Block: **CTL** Address: **0x138**

Bits	Type	Default	Description
31	W		**BIST Start** Writing a 1 to this bit triggers the selected BIST test (see BIST Mode below).
30	R	0	**Fail** The BIST operation failed.
29	R	1	**Pass** The BIST operation passed.
28:21			Reserved
20	R/W	1	**Auto Increment** When set, the RAM Address field will auto-increment after each RAM access.
19	R/W		**BIST Enable** Enable BIST mode operation.
18:16	R/W	000	**BIST Mode** Set the BIST test mode: 000b – Reserved. 001b – PATTERN. 010b – FILL 0. 011b – READ 0. 100b – FILL 1. 101b – READ 1. 110b – BYPASS. 111b – Reserved.
15:14			Reserved
13:0	R/W	0x000	**RAM Address** Set the address of the RAM that is accessed via BBDR in BYPASS mode.

7.6.13 BIST Bypass Mode Data Register

Name: **BBDR** Reset Val: **N/A** Block: **CTL** Address: **0x13C**

Bits	Type	Default	Description
31:0	R/W		**RAM Data** Reads and writes to these bits go directly to the QMEM RAM at the location indicated by BCR only when the BIST mode is set to BYPASS.

7.6.14 Station Management Data Register

Name: **MDDAR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x140**

Bits	Type	Default	Description
31:16	X	0000	Reserved
15:0	RW	0	**SMI Data** Data read from or data to be written to the PHY. See Section 7.7.

7.6.15 Station Management Control and Address Register

Name: **MDCAR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x144**

Bits	Type	Default	Description
31:13	X	0000	Reserved
12	RW	0	**Preamble** Writing a 1 suppresses the generation of the 32-bit PHY station management preamble before the PHY register transfer. The internal PHY of the 8430 does not require the preamble.
11	RW	0	**Busy** Writing a 1 initiates the PHY register transfer. The hardware will clear the bit when the operation completes.
10	RW	0	**RegWr** Writing a 1 indicated the MDDAR data is to be written to the PHY. Writing a 0 causes the PHY register to be read and the data placed in the MDDAR .
9:5	RW	0	**PHY Addr** Address of the PHY to access.
4:0	RW	0	**PHY Reg** Address of the PHY register to access.

7.6.16 PROM Data Register

Name: **PRDR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x148**

Bits	Type	Default	Description
31:16	X	0000	Reserved
15:0	RW	0000	**PROM Data** Data to write to or read from the EEPROM device.

7.6.17 PROM Control Register

Name: **PRCR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x14C**

Bits	Type	Default	Description
31:9	X	0000	Reserved
8	RW	0	**Busy** Writing a 1 initiates the EEPROM data transfer. The hardware will clear the bit when the operation completes.
7:6	RW	0x0	**Operation** 1 1 = Erase. 1 0 = Read. 0 1 = Write. 0 0 = Enable or Disable Writing, as specified in PROM Addr: [5:4] = 11, Enable [5:4] = 00, Disable
5:0	RW	0x00	**PROM Addr** Address of the EEPROM to access.

7.6.18 MAC Control Register

Name: **MCR** Reset Val: **0x0080_0050** Block: **CTL** Address: **0x154**

Bits	Type	Default	Description
31:28	X	0000	Reserved
27	RW	0	**Tx Enable** When this bit is clear transmitting stops immediately.
26	RW	0	**Tx Halt** When this bit is set transmitting stops at the end of the current frame.
25	RW	0	**Rx Enable** When this bit is clear receiving stops immediately.
24	RW	0	**Rx Halt** When this bit is set receiving stops at the end of the current frame.
23	RW	1	**Rx Drop Error** When this bit is set then an error in the first 256 bytes will cause a packet to be dropped. If clear, error packets are forwarded to the host.
22	RW	0	**Keep Dropped Status** Normally, the status for a dropped frame is not added to the receive status FIFO. When this bit is set then a status for all frames, including dropped frames, is added to the receive status FIFO. The status for a dropped frame will have a size of zero in the RPSR.
21	RW	0	**Jumbo OK** Normally frames in excess of the maximum allowed by 802.3 are flagged as bad. If this bit is set then larger frame sizes are allowed.
20:18		0000	Reserved
17	RW	0	**MACRST** Software re-initialization. Setting this bit will also automatically set both Rx and Tx Halt bits and clear both Rx and Tx Enable bits. This bit is only cleared by writing a zero.
16	RW	0	**MACLOOP** Loopback mode for the MAC.
15:8	X	0x000	Reserved
7	RW	0	**No Rx PAD** Strip the padding bytes from the end of received frames that are 64 bytes in length. When the padding is stripped from a frame the CRC is stripped as well.

6	RW	1	**FullDup** 1 = Full Duplex 0 = Half Duplex The default setting for the MAC is full duplex mode. This bit needs to be updated each time there is a link status change in the PHY.
5	RW	0	**SQE** Enable SQE checking.
4	RW	1	**No Ex Diff** Disable checking for excessive deferrals.
3	X	0	Reserved
2	X	0	Reserved
1	RW	0	**No Rx CRC** When this bit is set, the MAC receiver will strip the CRC bytes from the end of received frames after the CRC check is complete.
0	RW	0	**No CRC Chk** When this bit is set, CRC checking is disabled. This bit should never be set when the No Rx CRC bit is set as there will be no way to verify the CRC.

7.6.19 Count Data Register

Name: **CDR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x164**

Bits	Type	Default	Description
31:0	RW		**Count** Value of the counter indicated by CCR.

7.6.20 Counter Control Register

Name: **CCR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x168**

Bits	Type	Default	Description
31:11	X		Reserved
10	RW		**Auto Increment** When this bit is set, the address of the counter being accessed is automatically incremented after each access to the CDR.
9	RW		**Clear on Read** When this bit is set, the counter being read is automatically cleared to zero after each access to the CDR.
8	RW		**Access Mode** When this bit is clear, the CDR is in read mode. When set, the CDR is in write mode.
7:6	X		Reserved
5:0	RW		**Address** Address of the counter to access. (00 to 0E, Transmit Counters; 0F to 25, Receive Counters)

7.6.21 Counter Management Register

Name: **CMR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x16C**

Bits	Type	Default	Description
31:3	X		Reserved
2	RW		**Freeze** When this bit is set, the values of the counters are frozen until the bit is cleared. Countable events that occur while this bit is set are stored in a FIFO and processed after the bit is cleared such that no counts are lost. If the FIFO fills before the Freeze bit is cleared then the bit is automatically cleared and the counters updated.
1	W		**Clear Receive** When a 1 is written to this bit then all receive counters are automatically cleared.
0	W		**Clear Transmit** When a 1 is written to this bit than all transmit counters are automatically cleared.

7.6.22 Snoop Control Register

Name: **SNCR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x170**

Bits	Type	Default	Description
31:7	X		Reserved
6:0	RW	0x00	**BLOCK** Pointer to the BLOCK that is accessed directly via the SNOOP register space.

7.6.23 Interrupt Delay Count Register

Name: **IDCR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x180**

Bits	Type	Default	Description
31:24	X		Reserved
23:0	RW		**IDC** How long to delay the data received interrupt, measured in byte times.

7.6.24 Pause Delay Count Register

Name: **PDCR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x184**

Bits	Type	Default	Description
31:17	X		Reserved
16	WO		**Start** Start local pause. Writing a one to this bit triggers a local pause condition immediately.
15:0	RW		**Pause** How long to halt transmit QUEs for a local pause condition, measured in delay quanta of 512 Rx bit times.

7.6.25 Host Not Responding Count Register

Name: **HNRCR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x188**

Bits	Type	Default	Description
31:0	RW		**Count** Number of system cycles to wait for the host to respond to a wake condition before sending an HNR response.

7.6.26 Wake Up Status Register

Name: **WUSR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x18C**

Bits	Type	Default	Description
31:8	X		Reserved
7:0	RO		**Class** The classification result that triggered the wake up event.

7.6.27 Water Mark Values Register

Name: **WMVR** Reset Val: **0x0000_0400** Block: **CTL** Address: **0x190**

Bits	Type	Default	Description
31	X		Reserved
30:24	RO	0x7D	**Free** A count of the number of free memory blocks in the memory manager.
23	X		**Reserved**
22:16	RW	0x00	**Interrupt** Minimum number of free blocks before the host is interrupted.
15	X		Reserved
14:8	RW	0x04	**Headroom** Minimum number of free blocks before the MAC receiver is halted.
7	X		Reserved
6:0	RW	0x00	**PAUSE** Minimum number of free blocks before the PAUSE packet is sent.

Note: For all watermarks, a value of zero will disable the related feature.

7.6.28 Power Management Capabilities

Name: **PMCAP** Reset Val: 0x120A_4801 Block: **CTL** Address: **0x198**

Bits	Type	Default	Description
31:27	RO	0x02	**Support** Power management events supported. This field always reads back 00010b to indicate $\overline{\text{PME}}$ from D1 is supported.
26	RO	0	**D2 Support** Reads back 0 to indicate D2 is not supported.
25	RO	1	**D1 Support** Reads back 1 to indicate D1 is supported.
24:20	RO	0x00	**Init** Reads back 00000b to indicate no device specific initialization.
19	RO	1	**CLK** Reads back 1 to indicate the clock (BUSCLK) is needed for $\overline{\text{PME}}$ operation.
18:16	RO	010	**VER** Reads back 010b to indicate specification version 1.1 compliance.

Name: **PMCAP** Reset Val: 0x120A_4801 Block: **CTL** Address: **0x198**

Bits	Type	Default	Description
15:8	RO	0x48	**Next** Reads back 0x48. Points to next capability.
7:0	RO	0x01	**ID** Reads back 0x01.

7.6.29 Power Management Control and Status Register

Name: **PMCSR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x19C**

Bits	Type	Default	Description
31:24	X		Reserved
23:22	RW	00	**Psmarg1** Voltage regulator #1 margin.
21:20	RW	00	**Psmarg2** Voltage regulator #2 margin.
19:18	RW	00	**Psmarg3** Voltage regulator #3 margin.
17:16	X		Reserved
15	RW	0	**PME** Power management event status. This bit is set by a WAKE signal from the CAM and only cleared when the host writes a 1 to this bit.
14:9	X		Reserved
8	RW	0	**PME_ENB** Enables assertion of $\overline{\text{PME}}$ when there is a power management event.
7:2	X		Reserved
1:0	RW	00	**PS** Present power management state, 01b = D1, 00b = D0. (Any non-zero value here tells the part that the host is in power down mode). In any state other than D0, wake signals from classification are allowed to generate $\overline{\text{PME}}$ interrupts and the movement of receive data into QUEs is inhibited.

7.6.30 CAM Address Register

Name: **CAR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1A0**

Bits	Type	Default	Description
31:7	X		Reserved
6:0	RW	0x00	**ADDR** CAM address of rule being accessed by the RMR and RCR.

7.6.31 Rule Match Register

Name: **RMR** Reset Val: **0xFE3E_FF00** Block: **CTL** Address: **0x1A4**

Bits	Type	Default	Description
31:25	RW	0x7F	**Previous Hit Mask** Mask bits to match for the previous hit match. A zero means the corresponding bit in the previous hit match does not have to match to be a hit.
24	X		Reserved
23:17	RW	0x1F	**Previous Hit Match** This CAM entry matches against the address of the previous CAM hit.
16	X		Reserved
15:8	RW	0xFF	**Data Mask** Mask bits to match for the data match. A zero means the corresponding bit in the data match does not have to match to be a hit.
7:0	RW	0x00	**Data Match** This CAM field matches against either the packet byte or the control logic 'X' register value selected by the match control field of the control word register.

Note:

1. If all previous hit mask bits are zero, then the rule is disabled and will never match.
2. The RMR value is not valid for CAR ADDR values of zero or one.

7.6.32 Rule Control Register

Name: **RCR** Reset Val: **0x0000_0002** Block: **CTL** Address: **0x1A8**

Bits	Type	Default	Description
31:22	X		Reserved
21:16	RW	0x00	**Byte Offset** When this rule matches, do not attempt another match for this number of bytes. A zero means that the very next byte will be executed. A value of one means that the very next packet byte is ignored but the byte after that is executed, etc. When this field is used to initialize the counter, no offset is applied (see the TOC Control Logic Action).
15:8	X		Reserved
7	RW	0	**Interrupt** When a match is made for this rule then trigger an interrupt to the host.
6:2	RW	0x0	**Control Logic Action** Specifies what action to take when a match is made. The Control Logic Actions are described in detail in Table 26. 0x0 = NOP 0x14 = THXA 0x2 = PAUSE 0x15 = SETMC 0x4 = WAKE 0x16 = VLAN 0x6 = IPCK 0x17 = SETBC 0x7 = TIPO 0x18 = TOC 0x8 = TDX 0x1A = DEC 0xA = TAX 0x1B = MCTL 0xC = TAXH 0x1C = TDPH 0xD = TAXL 0x1D = TDLTH 0x10 = TXA 0x1E = TDPL 0x12 = TLXA 0x1F = TDLTL

Name: **RCR** Reset Val: **0x0000_0002** Block: **CTL** Address: **0x1A8**

Bits	Type	Default	Description
1:0	RW	10	**Match Control** How to generate a CAM reference word for the next pass. Match control is described in detail in Table 27. 00 = DONE 10 = MD 01 = MX 11 = DROP

7.6.33 Que Status Interrupt Register

Name: **QSIR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1C0**

Bits	Type	Default	Description
31	RO		**QDR Rise** Rising edge detected on QUE 7 QDR bit.
30	RO		**QDR Fall** Falling edge detected on QUE 7 QDR bit.
29	RO		**A Rise** Rising edge detected on QUE 7 QSR A bit. (See QSR)
28	RO		**B Rise** Rising edge detected on QUE 7 QSR B bit. (See QSR)
27:24	RO		**QUE 6** QDR Rise, QDR Fall, A Rise and B Rise interrupt bits for QUE 6.
23:20	RO		**QUE 5** QDR Rise, QDR Fall, A Rise and B Rise interrupt bits for QUE 5.
19:16	RO		**QUE 4** QDR Rise, QDR Fall, A Rise and B Rise interrupt bits for QUE 4.
15:12	RO		**QUE 3** QDR Rise, QDR Fall, A Rise and B Rise interrupt bits for QUE 3.
11:8	RO		**QUE 2** QDR Rise, QDR Fall, A Rise and B Rise interrupt bits for QUE 2.
7:4	RO		**QUE 1** QDR Rise, QDR Fall, A Rise and B Rise interrupt bits for QUE 1.
3:0	RO		**QUE 0** QDR Rise, QDR Fall, A Rise and B Rise interrupt bits for QUE 0.

Note: All bits are cleared on read.

7.6.34 Que Status Mask Register

Name: **QSMR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1C4**

Bits	Type	Default	Description
31:0	RW		**QUE Status Interrupt Mask** When a bit is set it enables the QUE status interrupt for the corresponding bit in the QSIR. When a bit is clear, the corresponding bit in the QSIR will still be set on its event and cleared on read but will not be passed on to the HIR.

7.6.35 Overflow/Underrun Interrupt Register

Name: **OUIR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1C8**

Bits	Type	Default	Description
31	RO	0	**QUE Data Overflow** Overflow condition detected on QUE 7.
30	RO	0	**QUE Data Underrun** Under-run condition detected on QUE 7.
29:28	RO	00	Reserved
27:26	RO	0x0	**QUE 6** QUE Data Overflow and QUE Data Underrun bits for QUE 6.
25:24	RO	00	Reserved
23:22	RO	0x0	**QUE 5** QUE Data Overflow and QUE Data Underrun bits for QUE 5.
21:20	RO	00	Reserved
19:18	RO	0x0	**QUE 4** QUE Data Overflow and QUE Data Underrun bits for QUE 4.
17:16	RO	00	Reserved
15:14	RO	0x0	**QUE 3** QUE Data Overflow and QUE Data Underrun bits for QUE 3.
13:12	RO	00	Reserved
11:10	RO	0x0	**QUE 2** QUE Data Overflow and QUE Data Underrun bits for QUE 2.
9:8	RO	00	Reserved
7:6	RO	0x0	**QUE 1** QUE Data Overflow and QUE Data Underrun bits for QUE 1.
5:4	RO	00	Reserved
3:2	RO	0x0	**QUE 0** QUE Data Overflow and QUE Data Underrun bits for QUE 0.
1:0	RO	00	Reserved

Note: All bits are cleared on read.

7.6.36 Overflow/Underrun Mask Register

Name: **OUMR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1CC**

Bits	Type	Default	Description
31:0	RW	0x0000 0000	**Overflow/Underrun Interrupt Mask** When a bit is set, it enables the overflow/underrun interrupt for the corresponding bit in the OUIR. When a bit is clear, the corresponding bit in the OUIR will still be set on its event and cleared on read but will not be passed on to the HIR.

7.6.37 Transmit RMON Interrupt Register

Name: **TRIR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1D0**

Bits	Type	Default	Description
31:0	RO	0x0000 0000	**RMON Tx Counter Rollover** Set when the RMON Tx counter with the same index number as the bit number has rolled over.

Note: All bits are cleared on read.

7.6.38 Transmit RMON Mask Register

Name: **TRMR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1D4**

Bits	Type	Default	Description
31:0	RW	0x0000 0000	**Tx RMON Interrupt Mask** When a bit is set, it enables the Tx RMON interrupt for the corresponding bit in the TRIR. When a bit is clear, the corresponding bit in the TRIR will still be set on its event and cleared on read but will not be passed on to the HIR.

7.6.39 Receive RMON Interrupt Register

Name: **RRIR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1D8**

Bits	Type	Default	Description
31:0	RO	0x0000 0000	**RMON Rx Counter Rollover** Set when the RMON Rx counter with an index equal to the bit number plus 32 has rolled over.

Note: All bits are cleared on read.

7.6.40 Receive RMON Mask Register

Name: **RRMR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1DC**

Bits	Type	Default	Description
31:0	RW	0x0000 0000	**Rx RMON Interrupt Mask** When a bit is set, it enables the Rx RMON interrupt for the corresponding bit in the RRIR. When a bit is clear, the corresponding bit in the RRIR will still be set on its event and cleared on read but will not be passed on to the HIR.

7.6.41 Host Interrupt Register

Name: **HIR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1E8**

Bits	Type	Default	Description
31:21	X	0x000	Reserved
20	RO	0	**WAKE** $\overline{\text{PME}}$ is asserted low (a power event has occurred).
19	RO	0	**QUE Status** QSIR interrupt.
18	RO	0	**QUE Overflow/Underrun** OUIR interrupt.
17	RO	0	**PHY**
16	RO	0	**RMON**
15:13	X	0	Reserved
12	RO	0	**Tx Bad** A transmitted frame had an error.
11	RO	0	**Rx Bad** A frame was received with an error.
10:9	X		Reserved
8	RO	0	**Late Rx Notify** This interrupt is asserted each time an entire frame is added to the receive QUE.
7	RO	0	**Early Rx Notify** Data reception has started (delayed by the IDCR).

Name: **HIR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1E8**

Bits	Type	Default	Description
6	RO	0	Reserved.
5	RO	0	**Late Tx Notify** Interrupt on completion. (See PCWR)
4	RO	0	**Early Tx Notify** Interrupt at the start of transmission. (See PCWR)
3	RO	0	**WATER MARK** Interrupt when the free BLOCK count hits the low water mark.
2	RO	0	**QUE Overflow** Interrupt when a QUE requests memory and there is none.
1	RO	0	**PAUSE** Interrupt when the local pause changes state (on/off).
0	RO	0	**Class** Packet classification interrupt.

Note: Bits 15:0 are cleared on read. Bits 31:16 are only cleared when the source is cleared.

7.6.42 Host Interrupt Mask Register

Name: **HIMR** Reset Val: **0x0000_0000** Block: **CTL** Address: **0x1EC**

Bits	Type	Default	Description
31:0	RW		**Host Interrupt Mask** When a bit is set here it enables the host interrupt for the corresponding bit in the HIR. When a bit is clear here, the corresponding bit in the HIR will still be set on its event and cleared on read but will not trigger an interrupt on $\overline{\text{INT}}$.

7.7 PHY Management Registers

7.7.1 PHY Register Overview

The 78Q8430 PHY implements sixteen-bit registers which are accessible via the MAC Station Management Access Registers. The supported registers are shown below. Unsupported registers will be read as all zeroes. The 78Q8430 PHY responds to PHYAD value 00001b.

The types of PHY Register access are summarized in Table 34.

Table 34: PHY Register Group

Address	Symbol	Name	Default (Hex)
0	MR0	Control	3100
1	MR1	Status	(7849)
2	MR2	PHY Identifier 1	000E
3	MR3	PHY Identifier 2	7237
4	MR4	Auto-Negotiation Advertisement	(01E1)
5	MR5	Auto-Negotiation Link Partner Ability	0001
6	MR6	Auto-Negotiation Expansion	0000
7-15		Reserved	0000
16	MR16	Vendor Specific	(0140)
17	MR17	Interrupt Control/Status	0000
18	MR18	Diagnostic Register	0000
19	MR19	Transceiver Control	4XXX
20-22		Reserved	XXXX
23	MR23	LED Configuration	0010
24	MR24	MDI/MDIX Control	(00C0)

Notes:

1. These registers can only be accessed indirectly via the MDDAR and MDCAR registers. They cannot be accessed directly through the GBI address space.
2. The default values annotated with () are dependent on configuration states.

7.7.2 PHY Control Register – MR0

Bits	Symbol	Type	Default	Description
15	RESET	R/WC	0	**Reset** Setting this bit to 1 resets the device and sets all registers to the default states. This bit is self-clearing.
14	LOOPBK	R/W	0	**Loopback** When this bit is set to 1, input data at TXD[3:0] is output at RXD[3:0]. No transmission of data on the network medium occurs and receive data on the network medium is ignored. By default, the loopback signal path encompasses most of the digital functional blocks. This bit allows for diagnostic testing.
13	SPEEDSL	R/W	1	**Speed Selection** This bit determines the speed of operation of the 78Q8430 PHY. Setting this bit to 1 indicates 100Base-TX operation and a 0 indicates 10Base-T mode. This bit will default to 1 upon reset. When auto-negotiation is enabled, this bit will not be writable and will have no effect on the 78Q8430 PHY. If auto-negotiation is not enabled, this bit may be written to force manual configuration.
12	ANEGEN	R/W	1	**Auto-negotiation Enable** The auto-negotiation process is enabled by setting this bit to 1. This bit will default to 1. If this bit is cleared to 0, manual speed and duplex mode selection is accomplished through bit 13 (SPEEDSL) and bit 8 (DUPLEX) of the MR0 Control Register.
11	PWRDN	R/W	0	**Power-down** The device may be placed in a low power consumption state by setting this bit to 1. While in the power-down state, the device will still respond to management transactions.
10	RSVD	R	0	Reserved
9	RANEG	R/WC	0	**Restart Auto-negotiation** Normally, the Auto-Negotiation process is started at power up. The process can be restarted by setting this bit to 1. This bit is self-clearing.
8	DUPLEX	R/W	1	**Duplex Mode** This bit determines whether the device supports full- duplex or half duplex. A 1 indicates full duplex operation and a 0 indicates half duplex. This bit will default to 1 upon reset. When auto-negotiation is enabled, this bit will not be writable and will have no effect on the 78Q8430 PHY. If auto-negotiation is not enabled, this bit may be written to force manual configuration.
7	COLT	R/W	0	**Collision Test** When this bit is set to 1, the device will assert the COL signal in response to the assertion of the TX_EN signal. Collision test is disabled if the PCSBP bit, MR16[1], is high. The Collision test can be activated regardless of the duplex mode of operation.
6:0	RSVD	R	0	Reserved

7.7.3 PHY Status Register – MR1

MR1 bits 15 through 11 reflect the ability of the 78Q8430 PHY. They do not reflect any ability changes made via the MII Management interface to MR0 bits 13 (SPEEDSL), 12 (ANEGEN) and 8 (DUPLEX).

Bits	Symbol	Type	Default	Description
15	100T4	R	0	**100BASE-T4 Ability** Reads 0 to indicate the 78Q8430 PHY does not support 100BASE-T4 mode.
14	100X_F	R	1	**100BASE-TX Full Duplex Ability** 0 = Not able 1 = Able (default)
13	100X_H	R	1	**100BASE-TX Half Duplex Ability** 0 = Not able 1 = Able (default)
12	10T_F	R	1	**10BASE-T Full Duplex Ability** 0 = Not able 1 = Able (default)
11	10T_H	R	1	**10BASE-T Half Duplex Ability** 0 = Not able 1 = Able (default)
10	100T2_F	R	0	**100BASE-T2 Full Duplex Ability** Reads 0 to indicate the 78Q8430 PHY does not support 100BASE-T2 full duplex mode.
9	100T2_H	R	0	**100BASE-T2 Half Duplex Ability** Reads 0 to indicate the 78Q8430 PHY does not support 100BASE-T2 half duplex mode.
8	EXTS	R	0	**Extended Status Information Availability** Reads 0 to indicate the 78Q8430 PHY does not support Extended Status information in MR15.
7	RSVD	R	0	Reserved
6	MFPS	R	0	**Management Frame Preamble Suppression Support** A 0 indicates that the 78Q8430 PHY can read management frames with a preamble.
5	ANEGC	R	0	**Auto-negotiation Complete** Logic one indicates that the auto-negotiation process has been completed and that the contents of registers MR4, 5, 6 are valid.
4	RFAULT	RC/LH	0	**Remote Fault** A logic one indicates that a remote fault condition has been detected and when so, it remains set until it is cleared. This bit can only be cleared by reading this register (MR1) via the management interface.
3	ANEGA	R	(1)	**Auto-negotiation Ability** When set, this bit indicates the device's ability to perform Auto-Negotiation. The value of this bit is determined by the ANEGEN bit (MR0.12).
2	LINK	RC/LL	0	**Link Status** A logic one indicates that a valid link has been established. If the link status should transition from an OK status to a NOT-OK status, this bit will become cleared and remains cleared until it is read.

Bits	Symbol	Type	Default	Description
1	JAB	RC/LH	0	**Jabber Detect** In 10Base-T mode, this bit is set during a jabber event. After the event, the bit remains set until cleared by a read operation.
0	EXTD	R	1	**Extended Capability** Reads 1 to indicate the 78Q8430 PHY provides an extended register set (MR2 and beyond).

7.7.4 PHY Identifier Registers – MR2, MR3

MR2: PHY Identifier Register 1

Bits	Symbol	Type	Value	Description
15:0	OUI [23:6]	R	000Eh	Organizationally Unique Identifier This value is 00-C0-39 for Teridian Semiconductor Corporation. This register contains 16 of the upper 18 bits of the identifier.

MR3: PHY Identifier Register 2

Bits	Symbol	Type	Value	Description
15:10	OUI [5:0]	R	1Ch	**Organizationally Unique Identifier** The remaining 6 bits of the 24-bit OUI.
9:4	MN	R	23h	**Model Number** The 23 from the model number is encoded into the 6 bits.
3:0	RN	R	03h	**Revision Number** The value 0011 corresponds to the third revision of the silicon.

7.7.5 PHY Auto-Negotiation Advertisement Registers – MR4

Bits	Symbol	Type	Default	Description
15	NP	R	0	**Next Page** Not supported. Reads logic zero.
14	RSVD	R	0	Reserved
13	RF	R/W	0	**Remote Fault** Setting this bit to 1 allows the device to indicate to the link partner a Remote Fault Condition.
12:5	TAF	R/W	(0Fh)	**Technology Ability Field** The default value of this field is dependent upon the MR1.15: 11 register bits. This field can be overwritten by management to auto-negotiate to an alternate common technology. Writing to this register has no effect until auto-negotiation is re-initiated.
12	A7	R	0	Reserved
11	ASYMP	R/W	0	**Asymmetric PAUSE Operation for Full Duplex Links** 0 = Asymmetric PAUSE operation not supported 1 = Asymmetric PAUSE operation is supported Writing to this register has no effect until auto-negotiation is re-initiated.
10	PAUSE	R/W	0	**PAUSE Operation for Full Duplex Links** 0 = PAUSE operation not supported 1 = PAUSE operation is supported Writing to this register has no effect until auto-negotiation is re-initiated.
9	A4	R	0	**100BASE-T4** The 78Q8430 PHY does not support 100BASE-T4 operations.
8	A3	R/W	1	**100BASE-TX Full Duplex** This bit will be set to 1 upon reset and is writeable. Writing to this register has no effect until auto-negotiation is re-initiated.

Bits	Symbol	Type	Default	Description
7	A2	R/W	1	100BASE-TX Half Duplex This bit will be set to 1 upon reset and is writeable. Writing to this register has no effect until auto-negotiation is re-initiated.
6	A1	R/W	1	**10BASE-T Full Duplex** This bit will be set to 1 upon reset and is writeable. Writing to this register has no effect until auto-negotiation is re-initiated.
5	A0	R/W	1	**10BASE-T** This bit will be set to 1 upon reset and is writeable. Writing to this register has no effect until auto-negotiation is re-initiated.
4:0	S4:0	R	01h	**Protocol Selector Field** The value is 00001 for IEEE 802.3.

7.7.6 PHY Auto-Negotiation Line Partner Ability Register – MR5

Bits	Symbol	Type	Default	Description
15	NP	R	0	**Next Page** When 1 is read, it indicates the link partner wishes to engage in Next Page exchange.
14	ACK	R	0	**Acknowledge** When 1 is read, it indicates the link partner has successfully received at least 3 consecutive and consistent FLP bursts.
13	RF	R	0	**Remote Fault** When 1 is read, it indicates the link partner has a fault.
12:5	A7:0	R	0	**Technology Ability Field** This field contains the technology ability of the link partner. The bit definition is the same as MR4.12:5.
4:0	S4:0	R	00h	**Selector Field** This field contains the type of message sent by the link partner. For IEEE 802.3 compliant link partner, this field should be 00001.

When MR5 contains a next page message, the bit definition is the same as MR7.

7.7.7 PHY Auto-Negotiation Expansion Register – MR6

Bits	Symbol	Type	Default	Description
15:5	RSVD	R	0	Reserved
4	PDF	RC/LH	0	**Parallel Detection Fault** When 1 is read, it indicates that more than one technology has been detected during link up. This bit is cleared when read.
3	LPNPA	R	0	**Link Partner Next Page Able** When 1 is read, it indicates the link partner supports the Next Page function.
2	NPA	R	0	**Next Page Able** Reads 0 since the 78Q8430 PHY does not support the Next Page function.
1	PRX	RC/LH	0	**Page Received** Reads 1 when a new link code word has been received into the Auto-negotiation Link Partner Ability Register. This bit is cleared upon read.
6.0	LPANEGA	R	0	**Link Partner Auto-negotiation Able** When 1 is read, it indicates the link partner is able to participate in the Auto-Negotiation function.

7.7.8 PHY Vendor Specific Register – MR16

Bits	Symbol	Type	Default	Description
15	RSVD	R	0	Reserved
14	RSVD	R	0	Reserved
13	RSVD	R	0	Reserved
12	TXHIM	R/W	0	**Transmitter High-Impedance Mode** When set, the TXOP/TXON transmit pins and the TX_CLK pin are put into a high-impedance state. The receive circuitry remains fully functional.
11	SQEI	R/W	0	**SQE Test Inhibit** Setting this bit to 1 disables 10Base-T SQE testing. By default, this bit is 0 and generates a COL pulse following the completion of a packet transmission to perform the SQE test.
10	NL10	R/W	0	**10Base-T Natural Loopback** Setting this bit to 1 causes transmit data received on the TXD0-3 pins to be automatically looped back to the RXD0-3 pins when 10Base-T mode is enabled.
9	RSVD	R	0	Reserved
8	RSVD	R	1	Reserved
7	RSVD	R	0	Reserved
6	RSVD	R	1	Reserved
5	APOL	R/W	0	**Auto Polarity** During auto-negotiation and 10BASE-T mode, the 78Q8430 PHY is able to automatically invert the received signal due to a wrong polarity connection. It does so by detecting the polarity of the link pulses. Setting this bit to 1 disables this feature.
4	RVSPOL	R/W	0	**Reverse Polarity** The reverse polarity is detected either through 8 inverted 10Base-T link pulses (NLP) or through one burst of inverted clock pulses in the auto-negotiation link pulses (FLP). When the reverse polarity is detected and if the Auto Polarity feature is enabled, the 78Q8430 PHY will invert the receive data input and set this bit to 1. If Auto Polarity is disabled, then this bit is writeable. Writing a 1 to this bit forces the polarity of the receive signal to be reversed.
3:2	RSVD	R/W	0h	Reserved. Must set to 00.
1	PCSBP	R/W	0	**PCS Bypass Mode** When set, the 100Base-TX PCS and scrambling/ descrambling functions are bypassed. Scrambled 5-bit code groups for transmission are applied to the TX_ER, TXD3-0 pins and received on the RX_ER, RXD3-0 pins. The RX_DV and TX_EN signals are not valid in this mode. PCSBP mode is valid only when 100Base-TX mode is enabled and auto-negotiation is disabled.
0	RXCC	R/W	0	**Receive Clock Control** This function is valid only in 100Base-TX mode. When set to 1, the RX_CLK signal will be held low when there is no data being received (to save power). The RX_CLK signal will restart 1 clock cycle before the assertion of RX_DV and will be shut off 64 clock cycles after RX_DV goes low. RXCC is disabled when loopback mode is enabled (MR0.14 is high). This bit should be kept at logic zero when PCS Bypass mode is used.

7.7.9 PHY Interrupt Control / Status Register – MR17

The *Interrupt Control/Status Register* provides the means for controlling and observing the events that trigger an interrupt on the internal PHY interrupt signal. This register can also be used in a polling mode via the MII Serial Interface as a means to observe key events within the PHY via one register address. Bits 0 through 7 are status bits, which are each set to logic one based upon an event. These bits are cleared after the register is read. Bits 8 through 15 of this register, when set to logic one, enable their corresponding bit in the lower byte to signal an interrupt on the PHY interrupt signal.

Bits	Symbol	Type	Default	Description
15	JABBER_IE	R/W	0	**Jabber Interrupt Enable**
14	RXER_IE	R/W	0	**Receive Error Interrupt Enable**
13	PRX_IE	R/W	0	**Page Received Interrupt Enable**
12	PDF_IE	R/W	0	**Parallel Detect Fault Interrupt Enable**
11	LP_ACK_IE	R/W	0	**Link Partner Acknowledge Interrupt Enable**
10	LS_CHANGE_IE	R/W	0	**Link Status Change Interrupt Enable**
9	RFAULT_IE	R/W	0	**Remote Fault Interrupt Enable**
8	ANEG-COMP_IE	R/W	0	**Auto-Negotiation Complete Interrupt Enable**
7	JAB_INT	RC	0	**Jabber Interrupt** This bit is set high when a Jabber event is detected by the 10Base-T circuitry.
6	RXER_INT	RC	0	**Receive Error Interrupt** This bit is set high when the RX_ER signal transitions high.
5	PRX_INT	RC	0	**Page Received Interrupt** This bit is set high when a new page has been received from the link partner during auto-negotiation.
4	PDF_INT	RC	0	**Parallel Detect Fault Interrupt** This bit is set high by the auto-negotiation logic when a parallel detect fault condition is indicated.
3	LP_ACK_INT	RC	0	**Link Partner Acknowledge Interrupt** This bit is set high by the auto-negotiation logic when FLP bursts are received with the acknowledge bit set.
2	LS_CHANGE_INT	RC	0	**Link Status Change Interrupt** This bit is set when the link status transitions from an OK status to a FAIL status, or vice versa.
1	RFAULT_INT	RC	0	**Remote Fault Interrupt** This bit is set when a remote fault condition is detected.
0	ANEG_COMP_INT	RC	0	**Auto-Negotiation Complete Interrupt** This bit is set by the auto-negotiation logic upon completion of auto-negotiation.

7.7.10 PHY Transceiver Control Register – MR19

Bit	Symbol	Type	Default	Description
15:14	TXO[1:0]	R/W	01	**Transmit Amplitude Selection** Sets the transmit output amplitude to account for transmit transformer insertion loss. 00 = Gain set for 0.0dB of insertion loss 01 = Gain set for 0.4dB of insertion loss 10 = Gain set for 0.8dB of insertion loss 11 = Gain set for 1.2dB of insertion loss
13:0	RSVD	R/W	XXX	Reserved

7.7.11 PHY Diagnostic Register – MR18

This register contains both user accessible and non-user accessible bits (Reserved) for internal testmodes. The user-accessible bits are located at bit 12:8 locations.

Bit	Symbol	Type	Default	Description
15:13	RSVD	R	0	Reserved
12	ANEGF	RC	0	**Auto-Negotiation Fail Indication** This bit is set when auto-negotiation completes and no common technology was found. It remains set until read.
11	DPLX	R	0	**Duplex Indication** This bit indicates the result of the auto-negotiation for duplex arbitration as follows: 0 = half duplex was the highest common denominator 1 = full duplex was the highest common denominator
10	RATE	R	0	**Rate Indication** This bit indicates the result of the auto-negotiation for data rate arbitration as follows: 0 = 10Base-T was the highest common denominator 1 = 100Base-TX was the highest common denominator
9	RXSD	R	0	**Receiver Signal Detect Indication** In 10Base-T mode, this bit indicates that Manchester data has been detected. In 100Base-TX mode, it indicates that the receive signal activity has been detected (but not necessarily locked on to).
8	RXLCK	R	0	**Receive PLL Lock Indication** Indicates that the Receive PLL has locked onto the receive signal for the selected speed of operation (10Base-T or 100Base-TX).
7:0	RSVD	R	0	Reserved

7.7.12 PHY LED Configuration Register – MR23

Bit	Symbol	Type	Default	Description
15:8	RSVD	R/W	0	Reserved
7:4	LED1[3:0]	R	<1h>	0000 = Link OK 0001 = RX or TX Activity (Default LED1) 0010 = TX Activity 0011 = RX Activity 0100 = Collision 0101 = 100 BASE-TX mode 0110 = 10 BASE-T mode 0111 = Full Duplex 1000 = Link OK/Blink=RX or TX Activity
3:0	LED0[3:0]	R	<0h>	0000 = Link OK (Default LED0) 0001 = RX or TX Activity 0010 = TX Activity 0011 = RX Activity 0100 = Collision 0101 = 100 BASE-TX mode 0110 = 10 BASE-T mode 0111 = Full Duplex 1000 = Link OK/Blink=RX or TX Activity

7.7.13 PHY MDI / MDIX Control Register – MR24

Bit	Symbol	Type	Default	Description
15:8		R	0	Unused
7	PD_MODE	R/W	1	**Parallel Detect Mode** Write a 1 to this bit to add Parallel Detect mode. This will allow auto-switching to work when auto-negotiation is off while the other device has it on.
6	AUTO_SW	R/W	1	**Auto Switching** Write a 1 to this bit to enable auto switching.
5	MDIX	R/W	0	**MDI State** Indicates state of the MDI pair or force configuration: 1 = MDIX (cross over) 0 = MDI When AUTO_SW is a 1, this bit will only be readable. When AUTO_SW is a 0, this bit can be written to set the configuration.
4	MDIX_CM	R	0	**Auto-Switch Completion** Indicates completion of auto-switch sequence. 1 = Sequence completed 0 = Sequence in progress or auto-switch is disabled.
3:0	MDIX_SD	R/W	<0000>	**MDIX Seed** Write initial pattern seed for switching algorithm. Initial seed will directly affect attempts [9,8,5,4] respectively to written bits [3:0]. Setting to [0000] will result in device using its own seed of [0101].

8 Isolation Transformers

Table 35: Isolation Transformers

Name	Value	Condition
Turns Ratio	1 CT : 1 CT ± 5%	
Open-Circuit Inductance	350 µH (min)	@ 10 mV, 10 kHz
Leakage Inductance	0.40 µH (max)	@ 1 MHz (min)
Inter-Winding Capacitance	12 pF (max)	
D.C. Resistance	0.9 Ω (max)	
Insertion Loss	0.4 dB (typ)	0 - 65 MHz
HIPOT	1500 Vrms	

Two simple 1:1 isolation transformers are all that are required at the line interface, but transformers with integrated common-mode choke are recommended for exceeding FCC requirements. Table 35 gives the recommended line transformer characteristics. The 100Base-TX amplitude specifications assume a transformer loss of 0.4 dB. For the transmit line transformer with higher insertion losses, up to 1.2 dB of insertion loss can be compensated by selecting the appropriate setting in the Transmit Amplitude Selection bits in register MR19[11:10].

9 Reference Crystal

If the internal crystal oscillator is to be used, a crystal with the characteristics given in Table 36 should be chosen.

Table 36: Reference Crystal

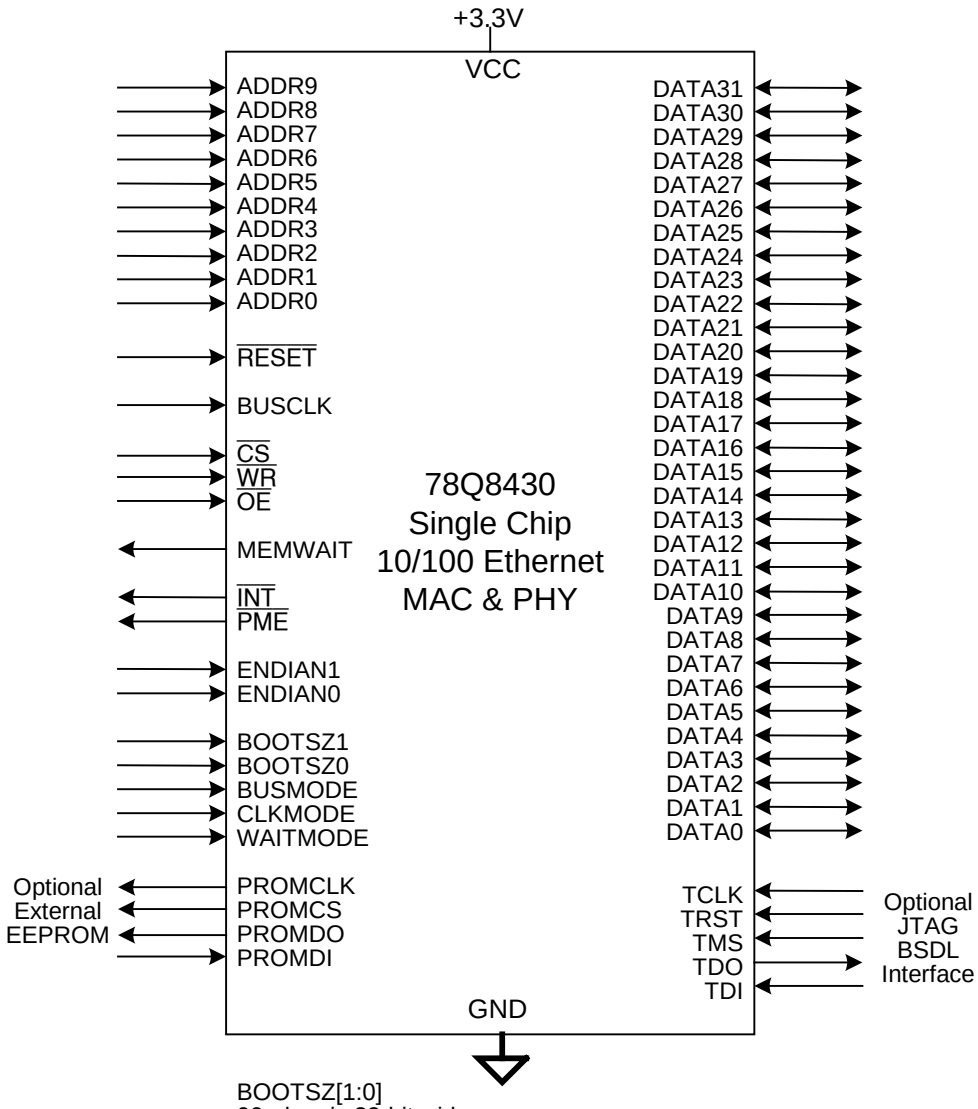
Name	Value	Units
Frequency	25.00000	MHz
Load Capacitance*	4**	pF
Frequency Tolerance	≤ ±50 per IEEE 802.3 requirement	PPM
Oscillation Mode	Parallel Resonance, Fundamental Mode	
Parameters at 25 °C ± 2 °C ; Drive Level = 0.5 mW		
Shunt Capacitance (max)	10	pF
Motional Capacitance (min)	10	pF
Series Resistance (max)	60	Ω
Spurious Response (max)	> 5 dB below main within 500 kHz	

* Equivalent differential capacitance across the XTLP/XTLN pins.

** If a crystal with a larger load is used, external shunt capacitors to ground should be added to make up the equivalent capacitance difference.

*** System vendors need to select the proper crystal according to their applications, such as operating environment, product lifetime, and etc since crystal aging, operating temperature, and other factors can affect the crystal frequency tolerance.

10 System Bus Interface Schematic



BOOTSZ[1:0]
00 - bus is 32-bit wide
01 - bus is 16-bit wide
10 - bus is 8-bit wide

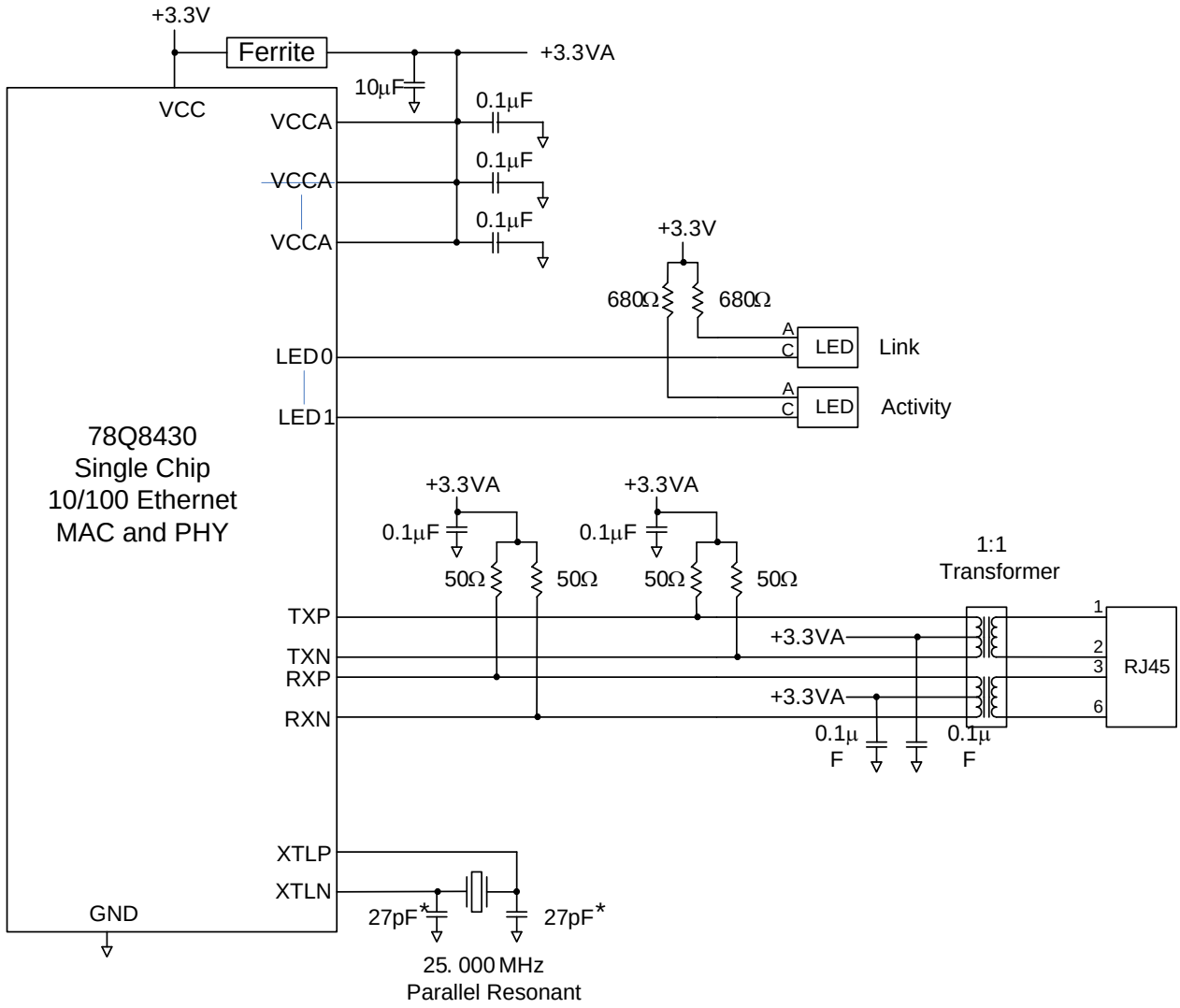
ENDIAN[1:0]
0,0 = Big Endian (MSB at high bit positions)
1,1 = Little Endian (MSB at low bit positions)

BUSMODE, CLKMODE, WAITMODE
0,0,0 = sync bus, ext. system clock, memwait act low
0,0,1 = sync bus, ext. system clock, memwait act high
1,0,0 = async bus, ext. system clock, memwait act low
1,0,1 = async bus, ext. system clock, memwait act high
1,1,0 = async bus, int. system clock, memwait act low
1,1,1 = async bus, int. system clock, memwait act high

Figure 15: System Bus Interface Schematic

11 Line Interface Schematic

Figure 16 shows a typical analog line interface schematic (not all components are shown).



*Shunt capacitor value will vary depending on crystal capacitance.

Figure 16: Line Interface Schematic

12 Package Mechanical Drawing (100-pin LQFP)

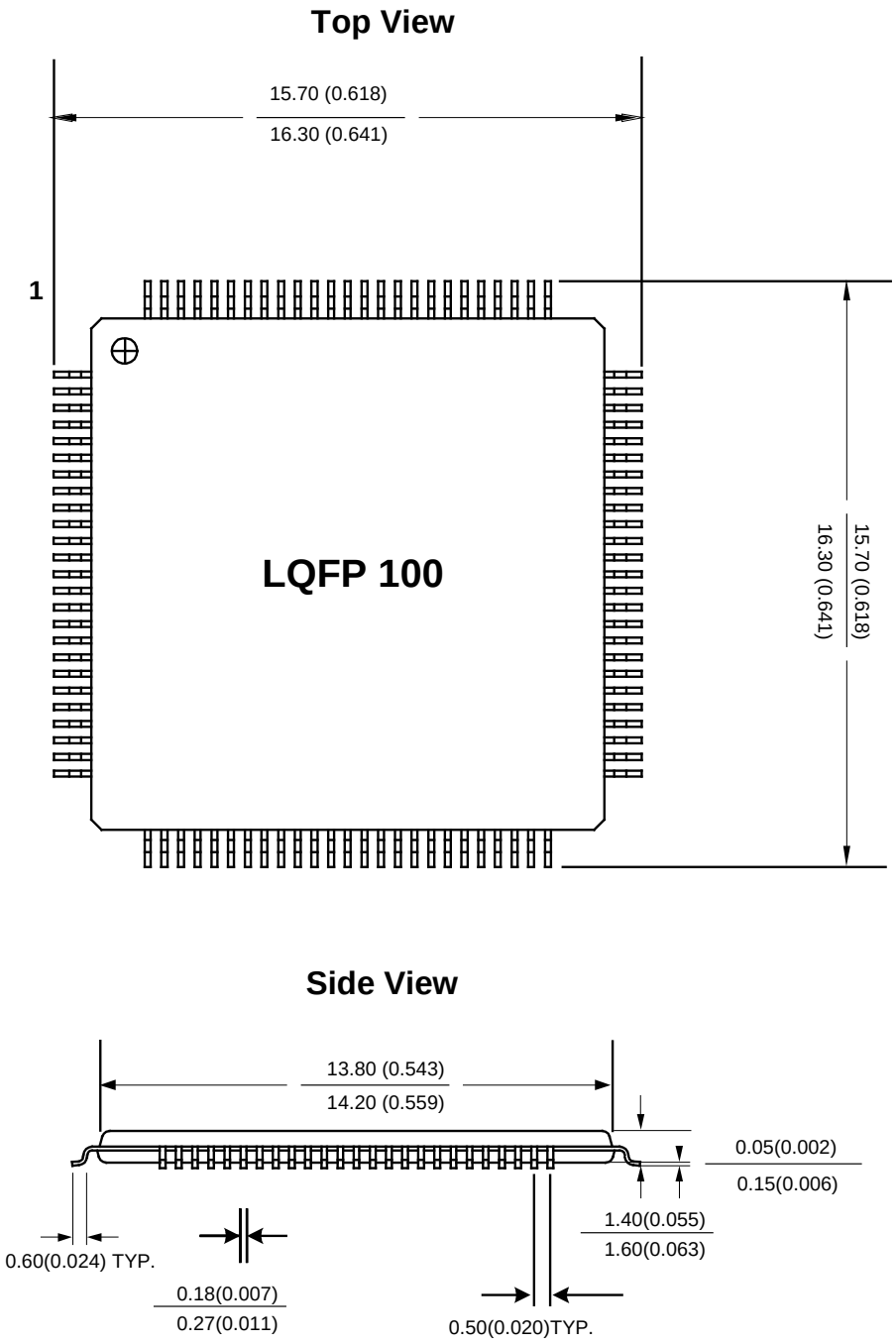


Figure 17: LQFP Drawing

13 Ordering Information

Table 37 lists the order numbers and packaging marks used to identify 78Q8430 products.

Table 37: 78Q8430 Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark
78Q8430 LQFP, Lead free	78Q8430-100IGT/F	78Q8430-100IGT
78Q8430 LQFP, Lead free, Tape and Reel	78Q8430-100IGTR/F	78Q8430-100IGT

14 Related Documentation

The following 78Q8430 documents are available from Teridian Semiconductor Corporation:

78Q8430 Data Sheet (this document)
78Q8430 Layout Guidelines
78Q8430 Software Driver Development Guidelines
78Q8430 Driver Guide for ST 5100/OS-20 with NexGen TCP/IP Stack
78Q8430 STEM Demo Board User Manual
78Q8430 Driver Guide for ARM920T Linux
78Q8430 ARM9(920T) Embest Evaluation Board User Manual
78Q8430 ARM9(920T) Linux Driver Diagnostic Guide

Check the website for the latest versions of these documents.

15 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 78Q8430, contact us at:

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For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	7/21/2008	First publication.
1.1	1/21/2009	Removed 128-pin package.
1.2	3/6/2009	Removed commercial temperature package.

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