

- Structure Silicon Monolithic Integrated Circuit
- Product 7 x 7 Matrix LED DRIVER for Mobile Phone
- Type **BH6948GU**
- Figure

1. Highly effective Charge Pump circuit that can be switched 1 time, 1.5 times, and 2 times pressure automatically. (190mA / MAX)
2. 7-channel LED DRIVER that can control PWM (IoMAX = 31mA/ch, Current step = 1mA)
3. 7-channel PMOS-SW controlled with 1/8TDMA
4. It is possible to make 49(7X7) LED shine by PMOS-SW and the LED driver
5. SPI Interface
6. Wafer Level CSP package for space constrained applications  
62pin (4.1mm × 4.1 mm height = 1.0mm-max)

● Absolute Maximum Ratings (Ta = 25°C)

| Parameter                   | Symbol           | Rating   | Unit |
|-----------------------------|------------------|----------|------|
| Maximum Supply Voltage      | V <sub>MAX</sub> | 5.5      | V    |
| Power Dissipation ※         | Pd               | 1.47     | W    |
| Operating Temperature Range | T <sub>opr</sub> | -30~+85  | °C   |
| Storage Temperature Range   | T <sub>stg</sub> | -55~+125 | °C   |

※ When using more than at Ta=25°C, it is reduced 14.7mW per 1°C.

When RHOM specification board 50mm X 58mm mounting.

Cautions : A device may be destroyed when it is used on the conditions beyond this value.

Moreover, the usual operation is not guaranteed.

● Operating Conditions

| Parameter         | Symbol             | Range    | Unit | Block    |
|-------------------|--------------------|----------|------|----------|
| VBAT1 Voltage ※1  | V <sub>BAT1</sub>  | 3.15~4.5 | V    | VREF/BGR |
| VBATCP Voltage ※1 | V <sub>BATCP</sub> |          | V    | DCDC     |
| DVDD1 Voltage ※2  | V <sub>DVDD1</sub> | 1.7~3.1  | V    | I/O      |
| DVDD2 Voltage ※2  | V <sub>DVDD2</sub> | 2.7~3.1  | V    | Logic    |

※1 49LED lighting

※2 DVDD1 ≤ DVDD2

©This product is not especially designed to be protected from radioactivity.

Status of this document.

The Japanese version of this document is the formal specification.

A customer may use this translation version only for reference to help reading the formal version.

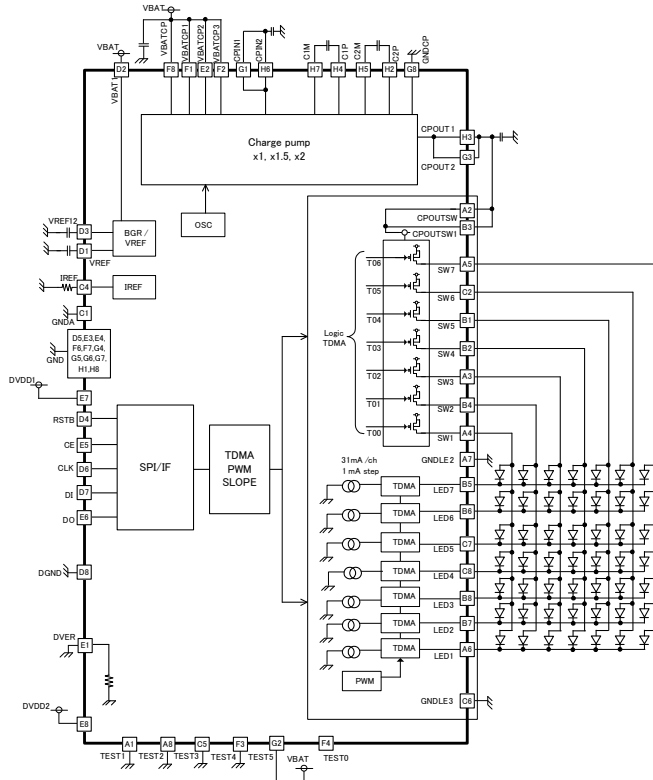
If there are any differences in translation version of this document, formal version takes priority.

# ● Electrical Characteristics

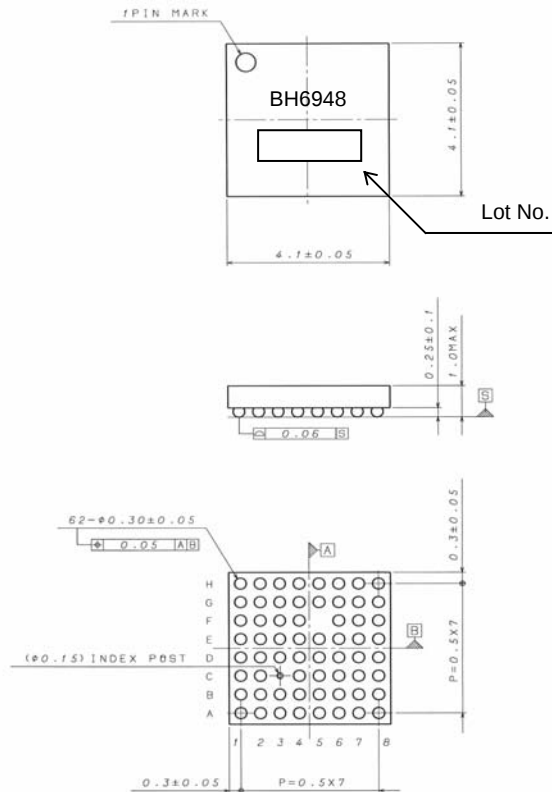
(Unless otherwise specified, Ta=25°C, VBAT1=VBATCP=VBATCP1-3=3.6V, DVDD1=1.8V, DVDD2=2.85V)

| Parameter                              |                                     | Symbol             | Spec |      |           | Units | Condition                                     |
|----------------------------------------|-------------------------------------|--------------------|------|------|-----------|-------|-----------------------------------------------|
|                                        |                                     |                    | MIN  | TYP  | MAX       |       |                                               |
| Circuit Current                        | Stand-by Circuit Current            | I <sub>ST</sub>    | -    | 0    | 8.8       | uA    | Stand-by mode (RSTB="H")                      |
|                                        | DC-DC Converter Current1            | I <sub>QCP1</sub>  | -    | 0.93 | 1.4       | mA    | 1times mode                                   |
|                                        | DC-DC Converter Current2            | I <sub>QCP2</sub>  | -    | 6.4  | 9.6       | mA    | 1.5times mode (CPOUT=4.75V)                   |
|                                        | DC-DC Converter Current3            | I <sub>QCP3</sub>  | -    | 4.8  | 7.2       | mA    | 2times mode (CPOUT=4.75V)                     |
| DCDC Converter                         | CPOUT Voltage1                      | V <sub>CP1</sub>   | 4.55 | 4.75 | 4.95      | V     | 1.5times mode No Load                         |
|                                        | CPOUT Output Current1               | I <sub>CP1</sub>   | -    | -    | 190       | mA    | 1.5times mode, VCPOUT>4V<br>49 LED lighting   |
|                                        | CPOUT Voltage2                      | V <sub>CP2</sub>   | 4.55 | 4.75 | 4.95      | V     | 2.0times mode No Load                         |
|                                        | CPOUT Output Current2               | I <sub>CP2</sub>   | -    | -    | 190       | mA    | 2.0times mode, VCPOUT>4V<br>49 LED lighting   |
|                                        | CPOUT Voltage3                      | V <sub>CP3</sub>   | 5.1  | 5.3  | 5.5       | V     | 1.5times mode No Load                         |
|                                        | CPOUT Output Current3               | I <sub>CP3</sub>   | -    | -    | 190       | mA    | 1.5times mode, VCPOUT>4V<br>49 LED lighting   |
|                                        | CPOUT Voltage4                      | V <sub>CP4</sub>   | 5.1  | 5.3  | 5.5       | V     | 2.0times mode No Load                         |
|                                        | CPOUT Output Current4               | I <sub>CP4</sub>   | -    | -    | 190       | mA    | 2.0times mode, VCPOUT>4V<br>49 LED lighting   |
|                                        | Oscillator Frequency                | f <sub>OSC</sub>   | 0.96 | 1.20 | 1.44      | MHz   |                                               |
| PMOS Switch                            | Leak Current when OFF (SW1~7 total) | I <sub>LEAKP</sub> | -    | -    | 7.0       | μ A   | When 35H(MATRIXCNT)bit0(START)=0              |
| Current Driver (Lo-Mode, LED1~7)       | Output Current1                     | I <sub>O1</sub>    | -8.5 | -    | +8.5      | %     | I=1mA Setting                                 |
|                                        | Output Current2、 3                  | I <sub>O2</sub>    | -8.0 | -    | +8.0      | %     | I=2~3mA Setting                               |
|                                        | Output Current4~31                  | I <sub>O4</sub>    | -7.0 | -    | +7.0      | %     | I=4~31mA Setting                              |
|                                        | Output Current matching1            | Mat1               | -    | -    | 11.5      | %     | I=1~3mA Setting, Mat1=(IoMax-IoMin)/IoMinx100 |
|                                        | Output Current matching2            | Mat2               | -    | -    | 10        | %     | I=4~31mA Setting Mat2=(IoMax-IoMin)/IoMinx100 |
|                                        | Leak Current when OFF (SW1~7 total) | I <sub>LEAK</sub>  | -    | -    | 7.0       | uA    | When 35H(MATRIXCNT)bit0(START)=0              |
| Current Driver (RGB with PWM : LED1~7) | PWM on duty1                        | PWMD1              | 1.54 | 5.04 | 8.54      | %     | PWM1~7SET=5digit                              |
|                                        | PWM on duty2                        | PWMD2              | 43.7 | 47.2 | 40.7      | %     | PWM1~7SET=32digit                             |
|                                        | PWM on duty3                        | PWMD3              | 84.6 | 88.1 | 91.6      | %     | PWM1~7SET=58digit                             |
| Under Voltage Lockout                  | UVLO Threshold                      | V <sub>UVLO</sub>  | 2.0  | 2.25 | 2.6       | V     | VBAT falling                                  |
|                                        | UVLO Hysteresis                     | V <sub>UVLO</sub>  | 50   | 100  | 150       | mV    |                                               |
| Soft-Start                             | SS Mode Time                        | T <sub>SS</sub>    | 1.6  | 2.0  | 2.4       | ms    |                                               |
| Short Circuit Protector                | SCP Threshold                       | V <sub>SCP</sub>   | 1.0  | 1.2  | 1.4       | V     | CPOUT falling                                 |
|                                        | Delay Time                          | T <sub>DLY</sub>   | 8    | 10   | 12        | mS    |                                               |
|                                        | Reset Time                          | T <sub>RST</sub>   | 80   | 100  | 120       | mS    |                                               |
| Over Current Protector                 | OCP Threshold                       | I <sub>OCP</sub>   | -    | 790  | -         | mA    |                                               |
| Over Voltage Protector                 | OVP Threshold                       | V <sub>ovp</sub>   | 5.50 | 5.62 | 5.74      | V     |                                               |
| LED Dropout Detector                   | Detect Voltage                      | V <sub>DR</sub>    | 0.36 | 0.40 | 0.44      | V     |                                               |
| SPI I/F                                | Input "H" Level                     | V <sub>IH</sub>    | 1.4  | -    | DVDD1+0.3 | V     |                                               |
|                                        | Input "L" Level                     | V <sub>IL</sub>    | -0.3 | -    | 0.4       | V     |                                               |
|                                        | "H" Level Input Current             | I <sub>IH</sub>    | -    | 0    | 1         | uA    |                                               |
|                                        | "L" Level Input Current             | I <sub>IL</sub>    | -    | 0    | 1         | uA    |                                               |
| RSTB                                   | Input "H" Level                     | V <sub>IH</sub>    | 1.4  | -    | DVDD1+0.3 | V     |                                               |
|                                        | Input "L" Level                     | V <sub>IL</sub>    | -0.3 | -    | 0.4       | V     |                                               |
|                                        | "H" Level Input Current             | I <sub>IH</sub>    | -    | 0    | 1         | uA    |                                               |
|                                        | "L" Level Input Current             | I <sub>IL</sub>    | -    | 0    | 1         | uA    |                                               |

## ● Block Diagram



## ● Package Outline



Drawing No: EX903-5021

(UNIT: mm)

REV. B

## ● Terminal List

| FBGA62R1 BALL Name | FBGA62R1 BALL No. | FUNCTION                                                      |
|--------------------|-------------------|---------------------------------------------------------------|
| TEST1              | A1                | Test terminal 1 (※ Please be sure connect to GND)             |
| CPOUTSW            | A2                | Power supply for SW1~7                                        |
| SW3                | A3                | P-MOS SW3 output                                              |
| SW1                | A4                | P-MOS SW1 output                                              |
| SW7                | A5                | P-MOS SW7 output                                              |
| LED1               | A6                | LED1 driver output                                            |
| GNDLE2             | A7                | GND for LED1~3                                                |
| TEST2              | A8                | Test terminal 2 (※ Please be sure connect to GND)             |
| SW5                | B1                | P-MOS SW5 output                                              |
| SW4                | B2                | P-MOS SW4 output                                              |
| CPOUTSW1           | B3                | Power supply for SW1~7                                        |
| SW2                | B4                | P-MOS SW2 output                                              |
| LED7               | B5                | LED7 driver output                                            |
| LED6               | B6                | LED6 driver output                                            |
| LED2               | B7                | LED2 driver output                                            |
| LED3               | B8                | LED3 driver output                                            |
| GND4               | C1                | GND for VREF, IREF                                            |
| SW6                | C2                | P-MOS SW6 output                                              |
| IREF               | C4                | LED Constant Current Driver Current setting Terminal          |
| TEST3              | C5                | Test terminal 3 (※ Please be sure connect to GND)             |
| GNDLE3             | C6                | GND for LED4~7                                                |
| LED5               | C7                | LED5 driver output                                            |
| LED4               | C8                | LED4 driver output                                            |
| VREF               | D1                | Stabilization Power Supply for IREF, VSATDET, OSC             |
| VBAT1              | D2                | Power supply for BGR, VREF, SCP                               |
| VREF12             | D3                | Standard for OSC, VSATDET, IREF                               |
| RSTB               | D4                | Reset terminal                                                |
| GND                | D5                | GND terminal                                                  |
| CLK                | D6                | 4 line serial interface CLK                                   |
| DI                 | D7                | 4 line serial interface DATAIN                                |
| DGND               | D8                | GND for internal logic                                        |
| DVER               | E1                | Device version                                                |
| VBATCP2            | E2                | Power supply for charge pump                                  |
| GND                | E3                | GND terminal                                                  |
| GND                | E4                | GND terminal                                                  |
| CE                 | E5                | 4 line serial interface CE                                    |
| DO                 | E6                | 4 line serial interface DATAOUT                               |
| DVDD1              | E7                | Power supply for interface                                    |
| DVDD2              | E8                | Power supply for internal logic                               |
| VBATCP1            | F1                | Power Supply for Charge Pump Section                          |
| VBATCP3            | F2                | Power Supply for Charge Pump Section                          |
| TEST4              | F3                | TEST terminal 4 (※ Please be sure connect to GND)             |
| TEST0              | F4                | Test output terminal (※ Please should be left open when used) |
| GND                | F6                | GND terminal                                                  |
| GND                | F7                | GND terminal                                                  |
| VBATCP             | F8                | Power Supply for Charge Pump section                          |
| CPIN1              | G1                | Power Supply for Charge Pump section Step-up Voltage Circuit  |
| TEST5              | G2                | TEST terminal 5 (※ Please be sure to connect to VBAT)         |
| CPOUT2             | G3                | Charge Pump section Constant Voltage Output                   |
| GND                | G4                | GND terminal                                                  |
| GND                | G5                | GND terminal                                                  |
| GND                | G6                | GND terminal                                                  |
| GND                | G7                | GND terminal                                                  |
| GNDCP              | G8                | GND for Charge pump section                                   |
| GND                | H1                | GND terminal                                                  |
| C2P                | H2                | Charge Pump section Flying Capacitor2 on Side of Plus         |
| CPOUT1             | H3                | Charge Pump section Constant Voltage Output                   |
| C1P                | H4                | Charge Pump section Flying Capacitor1 on Side of Plus         |
| C2M                | H5                | Charge Pump section Flying Capacitor2 on Side of Minus        |
| CPIN2              | H6                | Power Supply for Charge Pump section Step-up Voltage Circuit  |
| C1M                | H7                | Charge Pump section Flying Capacitor1 on Side of Minus        |
| GND                | H8                | GND terminal                                                  |

## ● Use-related Cautions

- (1) Absolute maximum ratings  
 If applied voltage ( $V_{MAX}$ ), operating temperature range ( $T_{opr}$ ), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.
- (2) Power supply lines  
 In the design of the board pattern, make power supply and GND line wiring low impedance.  
 When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.  
 When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.  
 Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.
- (3) GND voltage  
 Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.
- (4) Shorts between pins and misinstallation  
 When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.
- (5) Operation in strong magnetic fields  
 Be careful when using the LSI in a strong magnetic field, since it may malfunction.
- (6) Input pins  
 Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.
- (7) Externally attached capacitors  
 When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.
- (8) Thermal shutdown circuit (TSD)  
 When the junction temperature becomes higher, the thermal shutdown circuit operates and turns the switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.
- (9) Thermal design  
 Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.
- (10) Test terminal and unused terminal processing  
 Please process a test terminal and unused terminal according to explanations of the function manual and the application note, etc. to be unquestionable while real used. Moreover, please inquire of the person in charge of our company about the terminal without the explanation especially.
- (11) Rush current  
 For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

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