DS1267
Dual Digital Potentiometer Chip

www.dalsemi.com

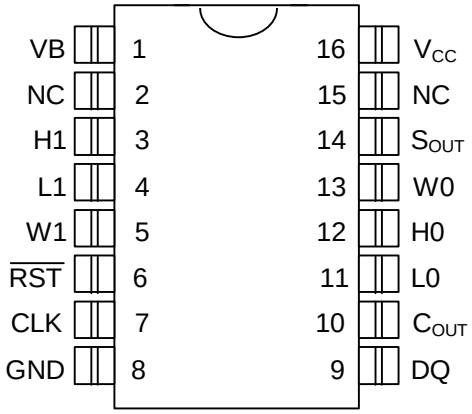
FEATURES

- Ultra-low power consumption, quiet, pumpless design
- Two digitally controlled, 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide increased total resistance
- 14-pin DIP, 16-pin SOIC, 20-pin TSSOP packages
- Resistive elements are temperature compensated to ±0.3 LSB relative linearity
- Standard resistance values:
  - DS1267-10 ~ 10 kΩ
  - DS1267-50 ~ 50 kΩ
  - DS1267-100 ~ 100 kΩ
- Operating Temperature Range:
  - Industrial: -40°C to +85°C

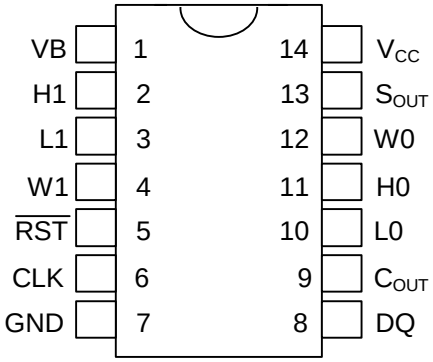
PIN DESCRIPTIONS

L0, L1	-	Low End of Resistor
H0, H1	-	High End of Resistor
W0, W1	-	Wiper Terminal of Resistor
V_B	-	Substrate Bias Voltage
S_{OUT}	-	Stacked Configuration Output
$\overline{RST}$	-	Serial Port Reset Input
DQ	-	Serial Port Data Input
CLK	-	Serial Port Clock Input
C_{OUT}	-	Cascade Port Output
V_{CC}	-	+5 Volt Supply
GND	-	Ground
NC	-	No Internal Connection

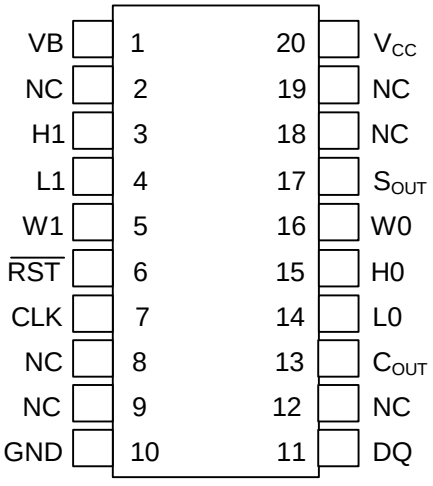
PIN ASSIGNMENT



16-Pin SOIC (300-mil)
See Mech. Drawings Section



14-Pin DIP (300-mil)
See Mech. Drawings Section



20-Pin TSSOP (173-mil)

DESCRIPTION

The DS1267 Dual Digital Potentiometer Chip consists of two digitally controlled, solid-state potentiometers. Each potentiometer is composed of 256 resistive sections. Between each resistive section and both ends of the potentiometer are tap points which are accessible to the wiper. The position of the wiper on the resistive array is set by an 8-bit value that controls which tap point is connected to the wiper output. Communication and control of the device are accomplished via a 3-wire serial port interface. This interface allows the device wiper position to be read or written.

Both potentiometers can be connected in series (or stacked) for an increased total resistance with the same resolution. For multiple-device, single-processor environments, the DS1267 can be cascaded or daisy-chained. This feature provides for control of multiple devices over a single 3-wire bus.

The DS1267 is offered in three standard resistance values which include 10, 50, and 100-kohm versions. Available packages for the device include a 14-pin DIP, 16-pin SOIC, and 20-pin TSSOP.

OPERATION

The DS1267 contains two 256-position potentiometers whose wiper positions are set by an 8-bit value. These two 8-bit values are written to a 17-bit I/O shift register that is used to store the two wiper positions and the stack select bit when the device is powered. A block diagram of the DS1267 is presented in Figure 1.

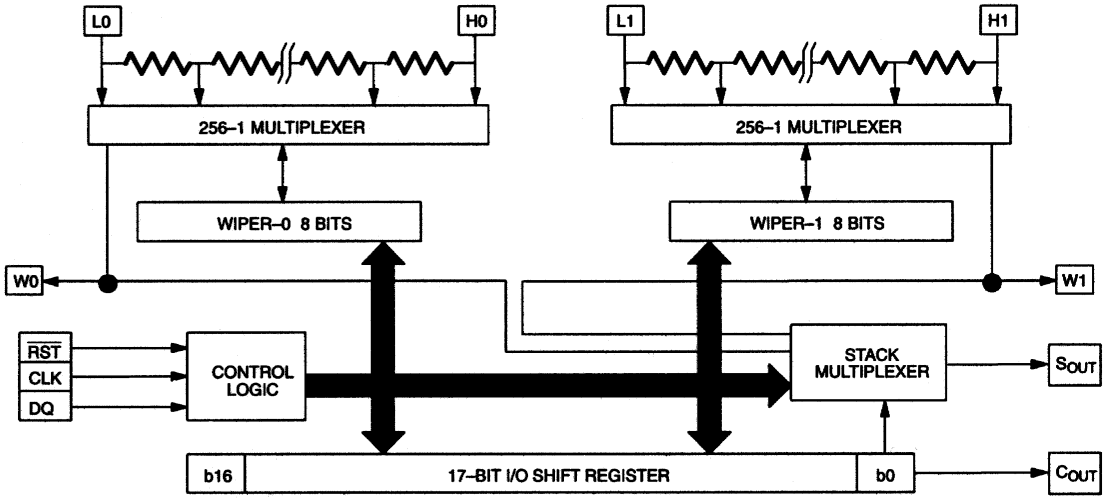
Communication and control of the DS1267 are accomplished through a 3-wire serial port interface that drives an internal control logic unit. The 3-wire serial interface consists of the three input signals: $\overline{RST}$, CLK, and DQ.

The $\overline{RST}$ control signal is used to enable the 3-wire serial port operation of the device. The chip is selected when $\overline{RST}$ is high; $\overline{RST}$ must be high to begin any communication to the DS1267. The CLK signal input is used to provide timing synchronization for data input and output. The DQ signal line is used to transmit potentiometer wiper settings and the stack select bit configuration to the 17-bit I/O shift register of the DS1267.

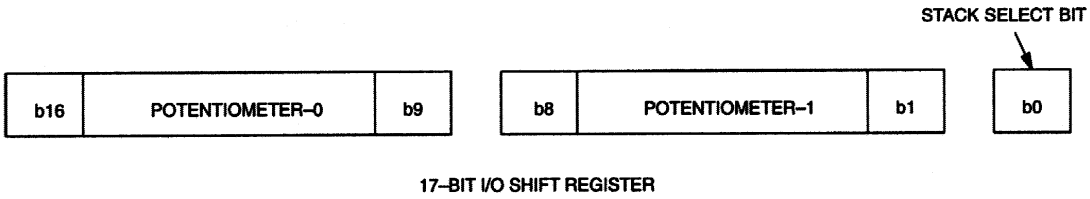
Figure 9(a) presents the 3-wire serial port protocol. As shown, the 3-wire port is inactive when the $\overline{RST}$ signal input is low. Communication with the DS1267 requires the transition of the $\overline{RST}$ input from a low state to a high state. Once the 3-wire port has been activated, data is entered into the part on the low to high transition of the CLK signal inputs. Three-wire serial timing requirements are provided in the timing diagrams of Figure 9(b)-(c).

Data written to the DS1267 over the 3-wire serial interface is stored in the 17-bit I/O shift register (see Figure 2). The 17-bit I/O shift register contains both 8-bit potentiometer wiper position values and the stack select bit. The composition of the I/O shift register is presented in Figure 2. Bit 0 of the I/O shift register contains the stack select bit, which will be discussed in the section entitled "Stacked Configuration." Bits 1 through 8 of the I/O shift register contain the potentiometer-1 wiper position value. Bit 1 contains the MSB of the wiper setting for potentiometer-1 and bit 8 the LSB for the wiper setting. Bits 9 through 16 of the I/O shift register contain the value of the potentiometer-0 wiper position, with the MSB for the wiper position occupying bit 9 and the LSB bit 16.

DS1267 BLOCK DIAGRAM Figure 1



I/O SHIFT REGISTER Figure 2



Transmission of data always begins with the stack select bit followed by the potentiometer-1 wiper position value and lastly the potentiometer-0 wiper position value.

When wiper position data is to be written to the DS1267, 17 bits (or some integer multiple) of data should always be transmitted. Transactions which do not send a complete 17-bits (or multiple) will leave the register incomplete and possibly an error in the desired wiper positions.

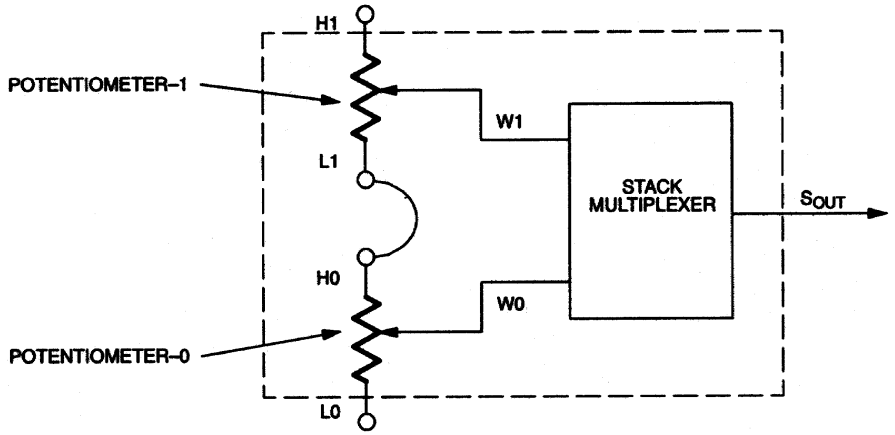
After a communication transaction has been completed, the $\overline{RST}$ signal input should be taken to a low state to prevent any inadvertent changes to the device shift register. Once $\overline{RST}$ has reached a low state, the contents of the I/O shift register are loaded into the respective multiplexers for setting wiper position. A new wiper position will only engage after a $\overline{RST}$ transition to the inactive state. On device power-up the DS1267 wiper positions will be set at 50% of the total resistance or binary value 1000 0000.

STACKED CONFIGURATION

The potentiometers of the DS1267 can be connected in series as shown in Figure 3. This is referred to as the stacked configuration. The stacked configuration allows the user to double the total end-to-end resistance of the part and the number of steps to 512 (or 9 bits of resolution).

The wiper output for the combined stacked potentiometer will be taken at the S_{OUT} pin, which is the multiplexed output of the wiper of potentiometer-0 (W0) or potentiometer-1 (W1). The potentiometer wiper selected at the S_{OUT} output is governed by the setting of the stack select bit (bit 0) of the 17-bit I/O shift register. If the stack select bit has value 0, the multiplexed output, S_{OUT}, will be that of the potentiometer-0 wiper. If the stack select bit has value 1, the multiplexed output, S_{OUT}, will be that of the potentiometer-1 wiper.

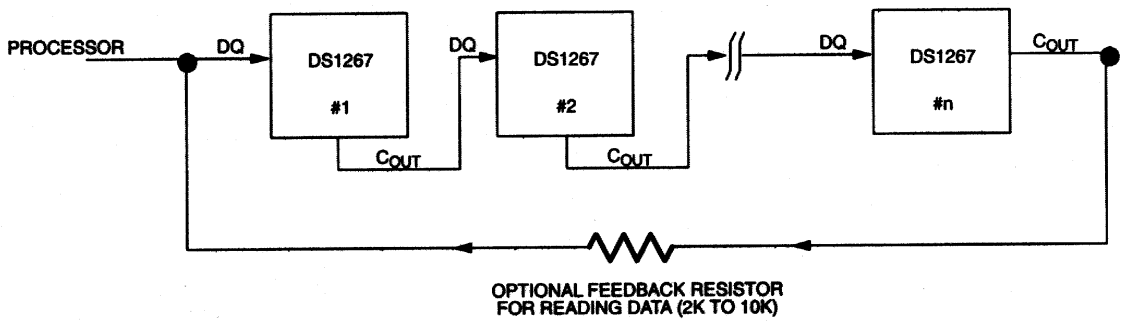
STACKED CONFIGURATION Figure 3



CASCADE OPERATION

A feature of the DS1267 is the ability to control multiple devices from a single processor. Multiple DS1267s can be linked or daisy-chained as shown in Figure 4. As a data bit is entered into the I/O shift register of the DS1267 a bit will appear at the C_{OUT} output within a maximum delay of 50 nanoseconds. The stack select bit of the DS1267 will always be the first out the part at the beginning of a transaction. Additionally the C_{OUT} pin is always active regardless of the state of $\overline{RST}$. This allows one to read the I/O shift register without changing its value.

CASCADING MULTIPLE DEVICES Figure 4



The C_{OUT} output of the DS1267 can be used to drive the DQ input of another DS1267. When connecting multiple devices, the total number of bits transmitted is always 17 times the number of DS1267s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the first DS1267 DQ input, thus allowing the controlling processor to read as well as write data or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 1 to 10 kohms.

When reading data via the C_{OUT} pin and isolation resistor, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the C_{OUT} pin, which is fed back to the input DQ pin through the isolation resistor. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on C_{OUT} and DQ of the next device. After 17 bits (or 17 times the number of DS1267s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper-0, wiper-1, and stack select bit I/O register.

ABSOLUTE AND RELATIVE LINEARITY

Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Figure 5 presents the test circuit used to measure absolute linearity. Absolute linearity is given in terms of a minimum increment or expected output when the wiper is moved one position. In the case of the test circuit, a minimum increment (MI) or one LSB would equal 10/512 volts. The equation for absolute linearity is given as follows:

(1) ABSOLUTE LINEARITY

$$AL=\{V_O \text{ (actual)} - V_O \text{ (expected)}\}/MI$$

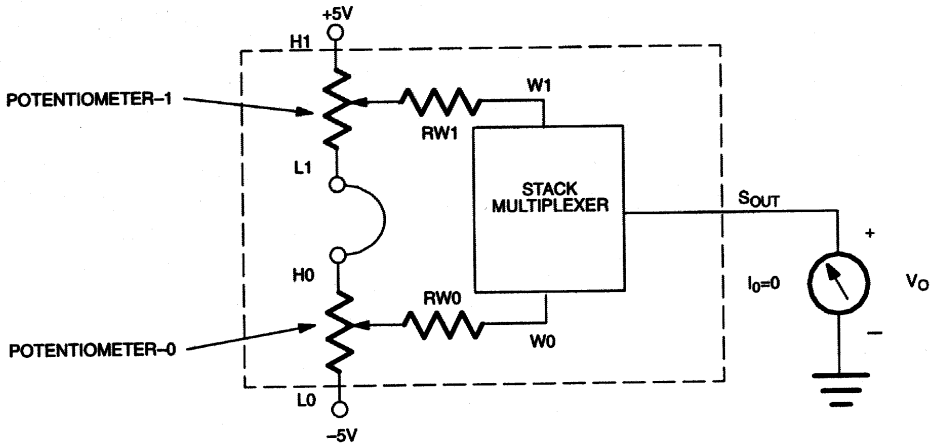
Relative Linearity is a measure of error between two adjacent wiper position points and is given in terms of MI by equation (2).

(2) RELATIVE LINEARITY

$$RL=\{V_O (n+1) - V_O (n)\}/MI$$

Figure 6 is a plot of absolute linearity and relative linearity versus wiper position for the DS1267 at 25°C. The specification for absolute linearity of the DS1267 is ±0.75 MI typical. The specification for relative linearity of the DS1267 is ±0.3 MI typical.

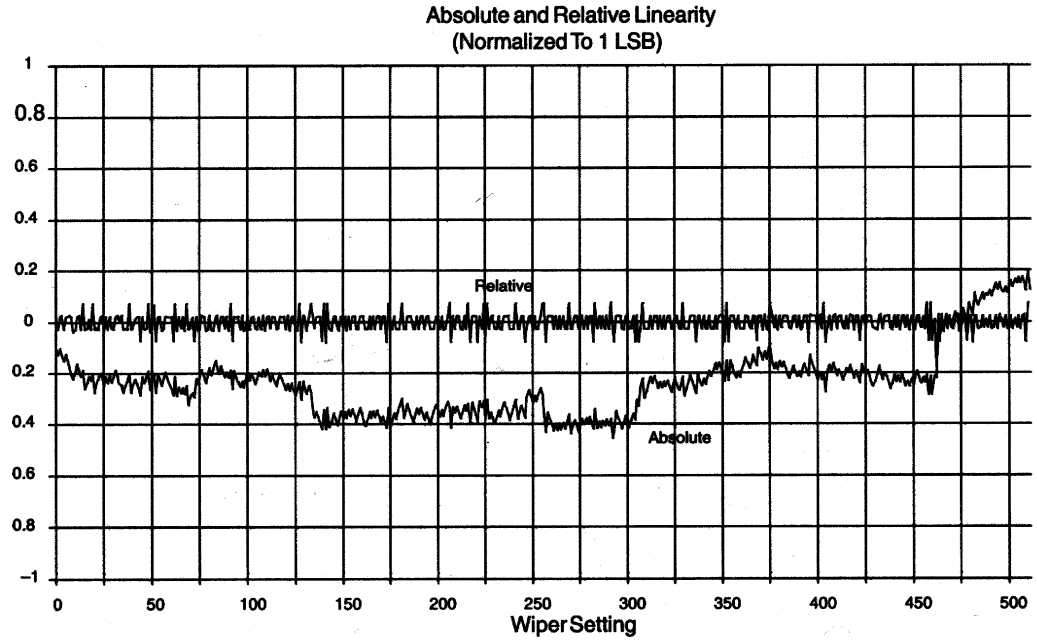
LINEARITY MEASUREMENT CONFIGURATION Figure 5



NOTE:

In this setup, a ±2% delta in total resistance R0 to R1 would cause a ±2.5 MI error.

DS1267 ABSOLUTE AND RELATIVE LINEARITY Figure 6



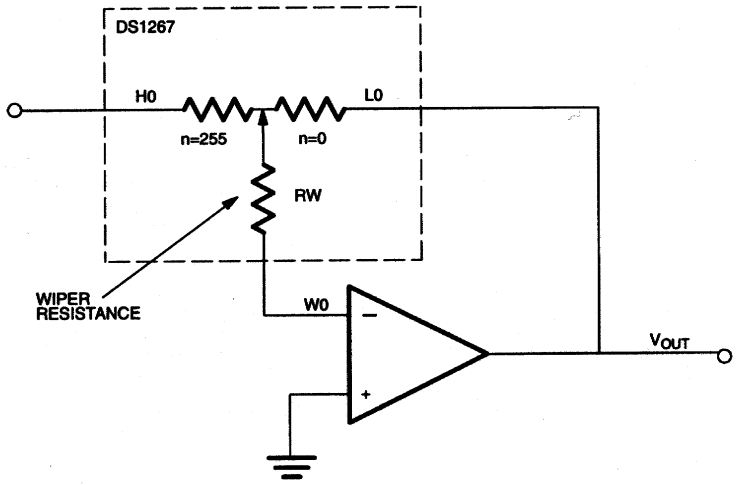
TYPICAL APPLICATION CONFIGURATIONS

Figures 7 and 8 show two typical application configurations for theDS1267. By connecting the wiper terminal of the part to a high-impedance load, the effects of the wiper resistance is minimized, since the wiper resistance can vary from 400 to 1000ohms depending on wiper voltage. Figure 7 presents the device connected in an inverting variable gain amplifier. The gain of the circuit on Figure 7 is given by the following equation:

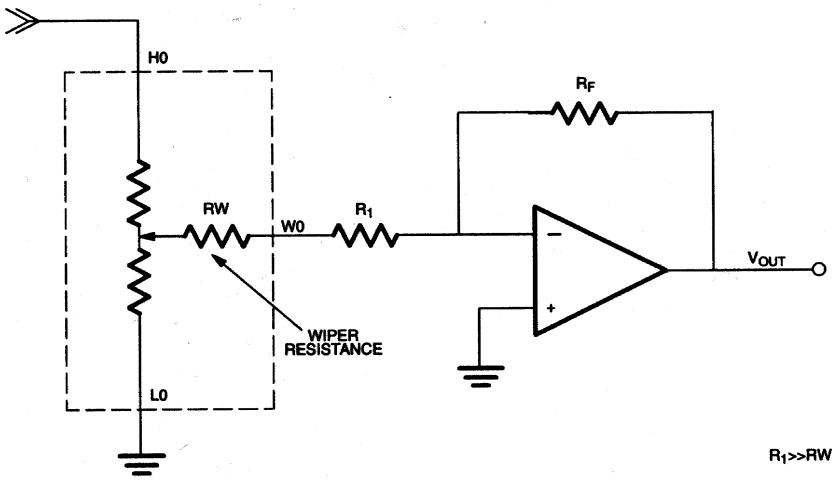
$$Av = -n/(255-n); \text{ where } n = 0 \text{ to } 255$$

Figure 8 shows the device operating in a fixed gain attenuator where the potentiometer is used to attenuate an incoming signal. Note the resistance R1 is chosen to be much greater than the wiper resistance to minimize its effect on circuit gain.

INVERTING VARIABLE GAIN AMPLIFIER Figure 7



FIX GAIN ATTENUATOR Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (VB=GND)	-0.1V to +7.0V
Voltage on Resistor Pins when VB=-5.5V	-5.5V to +7.0V
Voltage on V_B	-5.5V to GND
Operating Temperature	-40° to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C; V_{CC}=5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5		5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8	V	1
Substrate Bias	V_B	-5.5		GND	V	1
Resistor Inputs	L,H,W	V_B-0.5		V_{CC}+0.5	V	2

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		22	650	µA	9
Input Leakage	I_{LI}	-1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	5
Wiper Current	I_W			1	mA	
Output Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output @ 2.4V	I_{OH}	-1			mA	7
Logic 0 Output @ 0.4V	I_{OL}			4	mA	7
Standby Current	I_{STBY}		22		µA	5

ANALOG RESISTOR CHARACTERISTICS (-40°C to +85°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End-to-End Resistor Tolerance		-20		+20	%	10
Absolute Linearity			±.75		LDB	3
Relative Linearity			±0.3		LDB	4
-3 dB Cutoff Frequency	F_{CUTOFF}				Hz	6
Temperature Coefficient			750		ppm/C	

CAPACITANCE (T_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	8
Width of CLK Pulse	t_{CH}	50			ns	8
Data Setup Time	t_{DC}	30			ns	8
Data Hold Time	t_{CDH}	10			ns	8
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	8
Propagation Delay Time High to Low Level	t_{PHL}			50	ns	8
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	8
$\overline{RST}$ Low to Clock Input High	t_{HLT}	50			ns	8
$\overline{RST}$ Inactive	t_{RLT}	125			ns	8
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	8

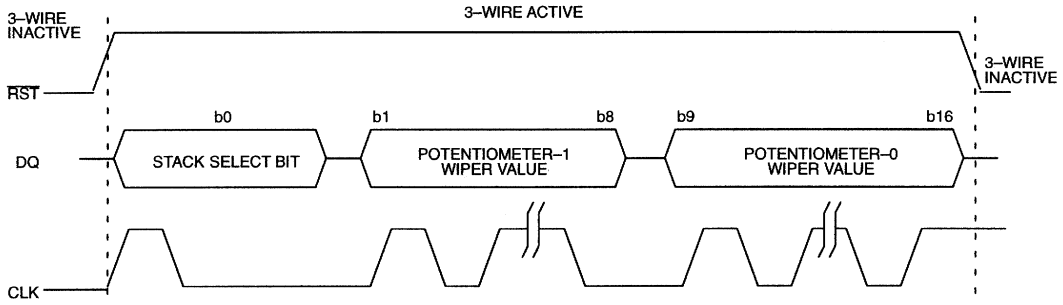
NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage, Vb, in the negative direction.
3. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position. Device test limits ±1.6 LSB.

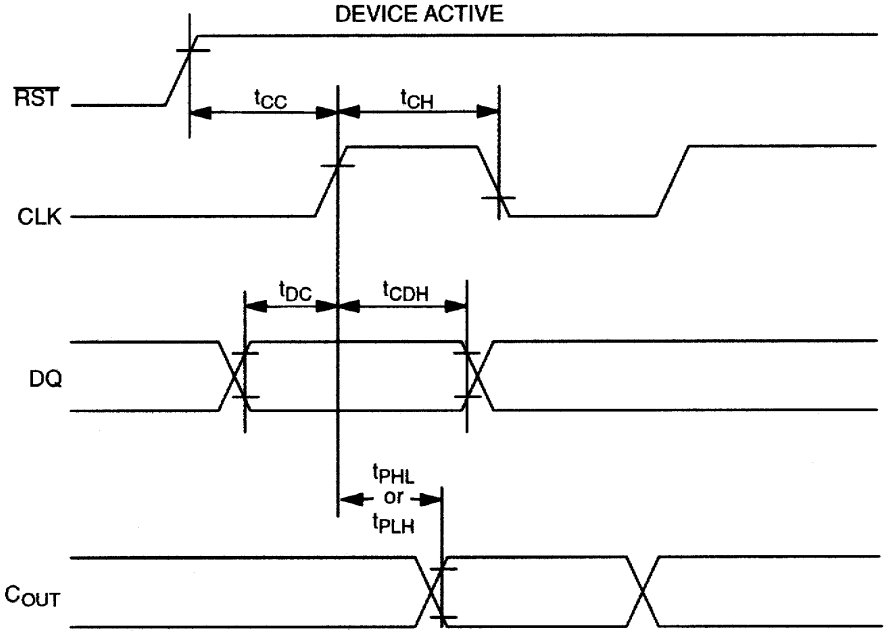
4. Relative linearity is used to determine the change in voltage between successive tap positions. Device test limits ±0.5 LSB.
5. Typical values are for T_A = 25°C and nominal supply voltage.
6. -3 dB cutoff frequency characteristics for the DS1267 depend on potentiometer total resistance: DS1267-010: 1 MHz; DS1267-050: 200 kHz; DS1267-100: 100 kHz.
7. C_{OUT} is active regardless of the state of $\overline{RST}$.
8. See Figure 9(a), (b), and (c).
9. See Figure 11.
10. Valid at 25°C only.

TIMING DIAGRAMS Figure 9

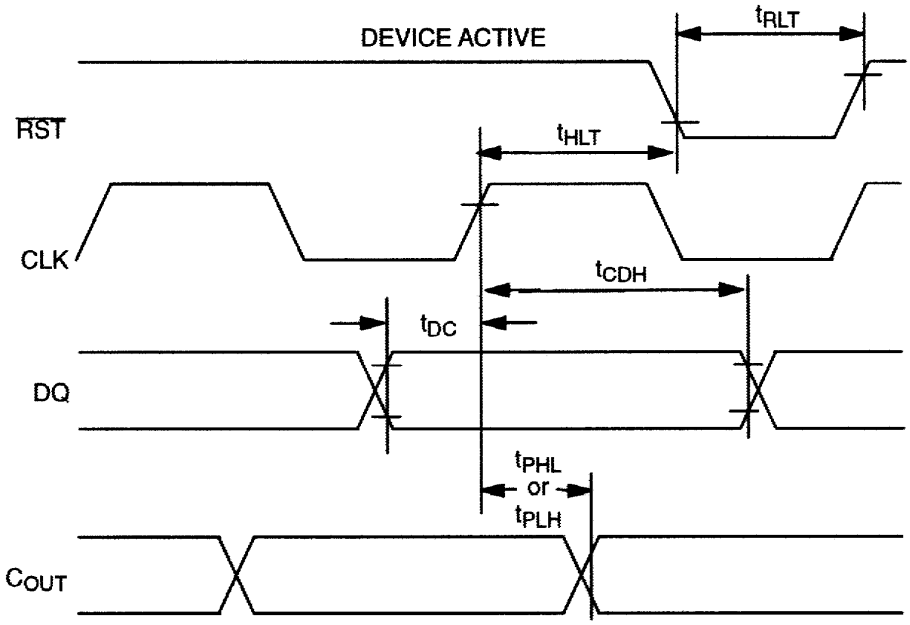
(A) 3-WIRE SERIAL INTERFACE GENERAL OVERVIEW



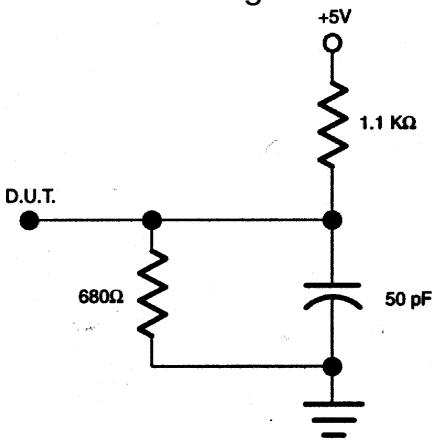
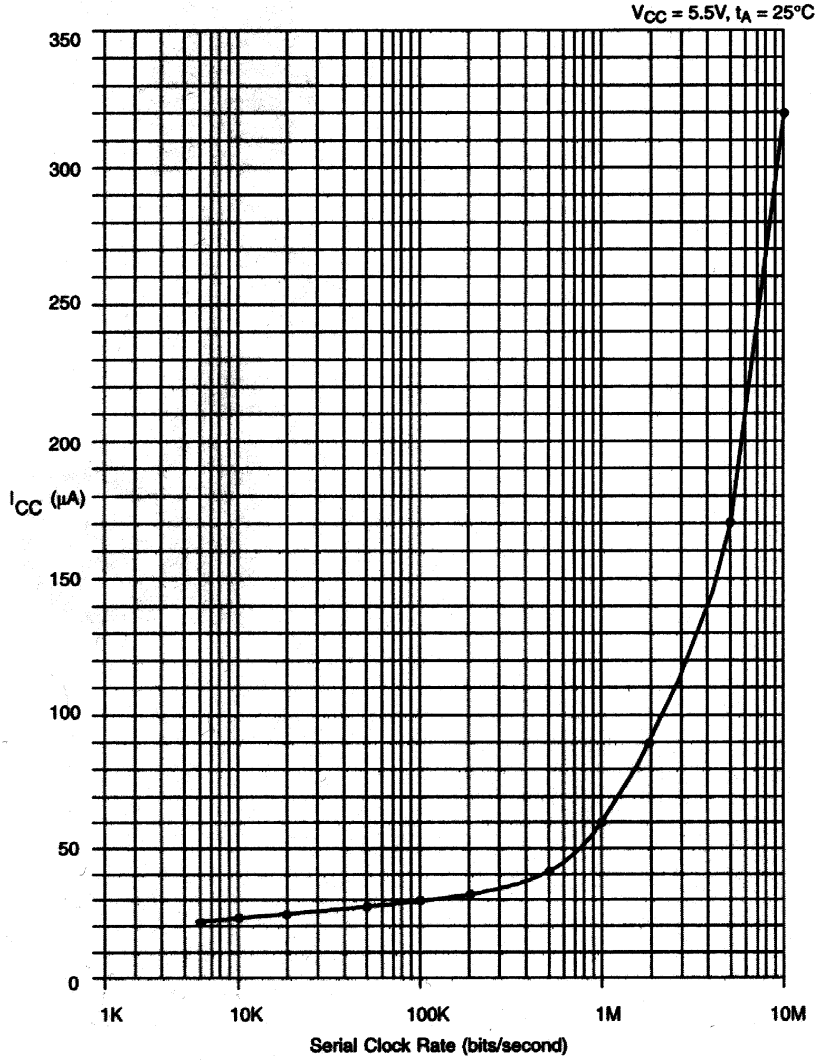
(B) START OF COMMUNICATION TRANSACTION



(C) END OF COMMUNICATION TRANSACTION



DIGITAL OUTPUT LOAD SCHEMATIC Figure 10



TYPICAL SUPPLY CURENT VS. SERIAL CLOCK RATE Figure 11