

2N6487, 2N6488, (NPN) 2N6490, 2N6491 (PNP)

2N6488 and 2N6491 are Preferred Devices

Complementary Silicon Plastic Power Transistors

These devices are designed for use in general-purpose amplifier and switching applications.

Features

- DC Current Gain Specified to 15 Amperes -
 $h_{FE} = 20 - 150 @ I_C = 5.0 \text{ Adc}$
 $= 5.0 \text{ (Min)} @ I_C = 15 \text{ Adc}$
- Collector-Emitter Sustaining Voltage -
 $V_{CEO(sus)} = 60 \text{ Vdc (Min)} - 2N6487, 2N6490$
 $= 80 \text{ Vdc (Min)} - 2N6488, 2N6491$
- High Current Gain - Bandwidth Product
 $f_T = 5.0 \text{ MHz (Min)} @ I_C = 1.0 \text{ Adc}$
- TO-220AB Compact Package
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage 2N6487, 2N6490 2N6488, 2N6491	V_{CEO}	60 80	Vdc
Collector-Base Voltage 2N6487, 2N6490 2N6488, 2N6491	V_{CB}	70 90	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current - Continuous	I_C	15	Adc
Base Current	I_B	5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.8 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	70	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

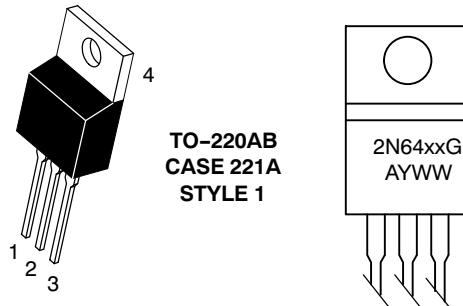


ON Semiconductor®

<http://onsemi.com>

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60-80 VOLTS, 75 WATTS

MARKING DIAGRAM



2N64xx = Specific Device Code
xx = See Table on Page 5
G = Pb-Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 5 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

2N6487, 2N6488, (NPN) 2N6490, 2N6491 (PNP)

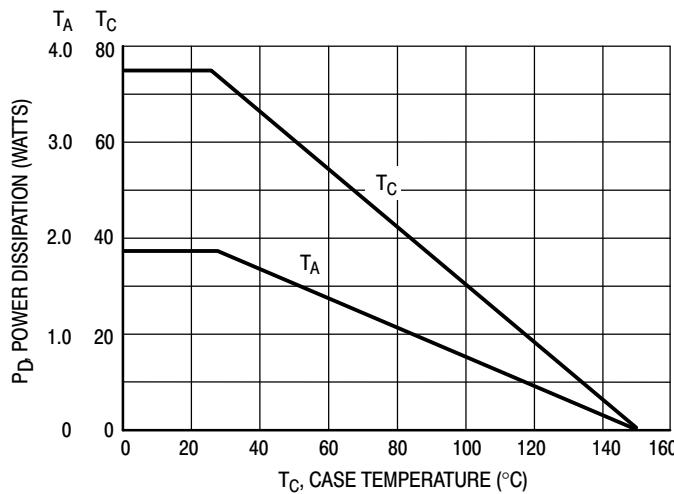


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (Note 3) ($I_C = 200 \text{ mA}_\text{dc}$, $I_B = 0$)	$V_{\text{CEO}(\text{sus})}$	60 80	-	V_dc
Collector-Emitter Sustaining Voltage (Note) ($I_C = 200 \text{ mA}_\text{dc}$, $V_{\text{BE}} = 1.5 \text{ V}_\text{dc}$)	V_{CEX}	70 90	-	V_dc
Collector Cutoff Current ($V_{\text{CE}} = 30 \text{ V}_\text{dc}$, $I_B = 0$) ($V_{\text{CE}} = 40 \text{ V}_\text{dc}$, $I_B = 0$)	I_{CEO}	- -	1.0 1.0	mA_dc
Collector Cutoff Current ($V_{\text{CE}} = 65 \text{ V}_\text{dc}$, $V_{\text{EB}(\text{off})} = 1.5 \text{ V}_\text{dc}$) ($V_{\text{CE}} = 85 \text{ V}_\text{dc}$, $V_{\text{EB}(\text{off})} = 1.5 \text{ V}_\text{dc}$) ($V_{\text{CE}} = 60 \text{ V}_\text{dc}$, $V_{\text{EB}(\text{off})} = 1.5 \text{ V}_\text{dc}$, $T_C = 150^\circ\text{C}$) ($V_{\text{CE}} = 80 \text{ V}_\text{dc}$, $V_{\text{EB}(\text{off})} = 1.5 \text{ V}_\text{dc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	- - - -	500 500 5.0 5.0	μA_dc
Emitter Cutoff Current ($V_{\text{BE}} = 5.0 \text{ V}_\text{dc}$, $I_C = 0$)	I_{EBO}	-	1.0	mA_dc

ON CHARACTERISTICS

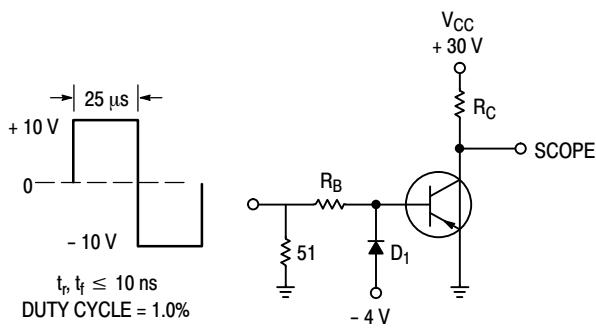
DC Current Gain ($I_C = 5.0 \text{ Adc}$, $V_{\text{CE}} = 4.0 \text{ Vdc}$) ($I_C = 15 \text{ Adc}$, $V_{\text{CE}} = 4.0 \text{ Vdc}$)	h_{FE}	20 5.0	150 -	-
Collector-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}$, $I_B = 0.5 \text{ Adc}$) ($I_C = 15 \text{ Adc}$, $I_B = 5.0 \text{ Adc}$)	$V_{\text{CE}(\text{sat})}$	- -	1.3 3.5	V_dc
Base-Emitter On Voltage ($I_C = 5.0 \text{ Adc}$, $V_{\text{CE}} = 4.0 \text{ Vdc}$) ($I_C = 15 \text{ Adc}$, $V_{\text{CE}} = 4.0 \text{ Vdc}$)	$V_{\text{BE}(\text{on})}$	- -	1.3 3.5	V_dc

DYNAMIC CHARACTERISTICS

Current-Gain - Bandwidth Product (Note 4) ($I_C = 1.0 \text{ Adc}$, $V_{\text{CE}} = 4.0 \text{ Vdc}$, $f_{\text{test}} = 1.0 \text{ MHz}$)	f_T	5.0	-	MHz
Small-Signal Current Gain ($I_C = 1.0 \text{ Adc}$, $V_{\text{CE}} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	25	-	-

2. Indicates JEDEC Registered Data.
3. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
4. $f_T = |h_{\text{fe}}| \cdot f_{\text{test}}$

2N6487, 2N6488, (NPN) 2N6490, 2N6491 (PNP)



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS.
FOR PNP, REVERSE ALL POLARITIES.

D_1 MUST BE FAST RECOVERY TYPE, e.g.:

1N5825 USED ABOVE $I_B \approx 100 \text{ mA}$

MSD6100 USED BELOW $I_B \approx 100 \text{ mA}$

Figure 2. Switching Time Test Circuit

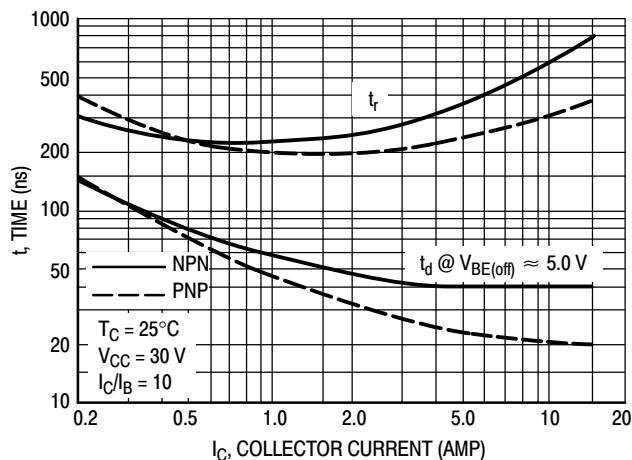


Figure 3. Turn-On Time

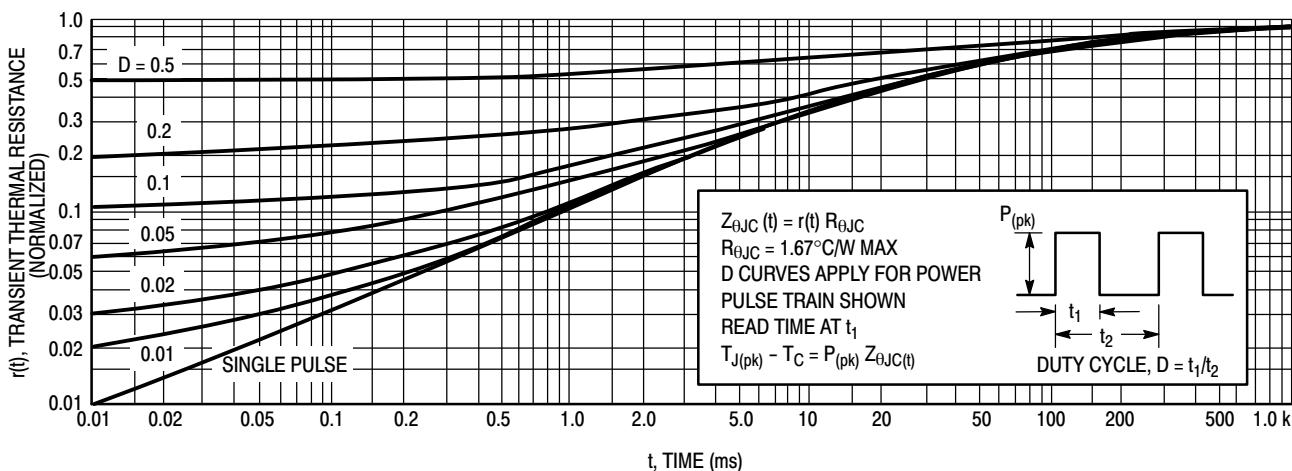


Figure 4. Thermal Response

2N6487, 2N6488, (NPN) 2N6490, 2N6491 (PNP)

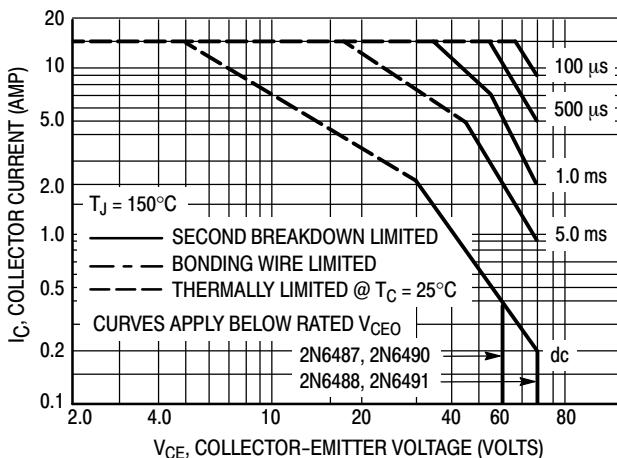


Figure 5. Active-Region Safe Operating Area

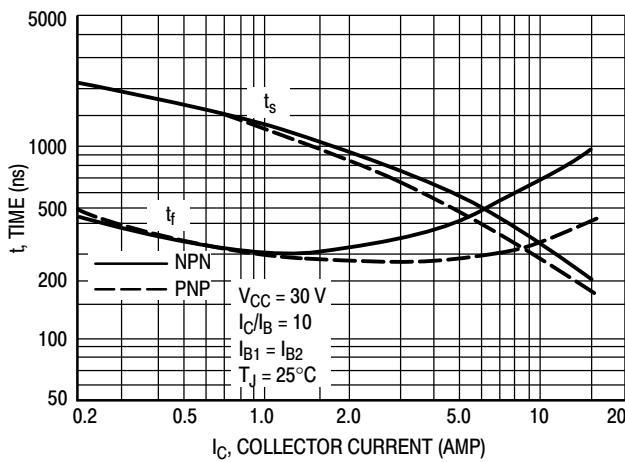


Figure 6. Turn-Off Time

There are two limitations on the power handling ability of a transistors average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

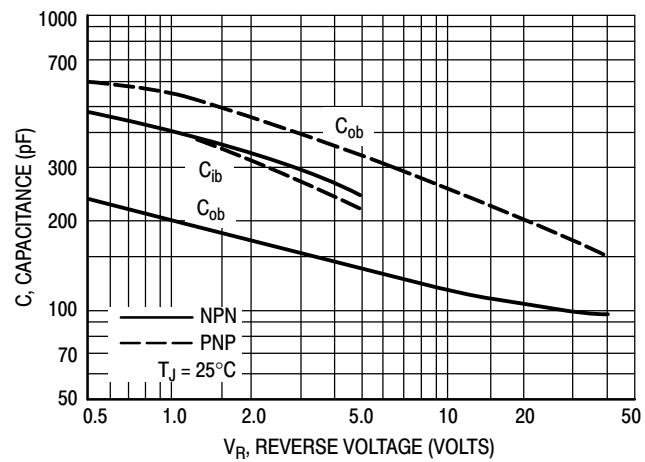


Figure 7. Capacitances

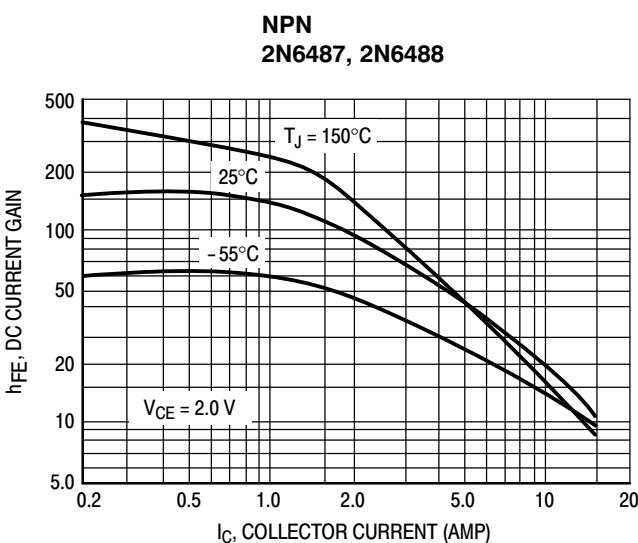
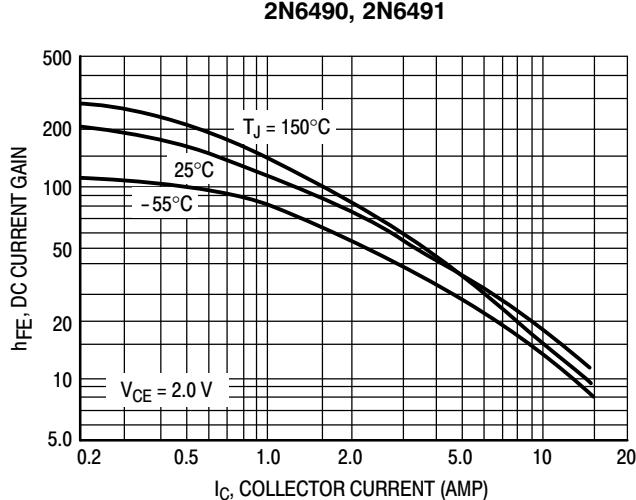


Figure 8. DC Current Gain



2N6487, 2N6488, (NPN) 2N6490, 2N6491 (PNP)

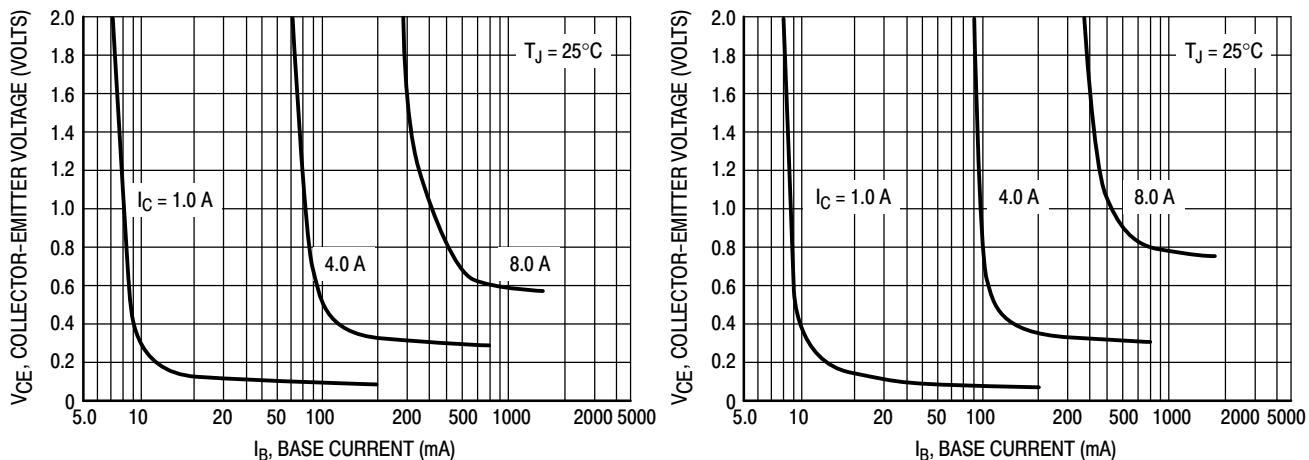


Figure 9. Collector Saturation Region

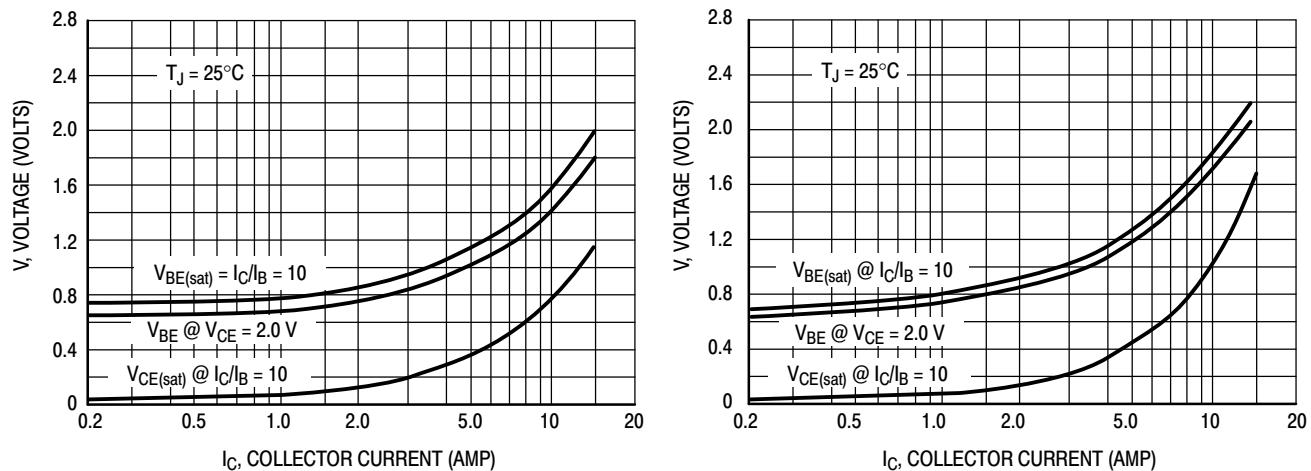
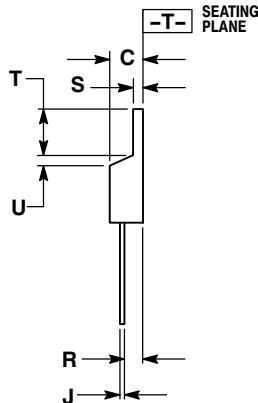
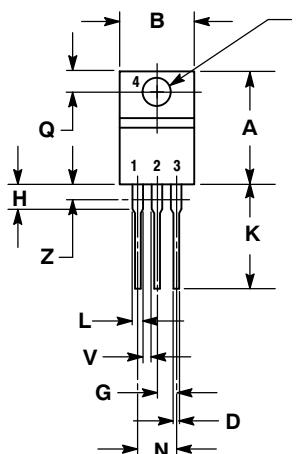


Figure 10. "On" Voltages

ORDERING INFORMATION

Device	Device Marking	Package	Shipping
2N6487	2N6487	TO-220AB	50 Units / Rail
2N6487G		TO-220AB (Pb-Free)	
2N6488	2N6488	TO-220AB	50 Units / Rail
2N6488G		TO-220AB (Pb-Free)	
2N6490	2N6490	TO-220AB	50 Units / Rail
2N6490G		TO-220AB (Pb-Free)	
2N6491	2N6491	TO-220AB	50 Units / Rail
2N6491G		TO-220AB (Pb-Free)	

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AE

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

USA/Canada

Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910

Japan Customer Focus Center

Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative