

# SN54ALS804A, SN54AS804B, SN74ALS804A, SN74AS804B HEX 2-INPUT NAND DRIVERS

SDAS022C – DECEMBER 1982 – REVISED JANUARY 1995

- **High Capacitive-Drive Capability**
- 'ALS804A Has Typical Delay Time of 4 ns ( $C_L = 50 \text{ pF}$ ) and Typical Power Dissipation of 3.4 mW Per Gate
- 'AS804B Has Typical Delay Time of 2.6 ns ( $C_L = 50 \text{ pF}$ ) and Typical Power Dissipation of Less Than 9 mW Per Gate
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

## description

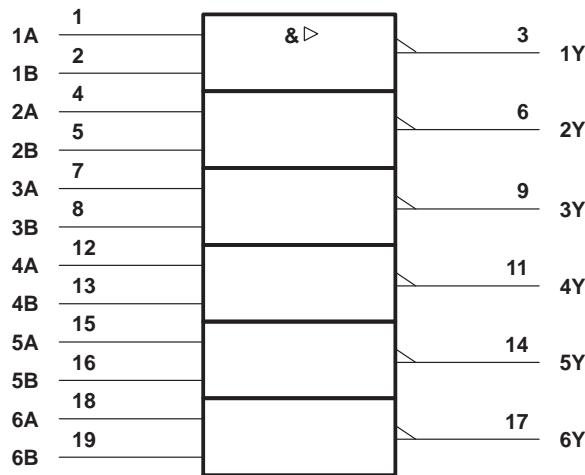
These devices contain six independent 2-input NAND drivers. They perform the Boolean functions  $Y = A \bullet B$  or  $Y = \bar{A} + \bar{B}$  in positive logic.

The SN54ALS804A and SN54AS804B are characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ALS804A and SN74AS804B are characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

FUNCTION TABLE  
(each driver)

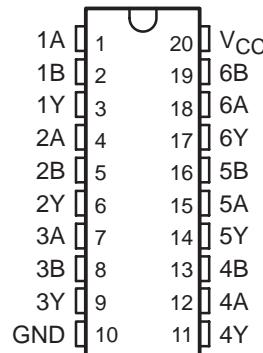
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

## logic symbol†

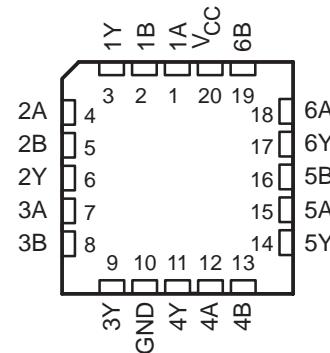


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

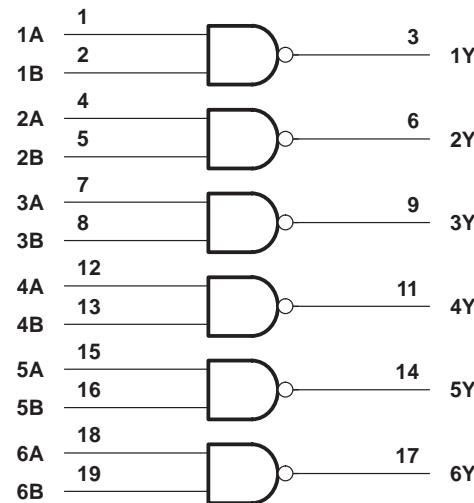
SN54ALS804A, SN54AS804B . . . J PACKAGE  
SN74ALS804A, SN74AS804B . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS804A, SN54AS804B . . . FK PACKAGE  
(TOP VIEW)



## logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# **SN54ALS804A, SN54AS804B, SN74ALS804A, SN74AS804B HEX 2-INPUT NAND DRIVERS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## **recommended operating conditions**

		SN54ALS804A			SN74ALS804A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			12			24	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS804A			SN74ALS804A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -0.4 mA	V <sub>CC</sub> - 2		V <sub>CC</sub> - 2			V
	I <sub>OH</sub> = -3 mA	2.4	3.2	2.4	3.2			
	I <sub>OH</sub> = -12 mA	2						
	I <sub>OH</sub> = -15 mA			2				
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4		V
		I <sub>OL</sub> = 24 mA			0.35	0.5		
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V		0.1		0.1	mA	
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V		20		20	µA	
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V		-0.1		-0.1	mA	
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-20	-112	-30	-112	mA	
I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0	0.9	2.5	0.9	2.5	mA	
I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 4.5 V	7	12	7	12	mA	

<sup>‡</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

# **SN54ALS804A, SN54AS804B, SN74ALS804A, SN74AS804B HEX 2-INPUT NAND DRIVERS**

SDAS022C – DECEMBER 1982 – REVISED JANUARY 1995

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R_L = 500\text{ }\Omega,$ $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54ALS804A		SN74ALS804A			
			MIN	MAX	MIN	MAX		
$t_{PLH}$	A or B	Y	2	9	2	7	ns	
$t_{PHL}$			2	9	2	8		

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### **recommended operating conditions§**

		SN54AS804B			SN74AS804B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-40			-48	mA
I <sub>OL</sub>	Low-level output current			40			48	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

§ These high sink- or source-current devices are not recommended for use above 40 MHz.

# SN54ALS804A, SN54AS804B, SN74ALS804A, SN74AS804B HEX 2-INPUT NAND DRIVERS

SDAS022C – DECEMBER 1982 – REVISED JANUARY 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54AS804B			SN74AS804B			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -40 \text{ mA}$	2					
		$I_{OH} = -48 \text{ mA}$				2		
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 40 \text{ mA}$	0.25	0.5				V
		$I_{OL} = 48 \text{ mA}$			0.35	0.5		
$I_I$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 7 \text{ V}$		0.1		0.1		mA	
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$			20		20	$\mu\text{A}$	
$I_{IL}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0.4 \text{ V}$			-0.5		-0.5	mA	
$I_O^{\ddagger}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 2.25 \text{ V}$	-50	-200	-50	-200		mA	
$I_{CCH}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0$		3.5	5	3.5	5	mA	
$I_{CCL}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 4.5 \text{ V}$	16	27	16	27		mA	

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

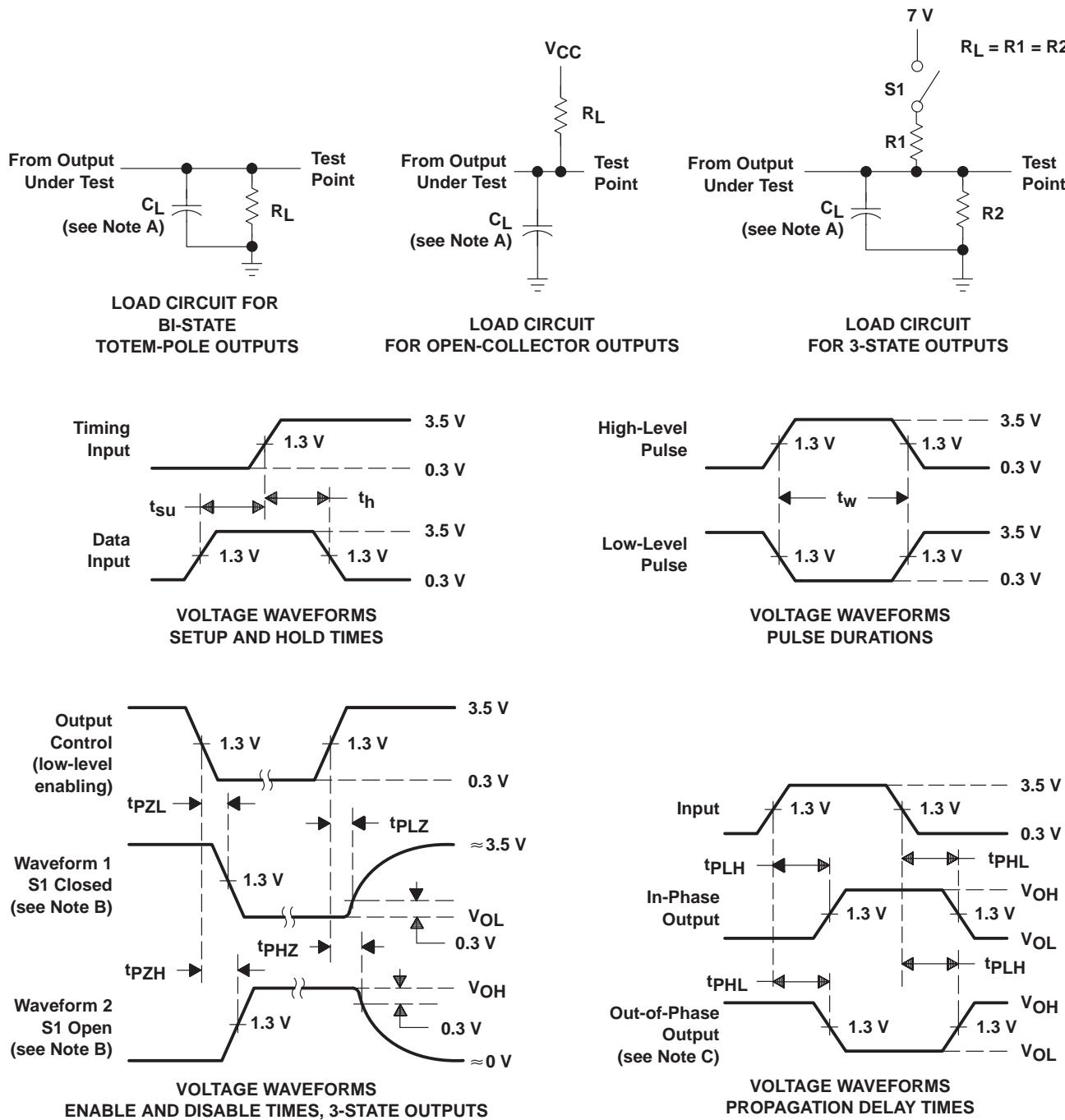
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , $T_A = \text{MIN to MAX}^{\$}$				UNIT	
			SN54AS804B		SN74AS804B			
			MIN	MAX	MIN	MAX		
$t_{PLH}$	A or B	Y	1	5	1	4	ns	
$t_{PHL}$			1	5	1	4		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $t_r = t_f = 2 \text{ ns}$ , duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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**PACKAGING INFORMATION**


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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-87766012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	<a href="#">Purchase Samples</a>
5962-8776601RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	<a href="#">Purchase Samples</a>
5962-8776601SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	<a href="#">Purchase Samples</a>
5962-88693012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	<a href="#">Purchase Samples</a>
5962-8869301RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SN54ALS804AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SN54AS804BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SN74ALS804ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN74ALS804ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN74ALS804ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN74ALS804AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SN74ALS804ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SN74AS804BDW	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
SN74AS804BDWE4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
SN74AS804BDWG4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
SN74AS804BDWR	NRND	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
SN74AS804BDWRE4	NRND	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
SN74AS804BDWRG4	NRND	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
SN74AS804BN	NRND	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Samples Not Available
SN74AS804BNE4	NRND	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Samples Not Available
SNJ54ALS804AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SNJ54ALS804AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SNJ54AS804BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	<a href="#">Purchase Samples</a>

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SNJ54AS804BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SNJ54AS804BW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	<a href="#">Purchase Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54ALS804A, SN54AS804B, SN74ALS804A, SN74AS804B :

- Catalog: [SN74ALS804A](#), [SN74AS804B](#)
- Military: [SN54ALS804A](#), [SN54AS804B](#)

NOTE: Qualified Version Definitions:



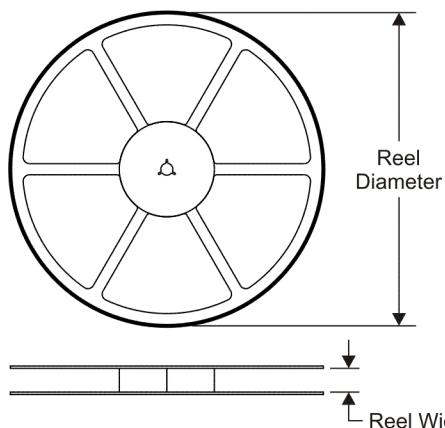
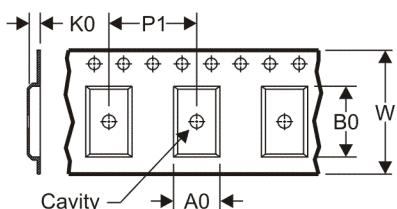
www.ti.com

## PACKAGE OPTION ADDENDUM

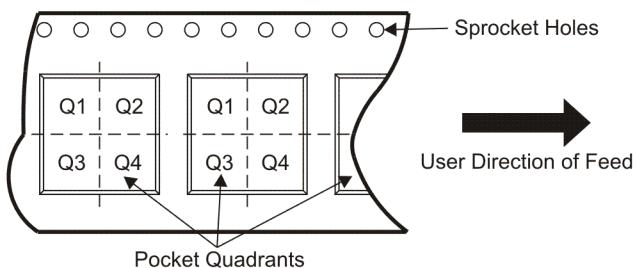
28-Aug-2010

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- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS804BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AS804BDWR	SOIC	DW	20	2000	346.0	346.0	41.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

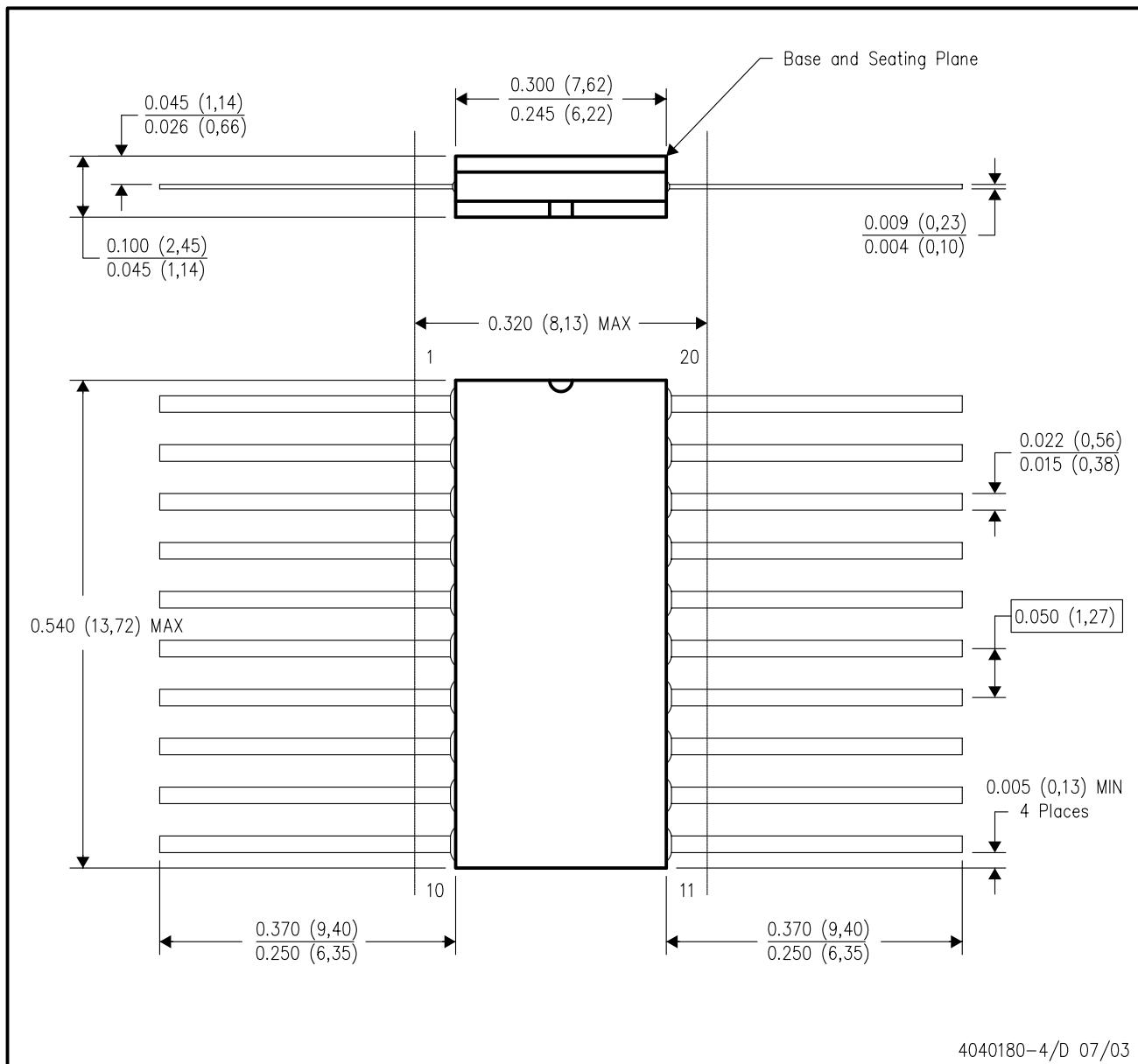


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

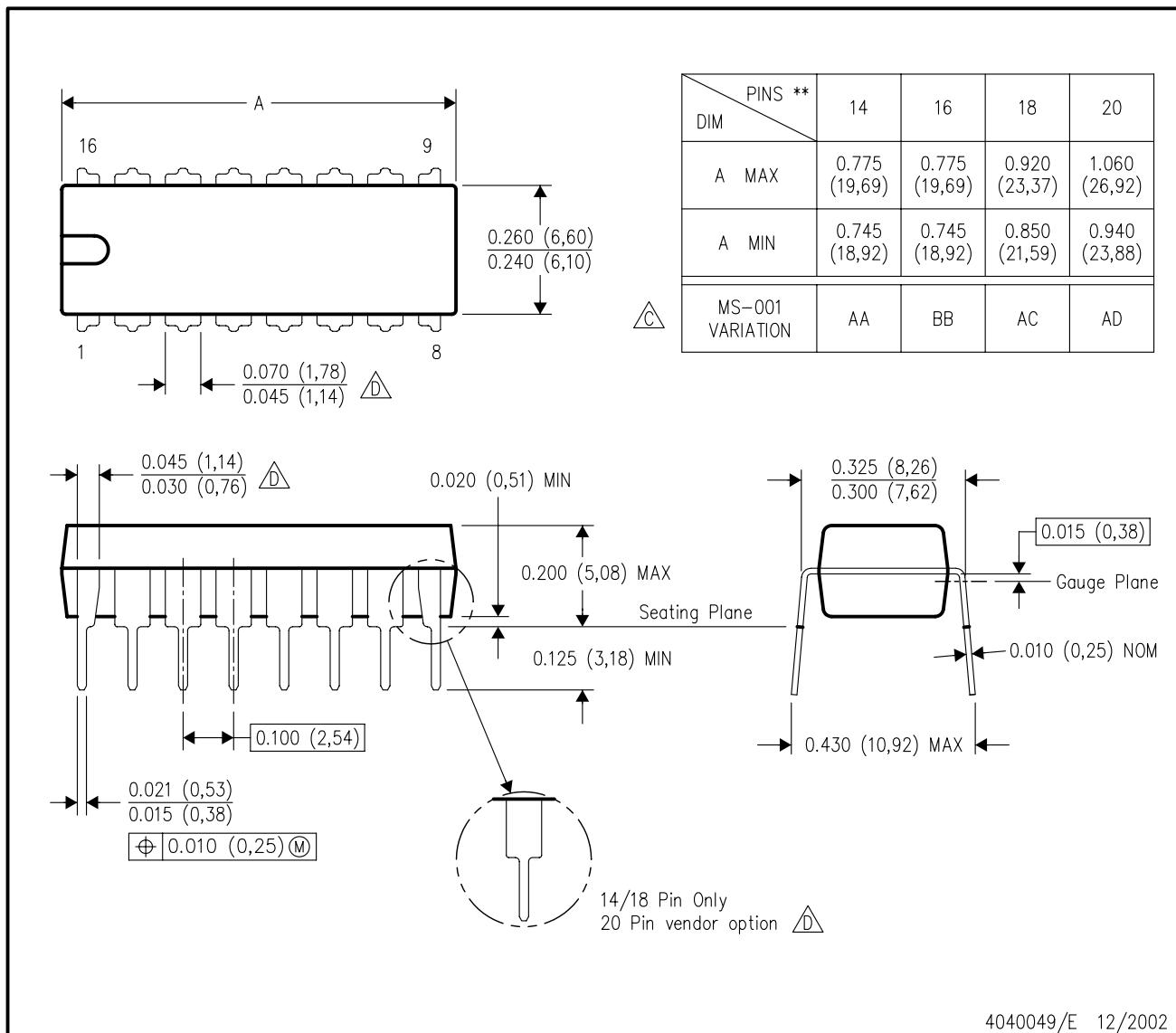
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

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## N (R-PDIP-T\*\*)

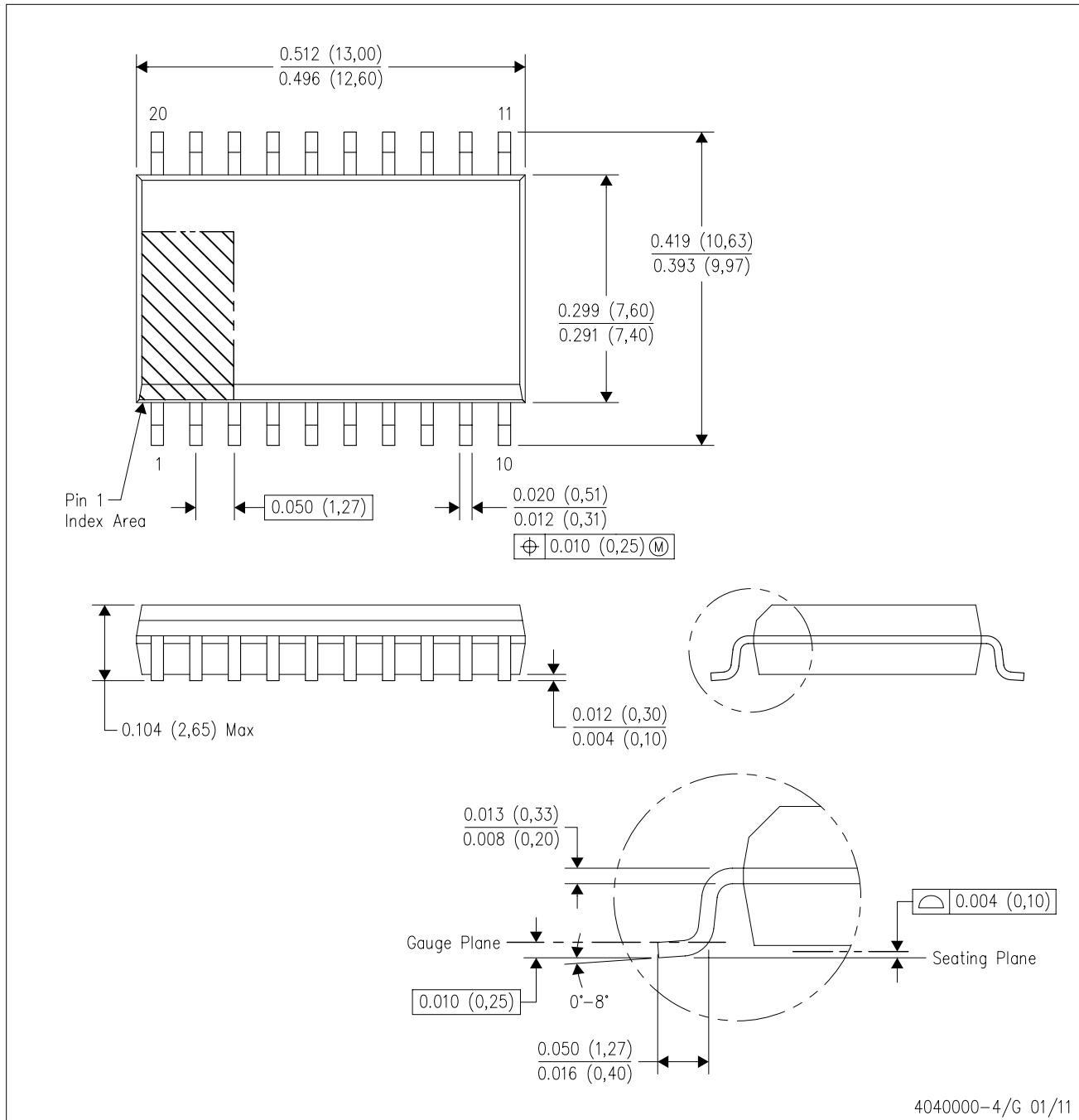
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

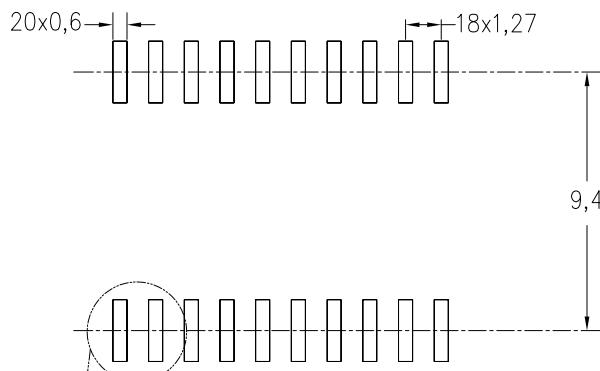
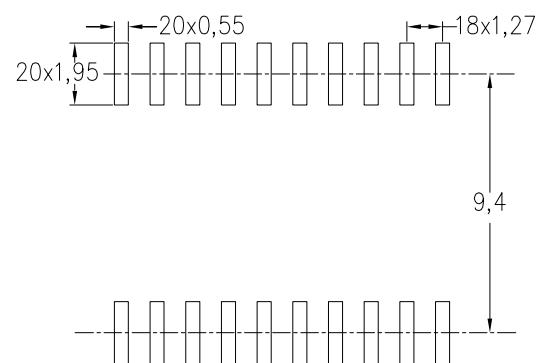


NOTES:

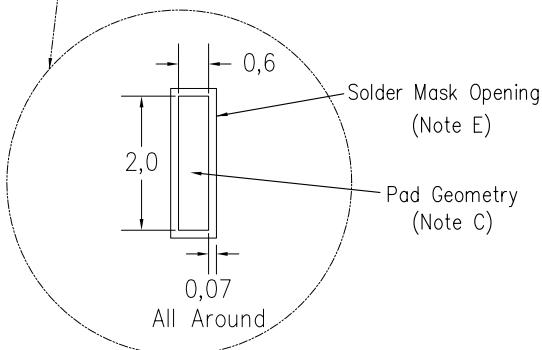
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



4209202-4/E 07/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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