

## CMOS 8-Stage Static Shift Registers

High-Voltage Types (20-Volt Rating)

**CD4014B:**

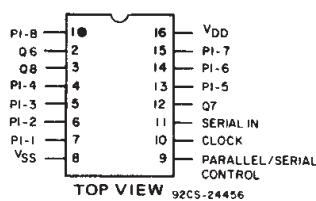
 Synchronous Parallel or  
 Serial Input/Serial Output

**CD4021B:**

 Asynchronous Parallel Input or  
 Synchronous Serial Input/Serial Output

■ CD4014B and CD4021B series types are 8-stage parallel- or serial-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the CD4014B. In the CD4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

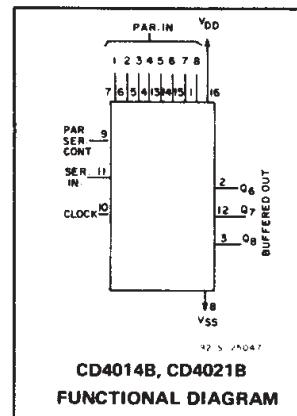
The CD4014B and CD4021B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).


**TERMINAL DIAGRAM**  
**CD4014B, CD4021B**

# CD4014B, CD4021B Types

**Features:**

- Medium-speed operation . . . 12 MHz (typ.) clock rate at  $V_{DD}-V_{SS} = 10$  V
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at  $V_{DD} = 5$  V  
2 V at  $V_{DD} = 10$  V  
2.5 V at  $V_{DD} = 15$  V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"


**Applications:**

- Parallel input/serial output data queueing
- Parallel to serial data conversion
- General-purpose register

**RECOMMENDED OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified**  
*For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.*

| CHARACTERISTIC   | $V_{DD}$<br>(V) | LIMITS |      | UNITS |
|--|-----------------|--------|------|-------|
|  |                 | Min.   | Max. |       |
| Supply-Voltage Range (T <sub>A</sub> = Full Package-Temperature Range) | —               | 3      | 18   | V     |
| Clock Pulse Width, t <sub>W</sub>                                      | 5               | 180    | —    | ns    |
|  | 10              | 80     | —    |       |
|  | 15              | 50     | —    |       |
| Clock Frequency, f <sub>C</sub> L                                      | 5               | —      | 3    | MHz   |
|  | 10              | —      | 6    |       |
|  | 15              | —      | 8.5  |       |
| Clock Rise and Fall Time, t <sub>rCL</sub> , t <sub>fCL</sub>          | 5               | —      | 15   | μs    |
|  | 10              | —      | 15   |       |
|  | 15              | —      | 15   |       |
| Set-up Time, t <sub>s</sub> :  | 5               | 120    | —    | ns    |
|  | 10              | 80     | —    |       |
|  | 15              | 60     | —    |       |
| Parallel Inputs<br>CD4014B<br>(ref. to CL)                             | 5               | 80     | —    | ns    |
|  | 10              | 50     | —    |       |
|  | 15              | 40     | —    |       |
| Parallel Inputs<br>CD4021B<br>(ref. to P/S)                            | 5               | 50     | —    | ns    |
|  | 10              | 30     | —    |       |
|  | 15              | 20     | —    |       |
| Parallel/Serial Control<br>CD4014B<br>(ref. to CL)                     | 5               | 180    | —    | ns    |
|  | 10              | 80     | —    |       |
|  | 15              | 60     | —    |       |
| Parallel/Serial Pulse Width, t <sub>W</sub> (CD4021B)                  | 5               | 160    | —    | ns    |
|  | 10              | 80     | —    |       |
|  | 15              | 50     | —    |       |
| Parallel/Serial Removal Time, t <sub>REM</sub> (CD4021B)               | 5               | 280    | —    | ns    |
|  | 10              | 140    | —    |       |
|  | 15              | 100    | —    |       |

## CD4014B, CD4021B Types

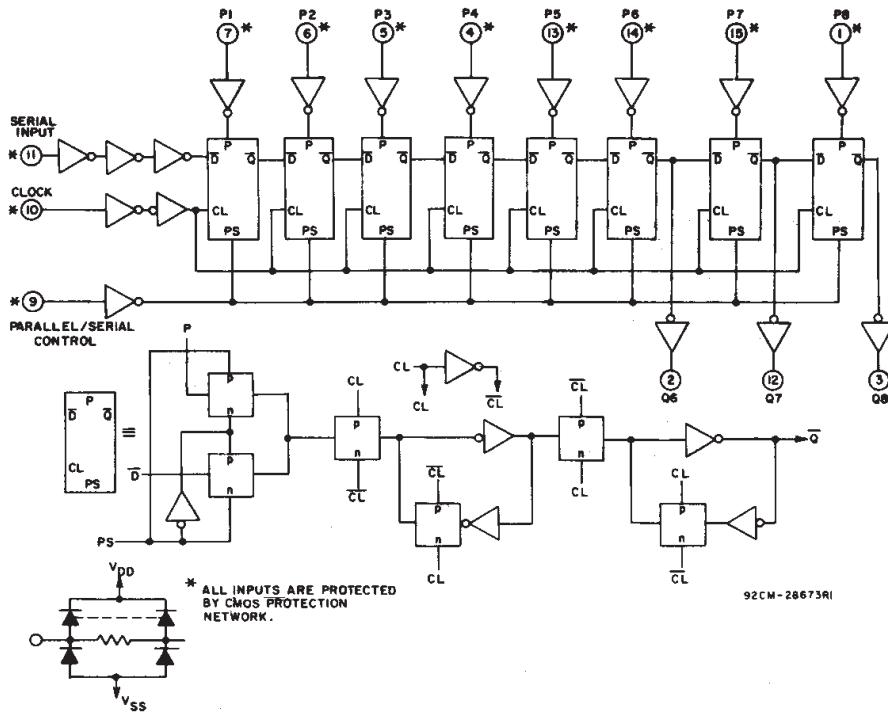


Fig. 1 – Logic diagram for CD4014B.

TRUTH TABLE – CD4014B

| CL | SER IN | PAR SER CONTROL | PI-1 | PI-n | Q <sub>1</sub> (INTERNAL) | Q <sub>n</sub>   |
|----|--------|-----------------|------|------|---------------------------|------------------|
| /  | X      | 1               | 0    | 0    | 0                         | 0                |
| /  | X      | 1               | 1    | 0    | 1                         | 0                |
| /  | X      | 1               | 0    | 1    | 0                         | 1                |
| /  | X      | 1               | 1    | 1    | 1                         | 1                |
| /  | 0      | 0               | X    | X    | 0                         | Q <sub>n-1</sub> |
| /  | 1      | 0               | X    | X    | 1                         | Q <sub>n-1</sub> |
| /  | X      | X               | X    | X    | Q <sub>1</sub>            | Q <sub>n</sub>   |

X = DON'T CARE CASE  
NC = NO CHANGE

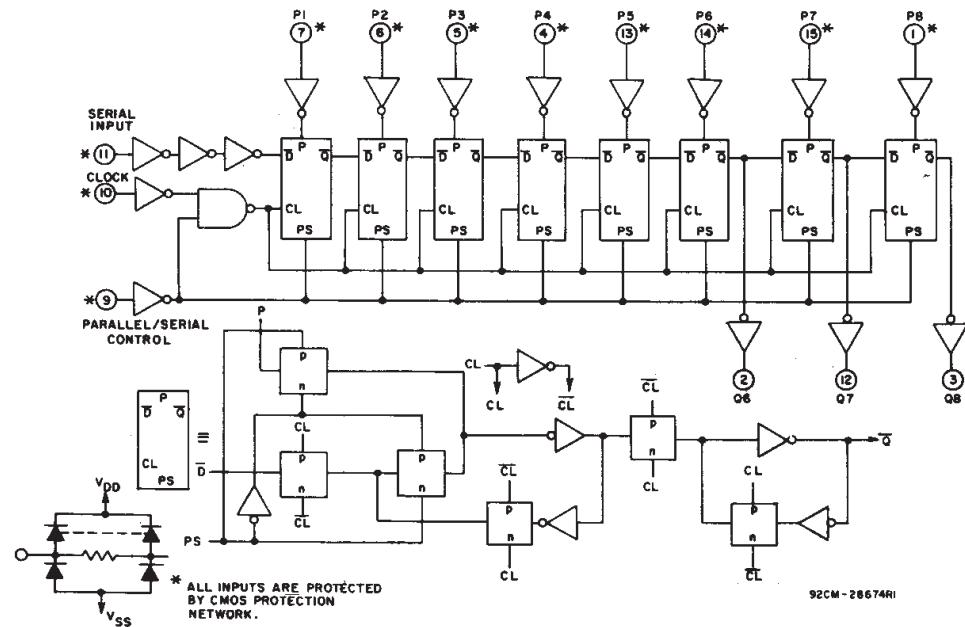


Fig. 2 – Logic diagram for CD4021B.

TRUTH TABLE – CD4021B

| CL | Serial Input | Parallel/Serial Control | PI-1 | PI-n | Q <sub>1</sub> (Internal) | Q <sub>n</sub>   |
|----|--------------|-------------------------|------|------|---------------------------|------------------|
| X  | X            | 1                       | 0    | 0    | 0                         | 0                |
| X  | X            | 1                       | 0    | 1    | 0                         | 1                |
| X  | X            | 1                       | 1    | 0    | 1                         | 0                |
| X  | X            | 1                       | 1    | 1    | 1                         | 1                |
| /  | 0            | 0                       | X    | X    | 0                         | Q <sub>n-1</sub> |
| /  | 1            | 0                       | X    | X    | 1                         | Q <sub>n-1</sub> |
| /  | X            | 0                       | X    | X    | Q <sub>1</sub>            | Q <sub>n</sub>   |

X = DON'T CARE CASE

# CD4014B, CD4021B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD}$  +0.5V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10$ mA

### POWER DISSIPATION PER PACKAGE (PD):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearity at 12mW/ $^\circ\text{C}$  to 200mW

### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) ..... -55 $^\circ\text{C}$  to +125 $^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{Storage}$ ) ..... -65 $^\circ\text{C}$  to +150 $^\circ\text{C}$

### LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch (1.59  $\pm$  0.79mm) from case for 10s max ..... +265 $^\circ\text{C}$

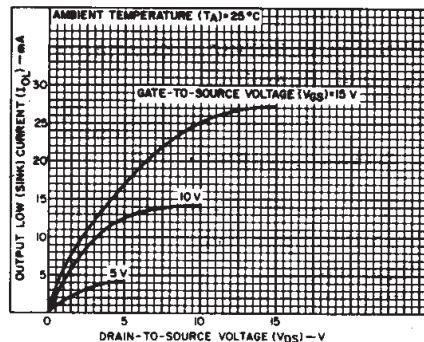


Fig. 3 – Typical output low (sink) current characteristics.

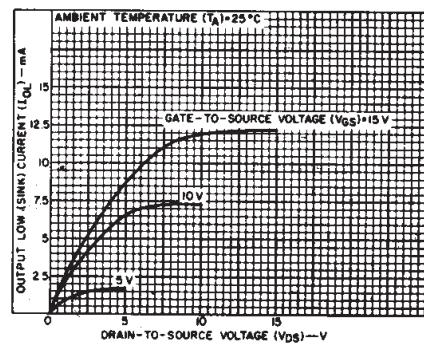


Fig. 4 – Minimum output low (sink) current characteristics.

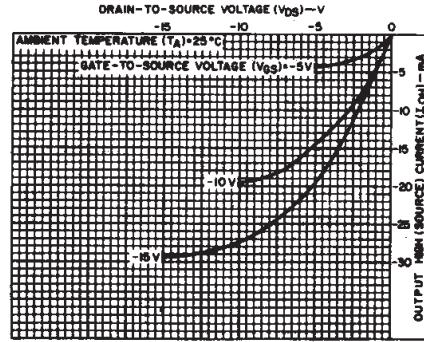


Fig. 5 – Typical output high (source) current characteristics.

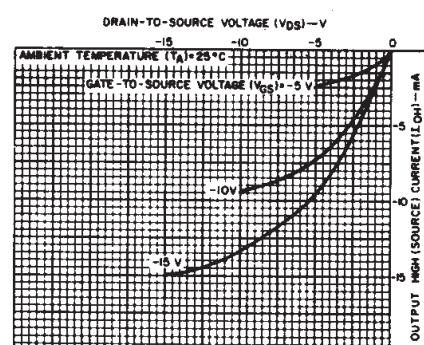


Fig. 6 – Minimum output high (source) current characteristics.

## STATIC ELECTRICAL CHARACTERISTICS

| CHARAC-<br>TERISTIC                                  | CONDITIONS   |                 |                 | LIMITS AT INDICATED TEMPERATURES (°C) |           |         |         |       |               | UNITS     |               |
|--|--------------|-----------------|-----------------|---------------------------------------|-----------|---------|---------|-------|---------------|-----------|---------------|
|  | $V_O$<br>(V) | $V_{IN}$<br>(V) | $V_{DD}$<br>(V) | -55                                   | -40       | +85     | +125    | +25   |               |           |               |
|  |              |                 |                 |                                       |           |         |         | Min.  | Typ.          | Max.      |               |
| Quiescent<br>Device<br>Current,<br>$I_{DD}$ Max.     | –            | 0.5             | 5               | 5                                     | 5         | 150     | 150     | –     | 0.04          | 5         | $\mu\text{A}$ |
|  | –            | 0.10            | 10              | 10                                    | 10        | 300     | 300     | –     | 0.04          | 10        |               |
|  | –            | 0.15            | 15              | 20                                    | 20        | 600     | 600     | –     | 0.04          | 20        |               |
|  | –            | 0.20            | 20              | 100                                   | 100       | 3000    | 3000    | –     | 0.08          | 100       |               |
| Output Low<br>(Sink) Current<br>$I_{OL}$ Min.        | 0.4          | 0.5             | 5               | 0.64                                  | 0.61      | 0.42    | 0.36    | 0.51  | 1             | –         | $\text{mA}$   |
|  | 0.5          | 0.10            | 10              | 1.6                                   | 1.5       | 1.1     | 0.9     | 1.3   | 2.6           | –         |               |
|  | 1.5          | 0.15            | 15              | 4.2                                   | 4         | 2.8     | 2.4     | 3.4   | 6.8           | –         |               |
| Output High<br>(Source)<br>Current,<br>$I_{OH}$ Min. | 4.6          | 0.5             | 5               | -0.64                                 | -0.61     | -0.42   | -0.36   | -0.51 | -1            | –         | $\text{mA}$   |
|  | 2.5          | 0.5             | 5               | -2                                    | -1.8      | -1.3    | -1.15   | -1.6  | -3.2          | –         |               |
|  | 9.5          | 0.10            | 10              | -1.6                                  | -1.5      | -1.1    | -0.9    | -1.3  | -2.6          | –         |               |
|  | 13.5         | 0.15            | 15              | -4.2                                  | -4        | -2.8    | -2.4    | -3.4  | -6.8          | –         |               |
| Output Voltage:<br>Low-Level,<br>$V_{OL}$ Max.       | –            | 0.5             | 5               | 0.05                                  |           |         |         | –     | 0             | 0.05      | $\text{V}$    |
|  | –            | 0.10            | 10              | 0.05                                  |           |         |         | –     | 0             | 0.05      |               |
|  | –            | 0.15            | 15              | 0.05                                  |           |         |         | –     | 0             | 0.05      |               |
| Output<br>Voltage:<br>High-Level,<br>$V_{OH}$ Min.   | –            | 0.5             | 5               | 4.95                                  |           |         |         | 4.95  | 5             | –         | $\text{V}$    |
|  | –            | 0.10            | 10              | 9.95                                  |           |         |         | 9.95  | 10            | –         |               |
|  | –            | 0.15            | 15              | 14.95                                 |           |         |         | 14.95 | 15            | –         |               |
| Input Low<br>Voltage<br>$V_{IL}$ Max.                | 0.5, 4.5     | –               | 5               | 1.5                                   |           |         |         | –     | –             | 1.5       | $\text{V}$    |
|  | 1.9          | –               | 10              | 3                                     |           |         |         | –     | –             | 3         |               |
|  | 1.5, 13.5    | –               | 15              | 4                                     |           |         |         | –     | –             | 4         |               |
| Input High<br>Voltage,<br>$V_{IH}$ Min.              | 0.5, 4.5     | –               | 5               | 3.5                                   |           |         |         | 3.5   | –             | –         | $\text{V}$    |
|  | 1.9          | –               | 10              | 7                                     |           |         |         | 7     | –             | –         |               |
|  | 1.5, 13.5    | –               | 15              | 11                                    |           |         |         | 11    | –             | –         |               |
| Input Current<br>$I_{IN}$ Max.                       | –            | 0.18            | 18              | $\pm 0.1$                             | $\pm 0.1$ | $\pm 1$ | $\pm 1$ | –     | $\pm 10^{-5}$ | $\pm 0.1$ | $\mu\text{A}$ |

## CD4014B, CD4021B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A=25^\circ\text{C}$ , Input  $t_r, t_f=20\text{ ns}$ ,  $C_L=50\text{ pF}$ ,  $R_L=200\text{ k}\Omega$

| CHARACTERISTIC   | TEST CONDITIONS | LIMITS              |      |      | UNITS       |
|--|-----------------|---------------------|------|------|-------------|
|  |                 | V <sub>DD</sub> (V) | Min. | Typ. |             |
| Propagation Delay Time, $t_{PLH}, t_{PHL}$               | 5               | —                   | 160  | 320  | ns          |
|  | 10              | —                   | 80   | 160  |             |
|  | 15              | —                   | 60   | 120  |             |
| Transition Time, $t_{THL}, t_{TLH}$                      | 5               | —                   | 100  | 200  | ns          |
|  | 10              | —                   | 50   | 100  |             |
|  | 15              | —                   | 40   | 80   |             |
| Maximum Clock Input Frequency, $f_{CL}$                  | 5               | 3                   | 6    | —    | MHz         |
|  | 10              | 6                   | 12   | —    |             |
|  | 15              | 8.5                 | 17   | —    |             |
| Minimum Clock Pulse Width, $t_W$                         | 5               | —                   | 90   | 180  | ns          |
|  | 10              | —                   | 40   | 80   |             |
|  | 15              | —                   | 25   | 50   |             |
| Clock Rise and Fall Time, $t_{rCL}, t_{fCL}^*$           | 5               | —                   | —    | 15   | \mu\text{s} |
|  | 10              | —                   | —    | 15   |             |
|  | 15              | —                   | —    | 15   |             |
| Minimum Set-up Time, $t_s$ :                             | 5               | —                   | 60   | 120  | ns          |
|  | 10              | —                   | 40   | 80   |             |
|  | 15              | —                   | 30   | 60   |             |
| Parallel Inputs CD4014B (ref. to CL)                     | 5               | —                   | 40   | 80   | ns          |
|  | 10              | —                   | 25   | 50   |             |
|  | 15              | —                   | 20   | 40   |             |
| Parallel Inputs CD4021B (ref. to P/S)                    | 5               | —                   | 25   | 50   | ns          |
|  | 10              | —                   | 15   | 30   |             |
|  | 15              | —                   | 10   | 20   |             |
| Parallel/Serial Control CD4014B (ref. to CL)             | 5               | —                   | 90   | 180  | ns          |
|  | 10              | —                   | 40   | 80   |             |
|  | 15              | —                   | 30   | 60   |             |
| Minimum Hold Time, $t_H$ :                               | 5               | —                   | —    | 0    | ns          |
|  | 10              | —                   | —    | 0    |             |
|  | 15              | —                   | —    | 0    |             |
| Minimum P/S Pulse Width, $t_{WH}$ (CD4021B)              | 5               | —                   | 80   | 160  | ns          |
|  | 10              | —                   | 40   | 80   |             |
|  | 15              | —                   | 25   | 50   |             |
| Minimum P/S Removal Time, $t_{REM}$ CD4021B (ref. to CL) | 5               | —                   | 140  | 280  | ns          |
|  | 10              | —                   | 70   | 140  |             |
|  | 15              | —                   | 50   | 100  |             |
| Average Input Capacitance, $C_I$                         | Any Input       | —                   | 5    | 7.5  | pF          |

\* If more than one unit is cascaded  $t_{rCL}$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

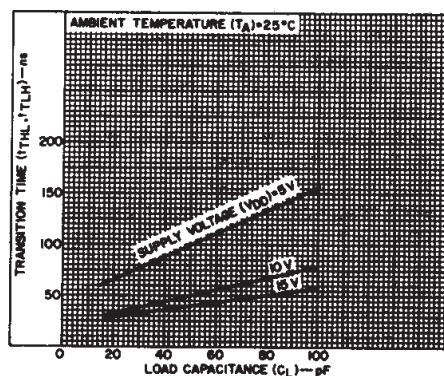


Fig. 7 – Typical transition time as a function of load capacitance.

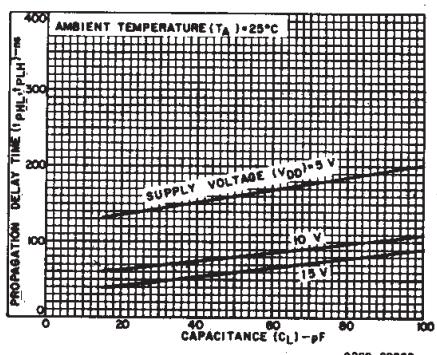


Fig. 8 – Typical propagation delay time as a function of load capacitance.

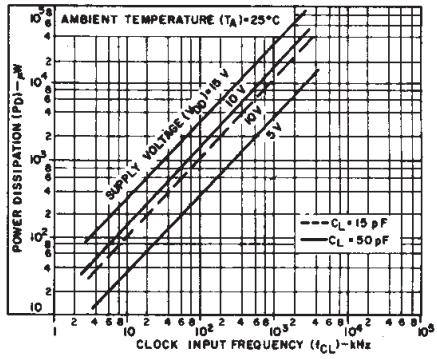


Fig. 9 – Typical dynamic power dissipation as a function of clock input frequency.

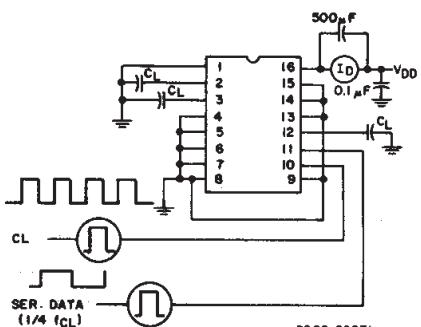


Fig. 10 – Dynamic power dissipation test circuit.

## CD4014B, CD4021B Types

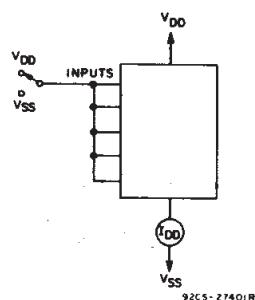


Fig. 11 – Quiescent device current test circuit.

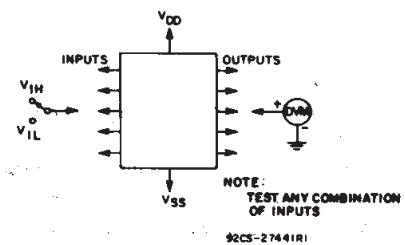


Fig. 12 – Input voltage test circuit.

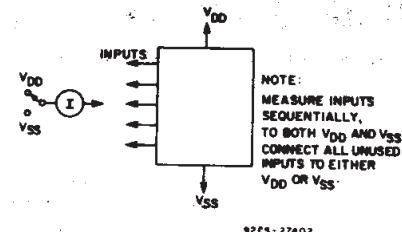
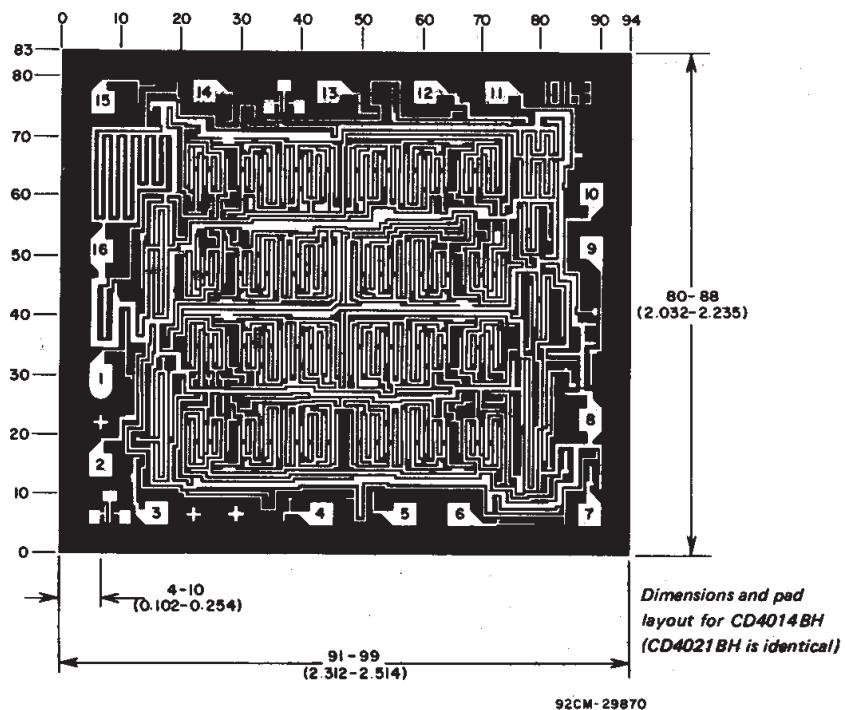


Fig. 13 – Input current test circuit.



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COMMERCIAL CMOS  
HIGH VOLTAGE ICs

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.  
Grid graduations are in mils ( $10^{-3}$  inch).

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4014BE         | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD4014BEE4       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD4014BF3A       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD4014BM         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BM96       | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BM96E4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BM96G4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BME4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BMG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BMT        | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BMTE4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BMTG4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BPW        | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BPWE4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BPWG4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BPWR       | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BPWRE4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4014BPWRG4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BE         | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD4021BEE4       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD4021BF         | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD4021BF3A       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD4021BF3AS2283  | OBsolete              | CDIP         | J               | 16   |             | TBD                     | Call TI          | Call TI                      |
| CD4021BM         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BM96       | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BM96E4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BM96G4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| no Sb/Br)        |                       |              |                 |      |             |                         |                  |                              |
| CD4021BME4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BMG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BMT        | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BMTE4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BMTG4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BNSR       | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BNSRE4     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BNSRG4     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BPW        | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BPWE4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BPWG4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BPWR       | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BPWRE4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4021BPWRG4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| JM38510/05754BEA | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

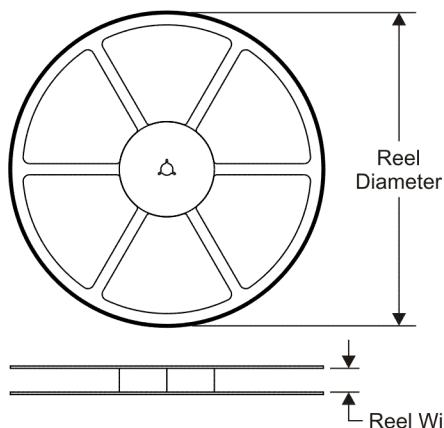
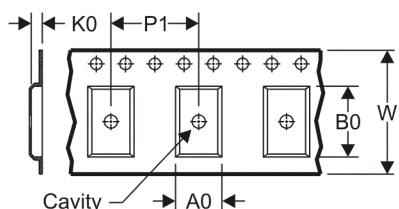
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

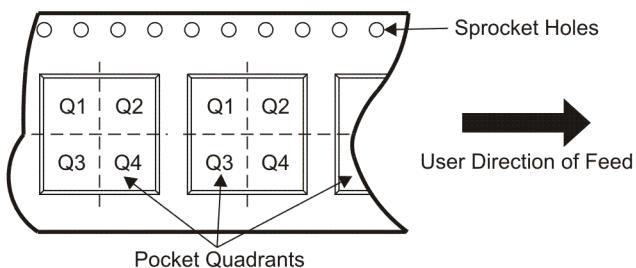
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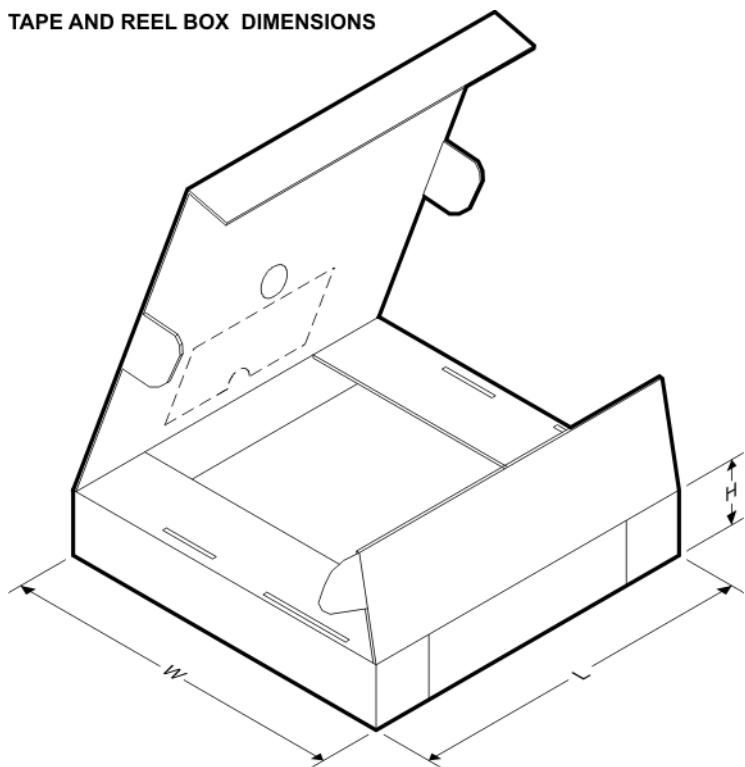
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4014BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4014BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 7.0     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD4021BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4021BNSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| CD4021BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 7.0     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


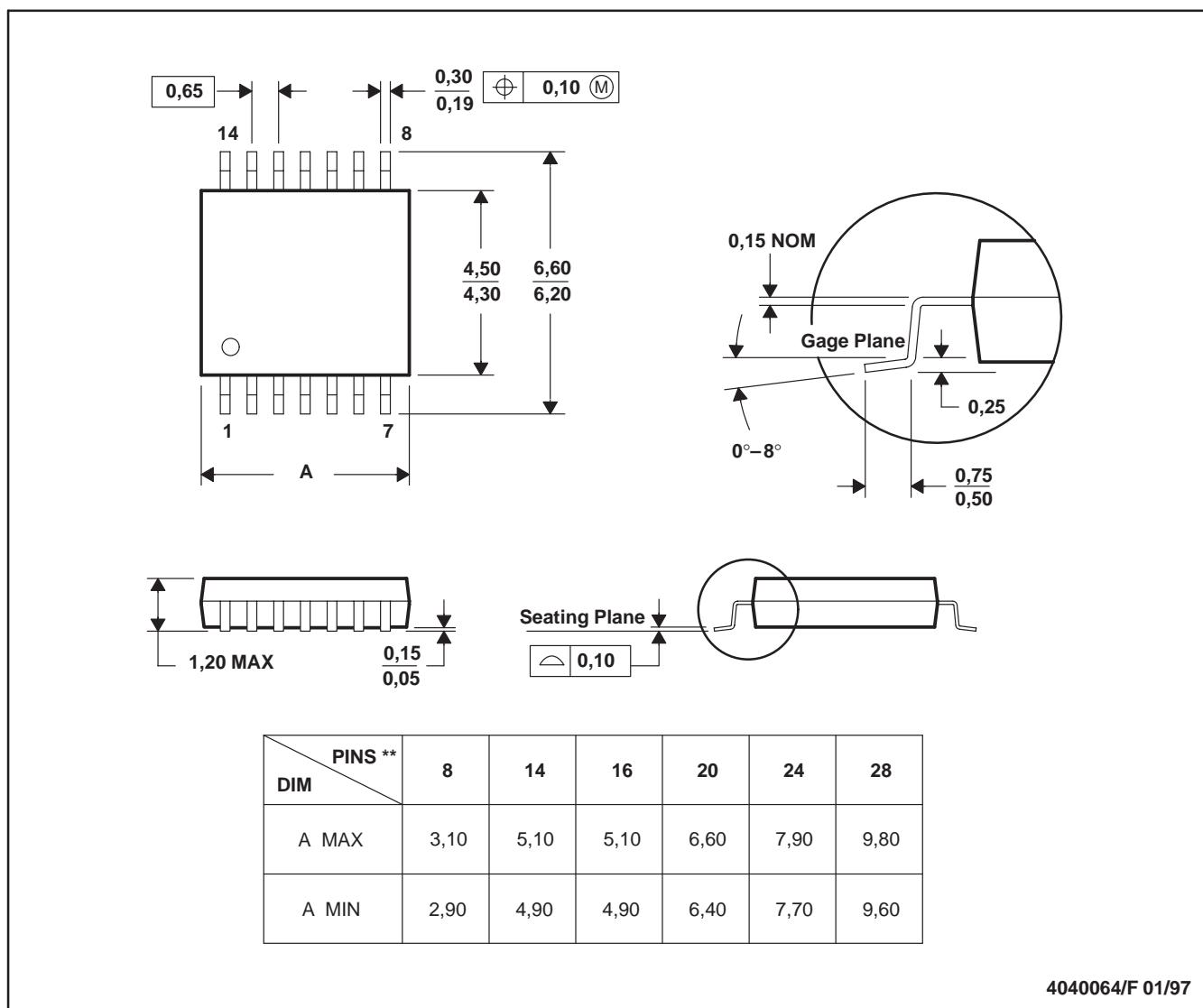
\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4014BM96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD4014BPWR | TSSOP        | PW              | 16   | 2000 | 346.0       | 346.0      | 29.0        |
| CD4021BM96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD4021BNSR | SO           | NS              | 16   | 2000 | 346.0       | 346.0      | 33.0        |
| CD4021BPWR | TSSOP        | PW              | 16   | 2000 | 346.0       | 346.0      | 29.0        |

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



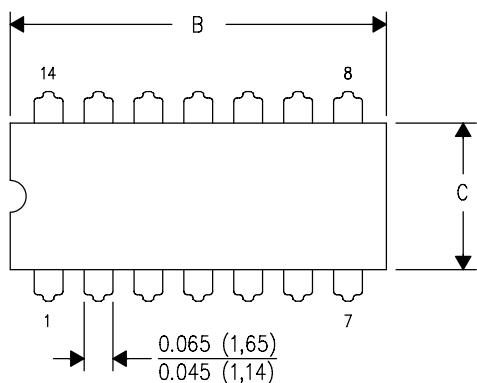
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

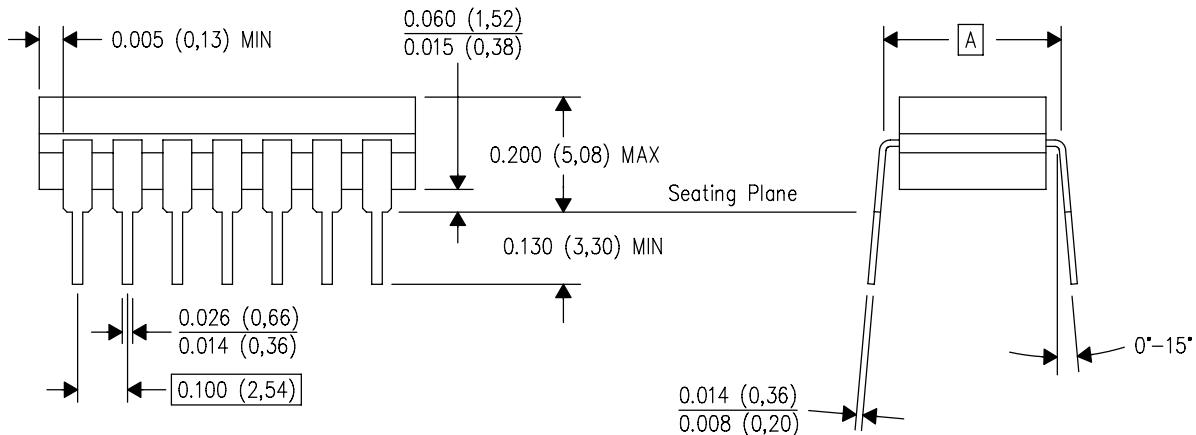
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

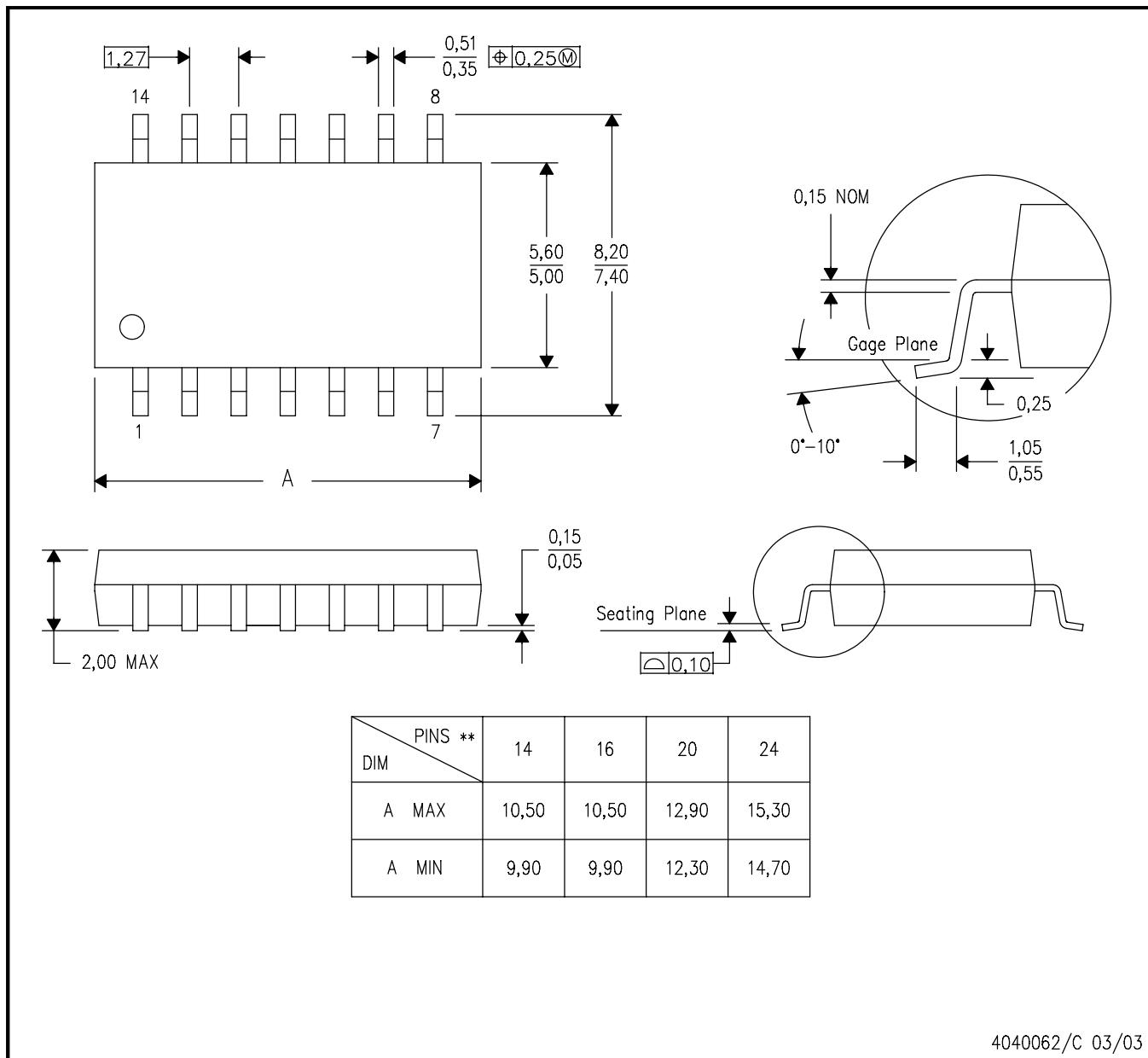
NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**

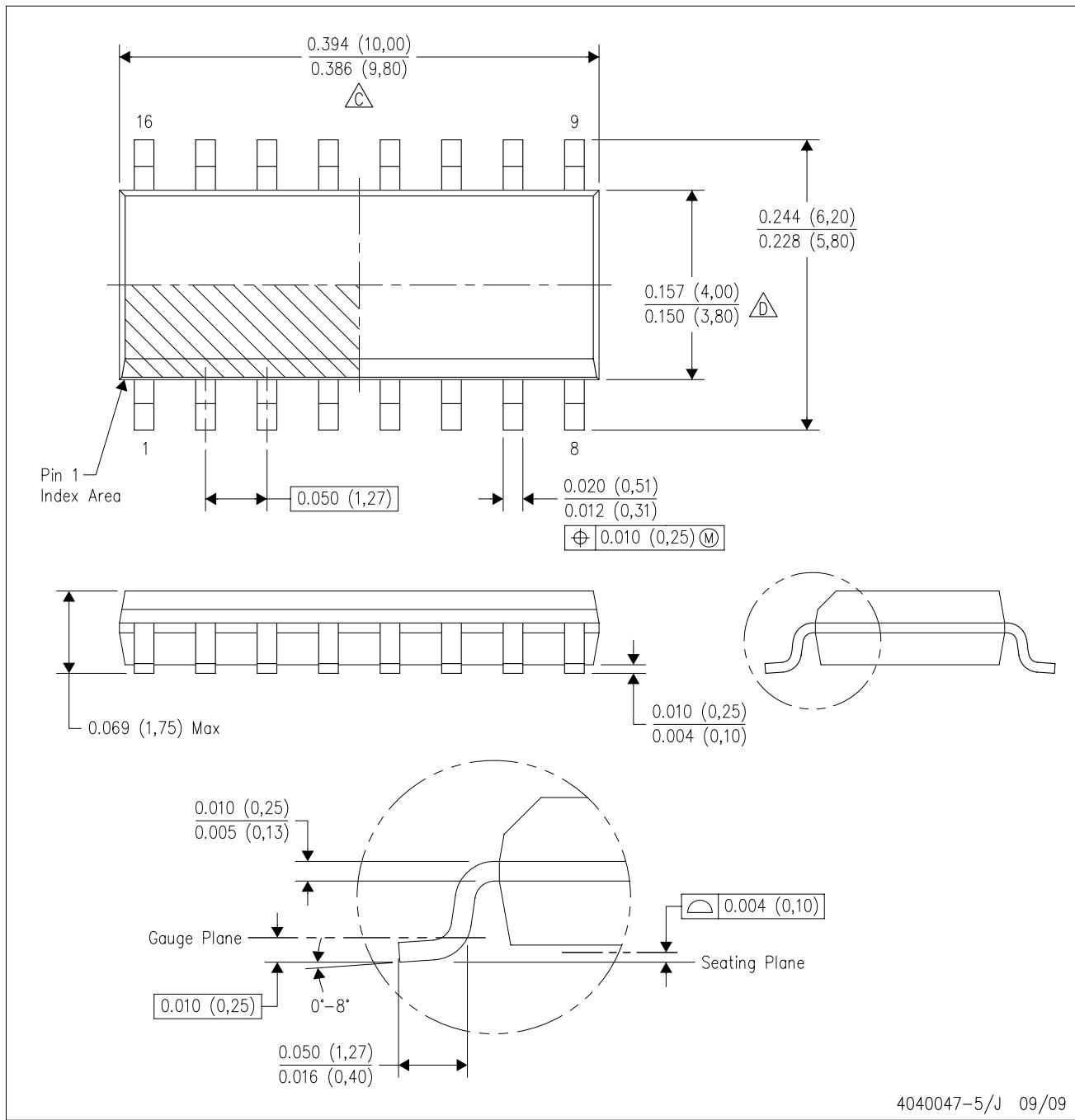


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

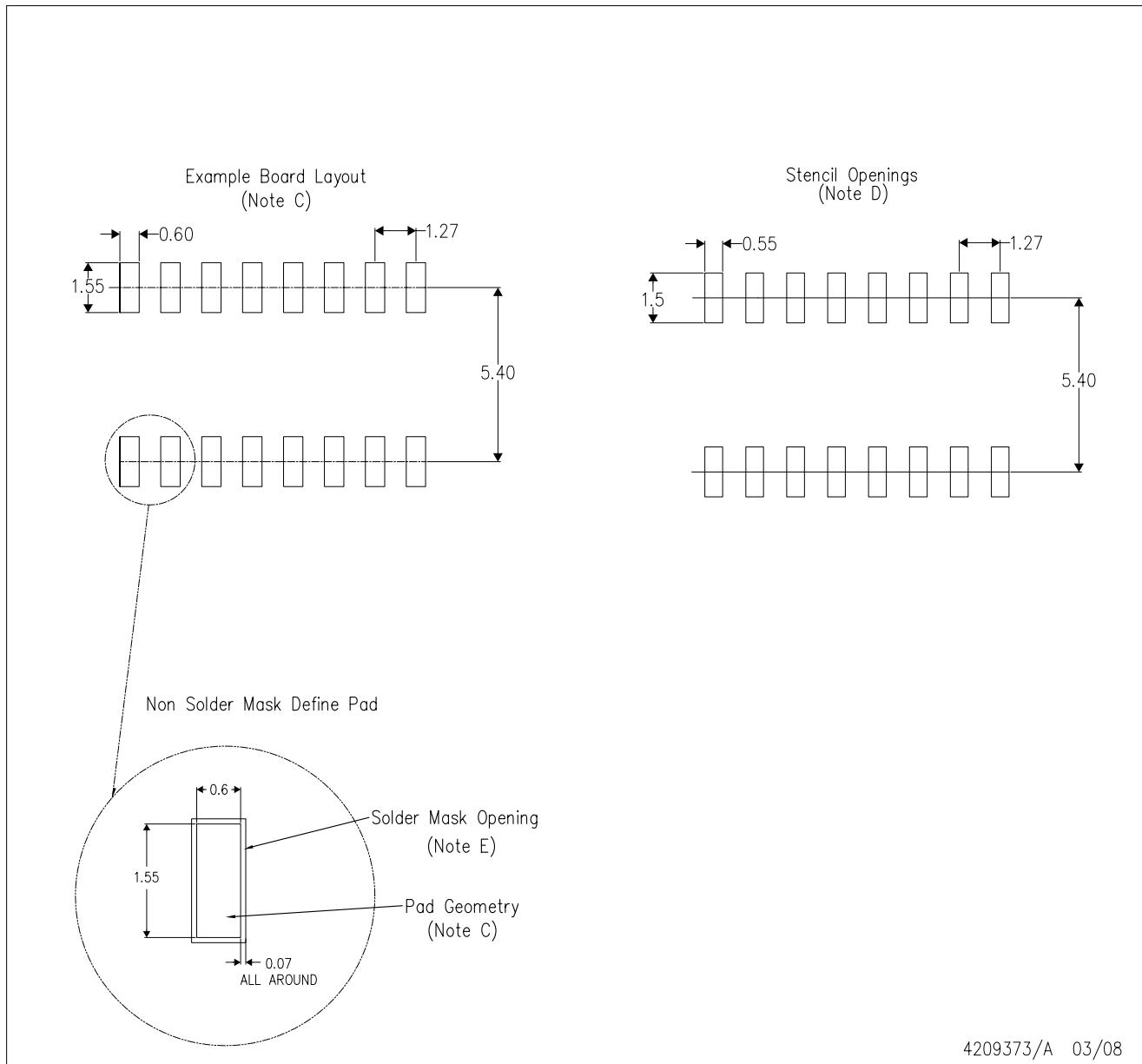
B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



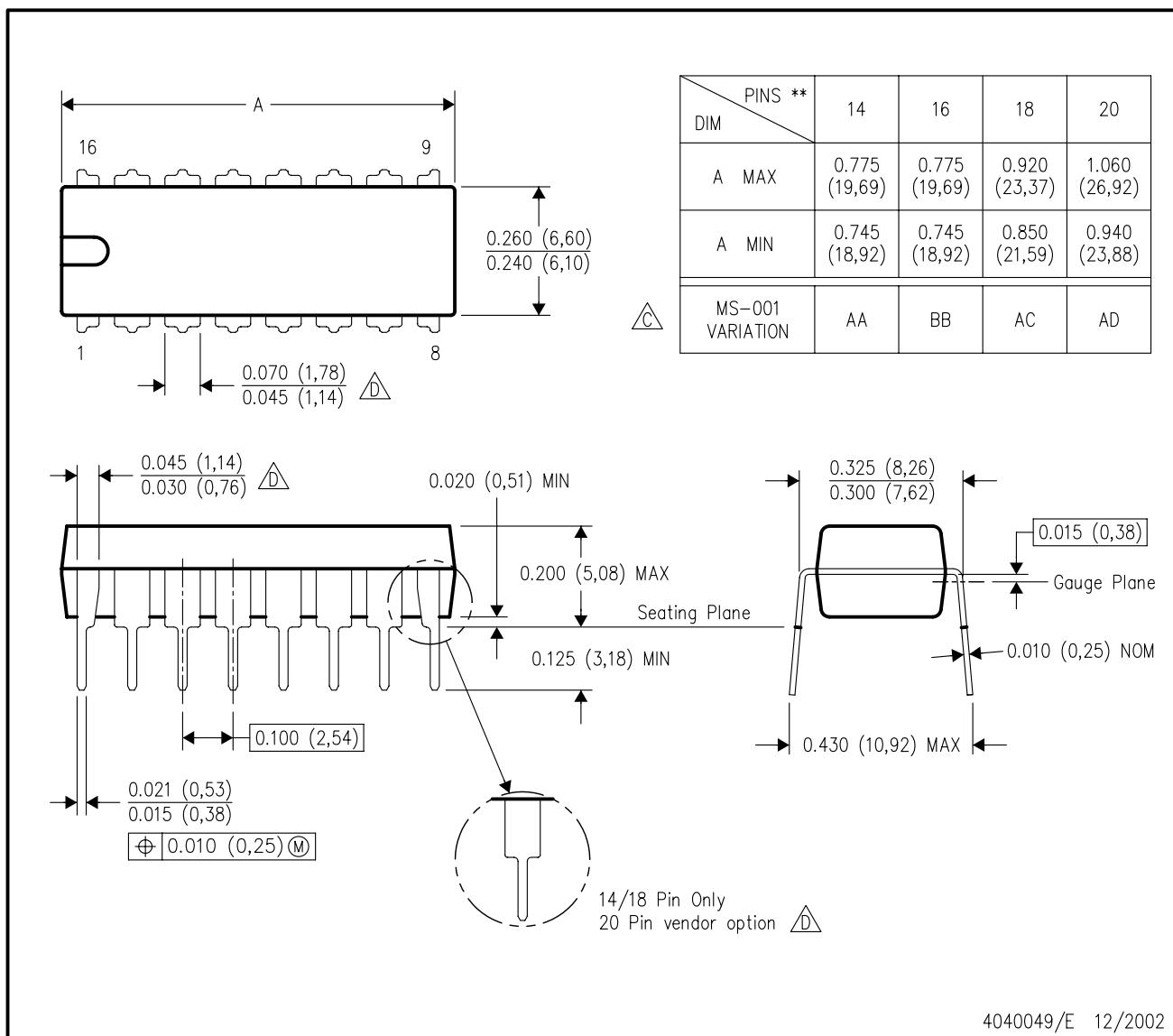
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| CD4014BE         | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD4014BE                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4014BEE4       | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD4014BE                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4014BF3A       | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | CD4014BF3A              | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4014BM         | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4014BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4014BM96       | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4014BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4014BMG4       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4014BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4014BMT        | ACTIVE        | SOIC         | D                  | 16   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4014BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4014BPW        | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CM014B                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4014BPWR       | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CM014B                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BE         | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD4021BE                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BEE4       | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD4021BE                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BF         | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | CD4021BF                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BF3A       | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | CD4021BF3A              | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BF3AS2283  | OBsolete      | CDIP         | J                  | 16   |                | TBD                        | Call TI                 | Call TI              |              |                         |   |
| CD4021BM         | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4021BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BM96       | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4021BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BM96E4     | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4021BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BMG4       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4021BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| CD4021BMT        | ACTIVE        | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CD4021BM                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BPW        | ACTIVE        | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CM021B                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BPWR       | ACTIVE        | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CM021B                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| CD4021BPWRG4     | ACTIVE        | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | CM021B                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| JM38510/05754BEA | ACTIVE        | CDIP         | J               | 16   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | JM38510/05754BEA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| M38510/05754BEA  | ACTIVE        | CDIP         | J               | 16   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | JM38510/05754BEA        | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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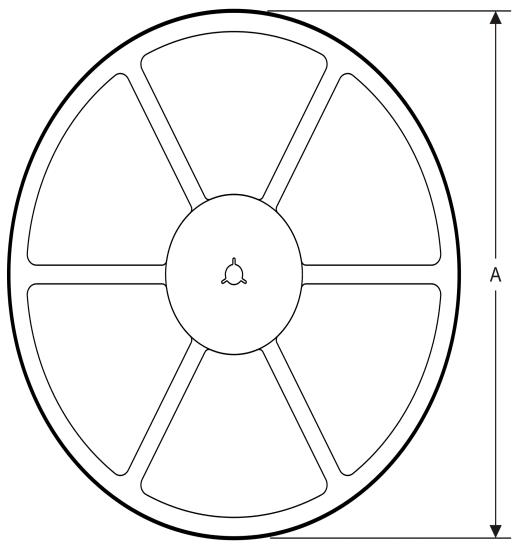
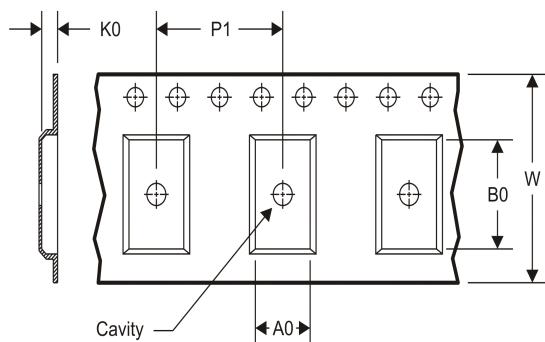
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4014B, CD4014B-MIL, CD4021B, CD4021B-MIL :**

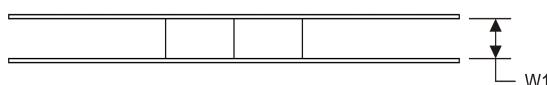
- Catalog: [CD4014B](#), [CD4021B](#)
- Automotive: [CD4021B-Q1](#), [CD4021B-Q1](#)
- Military: [CD4014B-MIL](#), [CD4021B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

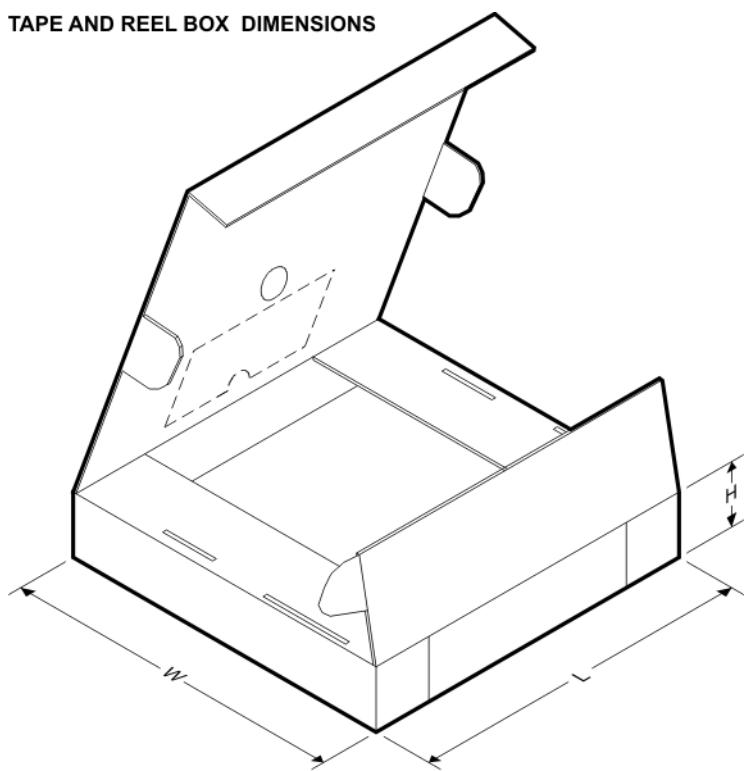
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |


**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4014BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4014BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD4021BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4021BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


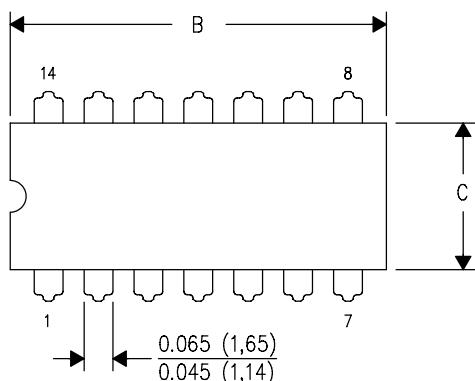
\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4014BM96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD4014BPWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| CD4021BM96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD4021BPWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |

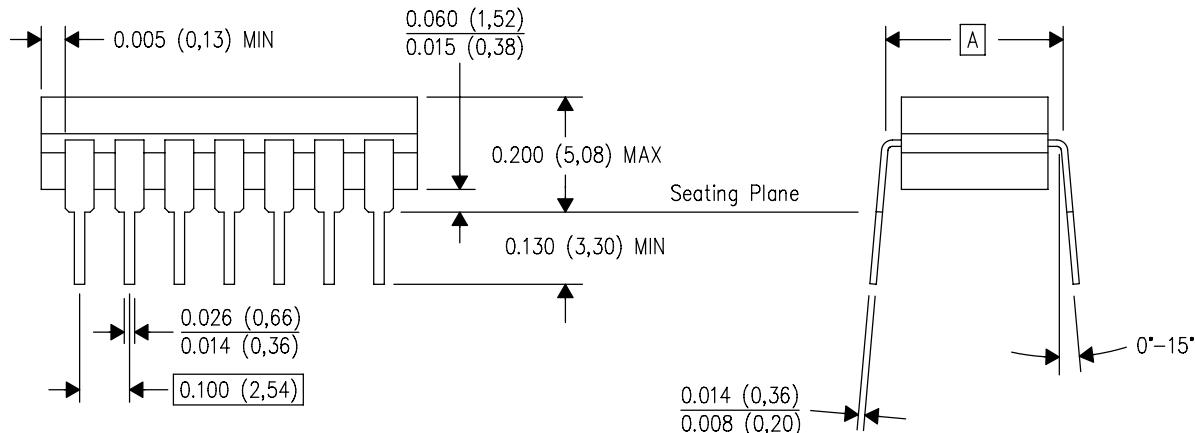
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



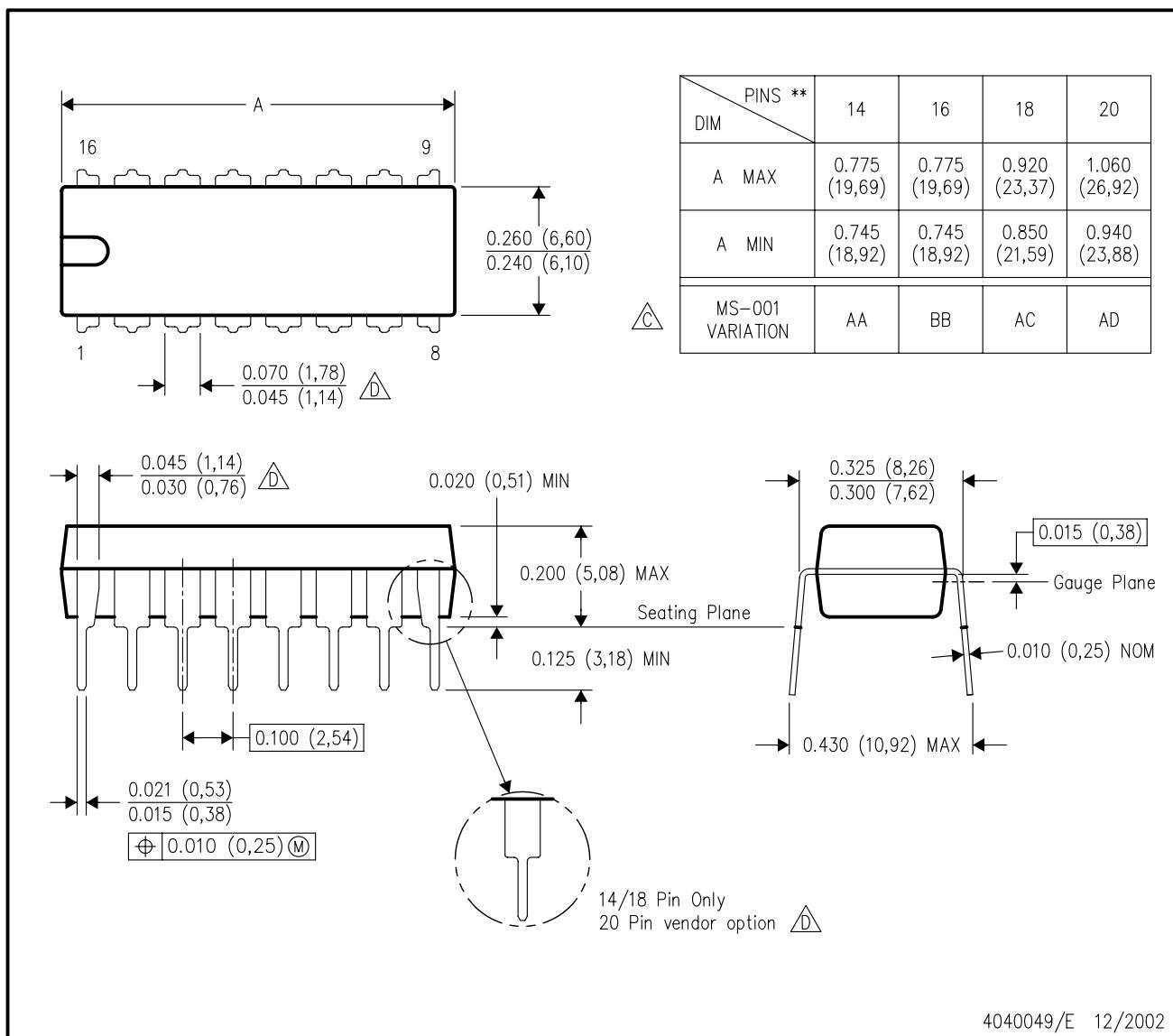
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



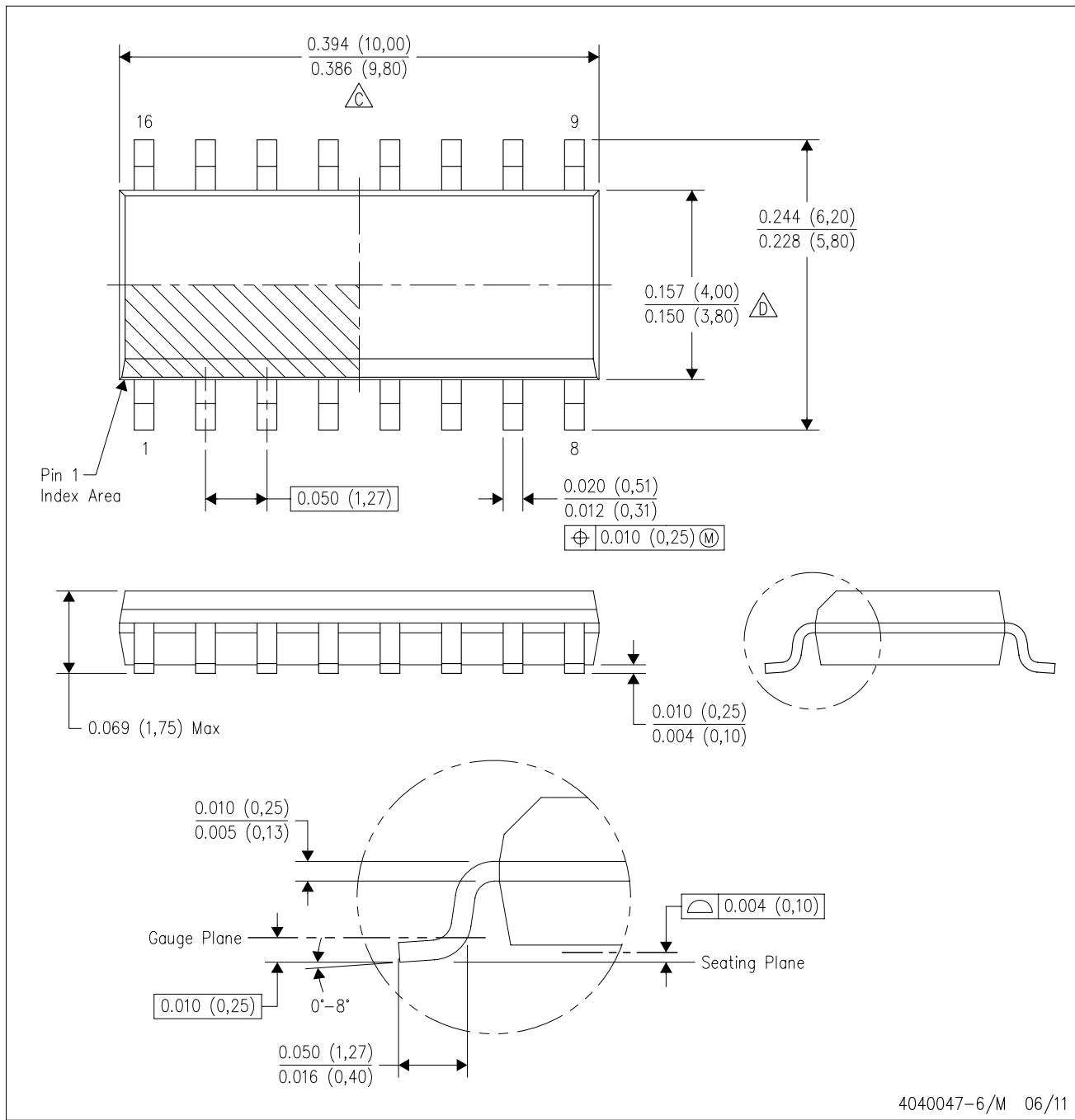
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

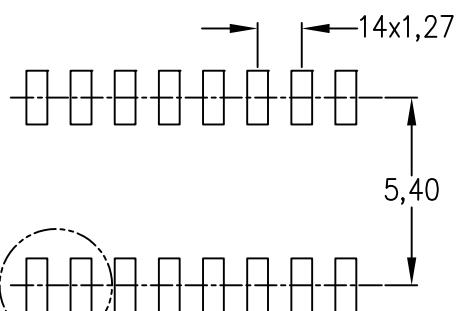
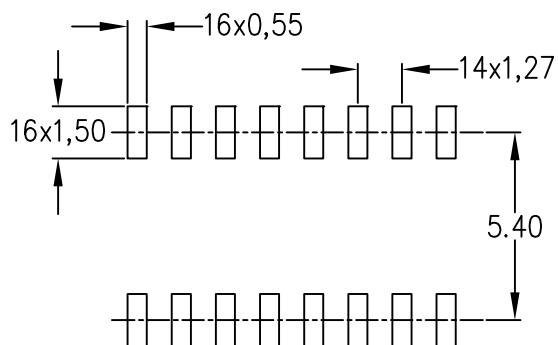
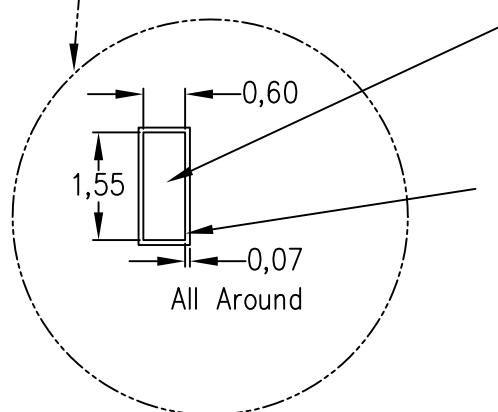
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

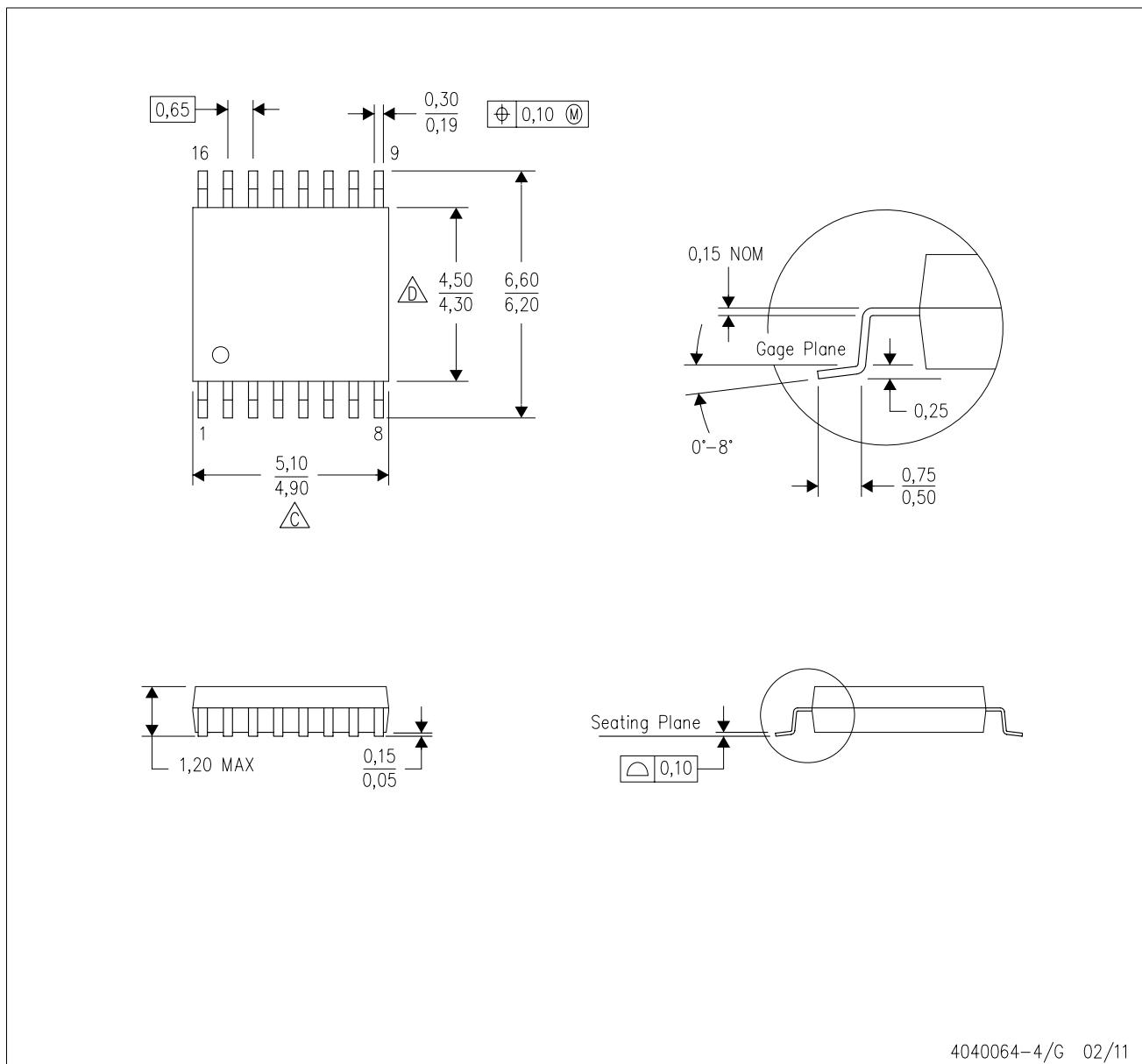
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

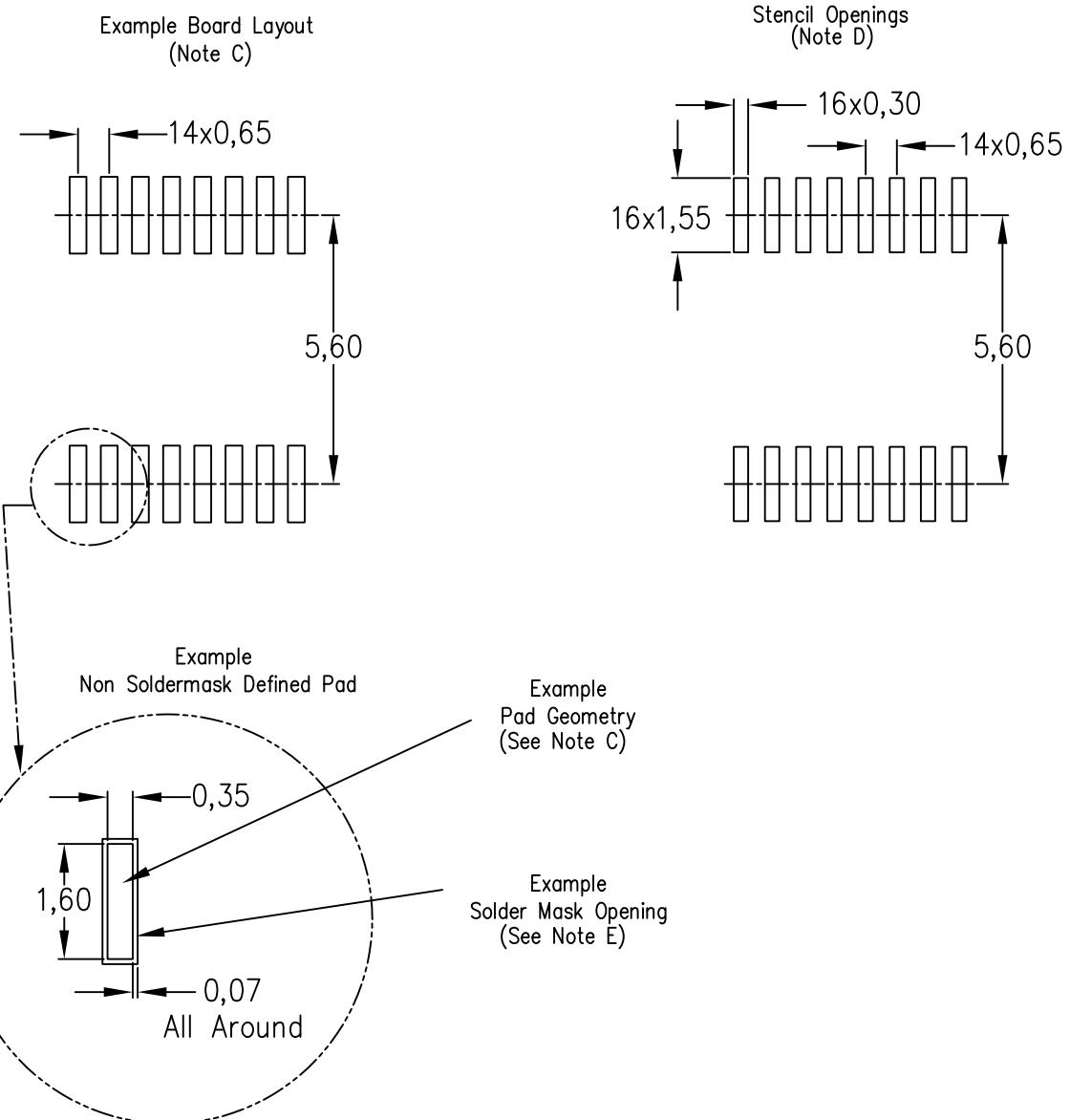
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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