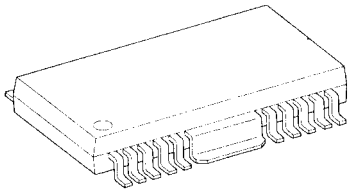
TOSHIBA BiCD Processor IC Silicon Monolithic

TB62206F/FG

BiCD PWM 2−Phase Bipolar Stepping Motor Driver

The TB62206F/FG is designed to drive a 2−phase bipolar setpping motor. With BiCD process technology, this device enables output withstand voltage of 40 V and maximum current of 1.8 A to be achieved.



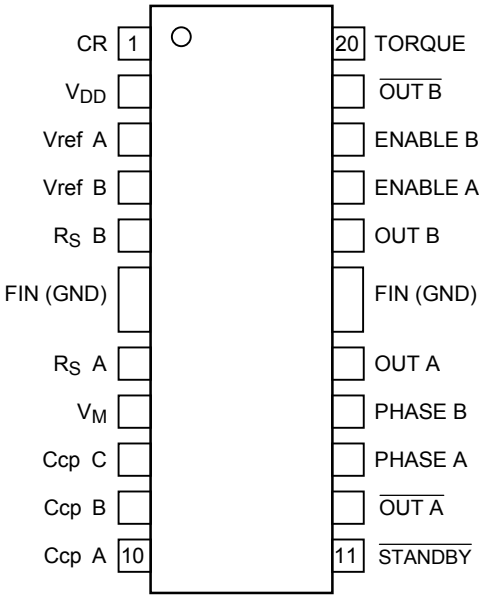
HSOP20-P-450-1.00

Weight: 0.79 g (typ.)

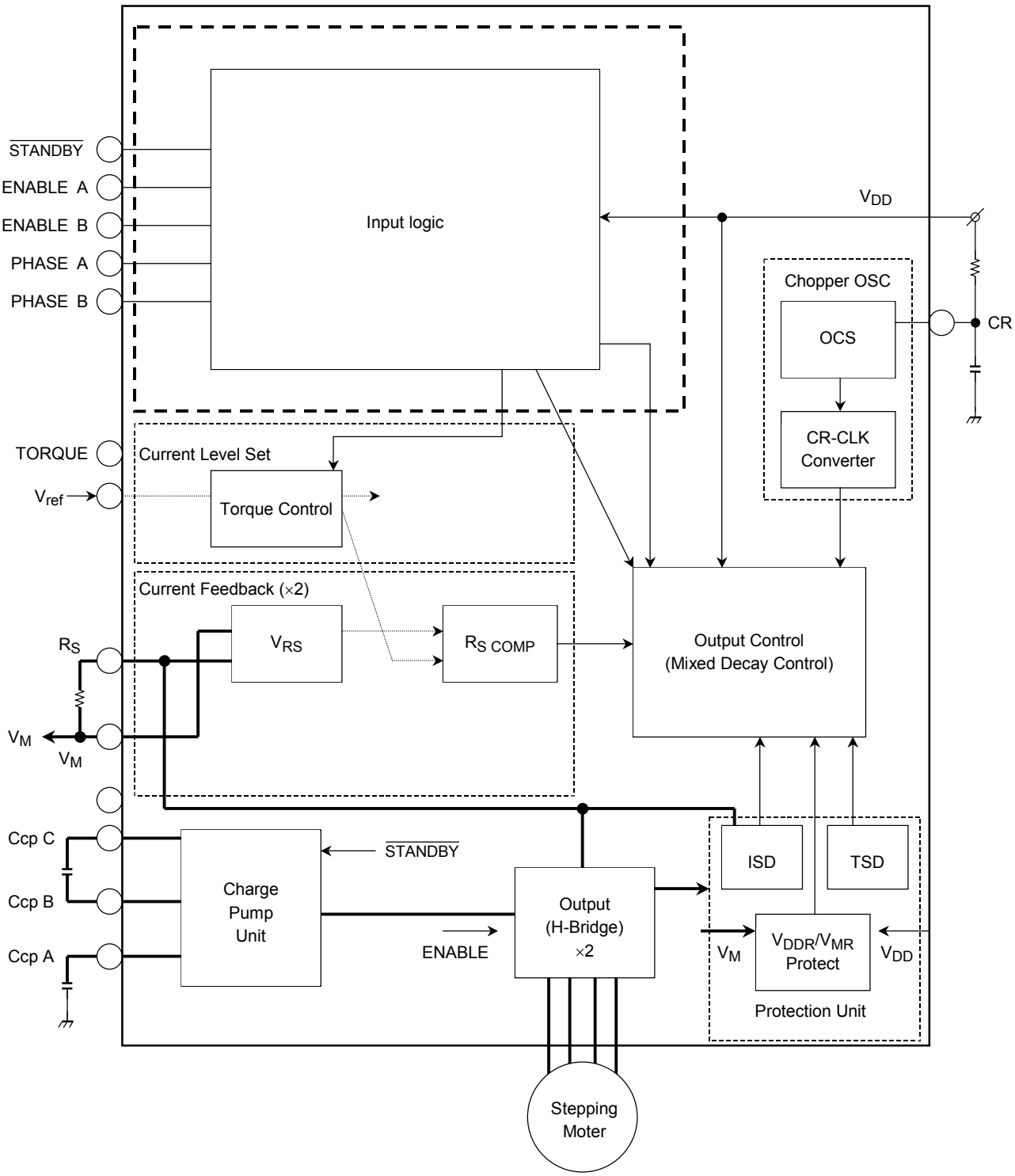
Features

- Bipolar stepping motor driver IC
- Internal PWM current control
- 2−phase/1−2 phase excitation is available
- Monolithic BiCD IC
  DMOS FET used for output power transistor
- High voltage output and High current: 40 V/1.8 A (max)
- On−chip thermal shutdown circuit, overcurrent protection circuit and power−on reset circuit (POR)
- Package: HSOP20−P−450−1.00

Pin Assignment



Block Diagram



Function Table－Output

Phase	Enable	OUT (+)	OUT (－)
X	L	OFF	OFF
H	H	H	L
L	H	L	H

X : Don't care

Others

Pin Name	H	L	Notes
ENABLE X	Output	Output OFF	Output is OFF regardless of its phase's state.
PHASE X	OUT X: H	OUT $\overline{X}$: H	In high level, current flows OUT X → OUT $\overline{X}$
$\overline{\text{STANDBY}}$	Motor operation enable	All functions of the IC stopped	When $\overline{\text{STANDBY}}$ = L, output stopped while charge pomp stopped.
TORQUE	100%	71%	High-level

Protection Function

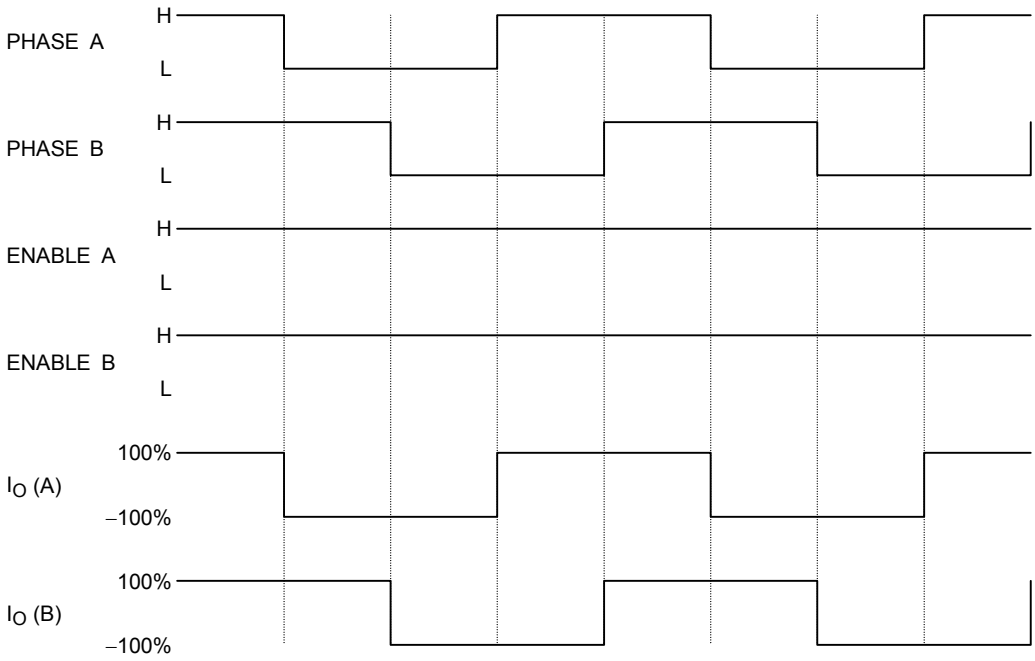
(1) Thermal shutdown circuit
While Tj = 150°C, all outputs are OFF. To turn-on, change the state of the $\overline{\text{STANDBY}}$ pin in the order of H, L, H.
It has temperature hysteresis to prevent the output from oscillating. (ΔT = 35°C)

(2) POR (Power-On Reset Circuit: V_M and V_{DD} power supply monitor circuit)
Output is forcibly turned off until V_M and V_{DD} reach their specified levels.

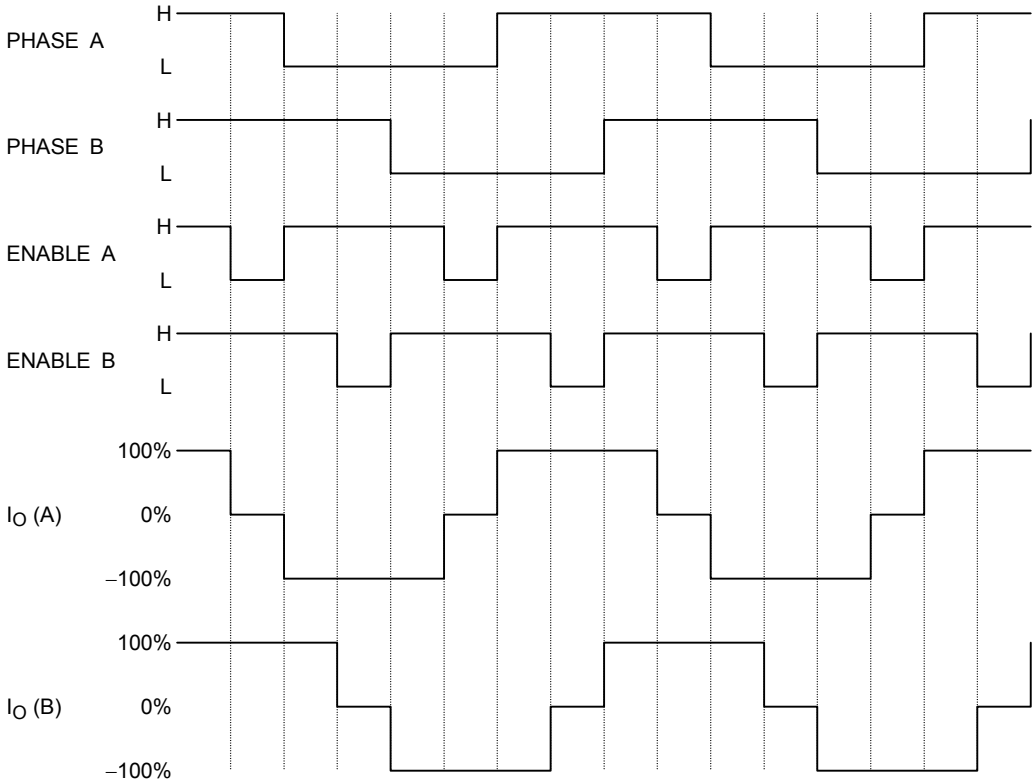
(3) ISD
Output is forcibly turned off when current higher than the specified level flows in the output block.
To turn-on, change the state of the $\overline{\text{STANDBY}}$ pin in the order of H, L, H.

Timing Chart

(1) Full Step



(2) Half Step



Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Logic supply voltage		V_{DD}	7	V
Motor supply voltage		V_M	40	V
Output current	(Note 1)	I_{OUT}	1.8	A/phase
Current detect pin voltage		V_{RS}	$V_M \pm 4.5$ V	V
Charge pump pin maximum voltage (CCP1 pin)		V_H	$V_M + 7.0$	V
Logic input voltage	(Note 2)	V_{IN}	to $V_{DD} + 0.4$	V
Power dissipation	(Note 3)	P_D	1.4	W
	(Note 4)		3.2	
Operating temperature		T_{opr}	−40 to 85	°C
Storage temperature		T_{stg}	−55 to 150	°C
Junction temperature		T_j	150	°C

Note 1: Perform thermal calculations for the maximum current value under normal conditions. Use the IC at 1.5 A or less per phase.
The current value maybe controled according to the ambient temperature or board conditions.

Note 2: Input 7 V or less as V_{IN}

Note 3: Measured for the IC only. (Ta = 25°C)

Note 4: Measured when mounted on the board. (Ta = 25°C)

Ta: IC ambient temperature

T_{opr}: IC ambient temperature when starting operation

T_j: IC chip temperature during operation T_j (max) is controlled by TSD (thermal shut down circuit)

Recommended Operating Conditions (Ta = 0 to 85°C, (Note 5))

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	4.5	5.0	5.5	V
Motor supply voltage	V_M	V_{DD} = 5.0 V, Ccp1 = 0.22 μF, Ccp2 = 0.02 μF	13	24	35	V
Output current	$I_{OUT\ (1)}$	Ta = 25°C, per phase	—	1.2	1.5	A
Logic input voltage	V_{IN}	—	GND	—	V_{DD}	V
Phase signal input frequency	f_{PHASE}	V_{DD} = 5.0 V	—	1.0	150	KHz
Chopping frequency	f_{chop}	V_{DD} = 5.0 V	50	100	150	KHz
V_{ref} reference voltage	V_{ref}	V_M = 24 V, Torque = 100%	GND	3.0	4.0	V
Current detect pin voltage	V_{RS}	V_{DD} = 5.0 V	0	±1.0	±4.5	V

Note 5: Because the maximum value of T_j is 120°C, recommended maximum current usage is below 120°C.

Electrical Characteristics 1 (unless otherwise specified, Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	HIGH	$V_{IN\ (H)}$	DC	Data input pins	2.0	V_{DD}	V_{DD} + 0.4	V
	LOW	$V_{IN\ (L)}$			GND − 0.4	GND	0.8	
Input hysteresis voltage		$V_{IN\ (HIS)}$	DC	Data input pins	200	400	700	mV
Input current		$I_{IN\ (H)}$	DC	Data input pins with resistor	—	—	1.0	μA
		$I_{IN\ (H)}$		Data input pins without resistor	35	50	75	
		$I_{IN\ (L)}$			—	—	1.0	
Power dissipation (V_{DD} pin)		I_{DD1}	DC	V_{DD} = 5 V, all inputs connected to ground, Logic, output all off	1.0	2.0	3.0	mA
		I_{DD2}		Output OPEN, f_{PHASE} = 1.0 kHz LOGIC ACTIVE, V_{DD} = 5 V, ChargePump = charged	1.0	2.5	3.5	
Power dissipation (V_M pin)		I_{M1}	DC	Output OPEN, all inputs connected to ground, Logic, output all off, ChargePump = no operation	1.0	2.0	3.0	mA
		I_{M2}		OUT OPEN, f_{PHASE} = 1 kHz LOGIC ACTIVE, V_{DD} = 5 V, V_M = 24 V, Output off, ChargePump = charged	2.0	4.0	5.0	
		I_{M3}		OUT OPEN, f_{PHASE} = 4 kHz LOGIC ACTIVE, 100 kHz chopping (emulation), Output OPEN, ChargePump = charged	—	10	13	
Output standby current	Upper	DC	DC	V_{RS} = V_M = 24 V, V_{OUT} = 0 V, $\overline{STANDBY}$ = H, PHASE = H	−200	−150	—	μA
Output bias current	Upper	I_{OB}	DC	V_{OUT} = 0 V, $\overline{STANDBY}$ = H	−100	−50	—	μA
Output leakage current	Lower	I_{OL}	DC	V_{RS} = V_M = CcpA = V_{OUT} = 24 V, LOGIC IN = ALL = L	—	1.0	1.0	μA
Comparator reference voltage ratio	HIGH (reference)	$V_{RS\ (H)}$	DC	V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (H) = 100% set	—	100	—	%
	LOW	$V_{RS\ (L)}$		V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (L) = 71% set	66	71	76	
Output current differential		ΔI_{OUT1}	DC	Differences between output current channels	−5	—	5	%
Output current setting differential		ΔI_{OUT2}	DC	I_{OUT} = 1000 mA	−5	—	5	%
RS pin current		I_{RS}	DC	V_{RS} = 24 V, V_M = 24 V $\overline{STANDBY}$ = L	—	1	2	μA
Output transistor drain-source ON-resistance		$R_{ON\ (D-S)\ 1}$	DC	I_{OUT} = 1.0 A, V_{DD} = 5.0 V T_j = 25°C, Drain-Source	—	0.5	0.6	Ω
		$R_{ON\ (S-D)\ 1}$		I_{OUT} = 1.0 A, V_{DD} = 5.0 V T_j = 25°C, Source-Drain	—	0.5	0.6	
		$R_{ON\ (D-S)\ 2}$		I_{OUT} = 1.0 A, V_{DD} = 5.0 V T_j = 105°C, Drain-Source	—	0.6	0.75	
		$R_{ON\ (S-D)\ 2}$		I_{OUT} = 1.0 A, V_{DD} = 5.0 V T_j = 105°C, Source-Drain	—	0.6	0.75	

Electrical Characteristics 2 (unless otherwise specified, Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
V_{ref} input voltage	V_{ref}	DC	V_M = 24 V, V_{DD} = 5 V, $\overline{STANDBY}$ = H, Output on, PHASE = 1 kHz	GND	—	4.0	V
V_{ref} input current	I_{ref}	DC	$\overline{STANDBY}$ = H, Output on, V_M = 24 V, V_{DD} = 5 V, V_{ref} = 3.0 V	20	35	50	μA
V_{ref} attenuation ratio	V_{ref} (GAIN)	DC	V_M = 24 V, V_{DD} = 5 V, $\overline{STANDBY}$ = H, Output on, V_{ref} = 0.0 to 4.0 V	1/4.8	1/5.0	1/5.2	—
TSD temperature (Note 1)	T_jTSD	DC	V_{DD} = 5 V, V_M = 24 V	130	—	170	°C
TSD return temperature difference (Note 1)	ΔT_jTSD	DC	T_jTSD = 130 to 170°C	T_jTSD − 50	T_jTSD − 35	T_jTSD − 20	°C
V_{DD} return voltage	V_{DDR}	DC	V_M = 24 V, $\overline{STANDBY}$ = H	2.0	3.0	4.0	V
V_M return voltage	V_{MR}	DC	V_{DD} = 5 V, $\overline{STANDBY}$ = H	8.0	9.0	10	V
Over current protected circuit operation current (Note 2)	ISD	—	V_{DD} = 5 V, V_M = 24 V	—	3.0	—	A

Note 1: Thermal shut down (TSD) circuit
When the IC junction temperature reaches the specified value and the TSD circuit is activated, the internal reset circuit is activated switching the outputs of both motors to off.
When the temperature is set between 130 (min) to 170°C (max), the TSD circuit operates.
When the TSD circuit is activated, the charge pump is halted, and TROTECT pin outputs V_{DD} voltage.
Even if the TSD circuit is activated and $\overline{STANDBY}$ goes H → L → H instantaneously, the IC is not reset until the IC junction temperature drops −20°C (typ.) below the TSD operating temperature (hysteresis function).

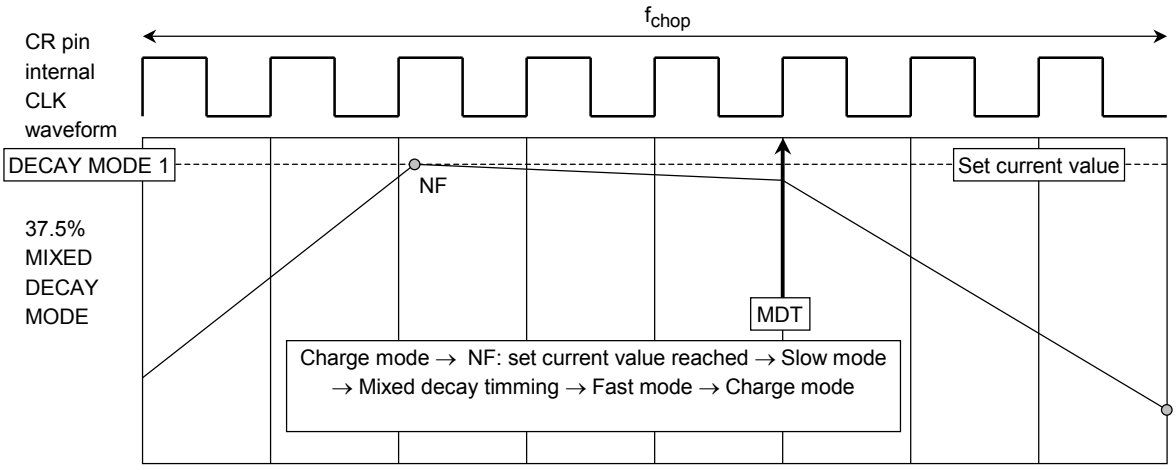
Note 2: Overcurrent protection circuit
When current exceeding the specified value flows to the output, the internal reset circuit is activated, and the ISD turns off the output.
Until the $\overline{STANDBY}$ signal goes Low to High, the overcurrent protection circuit remains activated.
During ISD, IC turns $\overline{STANDBY}$ mode and the charge pump halts.

AC Electrical Characteristics (Ta = 25°C, V_M = 24 V, V_{DD} = 5 V, 6.8 mH/5.7 Ω)

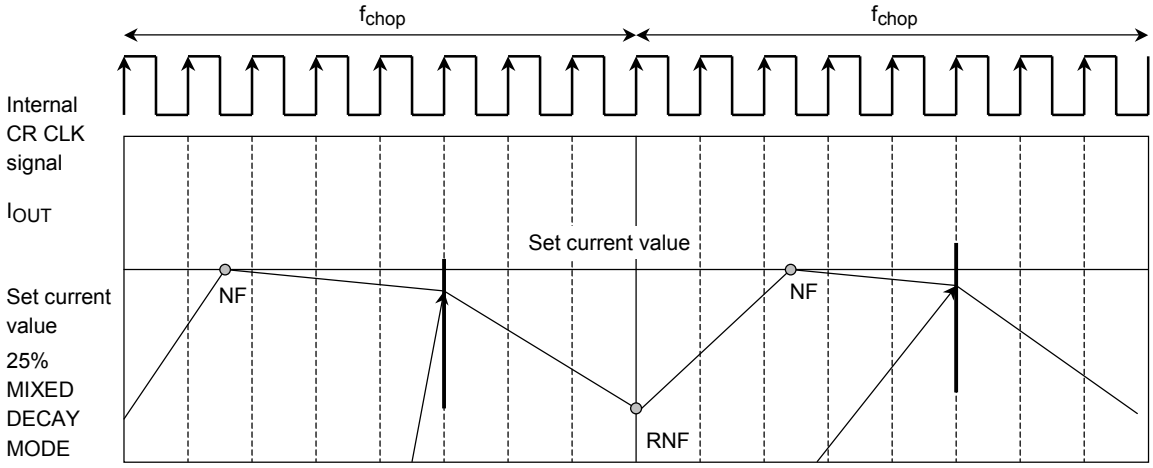
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock frequency	f_{PHASE}	AC	—	—	—	166	kHz
Minimum clock pulse width	t_w (t_{CLK})	—	—	100	—	—	μs
	t_{wp}	—	—	50	—	—	
	t_{wn}	AC	—	50	—	—	
Output transistor switching characteristic	t_r	—	Output Load: 6.8 mH/5.7 Ω	—	100	—	ns
	t_f	—	—	—	100	—	
	t_{pLH}	—	PHASE to OUT	—	1000	—	
	t_{pHL}	—	Output Load: 6.8 mH/5.7 Ω	—	2000	—	
	t_{pLH}	—	CR to OUT	—	500	—	
	t_{pHL}	—	Output Load: 6.8 mH/5.7 Ω	—	1000	—	
Noise rejection dead band time	t_{BRANK}	—	I_{OUT} = 1.0 A	200	300	500	ns
CR reference signal oscillation frequency	f_{CR}	—	C_{osc} = 560 pF, R_{osc} = 3.6 kΩ	—	800	—	kHz
Chopping frequency possible range	$f_{chop\ (min)}$ $f_{chop\ (max)}$	—	V_M = 24 V, V_{DD} = 5 V, Output ACTIVE (I_{OUT} = 1.0 A) Step fixed, Ccp1 = 0.22 μF, Ccp2 = 0.01 μF	40	100	150	kHz
Chopping set frequency	f_{chop}	—	Output ACTIVE (I_{OUT} = 1.0 A), CR CLK = 800 kHz	—	100	—	kHz
Charge pump rise time	t_{ONG}	—	Ccp = 0.22 μF, Ccp = 0.022 μF V_M = 24 V, V_{DD} = 5 V, $\overline{STANDBY}$ = ON → OFF	—	100	200	μs

Current Waveform and Setting of MIXED DECAY MODE

To control the constant current, the rate of Mixed Decay Mode which determines current amplitude (ripple current) should be 37.5%.

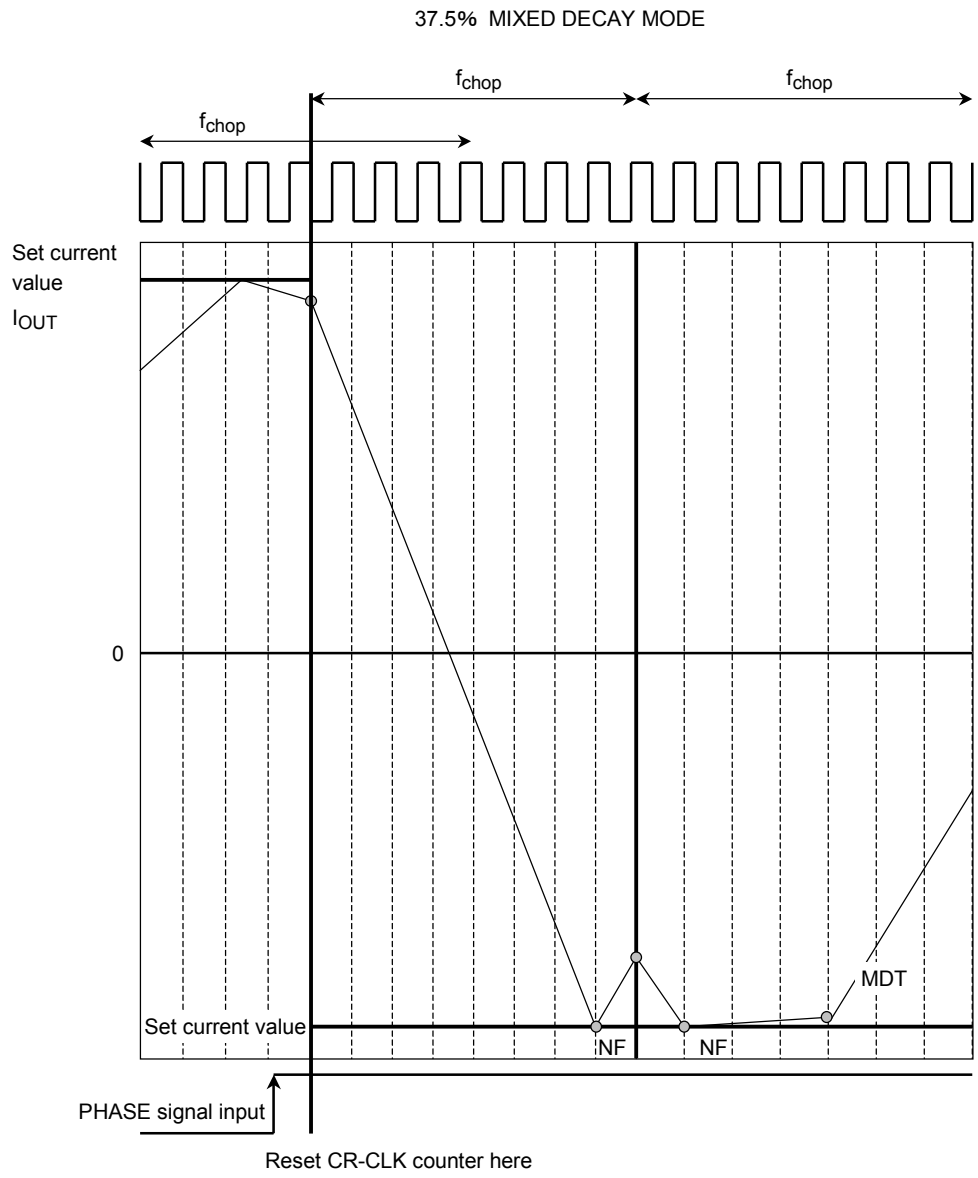


MIXED DECAY MODE Waveform (current waveform)



MDT (MIXED DECAY TIMMING) point: 37.5% fixed

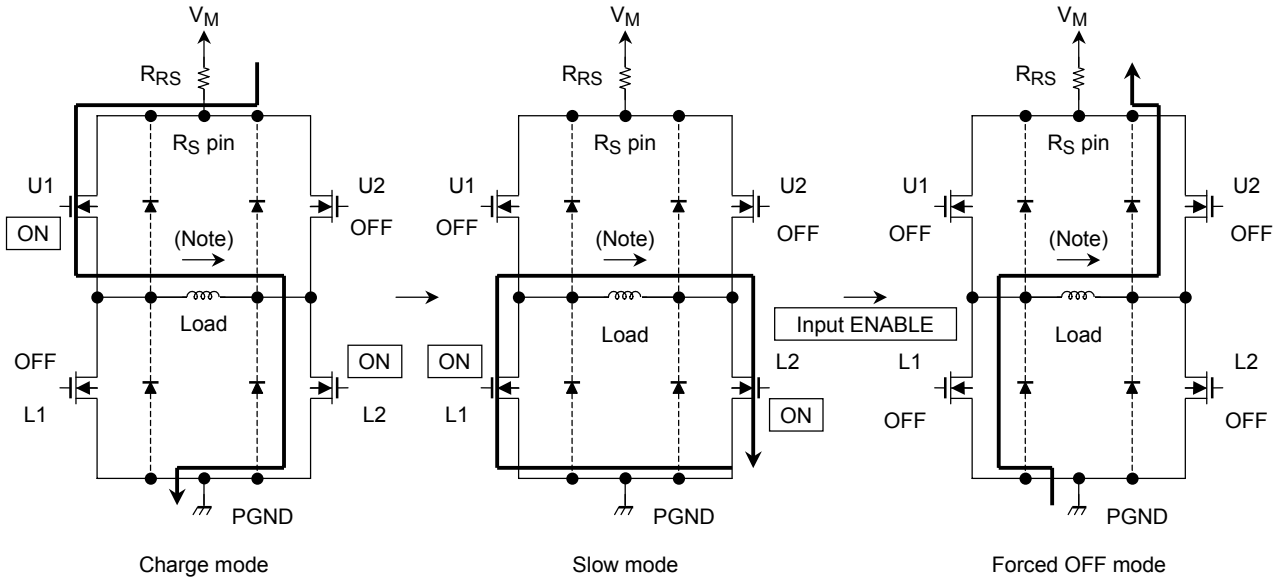
CLK Signal, Internal CR CLK, and Output Current Waveform (when CLK signal is input in 2 excitation mode)



Current Discharge Path when ENABLE Input During Operation

In Slow Mode, when all output transistors are forced to switch off, coil energy is discharged in the following MODES:

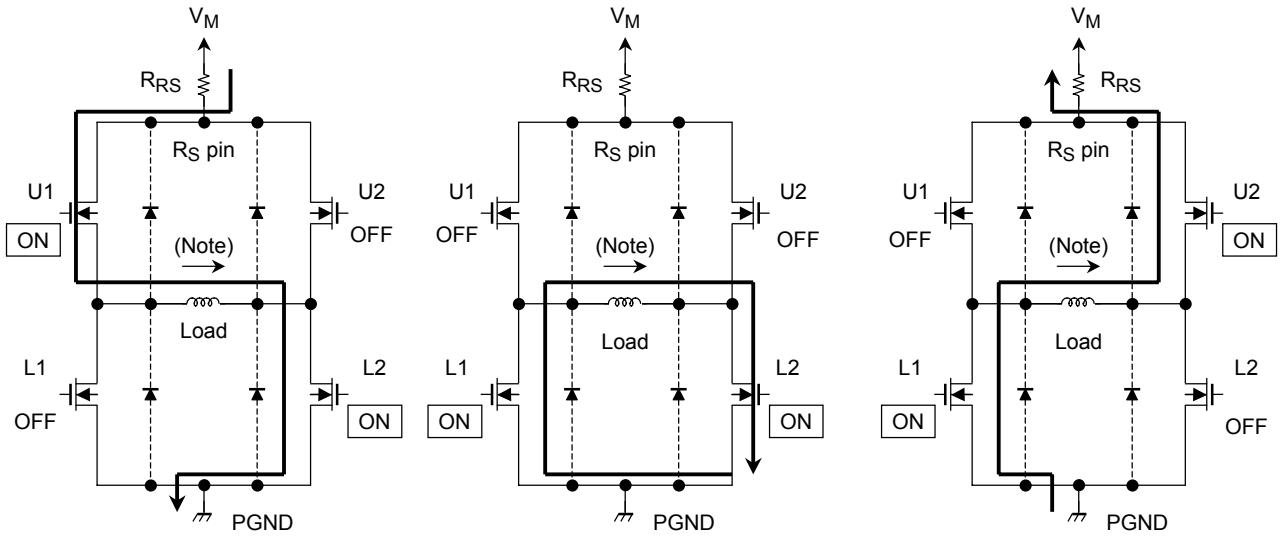
Note: Parasitic diodes are located on dotted lines. In normal MIXED DECAY MODE, the current does not flow to the parasitic diodes.



As shown in the figure above, an output transistor has parasitic diodes.

To discharge energy from the coil, each transistor is switched on allowing current to flow in the reverse direction to that in normal operation. As a result, the parasitic diodes are not used. If all the output transistors are forced to switch off, the energy of the coil is discharged via the parasitic diodes.

Output Transistor Operating Mode



Charge mode
Current flows into the coil.

Slow mode
Current flows between the coil and the IC.

Fast mode
The energy in the coil flows back to the power supply.

Output Transistor Operation Functions

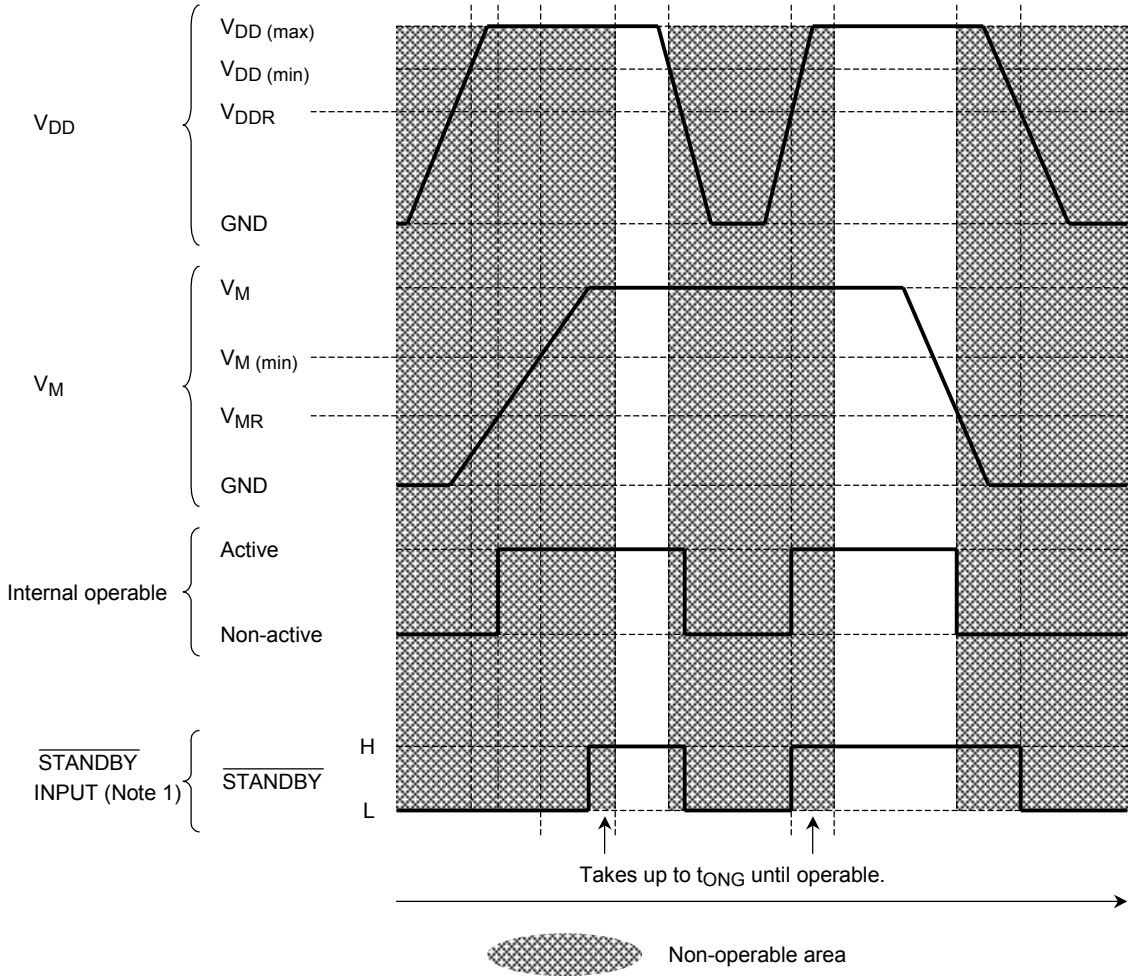
CLK	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above table is an example where current flows in the direction of the arrows in the above figures. When the current flows in the opposite direction of the arrows, see the table below.

CLK	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

In this IC, three modes as shown above are automatically switched to control the constant current.

Power Supply Sequence (recommended)



Note 1: If the V_{DD} drops to the level of the V_{DDR} or below while the specified voltage is input to the V_M pin, the IC is internally reset.
This is a protective measure against malfunction. Likewise, if the V_M drops to the level of the V_{MR} or below while regulation voltage is input to the V_{DD}, the IC is internally reset as a protective measure against malfunction.
To avoid malfunction, when turning on V_M or V_{DD}, to input the $\overline{\text{STANDBY}}$ signal at the above timing is recommended.
It takes time for the output control charge pump circuit to stabilize. Wait up to t_{ONG} time after power on before driving the motors.

Note 2: When the V_M value is between 8 to 11 V, the internal reset is released, thus output may be on. In such a case, the charge pump cannot drive stably because of insufficient voltage. The Standby state should be maintained until V_M reaches 13 V or more.

Note 3: Since V_{DD} = 0 V and V_M = voltage within the rating are applied, output is turned off by internal reset.
At that time, a current of several mA flows due to the Pass between V_M and V_{DD}.
When voltage increases on V_{DD} output, make sure that specified voltage is input.

How to Calculate Set Current

This IC drives the motor, controlling the PWM constant current in reference to the frequency of CR oscillator.

At that time, the maximum current value (set current value) can be determined by setting the sensing resistor (R_{RS}) and reference voltage (V_{ref}).

$$I_{OUT\,(max)} = \frac{1}{5.0} \times V_{ref}\ (V) \times \frac{Torque\ (Torque = 100, 71\%)}{R_{RS}\ (\Omega) \times 100(\%)}$$

1/5.0 is V_{ref} (gain): V_{ref} attenuation ratio. (for the specifications, see the electrical characteristics.)

For example, when applying V_{ref} = 3 V and torque = 100% to drive out I_{OUT} of 0.8 A, R_{RS} = 0.75 Ω (0.5 W or more) is required.
(for 1-2 phase excitation with 71% of torque, the peak current should be set to 100%).

How to Calculate the Chopping and OSC Frequencies

At constant current control, this IC chops frequency using the oscillation waveform (saw tooth waveform) determined by external capacitor and resistor as a reference.

The TB62206F requires an oscillation frequency of eight times the chopping frequency.

The oscillation frequency is calculated as follows:

$$f_{CR} = \frac{1}{0.523 \times (C \times R + 600 \times C)}$$

For example, when C_{osc} = 560 pF and R_{osc} = 3.6 kΩ are connected, f_{CR} = 813 kHz.

At this time, the chopping frequency f_{chop} is calculated as follows:

$f_{chop} = f_{CR}/8 = 101$ kHz

IC Power Dissipation

IC power dissipation is classified into two: power consumed by transistors in the output block and power consumed by the logic block and the charge pump circuit.

- Power consumed by the Power Transistor (calculated with R_{ON} = 0.60 Ω)
- In Charge mode, Fast Decay mode, or Slow Decay mode, power is consumed by the upper and lower transistors of the H bridges.

The following expression expresses the power consumed by the transistors of a H bridge.

$$P\ (out) = 2\ (T_r) \times I_{OUT}\ (A) \times V_{DS}\ (V) = 2 \times I_{OUT}^2 \times R_{ON} \quad \ldots\ldots (1)$$

The average power dissipation for output under 4-bit micro step operation (phase difference between phases A and B is 90°) is determined by expression (1).
Thus, power dissipation for output per unit is determined as follows (2) under the conditions below.

R_{ON} = 0.60 Ω (@1.0 A)
I_{OUT} (Peak: max) = 1.0 A
V_M = 24 V
V_{DD} = 5 V

$$P\ (out) = 2\ (T_r) \times 1.0^2\ (A) \times 0.60 \times 2\ (\Omega) = 2.40\ (W) \quad \ldots\ldots (2)$$

Power consumed by the logic block and IM
The following standard values are used as power dissipation of the logic block and IM at operation.

I (LOGIC) = 4.0 mA (typ.):
I (I_{M3}) = 15.0 mA (typ.): operation/unit
I (I_{M1}) = 4.0 mA (typ.): stop/unit

The logic block is connected to V_{DD} (5 V). IM (total of current consumed by the circuits connected to V_M and current consumed by output switching) is connected to V_M (24 V). Power dissipation is calculated as follows:

$$P\ (Logic\&IM) = 5\ (V) \times 0.004\ (A) + 24\ (V) \times 0.015\ (A) = 0.38\ (W) \quad \ldots\ldots (3)$$

Thus, the total power dissipation (P) is

$$P = P\ (out) + P\ (Logic\&IM) = 2.78\ (W)$$

Power dissipation at standby is determined as follows:

$$P\ (standby) + P\ (out) = 24\ (V) \times 0.004\ (A) + 5\ (V) \times 0.004\ (A) = 0.116\ (W)$$

For thermal design on the board, evaluate by mounting the IC.

Test Waveforms

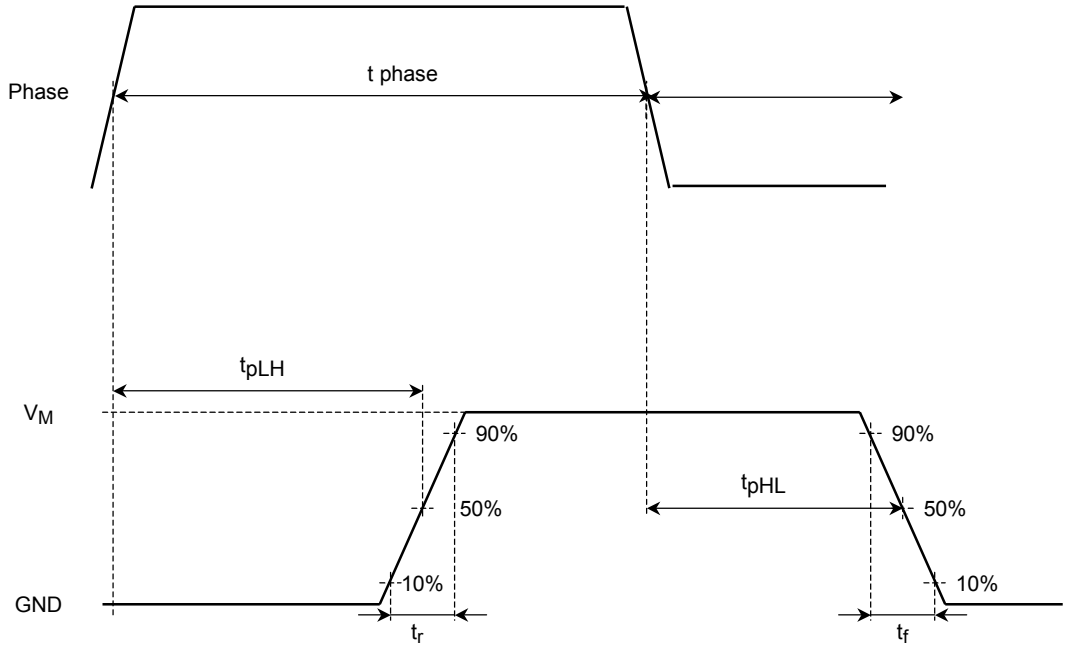
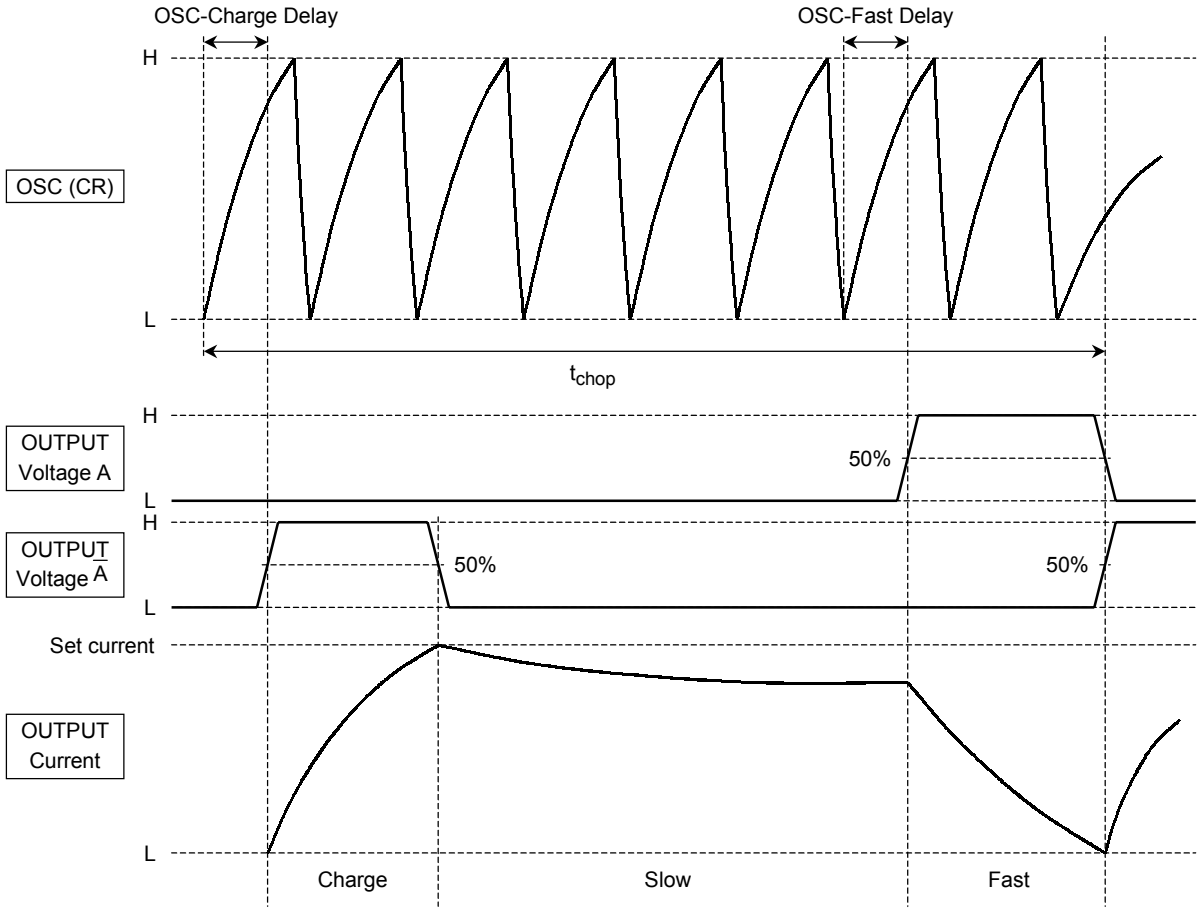


Figure 1 Timing Waveforms and Names



OSC-Charge DELAY:

Because the rising edge level of the OSC waveform is used for converting the OSC waveform to the internal CR CLK, a delay of up to 1.25 ns (@f_{chop} = 100 kHz: f_{CR} = 400 kHz) occurs between the OSC waveform and the internal CR CLK.

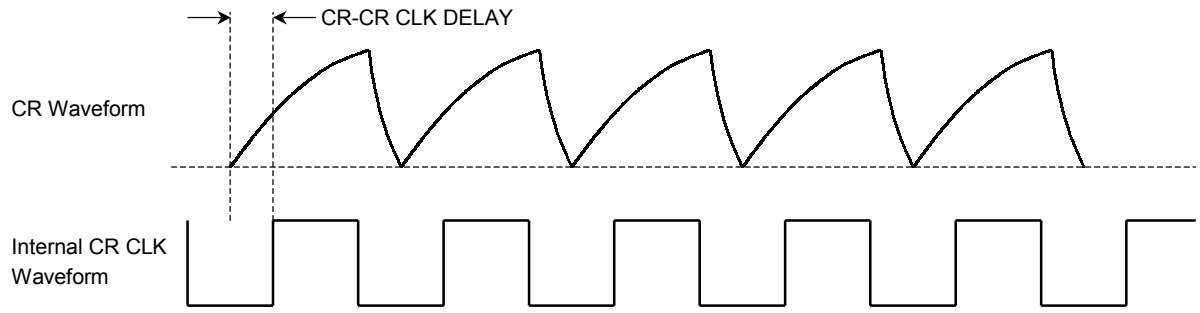
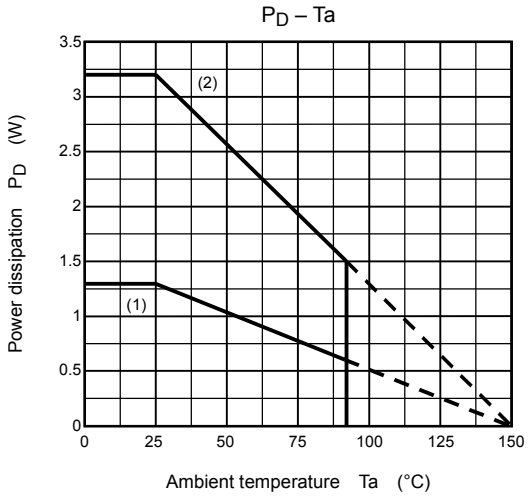


Figure 2 Timing Waveforms and Names (CR and output)

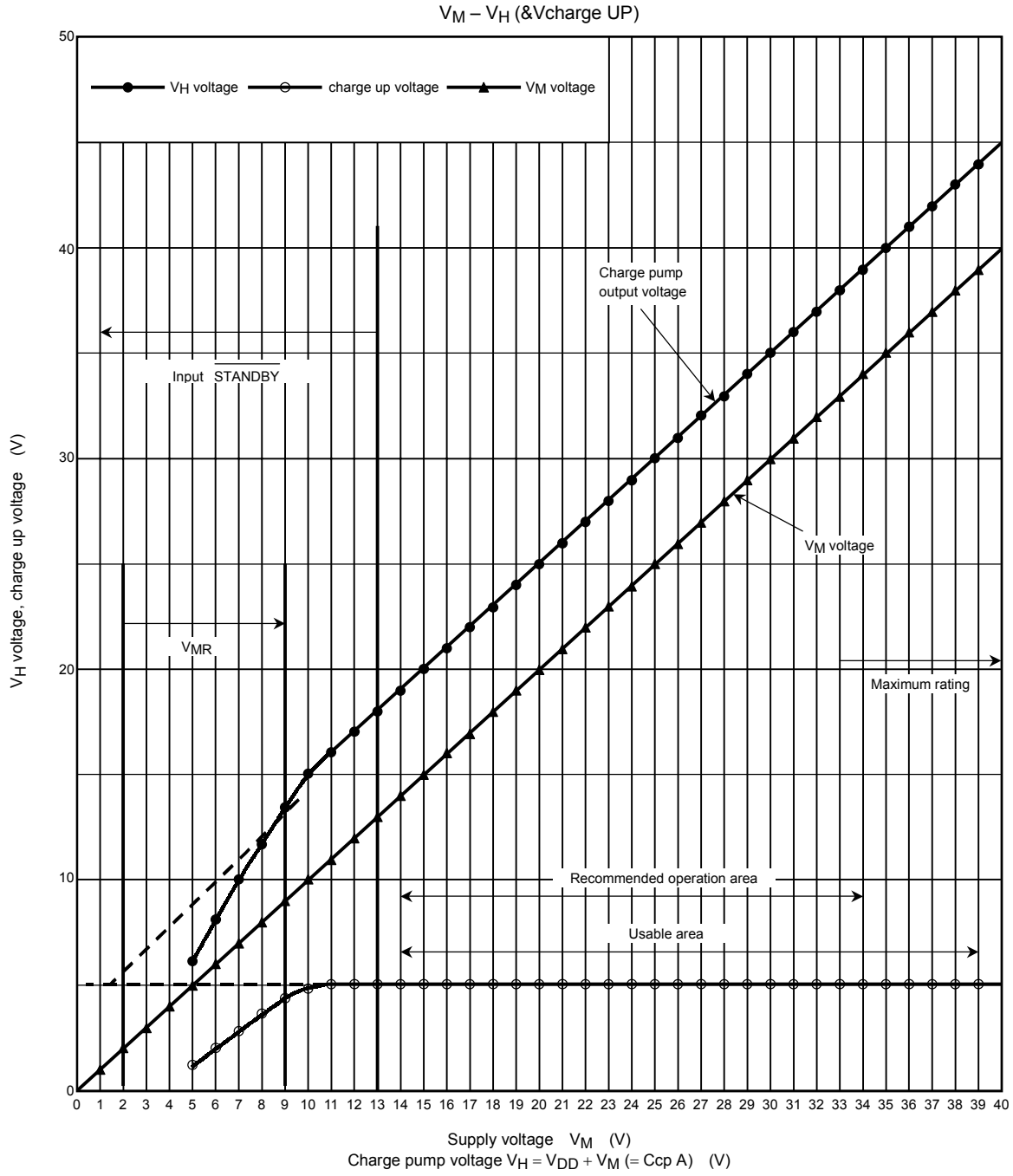
P_D – Ta (package power dissipation)



(4) HSOP20 $R_{th\ (j\text{-}a)}$ only (96°C/W)
(5) When mounted on the board (140 mm × 70 mm × 1.6 mm: 38°C/W: typ.: under evaluation)

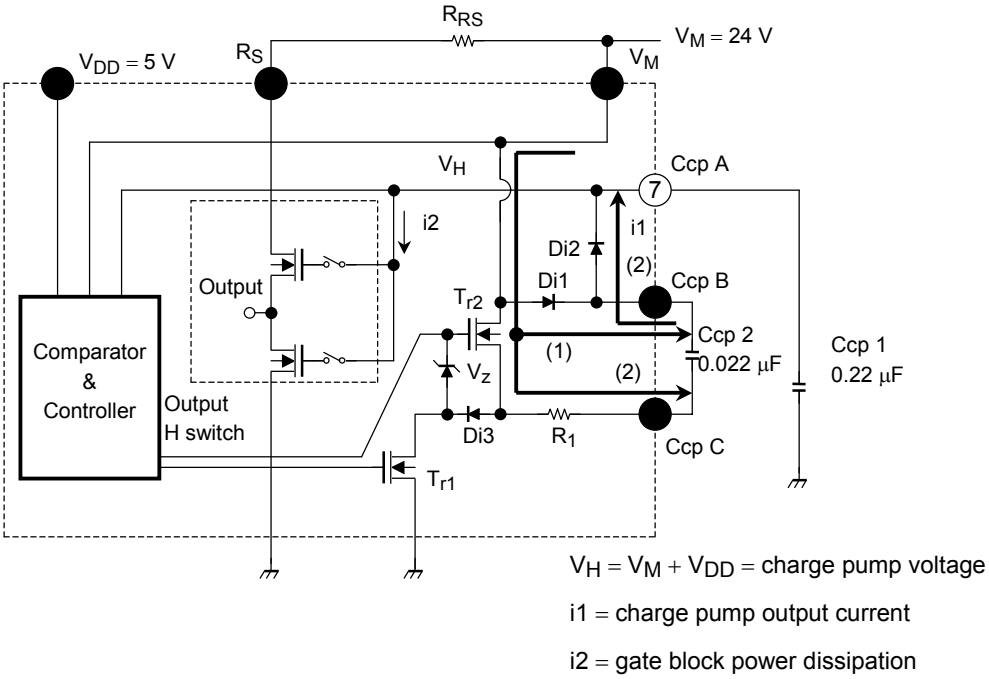
Note: $R_{th\ (j\text{-}a)}$: 8.5°C/W

Relationship between V_M and V_H (charge pump voltage)

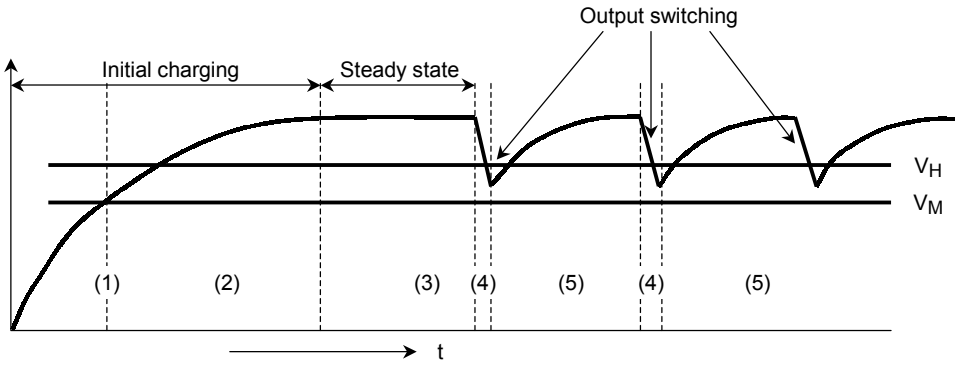


Note: V_{DD} = 5 V

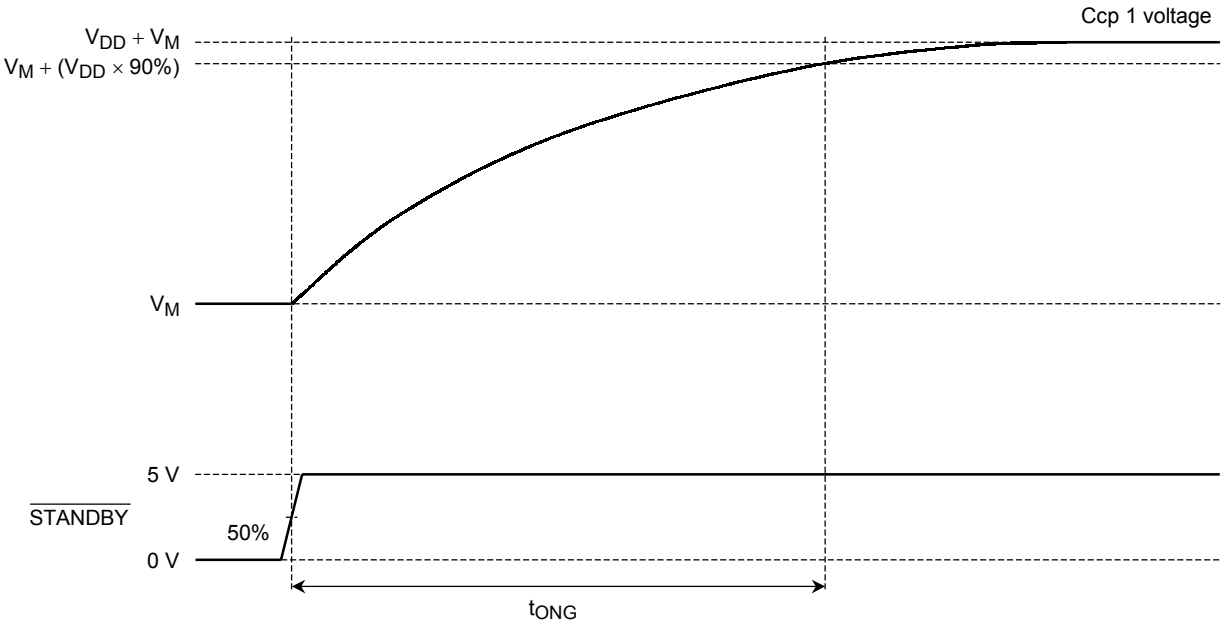
Operation of Charge Pump Circuit



- Initial charging
  - (1) When RESET is released, T_{r1} is turned ON and T_{r2} turned OFF. Ccp 2 is charged from Ccp 2 via Di1.
  - (2) T_{r1} is turned OFF, T_{r2} is turned ON, and Ccp 1 is charged from Ccp 2 via Di2.
  - (3) When the voltage difference between V_M and V_H (Ccp A pin voltage = charge pump voltage) reaches V_{DD} or higher, operation halts (steady state).
- Actual operation
  - (4) Ccp 1 charge is used at f_{chop} switching and the V_H potential drops.
  - (5) Charges up by (1) and (2) above.



Charge Pump Rise Time



t_{ONG}:

Delay time taken for capacitor Ccp 2 (charging capacitor) to fill up Ccp 1 (storing capacitor) to $V_M + V_{DD}$ after $\overline{STANDBY}$ is released.

The internal IC cannot drive the gates correctly until the voltage of Ccp 1 reaches $V_M + V_{DD}$. Be sure to wait for t_{ONG} or longer before driving the motors.

Basically, the larger the Ccp 1 capacitance, the smaller the voltage fluctuation, though the initial charge up time is longer.

The smaller the Ccp 1 capacitance, the shorter the initial charge-up time but the voltage fluctuation is larger.

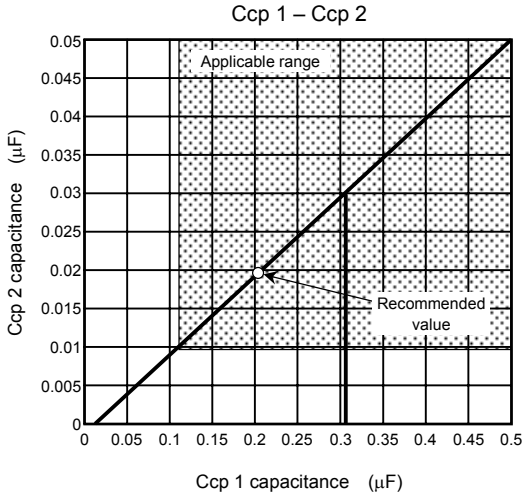
Depending on the combination of capacitors (especially with small capacitance), voltage may not be sufficiently boosted.

When the voltage does not increase sufficiently, output DMOS R_{ON} turns lower than the normal, and it raises the temperature.

Thus, use the capacitors under the capacitor combination conditions (Ccp 1 = 0.22 μF, Ccp 2 = 0.022 μF) recommended by Toshiba.

External Capacitor for Charge Pump

When driving the stepping motor with V_{DD} = 5 V, f_{chop} = 150 kHz, L = 10 mH under the conditions of V_M = 13 V and 1.5 A, the logical values for Ccp 1 and Ccp 2 are as shown in the graph below:



Choose Ccp 1 and Ccp 2 to be combined from the above applicable range. We recommend Ccp 1:Ccp 2 at 10:1 or more. (if our recommended values (Ccp = 0.22 μF, Ccp 2 = 0.02 μF) are used, the drive conditions in the specification sheet are satisfied. (there is no capacitor temperature characteristic as a condition.)

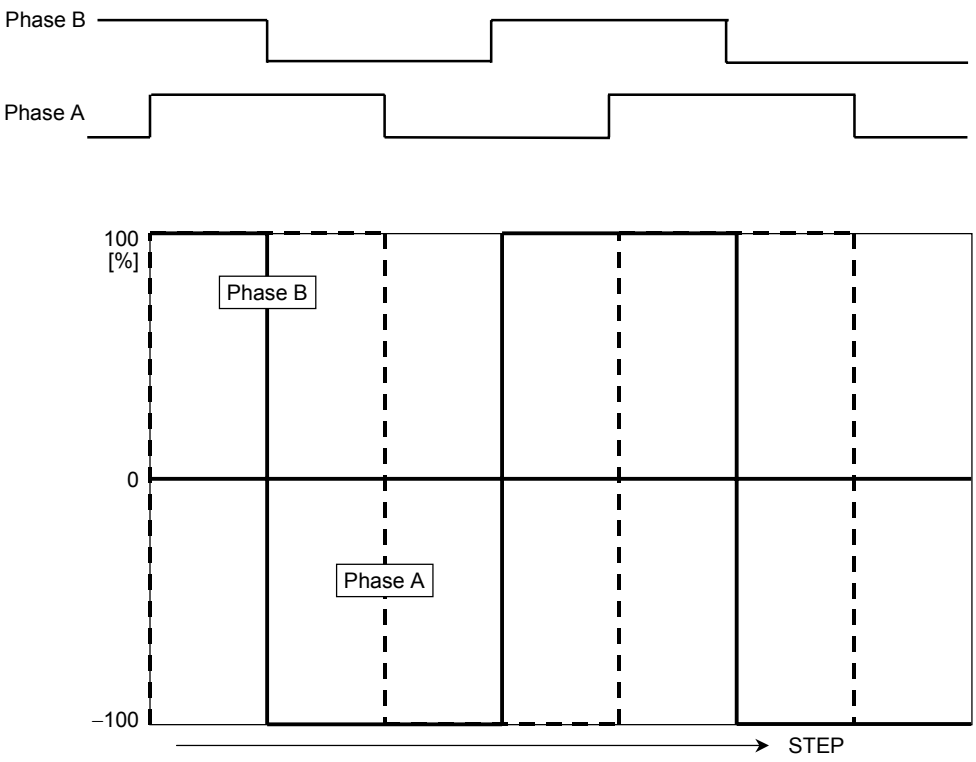
When setting the constants, make sure that the charge pump voltage is not below the specified value and set the constants with a margin (the larger Ccp 1 and Ccp 2, the more the margin).

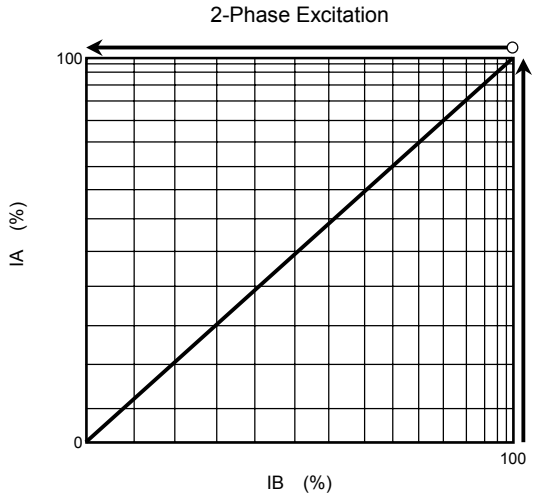
Some capacitors exhibit a large change in capacitance according to the temperature. Make sure the above capacitance is obtained under the usage environment temperature.

Driving Mode

2-Phase Excitation Mode

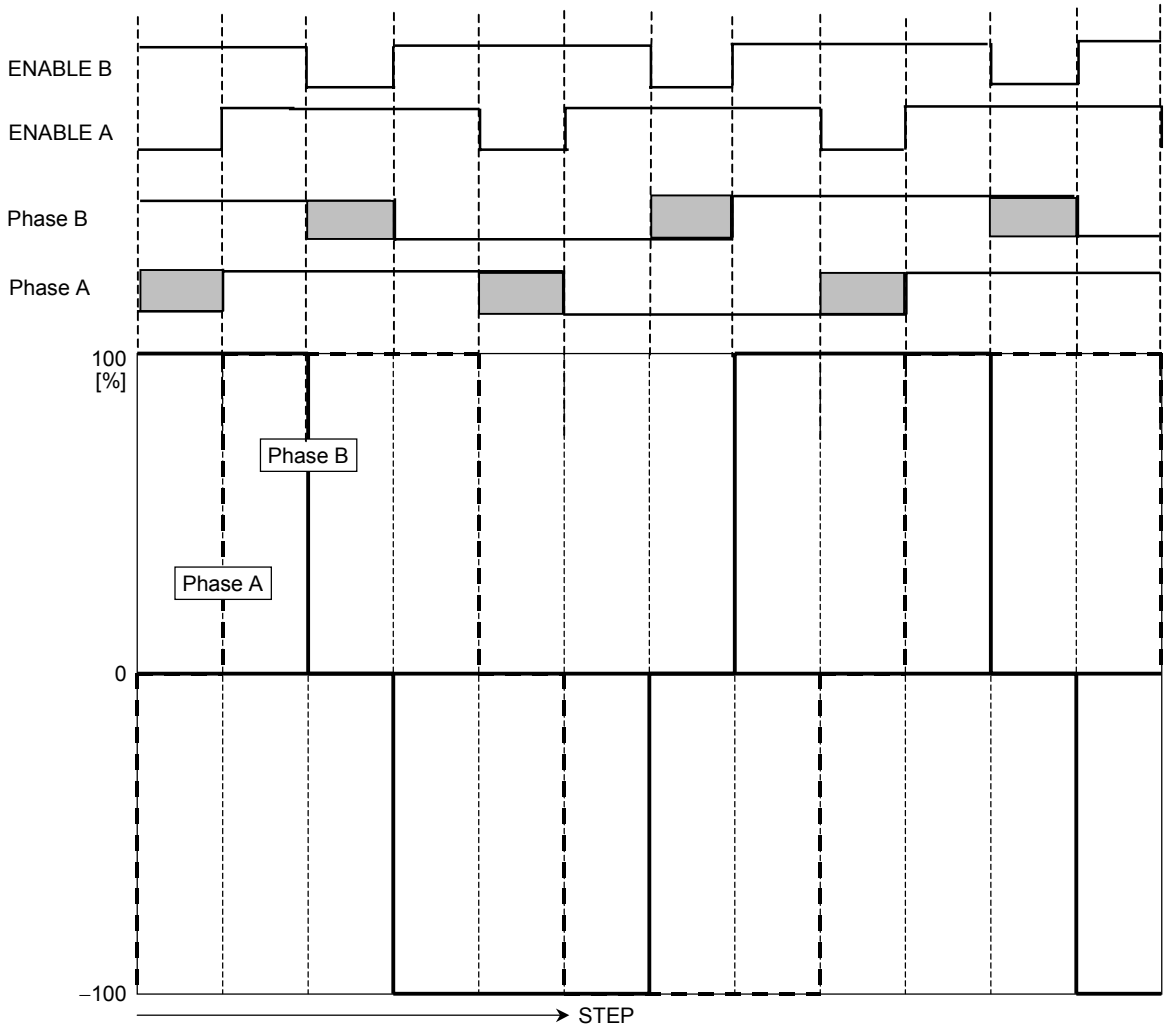
2-Phase Excitation

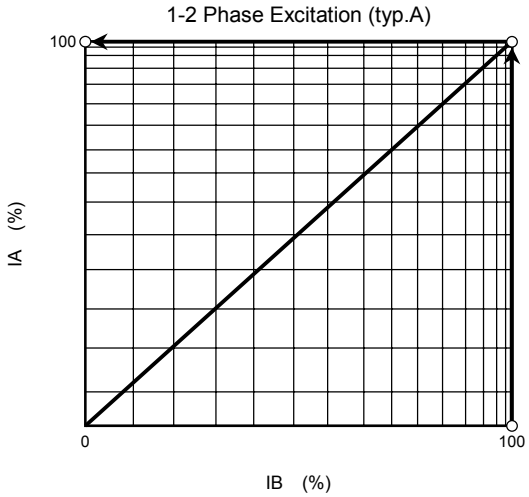




Note: 2-phase excitation has a large load change due to motor induced electromotive force. If a mode in which the current attenuation capability (current control capability) is small is used, current increase due to induced electromotive force may not be suppressed.

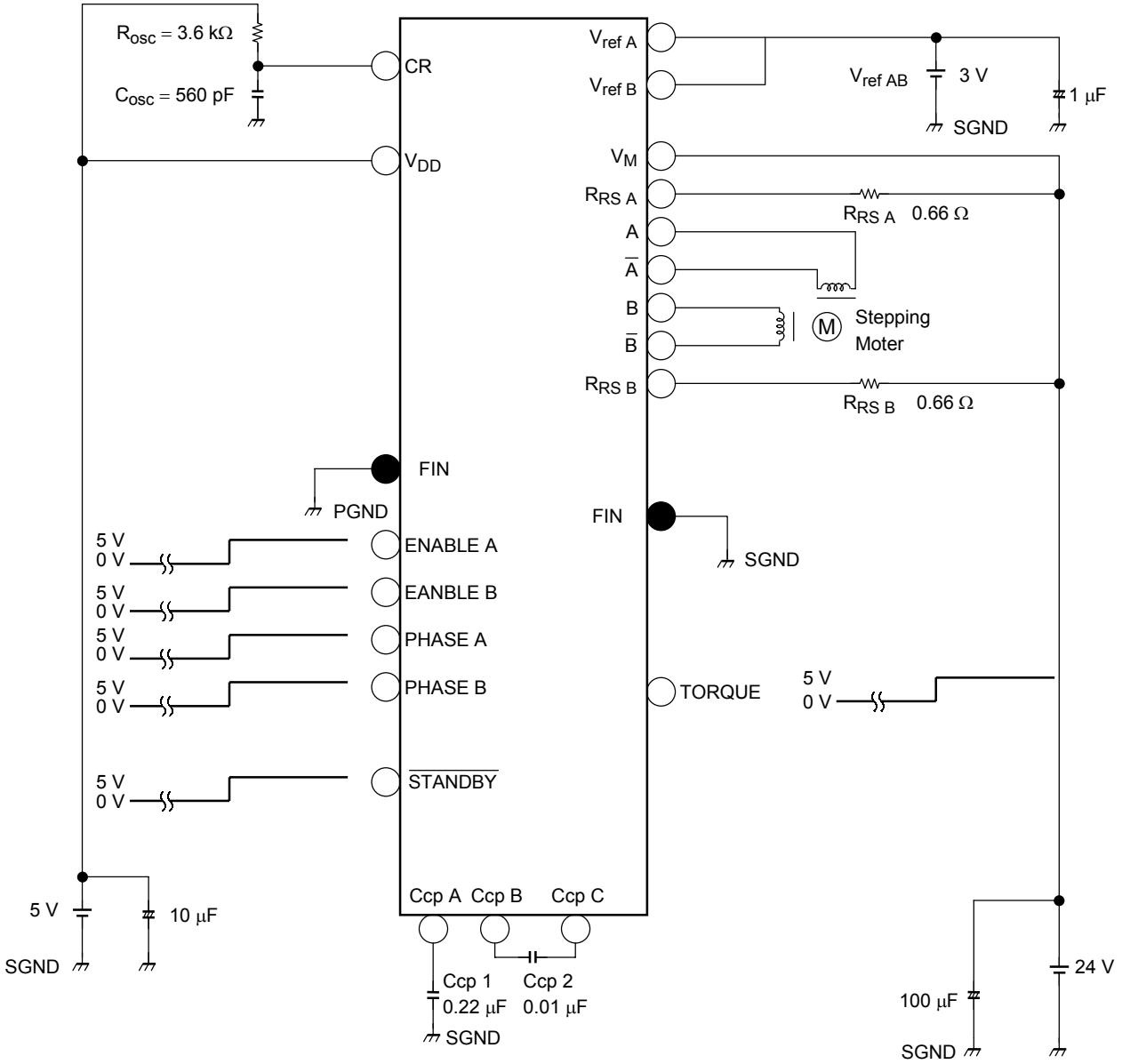
1-2 Phase Excitation





Recommended Application Circuit

The values for the respective devices are all recommended values. For values under each input condition, see the above-mentioned recommended operating conditions.

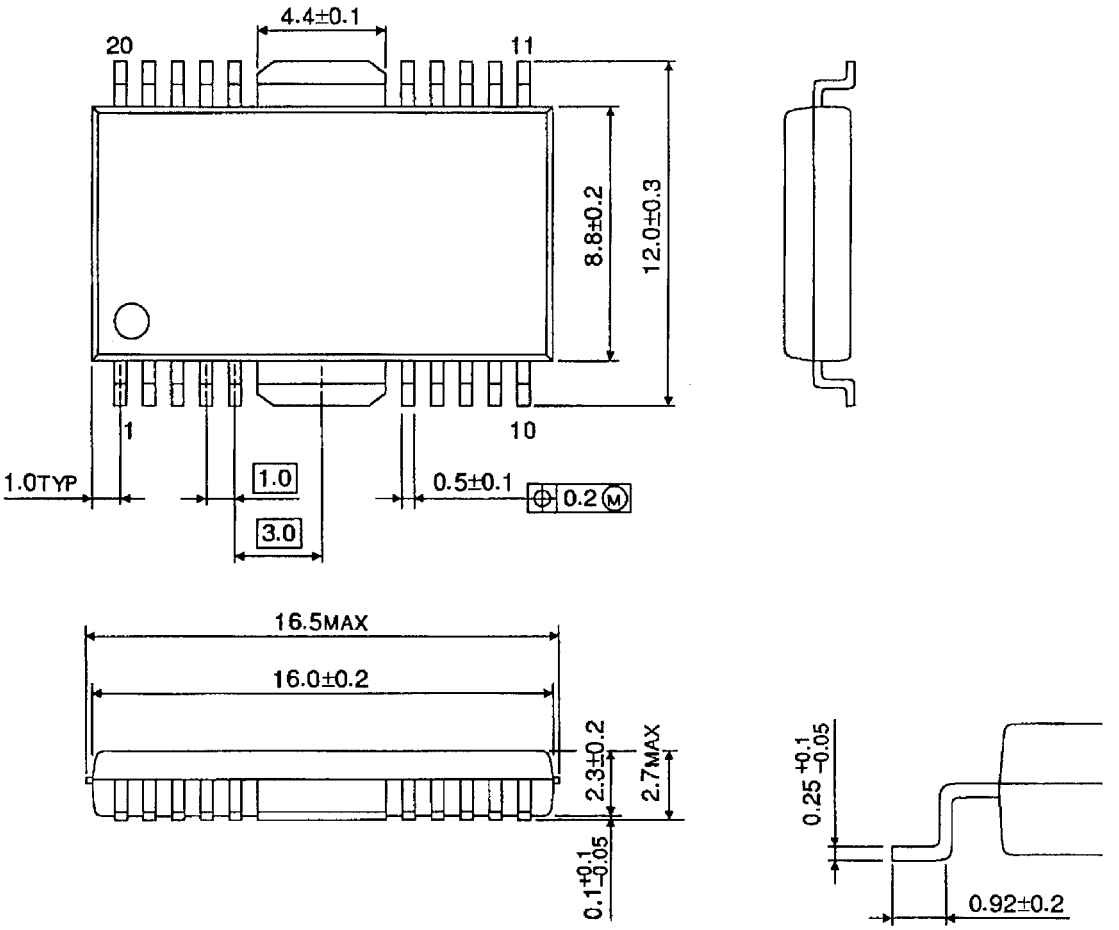


Note: Adding bypass capacitors is recommended.
Make sure that GND wiring has only one contact point, and to design the pattern that allows the heat radiation.
To control setting pins in each mode by SW, make sure to pull down or pull up them to avoid high impedance.
To input the data, see the section on the recommended input data.

The IC may be destroyed due to short circuit between output pins, an output pin and the V_{DD} pin, or an output pin and the GND pin.
Design an output line, V_{DD} (V_M) line and GND line with great care.
Also a low-withstand-voltage device may be destroyed when mounted in the wrong orientation, which causes high-withstanding voltage to be applied to the device.

Package Dimensions

HSOP20-P-450-1.00 Unit : mm



Weight: 0.79 g (typ.)

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