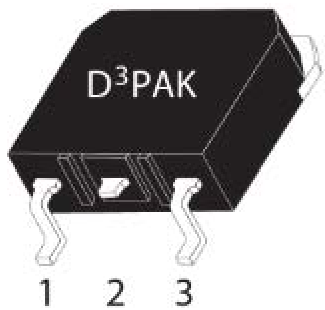
1200V, 17 mΩ N-Channel mSiC™ MOSFET

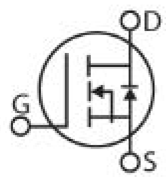
MSC017SMA120S

Product Overview

1200V, 17 mΩ typical at 20 V_{GS}, 19 mΩ typical at 18 V_{GS}, Silicon Carbide (SiC) N-Channel MOSFET, D3PAK.



1—Gate
2—Drain
3—Source
Backside—Drain



Features

- Low capacitances and low gate charge
- Fast switching speed due to low internal gate resistance (ESR)
- Stable operation at high junction temperature, $T_{J(max)}$ = 175 °C
- Fast and reliable body diode
- Superior avalanche ruggedness
- RoHS compliant

Benefits

- High efficiency to enable lighter and more compact system
- Simple to drive and easy to parallel
- Improved thermal capabilities and lower switching losses
- Eliminates the need for external freewheeling diode
- Lower system cost of ownership

Applications

- Photovoltaic (PV) inverter, converter, and industrial motor drives
- Smart grid transmission and distribution
- Induction heating and welding
- Hybrid Electric Vehicle (HEV) powertrain and Electric Vehicle (EV) charger
- Power supply and distribution

1. Device Specifications

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain source voltage	1200	V
I_D	Continuous drain current at T_C = 25 °C	114	A
	Continuous drain current at T_C = 100 °C	80	
I_{DM}	Pulsed drain current[1]	280	
V_{GS}	Gate-source voltage	23 to –10	V
	Transient gate-source voltage	25 to –12	
P_D	Total power dissipation at T_C = 25 °C	524	W
	Linear derating factor	3.45	W/°C

Note:

1. Repetitive rating: pulse width and case temperature are limited by the maximum junction temperature.

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic/Test Conditions	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance	—	0.22	0.29	°C/W
T_J	Operating junction temperature	–55	—	175	°C
T_{STG}	Storage temperature	–55	—	150	
—	Reflow temperature	—	—	260	°C
Wt	Package weight	—	0.14	—	oz
		—	4.0	—	g

ESD practices should comply with JESD-625.

1.2 Electrical Performance

The following table shows the static characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0V, I_D = 100 µA	1200	—	—	V
$R_{DS(on)}$	Drain-source on resistance[1]	V_{GS} = 20V, I_D = 40A	—	17	22	mΩ
		V_{GS} = 18V, I_D = 40A	—	19	—	
$V_{GS(th)}$	Gate-source threshold voltage	V_{GS} = V_{DS}, I_D = 4.5 mA	1.9	3	—	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1200V, V_{GS} = 0V	—	0.3	40	µA
		V_{DS} = 1200V, V_{GS} = 0V, T_J = 175 °C	—	3.5	—	
I_{GSS}	Gate-source leakage current	V_{GS} = 20V/–10V	—	—	±100	nA

Note:

1. Pulse test: pulse width < 380 µs, duty cycle < 2%.

The following table shows the dynamic characteristics of this device. T_J = 25 °C unless otherwise specified. The dynamic characteristics are characterized, not 100% tested, at the recommended operating V_{GS} = 20V/−5V.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0V V_{DD} = 1000V V_{AC} = 25 mV ƒ = 200 KHz	—	4960	—	pF
C_{rss}	Reverse transfer capacitance		—	18	—	
C_{oss}	Output capacitance		—	263	—	
Q_g	Total gate charge	V_{GS} = –5V/20V V_{DD} = 800V I_D = 40A	—	249	—	nC
Q_{gs}	Gate-source charge		—	63	—	
Q_{gd}	Gate-drain charge		—	32	—	
$t_{d(on)}$	Turn-on delay time	V_{DD} = 800V V_{GS} = –5V/20V I_D = 50A $R_{g(ext)}$ = 4Ω Freewheeling diode = MSC017SMA120S (V_{GS} = –5V); reference Figure 1-18	—	52	—	ns
t_f	Voltage rise time		—	21	—	
$t_{d(off)}$	Turn-off delay time		—	49	—	
t_r	Voltage fall time		—	18	—	
E_{on}	Turn-on switching energy		—	1677	—	μJ
E_{off}	Turn-off switching energy		—	395	—	
ESR	Gate equivalent series resistance	f = 1 MHz, 25 mV, drain short	—	0.71	—	Ω
SCWT	Short circuit withstand time	V_{DS} = 960V, V_{GS} = 20V	—	3	—	μs
E_{AS}	Avalanche energy, single pulse	I_D = 40A	—	3500	—	mJ

The following table shows the body diode characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-5. Body Diode Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	I_{SD} = 40A, V_{GS} = 0V	—	3.5	—	V
		I_{SD} = 40A, V_{GS} = –5V	—	3.9	—	
t_{rr}	Reverse recovery time	I_{SD} = 50A, V_{GS} = –5V, Drive R_g = 4Ω, V_{DD} = 800V, dI/dt = –2500 A/μs	—	40	—	ns
Q_{rr}	Reverse recovery charge		—	490	—	nC
I_{RRM}	Reverse recovery current		—	22	—	A

1.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Drain Current vs. V_{DS} at T_J

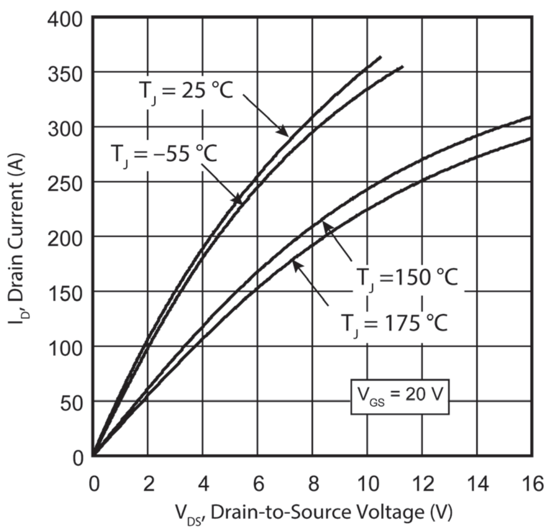


Figure 1-2. Drain Current vs. V_{DS} at V_{GS}

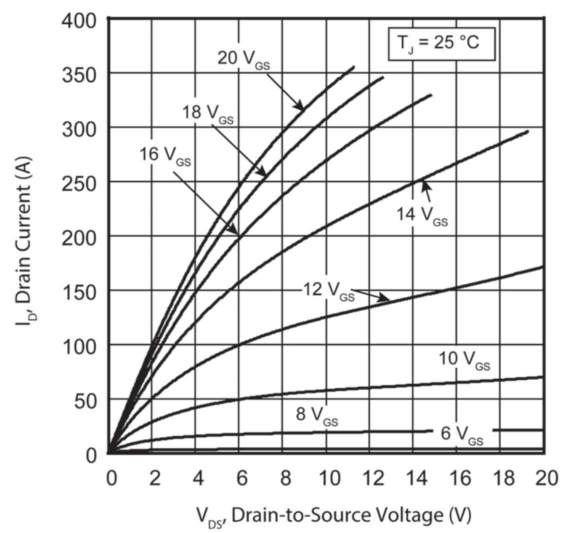


Figure 1-3. Drain Current vs. V_{DS} at V_{GS}

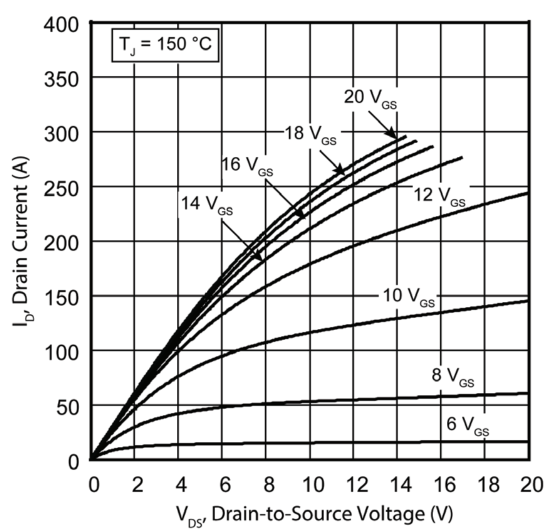


Figure 1-4. Drain Current vs. V_{DS} at V_{GS}

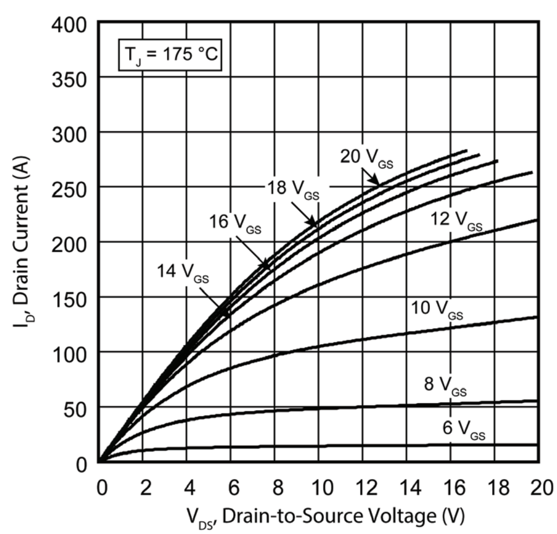


Figure 1-5. $R_{DS(on)}$ vs. Junction Temperature

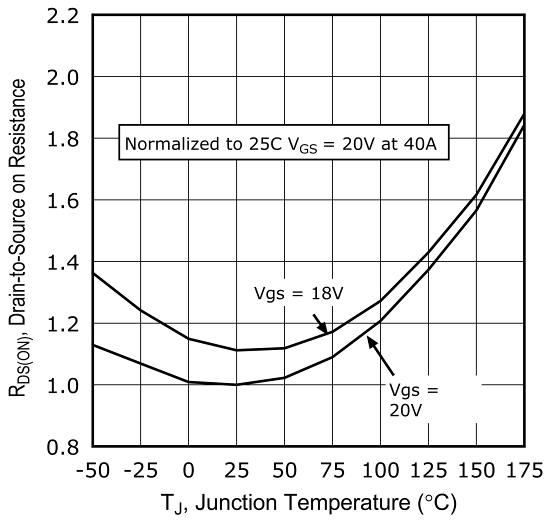


Figure 1-6. Gate Charge Characteristics

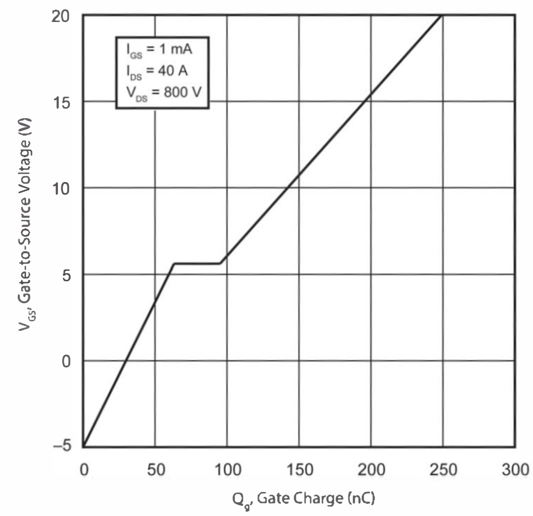


Figure 1-7. Capacitance vs. Drain-to-Source Voltage

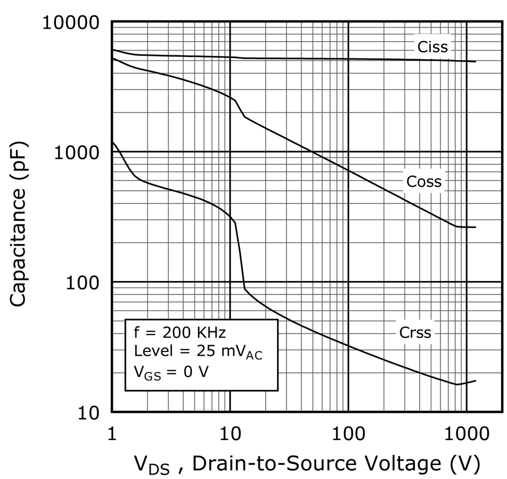


Figure 1-8. Output Charge vs. Drain-to-Source Voltage

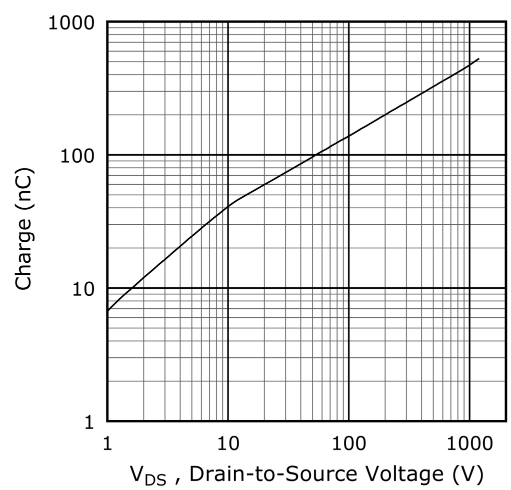


Figure 1-9. I_D vs. V_{DS} 3rd Quadrant Conduction

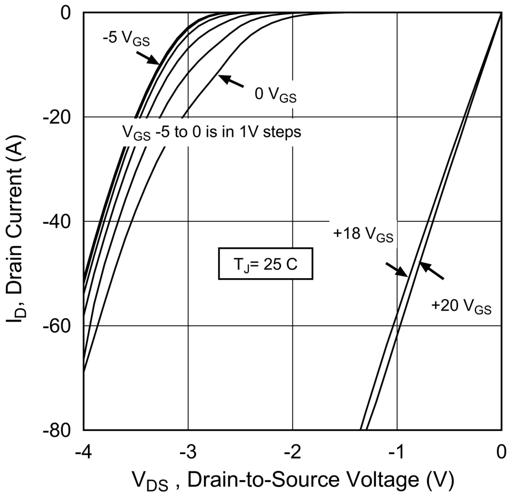


Figure 1-10. I_D vs. V_{DS} 3rd Quadrant Conduction

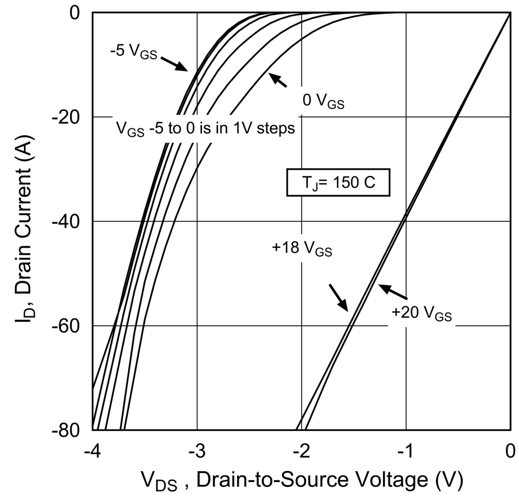


Figure 1-11. Switching Energy Eon vs. V_{DS} & I_D

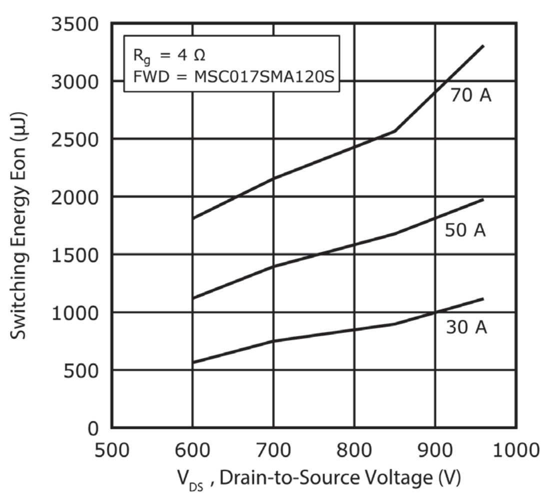


Figure 1-12. Switching Energy Eoff vs. V_{DS} & I_D

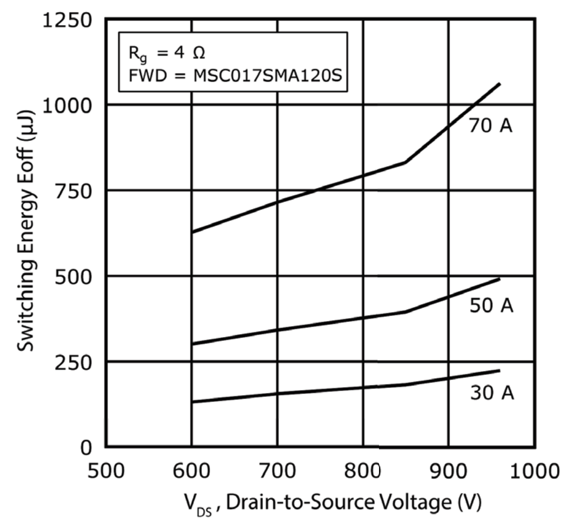


Figure 1-13. Switching Energy vs. R_g

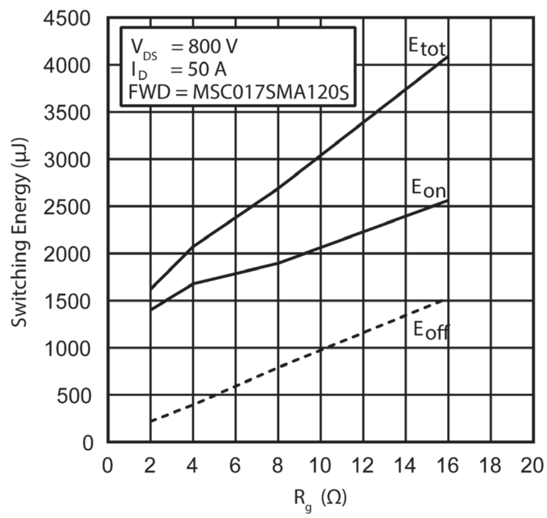


Figure 1-14. Switching Energy vs. Junction Temperature

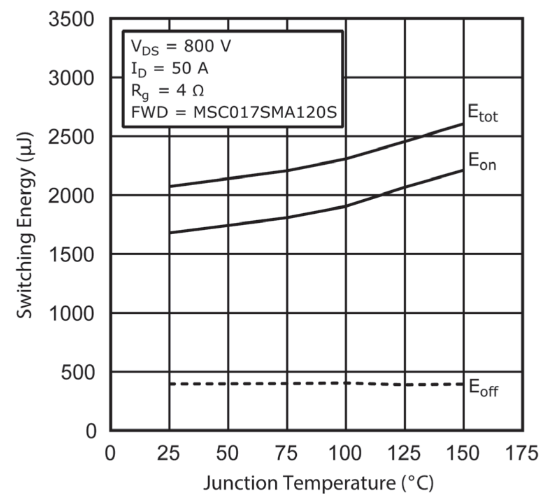


Figure 1-15. Threshold Voltage vs. Junction Temperature

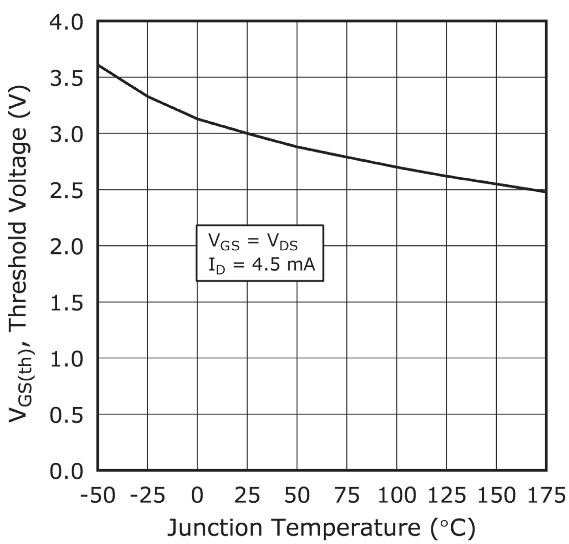


Figure 1-16. Forward Safe Operating Area

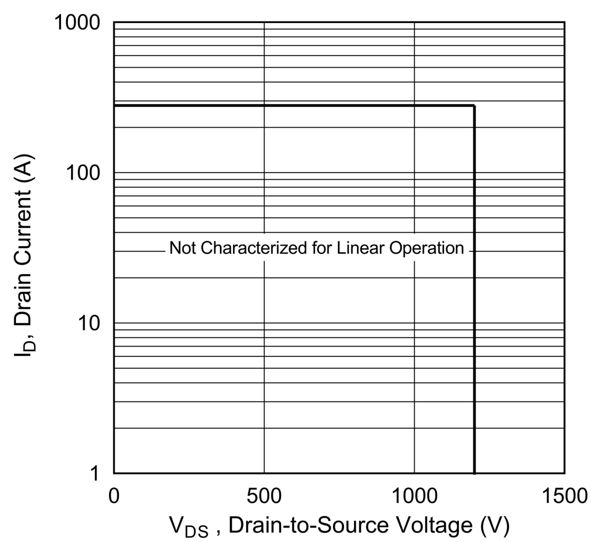
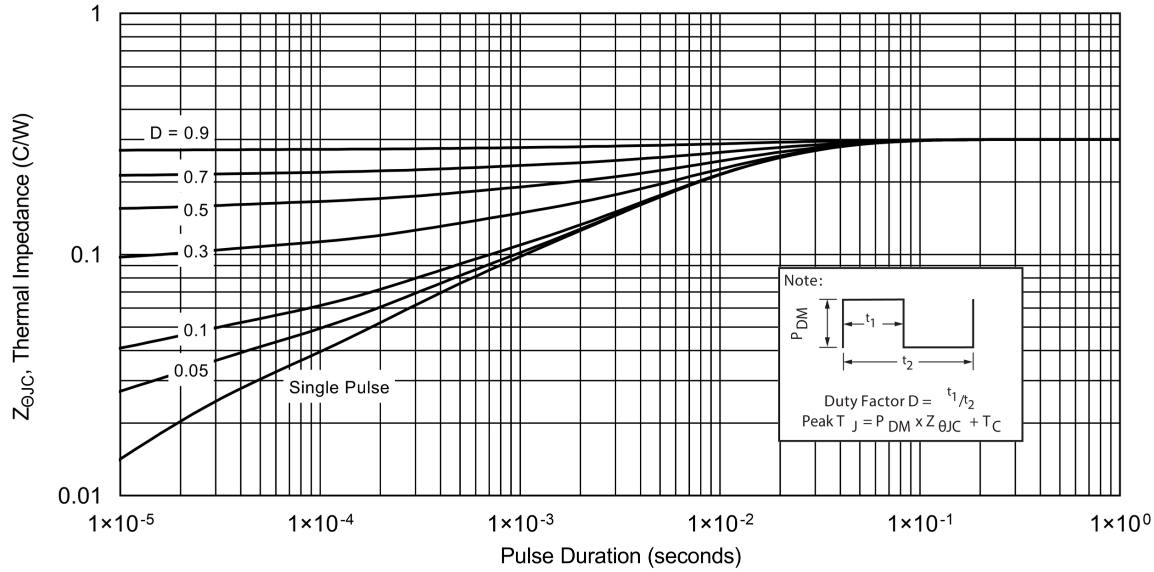
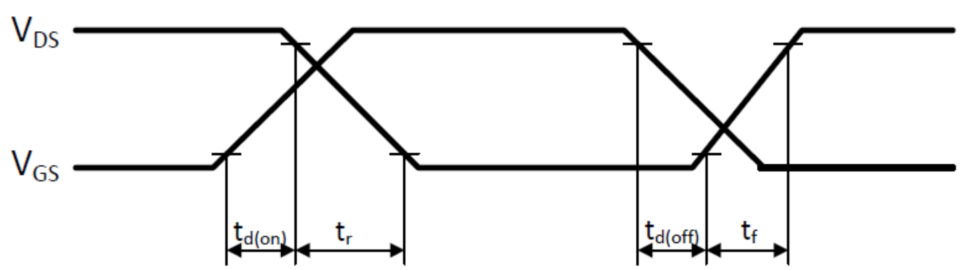


Figure 1-17. Maximum Transient Thermal Impedance



The following figure shows the switching waveform diagram of this device.

Figure 1-18. Switching Waveform



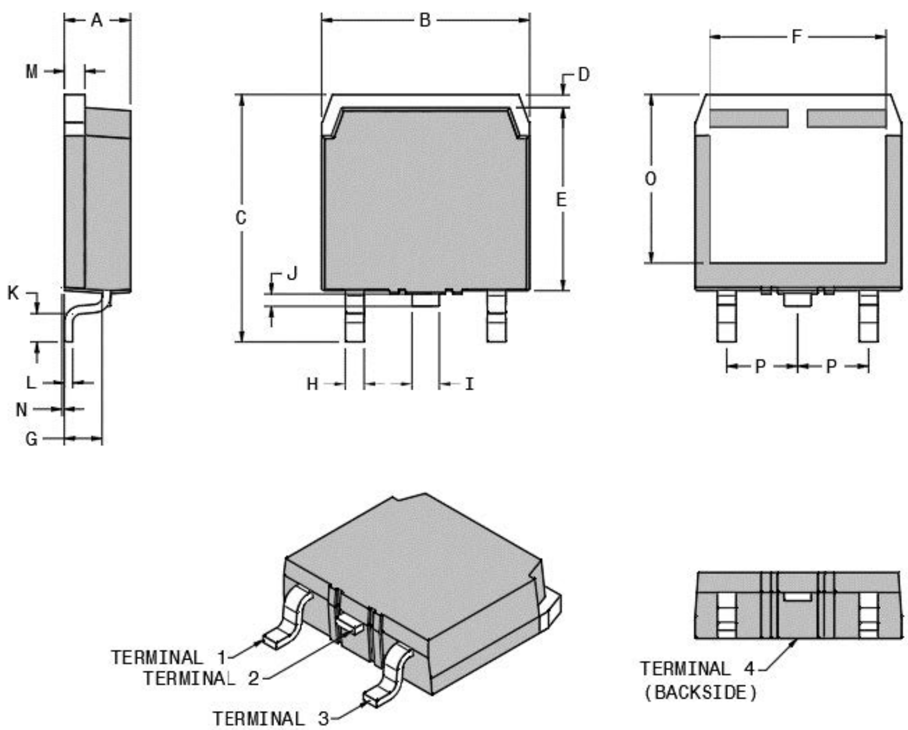
2. Package Specification

This section shows the package specification of this device.

2.1 Package Outline Drawing

The following figure illustrates the D3PAK package outline of this device.

Figure 2-1. Package Outline Drawing



The following table shows the D3PAK dimensions and should be used in conjunction with the package outline drawing.

Table 2-1. D3PAK Dimensions

Symbol	Min. (mm)	Max. (mm)	Min. (in.)	Max. (in.)
A	4.90	5.10	0.193	0.201
B	15.85	16.20	0.624	0.638
C	18.70	19.10	0.736	0.752
D	1.00	1.025	0.039	0.049
E	13.80	14.00	0.543	0.551
F	13.30	13.60	0.524	0.535
G	2.70	2.90	0.106	0.114
H	1.15	1.45	0.045	0.057
I	1.95	2.21	0.077	0.087
J	0.94	1.40	0.037	0.055
K	2.40	2.70	0.094	0.106
L	0.40	0.60	0.016	0.024

...........continued

Symbol	Min. (mm)	Max. (mm)	Min. (in.)	Max. (in.)
M	1.45	1.60	0.057	0.063
N	0.00	0.018	0.00	0.007
O	12.40	12.70	0.488	0.500
P	5.45 BSC (nom.)		0.215 BSC (nom.)	
Terminal 1	Gate			
Terminal 2	Drain			
Terminal 3	Source			
Terminal 4	Drain			

3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
A	09/2023	The following changes are made in this revision of the document: • Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00005091A, which replaces the previous Microsemi literature number 050-7781. • Added Figure 1-8. • Updated Figure 1-9, Figure 1-10 and Figure 1-15.
Initial release (Microsemi Revision A)	10/2020	Initial releases.

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