

SN74F657  
OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER  
AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

- Combines 'F245 and 'F280B Functions in One Package
- High-Impedance N-P-N Inputs for Reduced Loading (70  $\mu$ A in Low and High States)
- High Output Drive and Light Bus Loading
- 3-State B Outputs Sink 64 mA and Source 15 mA
- Input Diodes for Termination Effects
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

#### description

The SN74F657 contains eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a specified current sinking capability of 24 mA at the A port and 64 mA at the B port.

The transmit/receive ( $T/\bar{R}$ ) input determines the direction of the data flow through the bidirectional transceivers. When  $T/\bar{R}$  is high, data is transmitted from the A port to the B port. When  $T/\bar{R}$  is low, data is received at the A port from the B port.

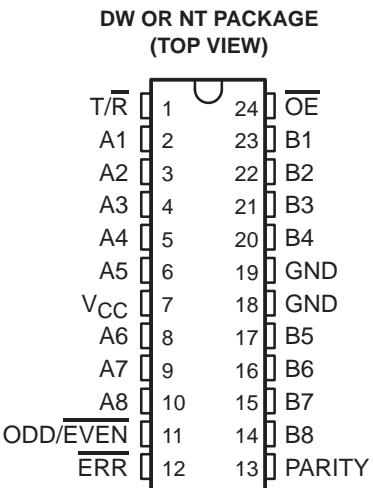
When the output enable ( $\bar{OE}$ ) input is high, both the A and B ports are placed in a high-impedance state (disabled). The ODD/EVEN input allows the user to select between odd or even parity systems. When transmitting from A port to B port ( $T/\bar{R}$  high), PARITY is an output from the generator/checker. When receiving from B port to A port ( $T/\bar{R}$  low), PARITY is an input.

When transmitting ( $T/\bar{R}$  high), the parity select (ODD/EVEN) input is made high or low as appropriate. The A port is then polled to determine the number of high bits. The PARITY output goes to the logic state determined by ODD/EVEN and the number of high bits on A port. When ODD/EVEN is low (for even parity) and the number of high bits on A port is odd, the PARITY will be high, transmitting even parity. If the number of high bits on A port is even, the PARITY will be low, keeping even parity.

When in the receive mode ( $T/\bar{R}$  low), the B port is polled to determine the number of high bits. If ODD/EVEN is low (for even parity) and the number of highs on B port is:

1. Odd and the PARITY input is high, then  $\bar{ERR}$  will be high signifying no error.
2. Even and the PARITY input is high, then  $\bar{ERR}$  will be low indicating an error.

The SN74F657 is characterized for operation from 0°C to 70°C.



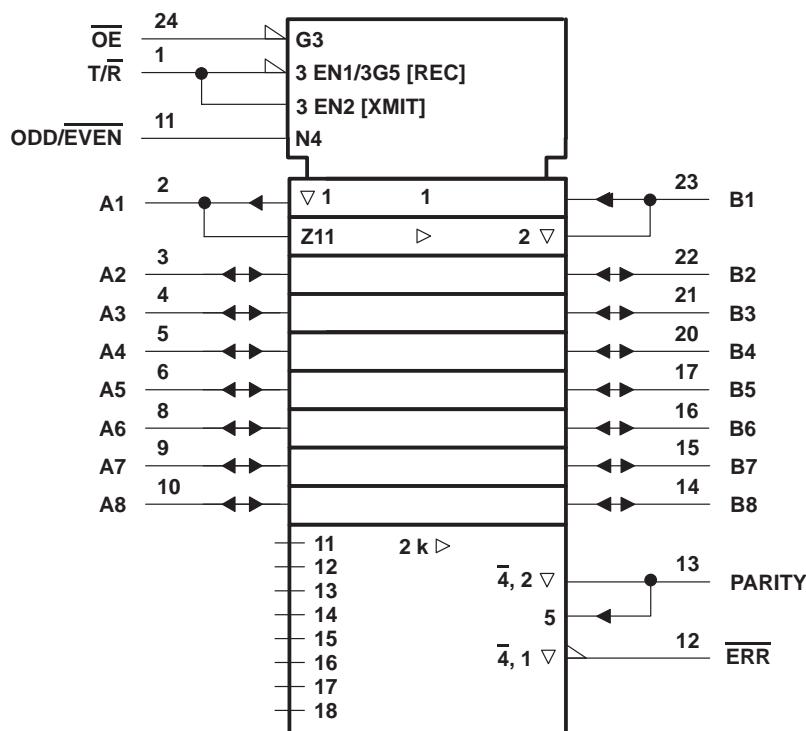
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FUNCTION TABLE

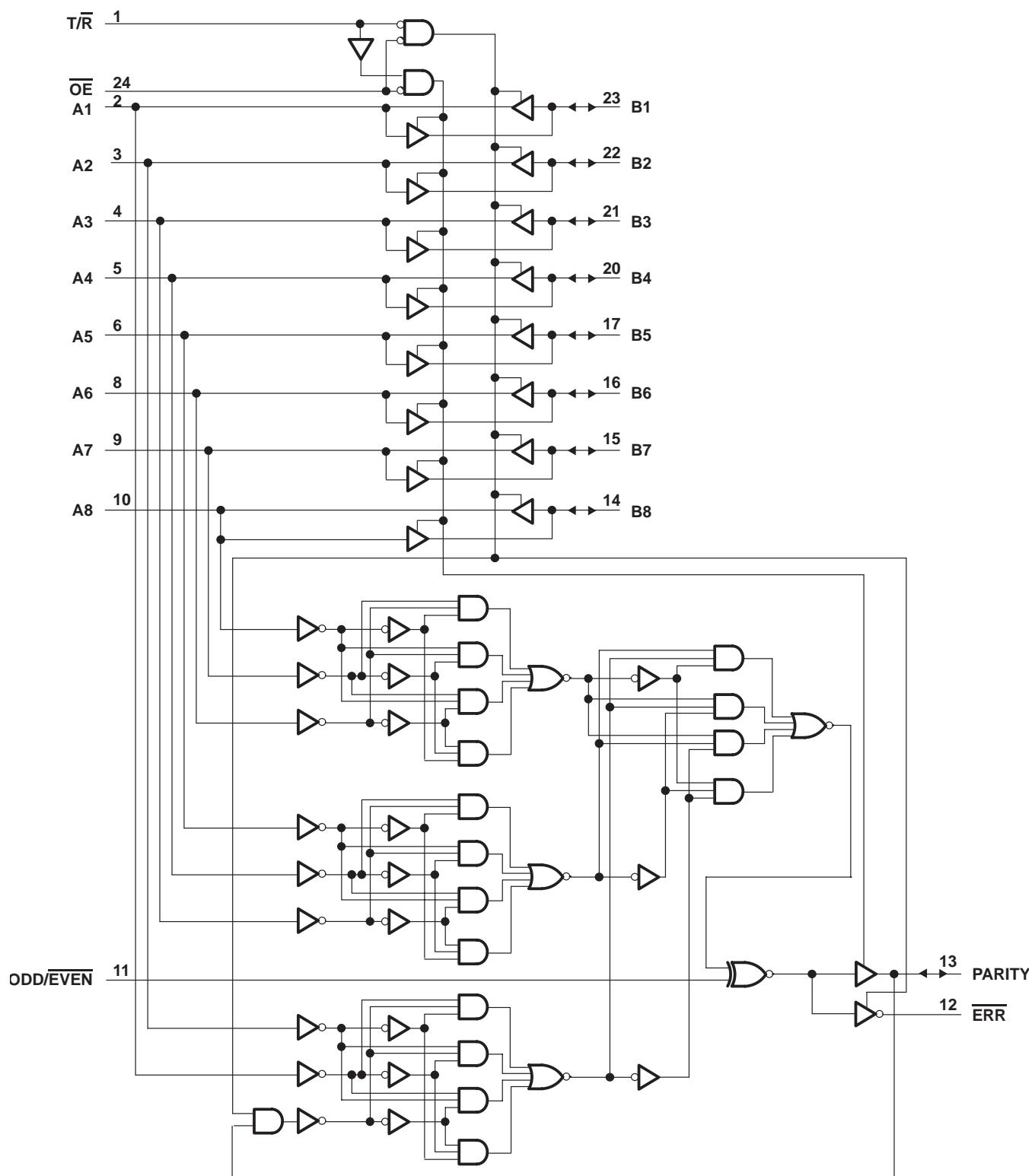
NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/R	ODD/EVEN		ERR	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

### **recommended operating conditions**

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V	
V <sub>IL</sub>	Low-level input voltage	0.8		V	
I <sub>OH</sub>	High-level output current	A1–A8		–3	
		B1–B8, PARITY, <u>ERR</u>		–12	
I <sub>OL</sub>	Low-level output current	A1–A8		24	
		B1–B8, PARITY, <u>ERR</u>		64	
T <sub>A</sub>	Operating free-air temperature	0		70	°C

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SDF5027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA				–1.2	V
V <sub>OH</sub>	Any output	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA		2.4	3.3		V
	B1–B8, PARITY, <u>ERR</u>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –15 mA		2	3.1		
	Any output	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = –1 mA to –3 mA			2.7		
V <sub>OL</sub>	A1–A8	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 24 mA		0.35	0.5	V
	B1–B8, PARITY, <u>ERR</u>		I <sub>OL</sub> = 64 mA		0.42	0.55	
I <sub>I</sub>	T/R	V <sub>CC</sub> = 0, V <sub>I</sub> = 7 V, <u>OE</u> = 4.5 V			0.1		mA
	<u>OE</u>	V <sub>CC</sub> = 0, V <sub>I</sub> = 7 V, T/R = 4.5 V			0.1		
	ODD/EVEN	V <sub>CC</sub> = 0, V <sub>I</sub> = 7 V			0.1		
	A1–A8	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			2		
	B1–B8				1		
I <sub>IH</sub> ‡	A, B, PARITY	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			70		μA
	T/R, <u>OE</u>				40		
	ODD/EVEN				20		
I <sub>IL</sub> ‡	A, B, PARITY	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V			–70		μA
	T/R, <u>OE</u>				–40		
	ODD/EVEN				–20		
I <sub>OS</sub> §	A1–A8	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0		–60	–150		mA
	B1–B8			–100	–225		
I <sub>OZH</sub>	<u>ERR</u>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			50	μA	
I <sub>OZL</sub>	<u>ERR</u>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V			–50	μA	
I <sub>CCH</sub>		V <sub>CC</sub> = 5.5 V		90	125	mA	
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5 V		106	150	mA	
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5 V		98	145	mA	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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**switching characteristics (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R1 = 500 \Omega$ , $R2 = 500 \Omega$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R1 = 500 \Omega$ , $R2 = 500 \Omega$ , $T_A = \text{MIN to MAX}^\dagger$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	2.5	4.2	7.5	2.5	8	ns
$t_{PHL}$			3	4	7.5	3	8	
$t_{PLH}$	A	PARITY	6	8.4	14	6	16	ns
$t_{PHL}$			6.8	8.5	15	6.8	16	
$t_{PLH}$	ODD/EVEN	PARITY, $\overline{ERR}$	4	6.4	11	4	12	ns
$t_{PHL}$			4.5	6.9	11.5	4.5	12.5	
$t_{PLH}$	B	$\overline{ERR}$	8	12.7	20.5	7.5	22.5	ns
$t_{PHL}$			8	13.4	20.5	7.5	22.5	
$t_{PLH}$	PARITY	$\overline{ERR}$	6	8.1	15.5	6	16.5	ns
$t_{PHL}$			7.5	8.8	15.5	7.5	17	
$t_{PZH}$	$\overline{OE}$	A, B, PARITY, or $\overline{ERR}^\ddagger$	3	5.3	8	3	9	ns
$t_{PZL}$			4	5.4	9.5	4	11	
$t_{PHZ}$	$\overline{OE}$	A, B, PARITY, or $\overline{ERR}^\ddagger$	2	4.2	7.5	2	8	ns
$t_{PLZ}$			2	3.7	6	2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These delay times reflect the 3-state recovery time only and not the signal through the buffers or parity check circuitry. To assure valid information at the  $\overline{ERR}$  output pin, time must be allowed for the signal to propagate through the drivers (B to A), and to the  $\overline{ERR}$  output. Valid data at the  $\overline{ERR}$  output is greater than or equal to (B to A) + (A to PARITY).

NOTE 2: Load circuits and waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74F657DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN74F657DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN74F657DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN74F657NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	<a href="#">Purchase Samples</a>
SN74F657NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	<a href="#">Purchase Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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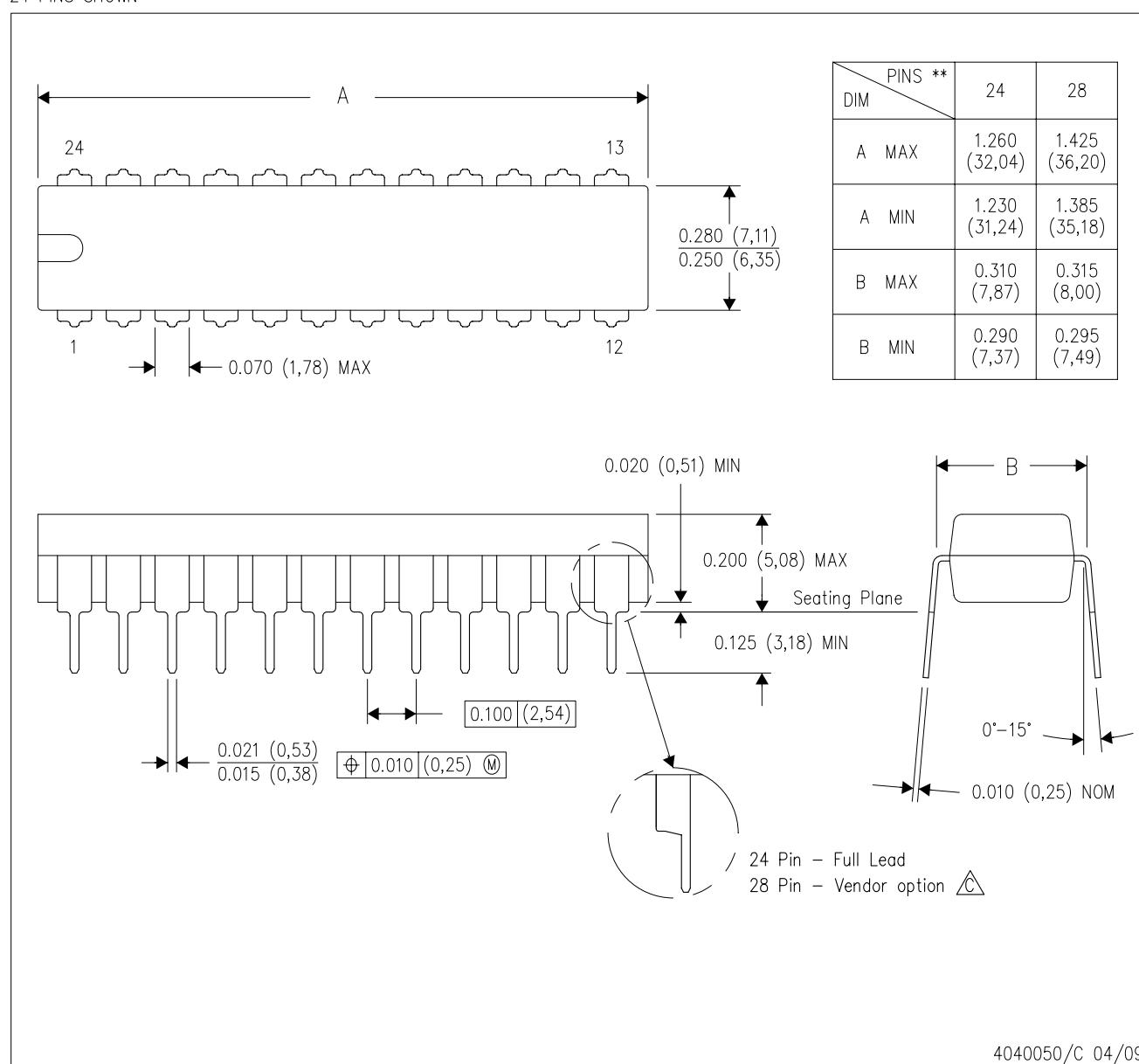
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## MECHANICAL DATA

NT (R-PDIP-T\*\*)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



4040050/C 04/09

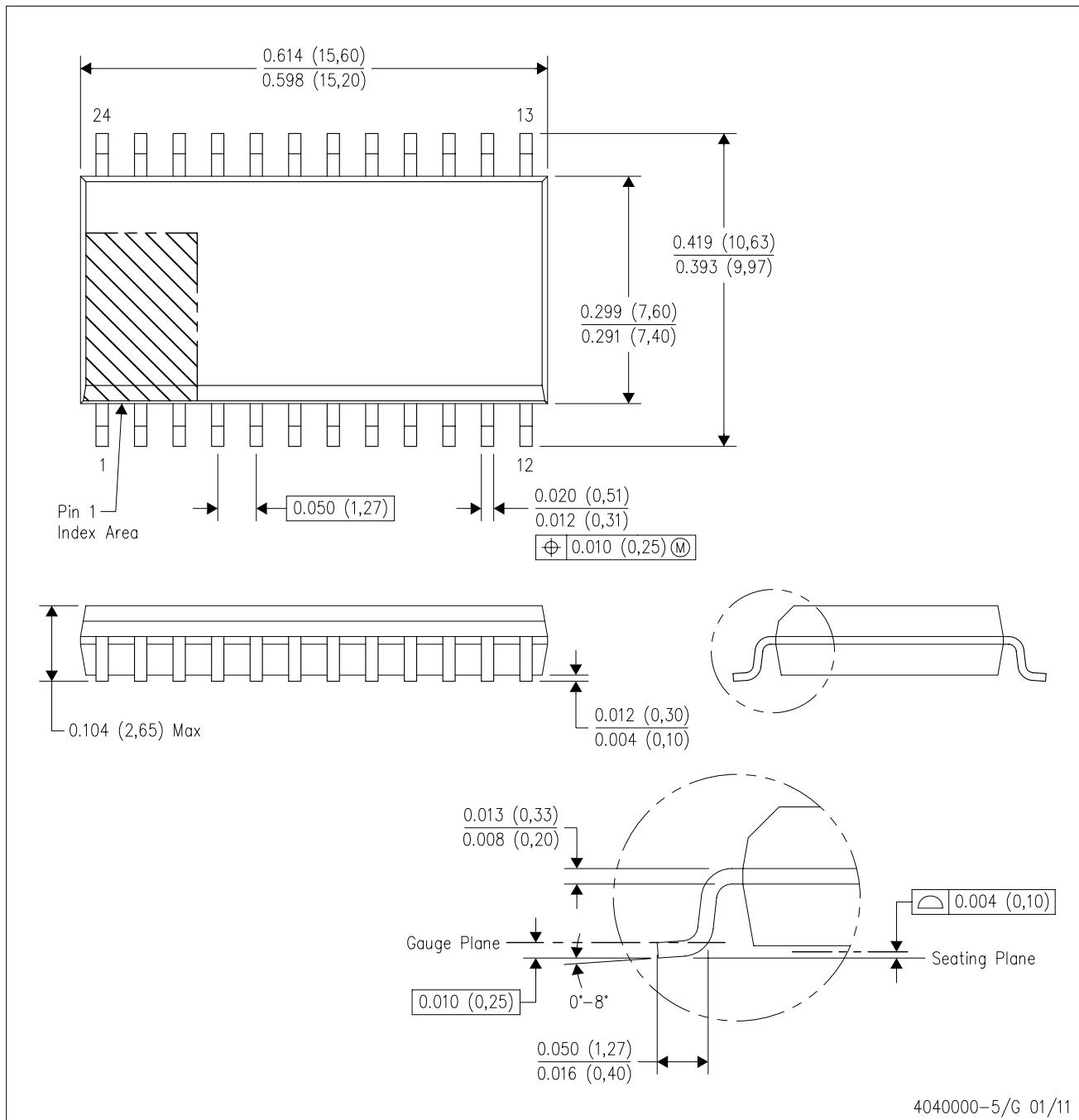
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

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