DATA SHEET

ARA2017: Programmable Gain Amplifier

Applications

- DOCSIS 3.0 data cable modems and E-MTAs
- CATV set-top boxes

Features

- High-linearity, high-output power integrated amplifier with programmable gain control
- Attenuation range: 0 to 58 dB, adjustable in 2 dB increments by means of a 3-wire serial control
- 33 dB gain (at minimum attenuation)
- Low distortion products at output power levels up to +64 dBmV
- Low noise figure and output noise
- Frequency range: 5 to 85 MHz
- 5 V operation
- Materials set consistent with ROHS directives
- QFN (28-pin 5 mm x 5 mm x 1 mm) surface-mount package

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Description

The ARA2017 is a highly linear, high output power, programmable gain amplifier optimized for DOCSIS 3.0 cable modem and E-MTA applications. Using a low-noise input amplification stage and an ultra-linear output driver amplifier, the device generates extremely low distortion products at the high output power levels required by DOCSIS 3.0 signals. The balanced circuit design of the device provides superior harmonic performance. An integrated digitally-controlled, multiple-stage precision step attenuator enables system solutions to meet DOCSIS power step accuracy requirements.

The ARA2017 supports output power levels of +64 dBmV while minimizing harmonics, distortion, and output noise levels. Its precision attenuator provides up to 58 dB of attenuation in 2 dB increments, which is set by programming the register via a 3-wire serial interface. The output stage current, a feature which allows the device to be operated in reduced power modes for extended backup battery life, is also programmed through the 3-wire serial interface. The ARA2017 is offered in a 28-pin 5 mm x 5 mm x 1 mm QFN package.

A functional block diagram of the ARA2017 is shown in Figure 1. The device package and pinout are shown in Figure 2. Signal pin assignments and functional pin descriptions are described in Table 1.

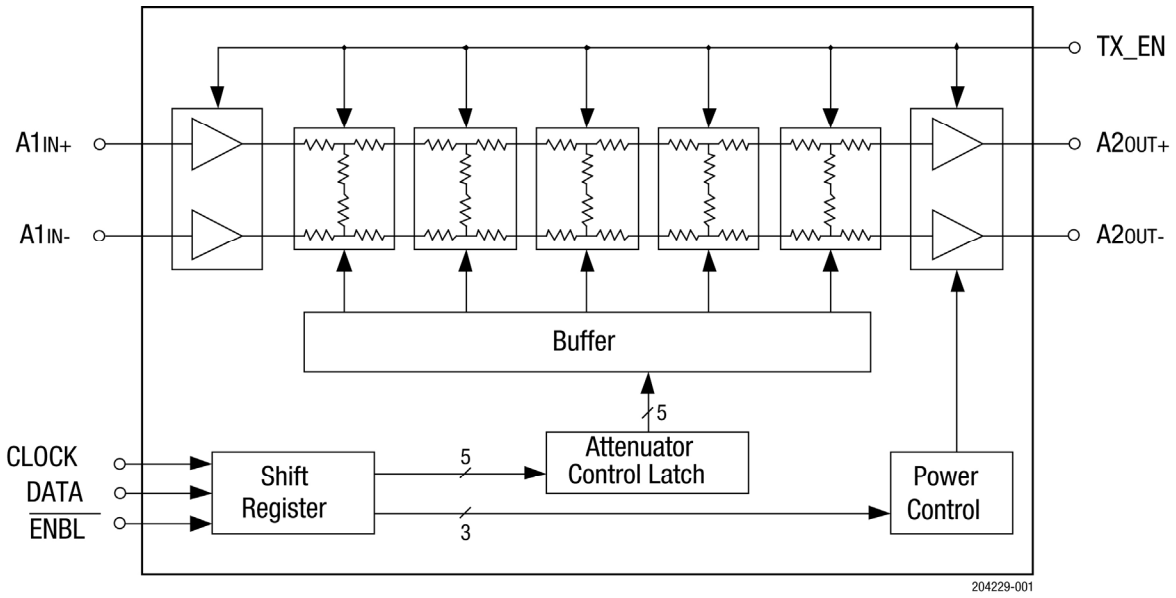


Figure 1. ARA2017 Functional Block Diagram

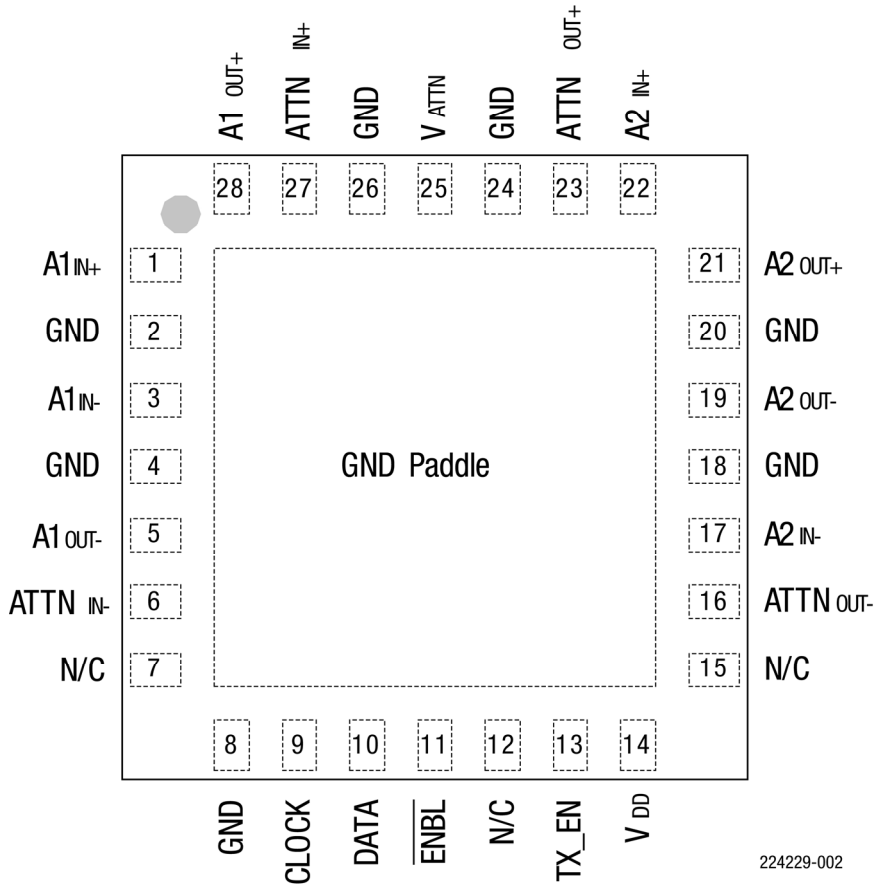


Figure 2. ARA2017 Pinout
(Top View)

Table 1. ARA2017 Signal Pin Descriptions

Pin	Name	Description	Pin	Name	Description
1	$A1_{IN+}$	Amplifier A1 (+) input	15	N/C	No connection
2	GND	Ground	16	$ATTN_{OUT-}$	Attenuator output (-)
3	$A1_{IN-}$	Amplifier A1 (-) input	17	$A2_{IN-}$	Amplifier A2 (-) input
4	GND	Ground	18	GND	Ground
5	$A1_{OUT-}$	Amplifier A1 (-) output and supply	19	$A2_{OUT-}$	Amplifier A2 (-) output and supply
6	$ATTN_{IN-}$	Attenuator input (-)	20	GND	Ground
7	N/C	No connection	21	$A2_{OUT+}$	Amplifier A2 (+) output and supply
8	GND	Ground	22	$A2_{IN+}$	Amplifier A2 (+) input
9	CLOCK	Clock	23	$ATTN_{OUT+}$	Attenuator output (+)
10	DATA	Data	24	GND	Ground
11	ENBL	Enable	25	V_{ATTN}	Attenuator supply
12	N/C	No connection (reserved for future use - leave floating)	26	GND	Ground
13	TX_EN	Transmit enable	27	$ATTN_{IN+}$	Attenuator input (+)
14	V_{DD}	Supply	28	$A1_{OUT+}$	Amplifier A1 (+) output and supply

Electrical and Mechanical Specifications

The absolute maximum ratings of the ARA2017 are provided in Table 2. Recommended operating conditions are specified in Table 3.

Electrical specifications are provided in Tables 4 and 5. Typical performance characteristics are shown in Figures 3 through 16.

Table 2. ARA2017 Absolute Maximum Ratings[1]

Parameter	Minimum	Maximum	Units
Supply V_{DD} (pins 5, 14, 19, 21, and 28) V_{ATTN} (pin 25)	0	+6	V
RF power at inputs (pins 1 and 3) ($Z_{PIN1\text{-}TO\text{-}PIN3}$ = 200 Ω differential)		+40	dBmV
Digital interface (pins 9, 10, 11, and 13)	-0.5	V_{DD} + 0.5	V
Storage temperature	-55	+150	°C

[1] Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***ESD HANDLING**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. ARA2017 Recommended Operating Conditions[1]

Parameter	Symbol	Min	Typ	Max	Units
Operating frequency	f	5	-	85	MHz
Supply: V_{DD} (pins 5, 14, 19, 21, 28)		+4.5	+5	+5.5	V
Digital interface (pins 9, 10, 11, 13)		0	-	V_{DD}	V
Case temperature	T_C	-40	+25	+95	°C

[1] Performance is guaranteed only under the conditions listed in this table.

Table 4. ARA2017 Digital Interface Specifications (V_{DD} = +5.0 V)

Parameter	Symbol	Min	Typ	Max	Units
Logic high input voltage	V_{IN_HIGH}	+2.0		VDD	V
Logic low input voltage	V_{IN_LOW}	0		+0.8	V

[1] Logic control levels apply to the 3-wire programming bus (pins 9, 10, 11) and the transmit enable control (pin 13).

Table 5. ARA2017 Electrical Specifications
(V_{DD} = +5.0 V, T_C = 25 °C, Tx Enabled, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Gain	G	0 dB attenuation setting	34	36	37	dB
Gain flatness		5 to 42 MHz 5 to 85 MHz		0.5 1.0		dB dB
Gain variation over temperature				-0.02		dB/°C
Gain range with attenuator			58			dB
Incremental attenuator step size			1.5	2	2.5	dB
2nd harmonic distortion level[1,2]		+64 dBmV into 75 Ω		-67	-55	dBc
3rd harmonic distortion level[1,2]		+64 dBmV into 75 Ω		-72	-55	dBc
Third order output intercept		2 tone, +61 dBmV/tone	+88	+93		dBmV
1 dB gain compression[1,2]				+73		dBmV
Noise figure	NF	Full gain @ 0 dB attenuator setting; Includes input balun loss		2.5	4.5	dB
Output noise power: Active / no signal / min. atten. set. Active / no signal / max. atten. set.		Any 160 kHz bandwidth from 5 to 85 MHz		 -38.5 -53.8		 dBmV dBmV
Isolation (85 MHz) in Tx disable mode				60		dB
Differential input impedance		Between pins 1 and 3 (Tx enabled)		200		Ω
Differential output impedance		Between pins 19 and 21		75		Ω
Output impedance		With transformer		75		Ω
Output return loss (75 ohm characteristic impedance)		Tx enabled Tx disabled		-15 -12		dB dB
Output voltage transient Tx enable / Tx disable		0 dB attenuator setting 24 dB attenuator setting		50 7		mVp-p mVp-p
Total supply current[1,2] (pins 5, 14, 19, 21, 25, 28)		Tx enabled (TX_EN high) Tx disabled (TX_EN low)		340 10.5	400	mA mA
Total power consumption		Tx enabled (TX_EN high) Tx disabled (TX_EN low)		1.7 52.5		W mW
Thermal resistance	θ_{JC}			30		°C/W

1 As measured in test fixture.
2 Measured using the maximum current setting. See the *Application Information* section.

Typical Performance Characteristics

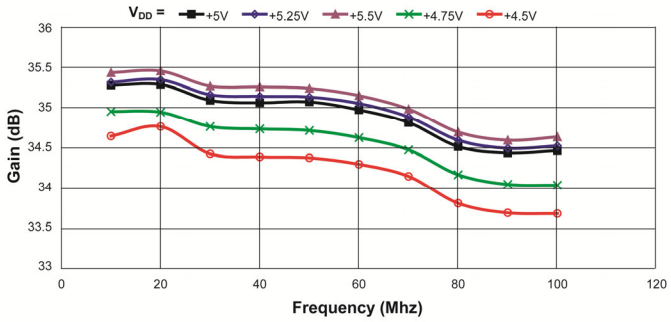


Figure 3. Gain vs Frequency over Voltage (Tc = 25 °C)

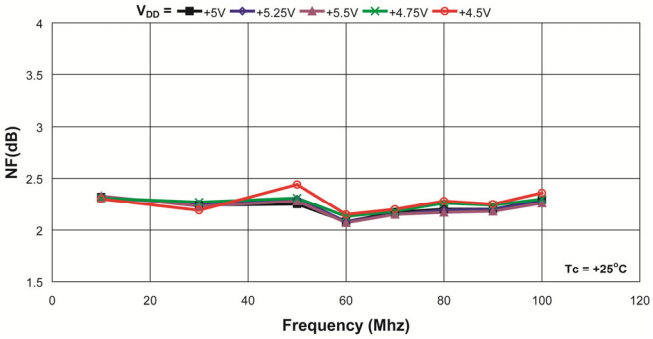


Figure 4. Noise Figure vs Frequency over Voltage (Tc = 25 °C)

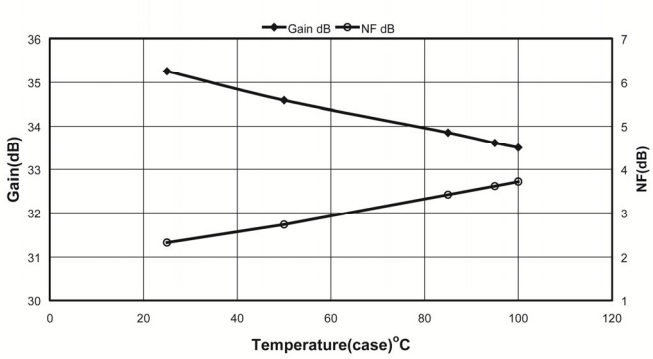


Figure 5. Gain and Noise Figure vs Temperature (VDD = +5 VDC, f1 = 10 MHz)

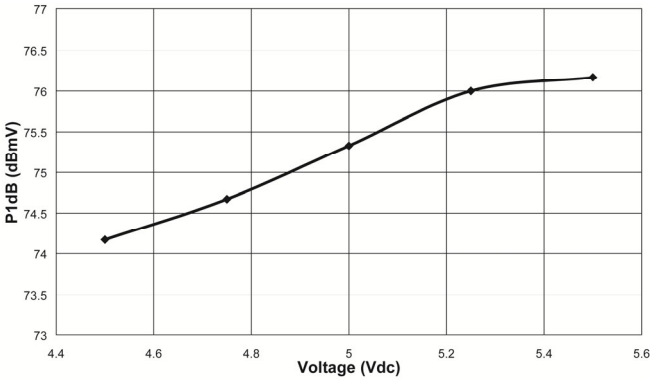


Figure 6. 1 dB Gain Compression (P1dB) vs Voltage (Tc = 25 °C, f1 = 10 MHz)

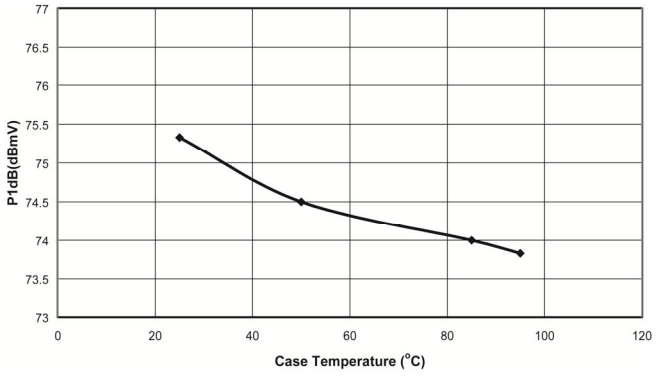


Figure 7. 1 dB Gain Compression (P1dB) vs Temperature (VDD = +5 VDC, f1 = 10 MHz)

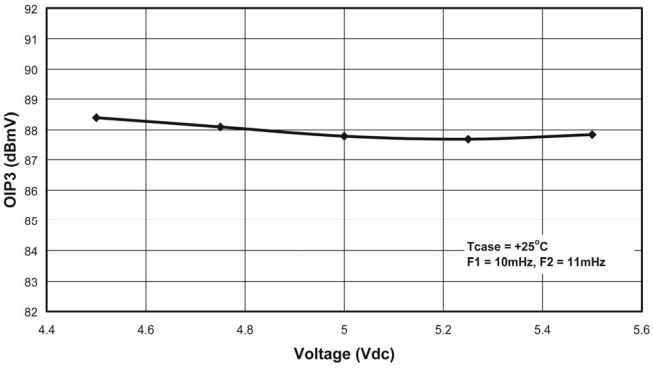


Figure 8. Output Third Order Intercept Point (OIP3) vs Voltage (Tc = 25 °C, f1 = 10 MHz, f2 = 11 MHz)

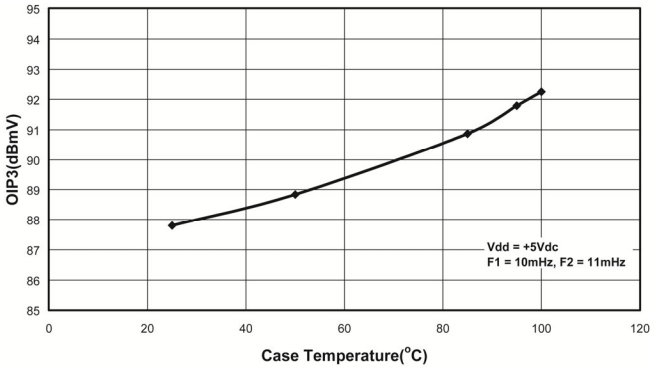


Figure 9. Output Third Order Intercept Point (OIP3) vs Temperature
(V_{DD} = +5 V, f1 = 10 MHz, f2 = 11 MHz)

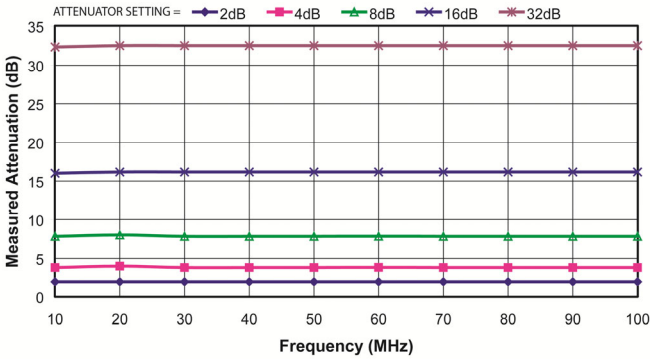


Figure 10. Attenuator Accuracy over Frequency
(T_C = 25 °C, V_{DD} = +5 V)

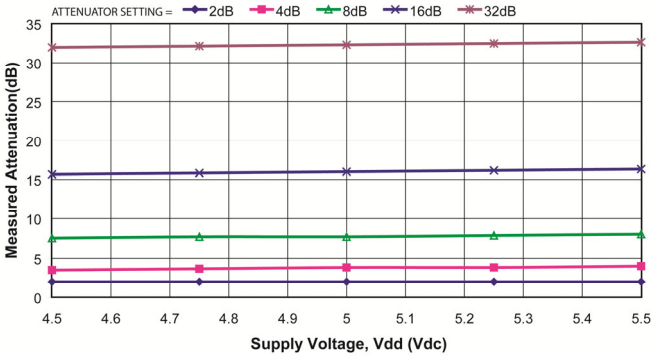


Figure 11. Attenuator Accuracy over Voltage
(T_C = +25 °C, f1 = 10 MHz)

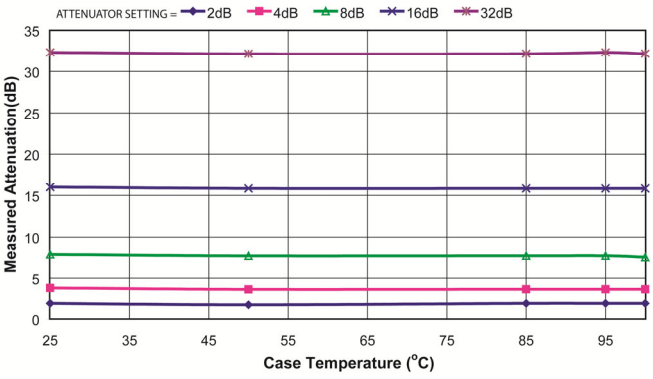


Figure 12. Attenuator Accuracy over Temperature
(V_{DD} = +5 V, f1 = 10 MHz)

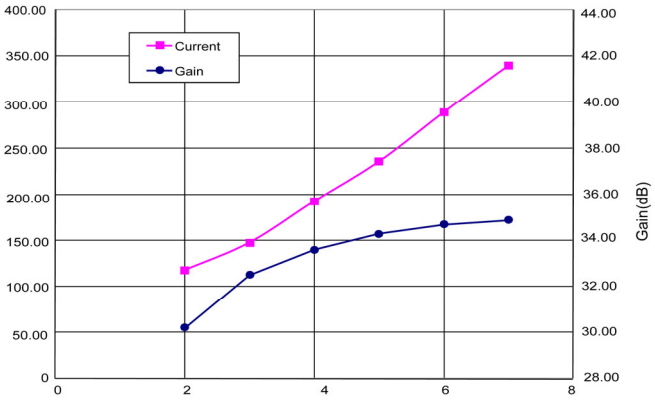


Figure 13. Gain and I_{DD} vs Power Control Setting

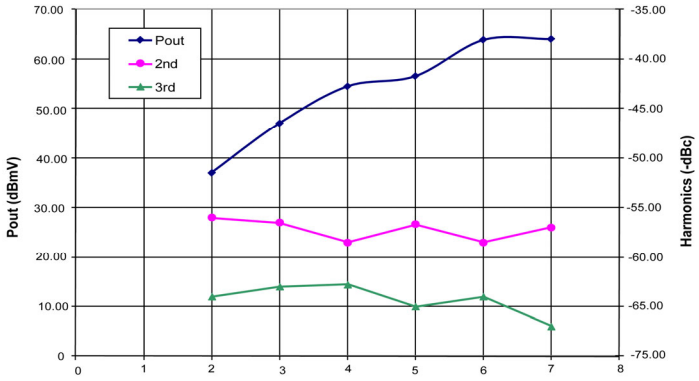


Figure 14. P_{OUT} and Harmonics vs Power Control Setting

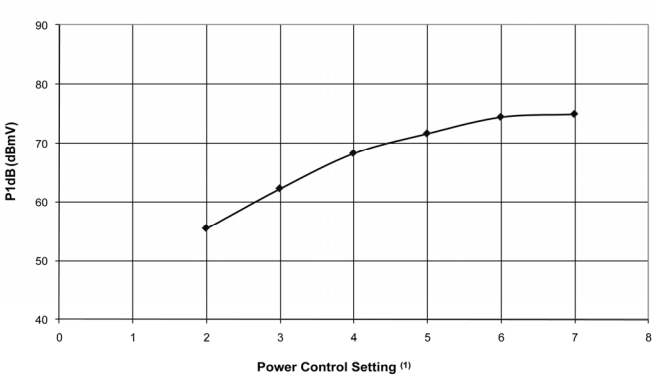
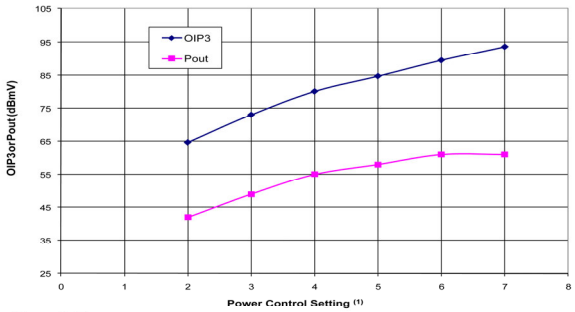


Figure 15. P1dB vs Power Control Setting



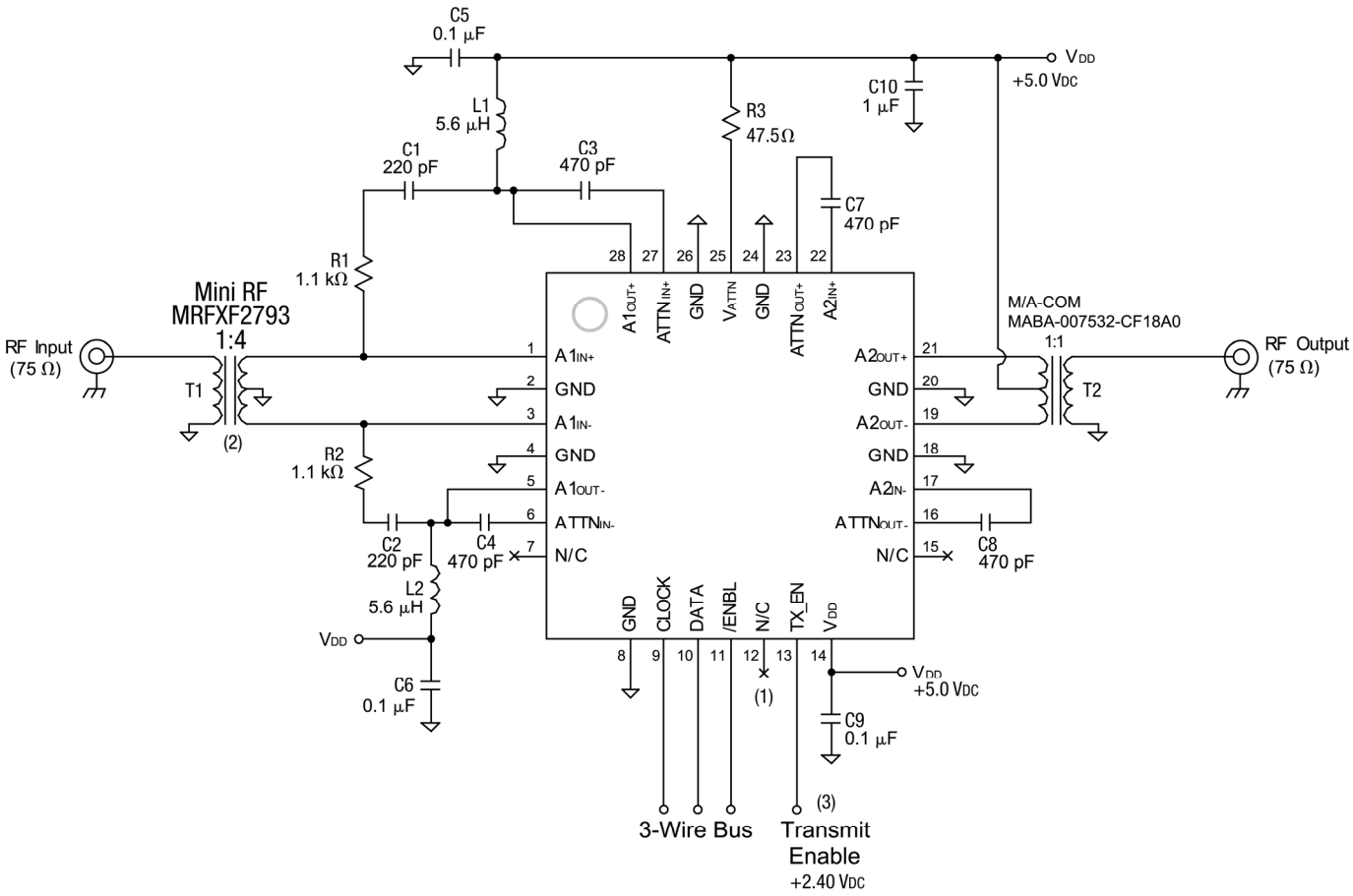
Notes (Figures 13-16):
(1) Power control setting refers to the programming register bits 7, 8, and 9 (see Table 6). The power control can be set using Tuner Control Software, version 1.2.3, in the "Advanced settings" window. The software is used in conjunction with the ARA2017 evaluation board.

Figure 16. OIP3 and POUT vs Power Control Setting

Evaluation Board Description

The ARA2017 Evaluation Board is used to test the performance of the ARA2017 device.

An Evaluation Board schematic is provided in Figure 17. Table 6 lists the Evaluation Board Bill of Materials (BOM).



Notes:
(1) Pin 12 is reserved for future use. Do not connect (leave floating).
(2) Input balun is used for evaluation test purposes only in 75 Ω system. Applications using differential drivers do not require a 4:1 balun on the input.
(3) TX_EN must be cycled LOGIC LOW-to-HIGH (GND-to-2.4V) to implement the settings loaded into the programming registers via the 3-wire bus.

Figure 17. ARA2017 Evaluation Board Schematic

Table 6. ARA2017 Evaluation Board Bill of Materials (BOM)

Component	Description	Value	Size	Manufacturer	Part Number
C1	Capacitor	220 pF	0402	muRata	GRM1555C1H221GA01
C2	Capacitor	220 pF	0402	muRata	GRM1555C1H221GA01
C3	Capacitor	470 pF	0402	muRata	GRM1555C1H471GA01
C4	Capacitor	470 pF	0402	muRata	GRM1555C1H471GA01
C5	Capacitor	0.1 uF	0603	muRata	GRM188R71C104MA01D
C6	Capacitor	0.1 uF	0603	muRata	GRM188R71C104MA01D
C7	Capacitor	470 pF	0402	muRata	GRM1555C1H471GA01
C8	Capacitor	470 pF	0402	muRata	GRM1555C1H471GA01
C9	Capacitor	0.1 uF	0603	muRata	GRM188R71C104MA01D
C10	Capacitor	1 uF	0603	muRata	GCM188R71E105KA64D
L1	Inductor	5.6 uH	1210	TDK	NLV32T-5R6J-EF
L2	Inductor	5.6 uH	1210	TDK	NLV32T-5R6J-EF
R1	Resistor	1.1 kΩ	0402	Panasonic	ERJ-2GEJ112X
R2	Resistor	1.1 kΩ	0402	Panasonic	ERJ-2GEJ112X
R3	Resistor	47.5	0603	Panasonic	ERJ-3EKF47R5V
T1	Balun	1:4	S20	Minirf	MRFXF2793
T2	Balun	1:1		Macom	MABA-007532-CF18A0
U1	Amplifier	28L	5X5mm	Skyworks	ARA2017

Logic Programming

The programming word is set through a 10-bit shift register via the data, clock and enable lines. The data is entered in order with the most significant bit (MSB) first and the least significant bit (LSB) last.

Programming Instructions

The enable line must be low for the duration of the data entry, then set high to latch the shift register. The rising edge of the clock pulse shifts each data value into the register.

Table 7. Programming Register

Data bit	9	8	7	6	5	4	3	2	1	0
Function	Current			Gain					0	1

1 Refer to Application Information section for Current and Gain bit settings.

2 Data bit 0 should always be set to 1.

3 Data bit 1 is reserved for future use, and should be set to 0.)

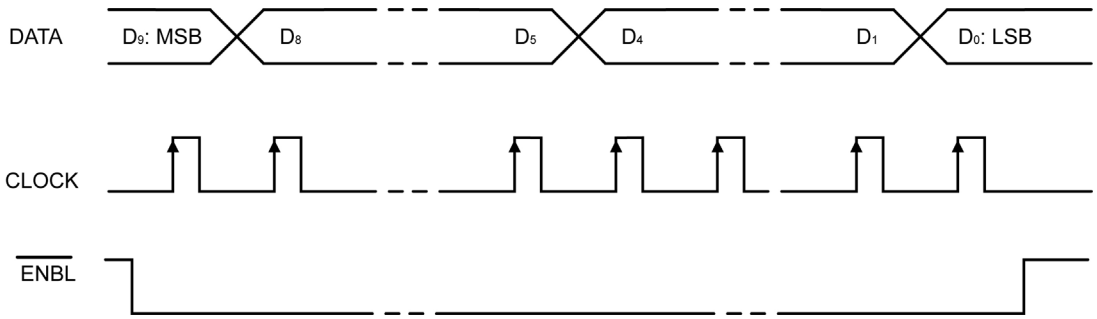


Figure 18. Serial Data Input Timing

Application Information

Transmit Enable / Disable

The ARA2017 can be switched on (Tx enable) and off (Tx disable) via an asynchronous input TX_EN (pin 13). A logic high will turn the amplifier on. The gain and current settings are retained during Tx disable and do not need to be reloaded.

Gain/Attenuator Setting

The gain of the ARA2017 can be controlled via the 3-wire bus. Data bits D2 through D6 set the gain/ attenuator level, with 00000 being the min gain setting, and 11111 being the max gain setting. A new gain/ attenuator setting can be loaded while the PGA is on (Tx enable), but will not take effect until TX_EN has been cycled off /on.

Output Stage Current Setting

The ARA2017 consists of two gain stages. The input stage operates at a constant fixed current when Tx is enabled. The current in the output stage can be controlled via the 3-wire bus. Data bits D7 to D9 set the current. A setting of 111 will set the output stage to maximum current for maximum linearity. The current can be lowered for improved efficiency at lower output power levels, or lower linearity requirements. 000 will turn both stages off, the same as Tx disable. A new current setting can be loaded while the PGA is on (Tx Enable), but will not take effect until TX_EN has been cycled off /on.

Output Transformer

Matching the balanced output of the ARA2017 to a single-ended 75 Ω load is accomplished using a 1:1 turns ratio transformer. In addition to the balanced to single-ended conversion, this transformer provides the bias to the output amplifier stage via the center tap.

The transformer also cancels even mode distortion products and common mode signals, such as the voltage transients that occur while enabling and disabling the amplifiers. As a result, care must be taken when selecting the transformer to be used at the output. It must be capable of handling the RF and DC power requirements without saturating the core, and it must have adequate isolation and good phase and amplitude balance. It also must operate over the desired frequency and temperature range for the intended application.

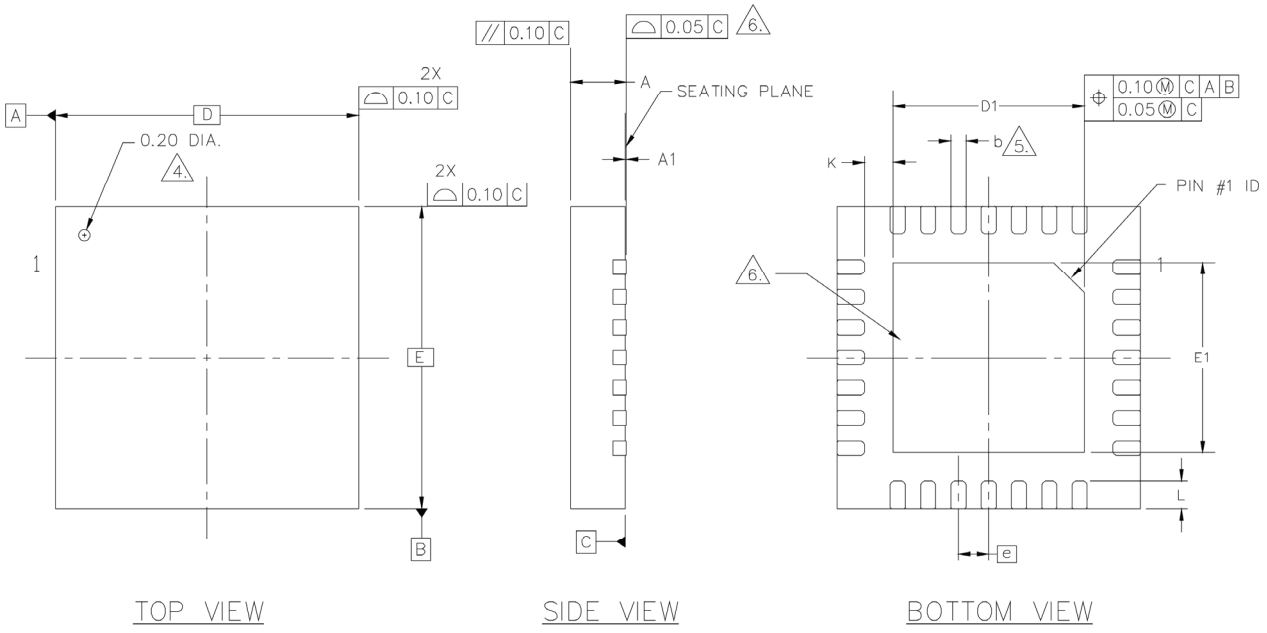
Package Dimensions

Package dimensions for the ARA2017 are shown in Figure 19. The typical part marking is shown in Figure 20. The PCB layout footprint is shown in Figure 21.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



SYMBOL	DIMENSIONS–MM			NOTE
	MIN.	NOM.	MAX.	
A	0.85	–	1.00	
A1	0.00	–	0.05	
b	0.18	0.25	0.30	
D		5.00 BSC		
D1	3.00	3.15	3.30	
F		5.00 BSC		
E1	3.00	3.15	3.30	
e		0.50 BSC		
K		0.475 MIN.		
L	0.425	0.45	0.475	

SYMBOL	DIMENSIONS–INCHES			NOTE
	MIN.	NOM.	MAX.	
A	0.033	–	0.039	
A1	0.000	–	0.002	
b	0.007	0.010	0.012	
D		0.197 BSC		
D1	0.118	0.124	0.130	
F		0.197 BSC		
E1	0.118	0.124	0.130	
e		0.020 BSC		
K		0.019 MIN.		
L	0.017	0.018	0.019	

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER MARKED.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
6. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. REFERENCE JEDEC OUTLINE MO–220.

Figure 19. ARA2017 Package Dimensions

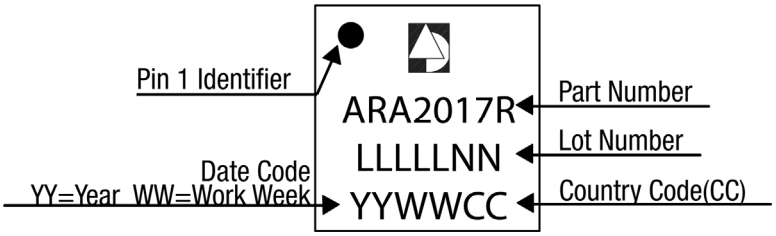


Figure 20. ARA2017 Typical Part Marking

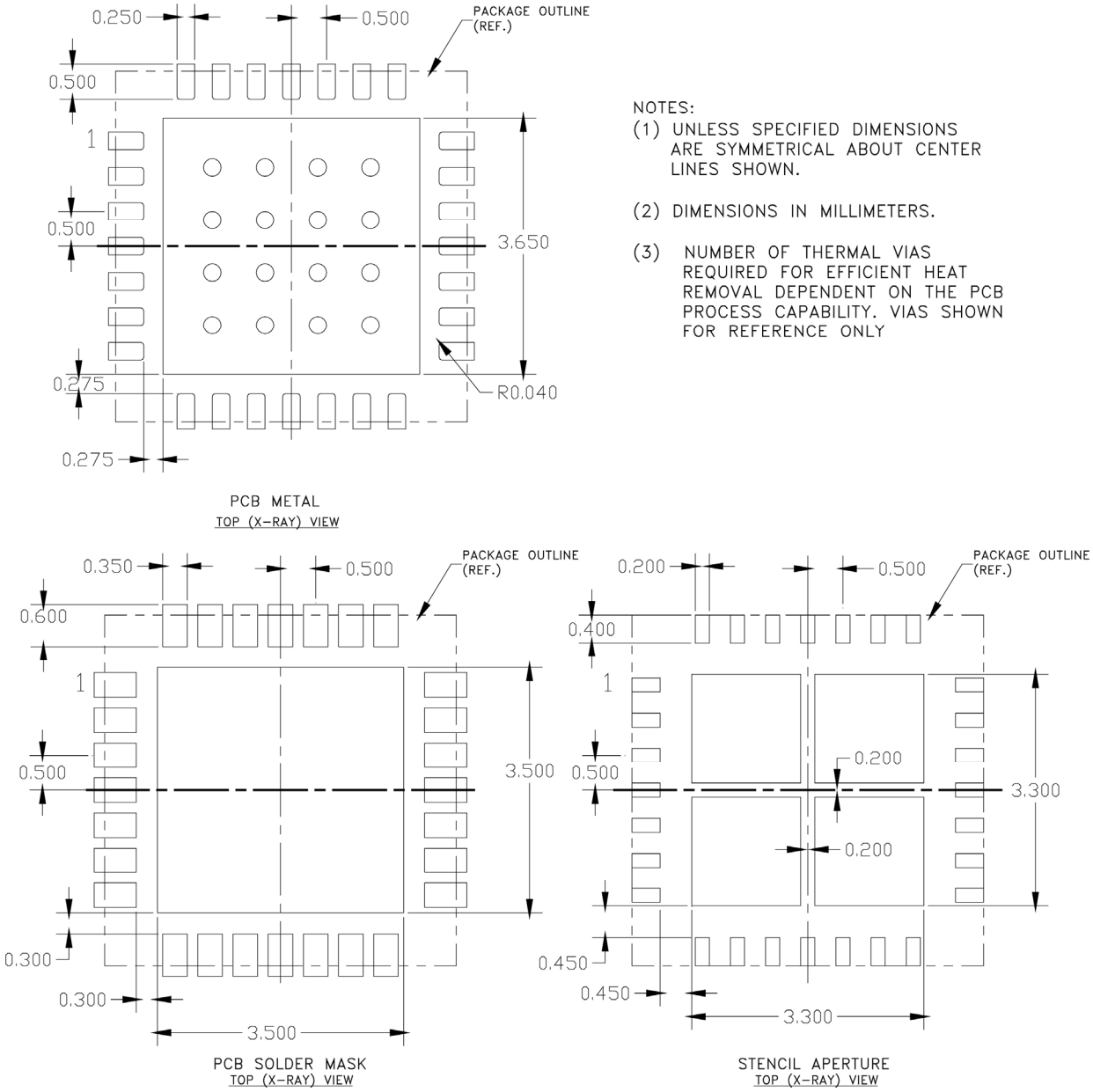


Figure 21. ARA2017 PCB Board Layout

Ordering Information

Part Number	Product Description	Component Packaging
ARA2017RS29P8	28 Pin QFN Package 5 mm x 5 mm x 1 mm	2500-piece tape and reel