PLA133-97

Low-Power DC to 160 MHz 1:9 Fanout Buffer IC for Automotive

Features

- Automotive AEC-Q100 Qualified
- 1:9 LVCMOS Output Fanout Buffer from DC to 160 MHz
- Low Additive Phase Jitter of 60 fs RMS
- 8 mA Output Drive Strength
- Low Power Consumption for Portable Applications
- Automotive Applications Grade 1 Compliant
- Low Input-Output Delay
- Output-Output Skew <250 ps
- 2.5V to 3.3V, ±10% Operation
- 1.8V +10%/–5% Operation up to 67 MHz
- Wide Temperature Range: –40°C to +125°C
- Available in 16-Pin Wettable Flanks VQFN Package

Applications

- Automotive Applications
  - ADAS Vision System
  - Infotainment and Dashboard

General Description

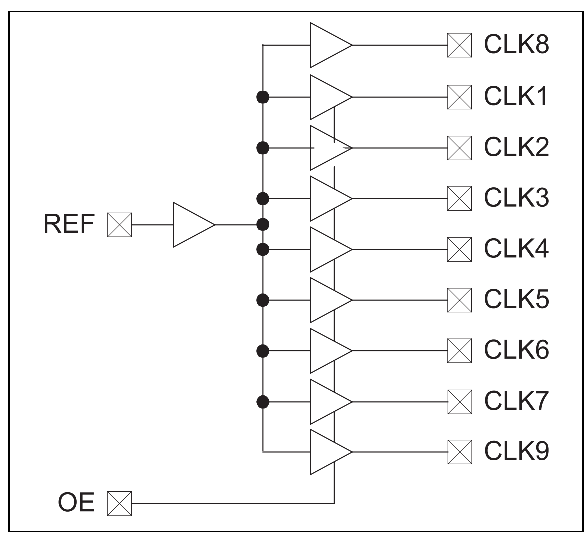
The PLA133-97 is an advanced fanout buffer designed for automotive applications and other high performance, low-power, small form factor applications. The PLA133-97 accepts a reference clock input from DC to 160 MHz and provides nine outputs of the same frequency with ultra-low additive jitter. The device is AEC-Q100 qualified.

The PLA133-97 is offered in a small 3 mm x 3 mm wettable flanks VQFN-16L package.

The PLA133-97 outputs can be disabled to a high impedance (tri-state) by pulling low the OE pin. When the OE pin is high, the outputs are enabled and follow the REF input signal. When the OE pin is left open, a pull-up resistor on the chip will default the OE pin to logic 1 so the outputs are enabled.

CLK8 is a free running output that remains enabled when the OE pin is pulled low.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage to Ground Potential .... –0.5V to +4.6V
DC Input Voltage .... V_{SS} –0.5V to +4.6V
Static Discharge Voltage
(Per MIL-STD-883, Method 3015)........ >2000V

Operating Ratings †

Supply Voltage, V_{DD}........ 1.71V to 3.63V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Low Voltage	V_{IL}	—	—	$0.3xV_{DD}$	V	Note 1
Input High Voltage	V_{IH}	$0.7xV_{DD}$	—	—	V	Note 1
Input Low Current	I_{IL}	—	—	50	µA	V_{IN} = 0V
Input High Current	I_{IH}	—	—	100	µA	$V_{IN} = V_{DD}$
Supply Current	I_{DD}	—	—	32	mA	66.67 MHz with unloaded outputs
Output Low Voltage	V_{OL}	—	—	0.5	V	I_O = 8 mA, V_{DD} = 3.3V
		—	—	0.5		I_O = 6 mA, V_{DD} = 2.5V
		—	—	0.5		I_O = 4 mA, V_{DD} = 1.8V
Output High Voltage	V_{OH}	V_{DD} - 0.5	—	—	V	I_O = –8 mA, V_{DD} = 3.3V
		V_{DD} - 0.5	—	—		I_O = –6 mA, V_{DD} = 2.5V
		V_{DD} - 0.5	—	—		I_O = –4 mA, V_{DD} = 1.8V
OE Pin Pull-Up Resistance	R_{PU}	—	120	—	kΩ	—
Load Capacitance	C_L	—	—	30	pF	Load Capacitance, below 100 MHz, V_{DD} > 2.25V
		—	—	10		Load Capacitance between 100 MHz and 134 MHz, V_{DD} > 2.25V
		—	—	5		Load Capacitance, above 134 MHz, V_{DD} > 2.25V
		—	—	15		Load Capacitance, below 67 MHz, 1.71V < V_{DD} < 2.25V
Input Capacitance	C_{IN}	—	—	7	pF	—
Power-Up Time	t_{PU}	0.05	—	50	ms	Power-up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)

Note 1: REF input has a threshold voltage of V_{DD}/2.

SWITCHING CHARACTERISTICS Note 2

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Frequency	f	DC	—	160	MHz	V_{DD} = 3.3V, 2.5V
		DC	—	67	MHz	V_{DD} = 1.8V
Duty Cycle = $t_2 \div t_1$	—	40	50	60	%	Measured at V_{DD}/2, Input is 50%
Rise Time	t_3	—	—	1.5	ns	Measured between 0.8V and 2.0V
Fall Time	t_4	—	—	1.5	ns	Measured between 0.8V and 2.0V
Output to Output Skew Note 1	t_5	—	—	250	ps	All outputs equally loaded
Propagation Delay, REF Rising Edge to CLKX Rising Edge Note 1	t_6	1	5	9.2	ns	Measured at V_{DD}/2

Note 1: Parameter is guaranteed by design and characterization.

2: All parameters are specified with loaded outputs.

NOISE CHARACTERISTICS

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Additive Phase Jitter	—	—	60	—	fs	V_{DD} = 3.3V, Frequency = 100 MHz Integration range 12 kHz - 20 MHz

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Operating Temperature (T)	T_A	–40	—	+125	°C	—
Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
16-Lead VQFN	$R_{\theta JA}$	—	—	82.3	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

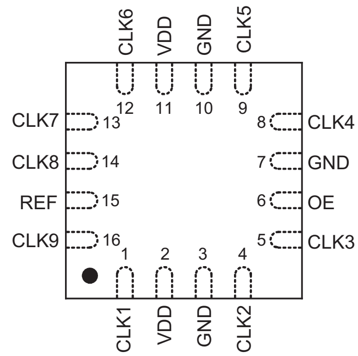


FIGURE 2-1: *Pin Configuration, 16-Lead VQFN Package.*

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	P8in Name	Type	Description
15	REF	I	Input reference frequency.
1	CLK1	O	Buffered clock output.
4	CLK2	O	Buffered clock output.
5	CLK3	O	Buffered clock output.
8	CLK4	O	Buffered clock output.
9	CLK5	O	Buffered clock output.
12	CLK6	O	Buffered clock output.
13	CLK7	O	Buffered clock output.
14	CLK8	O	Buffered clock output.
16	CLK9	O	Buffered clock output.
2, 11	VDD	P	VDD connection.
3, 7, 10	GND	P	GND connection.
6	OE	I	Output enable control input with 120 kΩ pull-up.
ePAD	—	—	Center Pad for Thermal Relief. Connect to GND.

3.0 NOMINAL PERFORMANCE CHARACTERISTICS

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

U

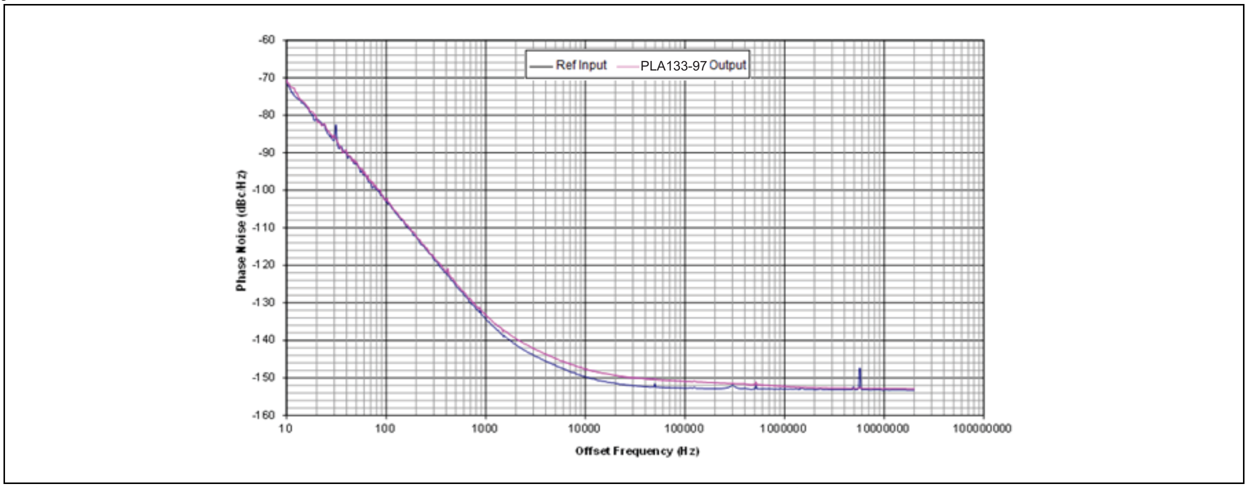


FIGURE 3-1: *PLA133-97 Additive Phase Jitter: V_{DD} = 3.3V, CLK-100 MHz, Integration Range 12 kHz - 20 MHz.*

When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. The noise added by the buffer to the input signal is quantified by the additive phase jitter defined by the following formula:

EQUATION 3-1:

$$AdditivePhaseJitter = \sqrt{(OutputPhaseJitter)^2 - (InputPhaseJitter)^2}$$

4.0 SWITCHING WAVEFORMS

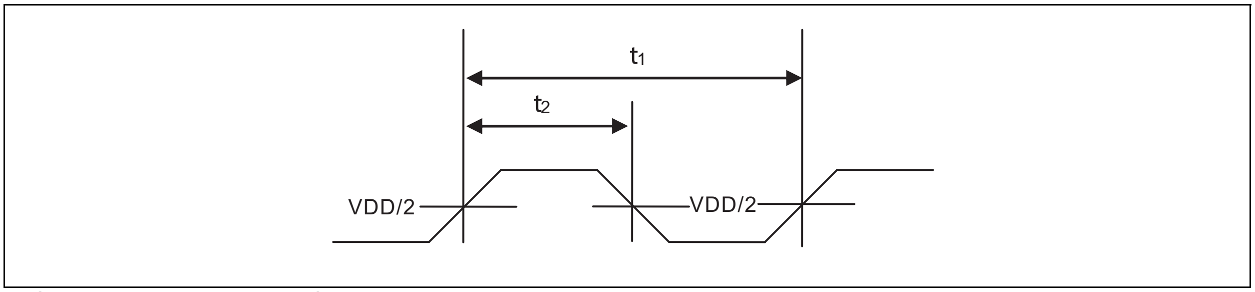


FIGURE 4-1: *Duty Cycle Timing.*

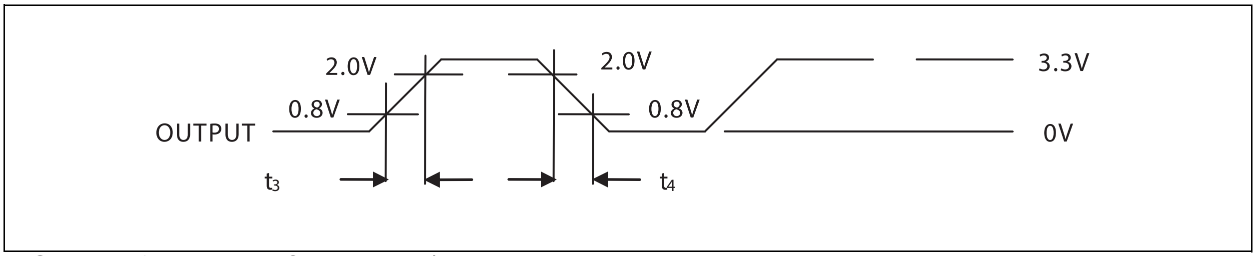


FIGURE 4-2: *All Outputs rise/Fall Time.*

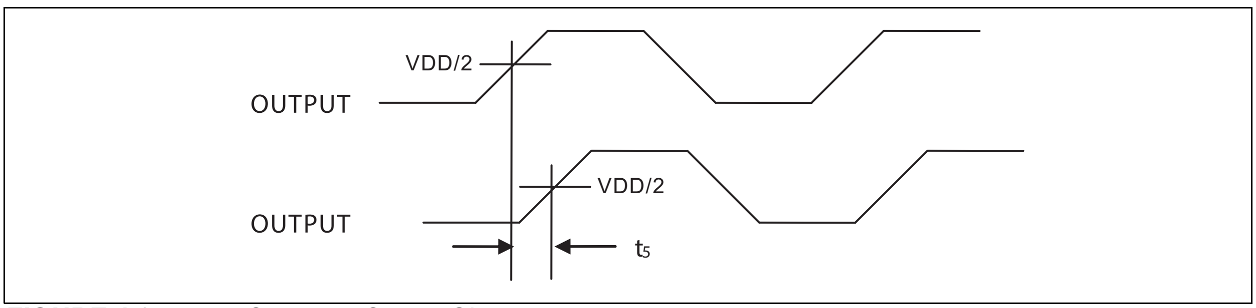


FIGURE 4-3: *Output to Output Skew.*

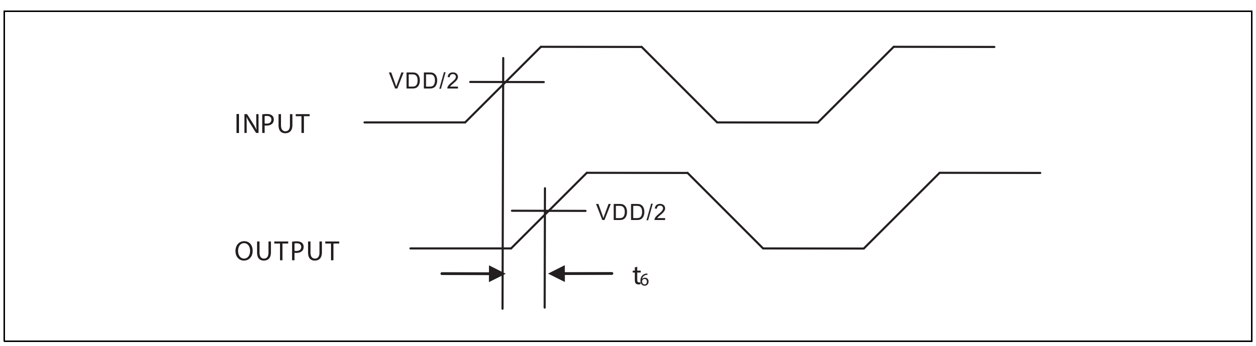


FIGURE 4-4: *Input-Output Propagation Delay.*

5.0 TEST CIRCUIT

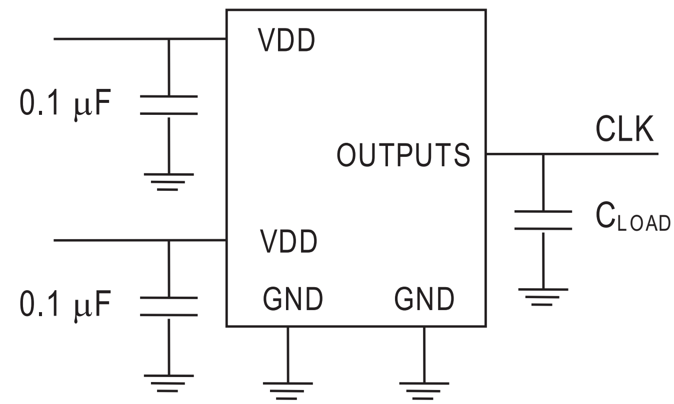


FIGURE 5-1: *Test Circuit.*

6.0 LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

6.1 Signal Integrity and Termination Considerations

- Keep traces short
- Trace = Inductor. With a capacitive load this equals ringing
- Long trace = Transmission Line. Without proper termination this will cause reflections ringing and waveforms and degradations.
- Use stripline or microstrip with defined impedance for long traces (> 1 inch)
- Match traces on one side of the board to avoid reflections bouncing back and forth.

6.2 Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1 µF for designs using frequencies <50 MHz and 0.01 µF for designs using frequencies >50 MHz

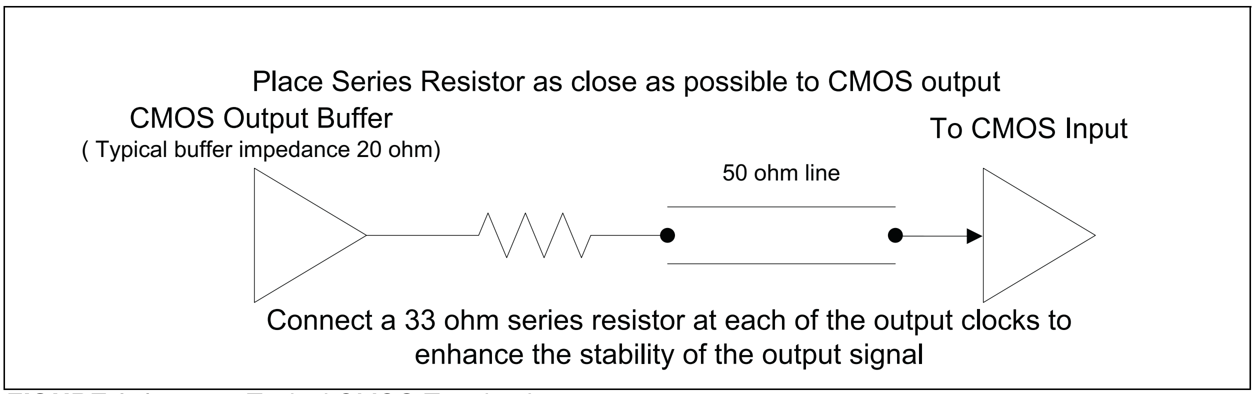
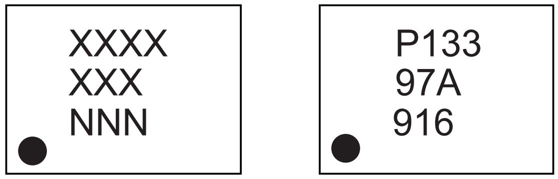


FIGURE 6-1: *Typical CMOS Termination.*

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

16-Lead VQFN* Example



Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

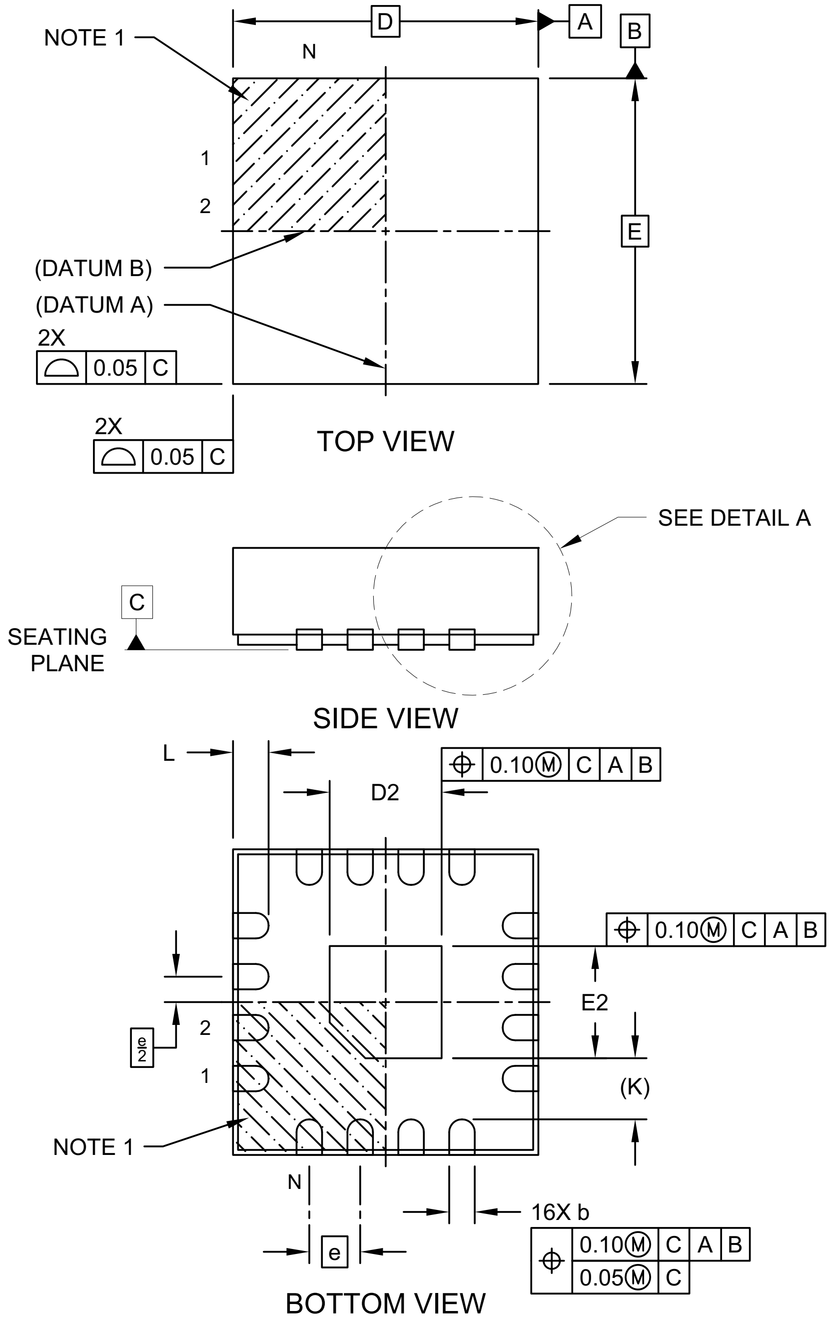
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

16-Lead Plastic Quad Flat, No Lead Package (8N) - 3x3x1.0 mm Body [VQFN] Wettable Flanks (Stepped) Package Outline and Recommended Land Pattern

16-Lead Plastic Quad Flat, No Lead Package (8N) - 3x3x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.35 mm Terminal Length

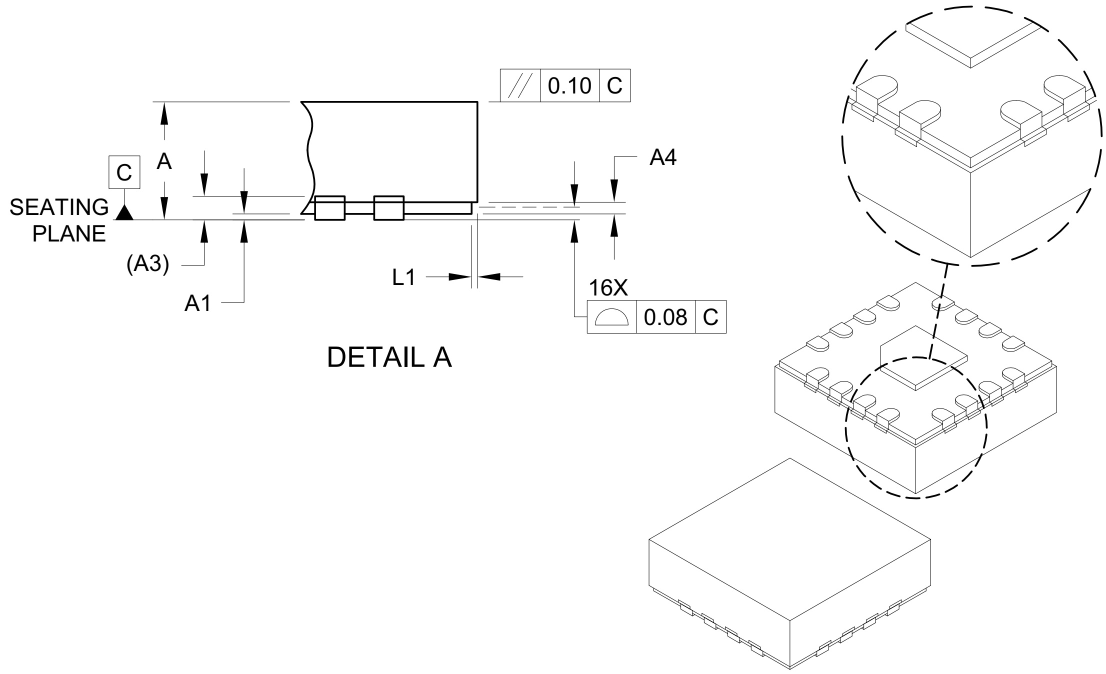
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-404C Sheet 1 of 2

16-Lead Plastic Quad Flat, No Lead Package (8N) - 3x3x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.35 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Step Height	A4	0.05	0.12	0.19
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.00	1.10	1.20
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.00	1.10	1.20
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Step Length	L1	0.035	0.060	0.085
Terminal-to-Exposed Pad	K		0.60 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

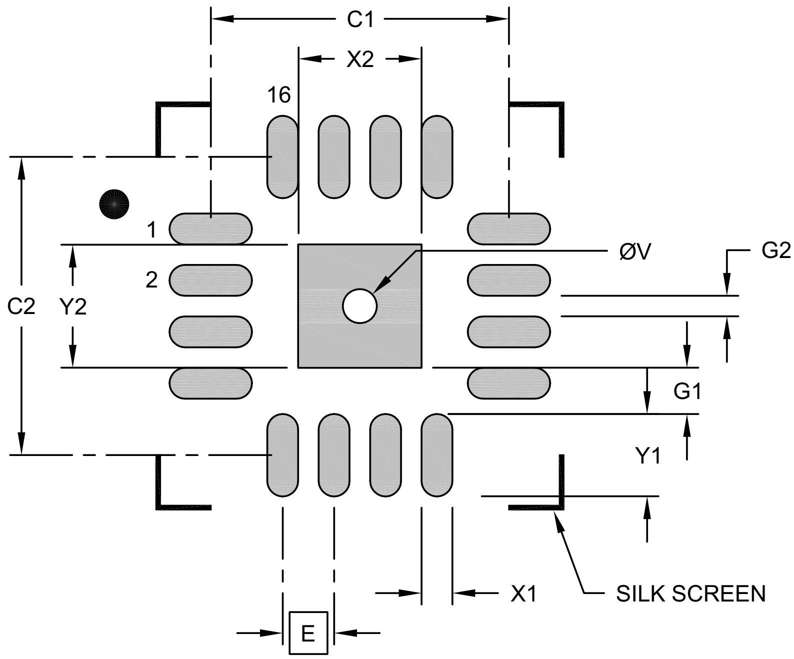
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-404C Sheet 2 of 2

16-Lead Plastic Quad Flat, No Lead Package (8N) - 3x3x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.35 mm Terminal Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.20
Optional Center Pad Length	Y2			1.20
Contact Pad Spacing	C1		2.90	
Contact Pad Spacing	C2		2.90	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.80
Contact Pad to Center Pad (X16)	G1	0.30		
Contact Pad to Contact Pad (X12)	G2	0.20		
Thermal Via Diameter	V		0.33	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2404B

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2020)

- Initial release of PLA133-97 as Microchip data sheet DS20006359A.

Revision B (July 2020)

- Added the thermal spec. for the 16-lead VQFN package.
- Updated with the VQFN 16-lead Wettable Flanks package diagram.

Revision C (October 2020)

- Changed the operating frequency to 160 MHz which was wrongly input as 150 MHz.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	XXX
Device	Package	Temperature Range	Media Type	Automotive Suffix

Device:	PLA133-97:	Low-Power DC to 160 MHz 1:9 Fanout Buffer IC
Package:	Q =	16-Lead Wettable Flanks VQFN Package (NiPdAu)
Temperature Range:	A =	–40°C to +125°C (Automotive Grade)
Media Type:	(blank) = R =	120/Tube 3,300/Reel
Automotive Suffix:	VXX =	Automotive Suffix in which “XX” is assigned by Microchip. Standard value “AO” is for standard automotive part.

Examples:

a) PLA133-97QAVAO — Low-Power DC to 160 MHz 1:9 Fanout Buffer IC, VQFN Package, –40°C to +125°C, 120/Tube, Standard automotive

b) PLA133-97QA-RVAO — Low-Power DC to 160 MHz 1:9 Fanout Buffer IC, VQFN Package, –40°C to +125°C, 3,300/Reel, Standard automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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