UltraScale Architecture and Product Data Sheet: Overview

DS890 (v3.10) August 21, 2019 **Product Specification**

General Description

Xilinx® UltraScale™ architecture comprises high-performance FPGA, MPSoC, and RFSoC families that address a vast spectrum of system requirements with a focus on lowering total power consumption through numerous innovative technological advancements.

Kintex® UltraScale FPGAs: High-performance FPGAs with a focus on price/performance, using both monolithic and next-generation stacked silicon interconnect (SSI) technology. High DSP and block RAM-to-logic ratios and next-generation transceivers, combined with low-cost packaging, enable an optimum blend of capability and cost.

Kintex UltraScale+™ FPGAs: Increased performance and on-chip UltraRAM memory to reduce BOM cost. The ideal mix of high-performance peripherals and cost-effective system implementation. Kintex UltraScale+ FPGAs have numerous power options that deliver the optimal balance between the required system performance and the smallest power envelope.

Virtex® UltraScale FPGAs: High-capacity, high-performance FPGAs enabled using both monolithic and next-generation SSI technology. Virtex UltraScale devices achieve the highest system capacity, bandwidth, and performance to address key market and application requirements through integration of various system-level functions.

Virtex UltraScale+ FPGAs: The highest transceiver bandwidth, highest DSP count, and highest on-chip and in-package memory available in the UltraScale architecture. Virtex UltraScale+ FPGAs also provide numerous power options that deliver the optimal balance between the required system performance and the smallest power envelope.

Zynq® UltraScale+ MPSoCs: Combine the Arm® v8-based Cortex®-A53 high-performance energy-efficient 64-bit application processor with the Arm Cortex-R5F real-time processor and the UltraScale architecture to create the industry's first programmable MPSoCs. Provide unprecedented power savings, heterogeneous processing, and programmable acceleration.

Zynq® UltraScale+ RFSoCs: Combine RF data converter subsystem and forward error correction with industry-leading programmable logic and heterogeneous processing capability. Integrated RF-ADCs, RF-DACs, and soft-decision FECs (SD-FEC) provide the key subsystems for multiband, multi-mode cellular radios and cable infrastructure.

Family Comparisons

Table 1: **Device Resources**

	Kintex UltraScale FPGA	Kintex UltraScale+ FPGA	Virtex UltraScale FPGA	Virtex UltraScale+ FPGA	Zynq UltraScale+ MPSoC	Zynq UltraScale+ RFSoC
MPSoC Processing System					✓	✓
RF-ADC/DAC						✓
SD-FEC						✓
System Logic Cells (K)	318–1,451	356–1,143	783–5,541	862–8,938	103–1,143	678–930
Block Memory (Mb)	12.7–75.9	12.7–34.6	44.3–132.9	23.6–94.5	4.5–34.6	27.8–38.0
UltraRAM (Mb)		0–36		90–360	0–36	13.5–22.5
HBM DRAM (GB)				0–16		
DSP (Slices)	768–5,520	1,368–3,528	600–2,880	2,280–12,288	240–3,528	3,145–4,272
DSP Performance (GMAC/s)	8,180	6,287	4,268	21,897	6,287	7,613
Transceivers	12–64	16–76	36–120	32–128	0–72	8–16
Max. Transceiver Speed (Gb/s)	16.3	32.75	30.5	58.0	32.75	32.75
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,268	5,616	8,384	3,268	1,048
Memory Interface Performance (Mb/s)	2,400	2,666	2,400	2,666	2,666	2,666
I/O Pins	312–832	280–668	338–1,456	208–2,072	82–668	280–408

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Summary of Features

RF Data Converter Subsystem Overview

Most Zynq UltraScale+ RFSoCs include an RF data converter subsystem, which contains multiple radio frequency analog to digital converters (RF-ADCs) and multiple radio frequency digital to analog converters (RF-DACs). The high-precision, high-speed, power efficient RF-ADCs and RF-DACs can be individually configured for real data or can be configured in pairs for real and imaginary I/Q data.

Soft Decision Forward Error Correction (SD-FEC) Overview

Some Zynq UltraScale+ RFSoCs include highly flexible soft-decision FEC blocks for decoding and encoding data as a means to control errors in data transmission over unreliable or noisy communication channels. The SD-FEC blocks support low-density parity check (LDPC) decode/encode and Turbo decode for use in 5G wireless, backhaul, DOCSIS, and LTE applications.

Processing System Overview

Zynq UltraScale+ MPSoCs and RFSoCs feature dual and quad core variants of the Arm Cortex-A53 (APU) with dual-core Arm Cortex-R5F (RPU) processing system (PS). Some devices also include a dedicated Arm Mali™-400 MP2 graphics processing unit (GPU). See Table 2.

Table 2: **Zynq UltraScale+ MPSoC and RFSoC Device Features**

	MPSoC			RFSoC
	CG Devices	**EG Devices**	**EV Devices**	**DR Devices**
APU	Dual-core Arm Cortex-A53	Quad-core Arm Cortex-A53	Quad-core Arm Cortex-A53	Quad-core Arm Cortex-A53
RPU	Dual-core Arm Cortex-R5F	Dual-core Arm Cortex-R5F	Dual-core Arm Cortex-R5F	Dual-core Arm Cortex-R5F
GPU	–	Mali-400MP2	Mali-400MP2	–
VCU	–	–	H.264/H.265	–

To support the processors' functionality, a number of peripherals with dedicated functions are included in the PS. For interfacing to external memories for data or configuration storage, the PS includes a multi-protocol dynamic memory controller, a DMA controller, a NAND controller, an SD/eMMC controller and a Quad SPI controller. In addition to interfacing to external memories, the APU also includes a Level-1 (L1) and Level-2 (L2) cache hierarchy; the RPU includes an L1 cache and Tightly Coupled memory subsystem. Each has access to a 256KB on-chip memory.

For high-speed interfacing, the PS includes 4 channels of transmit (TX) and receive (RX) pairs of transceivers, called PS-GTR transceivers, supporting data rates of up to 6.0Gb/s. These transceivers can interface to the high-speed peripheral blocks that support PCIe at 5.0GT/s (Gen 2) as a root complex or Endpoint in x1, x2, or x4 configurations; Serial-ATA (SATA) at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates; and up to two lanes of Display Port at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s data rates. The PS-GTR transceivers can also interface to components over USB 3.0 and Serial Gigabit Media Independent Interface (SGMII).

For general connectivity, the PS includes: a pair of USB 2.0 controllers, which can be configured as host, device, or On-The-Go (OTG); an I2C controller; a UART; and a CAN2.0B controller that conforms to

ISO11898-1. There are also four triple speed Ethernet MACs and 128 bits of GPIO, of which 78 bits are available through the MIO and 96 through the EMIO.

High-bandwidth connectivity based on the Arm AMBA® AXI4 protocol connects the processing units with the peripherals and provides interface between the PS and the programmable logic (PL).

For additional information, go to: DS891, *Zynq UltraScale+ MPSoC Overview*.

I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken

Data is transported on and off chip through a combination of the high-performance parallel SelectIO™ interface and high-speed serial transceiver connectivity. I/O blocks provide support for cutting-edge memory interface and network protocols through flexible I/O standard and voltage support. The serial transceivers in the UltraScale architecture-based devices transfer data up to 58.0Gb/s, enabling 25G+ backplane designs with dramatically lower power per bit than previous generation transceivers. All transceivers, except the PS-GTR, support the required data rates for 8.0GT/s (Gen3), and 16.0GT/s (Gen4) for PCIe. The integrated blocks for PCIe can be configured for Endpoint or Root Port, supporting a variety of link widths and speeds depending on the targeted device speed grade and package. Integrated blocks for 150Gb/s Interlaken and 100Gb/s Ethernet (100G MAC/PCS) extend the capabilities of UltraScale devices, enabling simple, reliable support for Nx100G switch and bridge applications. Virtex UltraScale+ HBM devices include Cache Coherent Interconnect for Accelerators (CCIX) ports for coherently sharing data with different processors.

Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as hybrid memory cube (HMC).

Routing, SSI, Logic, Storage, and Signal Processing

Configurable Logic Blocks (CLBs) containing 6-input look-up tables (LUTs) and flip-flops, DSP slices with 27x18 multipliers, 36Kb block RAMs with built-in FIFO and ECC support, and 4Kx72 UltraRAM blocks (in UltraScale+ devices) are all connected with an abundance of high-performance, low-latency interconnect. In addition to logical functions, the CLB provides shift register, multiplexer, and carry logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable block RAMs. The DSP slice, with its 96-bit-wide XOR functionality, 27-bit pre-adder, and 30-bit A input, performs numerous independent functions including multiply accumulate, multiply add, and pattern detect. In addition to the device interconnect, in devices using SSI technology, signals can cross between super-logic regions (SLRs) using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation bus data widths. Virtex UltraScale+ HBM devices include up to 16GB of high bandwidth memory.

Configuration, Encryption, and System Monitoring

The configuration and encryption block performs numerous device-level functions critical to the successful operation of the FPGA, MPSoC, or RFSoC. This high-performance configuration block enables device configuration from external media through various protocols, including PCIe, often with no requirement to use multi-function I/O pins during configuration. The configuration block also provides 256-bit AES-GCM decryption capability at the same performance as unencrypted configuration. Additional features include SEU detection and correction, partial reconfiguration support, and battery-backed RAM or eFUSE technology for AES key storage to provide additional security. The System Monitor enables the monitoring of the physical environment via on-chip temperature and supply sensors and can also monitor up to 17 external analog inputs. With Zynq UltraScale+ MPSoCs and RFSoCs, the device is booted via the Configuration and Security Unit (CSU), which supports secure boot via the 256-bit AES-GCM and SHA/384 blocks. The cryptographic engines in the CSU can be used after boot for user encryption.

Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale devices in the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to UG583, *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

Kintex UltraScale FPGA Feature Summary

Table 3: **Kintex UltraScale FPGA Feature Summary**

	KU025[1]	KU035	KU040	KU060	KU085	KU095	KU115
System Logic Cells	318,150	444,343	530,250	725,550	1,088,325	1,176,000	1,451,100
CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Maximum Distributed RAM (Mb)	4.1	5.9	7.0	9.1	13.4	4.7	18.3
Block RAM Blocks	360	540	600	1,080	1,620	1,680	2,160
Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
CMTs (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
I/O DLLs	24	40	40	48	56	64	64
Maximum HP I/Os[2]	208	416	416	520	572	650	676
Maximum HR I/Os[3]	104	104	104	104	104	52	156
DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
System Monitor	1	1	1	1	2	1	2
PCIe Gen3 x8	1	2	3	3	4	4	6
150G Interlaken	0	0	0	0	0	2	0
100G Ethernet	0	0	0	0	0	2	0
GTH 16.3Gb/s Transceivers[4]	12	16	20	32	56	32	64
GTY 16.3Gb/s Transceivers[5]	0	0	0	0	0	32	0
Transceiver Fractional PLLs	0	0	0	0	0	16	0

Notes:
1. Certain advanced configuration features are not supported in the KU025. Refer to the Configuring FPGAs section for details.
2. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s. See Table 4.
5. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See Table 4.

Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 4: **Kintex UltraScale Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)	Package Dimensions (mm)	KU025	KU035	KU040	KU060	KU085	KU095	KU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY(4)	HR, HP GTH
SFVA784(5)	23x23		104, 364 8	104, 364 8				
FBVA676(5)	27x27		104, 208 16	104, 208 16				
FBVA900(5)	31x31		104, 364 16	104, 364 16				
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48
FFVC1517	40x40						52, 468 20, 20	
FLVD1517	40x40							104, 234 64
FFVB1760	42.5x42.5						52, 650 32, 16	
FLVB1760	42.5x42.5					104, 572 44		104, 598 52
FLVD1924	45x45							156, 676 52
FLVF1924	45x45					104, 520 56		104, 624 64
FLVA2104	47.5x47.5							156, 676 52
FFVB2104	47.5x47.5						52, 650 32, 32	
FLVB2104	47.5x47.5							104, 598 64

Notes:

1. Go to Ordering Information for package designation details.
2. FB/FF/FL packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.
4. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s.
5. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s.

Kintex UltraScale+ FPGA Feature Summary

Table 5: **Kintex UltraScale+ FPGA Feature Summary**

	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
System Logic Cells	355,950	474,600	599,550	653,100	746,550	1,143,450
CLB Flip-Flops	325,440	433,920	548,160	597,120	682,560	1,045,440
CLB LUTs	162,720	216,960	274,080	298,560	341,280	522,720
Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8
Block RAM Blocks	360	480	912	600	744	984
Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6
UltraRAM Blocks	48	64	0	80	112	128
UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0
CMTs (1 MMCM and 2 PLLs)	4	4	4	8	4	11
Max. HP I/O(1)	208	208	208	416	208	572
Max. HD I/O(2)	96	96	96	96	96	96
DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968
System Monitor	1	1	1	1	1	1
GTH Transceiver 16.3Gb/s	0	0	28	32	28	44
GTY Transceivers 32.75Gb/s(3)	16	16	0	20	0	32
Transceiver Fractional PLLs	8	8	14	26	14	38
PCIe Gen3 x16	1	1	0	4	0	5
150G Interlaken	0	0	0	1	0	4
100G Ethernet w/RS-FEC	0	1	0	2	0	4

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s. See Table 6.

Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 6: **Kintex UltraScale+ Device-Package Combinations and Maximum I/Os**

Package (1)(2)(4)	Package Dimensions (mm)	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SFVB784(3)	23x23	96, 208 0, 16	96, 208 0, 16				
FFVA676(3)	27x27	48, 208 0, 16	48, 208 0, 16				
FFVB676	27x27	72, 208 0, 16	72, 208 0, 16				
FFVD900(3)	31x31	96, 208 0, 16	96, 208 0, 16		96, 312 16, 0		
FFVE900	31x31			96, 208 28, 0		96, 208 28, 0	
FFVA1156(3)	35x35				48, 416 20, 8		48, 468 20, 8
FFVE1517	40x40				96, 416 32, 20		96, 416 32, 24
FFVA1760	42.5x42.5						96, 416 44, 32
FFVE1760	42.5x42.5						96, 572 32, 24

Notes:

1. Go to Ordering Information for package designation details.
2. FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s.
4. Packages with the same last letter and number sequence, e.g., A676, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.

Virtex UltraScale FPGA Feature Summary

Table 7: **Virtex UltraScale FPGA Feature Summary**

	VU065	VU080	VU095	VU125	VU160	VU190	VU440
System Logic Cells	783,300	975,000	1,176,000	1,566,600	2,026,500	2,349,900	5,540,850
CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Maximum Distributed RAM (Mb)	4.8	3.9	4.8	9.7	12.7	14.5	28.7
Block RAM Blocks	1,260	1,421	1,728	2,520	3,276	3,780	2,520
Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
CMT (1 MMCM, 2 PLLs)	10	16	16	20	28	30	30
I/O DLLs	40	64	64	80	120	120	120
Maximum HP I/Os(1)	468	780	780	780	650	650	1,404
Maximum HR I/Os(2)	52	52	52	104	52	52	52
DSP Slices	600	672	768	1,200	1,560	1,800	2,880
System Monitor	1	1	1	2	3	3	3
PCIe Gen3 x8	2	4	4	4	4	6	6
150G Interlaken	3	6	6	6	8	9	0
100G Ethernet	3	4	4	6	9	9	3
GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48
GTY 30.5Gb/s Transceivers	20	32	32	40	52	60	0
Transceiver Fractional PLLs	10	16	16	20	26	30	0

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Virtex UltraScale Device-Package Combinations and Maximum I/Os

Table 8: **Virtex UltraScale Device-Package Combinations and Maximum I/Os**

Package(1)(2)(3)	Package Dimensions (mm)	VU065	VU080	VU095	VU125	VU160	VU190	VU440
		HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY
FFVC1517	40x40	52, 468 20, 20	52, 468 20, 20	52, 468 20, 20				
FFVD1517	40x40		52, 286 32, 32	52, 286 32, 32				
FLVD1517	40x40				52, 286 40, 32			
FFVB1760	42.5x42.5		52, 650 32, 16	52, 650 32, 16				
FLVB1760	42.5x42.5				52, 650 36, 16			
FFVA2104	47.5x47.5		52, 780 28, 24	52, 780 28, 24				
FLVA2104	47.5x47.5				52, 780 28, 24			
FFVB2104	47.5x47.5		52, 650 32, 32	52, 650 32, 32				
FLVB2104	47.5x47.5				52, 650 40, 36			
FLGB2104	47.5x47.5					52, 650 40, 36	52, 650 40, 36	
FFVC2104	47.5x47.5			52, 364 32, 32				
FLVC2104	47.5x47.5				52, 364 40, 40			
FLGC2104	47.5x47.5					52, 364 52, 52	52, 364 52, 52	
FLGB2377	50x50							52, 1248 36, 0
FLGA2577	52.5x52.5						0, 448 60, 60	
FLGA2892	55x55							52, 1404 48, 0

Notes:

1. Go to Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.

Virtex UltraScale+ FPGA Feature Summary

Table 9: **Virtex UltraScale+ FPGA Feature Summary**

	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P	VU27P	VU29P
System Logic Cells	862,050	1,313,763	1,724,100	2,586,150	2,835,000	3,780,000	8,937,600	2,835,000	3,780,000
CLB Flip-Flops	788,160	1,201,154	1,576,320	2,364,480	2,592,000	3,456,000	8,171,520	2,592,000	3,456,000
CLB LUTs	394,080	600,577	788,160	1,182,240	1,296,000	1,728,000	4,085,760	1,296,000	1,728,000
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	58.4	36.2	48.3
Block RAM Blocks	720	1,024	1,440	2,160	2,016	2,688	2,160	2,016	2,688
Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	75.9	70.9	94.5
UltraRAM Blocks	320	470	640	960	960	1,280	320	960	1,280
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	270.0	360.0
HBM DRAM (GB)	–	–	–	–	–	–	–	–	–
CMTs (1 MMCM and 2 PLLs)	10	20	20	30	12	16	40	16	16
Max. HP I/O(1)	520	832	832	832	624	832	1,976	520	676
Max. HD I/O(2)	–	–	–	–	–	–	96	–	–
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	3,840	9,216	12,288
System Monitor	1	2	2	3	3	4	4	4	4
GTY Transceivers 32.75Gb/s(3)	40	80	80	120	96	128	80	32	32
GTM Transceivers 58.0Gb/s(3)	–	–	–	–	–	–	–	48	48
100G / 50G KP4 FEC	–	–	–	–	–	–	–	24/48	24/48
Transceiver Fractional PLLs	20	40	40	60	48	64	40	40	40
PCIe Gen3 x16	2	4	4	6	3	4	0	1	1
PCIe Gen3 x16 / Gen4 x8 / CCIX(4)	–	–	–	–	–	–	8	–	–
150G Interlaken	3	4	6	9	6	8	0	8	8
100G Ethernet w/RS-FEC	3	4	6	9	9	12	0	15	15

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s. See Table 10.
4. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. Go to PG213, *UltraScale+ Devices Integrated Block for PCI Express Product Guide*, for details on compatibility mode.

Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 10: **Virtex UltraScale+ Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P	VU27P	VU29P
		HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, HD, GTY	HP, GTY, GTM	HP, GTY, GTM
FFVC1517	40x40	520, 40								
FLGF1924(5)	45x45					624, 64				
FLVA2104	47.5x47.5		832, 52	832, 52						
FLGA2104	47.5x47.5				832, 52					
FHGA2104	52.5x52.5(6)						832, 52			
FLVB2104	47.5x47.5		702, 76	702, 76						
FLGB2104	47.5x47.5				702, 76	572, 76				
FHGB2104	52.5x52.5(6)						702, 76			
FLVC2104	47.5x47.5		416, 80	416, 80						
FLGC2104	47.5x47.5				416, 104	416, 96				
FHGC2104	52.5x52.5(6)						416, 104			
FSGD2104	47.5x47.5				676, 76	572, 76				
FIGD2104	52.5x52.5(6)						676, 76		676, 16, 30	676, 16, 30
FLGA2577	52.5x52.5				448, 120	448, 96	448, 128			
FSGA2577	52.5x52.5						448, 128		448, 32, 48	448, 32, 48
FSVA3824	65x65							1976, 96, 48		
FSVB3824	65x65							1664, 96, 80		

Notes:

1. Go to Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.
4. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.
5. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s.
6. These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

Table 11: **Virtex UltraScale+ HBM FPGA Feature Summary**

	VU31P	VU33P	VU35P	VU37P	VU45P	VU47P
System Logic Cells	961,800	961,800	1,906,800	2,851,800	1,906,800	2,851,800
CLB Flip-Flops	879,360	879,360	1,743,360	2,607,360	1,743,360	2,607,360
CLB LUTs	439,680	439,680	871,680	1,303,680	871,680	1,303,680
Max. Distributed RAM (Mb)	12.5	12.5	24.6	36.7	24.6	36.7
Block RAM Blocks	672	672	1,344	2,016	1,344	2,016
Block RAM (Mb)	23.6	23.6	47.3	70.9	47.3	70.9
UltraRAM Blocks	320	320	640	960	640	960
UltraRAM (Mb)	90.0	90.0	180.0	270.0	180.0	270.0
HBM DRAM (GB)	4	8	8	8	16	16
CMTs (1 MMCM and 2 PLLs)	4	4	8	12	8	12
Max. HP I/O(1)	208	208	416	624	416	624
DSP Slices	2,880	2,880	5,952	9,024	5,952	9,024
System Monitor	1	1	2	3	2	3
GTY Transceivers 32.75Gb/s(2)	32	32	64	96	64	96
GTM Transceivers 58.0Gb/s(3)	–	–	–	–	–	–
100G / 50G KP4 FEC	–	–	–	–	–	–
Transceiver Fractional PLLs	16	16	32	48	32	48
PCIe Gen3 x16	0	0	1	2	1	2
PCIe Gen3 x16 / Gen4 x8 / CCIX(3)	4	4	4	4	4	4
150G Interlaken	–	–	2	4	2	4
100G Ethernet w/RS-FEC	2	2	5	8	5	8

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s. See Table 12.
3. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. Go to PG213, *UltraScale+ Devices Integrated Block for PCI Express Product Guide*, for details on compatibility mode.

Virtex UltraScale+ HBM Device-Package Combinations and Maximum I/Os

Table 12: **Virtex UltraScale+ HBM Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)	Package Dimensions (mm)	VU31P	VU33P	VU35P	VU37P	VU45P	VU47P
		HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY
FSVH1924	45x45	208, 32					
FSVH2104	47.5x47.5		208, 32	416, 64		416, 64	
FSVH2892	55x55			416, 64	624, 96	416, 64	624, 96

Notes:
1. Go to Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.
4. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.

Zynq UltraScale+ MPSoC: CG Device Feature Summary

Table 13: **Zynq UltraScale+ MPSoC: CG Device Feature Summary**

	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Application Processing Unit	Dual-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache						
Real-Time Processing Unit	Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM						
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC						
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters						
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII						
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8
Block RAM Blocks	150	216	128	144	714	312	912
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1
UltraRAM Blocks	0	0	48	64	0	96	0
UltraRAM (Mb)	0	0	13.5	18.0	0	27.0	0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520
CMTs	3	3	4	4	4	8	4
Max. HP I/O(1)	156	156	156	156	208	416	208
Max. HD I/O(2)	96	96	96	96	120	48	120
System Monitor	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s(3)	0	0	16	16	24	24	24
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0
Transceiver Fractional PLLs	0	0	8	8	12	12	12
PCIe Gen3 x16	0	0	2	2	0	2	0
150G Interlaken	0	0	0	0	0	0	0
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See Table 14.

Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Table 14: **Zynq UltraScale+ MPSoC: CG Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0					
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0					
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0			
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0	
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0
FFVC1156	35x35						48, 312 20, 0	
FFVF1517	40x40						48, 416 24, 0	

Notes:

1. Go to Ordering Information for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2CG and ZU3CG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os. Packages that bond out 170 PS I/O support DDR 32-bit only.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CCO} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+ MPSoC: EG Device Feature Summary

Table 15: **Zynq UltraScale+ MPSoC: EG Device Feature Summary**

	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache										
Real-Time Processing Unit	Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM										
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC										
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters										
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII										
Graphic Processing Unit	Arm Mali-400 MP2; 64KB L2 Cache										
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550	653,100	746,550	926,194	1,143,450
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160	597,120	682,560	846,806	1,045,440
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080	298,560	341,280	423,403	522,720
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
Block RAM Blocks	150	216	128	144	714	312	912	600	744	796	984
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
UltraRAM Blocks	0	0	48	64	0	96	0	80	112	102	128
UltraRAM (Mb)	0	0	13.5	18.0	0	27.0	0	22.5	31.5	28.7	36.0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
CMTs	3	3	4	4	4	8	4	8	4	11	11
Max. HP I/O(1)	156	156	156	156	208	416	208	416	208	572	572
Max. HD I/O(2)	96	96	96	96	120	48	120	96	120	96	96
System Monitor	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s(3)	0	0	16	16	24	24	24	32	24	44	44
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0	16	0	28	28
Transceiver Fractional PLLs	0	0	8	8	12	12	12	24	12	36	36
PCIe Gen3 x16	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	1	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	2	0	2	4

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See Table 16.

Zynq UltraScale+ MPSoC: EG Device-Package Combinations and Maximum I/Os

Table 16: **Zynq UltraScale+ MPSoC: EG Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0									
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0									
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0							
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0					
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0		48, 156 16, 0		
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0		120, 208 24, 0		
FFVC1156	35x35						48, 312 20, 0		48, 312 20, 0			
FFVB1517	40x40								72, 416 16, 0		72, 572 16, 0	72, 572 16, 0
FFVF1517	40x40						48, 416 24, 0		48, 416 32, 0			
FFVC1760	42.5x42.5								96, 416 32, 16		96, 416 32, 16	96, 416 32, 16
FFVD1760	42.5x42.5										48, 260 44, 28	48, 260 44, 28
FFVE1924	45x45										96, 572 44, 0	96, 572 44, 0

Notes:

1. Go to Ordering Information for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os. Packages that bond out 170 PS I/O support DDR 32-bit only.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CCO} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+ MPSoC: EV Device Feature Summary

Table 17: **Zynq UltraScale+ MPSoC: EV Device Feature Summary**

	ZU4EV	ZU5EV	ZU7EV
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache		
Real-Time Processing Unit	Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM		
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC		
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters		
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII		
Graphic Processing Unit	Arm Mali-400 MP2; 64KB L2 Cache		
Video Codec	1	1	1
System Logic Cells	192,150	256,200	504,000
CLB Flip-Flops	175,680	234,240	460,800
CLB LUTs	87,840	117,120	230,400
Distributed RAM (Mb)	2.6	3.5	6.2
Block RAM Blocks	128	144	312
Block RAM (Mb)	4.5	5.1	11.0
UltraRAM Blocks	48	64	96
UltraRAM (Mb)	13.5	18.0	27.0
DSP Slices	728	1,248	1,728
CMTs	4	4	8
Max. HP I/O(1)	156	156	416
Max. HD I/O(2)	96	96	48
System Monitor	2	2	2
GTH Transceiver 16.3Gb/s(3)	16	16	24
GTY Transceivers 32.75Gb/s	0	0	0
Transceiver Fractional PLLs	8	8	12
PCIe Gen3 x16	2	2	2
150G Interlaken	0	0	0
100G Ethernet w/ RS-FEC	0	0	0

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See Table 18.

Zynq UltraScale+: EV Device-Package Combinations and Maximum I/Os

Table 18: **Zynq UltraScale+ MPSoC: EV Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)(4)	Package Dimensions (mm)	ZU4EV	ZU5EV	ZU7EV
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SFVC784(5)	23x23	96, 156 4, 0	96, 156 4, 0	
FBVB900	31x31	48, 156 16, 0	48, 156 16, 0	48, 156 16, 0
FFVC1156	35x35			48, 312 20, 0
FFVF1517	40x40			48, 416 24, 0

Notes:

1. Go to Ordering Information for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.
5. Packages with the same last letter and number sequence, e.g., B900, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.

Zynq UltraScale+ RFSoC: Device Feature Summary

Table 19: **Zynq UltraScale+ RFSoC Feature Summary**

		XCZU21DR	XCZU25DR	XCZU27DR	XCZU28DR	XCZU29DR	XCZU39DR	XCZU43DR	XCZU46DR	XCZU47DR	XCZU48DR	XCZU49DR
12-bit RF-ADC w/ DDC	# of ADCs	0	8	8	8	16	16	–	–	–	–	–
	Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	–	–	–	–	–
14-bit RF-ADC w/ DDC	# of ADCs	–	–	–	–	–	–	4	8 | 4	8	8	16
	Max Rate (GSPS)	–	–	–	–	–	–	5.0	2.5 | 5.0	5.0	5.0	2.5
14-bit RF-DAC w/ DUC	# of DACs	0	8	8	8	16	16	4	12	8	8	16
	Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	10.0	10.0	10.0	10.0	10.0
SD-FEC		8	0	0	8	0	0	0	8	0	8	0
Application Processing Unit		Quad-core Arm Cortex-A53 MPCore with CoreSight™; NEON and Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache										
Real-Time Processing Unit		Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM										
Embedded and External Memory		256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC										
General Connectivity		214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; Watchdog Timers; Triple Timer Counters										
High-Speed Connectivity		4 PS-GTR; PCIe® Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII										
System Logic Cells		930,300	678,318	930,300	930,300	930,300	930,300	930,300	930,300	930,300	930,300	930,300
CLB Flip-Flops		850,560	620,176	850,560	850,560	850,560	850,560	850,560	850,560	850,560	850,560	850,560
CLB LUTs		425,280	310,088	425,280	425,280	425,280	425,280	425,280	425,280	425,280	425,280	425,280
Distributed RAM (Mb)		13.0	9.6	13.0	13.0	13.0	13.0	13.0	13.0	13.0	13.0	13.0
Block RAM Blocks		1,080	792	1,080	1,080	1,080	1,080	1,080	1,080	1,080	1,080	1,080
Block RAM (Mb)		38.0	27.8	38.0	38.0	38.0	38.0	38.0	38.0	38.0	38.0	38.0
UltraRAM Blocks		80	48	80	80	80	80	80	80	80	80	80
UltraRAM (Mb)		22.5	13.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5
DSP Slices		4,272	3,145	4,272	4,272	4,272	4,272	4,272	4,272	4,272	4,272	4,272
CMTs		8	6	8	8	8	8	8	8	8	8	8
Maximum HP I/O		208	299	299	299	312	312	299	299	299	299	312
Maximum HD I/O		72	48	48	48	96	96	48	48	48	48	96
System Monitor		1	1	1	1	1	1	1	1	1	1	1
GTY Transceivers		16	8	16	16	16	16	16	16	16	16	16
Transceivers Fractional PLLs		8	4	8	8	8	8	8	8	8	8	8
PCIe Gen3 x16		2	1	2	2	2	2	–	–	–	–	–
PCIe Gen3 x16 / Gen4 x8 / CCIX(3)		–	–	–	–	–	–	2	2	2	2	2
150G Interlaken		1	1	1	1	1	1	1	1	1	1	1
100G Ethernet w/ RS-FEC		2	1	2	2	2	2	2	2	2	2	2

Table 20: **Zynq UltraScale+ RFSoC Device-Package Combinations and Maximum I/Os**

Package[1]	Dimensions	XCZU21DR	XCZU25DR	XCZU27DR	XCZU28DR	XCZU29DR	XCZU39DR	XCZU43DR	XCZU46DR	XCZU47DR	XCZU48DR	XCZU49DR
		PSIO, HDIO, HPIO, PS-GTR, GTY, RF-ADC, RF-DAC										
FFVD1156	35x35	214, 72, 208 4, 16, 0, 0										
FFVE1156	35x35		214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8			214, 48, 104 4, 8, 4, 4		214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8	
FSVE1156	35x35		214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8			214, 48, 104 4, 8, 4, 4		214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8	
FFVG1517	40x40		214, 48, 299 4, 8, 8, 8	214, 48, 299 4, 16, 8, 8	214, 48, 299 4, 16, 8, 8			214, 48, 299 4, 16, 4, 4		214, 48, 299 4, 16, 8, 8	214, 48, 299 4, 16, 8, 8	
FSVG1517	40x40		214, 48, 299 4, 8, 8, 8	214, 48, 299 4, 16, 8, 8	214, 48, 299 4, 16, 8, 8			214, 48, 299 4, 16, 4, 4		214, 48, 299 4, 16, 8, 8	214, 48, 299 4, 16, 8, 8	
FFVF1760	42.5x42.5					214, 96, 312 4, 16, 16, 16	214, 96, 312 4, 16, 16, 16					214, 96, 312 4, 16, 16, 16
FSVF1760	42.5x42.5					214, 96, 312 4, 16, 16, 16	214, 96, 312 4, 16, 16, 16					214, 96, 312 4, 16, 16, 16
FFVH1760	42.5x42.5								214, 48, 312 4, 16, 12[2], 12			
FSVH1760	42.5x42.5								214, 48, 312 4, 16, 12[2], 12			

Notes:
1. Package[2]s with the same last letter and number sequence, e.g., B900, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
2. Of these 12 RF-ADCs, 8 can operate up to 2.5 GSPS and 4 can operate up to 5.0 GSPS.

Device Layout

UltraScale devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of Zynq UltraScale+ MPSoCs and RFSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. Figure 1 shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.

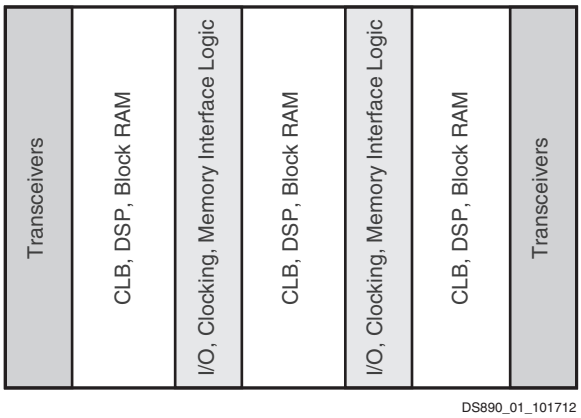

Figure 1: **FPGA with Columnar Resources**

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of device size or the mix of resources in the region, enabling repeatable timing results. Each segmented clock region contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.

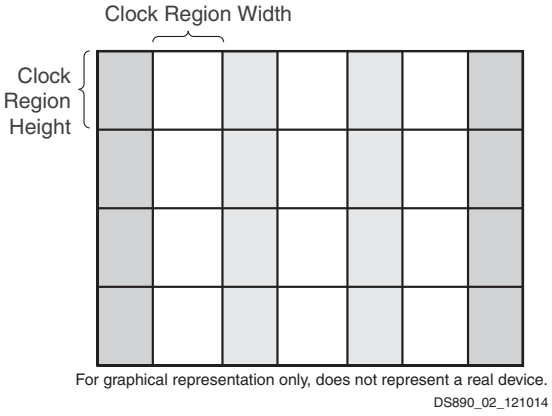

Figure 2: **Column-Based FPGA Divided into Clock Regions**

RF Data Converter Subsystem

Zynq UltraScale+ RFSoCs contain an RF data converter subsystem consisting of multiple RF-ADCs and RF-DACs.

RF-ADCs

Each of the RF-ADCs can be configured individually for real input signals or as a pair for I/Q input signals. The RF-ADC tile has one PLL and a clocking instance. Decimation filters in the RF-ADCs can operate in varying decimation modes at 80% of Nyquist bandwidth with 89dB stop-band attenuation. Each RF-ADC contains a 48-bit numerically controlled oscillator (NCO) and a dedicated high-speed, high-performance, differential input buffer with on-chip calibrated 100Ω termination.

RF-DACs

Each of the RF-DACs can be configured individually for real outputs or as a pair for I/Q output signal generation. The RF-DAC tile has one PLL and a clocking instance. Interpolation filters in the RF-DACs can operate in varying interpolation modes at 80% of Nyquist bandwidth with 89dB stop-band attenuation. Each RF-DAC contains a 48-bit NCO.

Soft-Decision Forward Error Correction (SD-FEC)

Some members of the Zynq UltraScale+ RFSoC family contain integrated SD-FEC blocks capable of encoding and decoding using LDPC codes and decoding using Turbo codes.

LDPC Decoding/Encoding

A range of quasi-cyclic codes can be configured over an AXI4-Lite interface. Code parameter memory can be shared across up to 128 codes. Codes can be selected on a block-by-block basis with the encoder able to reuse suitable decoder codes. The SD-FEC uses a normalized min-sum decoding algorithm with a normalization factor programmable from 0.0625 to 1 in increments of 0.0625. There can be between 1 and 63 iterations for each codeword. Early termination is specified for each codeword to be none, one, or both of the following:

- Parity check passes
- No change in hard information or parity bits since last operation

Soft or hard outputs are specified for each codeword to include information and optional parity with 6-bit soft log-likelihood ratio (LLR) on inputs and 8-bit LLR on outputs.

Turbo Decoding

In Turbo mode, the SD-FEC can use the Max, Max Scale, or Max Star algorithms. When using the Max Scale algorithm, the scale factor is programmable from 0.0625 to 1 in increments of 0.0625. There can be between 1 and 63 iterations for each codeword, specified using the AXI4-Stream control interface. Early termination is specified for each codeword to be none, one, or both of the following:

- CRC passes
- No change in hard decision since last iteration

Soft or hard outputs are specified for each codeword to include systematic and optionally parity 0 and parity 1 with 8-bit soft LLR on inputs and outputs.

Processing System (PS)

Zynq UltraScale+ MPSoCs and RFSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered Arm AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core Arm Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on Arm-v8A architecture, offering the best performance-to-power ratio. The Armv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port (ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the Arm CoreSight™ Debug System.

Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core Arm Cortex-R5F PS. Cortex-R5F cores are 32-bit real-time processor cores based on Arm-v7R architecture. Each of the Cortex-R5F cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5F cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the Arm CoreSight Debug System.

External Memory

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for Zynq UltraScale+ MPSoCs and RFSoCs and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

General Connectivity

There are many peripherals in the PS for connecting to external devices over industry standard protocols, including CAN2.0B, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption.

USB 3.0/2.0

The pair of USB controllers can be configured as host, device, or On-The-Go (OTG). The core is compliant to USB 3.0 specification and supports super, high, full, and low speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to 12 end points. While operating in USB 3.0 mode, the controller uses the serial transceiver and operates up to 5.0Gb/s. In USB 2.0 mode, the Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s. The ULPI is also connected in USB 3.0 mode to support high-speed operations.

Ethernet MAC

The four tri-speed ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. The MACs support jumbo frames and time stamping through the interfaces based on IEEE Std 1588v2. The ethernet MACs can be connected through the serial transceivers (SGMII), the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

High-Speed Connectivity

The PS includes four PS-GTR transceivers (transmit and receive), supporting data rates up to 6.0Gb/s and can interface to the peripherals for communication over PCIe, SATA, USB 3.0, SGMII, and DisplayPort.

PCIe

The integrated block for PCIe is compliant with PCI Express base specification 2.1 and supports x1, x2, and x4 configurations as root complex or end point, compliant to transaction ordering rules in both configurations. It has built-in DMA, supports one virtual channel and provides fully configurable base address registers.

SATA

Users can connect up to two external devices using the two SATA host port interfaces compliant to the SATA 3.1 specification. The SATA interfaces can operate at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates and are compliant with advanced host controller interface (AHCI) version 1.3 supporting partial and slumber power modes.

DisplayPort

The DisplayPort controller supports up to two lanes of source-only DisplayPort compliant with VESA DisplayPort v1.2a specification (source only) at 1.62Gb/s, 2.7Gb/s, and 5.4Gb/s data rates. The controller supports single stream transport (SST); video resolution up to 4Kx2K at a 30Hz frame rate; video formats Y-only, YCbCr444, YCbCr422, YCbCr420, RGB, YUV444, YUV422, xvYCC, and pixel color depth of 6, 8, 10, and 12 bits per color component.

Graphics Processing Unit (GPU)

The dedicated Arm Mali-400 MP2 GPU in the PS supports 2D and 3D graphics acceleration up to 1080p resolution. The Mali-400 supports OpenGL ES 1.1 and 2.0 for 3D graphics and Open VG 1.1 standards for 2D vector graphics. It has a geometry processor (GP) and 2 pixel processors to perform tile rendering operations in parallel. It has dedicated Memory management units for GP and pixel processors, which supports 4 KB page size. The GPU also has 64KB level-2 (L2) read-only cache. It supports 4X and 16X Full scene Anti-Aliasing (FSAA). It is fully autonomous, enabling maximum parallelization between APU and GPU. It has built-in hardware texture decompression, allowing the texture to remain compressed (in ETC format) in graphics hardware and decompress the required samples on the fly. It also supports efficient alpha blending of multiple layers in hardware without additional bandwidth consumption. It has a pixel fill rate of 2Mpixel/sec/MHz and a triangle rate of 0.1Mvertex/sec/MHz. The GPU supports extensive texture format for RGBA 8888, 565, and 1556 in Mono 8, 16, and YUV formats. For power sensitive applications, the GPU supports clock and power gating for each GP, pixel processors, and L2 cache. During power gating, GPU does not consume any static or dynamic power; during clock gating, it only consumes static power.

Video Codec Unit (VCU)

The video codec unit (VCU) provides multi-standard video encoding and decoding capabilities, including: High Efficiency Video Coding (HEVC), i.e., H.265; and Advanced Video Coding (AVC), i.e., H.264 standards. The VCU is capable of simultaneous encode and decode at rates up to 4Kx2K at 60 frames per second (fps) (approx. 600Mpixel/sec) or 8Kx4K at a reduced frame rate (~15fps).

Input/Output

All UltraScale devices, whether FPGA, MPSoC, or RFSoCs, have I/O pins for communicating to external components. In addition, in the PS, there are another 78 I/Os that the I/O peripherals use to communicate to external components, referred to as multiplexed I/O (MIO). If more than 78 pins are required by the I/O peripherals, the I/O pins in the PL can be used to extend the MPSoC or RFSoC interfacing capability, referred to as extended MIO (EMIO).

The number of I/O pins in UltraScale FPGAs and in the programmable logic of Zynq UltraScale+ MPSoCs and RFSoCs varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-range (HR), high-performance (HP), or high-density (HD). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V. The HD I/Os are reduced-feature I/Os organized in banks of 24, providing voltage support from 1.2V to 3.3V.

All I/O pins are organized in banks, with 52 HP or HR pins per bank or 24 HD pins per bank. Each bank has one common V_{CCO} output buffer power supply, which also powers certain input buffers. In addition, HR banks can be split into two half-banks, each with their own V_{CCO} supply. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Four types of transceivers are used in the UltraScale architecture: GTH, GTY, and GTM in FPGAs, GTH and GTY in the PL in MPSoCs and RFSoCs, and PS-GTR in the PS of MPSoCs and RFSoCs. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. Table 21 compares the available transceivers.

Table 21: **Transceiver Information**

	Kintex UltraScale		Kintex UltraScale+		Virtex UltraScale		Virtex UltraScale+		Zynq UltraScale+ MPSoCs and RFSoCs		
Type	GTH	GTY	GTH	GTY	GTH	GTY	GTY	GTM	PS-GTR	GTH	GTY
Qty	16–64	0–32	20–60	0–60	20–60	0–60	40–128	0–48	4	0–44	0–28
Max. Data Rate	16.3Gb/s	16.3Gb/s	16.3Gb/s	32.75Gb/s	16.3Gb/s	30.5Gb/s	32.75Gb/s	58.0Gb/s	6.0Gb/s	16.3Gb/s	32.75Gb/s
Min. Data Rate	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	9.8Gb/s	1.25Gb/s	0.5Gb/s	0.5Gb/s
Key Apps	• Backplane • HMC	• Backplane • HMC	• Backplane • HMC	• 100G+ Optics • Chip-to-Chip • 25G+ Backplane • HMC	• Backplane • HMC	• 100G+ Optics • Chip-to-Chip • 25G+ Backplane • HMC	• 100G+ Optics • Chip-to-Chip • 25G+ Backplane • HMC	• 50G • 100G • 200G • 400G • OTU	• PCIe Gen2 • USB • Ethernet	• Backplane • HMC	• 100G+ Optics • Chip-to-Chip • 25G+ Backplane • HMC

GTH/GTY Transceivers

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter (GTH/GTY)

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver (GTH/GTY)

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

GTM Transceivers

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 16 and 160 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter (GTM)

The transmitter is fundamentally a parallel-to-serial converter. These transmitter outputs drive pulse amplitude modulated signals with either 4 levels (PAM4) or 2 levels (NRZ) to the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data can optionally leverage a Reed-Solomon, RS(544,514) Forward Error Correction encoder and/or 64b66b data encoder. The bit-serial output signal drives two package pins with PAM4 differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver (GTM)

The receiver is fundamentally a serial-to-parallel converter, changing the incoming PAM4 differential signal into a parallel stream of words. The receiver takes the incoming differential data stream, feeds it through automatic gain compensation (AGC) and a continuous time linear equalizer (CTLE), after which it is sampled with a high-speed analog to digital converter. Further equalization is completed digitally via a decision feedback equalizer (DFE) and feed forward equalizer (FFE) implemented in DSP logic before the recovered bits are parallelized and provided to the PCS. This equalization provides the flexibility to receive data over channels ranging from very short chip-to-chip to high loss backplane applications across all supported rates. Clock recovery circuitry generates a clock derived from the high-speed PLL to clock in serial data and provides an appropriately divided and phase-aligned clock, RXOUTCLK, to internal logic. Parallel data can optionally be transferred into an RS-FEC and/or 64b/66b decoder before being presented to the FPGA interface.

Integrated Interface Blocks for PCI Express Designs

The UltraScale architecture uses three different integrated blocks for PCIe. The integrated block on UltraScale devices is compliant with the PCI Express Base Specification v3.1 and can operate with a lane width of up to x8 and a speed up to 8.0GT/s (Gen3).

UltraScale+ devices use two types of integrated blocks: PCIE4 and PCIE4C, with most using the PCIE4 blocks. PCIE4 blocks are compliant to PCI Express Base Specification v3.1 and support up to Gen3 x16, and can also be configured for lower link width and speeds. The PCIE4 block does not support Gen4 operation.

Some devices, such as Virtex UltraScale+ HBM FPGAs, have only PCIE4C blocks or a combination of both PCIE4 and PCIE4C blocks. The PCIE4C block can implement both PCI Express and CCIX while PCIE4 blocks can implement only PCI Express.

PCIE4C blocks are compliant to the PCI Express Base Specification v3.1 supporting up to 8.0GT/s (Gen3) and compatible with PCI Express Base Specification v4.0 supporting up to 16.0GT/s (Gen4). PCIE4C blocks are also compliant with CCIX Base Specification v1.0 Version 0.9, supporting speeds up to 16.0GT/s. PCIE4C blocks support up to 16 lanes at Gen3 or up to 8 lanes at Gen4 and can be configured for lower link widths and speeds to conserve resources and power.

All integrated blocks for PCIe in the UltraScale architecture can be configured as Endpoint or Root Port. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA, MPSoC, or RFSoC.

The maximum lane widths and data rates per family are listed in Table 22.

Table 22: **PCIe Maximum Configurations**

	Kintex UltraScale	Kintex UltraScale+	Virtex UltraScale	Virtex UltraScale+	Zynq UltraScale+
Gen1 (2.5GT/s)	x8	x16	x8	x16	x16
Gen2 (5GT/s)	x8	x16	x8	x16	x16
Gen3 (8GT/s)	x8	x16	x8	x16	x16
Gen4 (16GT/s)(1)				x8	

Notes:

1. Transceivers in UltraScale+ devices support 16.0GT/s. Soft PCIe IP is available from Xilinx partners.

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides LogiCORE™ IP options to configure the integrated blocks for PCIe in all UltraScale and UltraScale+ devices. This includes AXI Streaming interfaces at the PCIe packet level and more advanced IP such as AXI to PCIe Bridges and DMA engines. This IP gives the designer control over many configurable parameters such as link width and speed, maximum payload size, and reference clock frequency. For a complete list of features that can be configured for each of the IP, go to the specific Product Guide.

Cache Coherent Interconnect for Accelerators (CCIX)

CCIX is a chip-to-chip interconnect operating at data rates up to 25Gb/s that allows two or more devices to share memory in a cache coherent manner. Using PCIe for the transport layer, CCIX can operate at several standard data rates (2.5, 5, 8, and 16Gb/s) with an additional high-speed 25Gb/s option. The specification employs a subset of full coherency protocols and ensures that FPGAs used as accelerators can coherently share data with processors using different instruction set architectures.

Virtex UltraScale+ HBM devices support CCIX data rates up to 16Gb/s and contain four CCIX ports and at least four integrated blocks for PCIe. Each CCIX port requires the use of one integrated block for PCIe. If not used with a CCIX port, the integrated blocks for PCIe can still be used for PCIe communication.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.

Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 20,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 23 shows the number of SLRs in devices that use SSI technology and their dimensions.

Table 23: **UltraScale and UltraScale+ 3D IC SLR Count and Dimensions**

	Kintex UltraScale		Virtex UltraScale				Virtex UltraScale+								
Device	KU085	KU115	VU125	VU160	VU190	VU440	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
# SLRs	2	2	2	3	3	3	2	2	3	3	4	1	1	2	3
SLR Width (in regions)	6	6	6	6	6	9	6	6	6	8	8	8	8	8	8
SLR Height (in regions)	5	5	5	5	5	5	5	5	5	4	4	4	4	4	4

Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600MHz, the phase-shift timing increment is 11.2ps.

PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

Zynq UltraScale+ MPSoCs and RFSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

Clock Distribution

Clocks are distributed throughout UltraScale devices via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs and RFSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, UltraScale architecture-based devices can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale devices support the highest bandwidth HMC configuration of 64 lanes with a single FPGA.

Block RAM

Every UltraScale architecture-based device contains a number of 36 Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Programmable Data Width

Each port can be configured as 32K × 1; 16K × 2; 8K × 4; 4K × 9 (or 8); 2K × 18 (or 16); 1K × 36 (or 32); or 512 × 72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

UltraRAM

UltraRAM is a high-density, dual-port, synchronous memory block available in UltraScale+ devices. Both of the ports share the same clock and can address all of the 4K x 72 bits. Each port can independently read from or write to the memory array. UltraRAM supports two types of write enable schemes. The first mode is consistent with the block RAM byte write enable mode. The second mode allows gating the data and parity byte writes separately. UltraRAM blocks can be connected together to create larger memory arrays. Dedicated routing in the UltraRAM column enables the entire column height to be connected together. If additional density is required, all the UltraRAM columns in an SLR can be connected together with a few fabric resources to create single instances of RAM approximately 100Mb in size. This makes UltraRAM an ideal solution for replacing external memories such as SRAM. Cascadable anywhere from 288Kb to 100Mb, UltraRAM provides the flexibility to fulfill many different memory requirements.

Error Detection and Correction

Each 64-bit-wide UltraRAM can generate, store and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process.

High Bandwidth Memory (HBM)

Virtex UltraScale+ HBM devices incorporate 4GB or 8GB HBM stacks adjacent to the FPGA die. Using stacked silicon interconnect technology, the FPGA communicates to the HBM stacks through memory controllers that connect to dedicated low-inductance interconnect in the silicon interposer. Each Virtex UltraScale+ HBM FPGA contains one or two HBM stacks, resulting in up to 16GB of HBM per FPGA.

The FPGA has 32 HBM AXI interfaces used to communicate with the HBM. Through a built-in switch mechanism, any of the 32 HBM AXI interfaces can access any memory address on either one or both of the HBM stacks due to the flexible addressing feature. This flexible connection between the FPGA and the HBM stacks results in easy floorplanning and timing closure. The memory controllers perform read and write reordering to improve bus efficiency. Data integrity is ensured through error checking and correction (ECC) circuitry.

Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27 × 18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors and external channels to the ADC.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ FPGAs and the PL of Zynq UltraScale+ MPSoCs and RFSoCs is similar to the Kintex UltraScale and Virtex UltraScale devices but with additional features including a PMBus interface.

Zynq UltraScale+ MPSoCs contain an additional System Monitor block in the PS. See Table 24.

Table 24: **Key System Monitor Features**

	Kintex UltraScale Virtex UltraScale	Kintex UltraScale+ Virtex UltraScale+ Zynq UltraScale+ PL	Zynq UltraScale+ PS
ADC	10-bit 200kSPS	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP	JTAG, I2C, DRP, PMBus	APB

In FPGAs and the PL of the MPSoCs and RFSoCs, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the PS MPSoC and RFSoC uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

Configuration

The UltraScale architecture-based devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale architecture-based devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to UG570, *UltraScale Architecture Configuration User Guide*.

UltraScale architecture-based devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

Booting MPSoCs and RFSoCs

Zynq UltraScale+ MPSoCs and RFSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5F, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).

After copying the FSBL to OCM, the processor executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL) such as U-Boot. Users obtain example SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, eMMC, or Quad-SPI) is configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or executable after boot.

Configuring FPGAs

The SPI (serial NOR) interface (x1, x2, x4, and dual x4 modes) and the BPI (parallel NOR) interface (x8 and x16 modes) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself, eliminating the need for an external controller. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, x4, and dual x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide that are especially useful for processor-driven configuration are also supported by the FPGA. In addition, the new media configuration access port (MCAP) provides a direct connection between the integrated block for PCIe and the configuration logic to simplify configuration over PCIe.

SEU detection and mitigation (SEM) IP, RSA authentication, post-configuration CRC, and Security Monitor (SecMon) IP are not supported in the KU025 FPGA.

Packaging

The UltraScale devices are available in a variety of organic flip-chip and lidless flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

Ordering Information

Table 25 shows the speed and temperature grades available in the different device families. V_{CCINT} supply voltage is listed in parentheses.

Table 25: **Speed Grade and Temperature Grade**

Device Family	XC Devices	Speed Grade and Temperature Grade			
		Commercial (C)	Extended (E)		Industrial (I)
		0°C to +85°C	0°C to +100°C	0°C to +110°C	–40°C to +100°C
Kintex UltraScale	All		-3E[1] (1.0V)		
			-2E (0.95V)		-2I (0.95V)
		-1C (0.95V)			-1I (0.95V)
					-1LI[1] (0.95V or 0.90V)
Kintex UltraScale+	All		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE[2] (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI (0.85V or 0.72V)
Virtex UltraScale	VU065 VU080 VU095 VU125 VU160 VU190		-3E (1.0V)		
			-2E (0.95V)		-2I (0.95V)
			-1HE (0.95V or 1.0V)		-1I (0.95V)
	VU440		-3E (1.0V)		
			-2E (0.95V)		-2I (0.95V)
		-1C (0.95V)			-1I (0.95V)
Virtex UltraScale+	VU3P VU5P VU7P VU9P VU11P VU13P VU27P VU29P		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE[2] (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
	VU19P		-2E (0.85V)		
			-1E (0.85V)		
	VU31P VU33P VU35P VU37P VU45P VU47P		-3E (0.90V)		
			-2E (0.85V)		
				-2LE[2] (0.85V or 0.72V)	
			-1E (0.85V)		

Table 25: **Speed Grade and Temperature Grade *(Cont'd)***

Device Family	XC Devices	Speed Grade and Temperature Grade			
		Commercial (C)	Extended (E)		Industrial (I)
		0°C to +85°C	0°C to +100°C	0°C to +110°C	–40°C to +100°C
Zynq UltraScale+	CG Devices		-2E (0.85V)		-2I (0.85V)
				-2LE(2)(3) (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI(3) (0.85V or 0.72V)
	ZU2EG ZU3EG		-2E (0.85V)		-2I (0.85V)
				-2LE(2)(3) (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI(3) (0.85V or 0.72V)
	ZU4EG ZU5EG ZU6EG ZU7EG ZU9EG ZU11EG ZU15EG ZU17EG ZU19EG		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE(2)(3) (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI(3) (0.85V or 0.72V)
	EV Devices		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE(2)(3) (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI(3) (0.85V or 0.72V)
	ZU21DR ZU25DR ZU27DR ZU28DR ZU29DR		-2E (0.85V)		-2I (0.85V)
				-2LE(2)(3) (0.85V or 0.72V)	-2LI (0.72V)(4)
			-1E (0.85V)		-1I (0.85V)
					-1LI(3) (0.85V or 0.72V)
	ZU39DR				-2I (0.85V)
					-2LI (0.72V)(4)
	ZU43DR ZU46DR ZU47DR ZU48DR ZU49DR		-2E (0.85V)		-2I (0.85V)
					-2LI (0.72V)(4)
			-1E (0.85V)		-1I (0.85V)
					-1LI(3) (0.72V)

Notes:

1. KU025 and KU095 are not available in -3E or -1LI speed/temperature grades.
2. In -2LE speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal at 0.85V or low voltage at 0.72V). Operation at 110°C Tj is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of device lifetime.
3. In Zynq UltraScale+ MPSoCs and RFSoCs, when operating the PL at low voltage (0.72V), the PS operates at nominal voltage (0.85V).
4. In -2LI speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C. Operation at 110°C Tj is limited to 5% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 5% of device lifetime.

The ordering information shown in Figure 3 applies to all packages in the Kintex UltraScale and Virtex UltraScale FPGAs. Refer to the Package Marking section of UG575, *UltraScale and UltraScale+ FPGAs Packaging and Pinouts User Guide* for a more detailed explanation of the device markings.

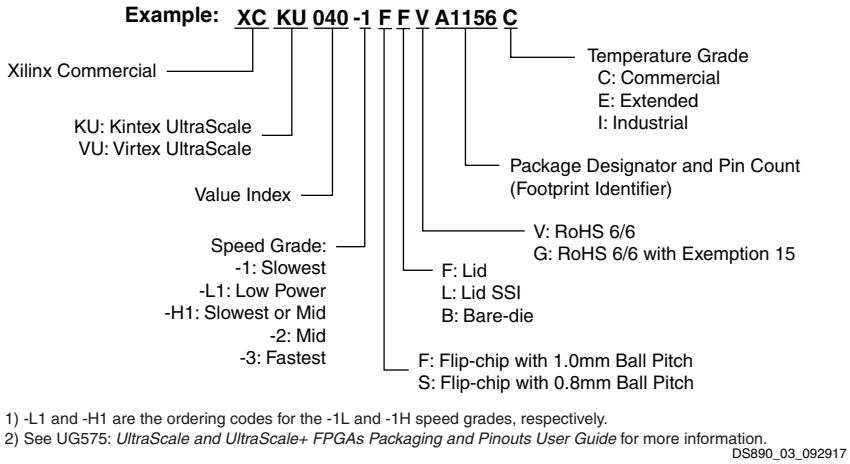

Figure 3: **Kintex UltraScale and Virtex UltraScale FPGA Ordering Information**

The ordering information shown in Figure 4 applies to all packages in the Kintex UltraScale+ and Virtex UltraScale+ FPGAs, and Figure 5 applies to Zynq UltraScale+MPSoCs and RFSoCs.

The -1L and -2L speed grades in the UltraScale+ families can run at one of two different V_{CCINT} operating voltages. At 0.72V, they operate at similar performance to the Kintex UltraScale and Virtex UltraScale devices with up to 30% reduction in power consumption. At 0.85V, they consume similar power to the Kintex UltraScale and Virtex UltraScale devices, but operate over 30% faster.

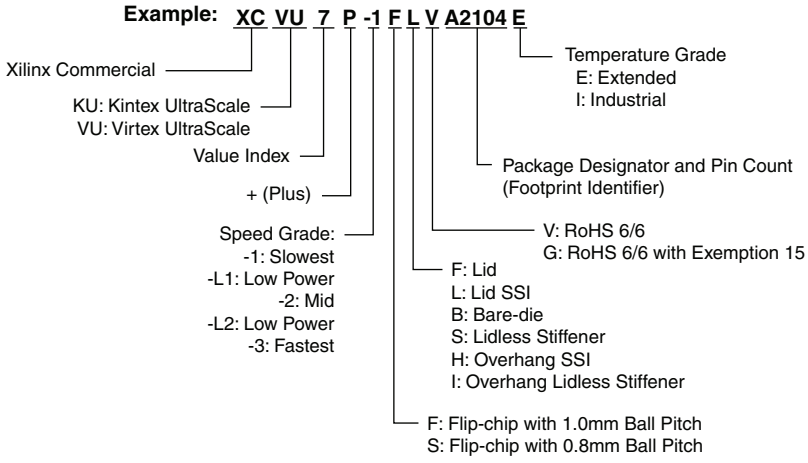

Figure 4: **UltraScale+ FPGA Ordering Information**

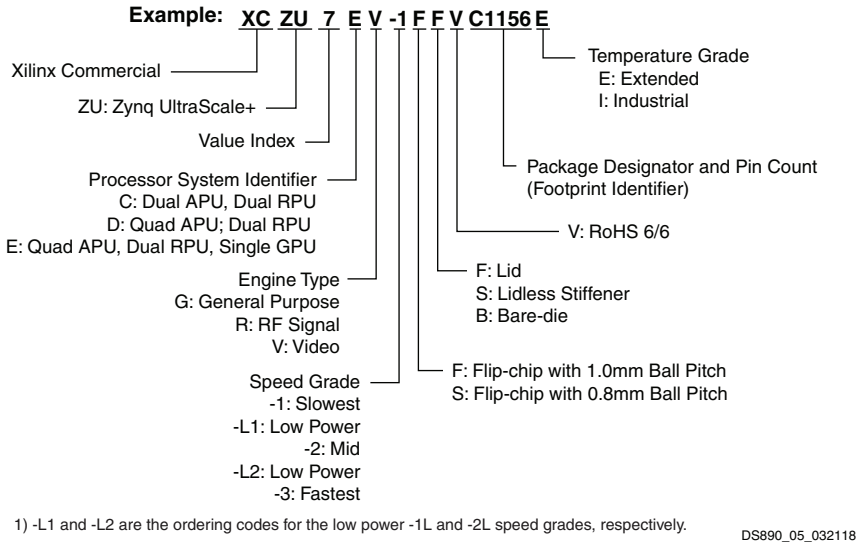

Figure 5: **Zynq UltraScale+ MPSoC and RFSoC Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
08/21/2019	3.10	Added VU19P and ZU43DR throughout document.
06/27/2019	3.9	Added VU45P and VU47P throughout document. Updated Routing, SSI, Logic, Storage, and Signal Processing, and High Bandwidth Memory (HBM). Added VU27P to Table 25.
05/13/2019	3.8	Updated VU27P in Table 9 and ZU39DR in Table 19.
02/20/2019	3.7	Added XCZU39DR, XCZU46DR, XCZU47DR, XCZU48DR, and XCZU49DR. Updated Table 19, Table 20, RF-ADCs, RF-DACs, and Table 25.
11/12/2018	3.6	Updated PCIe information throughout document: Processing System Overview, I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, Table 5, Table 13, Table 15, Table 17, Table 19, Table 21, Integrated Interface Blocks for PCI Express Designs, and Table 22. Updated VU27P resource and package information in Table 9 and Table 12.
08/21/2018	3.5	Changed document classification to Product Specification from Preliminary Product Specification. Updated RF Data Converter Subsystem Overview. Updated RF-ADCs and RF-DACs.
05/17/2018	3.4	Updated RF Data Converter Subsystem Overview, Table 19, RF-ADCs, and Table 25 (removed -3E, added -2LI and note 4 for the DR devices). Added FSGA2577 to Table 12.
03/12/2018	3.3	Added VU27P and VU29P: Updated Table 1, I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, Table 9, Table 12, High-Speed Serial Transceivers, and Table 21, and added GTM Transceivers. Updated Note 4 in Table 14 and Table 16.
01/23/2018	3.2	Updated RFADC/DAC rates in RF Data Converter Subsystem Overview, Table 19, RF-ADCs, and RF-DACs.
11/15/2017	3.1	Updated Table 20 with FSVE1156, FSVG1517, and FSVF1760 packages. Updated Figure 5.
10/03/2017	3.0	Added Zynq UltraScale+ RFSoC information throughout document. Updated General Description, Table 1, RF Data Converter Subsystem Overview, Soft Decision Forward Error Correction (SD-FEC) Overview, Processing System Overview (including Table 2), Configuration, Encryption, and System Monitoring, Table 23, Table 25, and Figure 5. Updated UltraRAM ZU4CG/ZU4EG/ZU4EV values in Table 13, Table 15, Table 17. Added Table 19, Table 20, RF Data Converter Subsystem Overview, and Soft Decision Forward Error Correction (SD-FEC) Overview. Updated Figure 3, Figure 4, and Figure 5.
02/15/2017	2.11	Updated Table 1, Table 9: Converted HBM from Gb to GB. Updated Table 13, Table 15, and Table 17: Updated DSP count for Zynq UltraScale+ MPSoCs. Updated Cache Coherent Interconnect for Accelerators (CCIX). Updated High Bandwidth Memory (HBM). Updated Table 25: Added-2E speed grade to all UltraScale+ devices. Removed -3E from XCZU2 and XCZU3.
11/09/2016	2.10	Updated Table 1. Added HBM devices to Table 9, Table 12, Table 23 and new High Bandwidth Memory (HBM) section. Added Cache Coherent Interconnect for Accelerators (CCIX) section.
09/27/2016	2.9	Updated Table 5, Table 14, Table 15, and Table 16.
06/03/2016	2.8	Added Zynq UltraScale+ MPSoC CG devices: Added Table 2. Updated Table 13, Table 14, Table 25, and Figure 5. Created separate tables for EG and EV devices: Table 15, Table 16, Table 17, and Table 18. Updated Table 1, Table 3, Table 5 and notes, Table 6 and notes, Table 7, Table 9, Table 12, Processing System Overview, and Processing System (PS) details.
02/17/2016	2.7	Added Migrating Devices. Updated Table 4, Table 5, Table 6, Table 12, Table 13, Table 14, and Figure 4.
12/15/2015	2.6	Updated Table 1, Table 5, Table 6, Table 9, Table 14, and Configuration.

Date	Version	Description of Revisions
11/24/2015	2.5	Updated Configuration, Encryption, and System Monitoring, Table 5, Table 9, Table 13, and Table 25.
10/15/2015	2.4	Updated Table 1, Table 3, Table 5, Table 7, Table 9, and Table 13 with System Logic Cells. Updated Figure 3. Updated Table 23.
09/29/2015	2.3	Added A1156 to KU095 in Table 4. Updated Table 5. Updated Max. Distributed RAM in Table 9. Updated Distributed RAM in Table 13. Added Table 23. Updated Table 25. Updated Figure 3.
08/14/2015	2.2	Updated Table 1. Added XCKU025 to Table 3, Table 4, and Table 25. Updated Table 7, Table 9, Table 13, Table 14, Table 22. Updated System Monitor. Added voltage information to Table 25.
04/27/2015	2.1	Updated Table 1, Table 3, Table 4, Table 5, Table 6, Table 7, Table 12, Table 13, Table 14, Table 21, I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, Integrated Interface Blocks for PCI Express Designs, USB 3.0/2.0, Clock Management, System Monitor, and Figure 3.
02/23/2015	2.0	UltraScale+ device information (Kintex UltraScale+ FPGA, Virtex UltraScale+ FPGA, and Zynq UltraScale+ MPSoC) added throughout document.
12/16/2014	1.6	Updated Table 1; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 3, Table 7; Table 8; and Table 21.
11/17/2014	1.5	Updated I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 1; Table 4; Table 7; Table 8; Table 21; Input/Output; and Figure 3.
09/16/2014	1.4	Updated Logic Cell information in Table 1. Updated Table 3; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 7; Table 8; Integrated Block for 100G Ethernet; and Figure 3.
05/20/2014	1.3	Updated Table 8.
05/13/2014	1.2	Added Ordering Information. Updated Table 1, Clocks and Memory Interfaces, Table 3, Table 7 (removed XCVU145; added XCVU190), Table 8 (removed XCVU145; removed FLVD1924 from XCVU160; added XCVU190; updated Table Notes), Table 21, Integrated Interface Blocks for PCI Express Designs, and Integrated Block for Interlaken, and Memory Interfaces.
02/06/2014	1.1	Updated PCIe information in Table 1 and Table 3. Added FFVJ1924 package to Table 8.
12/10/2013	1.0	Initial Xilinx release.

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