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SLTS259B – FEBRUARY 2006 – REVISED MAY 2007

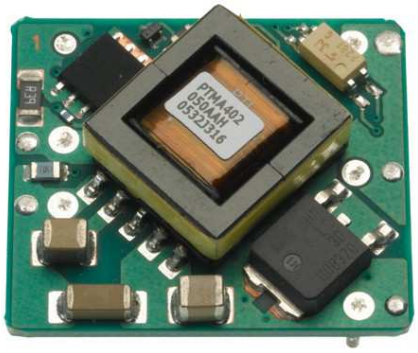
10-W, 36-V to 75-V INPUT, 1500-V ISOLATION, DC/DC CONVERTERS

FEATURES

- Input Voltage: 36 V to 75 V
- 10-W Total Output Power
- Output Voltages: 3.3 V, 5 V, and 12 V
- Output Voltage Trim ±10%
- Up To 87% Efficiency
- Overcurrent Protection
- Input Undervoltage Lockout
- Output Overvoltage Protection
- Positive or Negative Logic Enable Control Option
- Synchronization Option
- Space-Saving, Industry Standard Footprint (1.1 in x 1.0 in) / (27.94 mm × 24.38 mm)
- Industry Standard Pinout
- Surface Mount Package
- 1500-Vdc Isolation
- Agency Approvals: UL/IEC/CSA-C22.2 60950-1

APPLICATIONS

- Intermediate Bus Architectures
- Telecom, High-End Computing Platforms
- Power Over Ethernet Applications
- Multi-Rail Power Systems



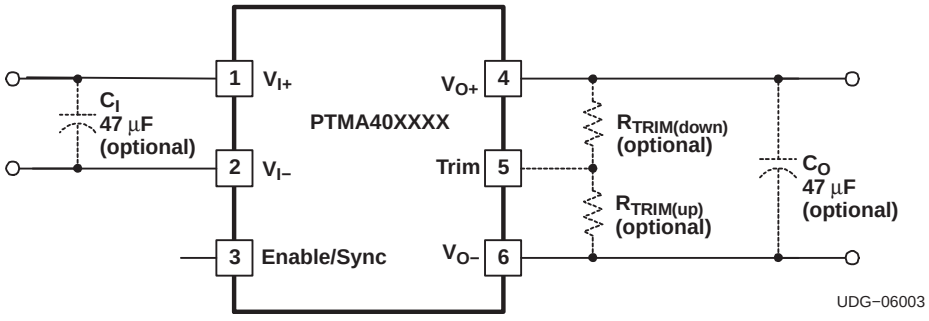
DESCRIPTION

The PTMA40XX is a series of 10-W rated isolated dc/dc converters, designed to operate from a standard -48-V telecom central office supply. Housed in an industry standard *1.1 in × 1.0 in (27.94 mm × 24.38 mm)* package, this series of isolated modules is set to one of the common intermediate bus voltages of 3.3 V, 5 V, or 12 V.

The PTMA40XX series includes many features expected of high-performance dc/dc converter modules. Operational features include an input undervoltage lockout (UVLO) and a dual-logic output enable control or synchronization option. Overcurrent protection ensures survival against load faults.

Typical applications include distributed power architectures in both telecom and computing environments, power over ethernet, and particularly complex digital systems requiring multiple power supply rails.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

PART NUMBERING SCHEME

	Input Voltage	Output Current	Output Voltage	Enable	Electrical Options		Pin Style	Shipping Package
PTMA	**4**	**02**	**050**	**P**	**2**	**A**	**D**	**T**
	4 = 48 V	01 = 1 A	033 = 3.3 V	A = None	1 = None		D = Through-hole, Pb-free	Blank = Tray
		02 = 2 A	050 = 5.0 V	N = Negative	2 = V_O Adjust		S = SMD, SnPb solder ball	T = Tape and Reel
		03 = 3 A	120 = 12.0 V	P = Positive	3 = V_O Adjust & Syncronization		Z = SMD, SnAgCu solder ball	

ABSOLUTE MAXIMUM RATINGS

				UNIT
V_I	Input Voltage	Continuous		75 V
		Surge, 1 s max		100 V (1)
T_A	Operating temperature range	Over V_I range		–40°C to 85°C
T_{WAVE}	Wave solder temperature	Surface temperature of module or pins **(20 seconds)**	AD suffix	260°C (2)
T_{REFLOW}	Solder reflow temperature	Surface temperature of module or pins **(20 seconds)**	AS suffix	235°C (2)
			AZ suffix	260°C (2)
T_{STG}	Storage temperature			–55°C to 125°C
P_O	Output Power			10 W

(1) The converter's internal protection circuitry may cause the output to turn off when the applied input voltage is greater than 75 V.
(2) During solder reflow of SMD package version, do not elevate the module PCB, pins, or internal component temperatures beyond this peak temperature.

PACKAGE SPECIFICATIONS

			UNITS
Weight			6.5 grams
Flammability	Meets UL94V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 Sine, mounted	Horizontal T/H (Suffix AD)	500 G (1)
		Horizontal SMD (Suffix AS & AZ)	500 G (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz, PCB mounted	Horizontal T/H (Suffix AD)	20 G (1)
		Horizontal SMD (Suffix AS & AZ)	10 G (1)
Reliability	Telcordia SR-332 50% stress, T_A = 40°C, ground benign	MTBF	7.3 10^6 Hr

(1) Qualification limit.

PTMA403033 ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_I = 48 V, V_O = 3.3 V, C_I = 0 µF, C_O = 0 µF, and I_O = $I_O$max (Unless otherwise stated)

PARAMETER		TEST CONDITIONS		PTMA403033			UNIT
				MIN	TYP	MAX	
P_O	Output power	Over V_I range				10	W
I_O	Output current	Over V_I range		0.1 (1)		3 (2)	A
I_{LIM}	Current Limit Threshold	Shutdown, followed by autorecovery			4.25		A
V_I	Input voltage range	Over I_O range		36	48	75	V
V_O	Set-point voltage tolerance				±2 (3)		%V_O
	Temperature variation	-40°C ≤ T_A ≤ 85°C			±1		%V_O
	Line regulation	Over V_I range			±3		mV
	Load regulation	Over I_O range			±10		mV
	Total output voltage variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C			3	5 (3)	%V_O
	Trim adjust range	Over V_I range		3.0		3.6	V
η	Efficiency	P_O = $P_O$max			82%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth			65		mV_{pp}
	Transient response	0.1 A/µs load step, 50% to 100% $I_O$max	Recovery time		750		µs
			V_O over/undershoot		±150		mV
	Output enable input (pin 3)	Referenced to V_I–	Input high voltage (V_{IH})	4.5		Open (4)	V
			Input low voltage (V_{IL})	–0.2		0.8	
			Input low current (I_{IL})		1		mA
	Standby input current	Pin 3 open			8		mA
UVLO	Undervoltage lockout			32		34	V
OVP	Output Overvoltage Protection			3.7		5.4	V
f_S	Switching frequency	Over V_I and I_O ranges (non-Sync option)		250	300	350	kHz
SYNC	Sync switching frequency	Free-running		180	215 (5)	250	kHz
		Synchronization range		250 (5)		350 (5)	
	high-level input voltage			3.5		6	V
	low-level input voltage			–0.3		0.5	V
	clock duty cycle			25		75	%
C_I	External input capacitance			0	47		µF
C_O	External output capacitance			0	47 (6)	1000	µF
V_{ISO}	Isolation voltage	Primary-Secondary		1,500			Vdc
C_{ISO}	Isolation capacitance				1,100		pF
R_{ISO}	Isolation resistance			10			MΩ

(1) The converter requires a minimum load current for proper operation. However, the converter is not damaged when operated under a no-load condition.
(2) See temperature derating curves for safe operating area (SOA), to determine output current derating at elevated ambient temperatures.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{TRIM}. The stated limit is unconditionally met if R_{TRIM} has a tolerance of ≤1%, with ≤100 ppm/°C temperature stability.
(4) The Enable input (pin 3) has an internal pullup resistor. Do not place an external pullup resistor on this input pin. If the enable feature is not used, for a positive enable device this input should be left open circuit and a negative enable device should be permanently connected to V_I– (pin 2). A discrete MOSFET or bipolar transistor is recommended for the enable control. The open-circuit voltage is typically less than 5 V. See the *Application Information* for a more detailed description.
(5) A device with the synchronization option has a reduced switching frequency of 215 kHz typical. The synchronization frequency can only be adjusted to a higher frequency, up to 350 kHz maximum.
(6) An output capacitor is not required for proper operation. However, additional capacitance at the load improves the transient response.

PTMA402050 ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_I = 48 V, V_O = 5 V, C_I = 0 µF, C_O = 0 µF, and I_O = $I_O$max (Unless otherwise stated)

PARAMETER		TEST CONDITIONS		PTMA402050			UNIT
				MIN	TYP	MAX	
P_O	Output power	Over V_I range				10	W
I_O	Output current	Over V_I range		0.1 (1)		2 (2)	A
I_{LIM}	Current Limit Threshold	Shutdown, followed by autorecovery			3		A
V_I	Input voltage range	Over I_O range		36	48	75	V
V_O	Set-point voltage tolerance				±2 (3)		%V_O
	Temperature variation	-40°C ≤ T_A ≤ 85°C			±1		%V_O
	Line regulation	Over V_I range			5		mV
	Load regulation	Over I_O range			10		mV
	Total output voltage variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C			3	5 (3)	%V_O
	Trim adjust range	Over V_I range		4.5		5.5	V
η	Efficiency	P_O = $P_O$max			85%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth			55		mV_{pp}
	Transient response	0.1 A/µs load step, 50% to 100% $I_O$max	Recovery time		250		µs
			V_O over/undershoot		±150		mV
	Output enable input (pin 3)	Referenced to V_I–	Input high voltage (V_{IH})	4.5		Open (4)	V
			Input low voltage (V_{IL})	–0.2		0.8	
			Input low current (I_{IL})		1		mA
	Standby input current	Pin 3 open			8		mA
UVLO	Undervoltage lockout			32		34	V
OVP	Output Overvoltage Protection			5.6		7.9	V
f_S	Switching frequency	Over V_I range		250	300	350	kHz
SYNC	Sync switching frequency	Free-running		180	215 (5)	250	kHz
		Synchronization range		250 (5)		350 (5)	
	high-level input voltage			3.5		6	V
	low-level input voltage			–0.3		0.5	V
	clock duty cycle			25		75	%
C_I	External input capacitance			0	47		µF
C_O	External output capacitance			0	47 (6)	1000	µF
V_{ISO}	Isolation voltage	Primary-Secondary		1,500			Vdc
C_{ISO}	Isolation capacitance				1,100		pF
R_{ISO}	Isolation resistance			10			MΩ

(1) The converter requires a minimum load current for proper operation. However, the converter is not damaged when operated under a no-load condition.
(2) See temperature derating curves for safe operating area (SOA), to determine output current derating at elevated ambient temperatures.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{TRIM}. The stated limit is unconditionally met if R_{TRIM} has a tolerance of ≤1%, with ≤100 ppm/°C temperature stability.
(4) The Enable input (pin 3) has an internal pullup resistor. Do not place an external pullup resistor on this input pin. If the enable feature is not used, for a positive enable device this input should be left open circuit and a negative enable device should be permanently connected to V_I– (pin 2). A discrete MOSFET or bipolar transistor is recommended for the enable control. The open-circuit voltage is typically less than 5 V. See the *Application Information* for a more detailed description.
(5) A device with the synchronization option has a reduced switching frequency of 215 kHz typical. The synchronization frequency can only be adjusted to a higher frequency, up to 350 kHz maximum.
(6) An output capacitor is not required for proper operation. However, additional capacitance at the load will improve the transient response.

PTMA401120 ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_I = 48 V, V_O = 12 V, C_I = 0 µF, C_O = 0 µF, and I_O = $I_O$max (Unless otherwise stated)

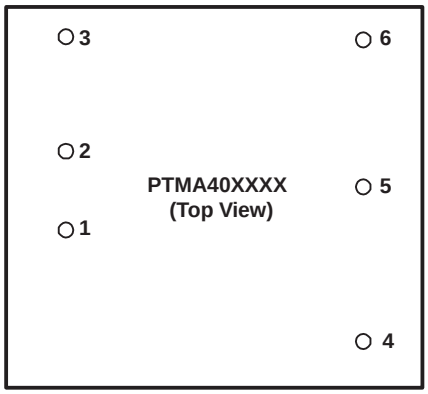
PARAMETER		TEST CONDITIONS		PTMA401120			UNIT
				MIN	TYP	MAX	
P_O	Output power	Over V_I range				12	W
I_O	Output current	Over V_I range		0.1 (1)		1 (2)	A
I_{LIM}	Current Limit Threshold	Shutdown, followed by autorecovery			1.5		A
V_I	Input voltage range	Over I_O range		36	48	75	V
V_O	Set-point voltage tolerance				±2 (3)		%V_O
	Temperature variation	-40°C ≤ T_A ≤ 85°C			±1		%V_O
	Line regulation	Over V_I range			10		mV
	Load regulation	Over I_O range			3		mV
	Total output voltage variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C			3	5 (3)	%V_O
	Trim adjust range	Over V_I range		10.8		13.2	V
η	Efficiency	P_O = $P_O$max			87%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth			85		mV_{pp}
	Transient Response	0.1 A/µs load step, 50% to 100% $I_O$max	Recovery time		400		µs
			V_O over/undershoot		±250		mV
	Output enable input (pin 3)	Referenced to V_I–	Input high voltage (V_{IH})	4.5		Open (4)	V
			Input low voltage (V_{IL})	–0.2		0.8	
			Input low current (I_{IL})		1		mA
	Standby input current	Pin 3 open			8		mA
UVLO	Undervoltage lockout			32		34	V
OVP	Output Overvoltage Protection			13.5		17.5	V
f_S	Switching frequency	Over V_I range		250	300	350	kHz
SYNC	Sync switching frequency	Free-running		180	215 (5)	250	kHz
		Synchronization range		250 (5)		350 (5)	
	high-level input voltage			3.5		6	V
	low-level input voltage			–0.3		0.5	V
	clock duty cycle			25		75	%
C_I	External input capacitance			0	47		µF
C_O	External output capacitance			0	47(6)	220	µF
V_{ISO}	Isolation voltage	Primary-Secondary		1,500			Vdc
C_{ISO}	Isolation capacitance				1,100		pF
R_{ISO}	Isolation resistance			10			MΩ

(1) The converter requires a minimum load current for proper operation. The converter is not damaged when operated under a no-load condition.
(2) See temperature derating curves for safe operating area (SOA), to determine output current derating at elevated ambient temperatures.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{TRIM}. The stated limit is unconditionally met if R_{TRIM} has a tolerance of 1%, with 100 ppm/°C temperature stability.
(4) The Enable input (pin 3) has an internal pullup resistor. Do not place an external pullup resistor on this input pin. If the enable feature is not used, for a positive enable device this input should be left open circuit and a negative enable device should be permanently connected to V_I– (pin 2). A discrete MOSFET or bipolar transistor is recommended for the enable control. The open-circuit voltage is typically less than 5 V. See the *Application Information* for a more detailed description.
(5) A device with the synchronization option has a reduced switching frequency of 215 kHz typical. The synchronization frequency can only be adjusted to a higher frequency, up to 350 kHz maximum.
(6) An output capacitor is not required for proper operation. However, additional capacitance at the load will improve the transient response.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
Enable/Sync (1)	3	The Enable input is an open-base logic input that is referenced to V_I–. Two ON/OFF enable options are available, positve logic and negative logic. Positive logic devices are enabled by applying a logic high voltage (Open) and are disabled by applying a logic low voltage (V_I–). Negative logic devices are enabled by applying a logic low voltage (V_I–) and are disabled by applying a logic high voltage (Open). See the Application Information section for more detailed information. This pin also has the option of a synchronization input. A module that has the synchronization option does not have ON/OFF enable control. A 5-V logic signal greater than the free-running frequency but ≤ 350 kHz is required for synchronization control. See the Application Information section for more detailed information.
V_I–(1)	2	The negative input supply for the module, and the 0-V reference for the Enable/Sync inputs. When powering the module from a positive source, this input is connected to the input source return.
V_I+ (1)	1	The positive input for the module with respect to V_I–. When powering the module from a negative input voltage, this input is connected to the input source ground.
V_O+	4	This is the positive power output with respect to V_O–. It is dc isolated from the input power pins.
Trim	5	This pin allows the output voltage set point of the module to be increased or decreased up to ± 10 %. Connecting a resistor between this terminal and V_O+ decreases the output voltage set point. Connecting a resistor between this terminal and V_O– increases the output voltage set point. A 0.05-W rated resistor may be used, with tolerance and temperature stability of 1% and 100 ppm/°C, respectively. If left open circuit, the converter output voltage defaults to its nominal value. The specification table gives the standard resistor values for the most common output voltages.
V_O–	6	This is the output power return for the V_O+ bus. This terminal should be connected to the common of the load circuit.

(1) These functions indicate signals electrically common with the input.



TYPICAL CHARACTERISTICS

PTMA403033 Characteristic Data (V_O = 3.3 V) (1)(2)

EFFICIENCY
vs OUTPUT CURRENT

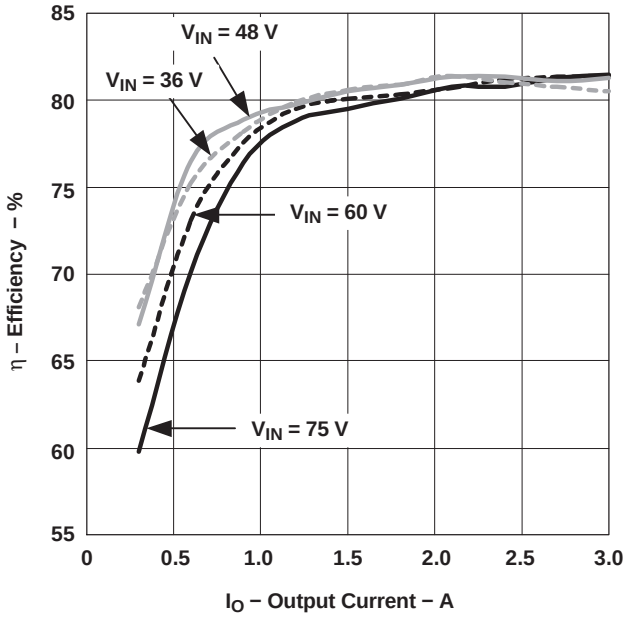


Figure 1.

POWER DISSIPATION
vs OUTPUT CURRENT

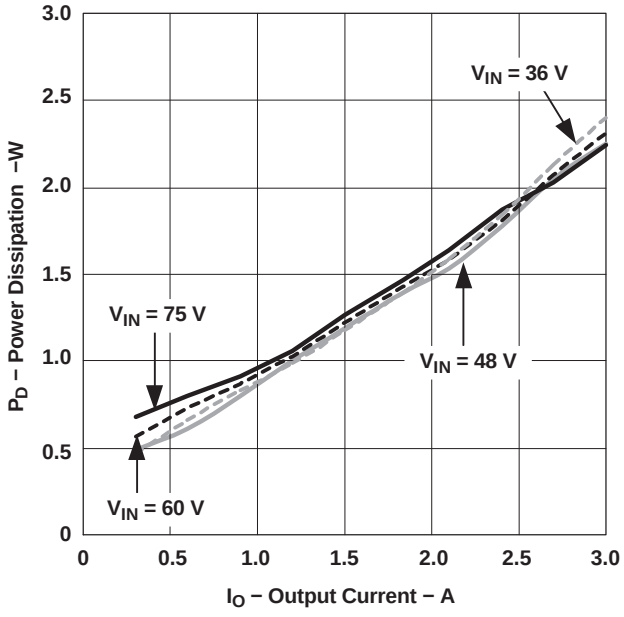


Figure 2.

OUTPUT VOLTAGE RIPPLE
vs OUTPUT CURRENT

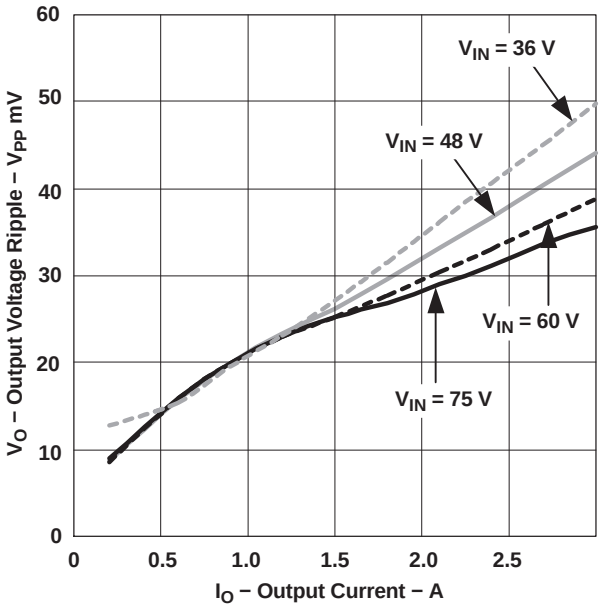


Figure 3.

TEMPERATURE DERATING
vs OUTPUT CURRENT

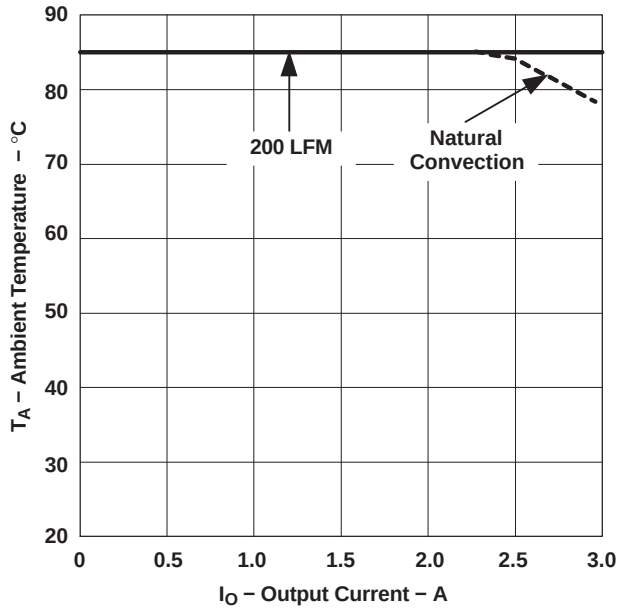


Figure 4.

(1) All data listed in Figure 1, Figure 2, and Figure 3 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

(2) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. Derating limits apply to modules soldered directly to a 100–mm × 100–mm, double-sided PCB with 2 oz. copper. For surface mount packages, multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 4.

TYPICAL CHARACTERISTICS (continued)

PTMA402050 Characteristic Data (V_O = 5 V) (3)(4)

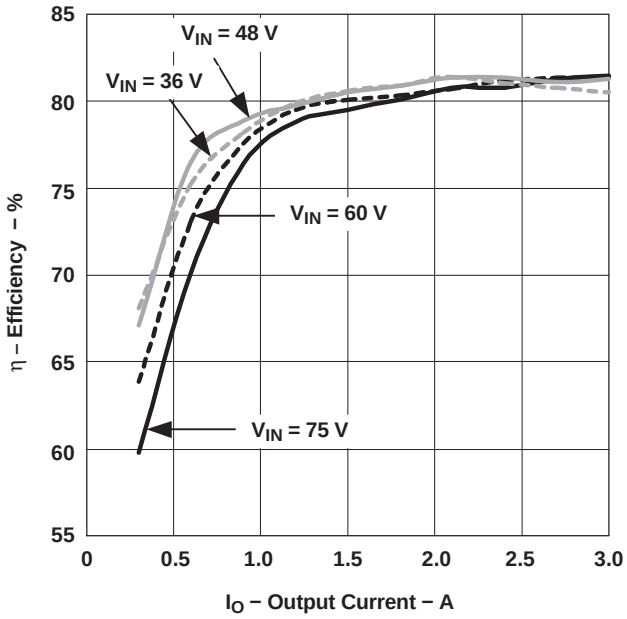


Figure 5.

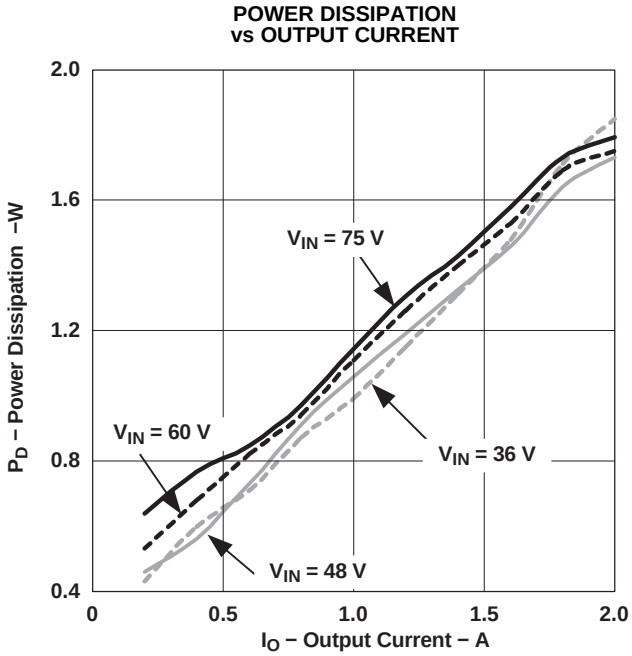


Figure 6.

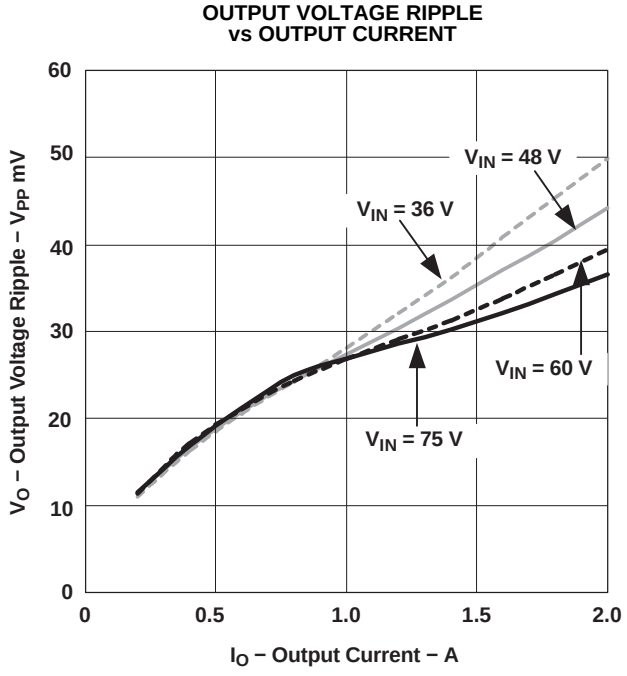


Figure 7.

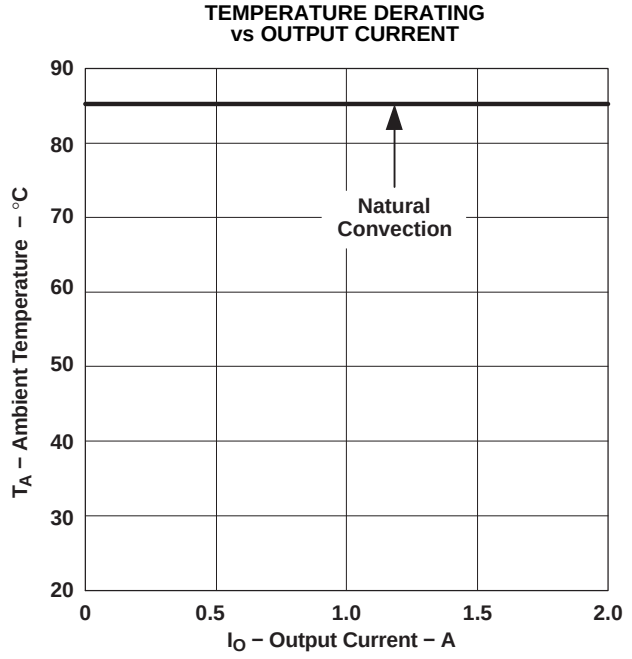


Figure 8.

(3) All data listed in Figure 5, Figure 7, and Figure 6 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

(4) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. Derating limits apply to modules soldered directly to a 100–mm × 100–mm, double-sided PCB with 2 oz. copper. For surface mount packages, multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 8.

TYPICAL CHARACTERISTICS (continued)

PTMA401120 Characteristic Data (V_O = 12 V) (5)(6)

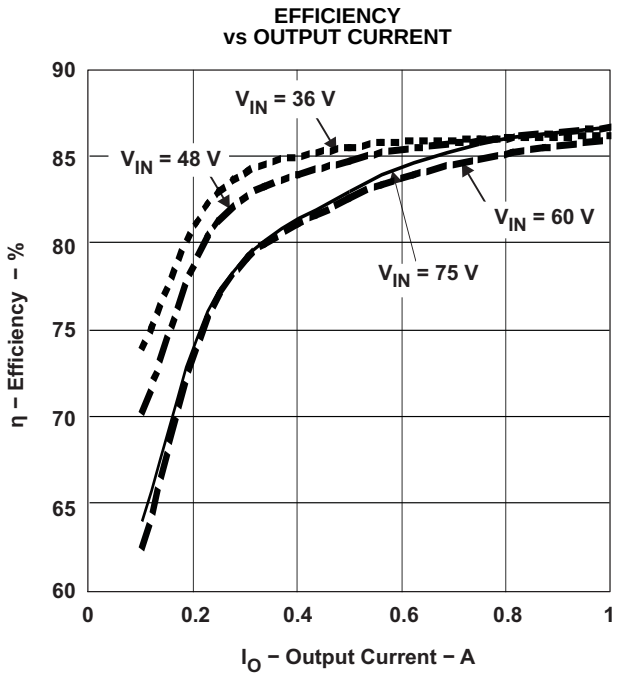


Figure 9.

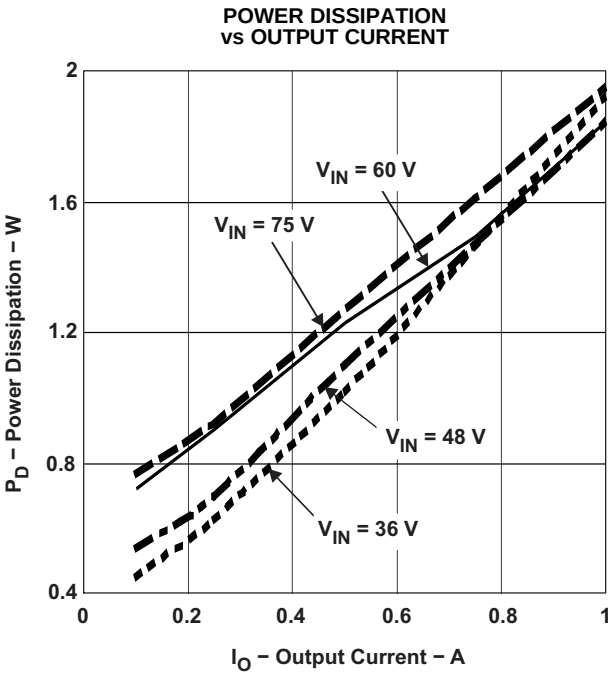


Figure 10.

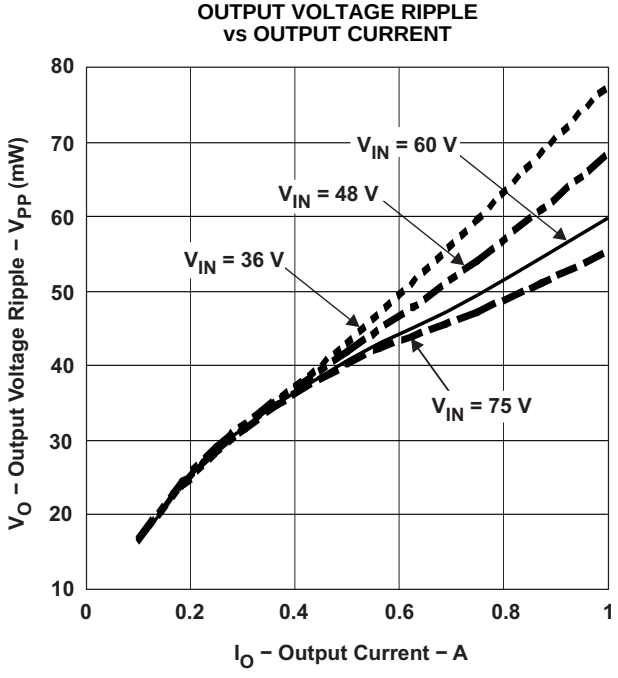


Figure 11.

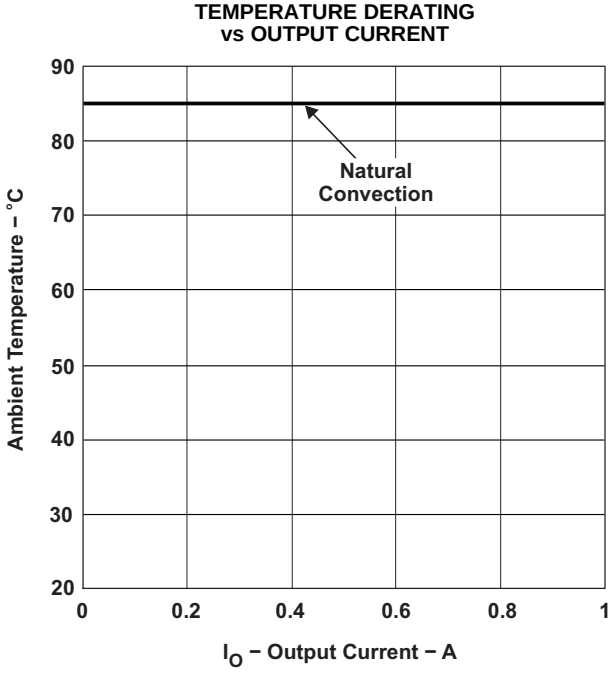


Figure 12.

(5) All data listed in Figure 9, Figure 10, and Figure 11 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

(6) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. Derating limits apply to modules soldered directly to a 100–mm × 100–mm, double-sided PCB with 2 oz. copper. For surface mount packages, multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 12.

APPLICATION INFORMATION

Operating Features and System Considerations for the PTMA40XX DC/DC Converters

Primary-Secondary Isolation

These converters incorporate electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are tested to a withstand voltage of 1500 Vdc. This complies with UL/cUL 60950 and EN 60950 and the requirements for functional isolation. It allows the converter to be configured for either a positive or negative input voltage source. The data sheet *Terminal Functions* table provides guidance as to the correct reference that must be used for the external control signals.

Undervoltage Lockout

The undervoltage lockout (UVLO) is designed to prevent the operation of the converter until the input voltage is close to the minimum operating voltage. The converter is held off when the input voltage is below the UVLO threshold, and turns on when the input voltage rises above the threshold. This prevents high start-up current during normal power up of the converter, and minimizes the current drain from the input source during low input voltage conditions. The converter meets full specifications when the minimum specified input voltage is reached. The UVLO circuitry also overrides the operation of the enable or synchronization controls. Only when the input voltage is above the UVLO threshold does this input become functional.

Output Overvoltage Clamp

The module is protected from an overvoltage on the output using an internal clamp. This protects against a break in the feedback path as well as a ground fault on the external Trim resistor, which would cause the output voltage to increase.

Overcurrent Protection

To protect against load faults, these converters incorporate output overcurrent protection. Applying a load to the output that exceeds the converter overcurrent threshold (see applicable specification) causes the output voltage to momentarily fold back, and then shut down. Following shutdown, the module periodically attempts to automatically recover by initiating a soft-start power up. This is often described as a *hiccup* mode of operation, whereby the module continues in the cycle of successive shutdown and power up until the load fault is removed. Once the fault is removed, the converter automatically recovers and returns to normal operation.

Soft-Start Power Up

When the converter is first powered, the internal soft-start circuit limits how fast the output voltage can rise. The soft-start circuit functions after a valid input source is applied and the output is enabled, after the converter output is enabled using the Enable input, or on a recovery from a load fault. The purpose of the soft-start feature is to limit the surge of current drawn from the input source when the converter begins to operate. By limiting the rate at which the output voltage rises, the magnitude of current required to charge up the load circuit capacitance is significantly reduced.

Figure 13 shows the power-up characteristic of a PTMA403033 converter. The output voltage is 3.3 V. The soft-start circuit causes a slow, soft rise of the output voltage. The output voltage will begin to rise after a time delay (typically 85 ms-100 ms) once a valid input voltage is applied. The output then progressively rises to the voltage set-point. The waveforms were recorded with a resistive load of 3 A.

APPLICATION INFORMATION (continued)

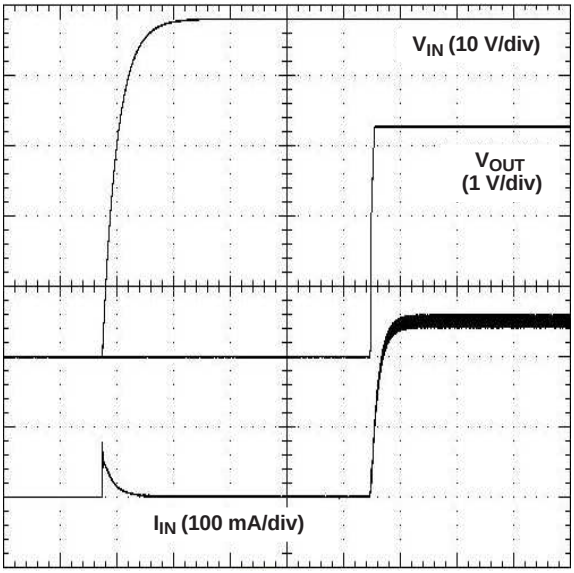


Figure 13. Power-up Waveforms

Output Voltage Trim Adjustment

An external resistor is required to increase or decrease the output voltage set point of the module by ± 10 %. The resistor, R_{TRIM}, must be connected between the TRIM pin (pin 5) and V_O+ (pin 4) to decrease the output voltage, or between the TRIM pin and V_O– (pin 6) to increase the output voltage. A 0.05-W rated resistor can be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor close to the converter and connect it using dedicated PCB traces (see Figure 14). Table 1 gives the nearest standard value of external resistor for the common voltages within each model's adjust range.

Table 1. Standard Values of R_{TRIM} for Common Output Voltages

PTMA403033			PTMA402050			PTMA401120		
V_O (required)	R_{TRIM} (kΩ)		V_O (required)	R_{TRIM} (kΩ)		V_O (required)	R_{TRIM} (kΩ)	
	down	up		down	up		down	up
3.0 V	118	—	4.5 V	18.7	—	10.8 V	64.9	—
3.1 V	187	—	4.6 V	24.9	—	11.0 V	80.6	—
3.2 V	392	—	4.7 V	35.7	—	11.2 V	105	—
3.3 V	open	open	4.8 V	57.6	—	11.4 V	143	—
3.4 V	—	249	4.9 V	121	—	11.6 V	221	—
3.5 V	—	124	5.0 V	open	open	11.8 V	464	—
3.6 V	—	82.5	5.1 V	—	124	12.0 V	open	open
—	—	—	5.2 V	—	61.9	12.2 V	—	118
—	—	—	5.3 V	—	40.2	12.4 V	—	57.6
—	—	—	5.4 V	—	29.4	12.6 V	—	36.5
—	—	—	5.5 V	—	23.2	12.8 V	—	26.1
—	—	—	—	—	—	13.0 V	—	19.6
—	—	—	—	—	—	13.2 V	—	15.8

For other output voltages, the value of the required trim resistor may be calculated using Equation 1 to adjust the voltage up or Equation 2 to adjust the voltage down.

$$R_{TRIM(up)} = \frac{R_O \times V_R}{(V_O - V_{SET})} - R_P\ (k\Omega) \quad (1)$$

$$R_{TRIM(dwn)} = \frac{R_O \times (V_O - V_R)}{(V_{SET} - V_O)} - R_P\ (k\Omega) \quad (2)$$

Table 2 gives the required R_{TRIM} equation constants for the converter model selected. To calculate the required value of R_{TRIM}, simply locate the applicable constants and substitute these into the formula along with the desired output voltage.

Table 2. Trim Adjust Equation Constants

Constants	PTMA403033	PTMA402050	PTMA401120
V_R (V)	1.24	2.50	2.50
R_O (Ω)	20	5.11	10
R_P (Ω)	1.0	2.05	5.11
V_{SET} (V)	3.3	5.0	12.0
V_O(V)	Desired Output Voltage	Desired Output Voltage	Desired Output Voltage

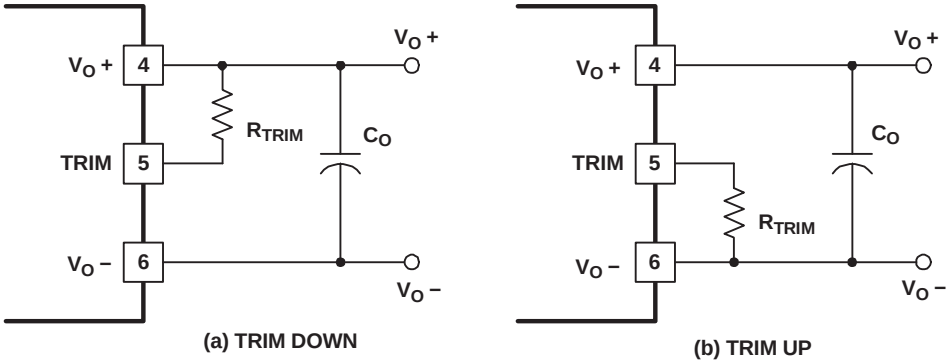


Figure 14. Output Voltage Adjustment

Thermal Considerations

Airflow may be necessary to ensure that the module can supply the desired load current in environments with elevated ambient temperatures. The required airflow rate is determined from the safe operating area (SOA). The SOA is the area beneath the applicable airflow rate curve on the graph of temperature derating vs output current. (See the Typical Characteristics.) Operating the converter within the SOA limits ensures that all the internal components are at or below their stated maximum operating temperatures.

On/Off Enable Controls

On/Off enable options include positive logic or negative logic. A positive logic device enables the module's output when a logic high voltage is present on the Enable pin (pin 3) and disables the output with a logic low voltage. A negative logic device disables the output when a logic high voltage is present on the Enable pin and enables the output during a logic low voltage. See the Electrical Characteristics table for logic high and logic low limits. The Enable pin is ideally controlled with an open-collector (or open-drain) discrete transistor. See Figure 15 below for a typical On/Off Enable control circuit. For automatic start-up, the Enable pin should be left open for a positive logic module and should be shorted to V_I– (pin 2) for a negative logic module. Both inputs are electrically referenced to V_I– on the primary (input) side of the converter. Do not place an external pull-up resistor on this input pin.

Enable Control Schematic

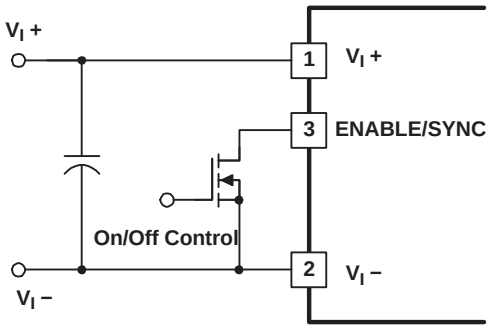


Figure 15. Typical On/Off Enable Control Circuit

On/Off Enable Turn-On Time

Once enabled, the converter executes a soft-start power up. The converter exibits a short delay of approximately 100 µs, measured from the transition of the enable signal to the instance the V_O Bus output begins to rise. The output is in regulation within 1.5 ms.

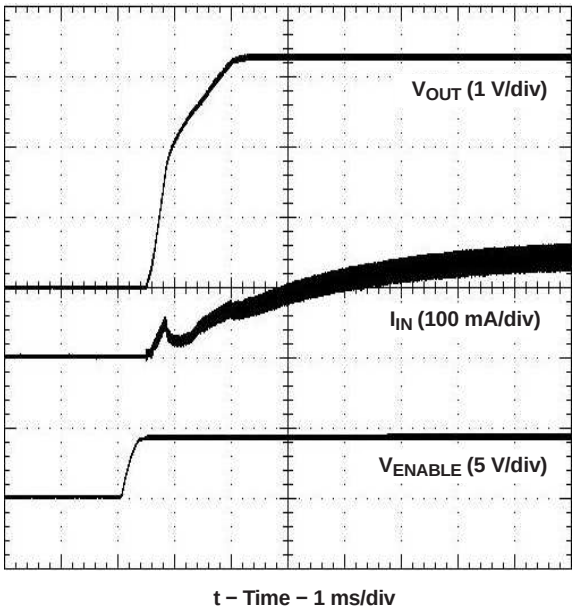


Figure 16. Output Enable Power-Up Characteristic

Synchronization

The Synchronization option allows multiple power modules to be synchronized to a common frequency. Driving the Sync pin (pin 3) with an external clock set to the desired frequency, synchronizes all connected modules to that frequency. Modules with the synchronization option have a reduced free-running switching frequency of 215 kHz typical. The synchronization frequency can only be adjusted to a higher frequency, up to 350 kHz. A 5-V logic signal is recommended for control. See Figure 17. See the Electrical Characteristics table for synchronization limits.

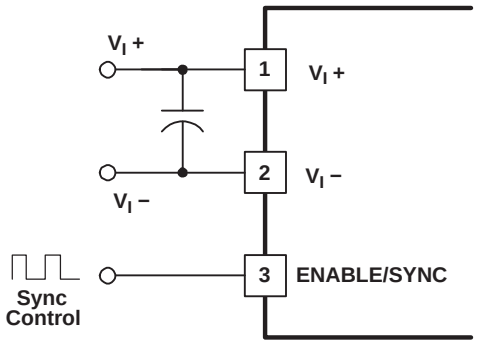
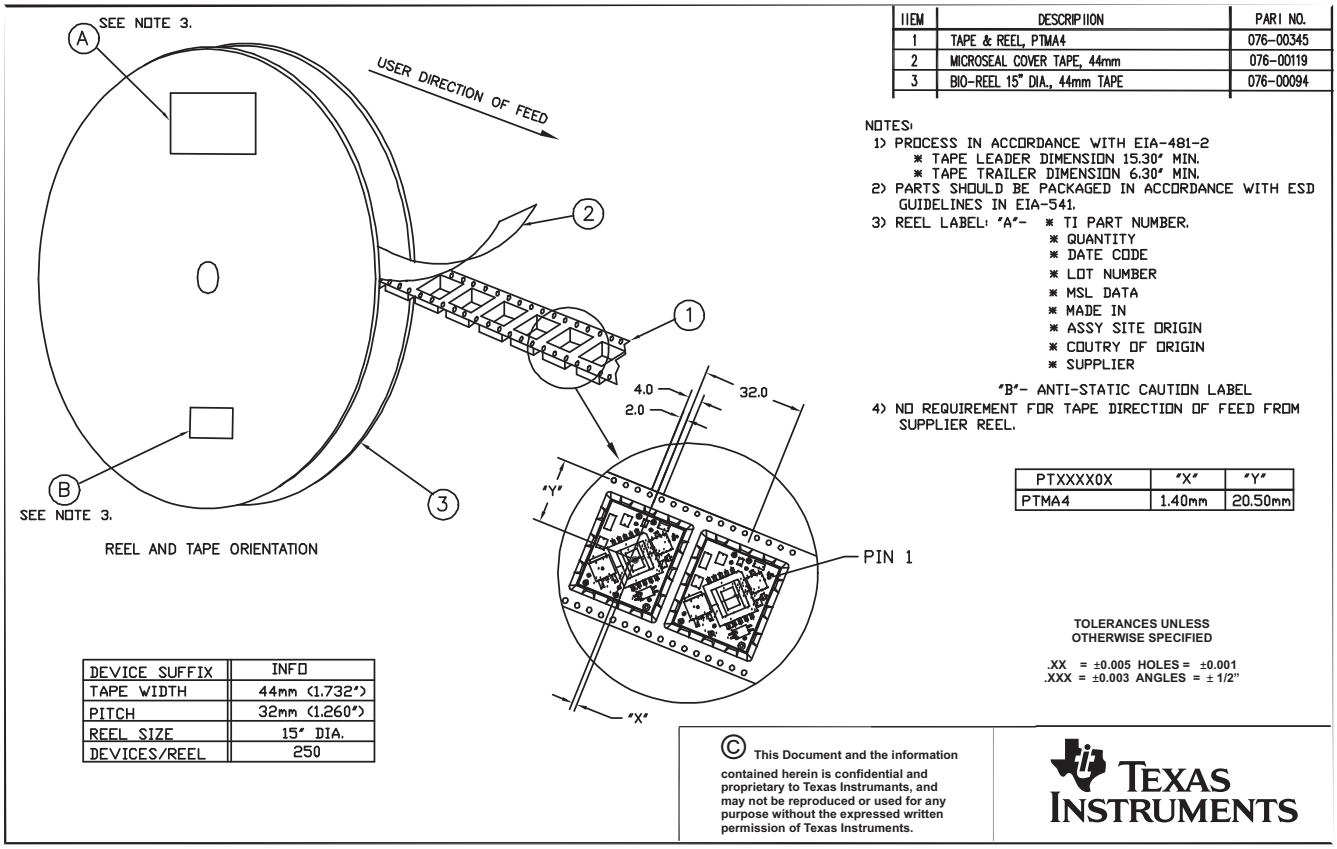


Figure 17. Synchronization Control

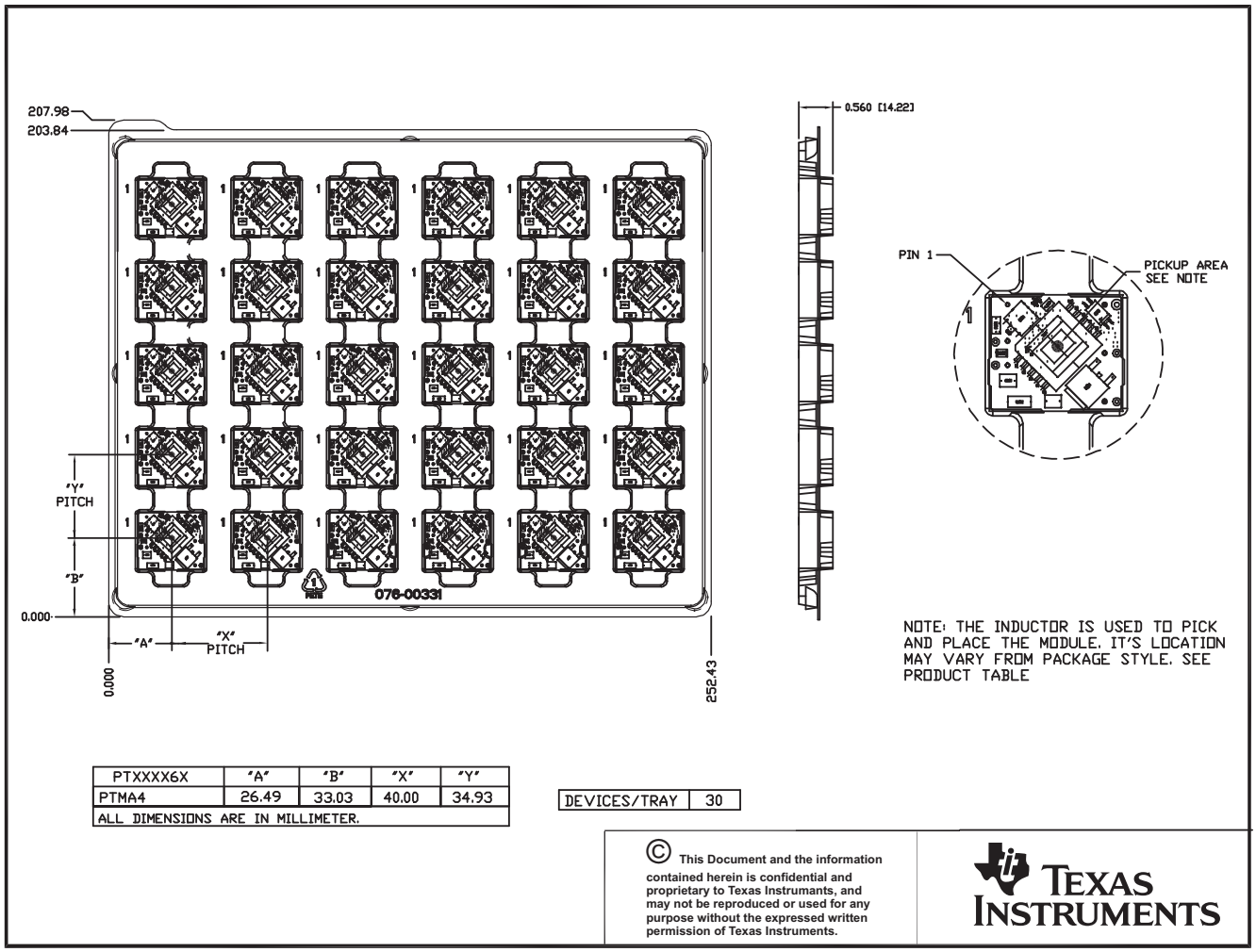
MECHANICALS

Tape and Reel



MECHANICALS (continued)

Tray



PTXXXX6X	"A"	"B"	"X"	"Y"
PTMA4	26.49	33.03	40.00	34.93
ALL DIMENSIONS ARE IN MILLIMETER.				

DEVICES/TRAY	30

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMA401120A1AD	NRND	Through-Hole Module	EEP	4	30	Pb-Free (RoHS)	SN	N / A for Pkg Type			
PTMA401120A1AZ	NRND	Surface Mount Module	BET	4	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR			
PTMA401120A2AD	NRND	Through-Hole Module	EEV	5	30	Pb-Free (RoHS)	SN	N / A for Pkg Type			
PTMA401120A2AS	NRND	Surface Mount Module	EEW	5	30	TBD	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS			
PTMA401120A2AZ	NRND	Surface Mount Module	BEW	5	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR			
PTMA401120A3AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type			
PTMA401120N1AD	NRND	Through-Hole Module	EEP	5	30	Pb-Free (RoHS)	SN	N / A for Pkg Type			
PTMA401120N1AZ	NRND	Surface Mount Module	BET	5	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR			
PTMA401120N2AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type			
PTMA401120N2AS	NRND	Surface Mount Module	EET	6	30	TBD	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS			
PTMA401120N2AZT	NRND	Surface Mount Module	BET	6	250	TBD	Call TI	Call TI			
PTMA401120P1AD	NRND	Through-Hole Module	EEP	5	30	Pb-Free (RoHS)	SN	N / A for Pkg Type			
PTMA401120P2AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type			
PTMA401120P2AZ	NRND	Surface Mount Module	BET	6	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR			
PTMA402050A1AD	NRND	Through-Hole Module	EEP	4	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA402050A1AZ	NRND	Surface Mount Module	BET	4	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTMA402050A2AD	NRND	Through-Hole Module	EEV	5	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMA402050A3AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA402050N2AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA402050N2AS	NRND	Surface Mount Module	EET	6	30	TBD	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		
PTMA402050N2AST	NRND	Surface Mount Module	EET	6	250	TBD	Call TI	Call TI	-40 to 85		
PTMA402050N2AZ	NRND	Surface Mount Module	BET	6	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTMA402050N2AZT	NRND	Surface Mount Module	BET	6	250	TBD	Call TI	Call TI	-40 to 85		
PTMA402050P2AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA402050P2AZ	NRND	Surface Mount Module	BET	6	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTMA403033A1AD	NRND	Through-Hole Module	EEP	4	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA403033A1AZ	NRND	Surface Mount Module	BET	4	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTMA403033A2AD	NRND	Through-Hole Module	EEV	5	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA403033A3AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA403033A3AZ	NRND	Surface Mount Module	BET	6	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTMA403033N1AD	NRND	Through-Hole Module	EEP	5	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA403033N1AZ	NRND	Surface Mount Module	BET	5	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTMA403033N1AZT	NRND	Surface Mount Module	BET	5	250	TBD	Call TI	Call TI	-40 to 85		
PTMA403033N2AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA403033N2AZ	ACTIVE	Surface Mount Module	BET	6	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMA403033N2AZT	ACTIVE	Surface Mount Module	BET	6	250	TBD	Call TI	Call TI	-40 to 85		Samples
PTMA403033P1AD	NRND	Through-Hole Module	EEP	5	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA403033P2AD	NRND	Through-Hole Module	EEP	6	30	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTMA403033P2AZ	NRND	Surface Mount Module	BET	6	30	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTMA403033P2AZT	NRND	Surface Mount Module	BET	6	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

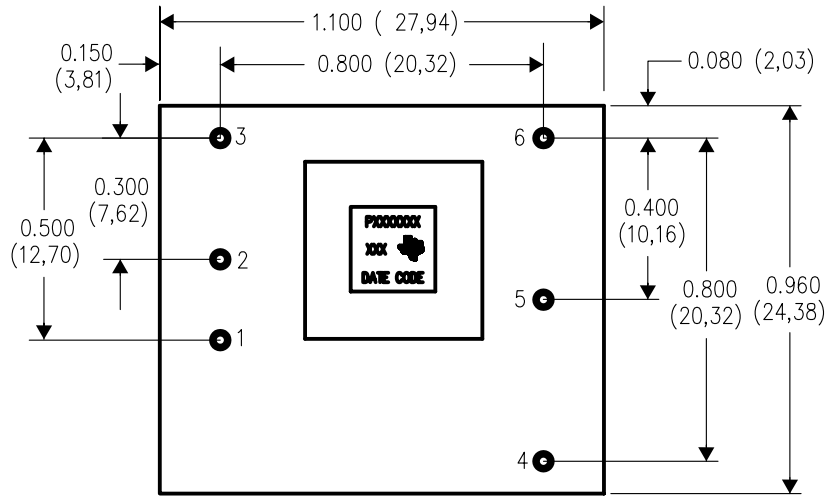
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

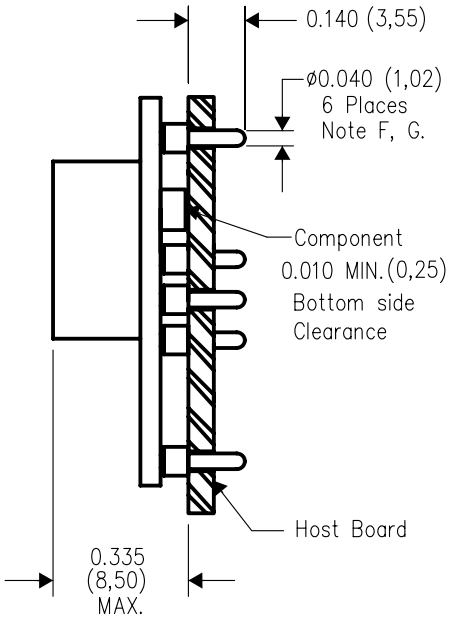
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

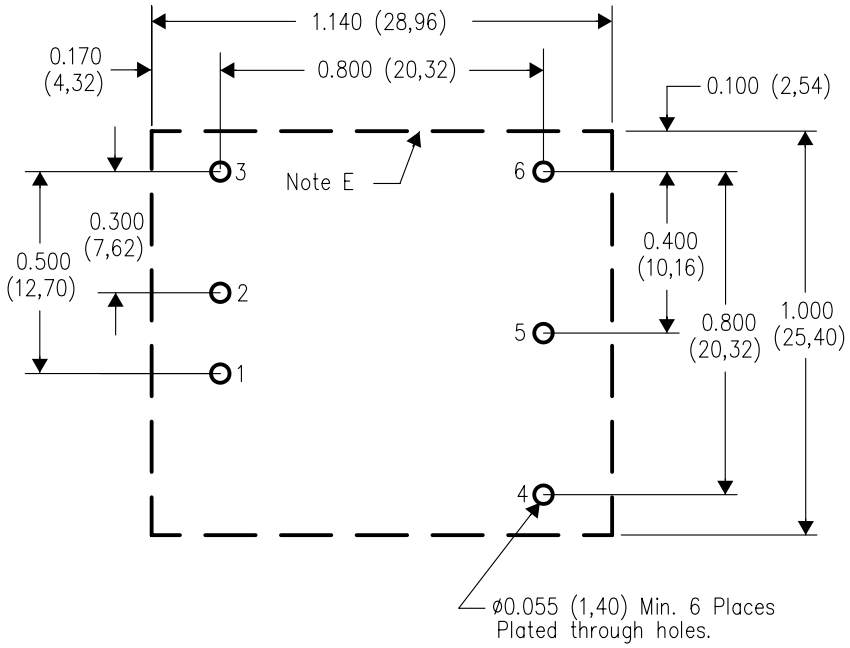
EEP (R–PDSS–T6) DOUBLE SIDED MODULE



TOP VIEW



SIDE VIEW

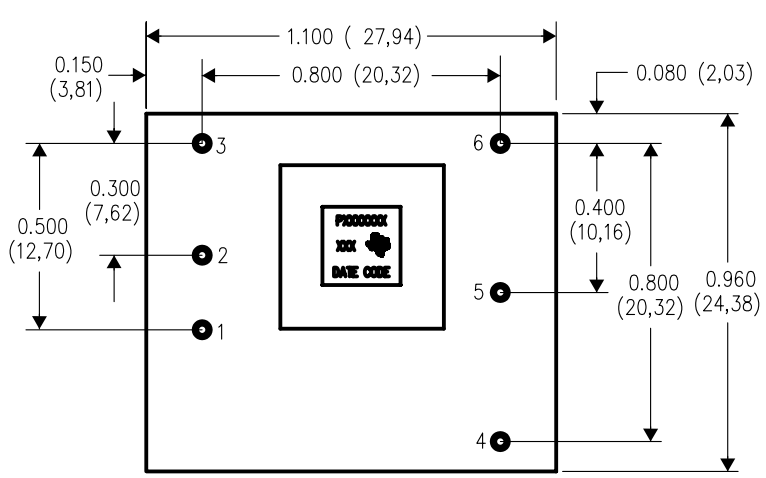


PC LAYOUT

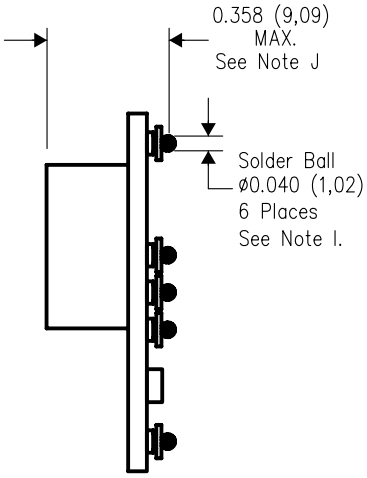
4207367–4/C 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

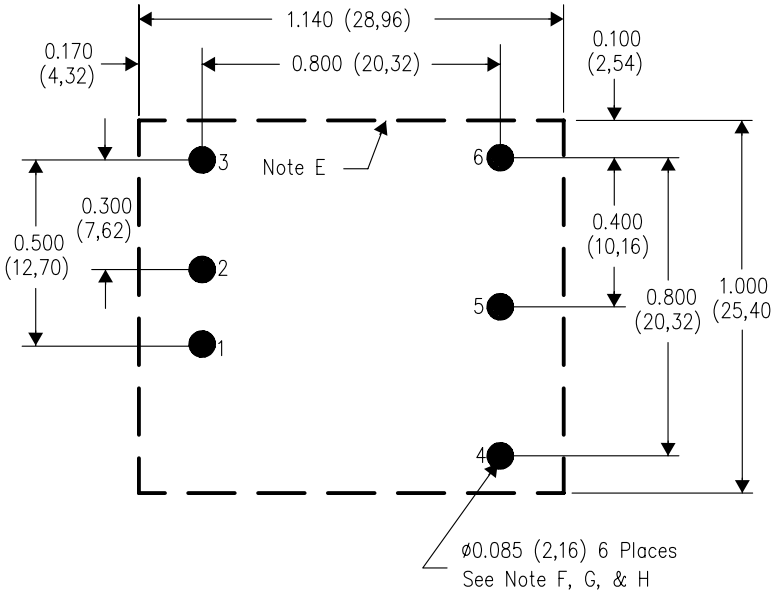
EET (R–PDSS–B6) DOUBLE SIDED MODULE



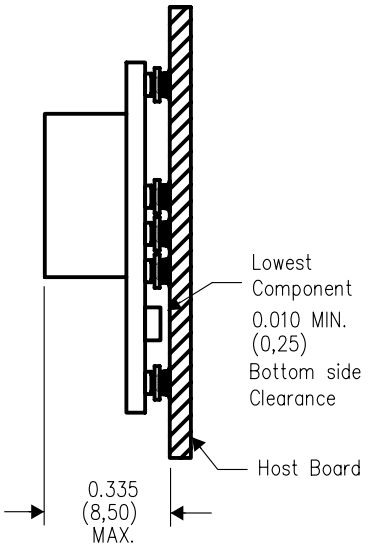
TOP VIEW



SIDE VIEW



PC LAYOUT



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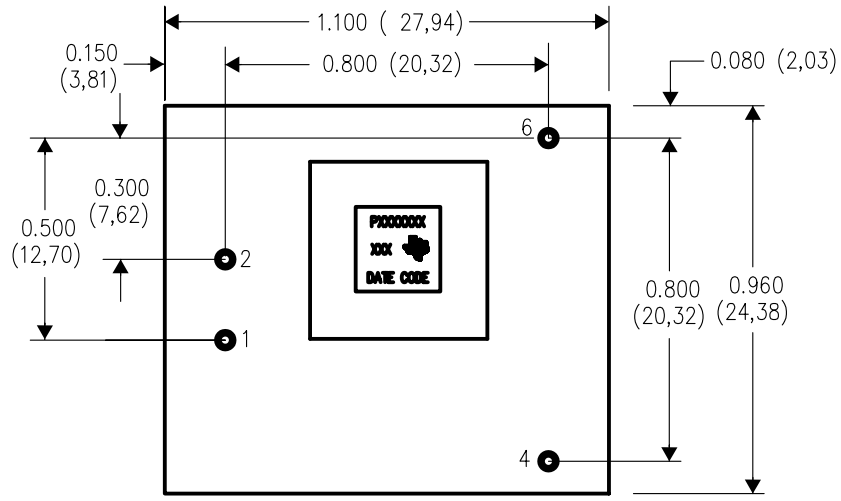
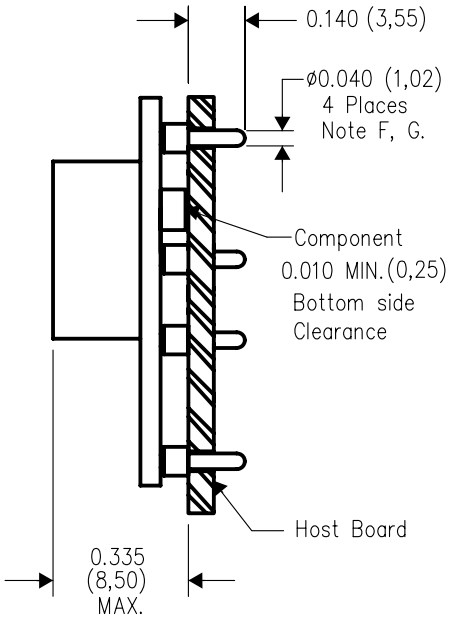
NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

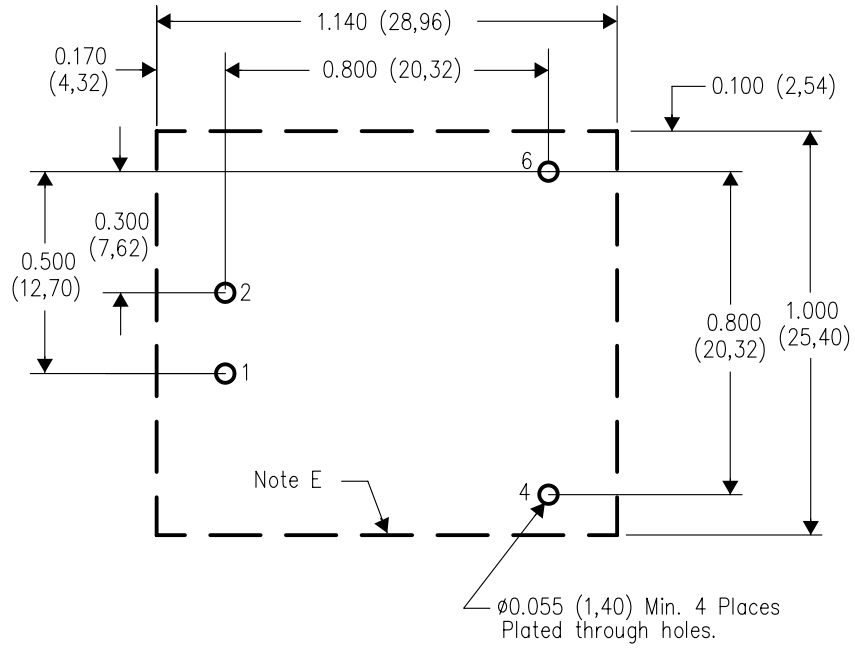
EEP (R–PDSS–T4) DOUBLE SIDED MODULE



TOP VIEW



SIDE VIEW

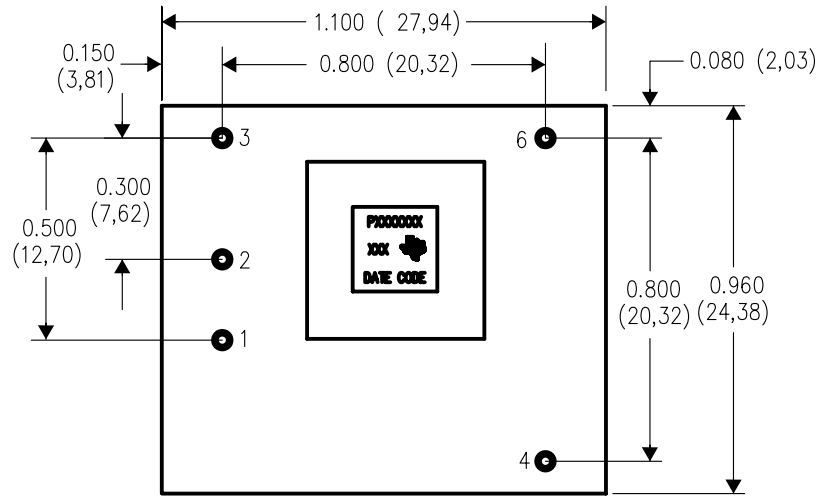


PC LAYOUT

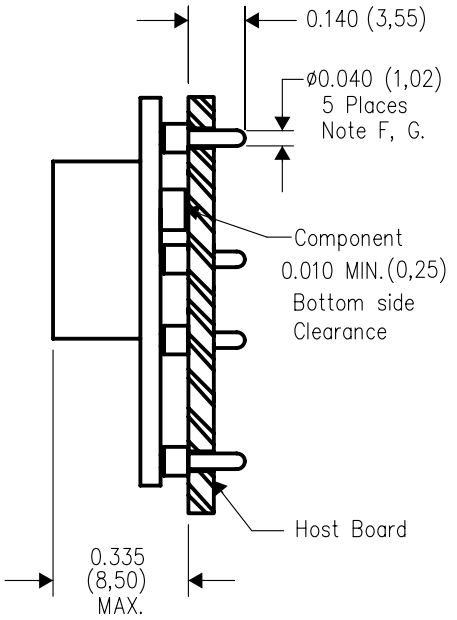
4207367–2/C 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

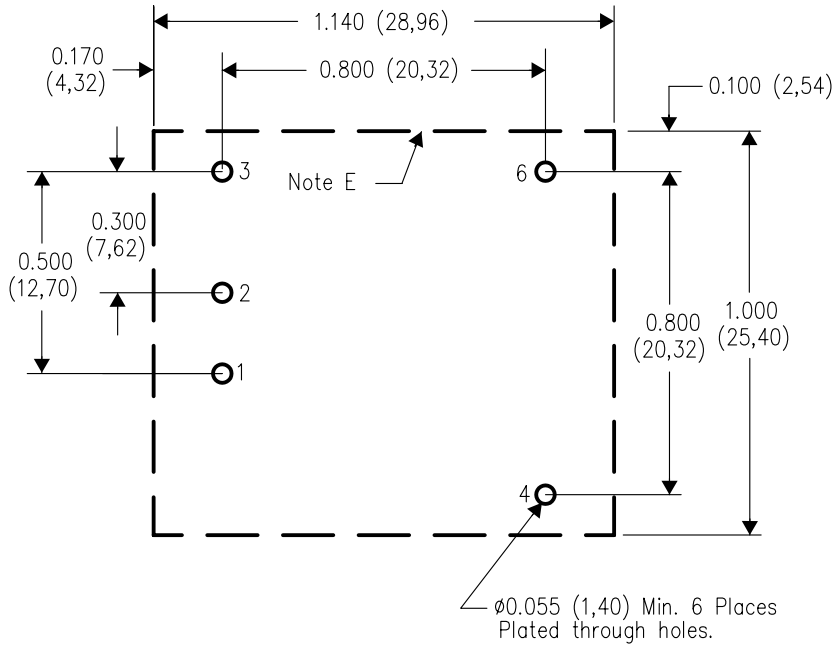
EEP (R–PDSS–T5) DOUBLE SIDED MODULE



TOP VIEW



SIDE VIEW

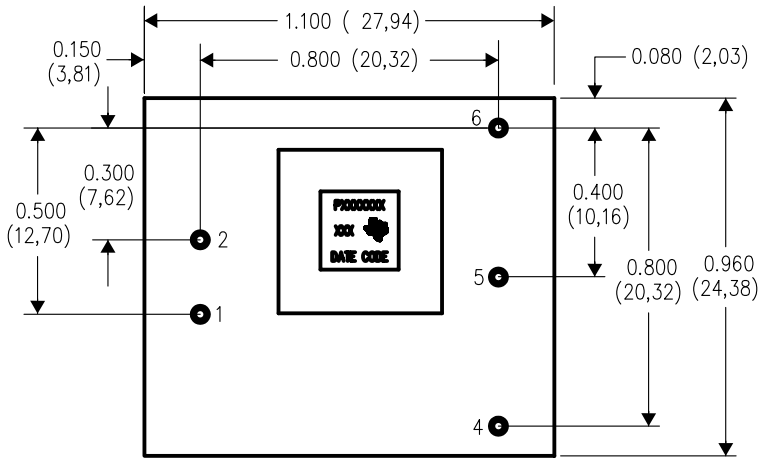


PC LAYOUT

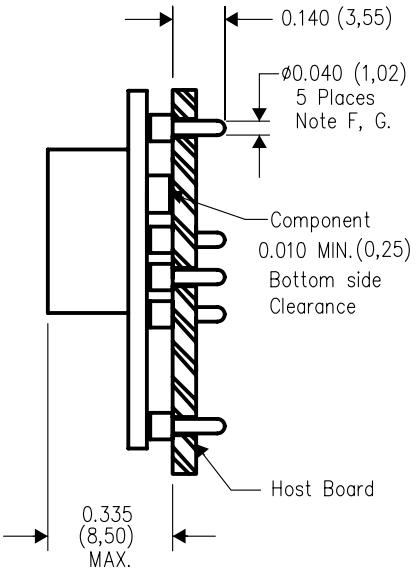
4207367–3/C 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

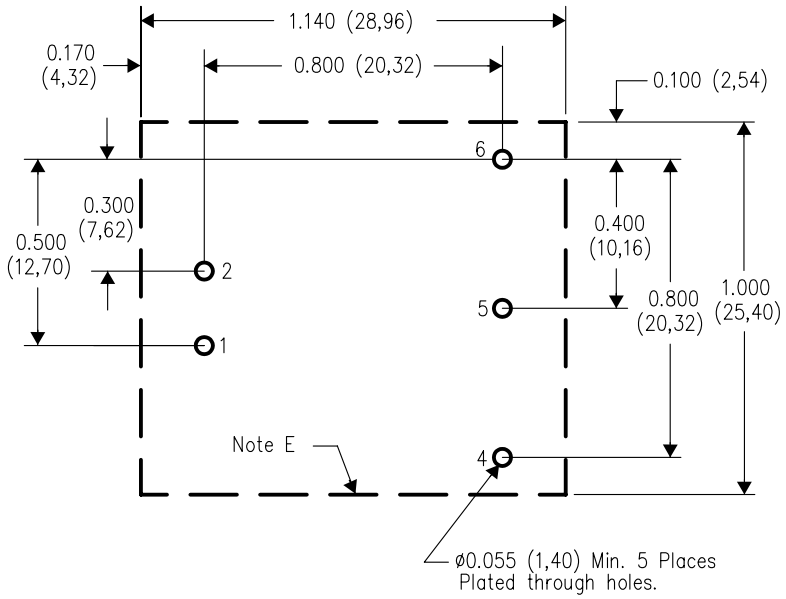
EEV (R–PDSS–T5) DOUBLE SIDED MODULE



TOP VIEW



SIDE VIEW

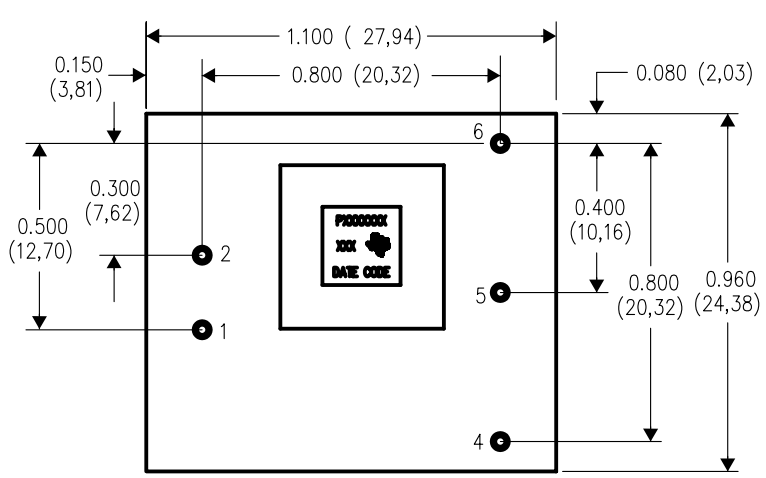


PC LAYOUT

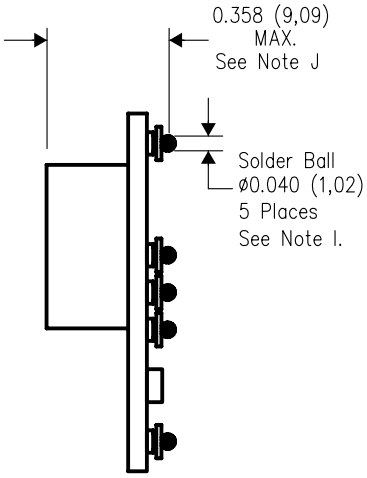
4207709/A 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

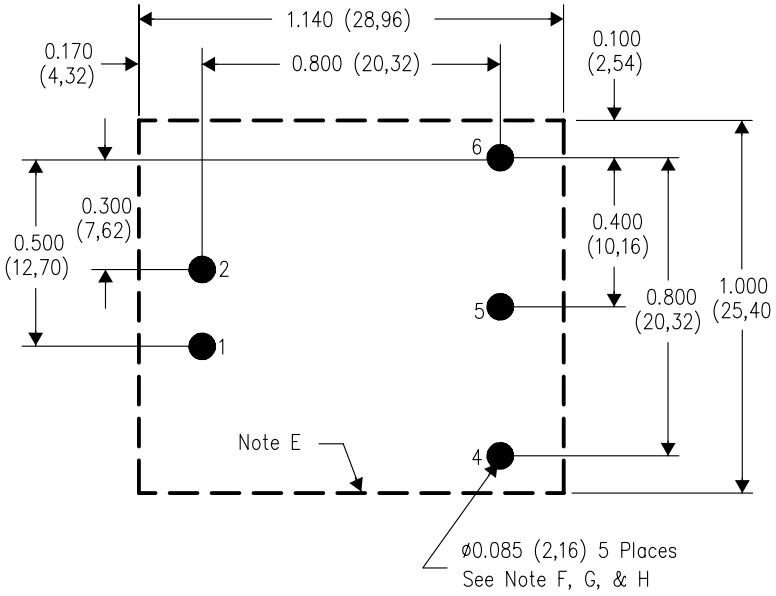
EEW (R–PDSS–B5) DOUBLE SIDED MODULE



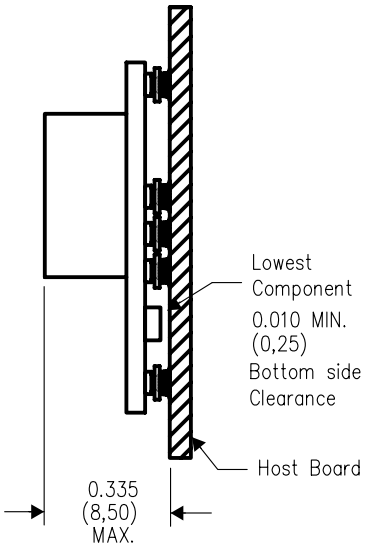
TOP VIEW



SIDE VIEW



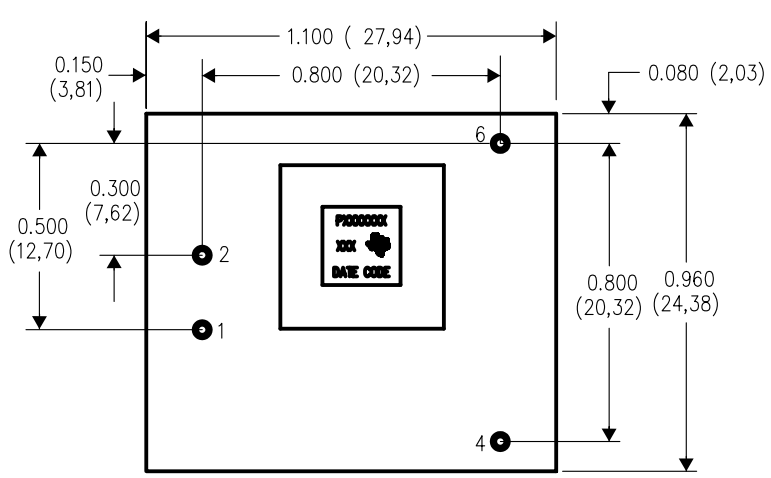
PC LAYOUT



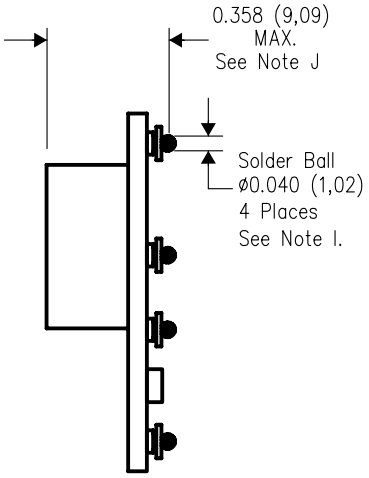
4207710/A 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

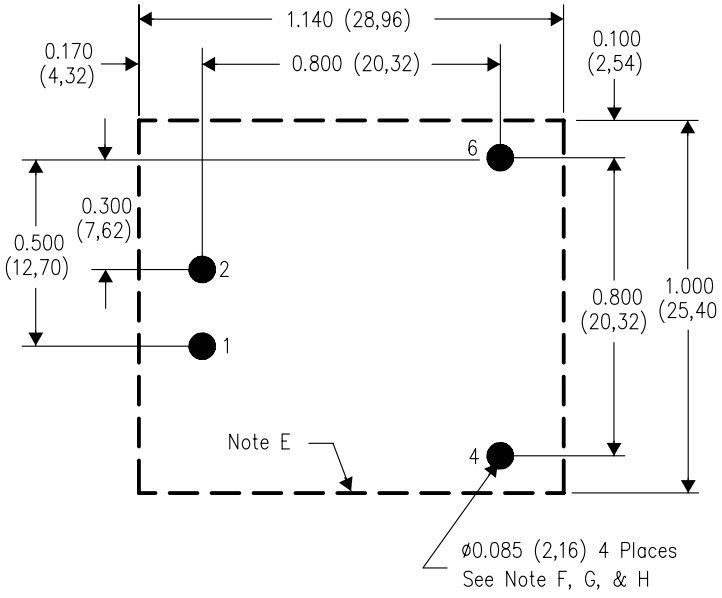
BET (R–PDSS–B4) DOUBLE SIDED MODULE



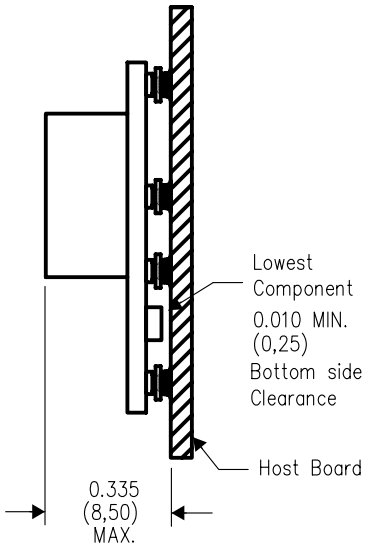
TOP VIEW



SIDE VIEW



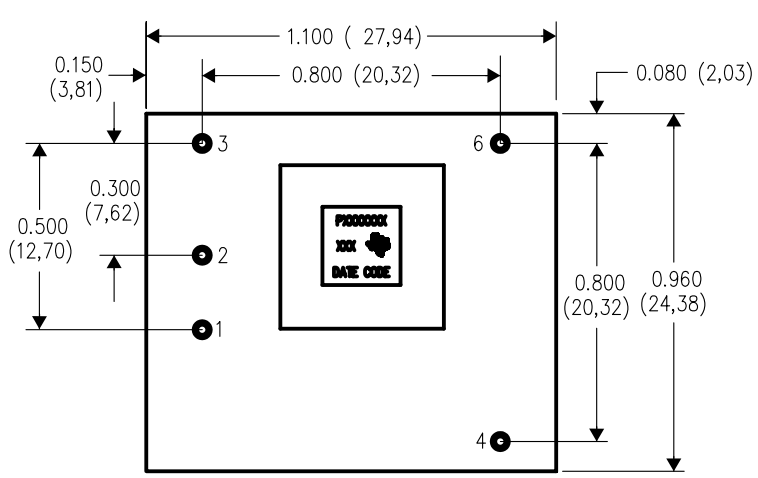
PC LAYOUT



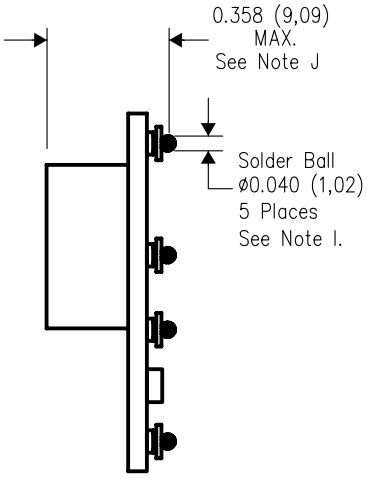
4207711–2/B 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. This is a lead–free solder ball design.
Finish: Tin (100%) over Nickel plate
Solder ball: 96.5 Sn/3.0 Ag/0.5 Cu
J. Dimension prior to reflow solder.

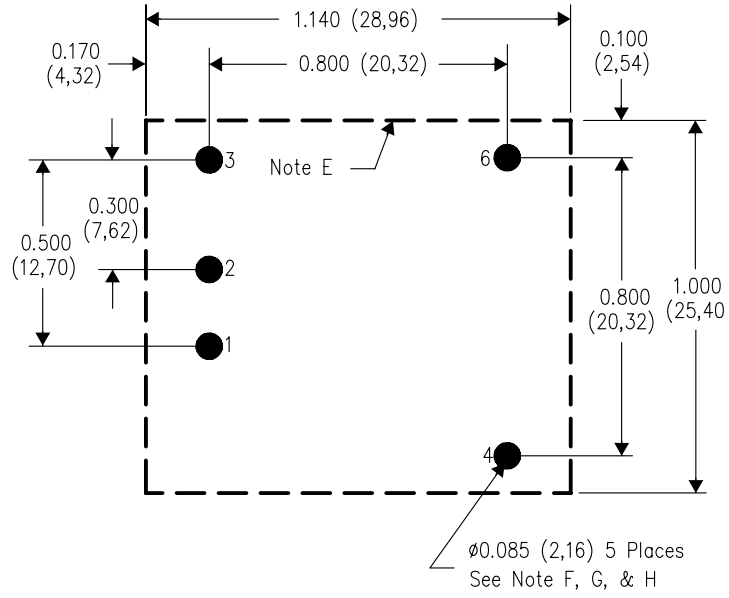
BET (R–PDSS–B5) DOUBLE SIDED MODULE



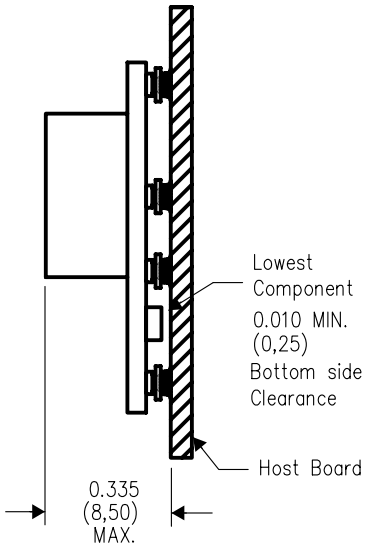
TOP VIEW



SIDE VIEW



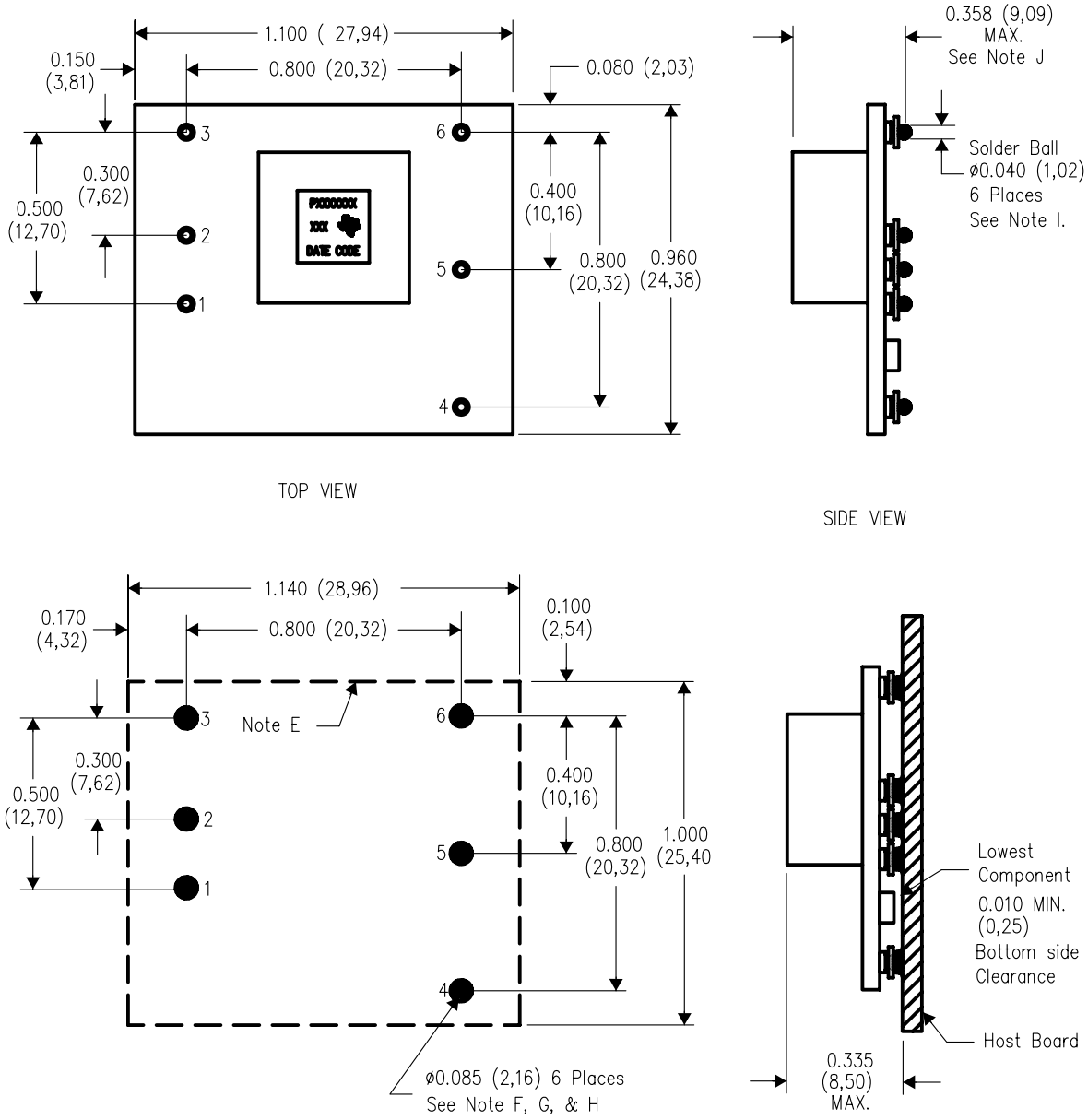
PC LAYOUT



4207711–3/B 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. This is a lead–free solder ball design.
Finish: Tin (100%) over Nickel plate
Solder ball: 96.5 Sn/3.0 Ag/0.5 Cu
J. Dimension prior to reflow solder.

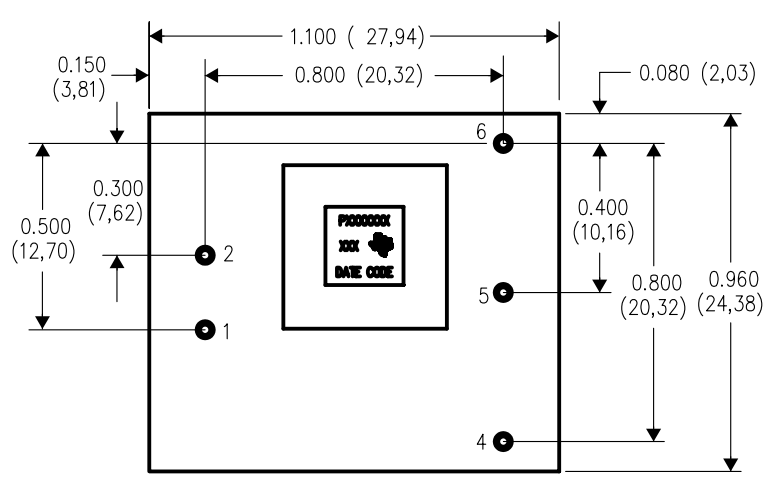
BET (R–PDSS–B6) DOUBLE SIDED MODULE



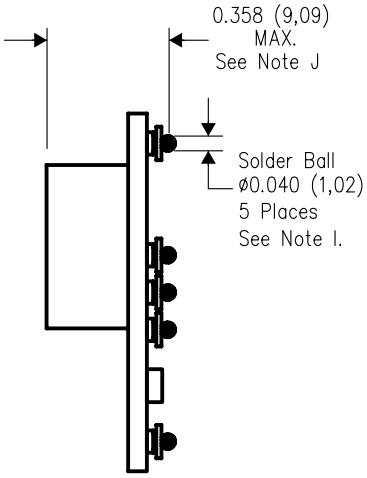
4207711–4/B 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. This is a lead–free solder ball design.
Finish: Tin (100%) over Nickel plate
Solder ball: 96.5 Sn/3.0 Ag/0.5 Cu
J. Dimension prior to reflow solder.

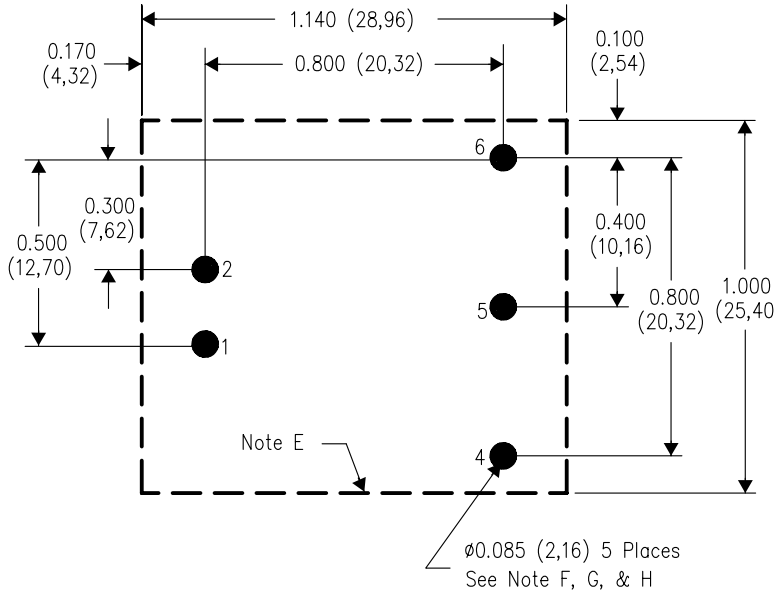
BEW (R–PDSS–B5) DOUBLE SIDED MODULE



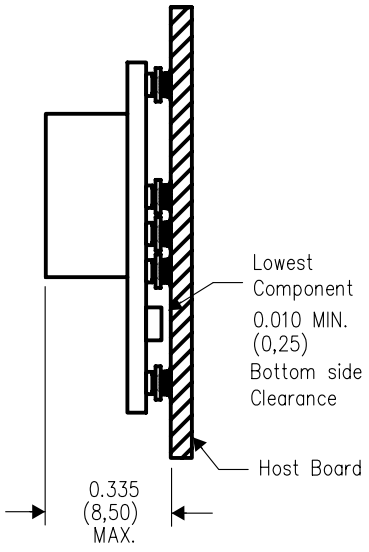
TOP VIEW



SIDE VIEW



PC LAYOUT



4207712/B 02/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. This is a lead–free solder ball design.
Finish: Tin (100%) over Nickel plate
Solder ball: 96.5 Sn/3.0 Ag/0.5 Cu
J. Dimension prior to reflow solder.

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