

## Features

- ➔ Precision supply-voltage monitor
  - 4.63V (PT7M78xxL)
  - 4.38V (PT7M78xxM)
  - 3.08V (PT7M78xxT)
  - 2.93V (PT7M78xxS)
  - 2.63V (PT7M78xxR)
  - 2.32V (PT7M78xxZ)
  - 2.20V (PT7M78xxY)
  - 4.00V (PT7M78xxJ)
  - 2.25V (PT7M78xxK)
  - 2.80V (PT7M78xxG)
- ➔ 200ms reset pulse width
- ➔ Debounced CMOS-compatible manual-reset input (7811, 7812, 7823, 7825)
- ➔ Reset Output Signal for Watchdog and Power Abnormal, Manual Reset
- ➔ Reset Push-Pull output (PT7M7809,7811,7823, 7824,7825)
- ➔ Reset Open-Drain output (PT7M7803)
- ➔ Voltage monitor for power-fail or low battery warning
- ➔ Guaranteed  $\overline{\text{RESET}}$ /RESET valid at  $V_{CC}=1.0V$

## Description

The PT7M78xx family microprocessor (μP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in μP systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

The main functions are:

1. Asserting reset output during power-up, power-down and brownout conditions for μP system.
2. Watchdog functions
3. Manual reset.

## Applications

- ➔ Power-supply circuitry in μP systems
- ➔ Networking
- ➔ Security System
- ➔ Server/Storage
- ➔ Embedded System

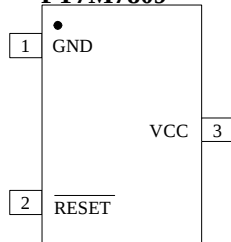
## Function Comparison Table

|   | Part No. | $\overline{\text{RESET}}$ output |            | RESET output (push-pull) | Manual Reset Input | Watchdog Input |
|---|----------|----------------------------------|------------|--------------------------|--------------------|----------------|
|   |          | Push-Pull                        | Open-Drain |                          |                    |                |
| 1 | PT7M7803 | -                                | √          | -                        | -                  | -              |
| 2 | PT7M7809 | √                                | -          | -                        | -                  | -              |
| 3 | PT7M7810 | -                                | -          | √                        | -                  | -              |
| 4 | PT7M7811 | √                                | -          | -                        | √                  | -              |
| 5 | PT7M7812 | -                                | -          | √                        | √                  | -              |
| 6 | PT7M7823 | √                                | -          | -                        | √                  | √              |
| 7 | PT7M7824 | √                                | -          | √                        | -                  | √              |
| 8 | PT7M7825 | √                                | -          | √                        | √                  | -              |

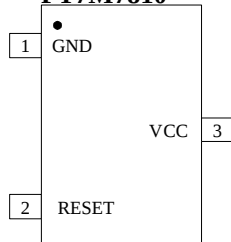
## Pin Configuration

**SOT23-3/SC70-3**

**PT7M7803  
PT7M7809**

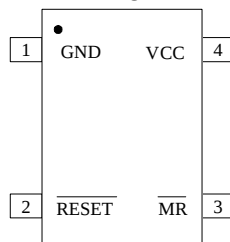


**PT7M7810**

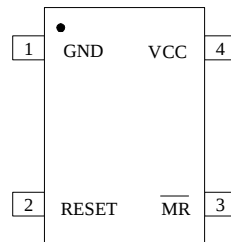


**SOT143-4**

**PT7M7811**

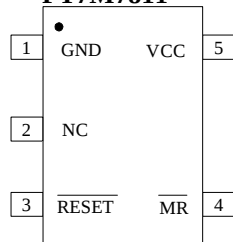


**PT7M7812**

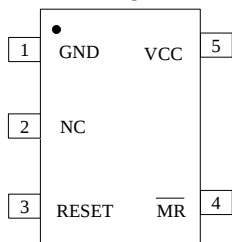


**SOT23-5**

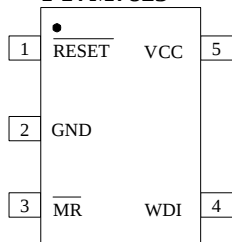
**PT7M7811**



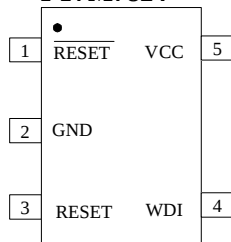
**PT7M7812**



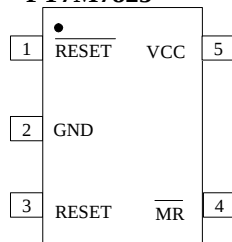
**PT7M7823**



**PT7M7824**



**PT7M7825**

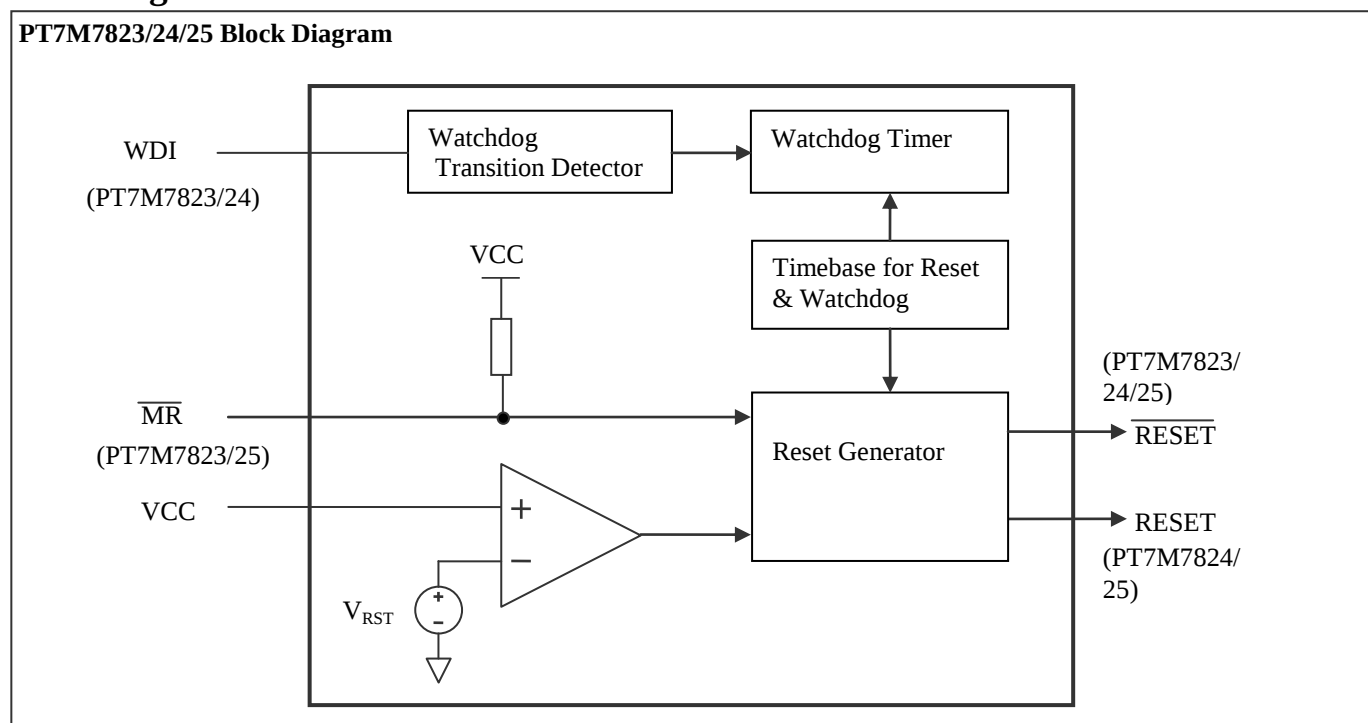


## Pin Description

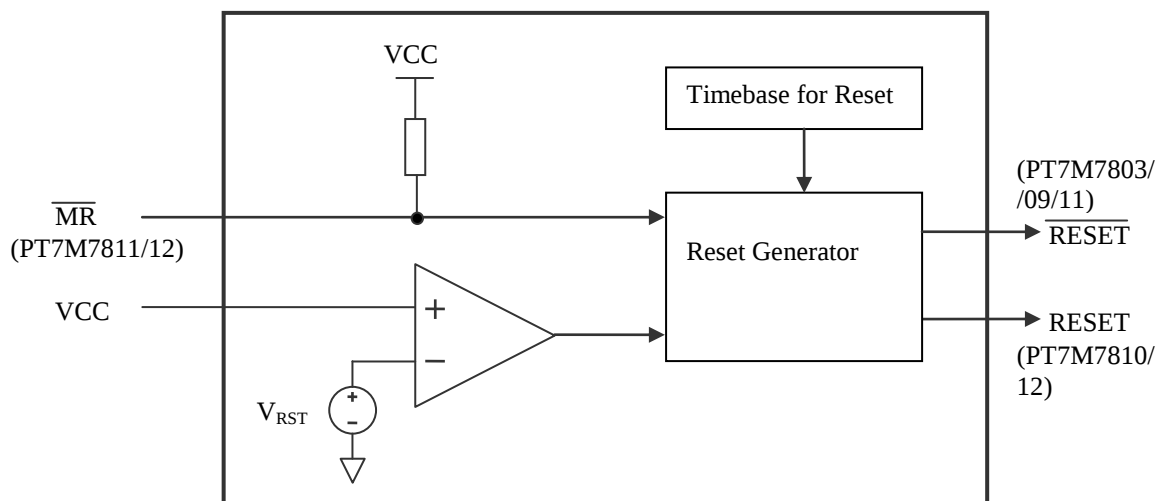
| Pin                       | Type  | Description                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{\text{MR}}$    | I     | <b>Manual-Reset: (CMOS).</b> Active low. Pull low to force a reset. Reset remains asserted for the duration of the Reset Timeout Period after $\overline{\text{MR}}$ transitions from low to high. Leave unconnected or connected to VCC if not used.                                                                                                                                       |
| VCC                       | Power | <b>Supply Voltage.</b> Reset is asserted when V <sub>CC</sub> drops below the Reset Threshold Voltage (V <sub>RST</sub> ). Reset remains asserted until V <sub>CC</sub> rises above V <sub>RST</sub> and keep asserted for the duration of the Reset Timeout Period (t <sub>RS</sub> ) once V <sub>CC</sub> rises above V <sub>RST</sub> .                                                  |
| GND                       | -     | <b>Ground Reference</b> for all signals.                                                                                                                                                                                                                                                                                                                                                    |
| WDI                       | I     | <b>Watchdog Input (CMOS).</b> If WDI remains high or low for the duration of the watchdog timeout period (t <sub>WD</sub> ), the internal watchdog timer trigger a reset output. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted or WDI occurs a rising or falling edge. |
| $\overline{\text{RESET}}$ | O     | <b>Active-Low Reset Output (Push-Pull or Open-Drain).</b> It goes low when Vcc is below the reset threshold. It remains low for about 200ms after one of the following occurs: Vcc rises above the reset threshold (VRST), the watchdog triggers a reset, or MR goes from low to high.                                                                                                      |
| RESET                     | O     | <b>The inverse of <math>\overline{\text{RESET}}</math>,</b> active high. Whenever $\overline{\text{RESET}}$ is high, RESET is low.                                                                                                                                                                                                                                                          |
| NC                        | -     | <b>No connection.</b>                                                                                                                                                                                                                                                                                                                                                                       |

## Block Diagram

**PT7M7823/24/25 Block Diagram**



**PT7M7803/09/10/11/12 Block Diagram**



## Maximum Ratings

|                                                                   |                                |
|-------------------------------------------------------------------|--------------------------------|
| Storage Temperature .....                                         | -65°C to +150°C                |
| Ambient Temperature with Power Applied.....                       | -40°C to +85°C                 |
| Supply Voltage to Ground Potential (V <sub>CC</sub> to GND) ..... | -0.3V to +7.0V                 |
| DC Input Voltage (All inputs except V <sub>CC</sub> and GND)..... | -0.3V to V <sub>CC</sub> +0.3V |
| Open-drain RESET .....                                            | -0.3V to +7.0V                 |
| DC Output Current (All outputs) .....                             | 20mA                           |
| Power Dissipation .....                                           | 320mW (Depend on package)      |

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operation Conditions

| Sym             | Description                                       | Test Conditions | Min.               | Typ. | Max.               | Unit |
|-----------------|---------------------------------------------------|-----------------|--------------------|------|--------------------|------|
| V <sub>CC</sub> | Supply Voltage for 78xxL/M/J                      | -               | 4.5                | 5.0  | 5.5                | V    |
|                 | Supply Voltage for 78xxT/S                        | -               | 3.0                | 3.3  | 5.5                | V    |
|                 | Supply Voltage for 78xxR/Z/Y/K/G                  | -               | 2.7                | 3.0  | 5.5                | V    |
| V <sub>IH</sub> | Input High Voltage (WDI, $\overline{\text{MR}}$ ) | -               | 0.7V <sub>CC</sub> | -    | V <sub>CC</sub>    | V    |
|                 | Input High Voltage for Open-drain RESET           | -               | 0                  | --   | 5.5                | V    |
| V <sub>IL</sub> | Input Low Voltage                                 | -               | -                  | -    | 0.3V <sub>CC</sub> | V    |
| T <sub>A</sub>  | Operating Temperature                             | -               | -40                | -    | 85                 | °C   |

## DC Electrical Characteristics

( $V_{CC} = V_{RN} + 5\%$  to 5.5V,  $T_A = -40 \sim 85^\circ\text{C}$ , unless otherwise noted.)(Note 1)

| Symbol       | Description                                                  | Test Conditions                                                                 |                        | Min.                | Typ.     | Max.             | Unit             |
|--------------|--------------------------------------------------------------|---------------------------------------------------------------------------------|------------------------|---------------------|----------|------------------|------------------|
| $V_{CC}$     | Operating Voltage Range                                      | -                                                                               |                        | 1.0                 | -        | 5.5              | V                |
| $I_{CC}$     | Supply Current                                               | $V_{CC} = 5\text{V}$ , No load                                                  | 7803/09/10/11/12       | -                   | 10       | 30               | $\mu\text{A}$    |
|              |                                                              |                                                                                 | 7823/24/25             | -                   | 13       | 36               |                  |
| $V_{IH}$     | Input High Voltage                                           | Pin: $\overline{\text{MR}}$ , WDI                                               |                        | $0.7V_{CC}$         | -        | $V_{CC}$         | V                |
| $V_{IL}$     | Input Low Voltage                                            | Pin: $\overline{\text{MR}}$ , WDI                                               |                        | -                   | -        | $0.3V_{CC}$      | V                |
| $V_{RST}$    | Threshold Voltage(Falling-edge)(Note 2)                      | $T_A = 25^\circ\text{C}$                                                        | 78xx                   | $V_{RN} - 1.5\%$    | $V_{RN}$ | $V_{RN} + 1.5\%$ | V                |
|              |                                                              | $T_A = -40 \sim 85^\circ\text{C}$                                               |                        | $V_{RN} - 2.5\%$    | $V_{RN}$ | $V_{RN} + 2.5\%$ |                  |
| $V_{RTH}$    | Reset Threshold Hysteresis (Note 2)                          | $V_{CC}$ varies between $V_{RN} \pm 5\%$                                        | 7823/24/25L/M          | -                   | 12       | -                | mV               |
|              |                                                              |                                                                                 | 7823/24/25 T/S/R/K/Z/Y | -                   | 4        | -                |                  |
|              |                                                              |                                                                                 | Others                 | -                   | 50       | -                |                  |
|              |                                                              |                                                                                 |                        |                     |          |                  |                  |
| $V_{OH}$     | Output High Voltage(Except 7823/24/25)                       | $V_{CC} \geq 4.5\text{V}$ $I_{source}=800\mu\text{A}$                           |                        | $V_{CC}-1.5$        | -        | -                | V                |
|              |                                                              | $V_{CC} \geq 2.7\text{V}$ $I_{source}=500\mu\text{A}$                           |                        | $0.8 \times V_{CC}$ | -        | -                |                  |
|              |                                                              | $V_{CC} \geq 1.8\text{V}$ $I_{source}=150\mu\text{A}$                           |                        | $0.8 \times V_{CC}$ | -        | -                |                  |
|              |                                                              | $V_{CC} \geq 1.0\text{V}$ $I_{source}=4\mu\text{A}$                             |                        | $0.8 \times V_{CC}$ | -        | -                |                  |
|              | Output High Voltage(7823/24/25)                              | 7823/24/25L/M, $V_{CC}=V_{RST}$ $I_{source}=120\mu\text{A}$                     |                        | $V_{CC}-1.5$        | -        | -                | V                |
|              |                                                              | 7823/24/25T/S/R/K, $V_{CC}=V_{RST}$ $I_{source}=30\mu\text{A}$                  |                        | $0.8 \times V_{CC}$ | -        | -                | V                |
| $V_{OL}$     | Output Low Voltage                                           | $V_{CC} \geq 4.5\text{V}$ $I_{sink}=3.2\text{mA}$                               |                        | -                   | -        | 0.4              | V                |
|              |                                                              | $V_{CC} \geq 2.7\text{V}$ $I_{sink}=1.2\text{mA}$                               |                        | -                   | -        | 0.3              |                  |
|              |                                                              | $V_{CC} \geq 1.0\text{V}$ $I_{sink}=100\mu\text{A}$                             |                        | -                   | -        | 0.3              |                  |
| $I_{LKG}$    | Open-Drain Output Leakage Current                            | $V_{CC} > V_{TH(MAX)}$ for 7803                                                 |                        | -                   | -        | 1                | $\mu\text{A}$    |
| $I_{WDI}$    | Average WDI Input Current (Note 3)                           | WDI connected to $V_{CC}$ : 5.5V                                                |                        | -                   | 120      | 160              | $\mu\text{A}$    |
|              |                                                              | WDI connected to GND                                                            |                        | -20                 | -15      | -                |                  |
| $I_{source}$ | RESET Output Short-Circuit Current (only for PT7M7823/24/25) | PT7M782xL/M, $\overline{\text{RESET}}=0\text{V}$ , $V_{CC}=5.5\text{V}$         |                        | -                   | -        | 800              | $\mu\text{A}$    |
|              |                                                              | PT7M782xT/S/R/K/Z/Y, $\overline{\text{RESET}}=0\text{V}$ , $V_{CC}=3.6\text{V}$ |                        | -                   | -        | 400              |                  |
| $r$          | MR pull-up resistor (internal)                               | PT7M7811/7812                                                                   |                        | 10                  | 20       | 40               | $\text{k}\Omega$ |
|              |                                                              | PT7M7823/7824/7825                                                              |                        | 35                  | 52       | 75               |                  |

**Note:** 1. Parameters of room temperature guaranteed by production test and parameters of full-temperature guaranteed by design.

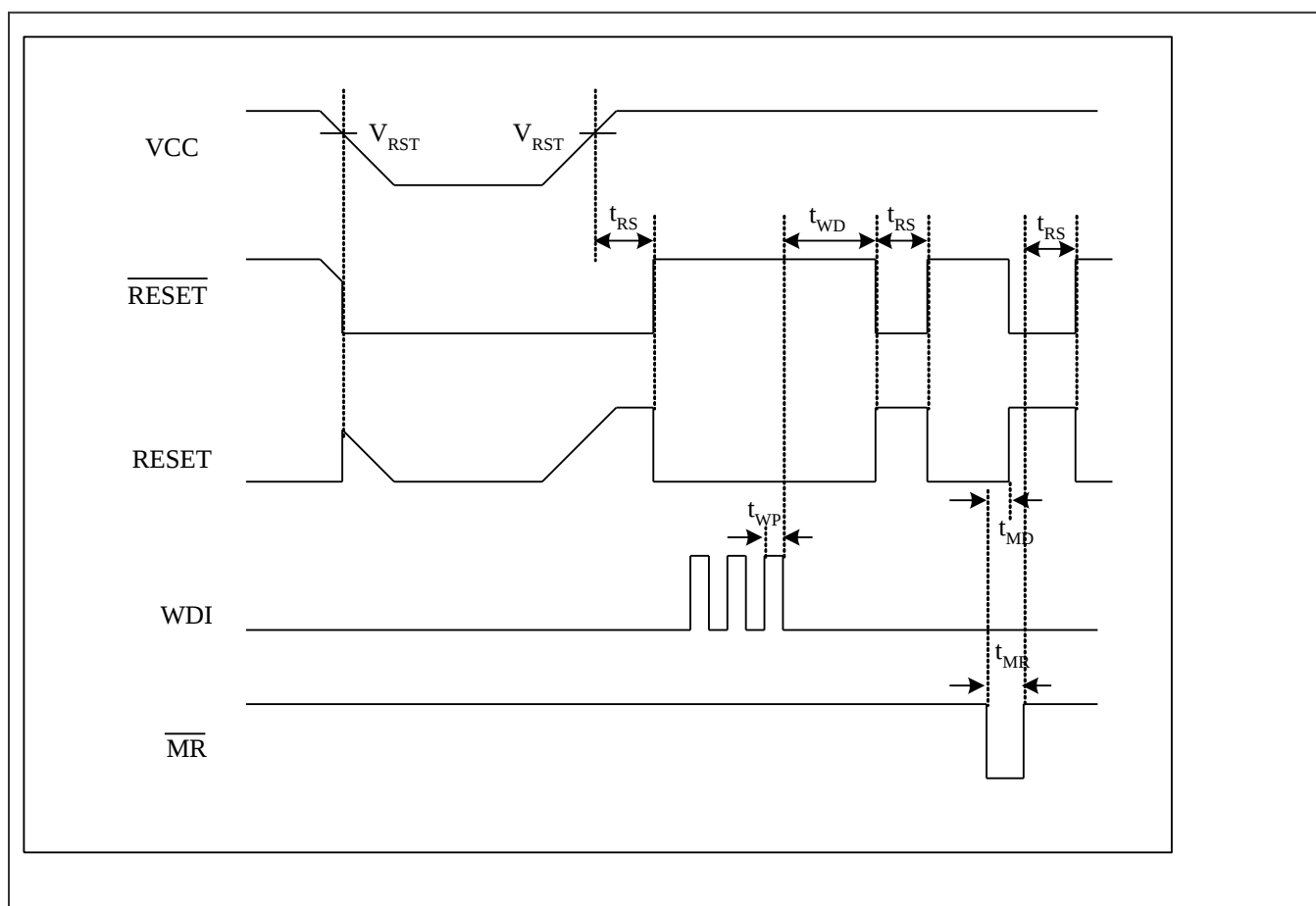
2. Valid for both RESET and RESET.  $V_{RST}$  ( $V_{RTH-}$ ) is the Reset threshold voltage when  $V_{CC}$  from high to low level, and  $V_{RTH+}$  is the Reset threshold voltage when  $V_{CC}$  from low to high level.  $V_{RN}$  is nominal reset threshold voltage.

3. WDI is internally serviced within the watchdog period if WDI is left unconnected.

## AC Electrical Characteristics

| Symbol   | Description                                 | Test Conditions                                                   | Min. | Typ. | Max. | Unit    |
|----------|---------------------------------------------|-------------------------------------------------------------------|------|------|------|---------|
| $t_{RS}$ | Reset Pulse Width                           | $\overline{MR}$ from low to High.                                 | 140  | 200  | 400  | ms      |
| $t_{WD}$ | Watchdog Timeout Period                     | WDI, $\overline{MR}$ tied to $V_{CC}$ , $V_{CC} > V_{RN} + 5\%$ . | 1.12 | 1.6  | 2.25 | s       |
| $t_{MR}$ | $\overline{MR}$ Pulse Width                 | -                                                                 | 200  | -    | -    | ns      |
| $t_{MD}$ | $\overline{MR}$ to $\overline{RESET}$ Delay | $V_{CC} = 5V$                                                     | -    | -    | 250  | ns </td |
| $t_{WP}$ | WDI Pulse Width                             | -                                                                 | 150  | -    | -    | ns      |

## Watchdog Timing Diagram



## Functional Description

### Reset Output

A microprocessor ( $\mu\text{P}$ ) reset input starts the  $\mu\text{P}$  in a known state. Whenever the  $\mu\text{P}$  is in an unknown state, it should be held in reset. The supervisory circuits assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once  $V_{CC}$  reaches about 1.0V,  $\overline{\text{RESET}}$  is a guaranteed logic low of 0.4V or less. As  $V_{CC}$  rises,  $\overline{\text{RESET}}$  stays low. When  $V_{CC}$  rises above the reset threshold, an internal timer releases  $\overline{\text{RESET}}$  after about 200ms.  $\overline{\text{RESET}}$  pulses low whenever  $V_{CC}$  drops below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 200ms. On power-down, once  $V_{CC}$  falls below the reset threshold,  $\overline{\text{RESET}}$  stays low and is guaranteed to be 0.4V or less until  $V_{CC}$  drops below 1.0V. Watchdog Timing Diagram shows the timing relationship.

The active-high RESET output is simply the inverse of the  $\overline{\text{RESET}}$  output, and is guaranteed to be valid with  $V_{CC}$  down to 1.0V.

### Watchdog Timer

The PT7M78xx watchdog circuit monitors the  $\mu\text{P}$  activity. If the  $\mu\text{P}$  does not toggle the watch-dog input (WDI) within 1.6s, reset asserts. As long as reset is asserted or the WDI input is toggled, the watchdog timer will stay clear and will not count. As soon as reset is released, the timer will start counting. WDI input pulses as short as 150ns can be detected.

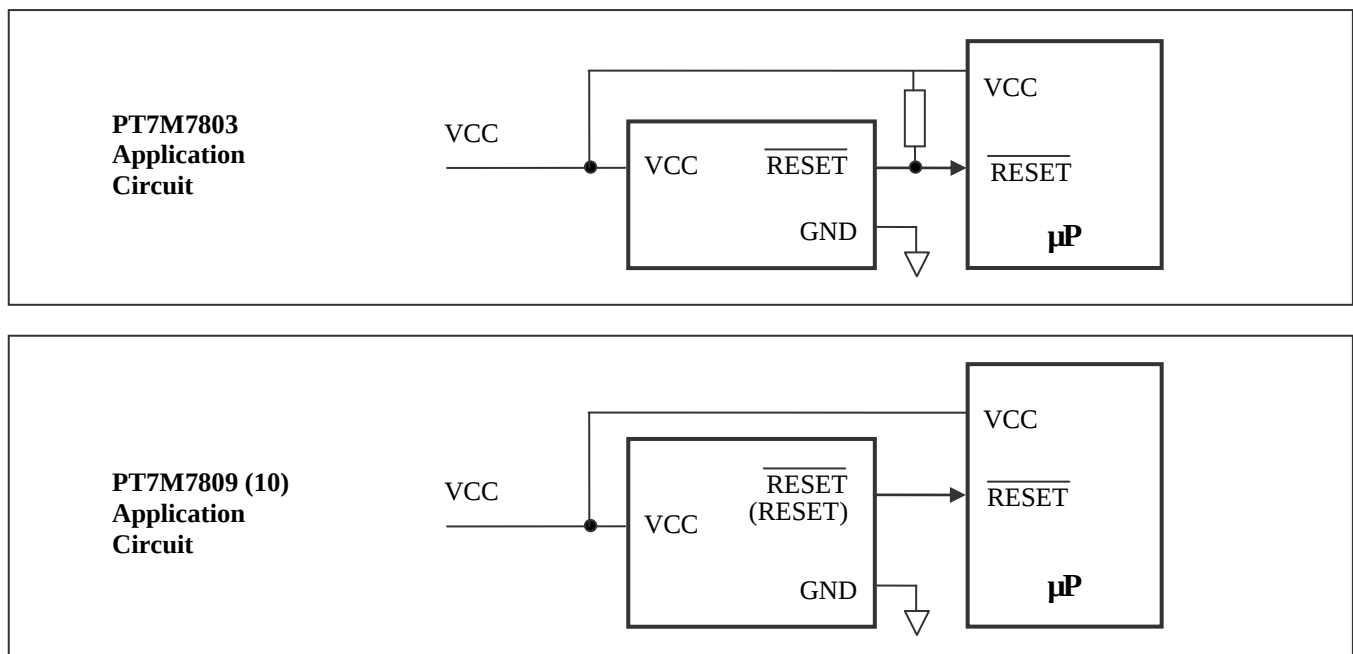
Disable the watchdog function by leaving WDI unconnected or by three-stating driver connected to WDI.

Do not apply voltage level on DCI over  $V_{CC}$ .

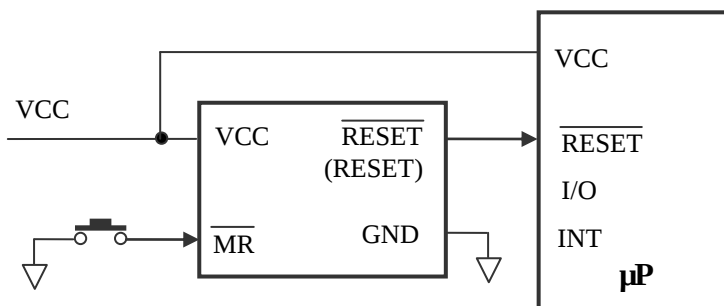
### Manual Reset

The manual-reset input ( $\overline{\text{MR}}$ ) allows reset to be triggered by a push button switch.  $\overline{\text{MR}}$  has an internal pullup resistor, so it can be left open when not used. Do not apply voltage level over  $V_{CC}$ .

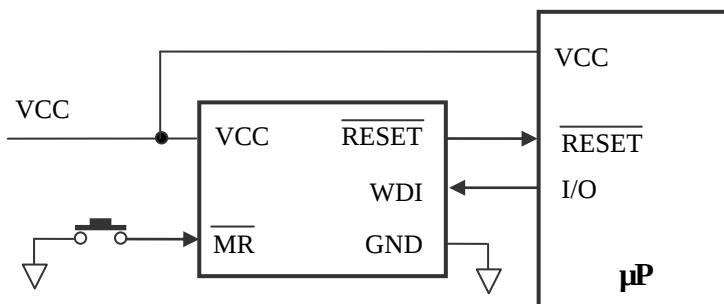
## Typical Application Circuit



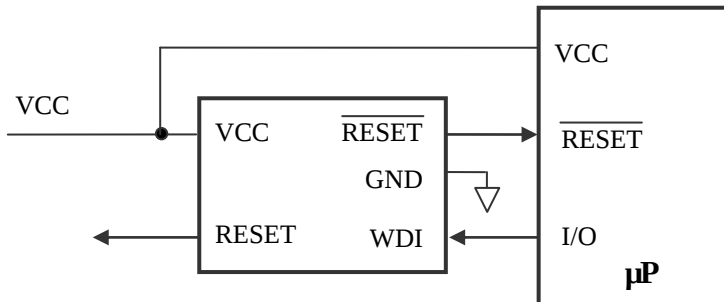
**PT7M7811 (12)  
Application  
Circuit**



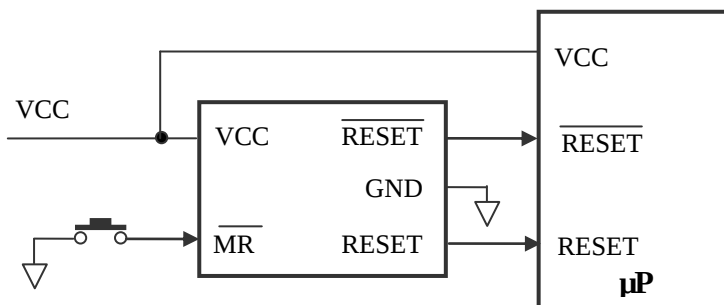
**PT7M7823  
Application  
Circuit**



**PT7M7824  
Application  
Circuit**

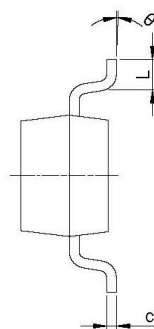
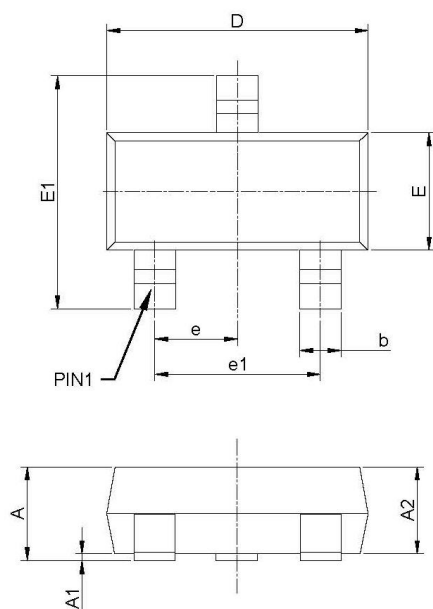


**PT7M7825  
Application  
Circuit**



## Mechanical Information

### T (SOT23)



| PKG. DIMENSIONS(MM) |          |      |
|---------------------|----------|------|
| SYMBOL              | Min      | Max  |
| A                   | 0.75     | 1.17 |
| A1                  | 0.00     | 0.15 |
| A2                  | 0.70     | 1.10 |
| b                   | 0.30     | 0.51 |
| c                   | 0.08     | 0.20 |
| D                   | 2.80     | 3.04 |
| E                   | 1.20     | 1.40 |
| E1                  | 2.10     | 2.64 |
| e                   | 0.95 BSC |      |
| e1                  | 1.90 BSC |      |
| L                   | 0.30     | 0.60 |
| θ                   | 0°       | 8°   |

#### Notes:

1. Comply with TO-236H/AA, except A1 Min, A2 Max, b Max and L Min.
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR



DATE: 03/29/16

DESCRIPTION: 3-Pin, Small Outline Transistor Plastic Package (SOT23)

PACKAGE CODE: T (T3)

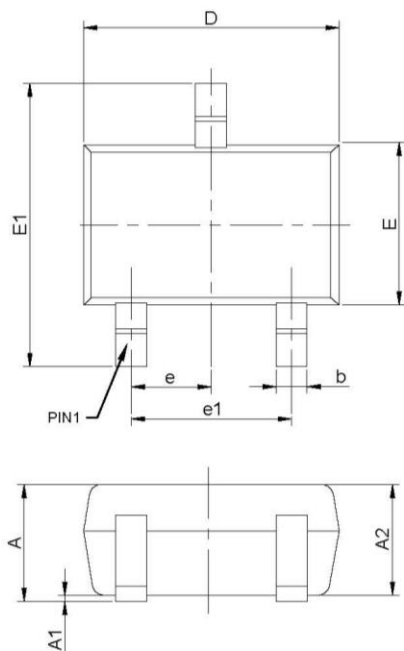
DOCUMENT CONTROL#: PD-2142

REVISION: A

16-0079

PT7M7803/7809-7812/7823-7825

C (SC70)



| PKG. DIMENSIONS(MM) |          |      |
|---------------------|----------|------|
| SYMBOL              | Min      | Max  |
| A                   | -        | 1.10 |
| A1                  | 0.00     | 0.10 |
| A2                  | 0.70     | 1.00 |
| b                   | 0.15     | 0.40 |
| c                   | 0.08     | 0.22 |
| D                   | 1.80     | 2.20 |
| E                   | 1.10     | 1.40 |
| E1                  | 1.75     | 2.45 |
| e                   | 0.65 BSC |      |
| e1                  | 1.30 BSC |      |
| L                   | 0.26     | 0.46 |
| θ                   | 0°       | 8°   |

**Note:**

1. Comply with MO-203C, except b Max, D Min, D Max, E1 Min and E1 Max.
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR



DATE: 03/29/16

DESCRIPTION: 3-Pin, SOT323 (SC70)

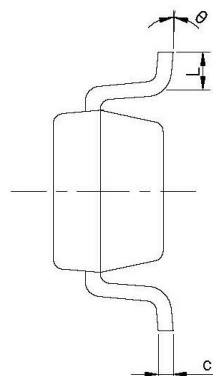
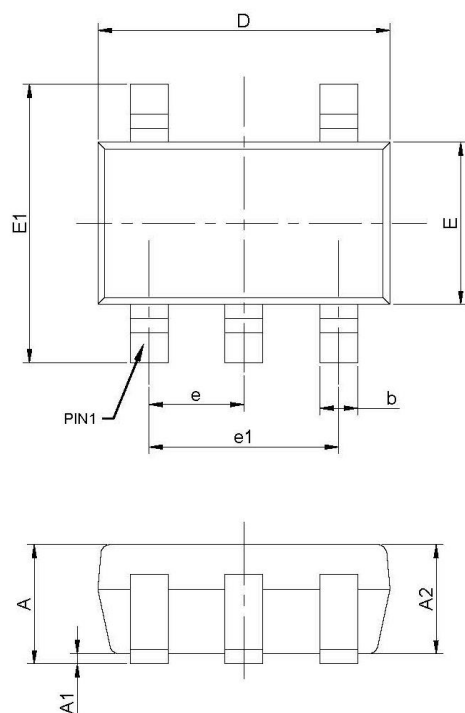
PACKAGE CODE: C (C3)

DOCUMENT CONTROL#: PD-2147

REVISION: A

16-0077

TA (SOT23)



| PKG. DIMENSIONS(MM) |          |      |
|---------------------|----------|------|
| SYMBOL              | Min      | Max  |
| A                   | -        | 1.45 |
| A1                  | 0.00     | 0.15 |
| A2                  | 0.90     | 1.30 |
| b                   | 0.30     | 0.50 |
| c                   | 0.08     | 0.22 |
| D                   | 2.75     | 3.05 |
| E                   | 1.45     | 1.75 |
| E1                  | 2.60     | 3.00 |
| e                   | 0.95 BSC |      |
| e1                  | 1.90 BSC |      |
| L                   | 0.30     | 0.60 |
| $\theta$            | 0°       | 8°   |

Note:

1. Ref: JEDEC MO-178C/AA
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BUR



DATE: 03/29/16

DESCRIPTION: 5-Pin, Small Outline Transistor Plastic Package (SOT23)

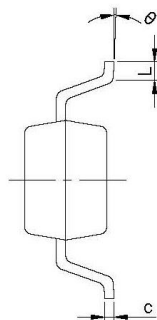
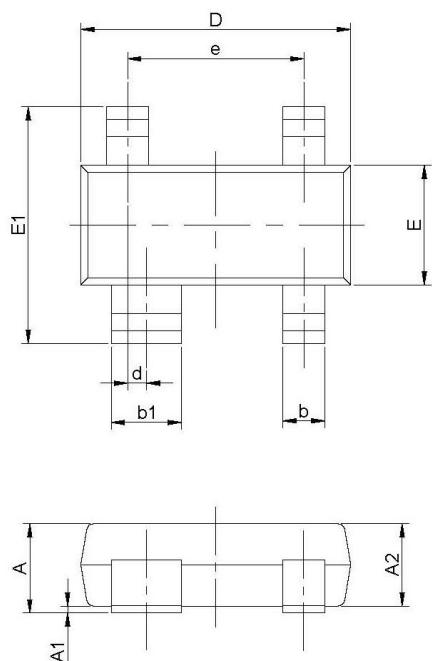
PACKAGE CODE: TA (TA5)

DOCUMENT CONTROL #: PD-2144

REVISION: A

16-0081

TB (SOT143)



| PKG. DIMENSIONS(MM) |          |      |
|---------------------|----------|------|
| SYMBOL              | Min      | Max  |
| A                   | 0.80     | 1.22 |
| A1                  | 0.00     | 0.15 |
| A2                  | 0.75     | 1.07 |
| b                   | 0.30     | 0.50 |
| b1                  | 0.75     | 0.90 |
| c                   | 0.08     | 0.20 |
| D                   | 2.80     | 3.04 |
| d                   | 0.20 BSC |      |
| E                   | 1.20     | 1.40 |
| E1                  | 2.10     | 2.64 |
| e                   | 1.92 BSC |      |
| L                   | 0.30     | 0.60 |
| θ                   | 0°       | 8°   |

**Note:**

1. Comply with TO-253D/AA, except A1 Min, b1 Min, b1 Max, and L Min.
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR



DATE: 03/29/16

DESCRIPTION: 4-Pin, SOT143

PACKAGE CODE: TB (TB4)

DOCUMENT CONTROL#: PD-2146

REVISION: A

16-0083

Note: For latest package info, please check: <http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/>

## Ordering Information

| Part Number   | Package Code | Package                                                              |
|---------------|--------------|----------------------------------------------------------------------|
| PT7M7803XTEX  | T            | 3-Pin, Small Outline Transistor Plastic (SOT23), Tape & Reel         |
| PT7M7809XTEX  | T            | 3-Pin, Small Outline Transistor Plastic (SOT23), Tape & Reel         |
| PT7M7810XTEX  | T            | 3-Pin, Small Outline Transistor Plastic (SOT23), Tape & Reel         |
| PT7M7803XC3EX | C3           | 3-Pin, SOT323 (SC70), Tape & Reel                                    |
| PT7M7809XC3EX | C3           | 3-Pin, SOT323 (SC70), Tape & Reel                                    |
| PT7M7810XC3EX | C3           | 3-Pin, SOT323 (SC70), Tape & Reel                                    |
| PT7M7811XTAEX | TA           | 5-Pin, Small Outline Transistor Plastic Package (SOT23), Tape & Reel |
| PT7M7812XTAEX | TA           | 5-Pin, Small Outline Transistor Plastic Package (SOT23), Tape & Reel |
| PT7M7823XTAEX | TA           | 5-Pin, Small Outline Transistor Plastic Package (SOT23), Tape & Reel |
| PT7M7824XTAEX | TA           | 5-Pin, Small Outline Transistor Plastic Package (SOT23), Tape & Reel |
| PT7M7825XTAEX | TA           | 5-Pin, Small Outline Transistor Plastic Package (SOT23), Tape & Reel |
| PT7M7811XTBEX | TB           | 4-Pin (SOT143), Tape & Reel                                          |
| PT7M7812XTBEX | TB           | 4-Pin (SOT143), Tape & Reel                                          |
| *PT7M7809XUWF | UWF          | Wafer form                                                           |

### Note:

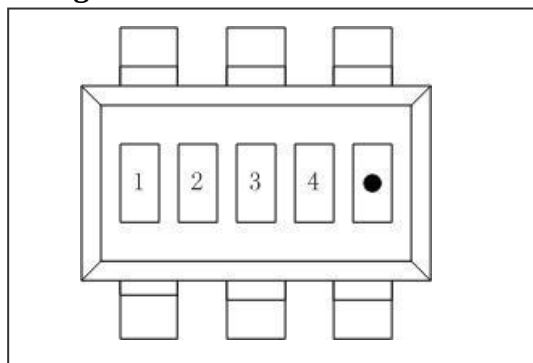
- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel
- “\*” for UWF package, please check the storage with related sales.

### Suffix: X—Monitored Voltage

| X                   | L    | M    | T    | S    | R    | Z    | Y    | J    | K    | G    |
|---------------------|------|------|------|------|------|------|------|------|------|------|
| Reset Threshold (V) | 4.63 | 4.38 | 3.08 | 2.93 | 2.63 | 2.32 | 2.20 | 4.00 | 2.25 | 2.80 |

**PT7M7803/7809-7812/7823-7825**

## Marking Information



| Code | Description        |
|------|--------------------|
| 1 2  | Part Number        |
| 3    | Year               |
| 4    | Work Week          |
| ●    | Only for PT7M7809M |

## Part Number Code

| Code 1 2 | Part No   | Code 1 2 | Part No   | Code 1 2 | Part No   | Code 1 2 | Part No   |
|----------|-----------|----------|-----------|----------|-----------|----------|-----------|
| AA       | PT7M7809L | AO       | PT7M7811L | BC       | PT7M7803L | BQ       | PT7M7824L |
| AB       | PT7M7809M | AP       | PT7M7811M | BD       | PT7M7803M | BR       | PT7M7824M |
| AC       | PT7M7809T | AQ       | PT7M7811T | BE       | PT7M7803T | BS       | PT7M7824T |
| AD       | PT7M7809S | AR       | PT7M7811S | BF       | PT7M7803S | BT       | PT7M7824S |
| AE       | PT7M7809R | AS       | PT7M7811R | BG       | PT7M7803R | BU       | PT7M7824R |
| AF       | PT7M7809Z | AT       | PT7M7811Z | BH       | PT7M7803Z | BV       | PT7M7824Z |
| AG       | PT7M7809Y | AU       | PT7M7811Y | BI       | PT7M7803Y | BW       | PT7M7824Y |
| jm       | PT7M7809J | sf       | PT7M7811J | sc       | PT7M7803J | si       | PT7M7824J |
| pE       | PT7M7809G |          |           |          |           | mQ       | PT7M7824K |
| AH       | PT7M7810L | AV       | PT7M7812L | BJ       | PT7M7823L | BX       | PT7M7825L |
| AI       | PT7M7810M | AW       | PT7M7812M | BK       | PT7M7823M | BY       | PT7M7825M |
| AJ       | PT7M7810T | AX       | PT7M7812T | BL       | PT7M7823T | BZ       | PT7M7825T |
| AK       | PT7M7810S | AY       | PT7M7812S | BM       | PT7M7823S | CA       | PT7M7825S |
| AL       | PT7M7810R | AZ       | PT7M7812R | BN       | PT7M7823R | CB       | PT7M7825R |
| AM       | PT7M7810Z | BA       | PT7M7812Z | BO       | PT7M7823Z | CC       | PT7M7825Z |
| AN       | PT7M7810Y | BB       | PT7M7812Y | BP       | PT7M7823Y | CD       | PT7M7825Y |
| se       | PT7M7810J | sg       | PT7M7812J | sh       | PT7M7823J | sj       | PT7M7825J |
|          |           |          |           | mP       | PT7M7823K |          |           |

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