

AAP Gen 7 (TO-240AA) Power Modules Thyristor/Diode and Thyristor/Thyristor, 75 A



ADD-A-PAK



FEATURES

- High voltage
- Industrial standard package
- Low thermal resistance
- UL approved file E78996 
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- Up to 1600 V
- High surge capability
- Easy mounting on heatsink

PRIMARY CHARACTERISTICS

$I_{T(AV)}$ or $I_{F(AV)}$	75 A
Type	Modules - thyristor, standard
Package	AAP Gen 7 (TO-240AA)

MECHANICAL DESCRIPTION

The AAP Gen 7 (TO-240AA), new generation of AAP module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

ELECTRICAL DESCRIPTION

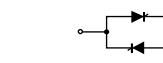
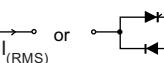
These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, temperature and motor speed control circuits, UPS and battery charger.

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$ or $I_{F(AV)}$	85 °C	75	A
$I_{O(RMS)}$	As AC switch	165	
I_{TSM} , I_{FSM}	50 Hz	1300	
	60 Hz	1360	
I^2t	50 Hz	8.45	kA^2s
	60 Hz	7.68	
$I^2\sqrt{t}$		84.5	$kA^2\sqrt{s}$
V_{RRM}	Range	400 to 1600	V
T_{Stg}		-40 to +125	°C
T_J		-40 to +125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS					
TYPE NUMBER	VOLTAGE CODE	V_{RRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	V_{DRM}, MAXIMUM REPETITIVE PEAK OFF-STATE VOLTAGE, GATE OPEN CIRCUIT V	I_{RRM}, I_{DRM} AT 125 °C mA
VS-VSK.71	04	400	500	400	15
	06	600	700	600	
	08	800	900	800	
	10	1000	1100	1000	
	12	1200	1300	1200	
	14	1400	1500	1400	
	16	1600	1700	1600	

ON-STATE CONDUCTION									
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS			
Maximum average on-state current (thyristors)	$I_{T(AV)}$	180° conduction, half sine wave, $T_C = 85^\circ C$			75	A			
Maximum average forward current (diodes)	$I_{F(AV)}$								
Maximum continuous RMS on-state current, as AC switch	$I_{O(RMS)}$	 or 			165				
Maximum peak, one-cycle non-repetitive on-state or forward current	I_{TSM} or I_{FSM}	$t = 10$ ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	1300				
		$t = 8.3$ ms			1360				
		$t = 10$ ms	100 % V_{RRM} reapplied		1093				
		$t = 8.3$ ms			1140				
Maximum I^2t for fusing	I^2t	$t = 10$ ms	No voltage reapplied	Initial $T_J = T_J$ maximum	8.45	kA ² s			
		$t = 8.3$ ms			7.68				
		$t = 10$ ms	100 % V_{RRM} reapplied		5.97				
		$t = 8.3$ ms			5.45				
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$ (1)	$t = 0.1$ ms to 10 ms, no voltage reapplied $T_J = T_J$ maximum			84.5	kA ² \sqrt{s}			
Maximum value or threshold voltage	$V_{T(TO)}$ (2)	Low level (3)	$T_J = T_J$ maximum		0.96	V			
		High level (4)			1.08				
Maximum value of on-state slope resistance	r_t (2)	Low level (3)	$T_J = T_J$ maximum		3.28	mΩ			
		High level (4)			2.86				
Maximum peak on-state or forward voltage	V_{TM}	$I_{TM} = \pi \times I_{T(AV)}$	$T_J = 25^\circ C$		1.72	V			
	V_{FM}	$I_{FM} = \pi \times I_{F(AV)}$							
Maximum non-repetitive rate of rise of turned on current	dl/dt	$T_J = 25^\circ C$, from 0.67 V_{DRM} , $I_{TM} = \pi \times I_{T(AV)}$, $I_g = 500$ mA, $t_r < 0.5$ μs, $t_p > 6$ μs			150	A/μs			
Maximum holding current	I_H	$T_J = 25^\circ C$, anode supply = 6 V, resistive load, gate open circuit			250	mA			
Maximum latching current	I_L	$T_J = 25^\circ C$, anode supply = 6 V, resistive load			400				

Notes

(1) I^2t for time $t_x = I^2\sqrt{t} \times \sqrt{t_x}$

(2) Average power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$

(3) 16.7 % $\times \pi \times I_{AV} < I < \pi \times I_{AV}$

(4) $I > \pi \times I_{AV}$

TRIGGERING								
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS		
Maximum peak gate power	P _{GM}				12	W		
Maximum average gate power	P _{G(AV)}				3.0			
Maximum peak gate current	I _{GM}				3.0	A		
Maximum peak negative gate voltage	- V _{GM}				10	V		
Maximum gate voltage required to trigger	V _{GT}	T _J = -40 °C	Anode supply = 6 V resistive load		4.0			
		T _J = 25 °C			2.5			
		T _J = 125 °C			1.7			
Maximum gate current required to trigger	I _{GT}	T _J = -40 °C	Anode supply = 6 V resistive load		270	mA		
		T _J = 25 °C			150			
		T _J = 125 °C			80			
Maximum gate voltage that will not trigger	V _{GD}	T _J = 125 °C, rated V _{DRM} applied			0.25	V		
Maximum gate current that will not trigger	I _{GD}	T _J = 125 °C, rated V _{DRM} applied			6	mA		

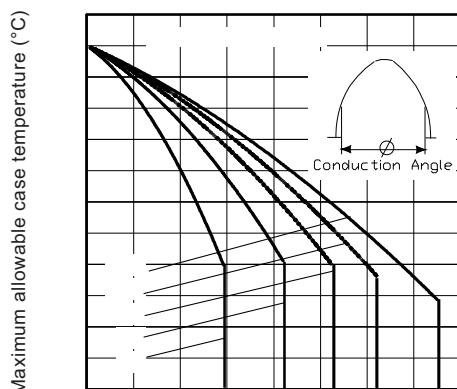
BLOCKING						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum peak reverse and off-state leakage current at V _{RRM} , V _{DRM}	I _{RRM} , I _{DRM}	T _J = 125 °C, gate open circuit			15	mA
Maximum RMS insulation voltage	V _{INS}	50 Hz			3000 (1 min) 3600 (1 s)	V
Maximum critical rate of rise of off-state voltage	dV/dt	T _J = 125 °C, linear to 0.67 V _{DRM}			1000	V/μs

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Junction operating and storage temperature range	T _J , T _{Stg}				-40 to +125	°C
Maximum internal thermal resistance, junction to case per leg	R _{thJC}	DC operation			0.29	°C/W
Typical thermal resistance, case to heatsink per module	R _{thCS}	Mounting surface flat, smooth and greased			0.1	
Mounting torque ± 10 %	to heatsink	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.			4	Nm
	busbar				3	
Approximate weight					75	g
					2.7	oz.
Case style		JEDEC®			AAP Gen 7 (TO-240AA)	

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.71..	0.052	0.062	0.079	0.116	0.197	0.037	0.064	0.085	0.121	0.200	°C/W

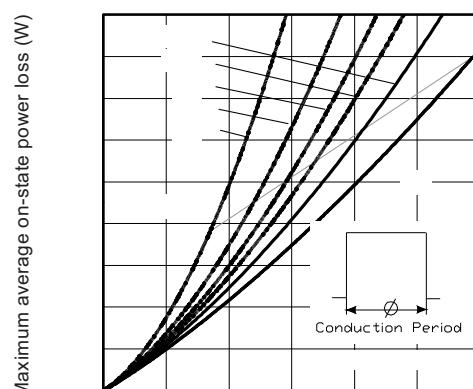
Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC



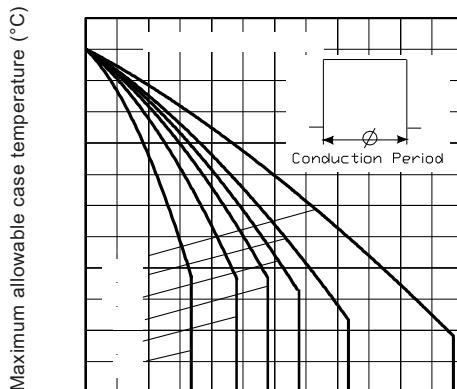
Average on-state current (A)

Fig. 1 - Current Ratings Characteristics



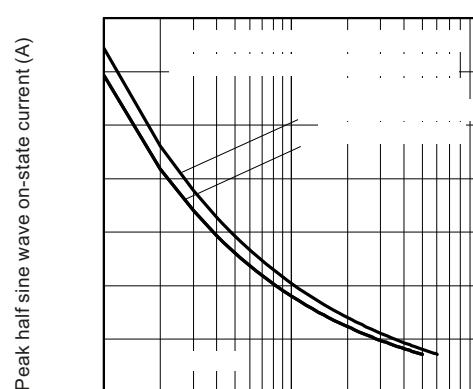
Average on-state current (A)

Fig. 4 - On-State Power Loss Characteristics



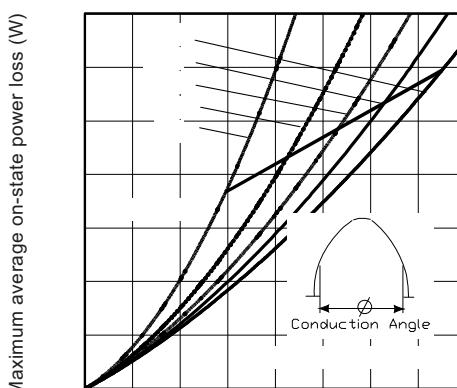
Average on-state current (A)

Fig. 2 - Current Ratings Characteristics



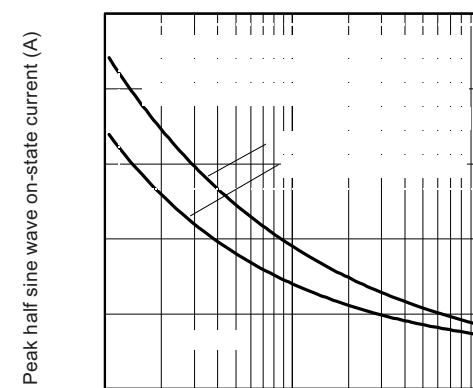
Number of equal amplitude half cycle current pulses (N)

Fig. 5 - Maximum Non-Repetitive Surge Current



Average on-state current (A)

Fig. 3 - On-State Power Loss Characteristics



Pulse train duration (s)

Fig. 6 - Maximum Non-Repetitive Surge Current

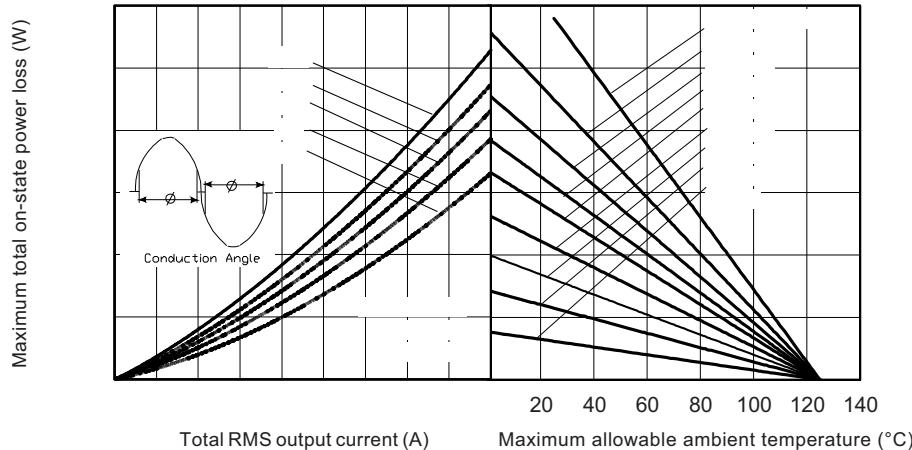


Fig. 7 - On-State Power Loss Characteristics

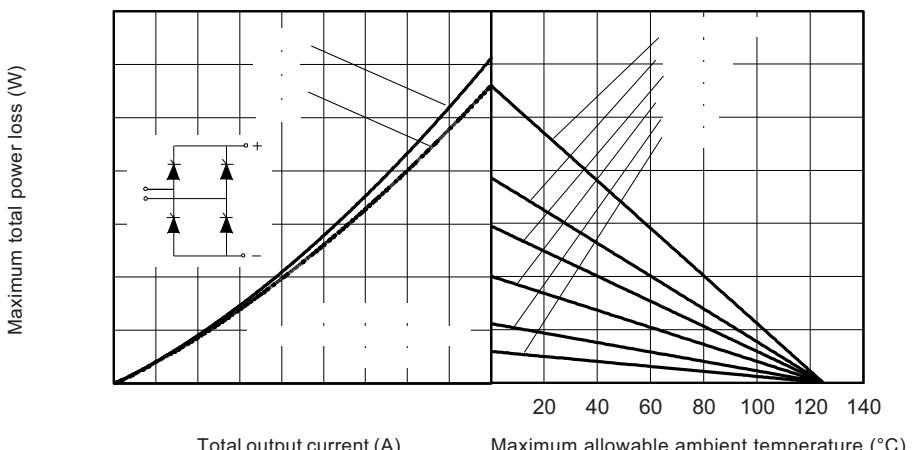


Fig. 8 - On-State Power Loss Characteristics

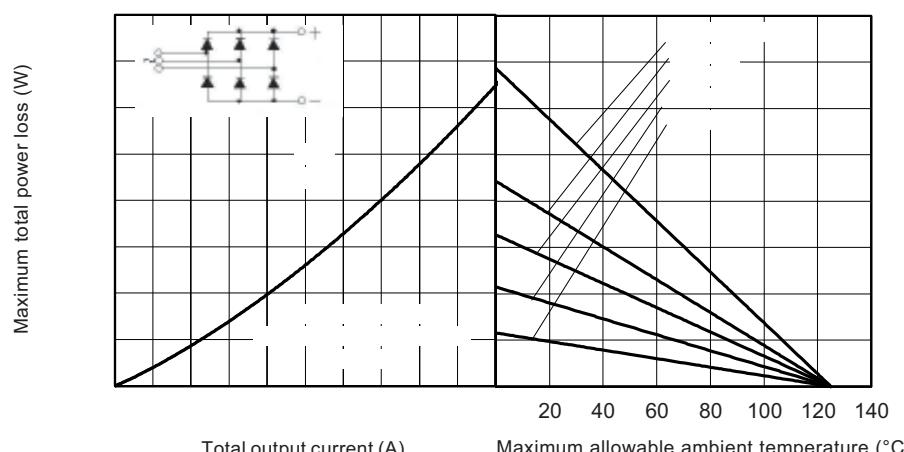


Fig. 9 - On-State Power Loss Characteristics

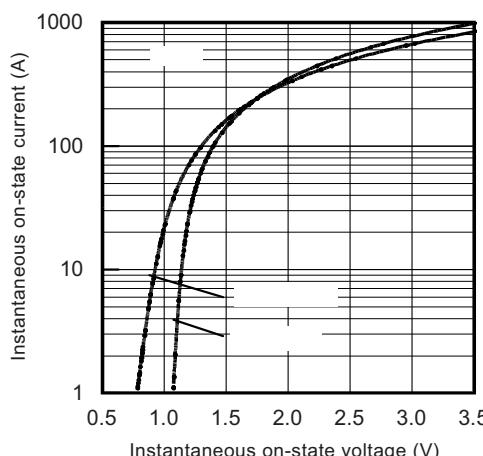


Fig. 10 - On-State Voltage Drop Characteristics

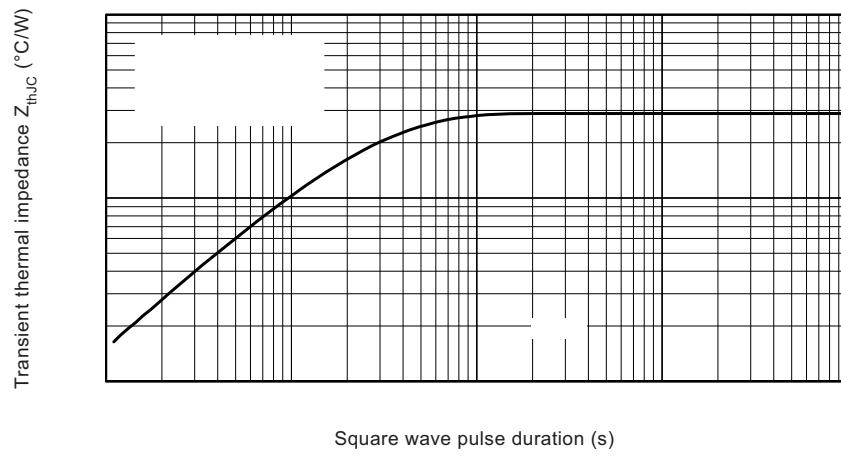


Fig. 11 - Thermal Impedance Z_{thJC} Characteristics

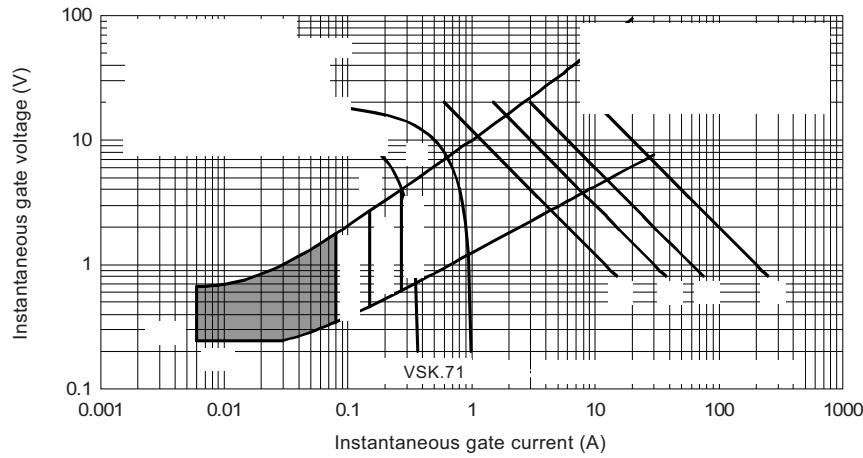


Fig. 12 - Gate Characteristics

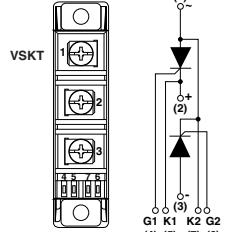
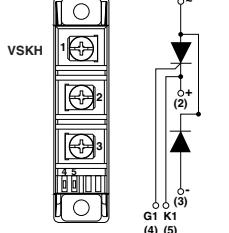
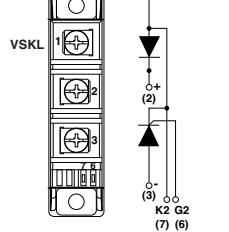
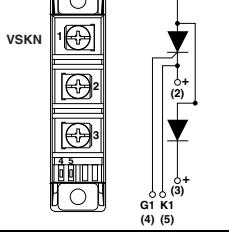
ORDERING INFORMATION TABLE

Device code	VS-VS	K	T	71	I	16
	(1)	(2)	(3)	(4)	(5)	

1	- Vishay Semiconductors product
2	- Module type
3	- Circuit configuration (see Circuit Configuration table)
4	- Current code (75 A)
5	- Voltage code (see Voltage Ratings table)

Note

- To order the optional hardware go to www.vishay.com/doc?95172

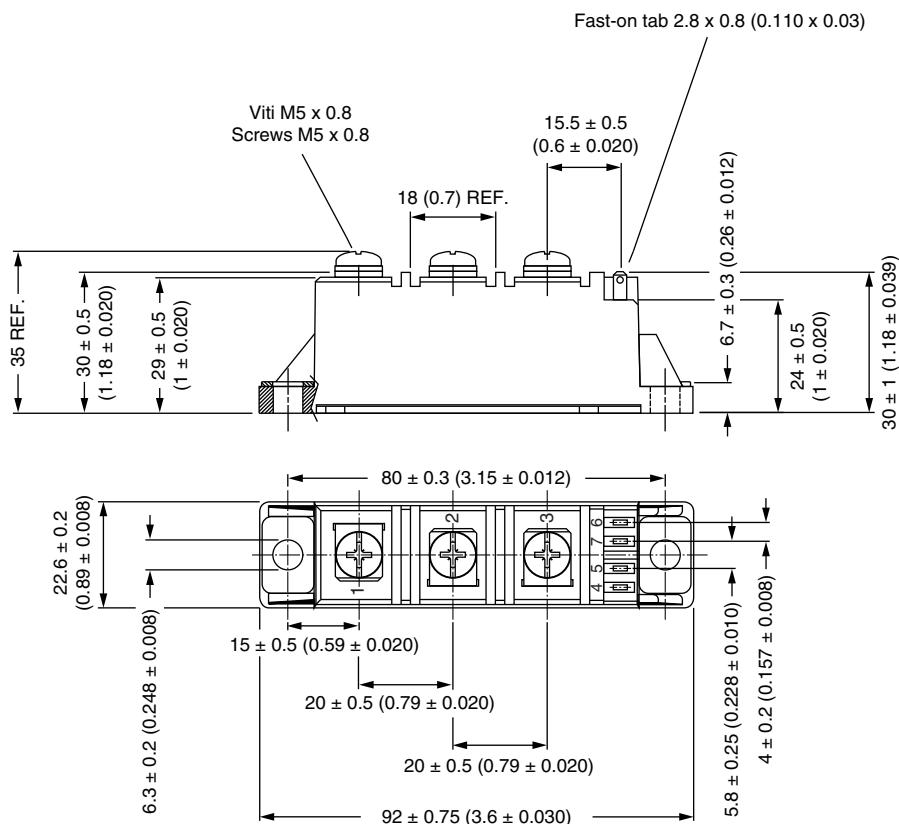
CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	T	
SCR/diode doubler circuit, positive control	H	
SCR/diode doubler circuit, negative control	L	
SCR/diode common anodes	N	

LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95368
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ADD-A-PAK Generation VII - Thyristor

DIMENSIONS in millimeters (inches)



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