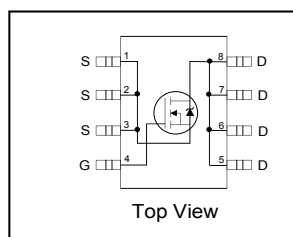


HEXFET® Chip-Set for DC-DC Converters

- N Channel Application Specific MOSFETs
- Ideal for Mobile DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Lead-Free


Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make this device ideal for high efficiency DC-DC Converters that power the latest generation of mobile microprocessors.

The IRF7805PbF offers maximum efficiency for mobile CPU core DC-DC converters.

Devices Features

	IRF7805PbF
V_{DS}	30V
R_{DS(on)}	11mΩ
Q_g	31nC
Q_{sw}	11.5nC
Q_{oss}	36nC

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF7805PbF	SO-8	Tape and Reel	4000	IRF7805PbF

Symbol	Parameter	Max.	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-to-Source Voltage	± 12	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V ③	13	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V ③	10	
I _{DM}	Pulsed Drain Current ①	100	
P _D @ T _A = 25°C	Maximum Power Dissipation ③	2.5	W
P _D @ T _A = 70°C	Maximum Power Dissipation ③	1.6	
	Linear Derating Factor	0.02	W/°C
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJL}	Junction-to-Drain Lead ⑤	—	20	°C/W
R _{θJA}	Junction-to-Ambient ③	—	50	

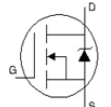
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage ⑥	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance ⑥	—	9.2	11	m Ω	$V_{GS} = 4.5V, I_D = 7.0A$ ②
$V_{GS(th)}$	Gate Threshold Voltage ⑥	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	70	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	10		$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 100^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -12V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Q_g	Total Gate Charge ⑥	—	22	31	nC	$V_{GS} = 5.0V$ $V_{DS} = 16V$ $I_D = 7.0A$
Q_{gs1}	Pre -Vth Gate-to-Source Charge	—	3.7	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	1.4	—		
Q_{gd}	Gate-to-Drain Charge	—	6.8	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$) ⑥	—	8.2	11.5		
Q_{oss}	Output Charge ⑥	—	30	36	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	0.5	—	1.7	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 16V, V_{GS} = 4.5V$ ② $I_D = 7.0A$ $R_G = 2\Omega$ Resistive Load
t_r	Rise Time	—	20	—		
$t_{d(off)}$	Turn-Off Delay Time	—	38	—		
t_f	Fall Time	—	16	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ①	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	106		
V_{SD}	Diode Forward Voltage ⑥	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 7.0A, V_{GS} = 0V$
Q_{rr}	Reverse Recovery Charge ④	—	88	—	nC	$di/dt = 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_S = 7.0A$
Q_{rr}	Reverse Recovery Charge ④	—	55	—		$di/dt = 700A/\mu s$ (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_S = 7.0A$

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ③ When mounted on 1" in square copper board, $t < 10$ sec.
- ④ Typ = measured - Q_{oss}
- ⑤ R_θ is measured at T_J of approximately 90°C .
- ⑥ Devices are 100% tested to these parameters.

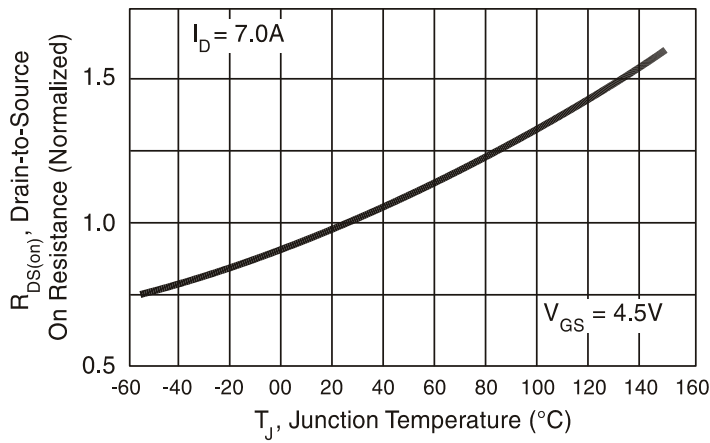


Fig. 1 Normalized On-Resistance vs. Temperature

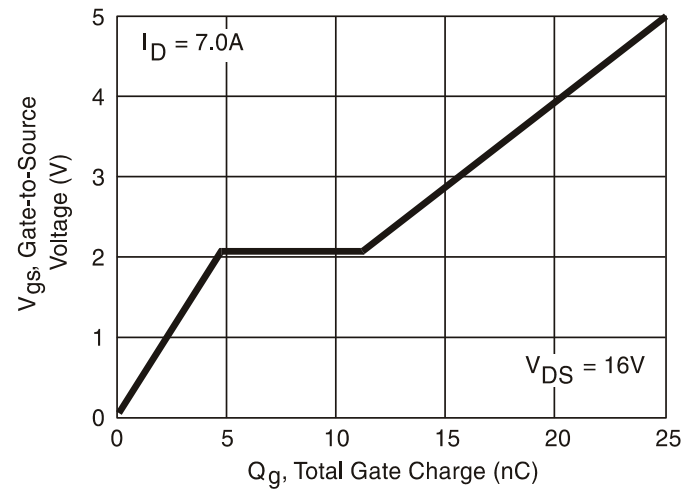


Fig. 2 Typical Gate Charge vs. Gate-to-Source Voltage

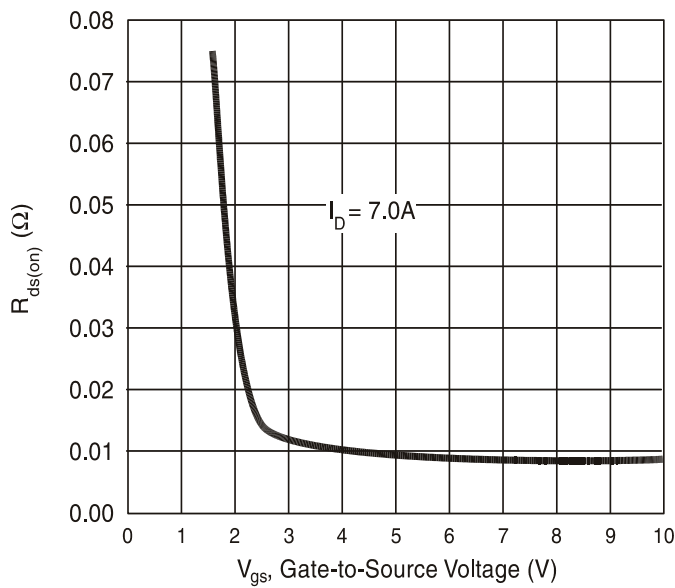


Fig. 3 Typical $R_{DS(on)}$ vs. Gate-to-Source Voltage

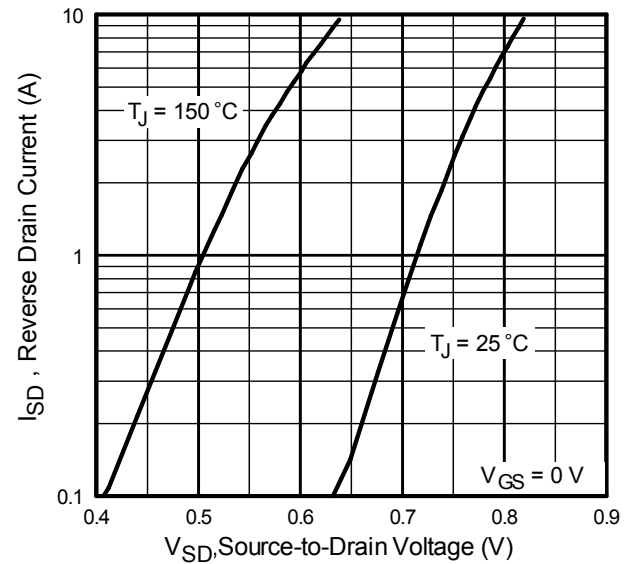


Fig. 4 Typical Source-Drain Diode Forward Voltage

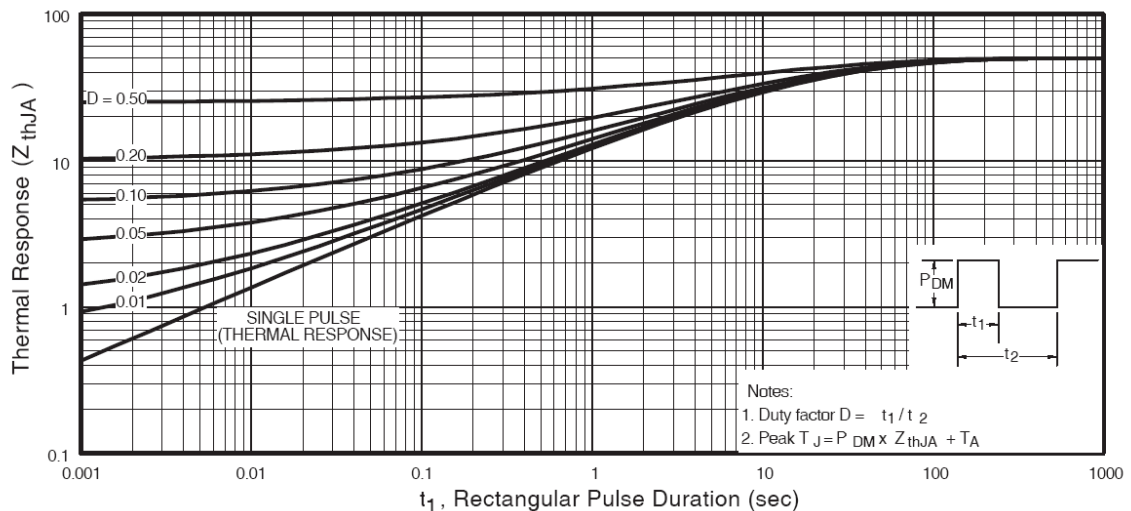
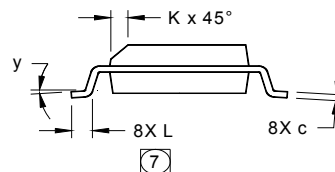
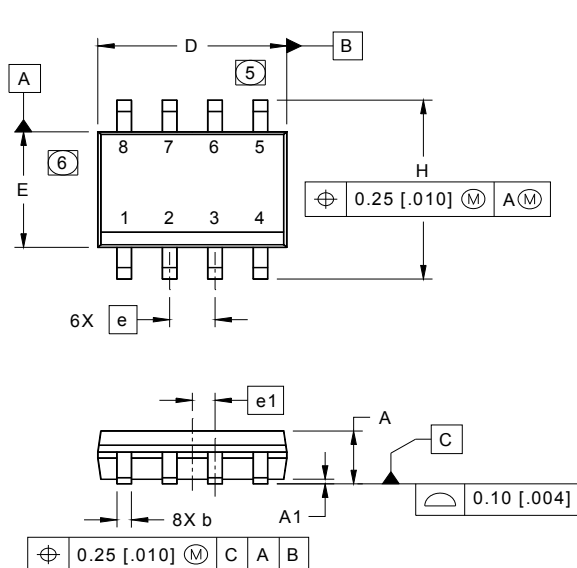
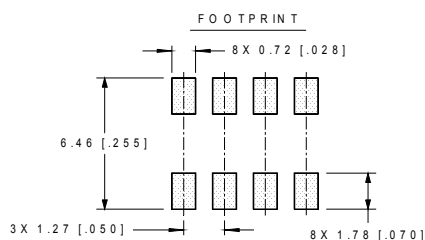


Fig. 5. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

SO-8 Package Outline (Dimensions are shown in millimeters (inches))

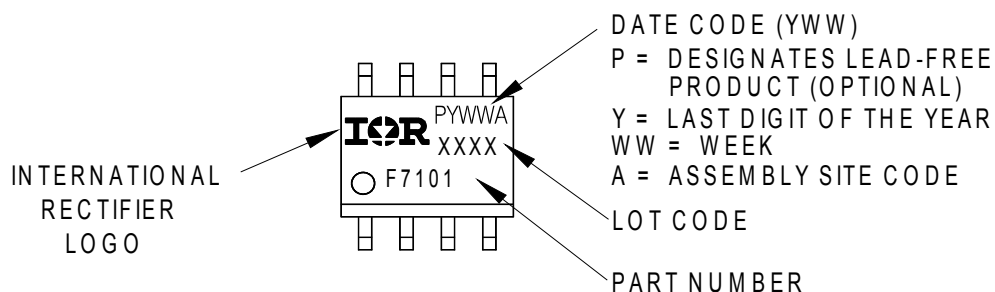


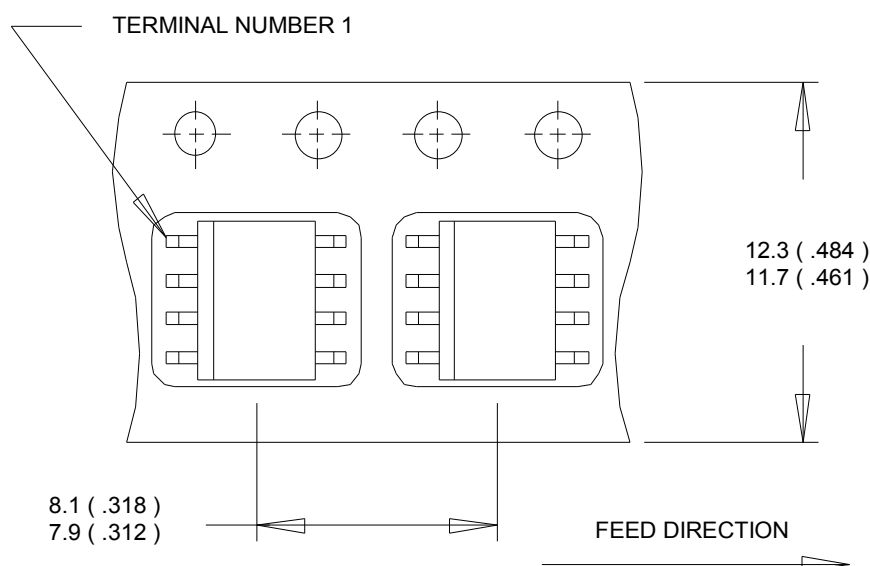
- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
 5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
 6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
 7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



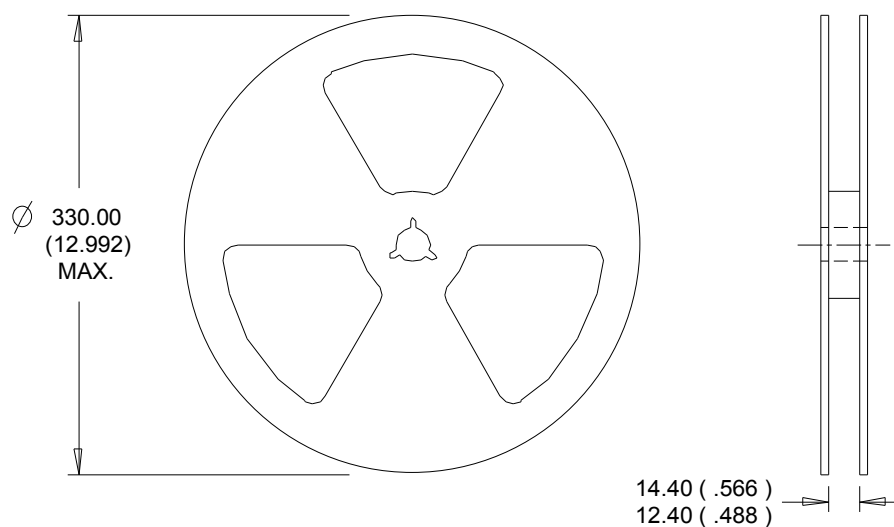
SO-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7101 (MOSFET)



SO-8 Tape and Reel (Dimensions are shown in millimeters (inches))

NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification Information

Qualification Level	Consumer	
Moisture Sensitivity Level	SO-8	MSL1 (per JEDEC J-STD-020D) [†]
RoHS Compliant	Yes	

[†] Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
08/23/2016	<ul style="list-style-type: none"> Changed datasheet with Infineon logo - all pages. Corrected typo Qoss from typ/max "3.0nC/3.6nC" to "30nC/36nC" on page 2. Added disclaimer on last page.

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