VN750

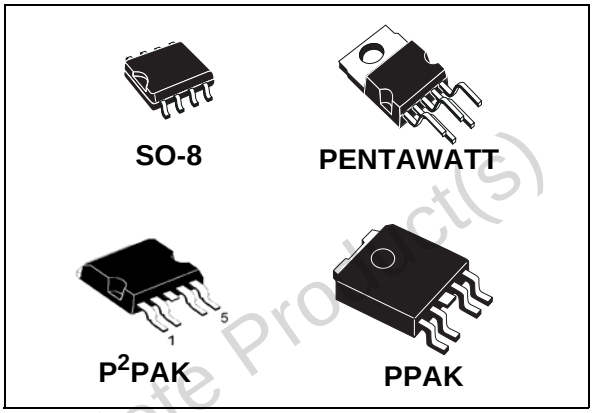
High-side driver

Datasheet – production data

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN750 VN750S VN750PT VN750-B5	60 mΩ	6 A	36 V

- CMOS compatible input
- On-state open-load detection
- Off-state open-load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protection



Description

The VN750 is a monolithic device designed using STMicroelectronic® VIPower® M0-3 technology. The VN750 is intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the device against low energy spikes.

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device detects the open-load condition in both the on-state and off-state. In the off-state the device detects if the output is shorted to V_{CC}. The device automatically turns off where the ground pin becomes disconnected.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PENTAWATT	VN750	—
SO-8	VN750S	VN750S13TR
P^2PAK	VN750-B5	VN750-B513TR
PPAK	VN750PT	VN750PT13TR

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

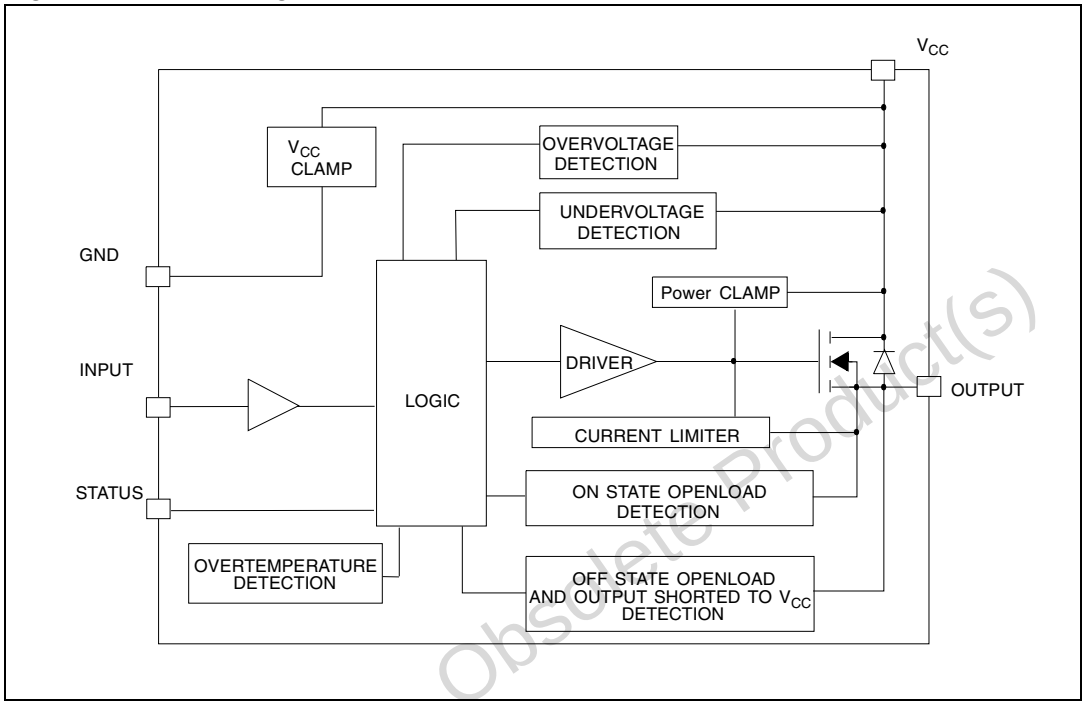


Figure 2. Configuration diagram (top view)

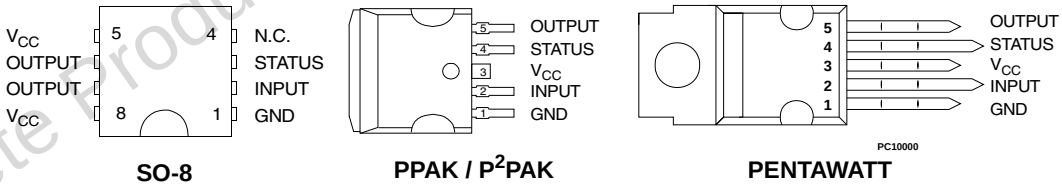
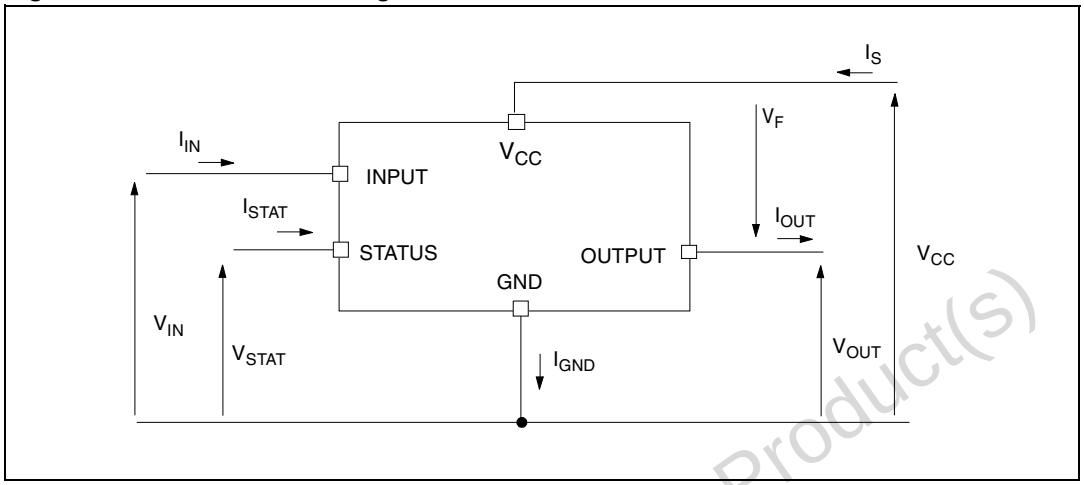


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		SO-8	PENTAWATT	P^2PAK	PPAK	
V_{CC}	DC supply voltage	41				V
$-V_{CC}$	Reverse DC supply voltage	-0.3				V
$-I_{gnd}$	DC reverse ground pin current	-200				mA
I_{OUT}	DC output current	Internally limited				A
$-I_{OUT}$	Reverse DC output current	-6				A
I_{IN}	DC input current	+/- 10				mA
I_{STAT}	DC Status current	+/- 10				mA
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – INPUT – STATUS – OUTPUT – V_{CC}	 4000 4000 5000 5000				 V V V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value				Unit
		SO-8	PENTAWATT	P^2PAK	PPAK	
E_{MAX}	Maximum switching energy ($L = 1.8$ mH; $R_L = 0\ \Omega$; $V_{bat} = 13.5$ V; $T_{jstart} = 150°C$; $I_L = 9$ A)	100				mJ
E_{MAX}	Maximum switching energy ($L = 2.46$ mH; $R_L = 0\ \Omega$; $V_{bat} = 13.5$ V; $T_{jstart} = 150°C$; $I_L = 9$ A)			138	138	mJ
P_{tot}	Power dissipation $T_C = 25°C$	4.2	60	60	60	W
T_j	Junction operating temperature	Internally limited				°C
T_c	Case operating temperature	-40 to 150				°C
T_{stg}	Storage temperature	-55 to 150				°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value				Unit
		S0-8	PENTAWATT	P^2PAK	PPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	-	2.1	2.1	2.1	°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead	30	-	-	-	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	93(1)	62.1	52.1(2)	77.1(2)	°C/W
		82(3)	62.1	37(4)	44(4)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5 cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 0.5 cm^2 of Cu (at least 35 µm thick). Horizontal mounting and no artificial air flow.
3. When mounted on a standard single-sided FR-4 board with 2 cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
4. When mounted on a standard single-sided FR-4 board with 6 cm^2 of Cu (at least 35 µm thick). Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 36 V; -40°C < T_j < 150°C, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On state resistance	I_{OUT} = 2 A; T_j = 25°C; V_{CC} > 8 V			60	mΩ
		I_{OUT} = 2 A; V_{CC} > 8 V			120	mΩ
I_S	Supply current	Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V		10	25	µA
		Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V; T_j = 25°C		10	20	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		2	3.5	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0 V; V_{OUT} = 3.5 V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C			3	µA

Table 6. Switching (V_{CC} = 13 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 6.5 Ω from V_{IN} rising edge to V_{OUT} = 1.3V		40		µs
$t_{d(off)}$	Turn-off delay time	R_L = 6.5 Ω from V_{IN} falling edge to V_{OUT} = 11.7 V		30		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 6.5 Ω from V_{OUT} = 1.3 V to V_{OUT}=10.4 V	See *Figure 21*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 6.5 Ω from V_{OUT} = 11.7 V to V_{OUT}=1.3 V	See *Figure 22*			V/µs

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{IH}	Input high level		3.25			V

Table 7. Input pin (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
V_{hyst}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		I_{IN} = -1 mA		-0.7		V

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$-I_{OUT}$ = 1.3 A; T_j = 150°C	—	—	0.6	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5 V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5 V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1 mA	6	6.8	8	V
		I_{STAT} = -1 mA		-0.7		V

Table 10. Protections(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
t_{SDL}	Status delay in overload condition	$T_j > T_{jsh}$			20	ms
I_{lim}	Current limitation	9 V < V_{CC} < 36 V	6	9	15	A
		5 V< V_{CC} < 36 V			15	A
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 2 A; V_{IN} = 0 V; L = 6 mH	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open-load ON-state detection threshold	V_{IN} = 5 V	50		200	mA
$t_{DOL(on)}$	Open-load ON-state detection delay	I_{OUT} = 0 A			200	µs

Table 11. Open-load detection (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load OFF-state voltage detection threshold	V_{IN} = 0 V	1.5		3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	µs

Figure 4. Status timings

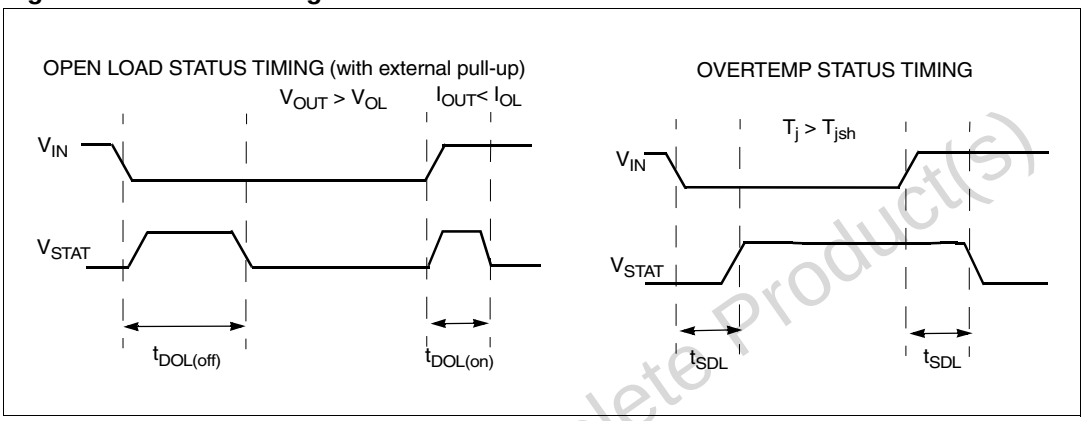


Figure 5. Switching time waveforms

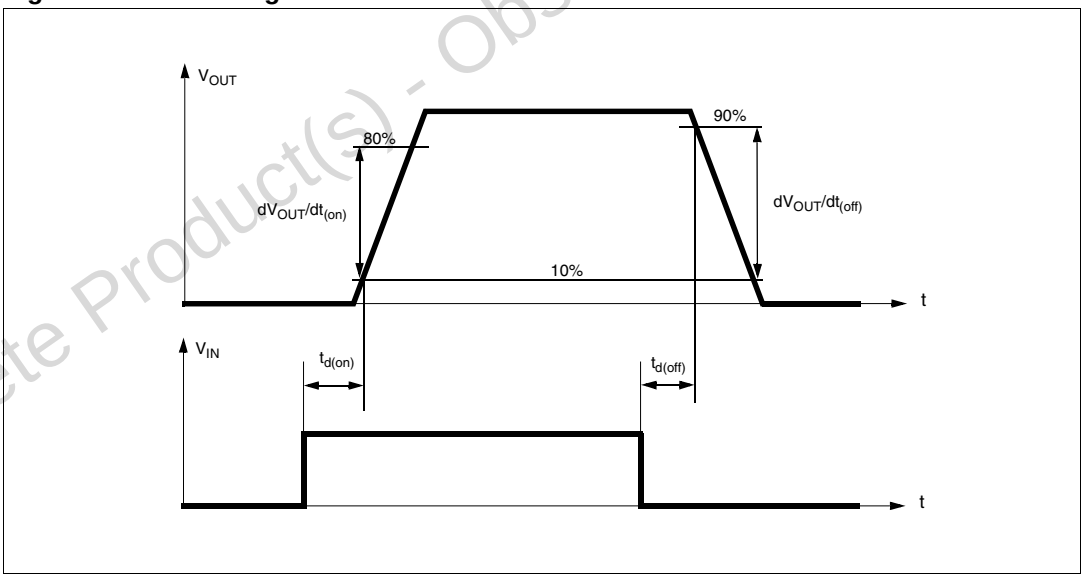


Table 12. Truth table

Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H
Output current < I_{OL}	L H	L H	H L

Table 13. Electrical transient requirements on V_{CC} pin (part 1)

ISO T/R 7637/1 Test pulse	Test levels				
	I	II	III	IV	Delays and impedance
1	- 25 V	- 50 V	- 75 V	- 100 V	2 ms 10 Ω
2	+ 25 V	+ 50 V	+ 75 V	+ 100 V	0.2 ms 10 Ω
3a	- 25 V	- 50 V	- 100 V	- 150 V	0.1 µs 50 Ω
3b	+ 25 V	+ 50 V	+ 75 V	+ 100 V	0.1 µs 50 Ω
4	- 4 V	- 5 V	- 6 V	- 7 V	100 ms, 0.01 Ω
5	+ 26.5 V	+ 46.5 V	+ 66.5 V	+ 86.5 V	400 ms, 2 Ω

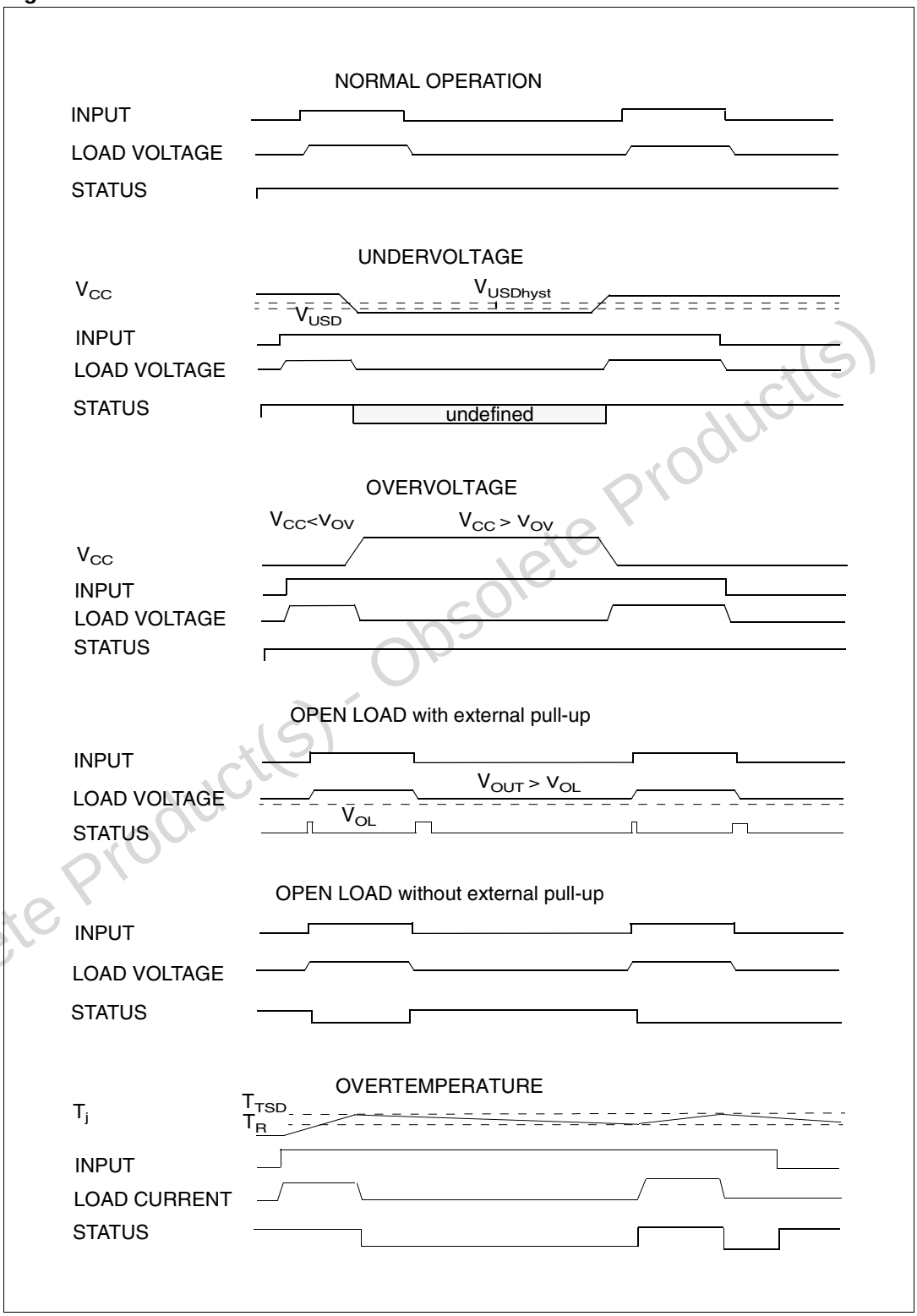
Table 14. Electrical transient requirements on V_{CC} pin (part 2)

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 15. Electrical transient requirements on V_{CC} pin (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

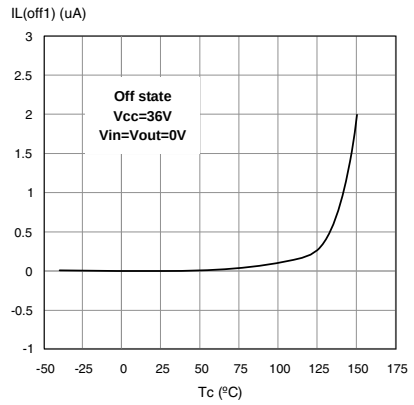


Figure 8. High level input current

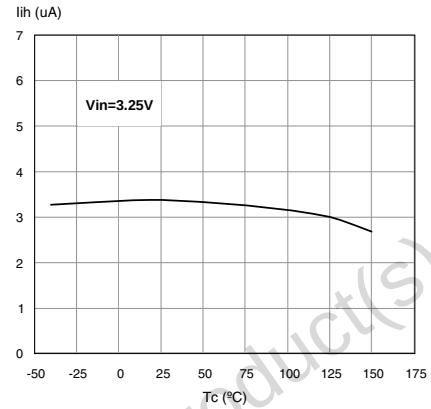


Figure 9. Input clamp voltage

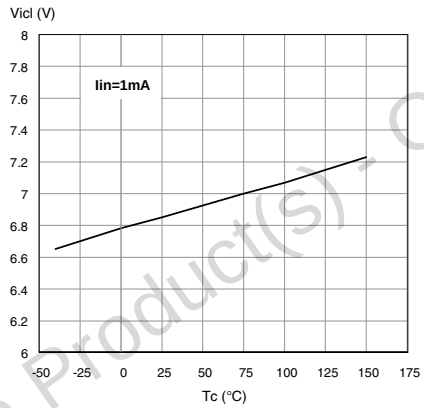


Figure 10. Status leakage current

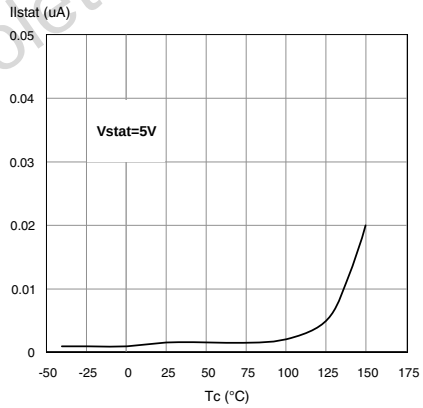


Figure 11. Status low output voltage

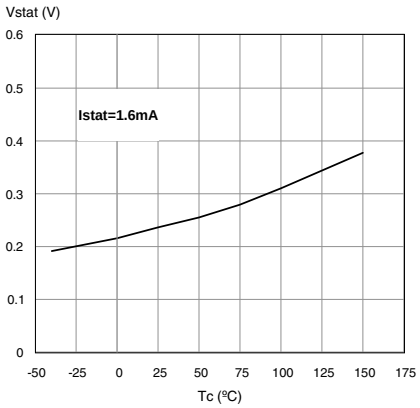


Figure 12. Status clamp voltage

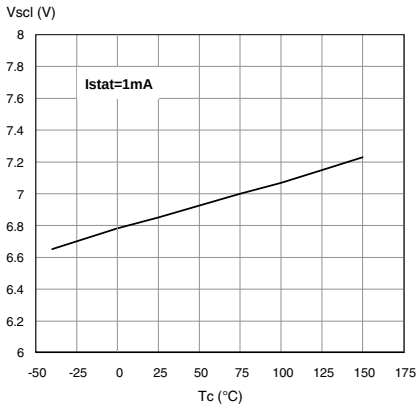


Figure 13. On-state resistance vs T_{case}

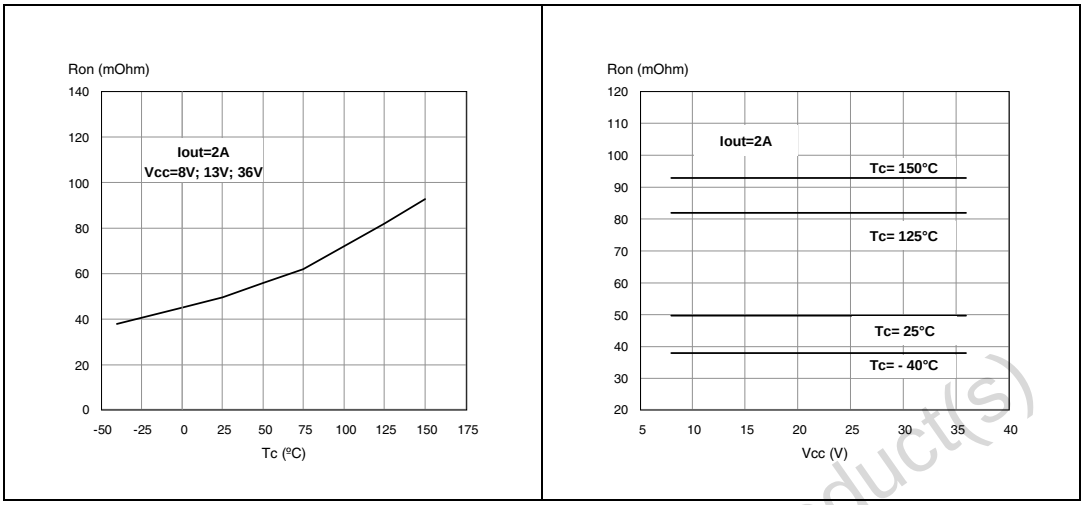


Figure 14. On-state resistance vs V_{CC}

Figure 15. Open-load On-state detection threshold

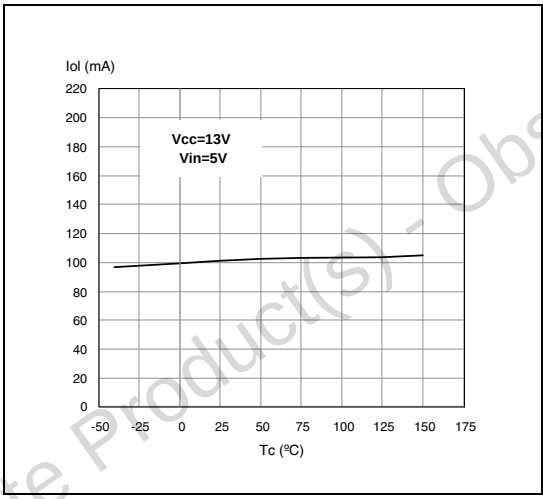


Figure 16. Input high level

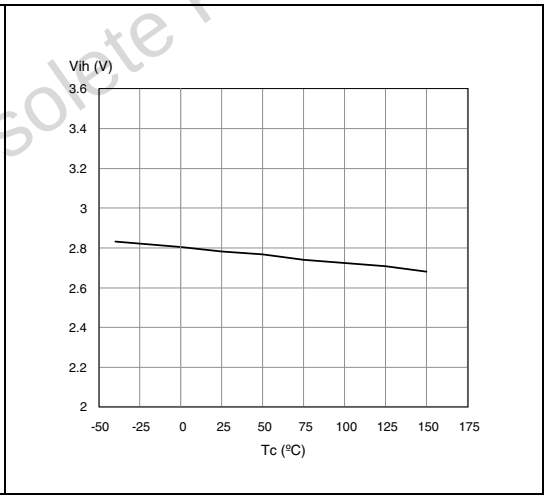


Figure 17. Input low level

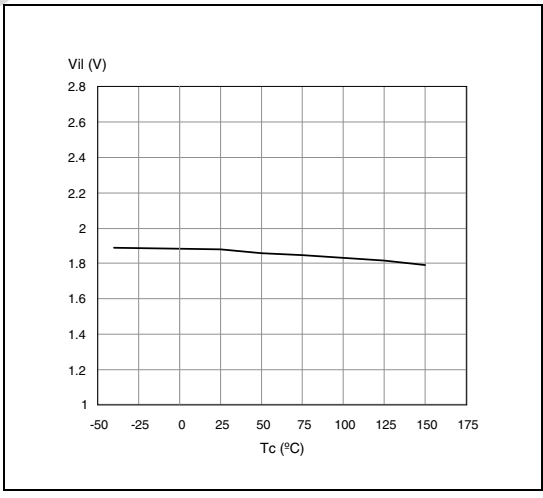


Figure 18. Input hysteresis voltage

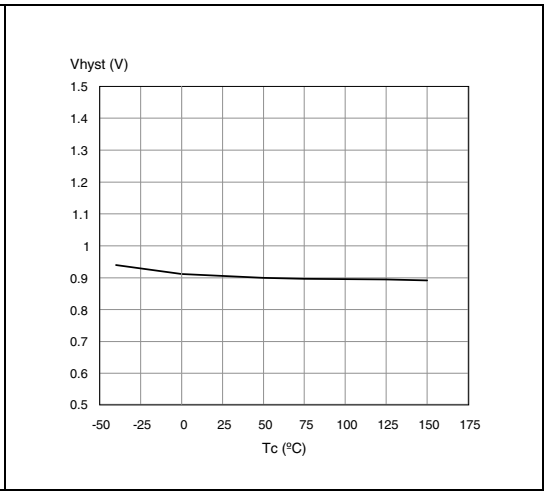


Figure 19. Overvoltage shutdown

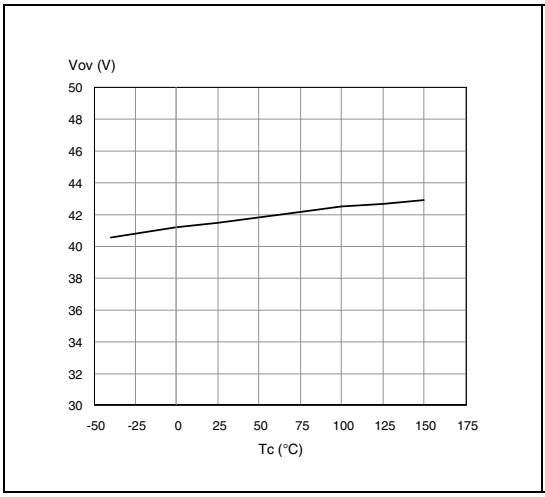


Figure 20. Open-load Off-state voltage detection threshold

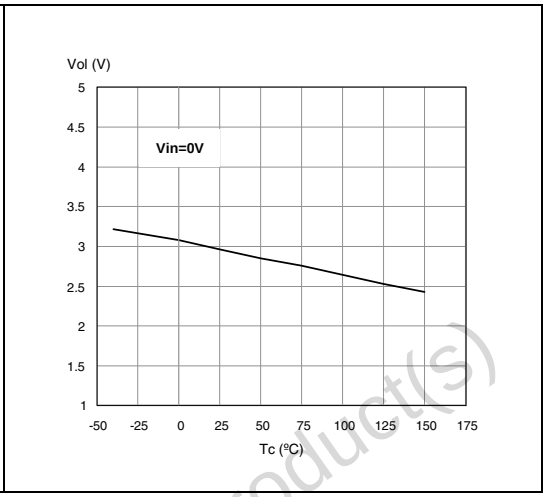


Figure 21. Turn-on voltage slope

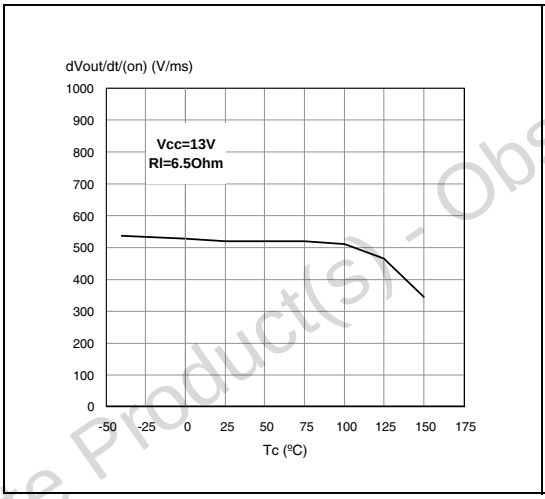


Figure 22. Turn-off voltage slope

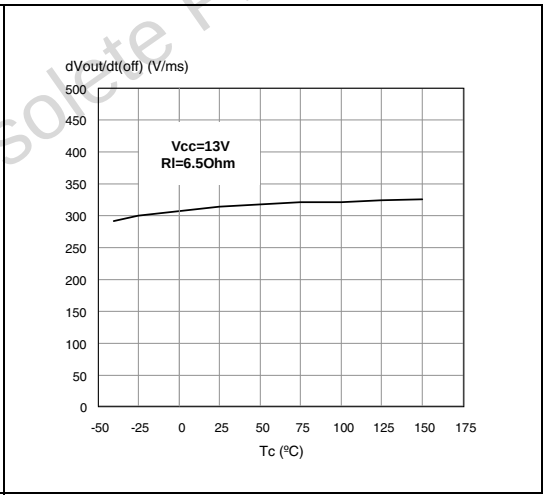


Figure 23. I_{lim} vs T_{case}

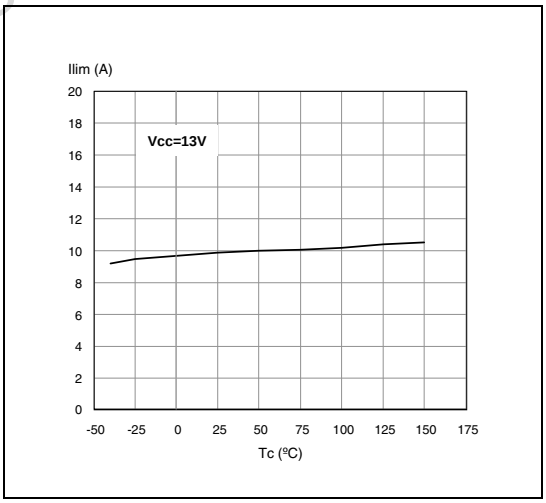
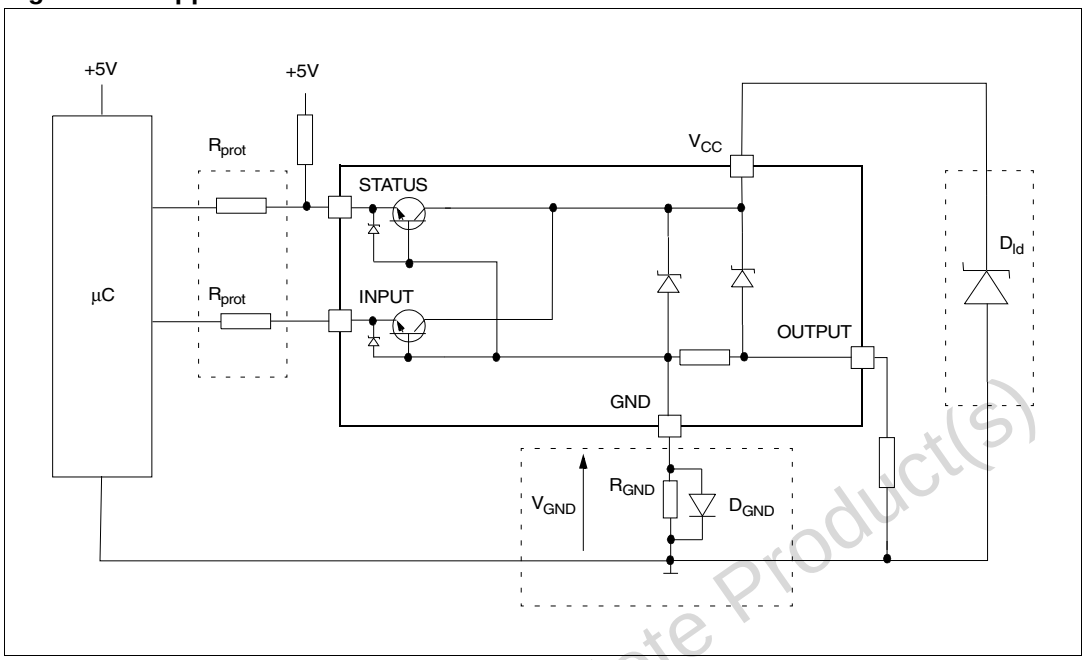


Figure 24. Application schematic



2.5 GND protection network against reverse battery

2.5.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to size the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D = (-V_{CC})^2 / R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

2.5.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

The safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

2.6 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

2.7 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended values: R_{prot} =10kΩ .

2.8 Open-load detection in Off-state

Off-state open-load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

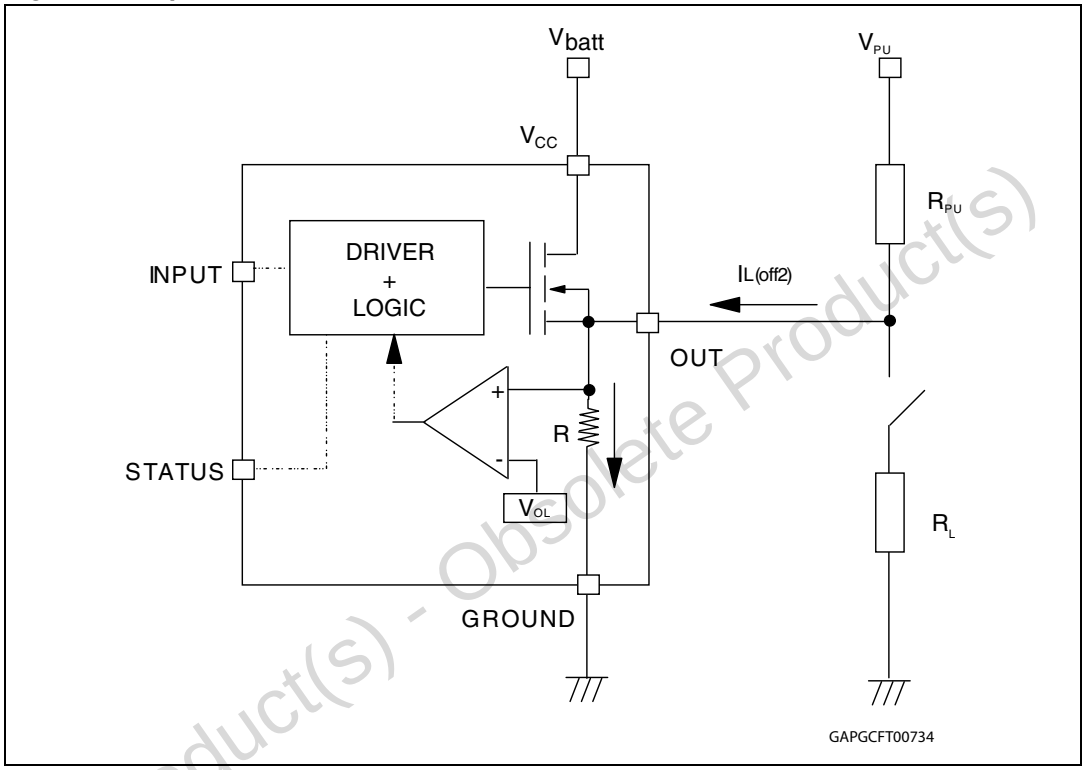
The external resistor has to be selected according to the following requirements:

1. No false open-load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT}= (V_{PU} / (R_L+R_{PU}))\ R_L < V_{Olmin}$.
2. No misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU} < (V_{PU} – V_{OLmax}) / I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

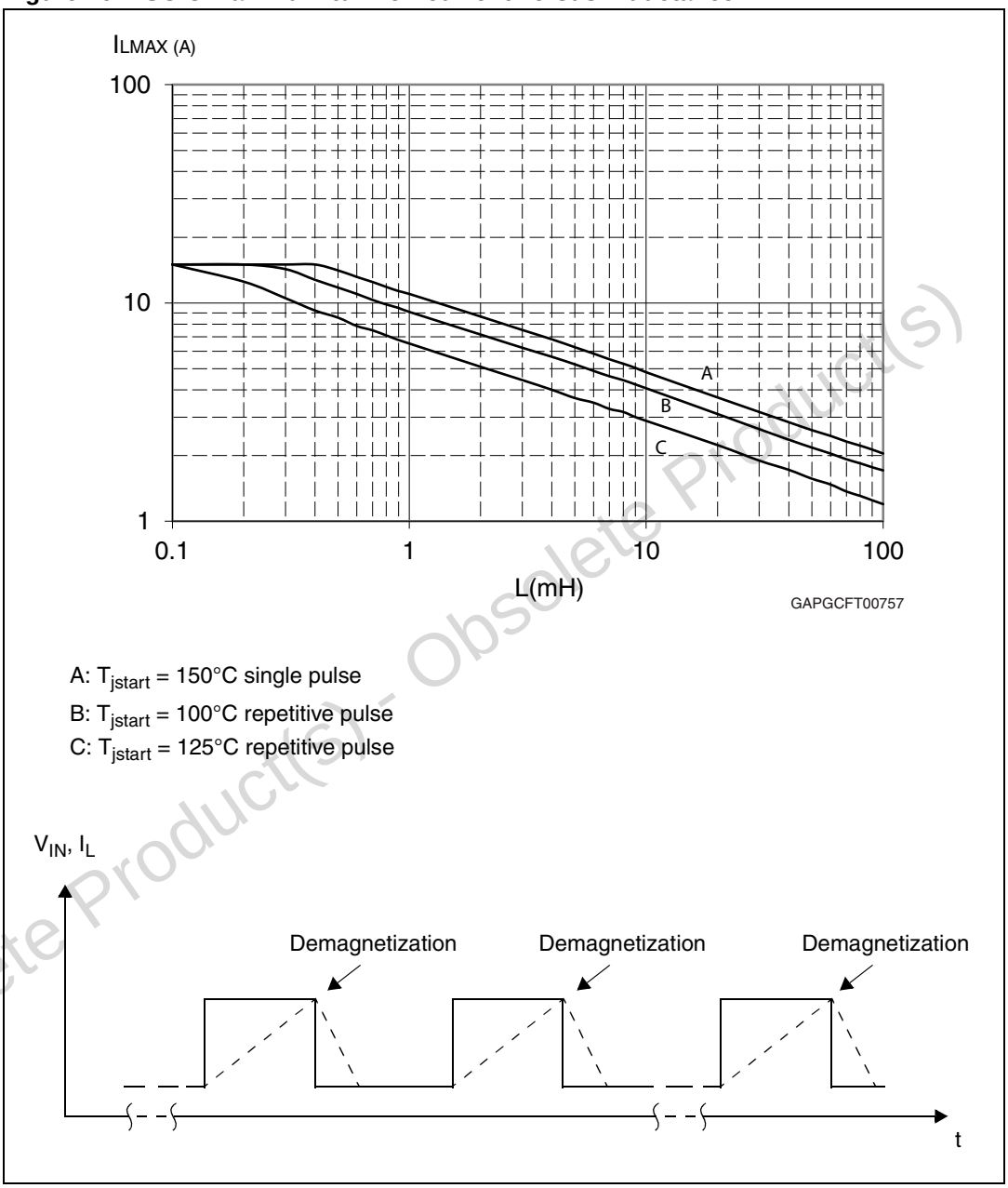
The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the electrical characteristics section.

Figure 25. Open-load detection in off-state



2.9 SO-8 maximum demagnetization energy (V_{CC} = 13.5V)

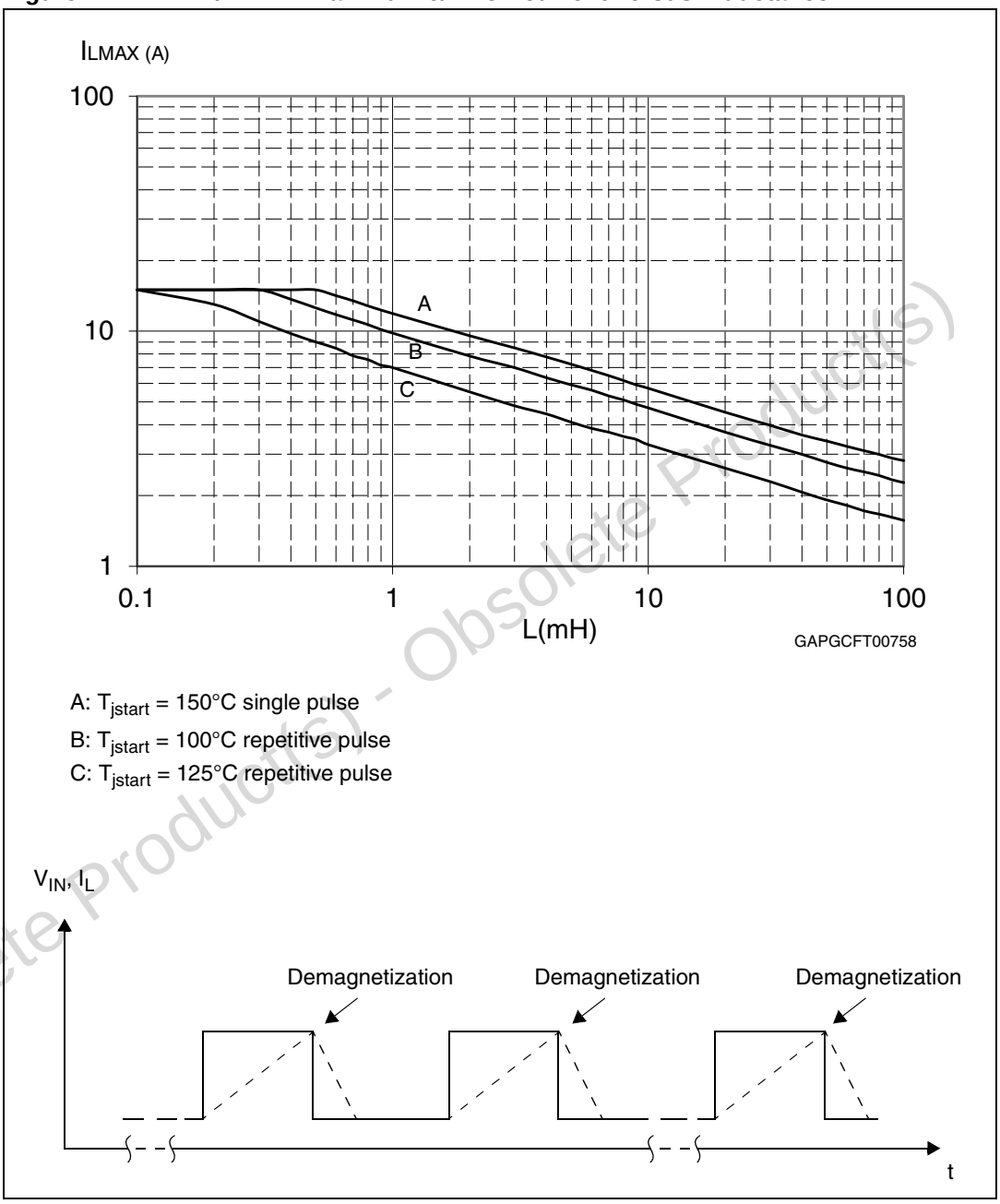
Figure 26. SO-8 maximum turn-off current versus inductance



1. *Values are generated with R_L = 0 Ω.In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.*

2.10 PPAK/P^{2}PAK maximum demagnetization energy (V_{CC} = 13.5V)

Figure 27. PPAK /P^{2}PAK maximum turn-off current versus inductance

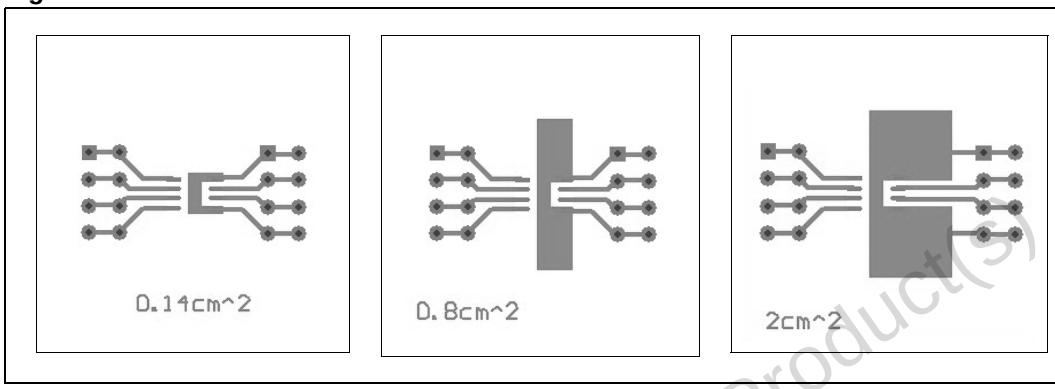


1. *Values are generated with R_L = 0 Ω.In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.*

3 Package and PCB thermal data

3.1 SO-8 thermal data

Figure 28. SO-8 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm,PCB thickness = 2 mm, Cu thickness = 35 µm , Copper areas: 0.14 cm^2, 0.8 cm^2, 2 cm^2).

Figure 29. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

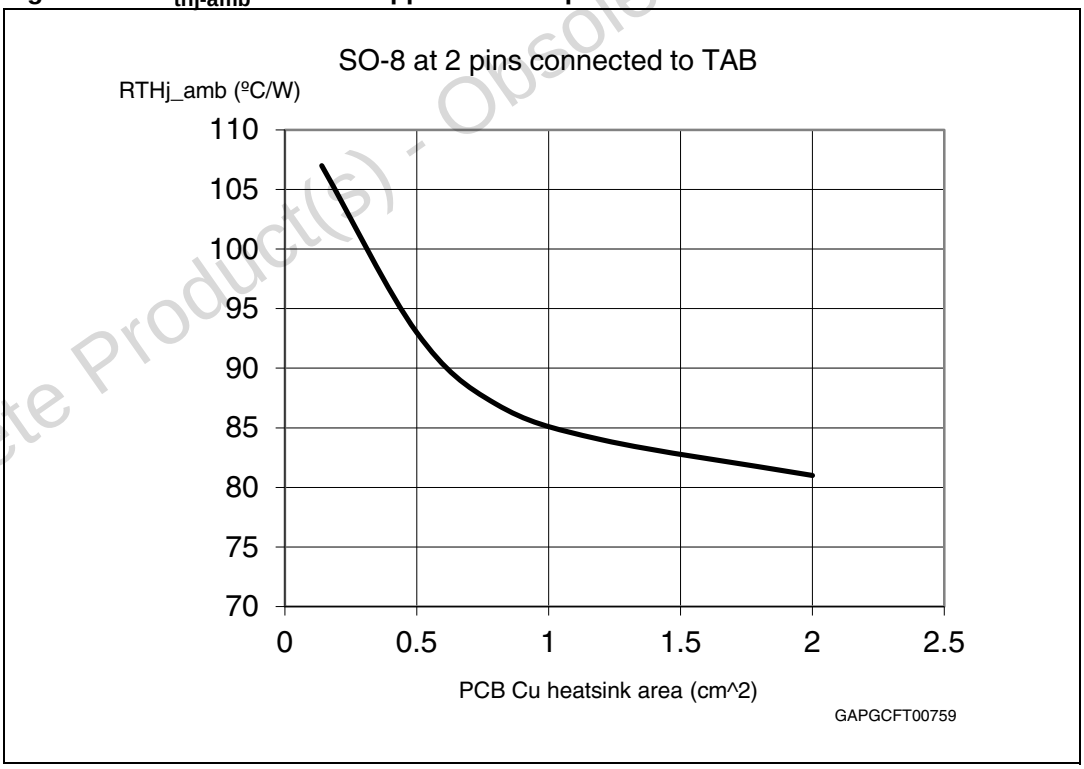
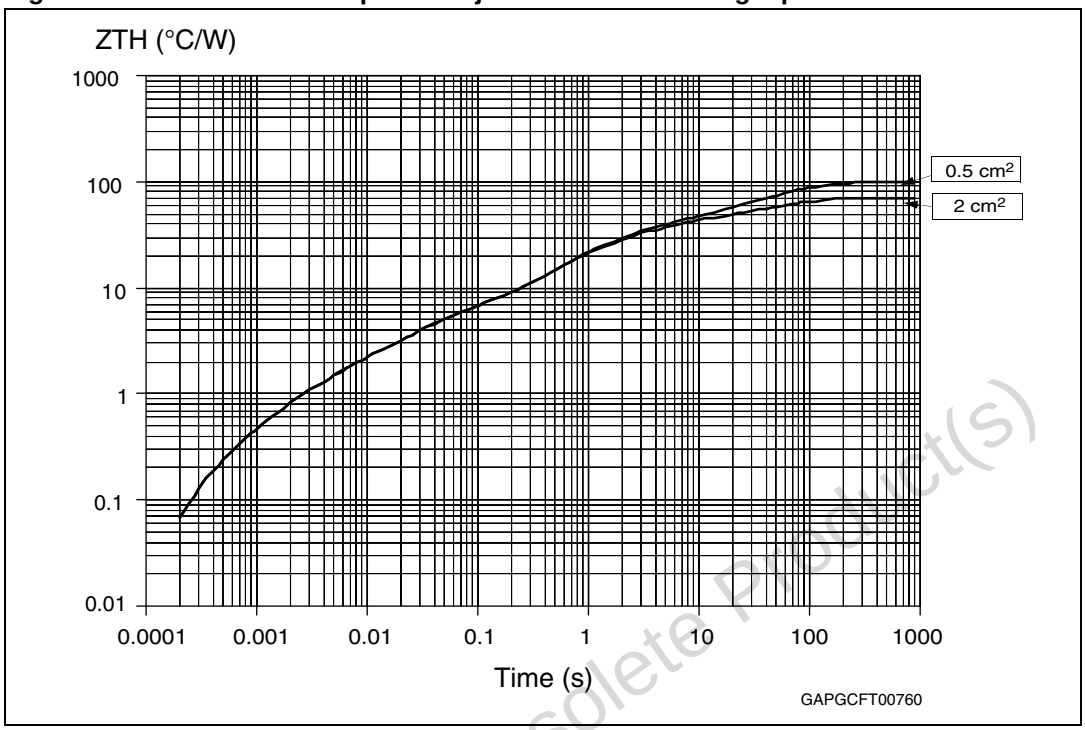


Figure 30. SO-8 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 31. Thermal fitting model of a single channel

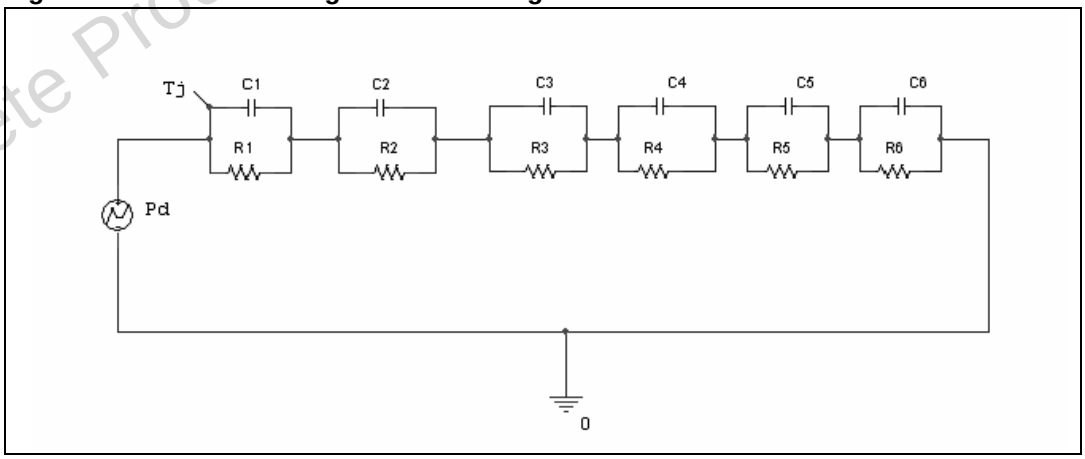
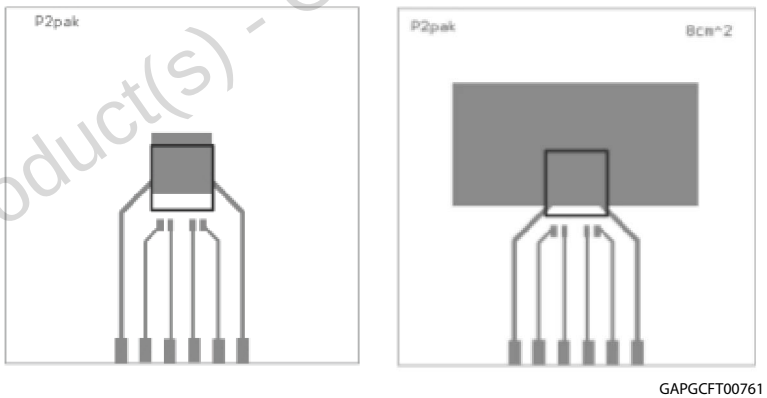


Table 16. Thermal parameter

Area/island (cm^2)	0.5	2
R1 (°C/W)	0.05	
R2 (°C/W)	0.8	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.006	
C2 (W·s/°C)	0.0026	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

3.2 P^2PAK thermal data

Figure 32. P^2PAK PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness = 35 µm , Copper areas: 0.97 cm^2, 8 cm^2).

Figure 33. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

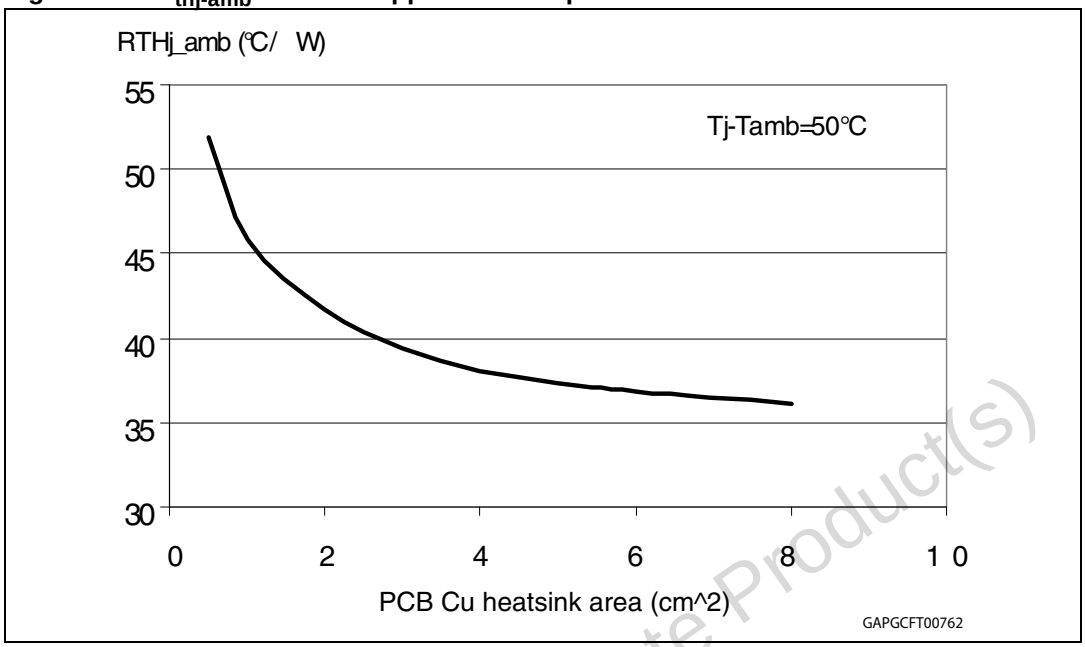
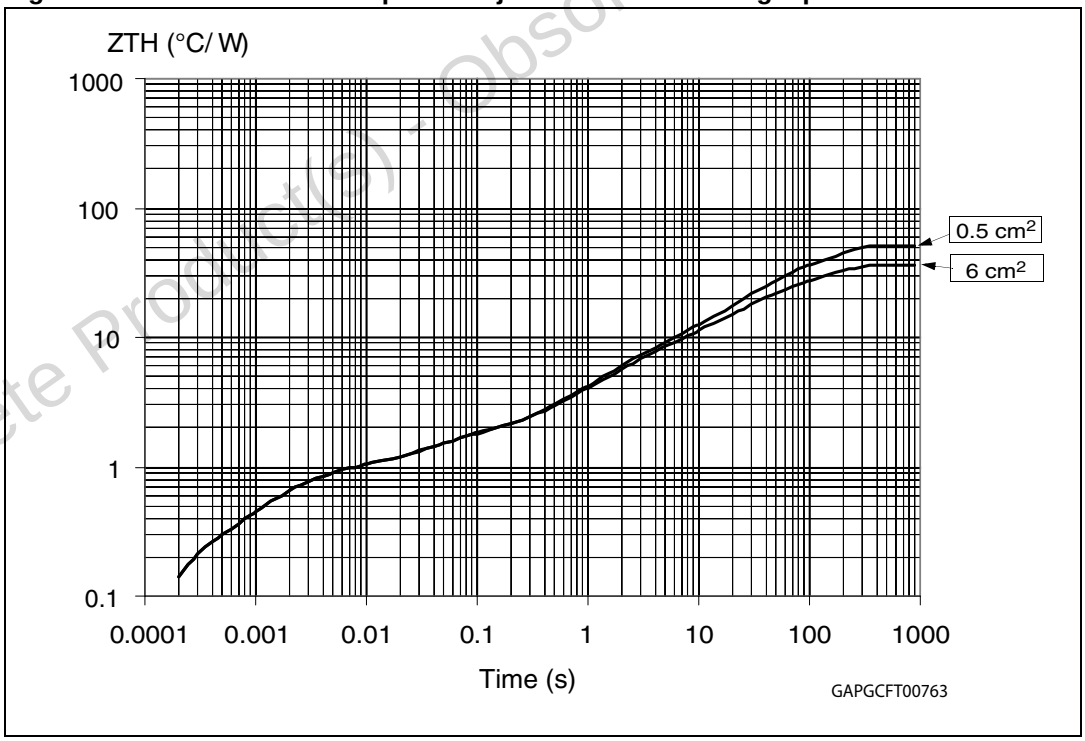


Figure 34. P²PAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 35. Thermal fitting model of a single channel

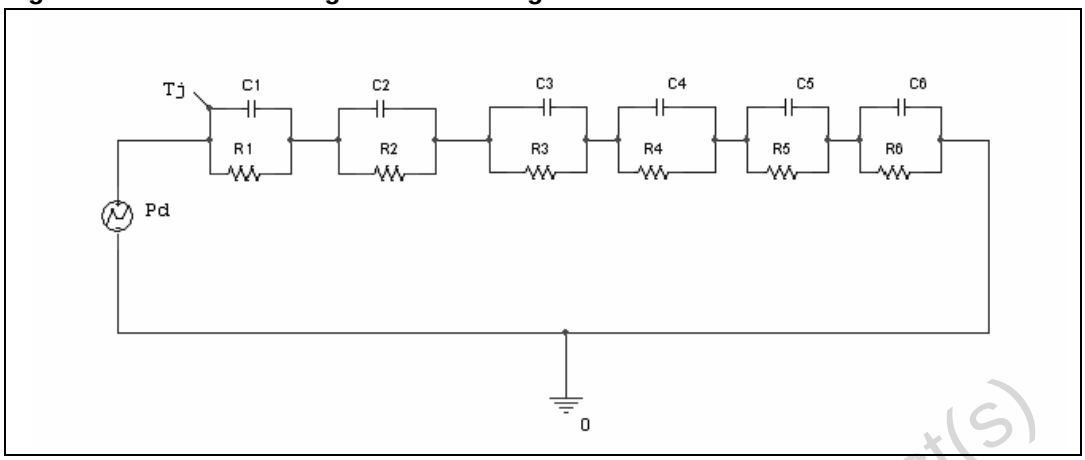
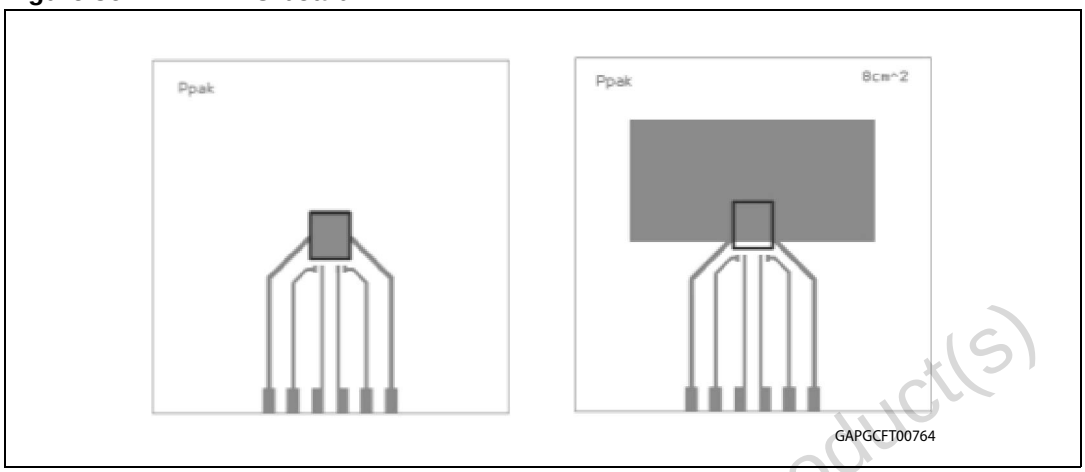


Table 17. Thermal parameter

Area/island (cm^2)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	0.7	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0006	
C2 (W·s/°C)	0.0025	
C3 (W·s/°C)	0.055	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

3.3 PPAK thermal data

Figure 36. PPAK PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness = 35 µm , Copper areas: 0.44 cm^2, 8 cm^2).

Figure 37. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

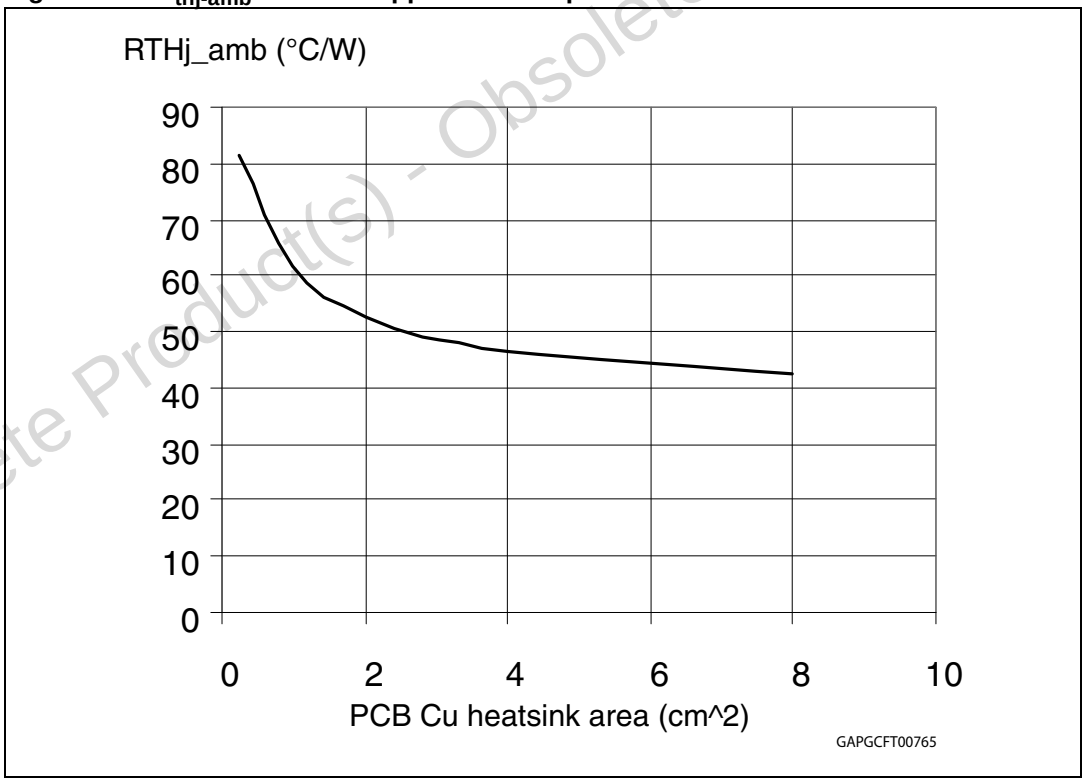
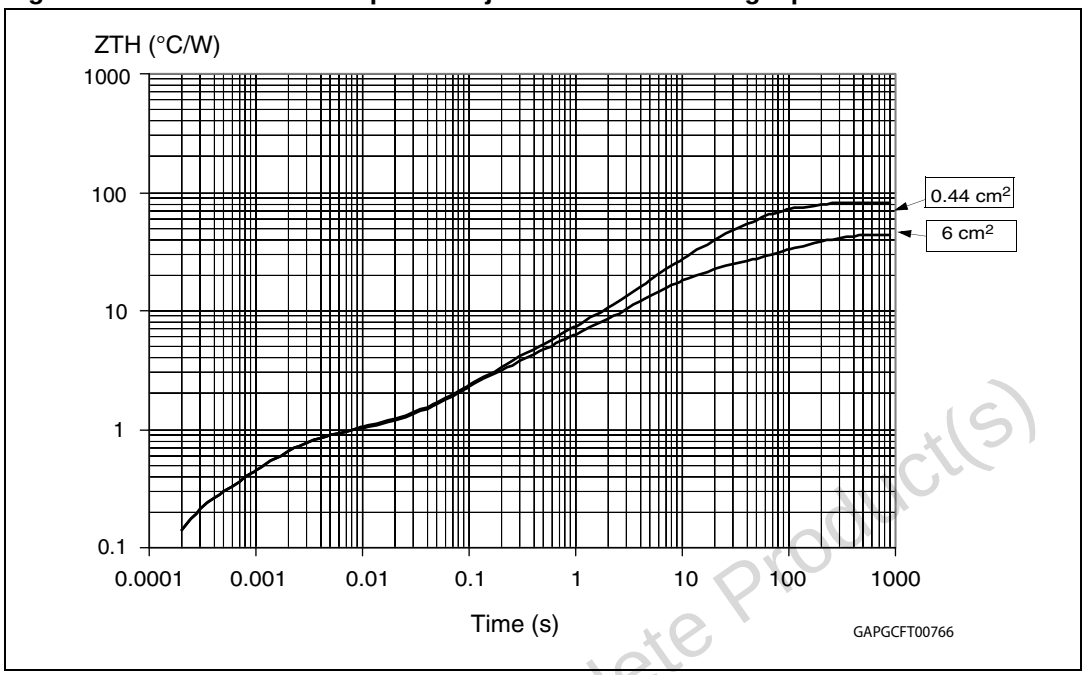


Figure 38. PPAK thermal impedance junction ambient single pulse



Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 39. Thermal fitting model of a single channel

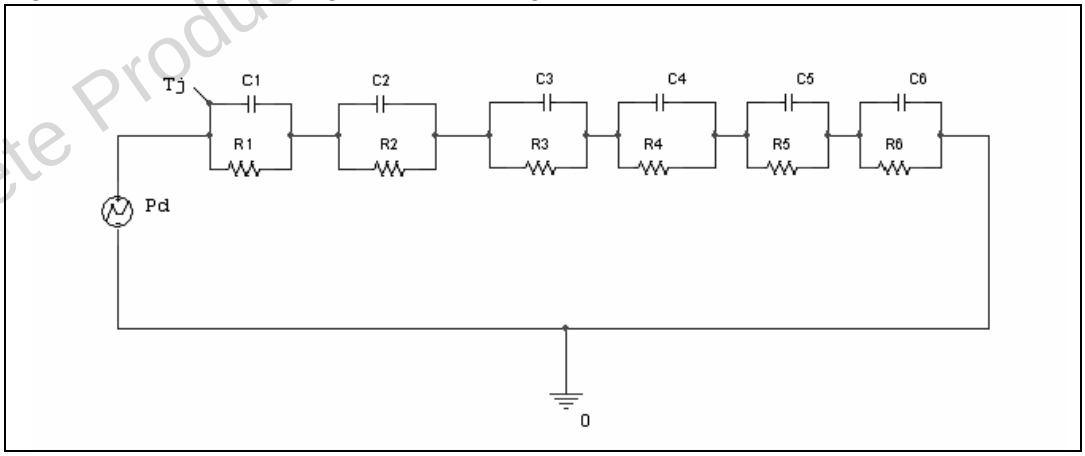


Table 18. Thermal parameter

Area/island (cm^2)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	1.6	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.0006	
C2 (W·s/°C)	0.0025	
C3 (W·s/°C)	0.08	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 SO-8 package information

Figure 40. SO-8 package dimensions

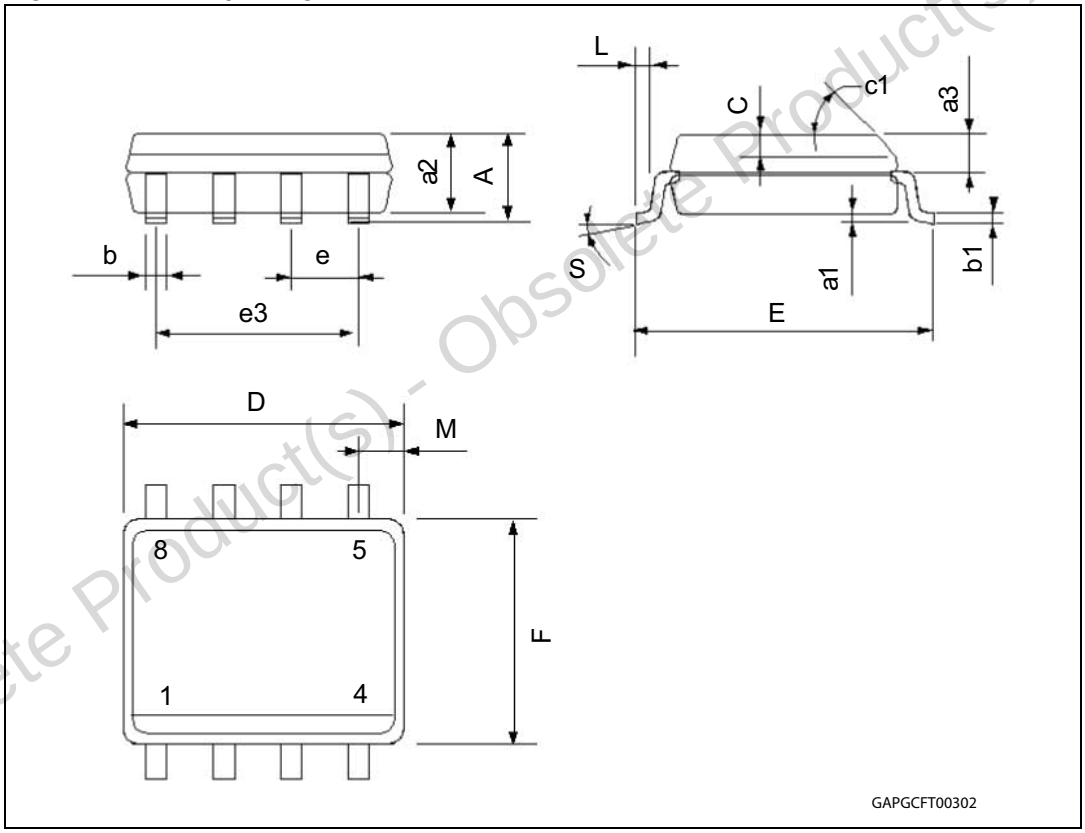


Table 19. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

4.3 PENTAWATT mechanical data

Figure 41. PENTAWATT package dimensions

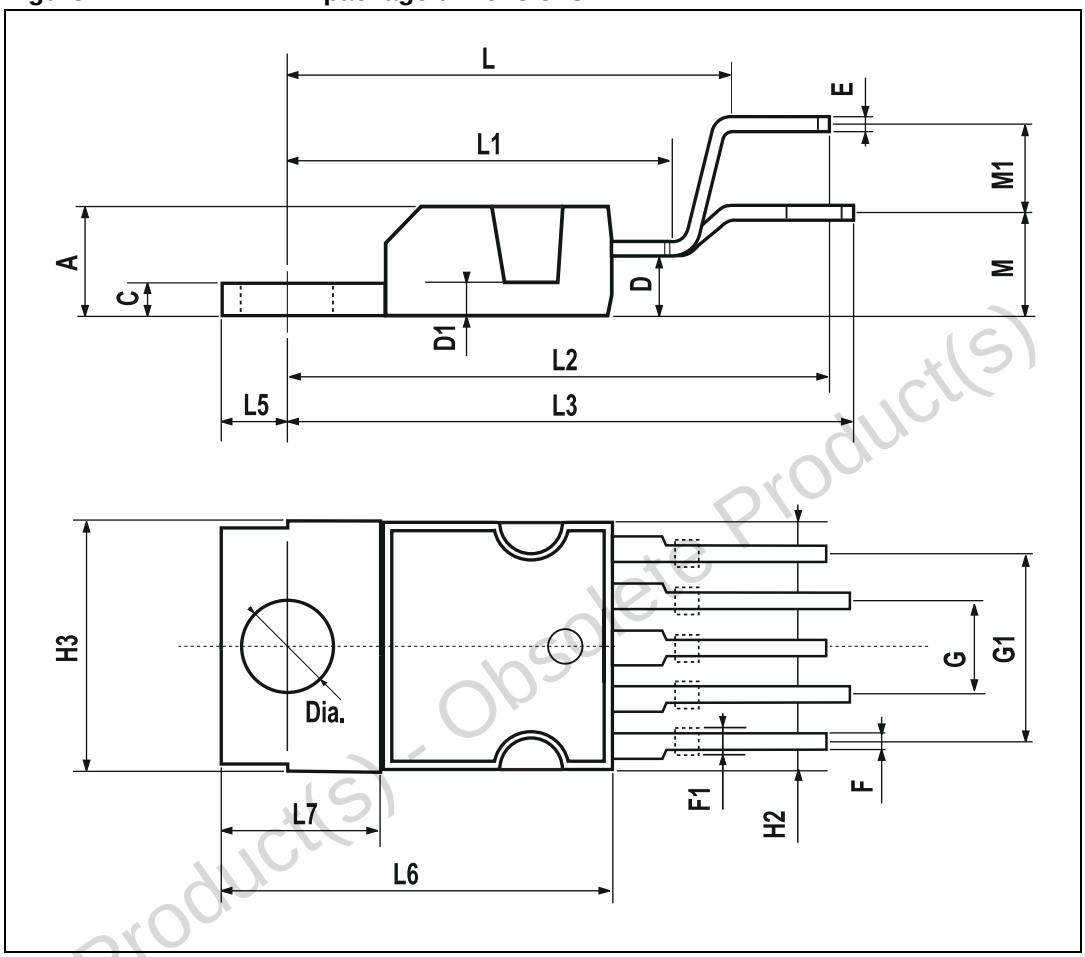


Table 20. PENTAWATT mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.8
C			1.37
D	2.4		2.8
D1	1.2		1.35
E	0.35		0.55
F	0.8		1.05
F1	1		1.4
G	3.2	3.4	3.6

Table 20. PENTAWATT mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
G1	6.6	6.8	7
H2			10.4
H3	10.05		10.4
L		17.85	
L1		15.75	
L2		21.4	
L3		22.5	
L5	2.6		3
L6	15.1		15.8
L7	6		6.6
M		4.5	
M1		4	
Diam.	3.65		3.85

4.4 P²PAK mechanical data

Figure 42. P²PAK package dimensions

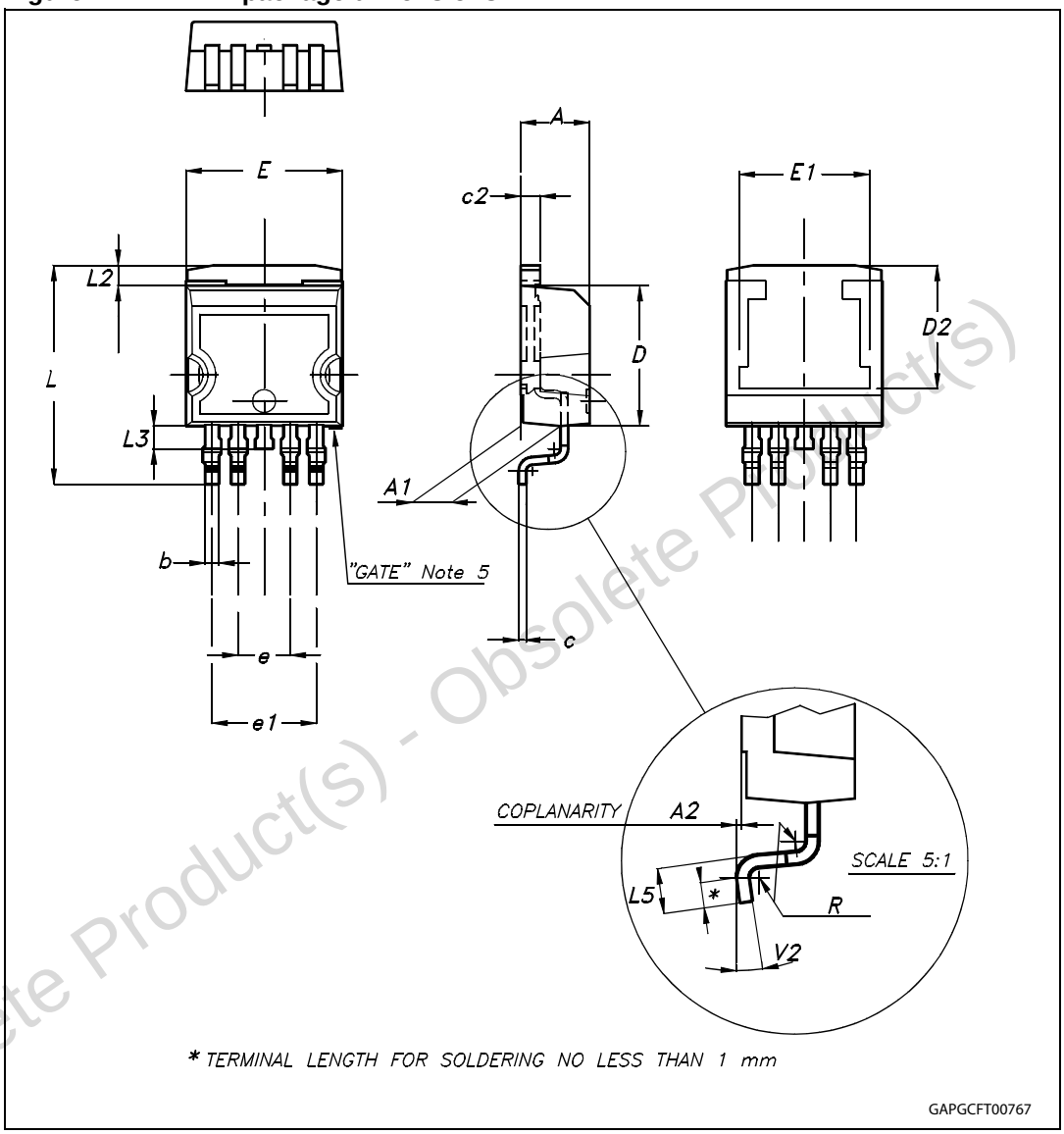


Table 21. P^2PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0º		8º
Package weight	1.40 Gr (typ)		

4.5 PPAK mechanical data

Figure 43. PPAK package dimensions

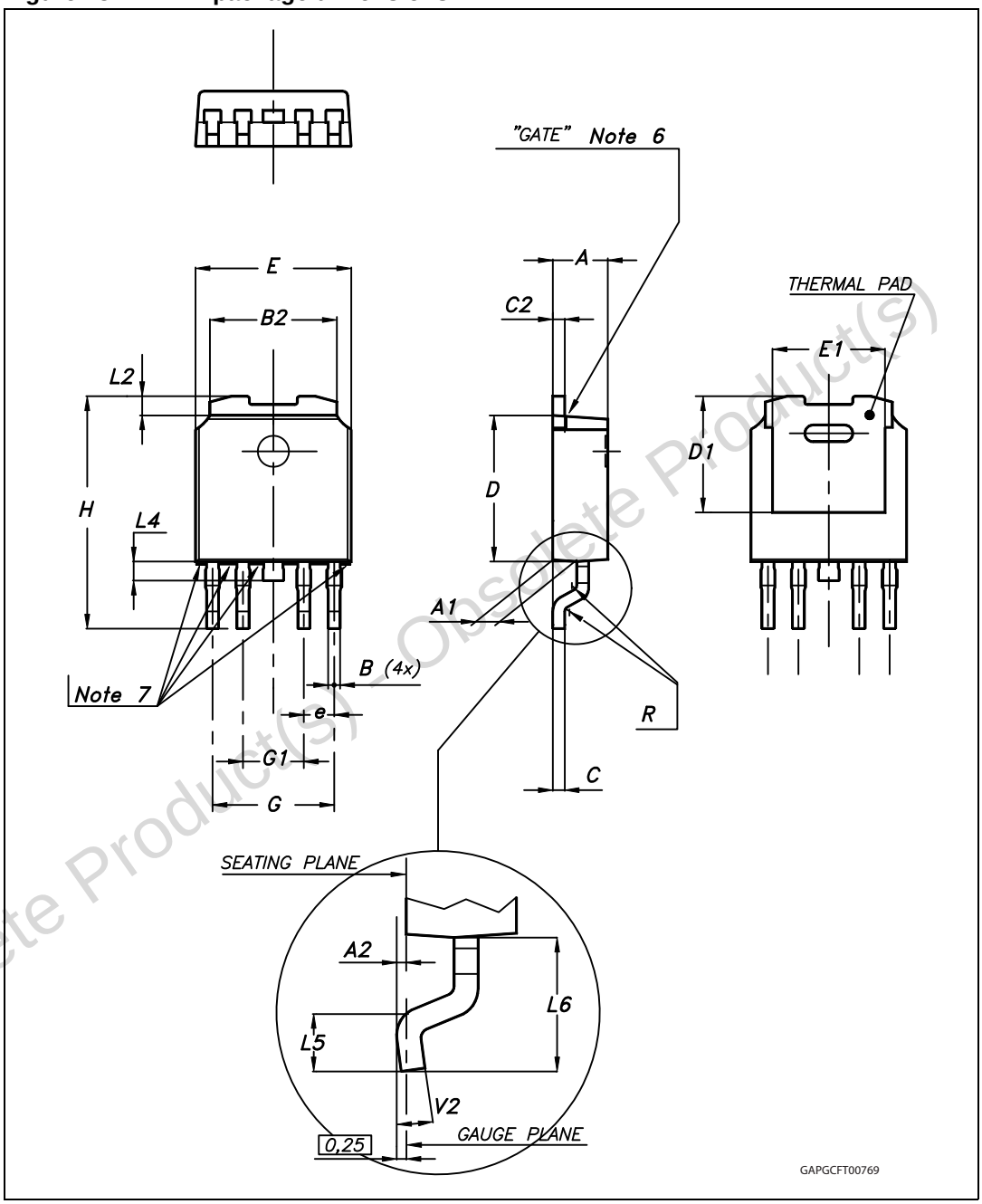


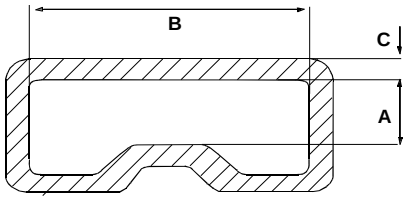
Table 22. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
L5	1		—
L6		2.80	
R		0.2	
V2	0°		8°
Package weight	Gr. 0.3		

4.6 SO-8 packing information

The devices can be packed in tube or tape and reel shipments (see the *Table 1: Device summary*).

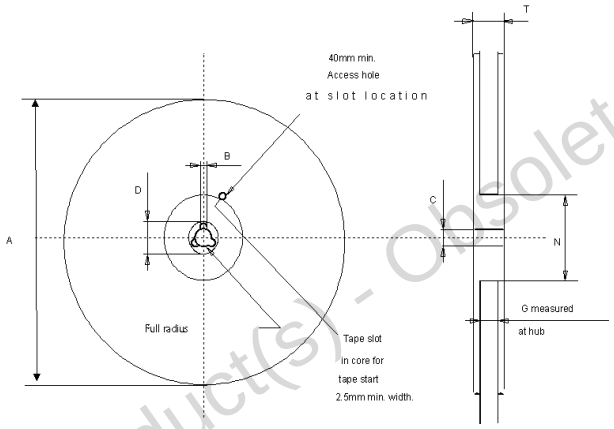
Figure 44. SO-8 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

Figure 45. SO-8 tape and reel shipment (suffix “TR”)



Reel dimensions

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

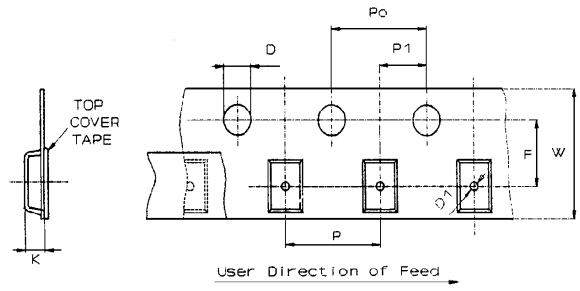
All dimensions are in mm.

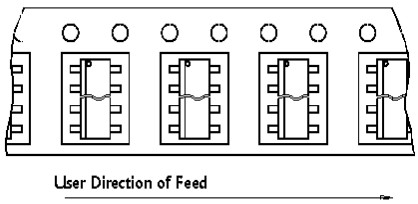
Tape dimensions

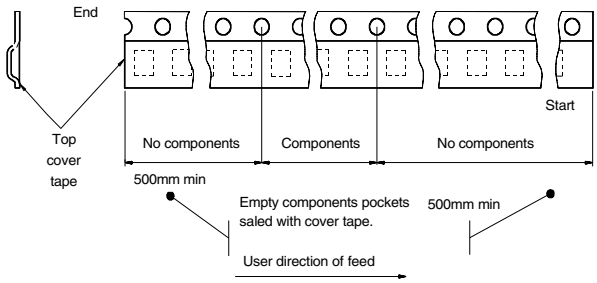
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.



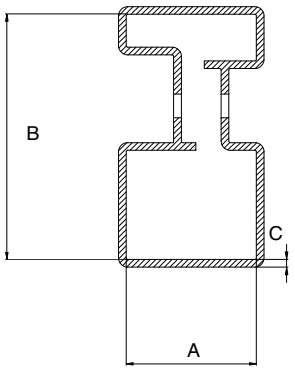




4.7 PENTAWATT packing information

The devices can be packed in tube or tape and reel shipments (see the *Table 1: Device summary*).

Figure 46. PENTAWATT tube shipment (no suffix)



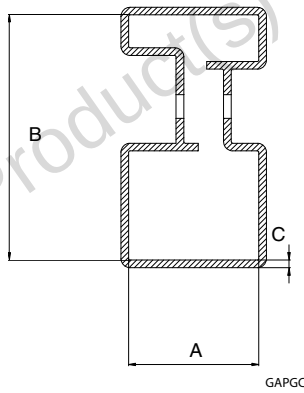
Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

4.8 P^{2}PAK packing information

The devices can be packed in tube or tape and reel shipments (see the *Table 1: Device summary*).

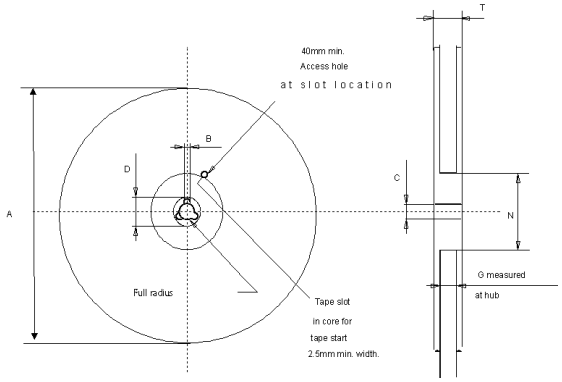
Figure 47. P^{2}PAK tube shipment (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

Figure 48. P²PAK tape and reel (suffix “13TR”)



REEL DIMENSIONS

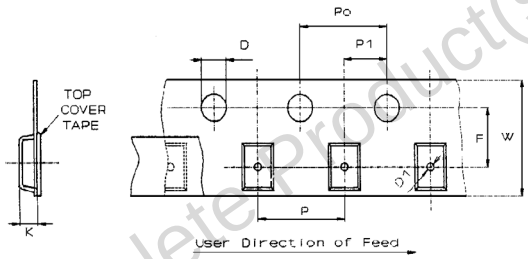
All dimensions are in mm.

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

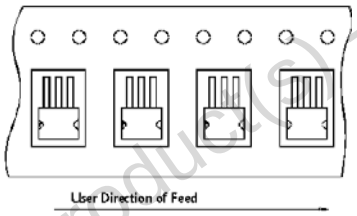
TAPE DIMENSIONS

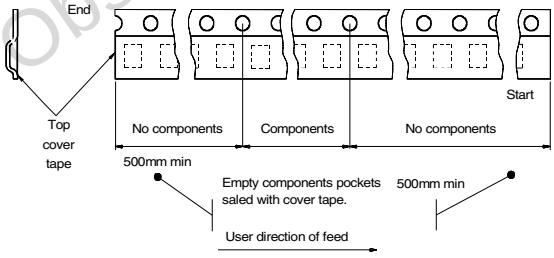
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2



All dimensions are in mm.





4.9 PPAK packing information

The devices can be packed in tube or tape and reel shipments (see the *Table 1: Device summary*).

Figure 49. PPAK suggested pad layout

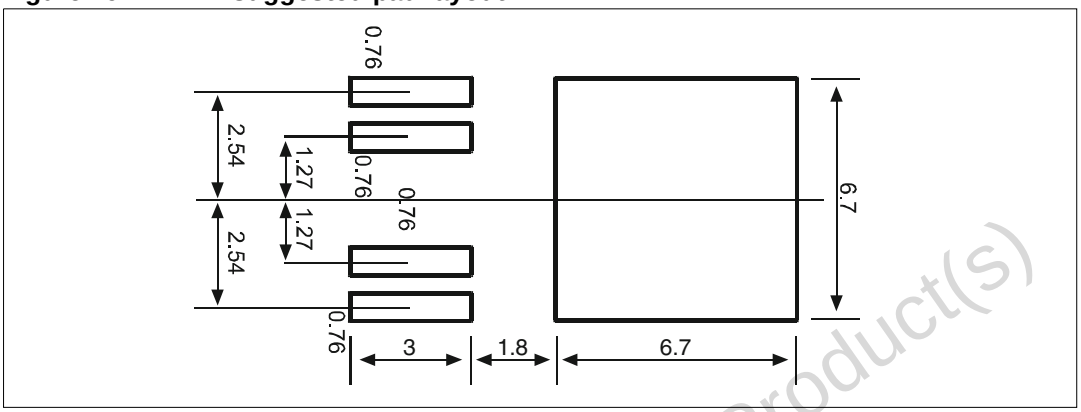
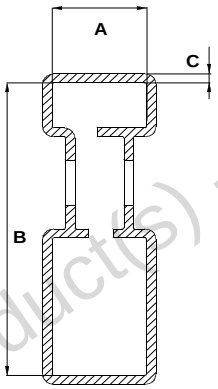


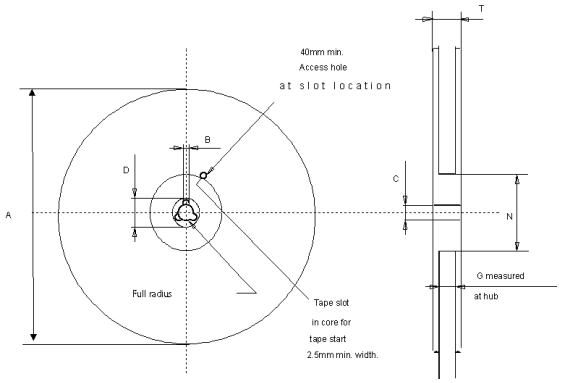
Figure 50. PPAK tube shipment (no suffix)



Base Q.ty	75
Bulk Q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

Figure 51. PPAK tape and reel (suffix “13TR”)



REEL DIMENSIONS

All dimensions are in mm.

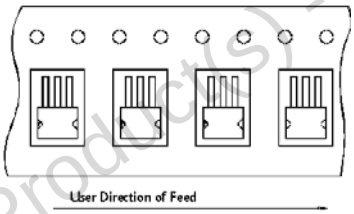
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

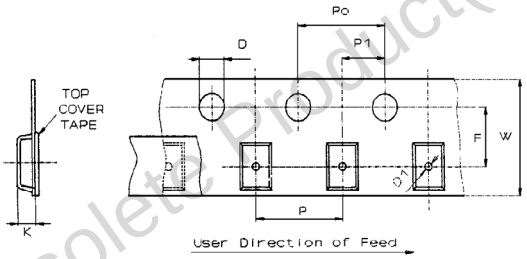
TAPE DIMENSIONS

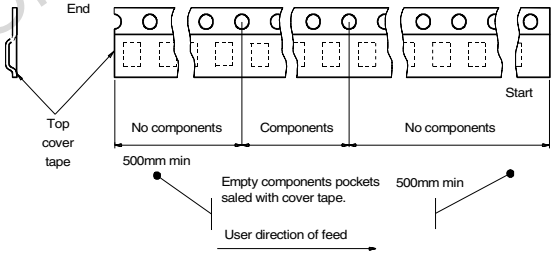
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	2.75
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







5 Revision history

Table 23. Document revision history

Date	Revision	Changes
21-Jun-2004	1	Initial release.
03-May-2006	2	Current and voltage convention update (page 2). Configuration diagram (top view) & suggested connections for unused and n.c. pins: insertion (page 2). 6cm2 Cu condition insertion in thermal data table (page 3). V_{CC} - output diode section update (page 4). Revision history table insertion (page 30). Disclaimers update (page 31).
24-Nov-2008	3	Document reformatted and restructured. Added content, list of figures and tables. Added *ECOPACK® packages* information. Updated *Figure 48.: P²PAK tape and reel (suffix "13TR")*: – changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.
18-May-2012	4	Updated *Section 4.5: PPAK mechanical data*

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