

RJM0603JSC

Silicon N/P Channel Power MOS FET (6 in 1 Type)
High Speed Power Switching

R07DS0339EJ0501

Rev.5.01

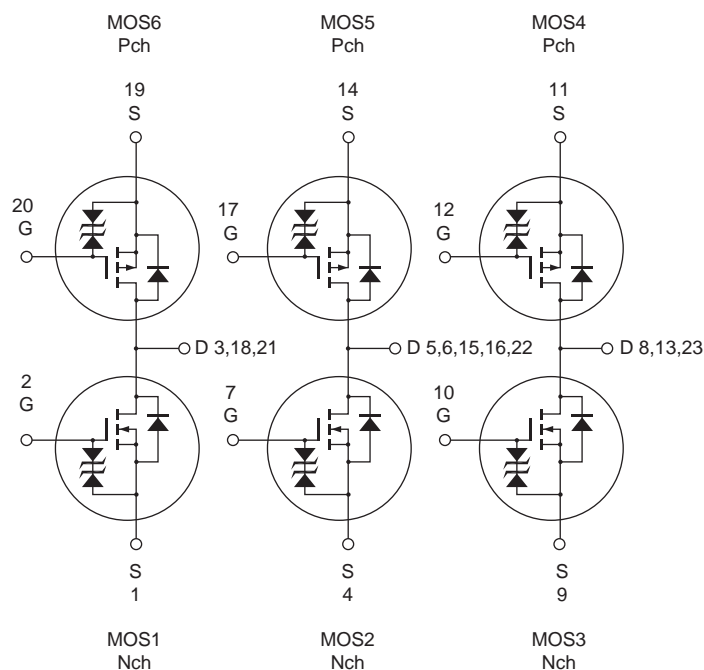
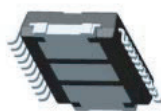
Jul 22, 2011

Features

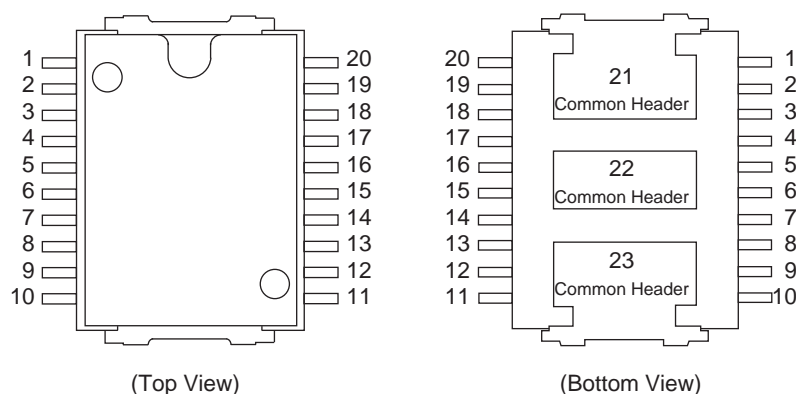
- For Automotive applications
- AEC-Q101 compliant
- N/P Channel MOS FET (6 in 1 Type). High density mounting
- Low on-resistance
- Capable of 4.5 V gate drive

Outline

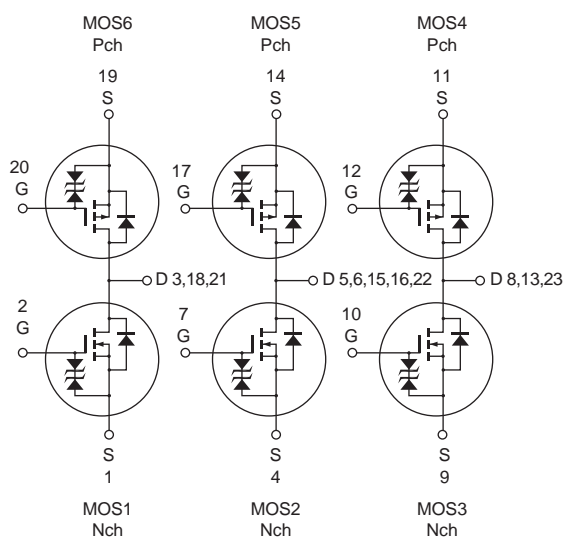
RENESAS Package Code: PRSP0020DF-A
(Package Name: HSOP-20)



Pin Arrangement



No.		
1	MOS1	Source
2	MOS1	Gate
3, 18	MOS1, 6	Drain
4	MOS2	Source
5, 6, 15, 16	MOS2, 5	Drain
7	MOS2	Gate
8, 13	MOS3, 4	Drain
9	MOS3	Source
10	MOS3	Gate
11	MOS4	Source
12	MOS4	Gate
14	MOS5	Source
17	MOS5	Gate
19	MOS6	Source
20	MOS6	Gate
21	MOS1, 6	Drain (Header)
22	MOS2, 5	Drain (Header)
23	MOS3, 4	Drain (Header)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		MOS1, 2, 3 (Nch)	MOS4, 5, 6 (Pch)	
Drain to source voltage	V _{DSS}	60	-60	V
Gate to source voltage	V _{GSS}	+20 / -5	-20 / +5	V
Drain current	I _D	20	-20	A
Drain peak current	I _D (pulse) ^{Note1}	80	-80	A
Channel dissipation	P _{ch} ^{Note2}	54	54	W
Avalanche current	I _{AP} ^{Note3}	20	20	A
Avalanche energy	E _{AR} ^{Note3}	34	34	mJ
Channel temperature	T _{ch} ^{Note4}	175	175	°C
Storage temperature	T _{stg}	-55 to +150	-55 to +150	°C

- Notes: 1. PW ≤ 10μs duty cycle ≤ 1%
 2. 1 Drive Operation ; Value at T_c = 25°C
 3. Value at T_{ch} = 25°C, R_g ≥ 50 Ω
 4. AEC-Q101 compliant

Thermal Impedance Characteristics

- Channel to case thermal impedance θ_{ch-c}: 2.78°C/W

Electrical Characteristics

• MOS1, MOS2, MOS3 (N Channel)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60 V, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = +20 V / -5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 V, I_D = 1 mA$
Static drain to source on state resistance	$R_{DS(on)}$	—	16	20	$m\Omega$	$I_D = 10 A, V_{GS} = 10 V$ ^{Note5}
		—	21	32	$m\Omega$	$I_D = 10 A, V_{GS} = 4.5 V$ ^{Note5}
Input capacitance	C_{iss}	—	2600	—	pF	$V_{DS} = 10 V, V_{GS} = 0,$ $f = 1 MHz$
Output capacitance	C_{oss}	—	290	—	pF	
Reverse transfer capacitance	C_{rss}	—	140	—	pF	
Total gate charge	Q_g	—	43	—	nC	$V_{DD} = 25 V, V_{GS} = 10 V,$ $I_D = 20 A$
Gate to source charge	Q_{gs}	—	6.2	—	nC	
Gate to drain charge	Q_{gd}	—	7.2	—	nC	
Turn-on delay time	$t_{d(on)}$	—	13	—	ns	$V_{GS} = 10 V, I_D = 10 A,$ $V_{DD} \cong 30 V, R_L = 3 \Omega,$ $R_G = 4.7 \Omega$
Rise time	t_r	—	6	—	ns	
Turn-off delay time	$t_{d(off)}$	—	65	—	ns	
Fall time	t_f	—	4.5	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.91	1.18	V	$I_F = 20 A, V_{GS} = 0$ ^{Note5}
Body-drain diode reverse recovery time	t_{rr}	—	35	—	ns	$I_F = 20 A, V_{GS} = 0$ $di_F/dt = 100 A/\mu s$

Note: 5. Pulse test

• MOS4, MOS5, MOS6 (P Channel)

(Ta = 25°C)

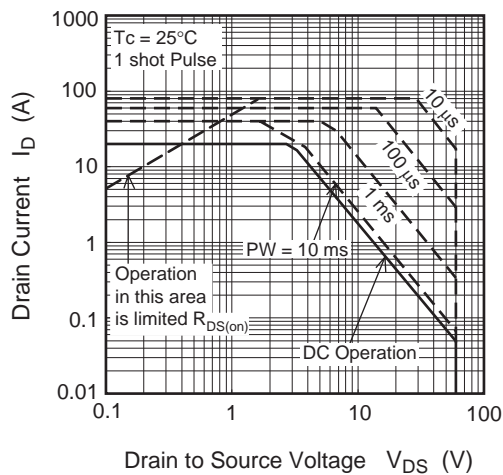
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60 V, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = -20 V / +5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 V, I_D = -1 mA$
Static drain to source on state resistance	$R_{DS(on)}$	—	32	40	$m\Omega$	$I_D = -10 A, V_{GS} = -10 V$ ^{Note6}
		—	42	64	$m\Omega$	$I_D = -10 A, V_{GS} = -4.5 V$ ^{Note6}
Input capacitance	C_{iss}	—	2600	—	pF	$V_{DS} = -10 V, V_{GS} = 0,$ $f = 1 MHz$
Output capacitance	C_{oss}	—	330	—	pF	
Reverse transfer capacitance	C_{rss}	—	240	—	pF	
Total gate charge	Q_g	—	53	—	nC	$V_{DD} = -25 V, V_{GS} = -10 V,$ $I_D = -20 A$
Gate to source charge	Q_{gs}	—	8.8	—	nC	
Gate to drain charge	Q_{gd}	—	13	—	nC	
Turn-on delay time	$t_{d(on)}$	—	22	—	ns	$V_{GS} = -10 V, I_D = -10 A,$ $V_{DD} \cong -30 V, R_L = 3 \Omega,$ $R_G = 4.7 \Omega$
Rise time	t_r	—	17	—	ns	
Turn-off delay time	$t_{d(off)}$	—	100	—	ns	
Fall time	t_f	—	20	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.95	-1.24	V	$I_F = -20 A, V_{GS} = 0$ ^{Note6}
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = -20 A, V_{GS} = 0$ $di_F/dt = 100 A/\mu s$

Note: 6. Pulse test

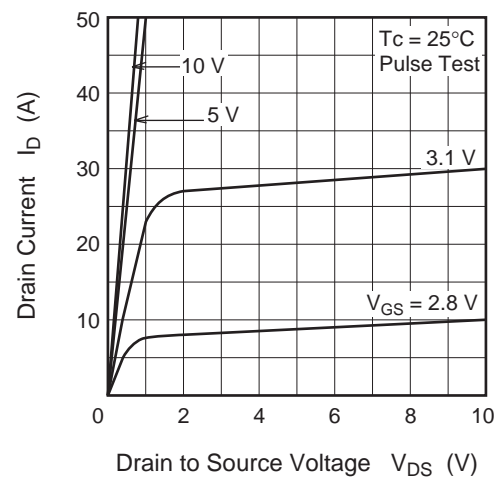
Main Characteristics

• MOS1, MOS2, MOS3 (N Channel)

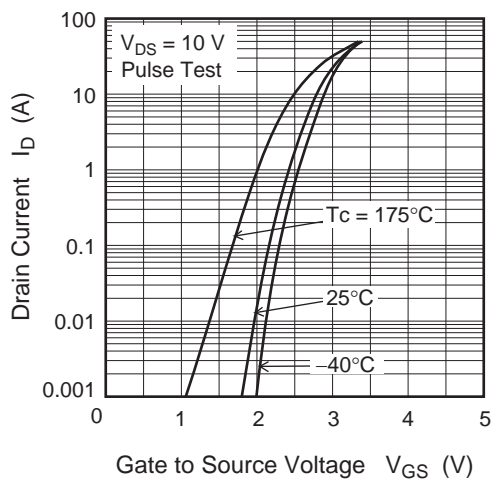
Maximum Safe Operation Area



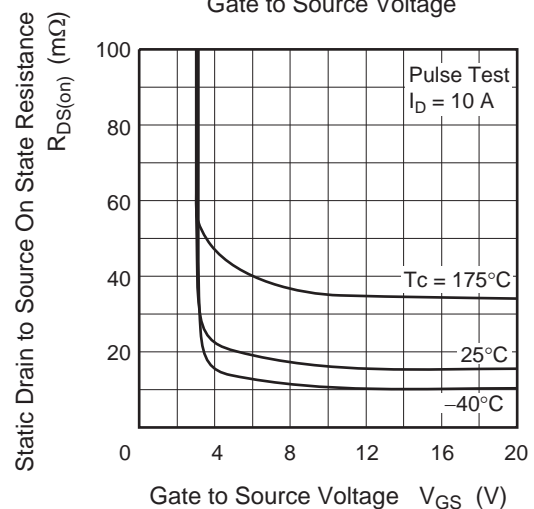
Typical Output Characteristics



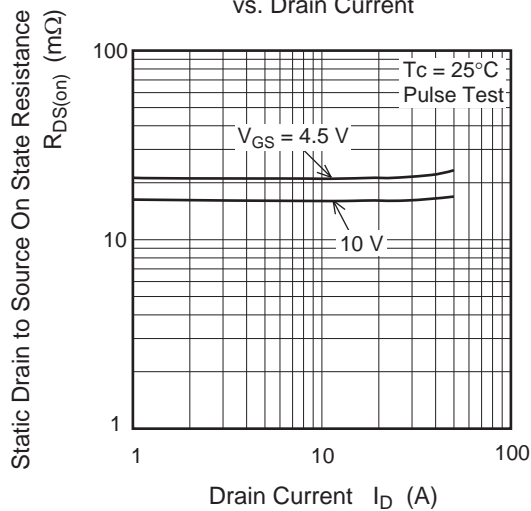
Typical Transfer Characteristics



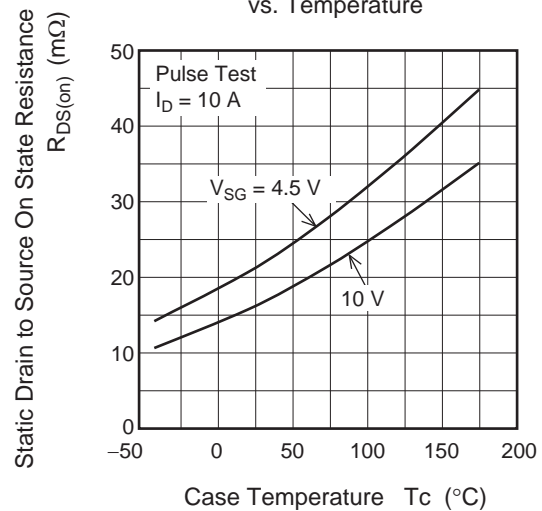
Static Drain to Source On State Resistance vs. Gate to Source Voltage



Static Drain to Source On State Resistance vs. Drain Current

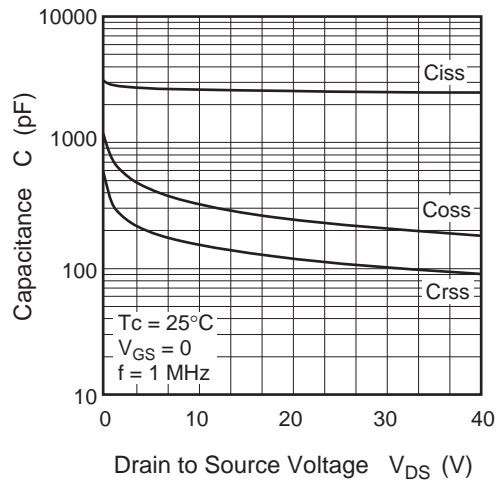


Static Drain to Source on State Resistance vs. Temperature

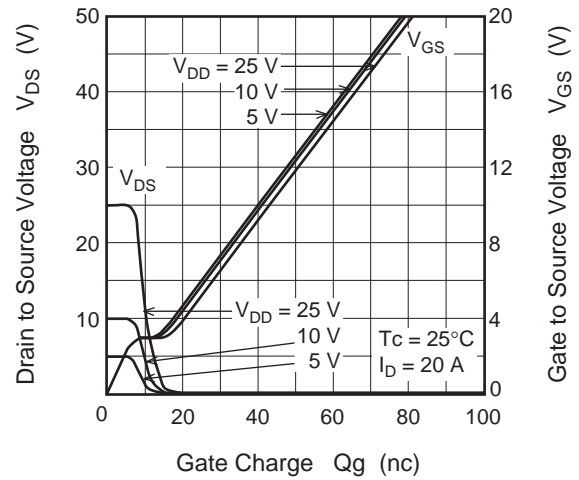


• MOS1, MOS2, MOS3 (N Channel)

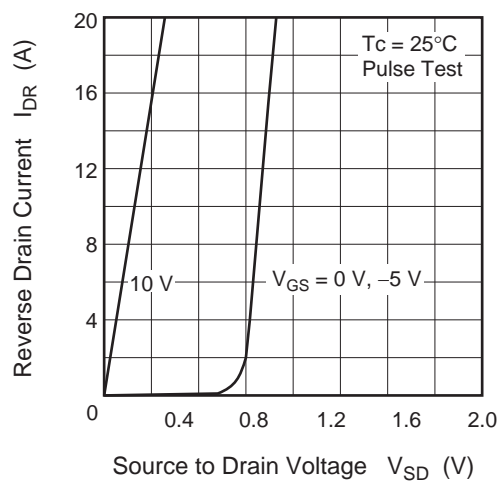
Typical Capacitance vs.
Drain to Source Voltage



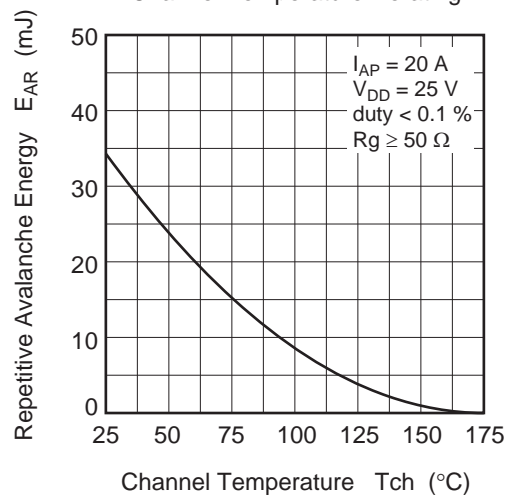
Dynamic Input Characteristics



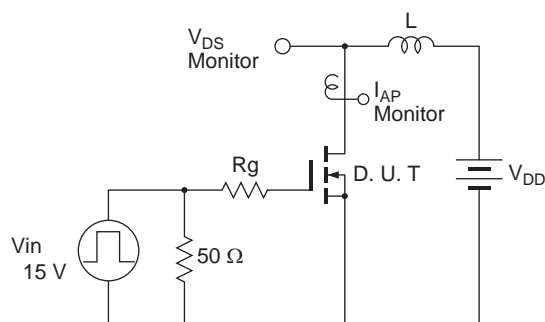
Reverse Drain Current vs.
Source to Drain Voltage



Avalanche Energy vs.
Channel Temperature Derating

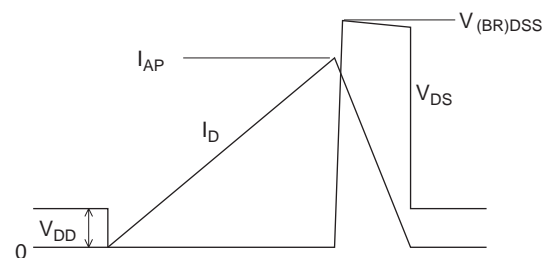


Avalanche Test Circuit

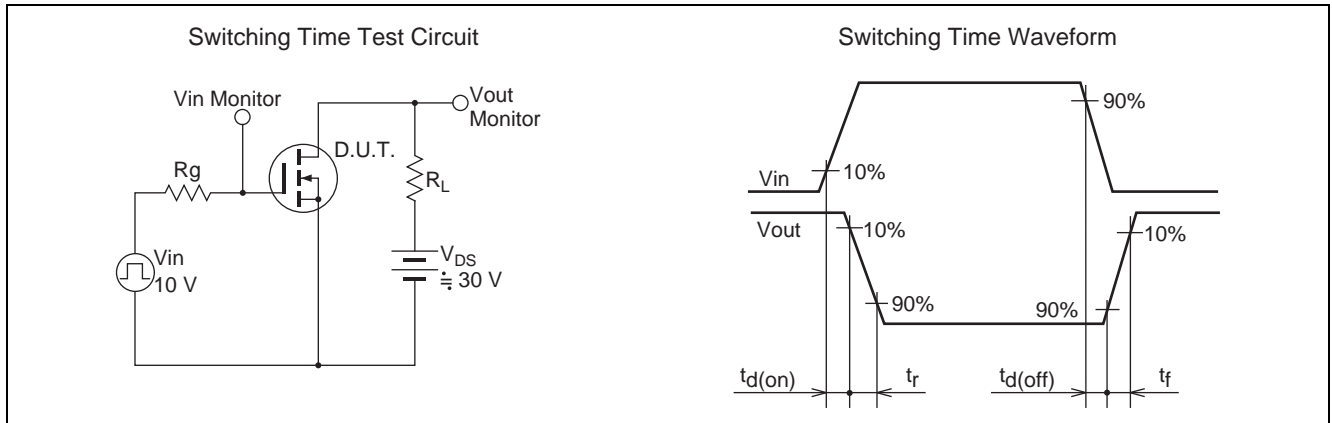


Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

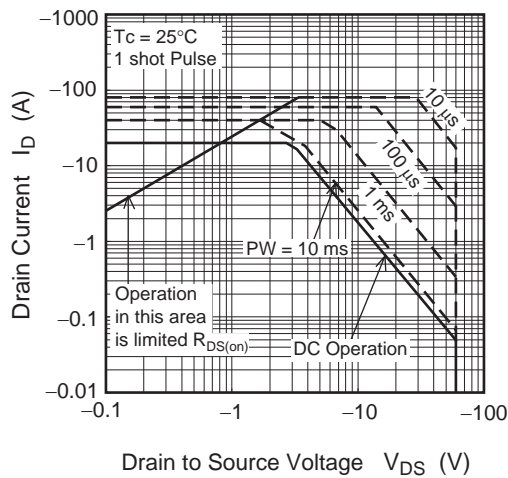


• MOS1, MOS2, MOS3 (N Channel)

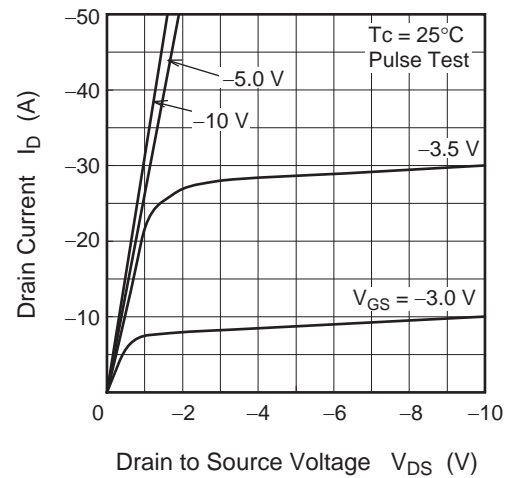


• MOS4, MOS5, MOS6 (P Channel)

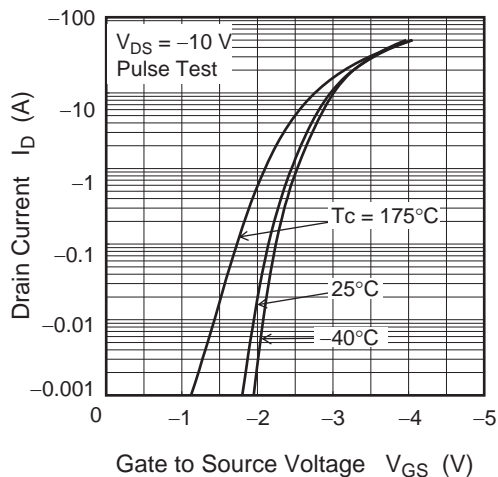
Maximum Safe Operation Area



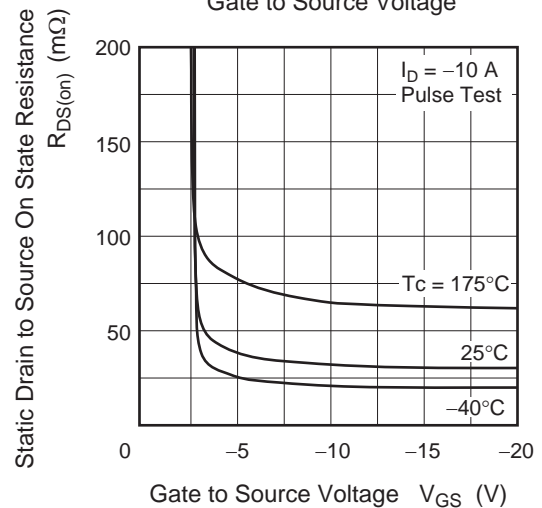
Typical Output Characteristics



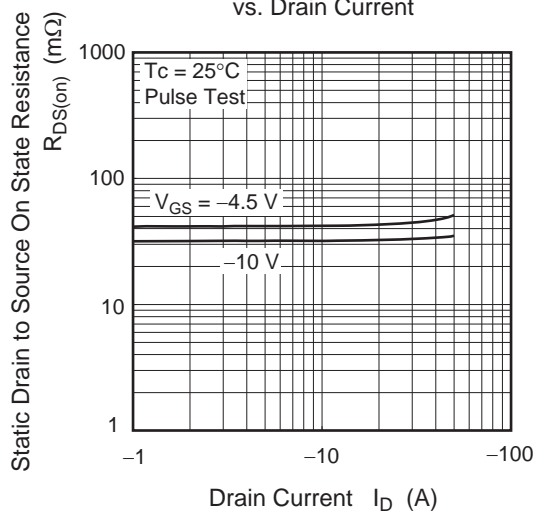
Typical Transfer Characteristics



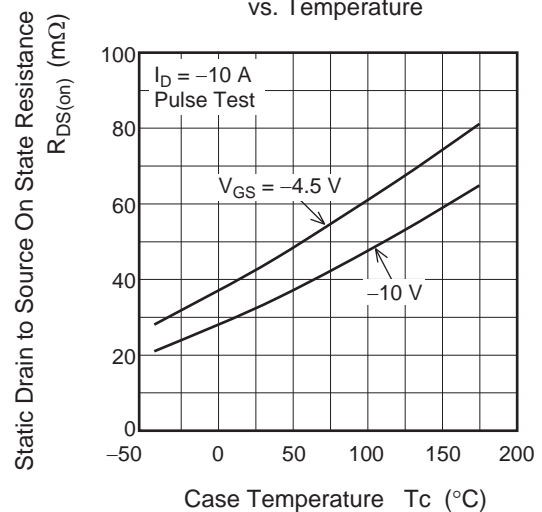
Static Drain to Source On State Resistance vs. Gate to Source Voltage



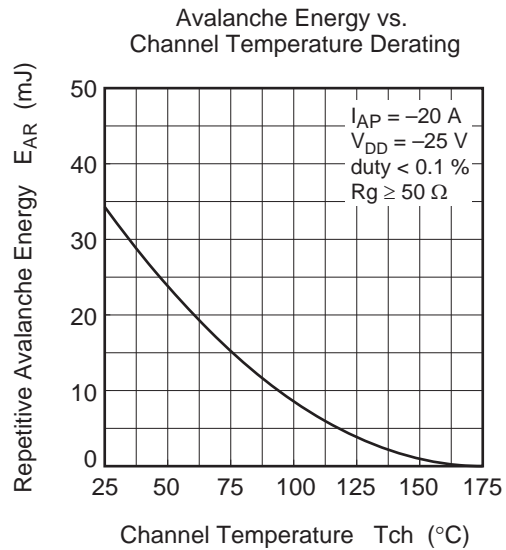
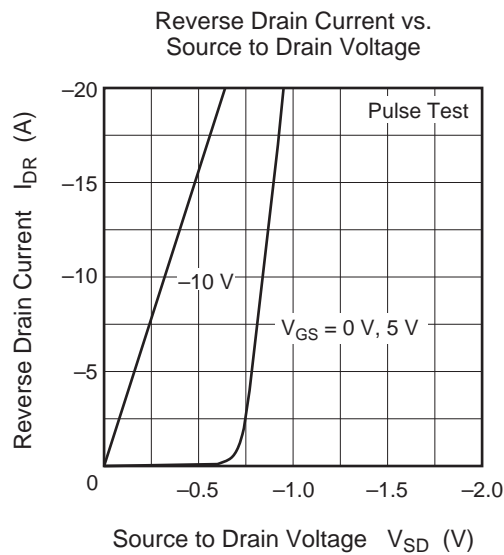
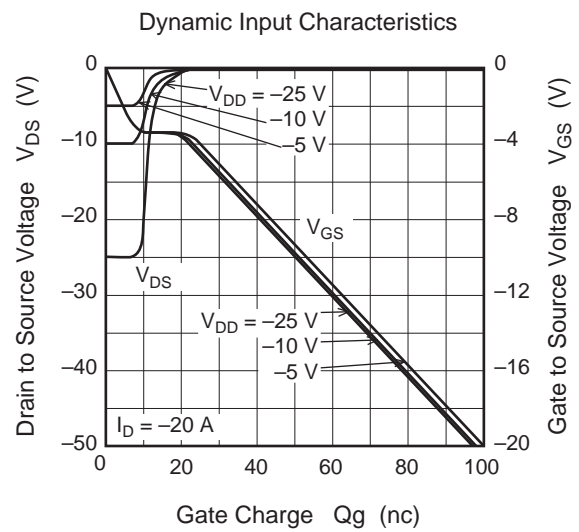
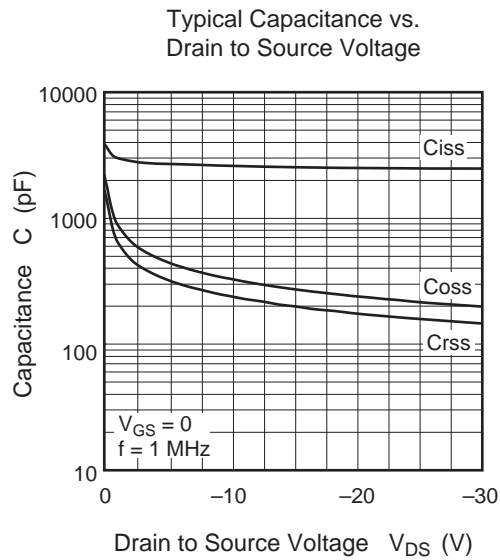
Static Drain to Source On State Resistance vs. Drain Current



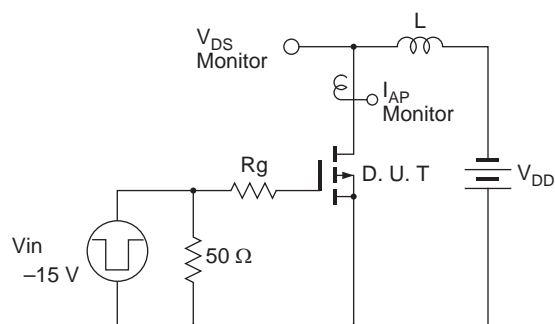
Static Drain to Source on State Resistance vs. Temperature



• MOS4, MOS5, MOS6 (P Channel)

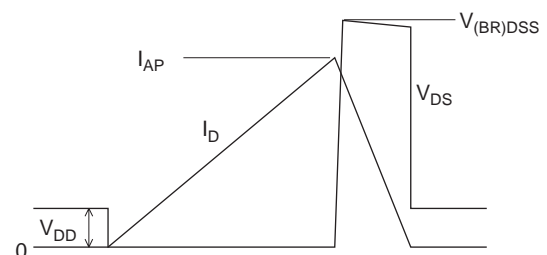


Avalanche Test Circuit

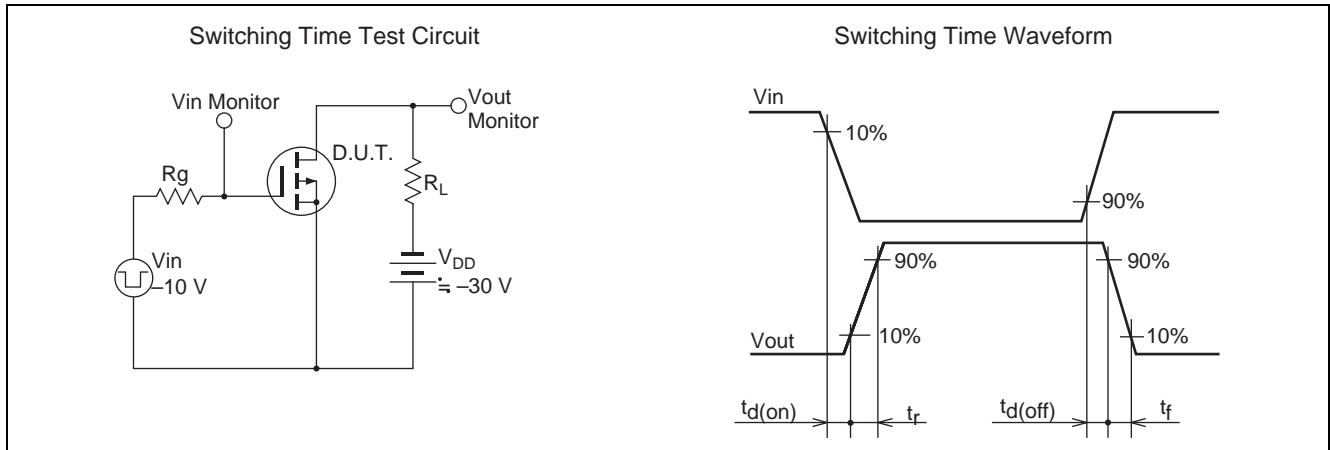


Avalanche Waveform

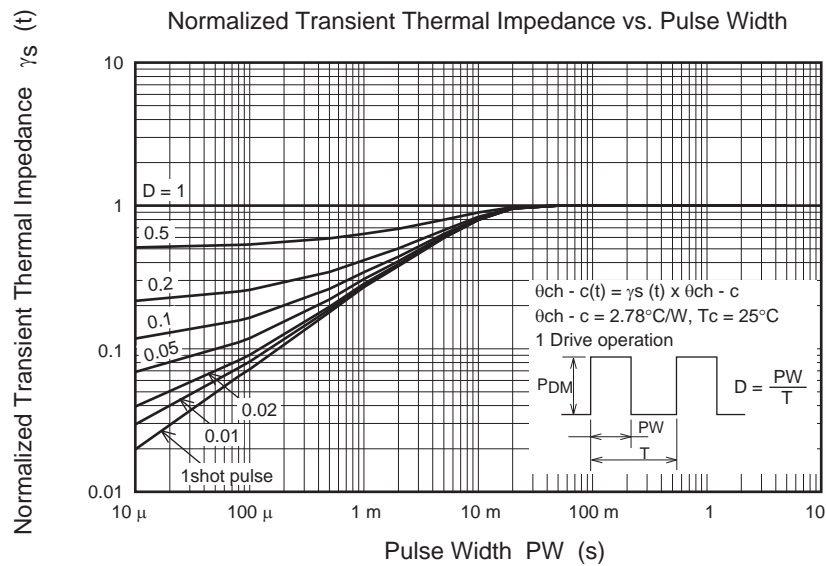
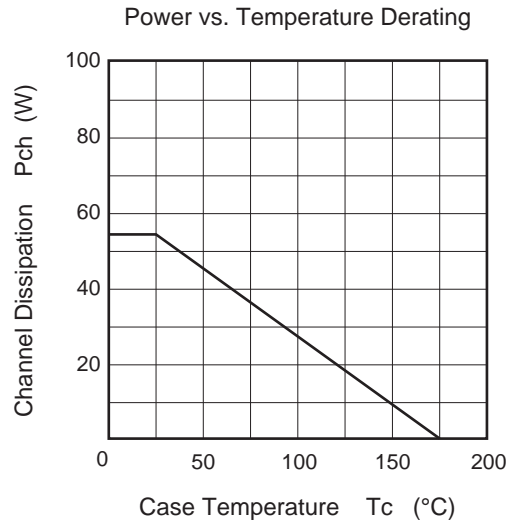
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



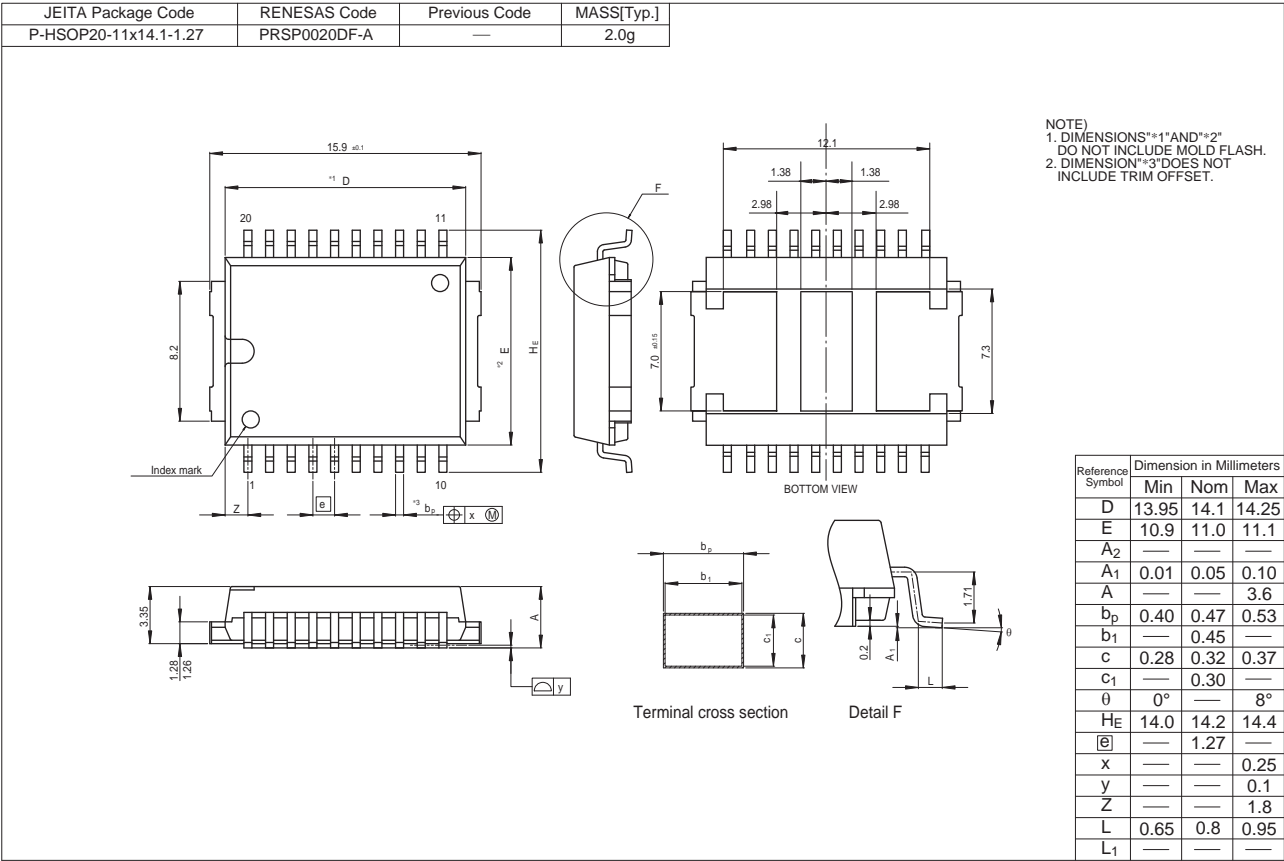
• MOS4, MOS5, MOS6 (P Channel)



• Common



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJM0603JSC-00-12	700 pcs	Tray

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