# TMS320DM6467T
# Digital Media System-on-Chip

Check for Samples: TMS320DM6467T

## 1 Digital Media System-on-Chip (DMSoC)

### 1.1 Features

- High-Performance Digital Media SoC
  - 1-GHz C64x+™ Clock Rate
  - 500-MHz ARM926EJ-S™ Clock Rate
  - Eight 32-Bit C64x+ Instructions/Cycle
  - 8000 C64x+ MIPS
  - Fully Software-Compatible With C64x / ARM9™
  - Industrial Temperature Devices Available
- Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x+™ DSP Core
  - Eight Highly Independent Functional Units
    - Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle
    - Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle
  - Load-Store Architecture With Non-Aligned Support
  - 64 32-Bit General-Purpose Registers
  - Instruction Packing Reduces Code Size
  - All Instructions Conditional
  - Additional C64x+™ Enhancements
    - Protected Mode Operation
    - Exceptions Support for Error Detection and Program Redirection
    - Hardware Support for Modulo Loop Operation
- C64x+ Instruction Set Features
  - Byte-Addressable (8-/16-/32-/64-Bit Data)
  - 8-Bit Overflow Protection
  - Bit-Field Extract, Set, Clear
  - Normalization, Saturation, Bit-Counting
  - Compact 16-Bit Instructions
  - Additional Instructions to Support Complex Multiplies
- C64x+ L1/L2 Memory Architecture
  - 32K-Byte L1P Program RAM/Cache (Direct Mapped)
  - 32K-Byte L1D Data RAM/Cache (2-Way Set-Associative)
  - 128K-Byte L2 Unified Mapped RAM/Cache (Flexible RAM/Cache Allocation)
- ARM926EJ-S Core
  - Support for 32-Bit and 16-Bit (Thumb® Mode) Instruction Sets
  - DSP Instruction Extensions and Single Cycle MAC
  - ARM® Jazelle® Technology
  - EmbeddedICE-RT™ Logic for Real-Time Debug
- ARM9 Memory Architecture
  - 16K-Byte Instruction Cache
  - 8K-Byte Data Cache
  - 32K-Byte RAM
  - 8K-Byte ROM
- Embedded Trace Buffer™ (ETB11™) With 4KB Memory for ARM9 Debug
- Endianness: Little Endian for ARM and DSP
- Dual Programmable High-Definition Video Image Co-Processor (HDVICP) Engines
  - Supports a Range of Encode, Decode, and Transcode Operations
    - H.264, MPEG2, VC1, MPEG4 SP/ASP
- 150-MHz Video Port Interface (VPIF)
  - Two 8-Bit SD (BT.656), Single 16-Bit HD (BT.1120), or Single Raw (8-/10-/12-Bit) Video Capture Channels
  - Two 8-Bit SD (BT.656) or Single 16-Bit HD (BT.1120) Video Display Channels
- Video Data Conversion Engine (VDCE)
  - Horizontal and Vertical Downscaling
  - Chroma Conversion (4:2:2↔4:2:0)
- Two Transport Stream Interface (TSIF) Modules (One Parallel/Serial and One Serial Only)
  - TSIF for MPEG Transport Stream
  - Simultaneous Synchronous or Asynchronous Input/Output Streams
  - Absolute Time Stamp Detection
  - PID Filter With 7 PID Filter Tables
  - Corresponding Clock Reference Generator (CRGEN) Modules for System Time-Clock Recovery

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- External Memory Interfaces (EMIFs)
  - Up to 400-MHz 32-Bit DDR2 SDRAM Memory Controller With 512M-Byte Address Space (1.8-V I/O)
  - Asynchronous16-Bit Wide EMIF (EMIFA) With 128M-Byte Address Reach
    - Flash Memory Interfaces
      - NOR (8-/16-Bit-Wide Data)
      - NAND (8-/16-Bit-Wide Data)
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
  - Programmable Default Burst Size
- 10/100/1000 Mb/s Ethernet MAC (EMAC)
  - IEEE 802.3 Compliant (3.3-V I/O Only)
  - Supports MII and GMII Media Independent Interfaces
  - Management Data I/O (MDIO) Module
- USB Port With Integrated 2.0 PHY
  - USB 2.0 High-/Full-Speed Client
  - USB 2.0 High-/Full-/Low-Speed Host (Mini-Host, Supporting One External Device)
- 32-Bit, 66-MHz, 3.3 V Peripheral Component Interconnect (PCI) Master/Slave Interface
  - Conforms to PCI Specification 2.3
- Two 64-Bit General-Purpose Timers (Each Configurable as Two 32-Bit Timers)
- One 64-Bit Watch Dog Timer
- Three Configurable UART/IrDA/CIR Modules (One With Modem Control Signals)
  - Supports up to 1.8432 Mbps UART
  - SIR and MIR (0.576 MBAUD)
  - CIR With Programmable Data Encoding
- One Serial Peripheral Interface (SPI) With Two Chip-Selects
- Master/Slave Inter-Integrated Circuit ($I^2C$ Bus™)
- Two Multichannel Audio Serial Ports (McASPs)
  - One Four Serializer Transmit/Receive Port
  - One Single DIT Transmit Port for S/PDIF
- 32-Bit Host Port Interface (HPI)
- VLYNQ™ Interface (FPGA Interface)
- Two Pulse Width Modulator (PWM) Outputs
- ATA/ATAPI I/F (ATA/ATAPI-6 Specification)
- Up to 33 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)
- On-Chip ARM ROM Bootloader (RBL)
- Individual Power-Saving Modes for ARM/DSP
- Flexible PLL Clock Generators
- IEEE-1149.1 (JTAG) Boundary-Scan-Compatible
- 529-Pin Pb-Free BGA Package (CUT Suffix), 0.8-mm Ball Pitch
- 0.09-µm/7-Level Cu Metal Process (CMOS)
- 3.3-V and 1.8-V I/O, 1.3-V Internal
- Applications:
  - Video Encode/Decode/Transcode/Transrate
  - Digital Media
  - Networked Media Encode/Decode
  - Video Imaging
  - Video Infrastructure
  - Video Conferencing


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## 1.2 Description

The TMS320DM6467T (also referenced as DM6467T) leverages TI's DaVinci™ technology to meet the networked media encode and decode digital media processing needs of next-generation embedded devices.

The DM6467T enables OEMs and ODMs to quickly bring to market devices featuring robust operating systems support, rich user interfaces, high processing performance, and long battery life through the maximum flexibility of a fully integrated mixed processor solution.

The dual-core architecture of the DM6467T provides benefits of both DSP and Reduced Instruction Set Computer (RISC) technologies, incorporating a high-performance TMS320C64x+ DSP core and an ARM926EJ-S core.

The ARM926EJ-S is a 32-bit RISC processor core that performs 32-bit or 16-bit instructions and processes 32-bit, 16-bit, or 8-bit data. The core uses pipelining so that all parts of the processor and memory system can operate continuously.

The ARM core incorporates:

- A coprocessor 15 (CP15) and protection module
- Data and program Memory Management Units (MMUs) with table look-aside buffers.
- Separate 16K-byte instruction and 8K-byte data caches. Both are four-way associative with virtual index virtual tag (VIVT).

The TMS320C64x+™ DSPs are the highest-performance fixed-point DSP generation in the TMS320C6000™ DSP platform. It is based on an enhanced version of the second-generation high-performance, advanced very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSP cores an excellent choice for digital media applications. The C64x is a code-compatible member of the C6000™ DSP platform. The TMS320C64x+ DSP is an enhancement of the C64x+ DSP with added functionality and an expanded instruction set.

Any reference to the C64x DSP or C64x CPU also applies, unless otherwise noted, to the C64x+ DSP and C64x+ CPU, respectively.

With performance of up to 8000 million instructions per second (MIPS) at a clock rate of 1 GHz, the C64x+ core offers solutions to high-performance DSP programming challenges. The DSP core possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. The C64x+ DSP core processor has 64 general-purpose registers of 32-bit word length and eight highly independent functional units—two multipliers for a 32-bit result and six arithmetic logic units (ALUs). The eight functional units include instructions to accelerate the performance in video and imaging applications. The DSP core can produce four 16-bit multiply-accumulates (MACs) per cycle for a total of 4000 million MACs per second (MMACS), or eight 8-bit MACs per cycle for a total of 8000 MMACS. For more details on the C64x+ DSP, see the *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRU732).

The DM6467T also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals similar to the other C6000 DSP platform devices. The DM6467T core uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 256K-bit direct mapped cache and the Level 1 data cache (L1D) is a 640K-bit 2-way set-associative cache. The Level 2 memory/cache (L2) consists of an 512K-bit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two.

The peripheral set includes: a configurable video port; a 10/100/1000 Mb/s Ethernet MAC (EMAC) with a Management Data Input/Output (MDIO) module; a 4-bit transfer/4-bit receive VLYNQ interface; an inter-integrated circuit (I2C) Bus interface; a multichannel audio serial port (McASP0) with 4 serializers; a secondary multichannel audio serial port (McASP1) with a single transmit serializer; 2 64-bit general-purpose timers each configurable as 2 independent 32-bit timers; 1 64-bit watchdog timer; a configurable 32-bit host port interface (HPI); up to 33-pins of general-purpose input/output (GPIO) with programmable

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interrupt/event generation modes, multiplexed with other peripherals; 3 UART/IrDA/CIR interfaces with modem interface signals on UART0; 2 pulse width modulator (PWM) peripherals; an ATA/ATAPI-6 interface; a 66-MHz peripheral component interface (PCI); and 2 external memory interfaces: an asynchronous external memory interface (EMIFA) for slower memories/peripherals, and a higher speed synchronous memory interface for DDR2.

The Ethernet Media Access Controller (EMAC) provides an efficient interface between the DM6467T and the network. The DM6467T EMAC support both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode; and 1000Base-TX (1 Gbps) in full-duplex mode with hardware flow control and quality of service (QOS) support.

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system. Once a PHY candidate has been selected by the ARM, the MDIO module transparently monitors its link state by reading the PHY status register. Link change events are stored in the MDIO module and can optionally interrupt the ARM, allowing the ARM to poll the link status of the device without continuously performing costly MDIO accesses.

The PCI, HPI, I2C, SPI, USB2.0, and VLYNQ ports allow the DM6467T to easily control peripheral devices and/or communicate with host processors.

The DM6467T also includes a High-Definition Video/Imaging Co-processor (HDVICP) and Video Data Conversion Engine (VDCE) to offload many video and imaging processing tasks from the DSP core, making more DSP MIPS available for common video and imaging algorithms. For more information on the HDVICP enhanced codecs, such as H.264 and MPEG4, please contact your nearest TI sales representative.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each of the peripherals, see the related sections later in this document and the associated peripheral reference guides.

The DM6467T has a complete set of development tools for both the ARM and DSP. These include C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.


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## 1.3 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.

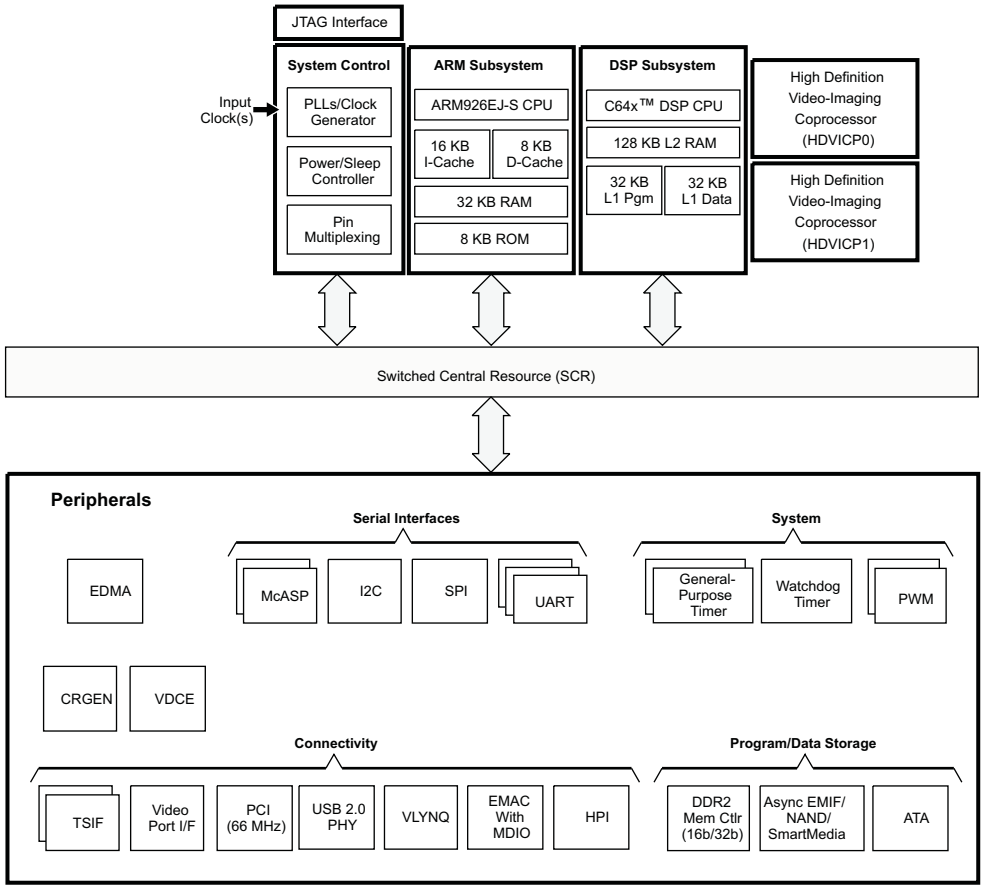


**Figure 1-1. TMS320DM6467T Functional Block Diagram**

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# 2 Revision History

This data manual revision history highlights the technical changes made to the SPRS605B device-specific data manual to make it an SPRS605C revision.

**Scope:** Applicable updates to the DM646x DMSoC device family, specifically relating to the TMS320DM6467 device (all Silicon Revisions 3.0, 1.1, and 1.0) which is now in teh production data (PD) stage of development have been incorporated.

- The ZUT 529-pin PBGA device orderables have now been classified as end of life (EOL) product and replaced with CUT 529-pin PBGA (Pb-Free die bump and solder ball) package orderables.

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# 3 Device Overview

## 3.1 Device Characteristics

Table 3-1 provides an overview of the TMS320DM6467T SoC. The table shows significant features of the device, including the capacity of on-chip RAM, peripherals, internal peripheral bus frequency relative to the C64x+ DSP, and the package type with pin count.

**Table 3-1. Characteristics of the DM6467T Processor**

| HARDWARE FEATURES | | DM6467T |
|---|---|---|
| Peripherals<br><br>Not all peripherals pins are available at the same time (for more detail, see the Device Configurations section). | DDR2 Memory Controller | DDR2 (Up to 400-MHz, 16/32-bit bus width) |
| | Asynchronous EMIF (EMIFA) | Asynchronous (8/16-bit bus width) RAM, Flash (NOR, NAND) |
| | EDMA | 64 independent channels<br>8 QDMA channels |
| | Timers | 2 64-Bit General Purpose (each configurable as 2 separate 32-bit timers)<br>1 64-Bit Watchdog |
| | UART | 3 (with SIR, MIR, CIR support and RTS/CTS flow control)<br>(UART0 Supports Modem Interface) |
| | SPI | 1 (supports 2 slave devices) |
| | $I^2C$ | 1 (Master/Slave) |
| | Multichannel Audio Serial Port (McASP) | 2 (one transmit/receive with 4 serializers, one DIT transmit *only* with 1 serializer for S/PDIF output) |
| | 10/100/1000 Ethernet MAC with Management Data Input/Output (MDIO) | 1 (with MII/GMII Interface) |
| | VLYNQ | 1 |
| | General-Purpose Input/Output Port (GPIO) | Up to 33 pins |
| | PWM | 2 outputs |
| | ATA | 1 (ATA/ATAPI-6) |
| | PCI | 1 (32-bit, 66 MHz) |
| | HPI | 1 (16-/32-bit multiplexed address/data) |
| | VDCE | 1 [horizontal and vertical downscaling, chroma conversion (4:2:2↔4:2:0)] |
| | Clock Recovery Generator (CRGEN) | 1 |
| | Power Sleep Controller (PSC) | 1 (peripheral/module clock gating) |
| | 150-MHz Configurable Video Port Interface (VPIF) | 2 8-bit BT.656 capture channels ***or***<br>1 16-bit Y/C capture channel ***or***<br>1 8-/10-/12-bit raw video capture channel ***and***<br>2 8-bit BT.656 display channels or<br>1 16-bit Y/C display channel |
| | Transport Stream Interface (TSIF) | MPEG transport stream interface<br><br>1 with 8-bit parallel *or* serial input and output<br>1 with serial-only input and output<br><br>Each with corresponding clock recovery generator (CRGEN) for external VCXO control. |
| | USB 2.0 (1) | High- and Full-Speed Device<br>High-, Full-, and Low-Speed Host |

(1) USB2.0 is not supported on -1G parts that are dated prior to May 1, 2010. See the TMS320DM6467T Silicon Errata (Literature Number: SPRZ307) for more details on how to decode the date from package markings.


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**Table 3-1. Characteristics of the DM6467T Processor (continued)**

| HARDWARE FEATURES | | DM6467T |
|---|---|---|
| On-Chip Memory | Size (Bytes) | 248KB RAM, 8KB ROM |
| | Organization | DSP<br>• 32KB L1 Program (L1P)/Cache (up to 32KB)<br>• 32KB L1 Data (L1D)/Cache (up to 32KB)<br>• 128KB Unified Mapped RAM/Cache (L2)<br>ARM<br>• 16KB I-cache<br>• 8KB D-cache<br>• 32KB RAM<br>• 8KB ROM |
| CPU ID + CPU Rev ID | Control Status Register (CSR.[31:16]) | 0x1000 |
| C64x+ Megamodule Revision | Revision ID Register (MM_REVID[15:0])<br>(address location: 0x0181 2000) | 0x0000 |
| JTAG BSDL_ID | JTAGID Register<br>(address location: 0x01C4 0028) | See Section 7.29.1, *JTAG ID (JTAGID) Register Description(s)* |
| CPU Frequency | MHz | DSP 1 GHz (-1G) |
| | | ARM926 500 MHz(-1G) |
| Cycle Time | ns | DSP 1.0 ns (-1G) |
| | | ARM926 2.0 ns (-1G) |
| Voltage | Core (V) | 1.3 V (-1G) |
| | I/O (V) | 1.8 V, 3.3 V (-1G) |
| PLL Options | DEV_CLKIN frequency multiplier (PLLC1)<br>(Between 27 – 35-MHz range) | x1 (Bypass), x14 to x32 (-1G) |
| | DEV_CLKIN frequency multiplier (PLLC2)<br>(Between 27 – 35-MHz range) | x1 (Bypass), x14 to x32 (-1G) |
| | AUX_CLKIN frequency | 24/48-MHz reference |
| BGA Package | 19 x 19 mm | 529-Pin BGA (CUT) |
| Process Technology | µm | 0.09 µm |
| Product Status(2) | Product Preview (PP),<br>Advance Information (AI),<br>or Production Data (PD) | PD |

(2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## 3.2 Device Compatibility

The ARM926EJ-S RISC CPU is compatible with other ARM9 CPUs from ARM Holdings plc.

The C64x+ DSP core is code-compatible with the C6000™ DSP platform and supports features of the C64xT DSP family.

## 3.3 ARM Subsystem

The ARM Subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP Subsystem, the VPSS Subsystem, and a majority of the peripherals and external memories.

The ARM Subsystem includes the following features:

- ARM926EJ-S RISC processor
- ARMv5TEJ (32/16-bit) instruction set
- Little endian operation
- Co-Processor 15 (CP15)
- MMU
- 16KB Instruction cache
- 8KB Data cache
- Write Buffer
- 32KB Internal Tightly-Coupled Memory (TCM) RAM (32-bit wide access)
- 8KB Internal ROM (ARM bootloader for non-EMIFA boot options)
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)
- ARM Interrupt Controller
- PLL Controller
- Power and Sleep Controller (PSC)
- System Module

### *3.3.1 ARM926EJ-S RISC CPU*

The ARM Subsystem integrates the ARM926EJ-S processor. The ARM926EJ-S processor is a member of ARM9 family of general-purpose microprocessors. This processor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM926EJ-S processor supports the 32-bit ARM and 16 bit THUMB instruction sets, enabling the user to trade off between high performance and high code density. Specifically, the ARM926EJ-S processor supports the ARMv5TEJ instruction set, which includes features for efficient execution of Java byte codes, providing Java performance similar to Just in Time (JIT) Java interpreter, but without associated code overhead.

The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM926EJ-S processor has a Harvard architecture and provides a complete high performance subsystem, including:

- ARM926EJ -S integer core
- CP15 system control coprocessor
- Memory Management Unit (MMU)
- Separate instruction and data Caches
- Write buffer
- Separate instruction and data Tightly-Coupled Memories (TCMs) [internal RAM] interfaces
- Separate instruction and data AHB bus interfaces
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)


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For more complete details on the ARM9, refer to the ARM926EJ-S Technical Reference Manual, available at http://www.arm.com

### 3.3.2 CP15

The ARM926EJ-S system control coprocessor (CP15) is used to configure and control instruction and data caches, Tightly-Coupled Memories (TCMs), Memory Management Unit (MMU), and other ARM subsystem functions. The CP15 registers are programmed using the MRC and MCR ARM instructions, when the ARM in a privileged mode such as supervisor or system mode.

### 3.3.3 MMU

The ARM926EJ-S MMU provides virtual memory features required by operating systems such as Linux®, Windows® CE, Ultron®, ThreadX®, etc. A single set of two level page tables stored in main memory is used to control the address translation, permission checks and memory region attributes for both data and instruction accesses. The MMU uses a single unified Translation Lookaside Buffer (TLB) to cache the information held in the page tables. The MMU features are:

- Standard ARM architecture v4 and v5 MMU mapping sizes, domains and access protection scheme.
- Mapping sizes are:
  - 1MB (sections)
  - 64KB (large pages)
  - 4KB (small pages)
  - 1KB (tiny pages)
- Access permissions for large pages and small pages can be specified separately for each quarter of the page (subpage permissions)
- Hardware page table walks
- Invalidate entire TLB, using CP15 register 8
- Invalidate TLB entry, selected by MVA, using CP15 register 8
- Lockdown of TLB entries, using CP15 register 10

### 3.3.4 Caches and Write Buffer

The size of the Instruction Cache is 16KB, Data cache is 8KB. Additionally, the Caches have the following features:

- Virtual index, virtual tag, and addressed using the Modified Virtual Address (MVA)
- Four-way set associative, with a cache line length of eight words per line (32-bytes per line) and with two dirty bits in the Dcache
- Dcache supports write-through and write-back (or copy back) cache operation, selected by memory region using the C and B bits in the MMU translation tables.
- Critical-word first cache refilling
- Cache lockdown registers enable control over which cache ways are used for allocation on a line fill, providing a mechanism for both lockdown, and controlling cache corruption
- Dcache stores the Physical Address TAG (PA TAG) corresponding to each Dcache entry in the TAG RAM for use during the cache line write-backs, in addition to the Virtual Address TAG stored in the TAG RAM. This means that the MMU is not involved in Dcache write-back operations, removing the possibility of TLB misses related to the write-back address.
- Cache maintenance operations provide efficient invalidation of, the entire Dcache or Icache, regions of the Dcache or Icache, and regions of virtual memory.

The write buffer is used for all writes to a noncachable bufferable region, write-through region and write misses to a write-back region. A separate buffer is incorporated in the Dcache for holding write-back for cache line evictions or cleaning of dirty cache lines. The main write buffer has 16-word data buffer and a four-address buffer. The Dcache write-back has eight data word entries and a single address entry.

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### 3.3.5 Tightly Coupled Memory (TCM)

ARM internal RAM is provided for storing real-time and performance-critical code/data and the Interrupt Vector table. ARM internal ROM enables non-EMIFA boot options, such as NAND and UART. The RAM and ROM memories interfaced to the ARM926EJ-S via the tightly coupled memory interface that provides for separate instruction and data bus connections. Since the ARM TCM does not allow instructions on the D-TCM bus or data on the I-TCM bus, an arbiter is included so that both data and instructions can be stored in the internal RAM/ROM. The arbiter also allows accesses to the RAM/ROM from extra-ARM sources (e.g., EDMA or other masters). The ARM926EJ-S has built-in DMA support for direct accesses to the ARM internal memory from a non-ARM master. Because of the time-critical nature of the TCM link to the ARM internal memory, all accesses from non-ARM devices are treated as DMA transfers.

Instruction and Data accesses are differentiated via accessing different memory map regions, with the instruction region from 0x0000 through 0x7FFF and data from 0x10000 through 0x17FFF. The instruction region at 0x0000 and data region at 0x10000 map to the same physical 32-KB TCM RAM. Placing the instruction region at 0x0000 is necessary to allow the ARM Interrupt Vector table to be placed at 0x0000, as required by the ARM architecture. The internal 32-KB RAM is split into two physical banks of 16KB each, which allows simultaneous instruction and data accesses to be accomplished if the code and data are in separate banks.

### 3.3.6 Advanced High-Performance Bus (AHB)

The ARM Subsystem uses the AHB port of the ARM926EJ-S to connect the ARM to the Config bus and the external memories. Arbiters are employed to arbitrate access to the separate D-AHB and I-AHB by the Config Bus and the external memories bus.

### 3.3.7 Embedded Trace Macrocell (ETM) and Embedded Trace Buffer (ETB)

To support real-time trace, the ARM926EJ-S processor provides an interface to enable connection of an Embedded Trace Macrocell (ETM). The ARM926ES-J Subsystem in the DM6467T also includes the Embedded Trace Buffer (ETB). The ETM consists of two parts:

- Trace Port provides real-time trace capability for the ARM9.
- Triggering facilities provide trigger resources, which include address and data comparators, counter, and sequencers.

The DM6467T trace port is not pinned out and is instead only connected to the Embedded Trace Buffer. The ETB has a 4KB buffer memory. ETB enabled debug tools are required to read/interpret the captured trace data.

### 3.3.8 ARM Memory Mapping

The ARM memory map is shown in Section 3.5, *Memory Map Summary* of this document. The ARM has access to memories shown in the following sections.

#### 3.3.8.1 ARM Internal Memories

The ARM has access to the following ARM internal memories:

- 32KB ARM Internal RAM on TCM interface, logically separated into two 16KB pages to allow simultaneous access on any given cycle if there are separate accesses for code (I-TCM bus) and data (D-TCM) to the different memory regions.
- 8KB ARM Internal ROM

#### 3.3.8.2 External Memories

The ARM has access to the following external memories:

- DDR2 Synchronous DRAM
- Asynchronous EMIF / NOR Flash / NAND Flash
- ATA


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#### 3.3.8.3 DSP Memories

The ARM has access to the following DSP memories:

- L2 RAM
- L1P RAM
- L1D RAM

#### 3.3.8.4 ARM-DSP Integration

DM6467T ARM and DSP integration features are as follows:

- DSP visibility from ARM's memory map, see Section 3.5, *Memory Map Summary*, for details
- Boot Modes for DSP - see *Device Configurations* section, Section 4.4.1, *DSP Boot*, for details
- ARM control of DSP boot / reset - see *Device Configurations* section, Section 4.4.2.4, *ARM Boot*, for details
- ARM control of DSP isolation and powerdown / powerup - see Section 4, *Device Configurations*, for details
- ARM & DSP Interrupts - see Section 7.8.1, *ARM CPU Interrupts*, and Section 7.8.2, *DSP Interrupts*, for details

### 3.3.9 Peripherals

The ARM9 has access to all of the peripherals on the DM6467T device.

### 3.3.10 PLL Controller (PLLC)

The ARM Subsystem includes the PLL Controller. The PLL Controller contains a set of registers for configuring DM6467T's two internal PLLs (PLL1 and PLL2). The PLL Controller provides the following configuration and control:

- PLL Bypass Mode
- Set PLL multiplier parameters
- Set PLL divider parameters
- PLL power down
- Oscillator power down

The PLLs are briefly described in this document in the Clocking section. For more detailed information on the PLLs and PLL Controller register descriptions, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

### 3.3.11 Power and Sleep Controller (PSC)

The ARM Subsystem includes the Power and Sleep Controller (PSC). Through register settings accessible by the ARM9, the PSC provides two levels of power savings: peripheral/module clock gating and power domain shut-off. Brief details on the PSC are given in Section 7.3, *Power Supplies*. For more detailed information and complete register descriptions for the PSC, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

### 3.3.12 ARM Interrupt Controller (AINTC)

The ARM Interrupt Controller (AINTC) accepts device interrupts and maps them to either the ARM's IRQ (interrupt request) or FIQ (fast interrupt request). The ARM Interrupt Controller is briefly described in this document in the Interrupts section. For detailed information on the ARM Interrupt Controller, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

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### 3.3.13 System Module

The ARM Subsystem includes the System module. The System module consists of a set of registers for configuring and controlling a variety of system functions. For details and register descriptions for the System module, see Section 4, *Device Configurations* and see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

### 3.3.14 Power Management

DM6467T has several means of managing power consumption. There is extensive use of clock gating, which reduces the power used by global device clocks and individual peripheral clocks. Clock management can be utilized to reduce clock frequencies in order to reduce switching power. For more details on power management techniques, see Section 4, *Device Configurations*, Section 7, *Peripheral and Electrical Specifications*, and see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

DM6467T gives the programmer full flexibility to use any and all of the previously mentioned capabilities to customize an optimal power management strategy. Several typical power management scenarios are described in the following sections.

## 3.4 DSP Subsystem

The DSP Subsystem includes the following features:

- C64x+ DSP CPU
- 32KB L1 Program (L1P)/Cache (up to 32KB)
- 32KB L1 Data (L1D)/Cache (up to 32KB)
- 128KB Unified Mapped RAM/Cache (L2)
- Little endian

### 3.4.1 C64x+ DSP CPU Description

The C64x+ Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 3-1. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C64x+ CPU extends the performance of the C64x core through enhancements and new features.

Each C64x+ .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes for 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for audio and other high-precision algorithms on a variety of signed and unsigned 32-bit data types.


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The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C64x+ core enhances the .S unit in several ways. In the C64x core, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C64x+ core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C64x+ compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C64x+ CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.
- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C64x+ CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRU732)
- *TMS320C64x Technical Overview* (literature number SPRU395)

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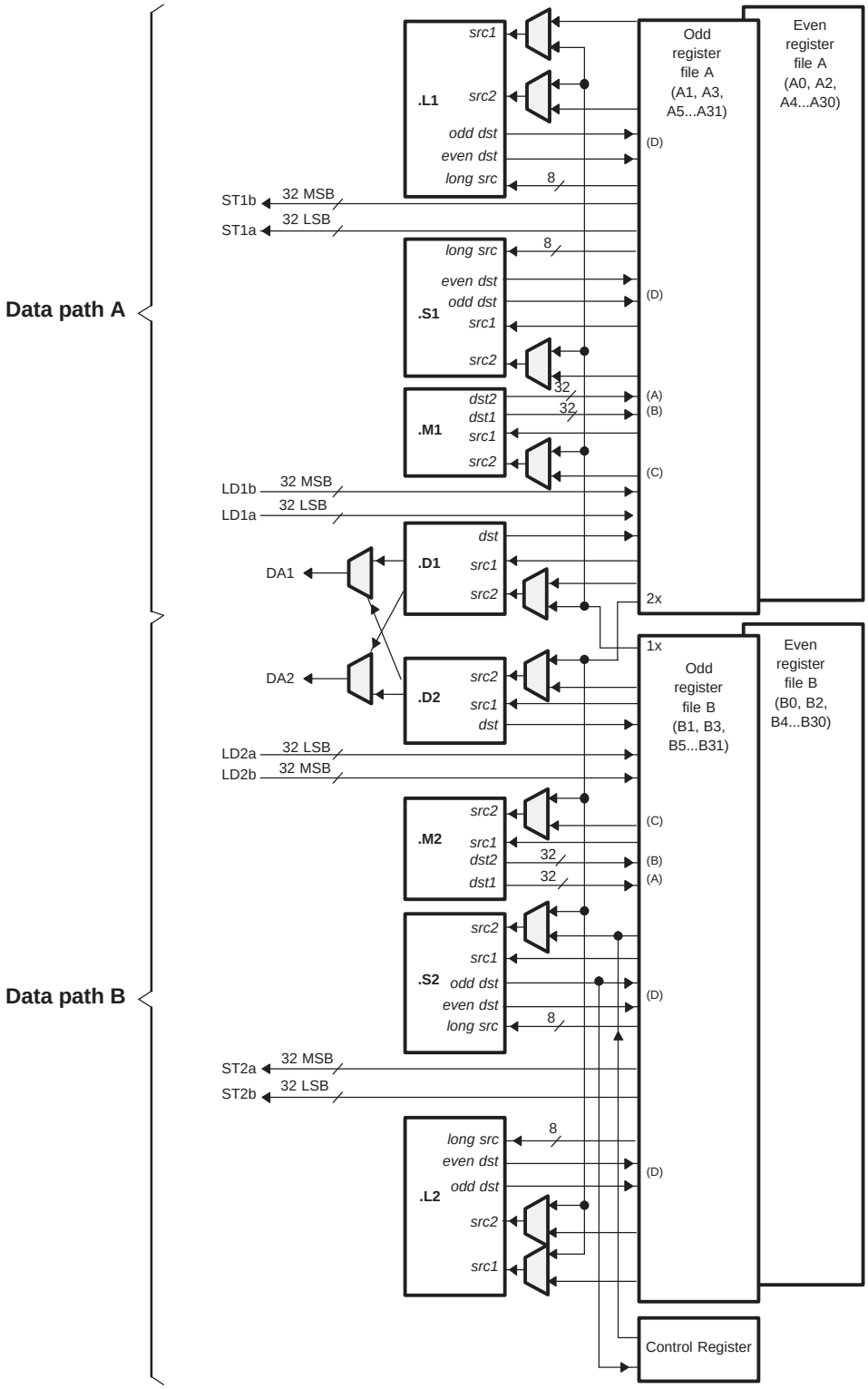


A. On .M unit, *dst2* is 32 MSB.
B. On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and *even dst* connects to even register files.

**Figure 3-1. TMS320C64x+™ CPU (DSP Core) Data Paths**


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### 3.4.2 DSP Memory Mapping

The DSP memory map is shown in Section 3.5, *Memory Map Summary*. Configuration of the control registers for DDR2, EMIFA, and ARM Internal RAM is supported by the ARM. The DSP has access to memories shown in the following sections.

#### 3.4.2.1 ARM Internal Memories

The DSP has access to the 32KB ARM Internal RAM on the ARM D-TCM interface (i.e., data only).

#### 3.4.2.2 External Memories

The DSP has access to the following External memories:

- DDR2 Synchronous DRAM
- Asynchronous EMIF / NOR Flash
- ATA

#### 3.4.2.3 DSP Internal Memories

The DSP has access to the following DSP memories:

- L2 RAM
- L1P RAM
- L1D RAM

#### 3.4.2.4 C64x+ CPU

The C64x+ core uses a two-level cache-based architecture. The Level 1 Program memory/cache (L1P) consists of 32 KB memory space that can be configured as mapped memory or direct mapped cache. The Level 1 Data memory/cache (L1D) consists of 32 KB that can be configured as mapped memory or 2-way set associated cache. The Level 2 memory/cache (L2) consists of a 128 KB RAM memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or a combination of both.

Table 3-2 shows a memory map of the C64x+ CPU cache registers for the device.

**Table 3-2. C64x+ Cache Registers**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 0000 | L2CFG | L2 Cache configuration register |
| 0x0184 0020 | L1PCFG | L1P Size Cache configuration register |
| 0x0184 0024 | L1PCC | L1P Freeze Mode Cache configuration register |
| 0x0184 0040 | L1DCFG | L1D Size Cache configuration register |
| 0x0184 0044 | L1DCC | L1D Freeze Mode Cache configuration register |
| 0x0184 0048 - 0x0184 0FFC | - | Reserved |
| 0x0184 1000 | EDMAWEIGHT | L2 EDMA access control register |
| 0x0184 1004 - 0x0184 1FFC | - | Reserved |
| 0x0184 2000 | L2ALLOC0 | L2 allocation register 0 |
| 0x0184 2004 | L2ALLOC1 | L2 allocation register 1 |
| 0x0184 2008 | L2ALLOC2 | L2 allocation register 2 |
| 0x0184 200C | L2ALLOC3 | L2 allocation register 3 |
| 0x0184 2010 - 0x0184 3FFF | - | Reserved |
| 0x0184 4000 | L2WBAR | L2 writeback base address register |
| 0x0184 4004 | L2WWC | L2 writeback word count register |
| 0x0184 4010 | L2WIBAR | L2 writeback invalidate base address register |
| 0x0184 4014 | L2WIWC | L2 writeback invalidate word count register |
| 0x0184 4018 | L2IBAR | L2 invalidate base address register |

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**Table 3-2. C64x+ Cache Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 401C | L2IWC | L2 invalidate word count register |
| 0x0184 4020 | L1PIBAR | L1P invalidate base address register |
| 0x0184 4024 | L1PIWC | L1P invalidate word count register |
| 0x0184 4030 | L1DWIBAR | L1D writeback invalidate base address register |
| 0x0184 4034 | L1DWIWC | L1D writeback invalidate word count register |
| 0x0184 4038 | - | Reserved |
| 0x0184 4040 | L1DWBAR | L1D Block Writeback |
| 0x0184 4044 | L1DWWC | L1D Block Writeback |
| 0x0184 4048 | L1DIBAR | L1D invalidate base address register |
| 0x0184 404C | L1DIWC | L1D invalidate word count register |
| 0x0184 4050 - 0x0184 4FFF | - | Reserved |
| 0x0184 5000 | L2WB | L2 writeback all register |
| 0x0184 5004 | L2WBINV | L2 writeback invalidate all register |
| 0x0184 5008 | L2INV | L2 Global Invalidate without writeback |
| 0x0184 500C - 0x0184 5027 | - | Reserved |
| 0x0184 5028 | L1PINV | L1P Global Invalidate |
| 0x0184 502C - 0x0184 5039 | - | Reserved |
| 0x0184 5040 | L1DWB | L1D Global Writeback |
| 0x0184 5044 | L1DWBINV | L1D Global Writeback with Invalidate |
| 0x0184 5048 | L1DINV | L1D Global Invalidate without writeback |
| 0x0184 8000 - 0x0184 803C | MAR0 - MAR15 | Reserved (corresponds to byte address 0x0000 0000 - 0x0FFF FFFF) |
| 0x0184 8040 | MAR16 | Memory Attribute Registers for ARM TCM (corresponds to byte address 0x1000 0000 - 0x10FF FFFF) |
| 0x0184 8044 - 0x0184 80FC | MAR17 - MAR63 | Reserved (corresponds to byte address 0x1100 0000 - 0x3FFF FFFF) |
| 0x0184 8100 | MAR64 | Reserved (corresponds to byte address 0x4000 0000 - 0x40FF FFFF) |
| 0x0184 8104 | MAR65 | Reserved (corresponds to byte address 0x4100 0000 - 0x41FF FFFF) |
| 0x0184 8108 - 0x0184 8124 | MAR66 - MAR73 | Memory Attribute Registers for EMIFA (corresponds to byte address 0x4200 0000 - 0x49FF FFFF) |
| 0x0184 8128 - 0x0184 812C | MAR74 - MAR75 | Reserved (corresponds to byte address 0x4A00 0000 - 0x4BFF FFFF) |
| 0x0184 8130 - 0x0184 813C | MAR76 - MAR79 | Memory Attribute Registers for VLYNQ (corresponds to byte address 0x4C00 0000 - 0x4FFF FFFF) |
| 0x0184 8140 - 0x0184 81FC | MAR80 - MAR127 | Reserved (corresponds to byte address 0x5000 0000 - 0x7FFF FFFF) |
| 0x0184 8200 - 0x0184 82FC | MAR128 - MAR191 | Memory Attribute Registers for DDR2 (corresponds to byte address 0x8000 0000 - 0xBFFF FFFF) |
| 0x0184 8300 - 0x0184 83FC | MAR192 - MAR255 | Reserved (corresponds to byte address 0xC000 0000 - 0xFFFF FFFF) |

### 3.4.3 Peripherals

The DSP has access/controllability of the following peripherals:

- HDVICP0/1
- EDMA
- McASP0/1
- 2 Timers (Timer0 and Timer1) that can each be configured as 1 64-bit or 2 32-bit timers

### 3.4.4 DSP Interrupt Controller

The DSP Interrupt Controller accepts device interrupts and appropriately maps them to the DSP's available interrupts. The DSP Interrupt Controller is briefly described in this document in the Interrupts section. For more detailed on the DSP Interrupt Controller, see the *TMS320C64x+ DSP Megamodule* Reference Guide (literature number SPRU871).


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## 3.5 Memory Map Summary

Table 3-3 shows the memory map address ranges of the device. Table 3-4 depicts the expanded map of the Configuration Space (0x0180 0000 through 0x0FFF FFFF). The device has multiple on-chip memories associated with its two processors and various subsystems. To help simplify software development a unified memory map is used where possible to maintain a consistent view of device resources across all bus masters.

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## Table 3-3. Memory Map Summary

| START ADDRESS | END ADDRESS | SIZE (Bytes) | ARM | C64x+ | EDMA/ PERIPHERAL | MASTER PERIPHERAL ACCESSIBILITY(1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Video Port | VDCE | TSIF (0/1) | EMAC | HPI | PCI | USB | VLYNQ | ATA |
| 0x0000 0000 | 0x0000 3FFF | 16K | ARM RAM0 (Instruction) | Reserved | Reserved | | | | | | | | | |
| 0x0000 4000 | 0x0000 7FFF | 16K | ARM RAM1 (Instruction) | | | | | | | | | | | |
| 0x0000 8000 | 0x0000 FFFF | 32K | ARM ROM (Instruction) | | | | | | | | | | | |
| 0x0001 0000 | 0x0001 3FFF | 16K | ARM RAM0 (Data) | | | | | | | | | | | |
| 0x0001 4000 | 0x0001 7FFF | 16K | ARM RAM1 (Data) | | | | | | | | | | | |
| 0x0001 8000 | 0x0001 FFFF | 32K | ARM ROM (Data) | | | | | | | | | | | |
| 0x0002 0000 | 0x000F FFFF | 896K | Reserved | | | | | | | | | | | |
| 0x0010 0000 | 0x003F FFFF | 3M | | | | | | | | | | | | |
| 0x0040 0000 | 0x004F FFFF | 1M | | | | | | | | | | | | |
| 0x0050 0000 | 0x005F FFFF | 1M | | | | | | | | | | | | |
| 0x0060 0000 | 0x006F FFFF | 1M | | | | | | | | | | | | |
| 0x0070 0000 | 0x007F FFFF | 1M | | | | | | | | | | | | |
| 0x0080 0000 | 0x0080 FFFF | 64K | | | | | | | | | | | | |
| 0x0081 0000 | 0x0081 7FFF | 32K | Reserved | Hole (MPPA Disable)(2) | Reserved | | | | | | | | | |
| 0x0081 8000 | 0x0083 7FFF | 128K | Reserved | L2 RAM/Cache | Reserved | | | | | | | | | |
| 0x0083 8000 | 0x008F FFFF | 800K | | Reserved | | | | | | | | | | |
| 0x0090 0000 | 0x0092 FFFF | 192K | | | | | | | | | | | | |
| 0x0093 0000 | 0x009F FFFF | 832K | | | | | | | | | | | | |
| 0x00A0 0000 | 0x00DF FFFF | 4M | | | | | | | | | | | | |
| 0x00E0 0000 | 0x00E0 7FFF | 32K | | L1P RAM/Cache | | | | | | | | | | |
| 0x00E0 8000 | 0x00EF FFFF | 992K | | Reserved | | | | | | | | | | |
| 0x00F0 0000 | 0x00F0 7FFF | 32K | | L1D RAM/Cache | | | | | | | | | | |
| 0x00F0 8000 | 0x017F FFFF | 9184K | | Reserved | | | | | | | | | | |
| 0x0180 0000 | 0x01BB FFFF | 3840K | | CFG Space | | | | | | | | | | |
| 0x01BC 0000 | 0x01BC 0FFF | 4K | ARM ETB Memory | | | | | | | | | | | |
| 0x01BC 1000 | 0x01BC 17FF | 2K | ARM ETB Registers | | | | | | | | | | | |
| 0x01BC 1800 | 0x01BC 18FF | 256 | ARM IceCrusher | | | | | | | | | | | |
| 0x01BC 1900 | 0x01BC 1BFF | 768 | Reserved | | | | | | | | | | | |
| 0x01BC 1C00 | 0x01BF FFFF | 249K | | | | | | | | | | | | |
| 0x01C0 0000 | 0x0FFF FFFF | 228M | CFG Bus Peripherals | CFG Bus Peripherals | CFG Bus Peripherals | | | | | x(3) | x(3) | | x(3) | |
| 0x1000 0000 | 0x1000 FFFF | 64K | Reserved | | Reserved | | | | | | | | | |
| 0x1001 0000 | 0x1001 3FFF | 16K | | ARM RAM0 (Data) | ARM RAM0 (Data) | | x | x | | x | x | x | x | x |
| 0x1001 4000 | 0x1001 7FFF | 16K | | ARM RAM1 (Data) | ARM RAM1 (Data) | | x | x | | x | x | x | x | x |
| 0x1001 8000 | 0x1001 FFFF | 32K | | ARM ROM (Data) | ARM ROM (Data) | | x | x | | x | x | x | x | x |
| 0x1002 0000 | 0x10FF FFFF | 16256K | | | | | | | | | | | | |
| 0x1100 0000 | 0x113F FFFF | 4M | | Reserved | Reserved | | | | | | | | | |
| 0x1140 0000 | 0x114F FFFF | 1M | | | | | | | | | | | | |
| 0x1150 0000 | 0x115F FFFF | 1M | | | | | | | | | | | | |
| 0x1160 0000 | 0x116F FFFF | 1M | | | | | | | | | | | | |
| 0x1170 0000 | 0x117F FFFF | 1M | | | | | | | | | | | | |
| 0x1180 0000 | 0x1180 FFFF | 64K | | | | | | | | | | | | |
| 0x1181 0000 | 0x1181 7FFF | 32K | Reserved | Hole (MPPA Disable)(2) | Reserved | | | | | | | | | |
| 0x1181 8000 | 0x1183 7FFF | 128K | L2 RAM/Cache | L2 RAM/Cache | L2 RAM/Cache | | | | x | x | x | x | x | x |
| 0x1183 8000 | 0x118F FFFF | 800K | Reserved | Reserved | Reserved | | | | | | | | | |
| 0x1190 0000 | 0x11DF FFFF | 5M | | | | | | | | | | | | |
| 0x11E0 0000 | 0x11E0 7FFF | 32K | L1P RAM/Cache | L1P RAM/Cache | L1P RAM/Cache | | | | | x | x | x | x | x |
| 0x11E0 8000 | 0x11EF FFFF | 992K | Reserved | Reserved | Reserved | | | | | | | | | |

(1) These peripherals have their own DMA engine or master port interface to the DMSoC system bus and ***do not*** use the EDMA for data transfers. The x symbol indicates that the peripheral has a valid connection through the device switch fabric to the memory region identified in the EDMA access column.

(2) MPPA should be used to disable the hole. For more information on MPPA, see the *TMS320C64x+ DSP Megamodule* Reference Guide (SPRU871).

(3) The HPI's, PCI's, and VLYNQ's access to the configuration bus peripherals is limited, see Table 3-4, *Configuration Memory Map Summary* for the details.


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## Table 3-3. Memory Map Summary (continued)

| START ADDRESS | END ADDRESS | SIZE (Bytes) | ARM | C64x+ | EDMA/ PERIPHERAL | MASTER PERIPHERAL ACCESSIBILITY(1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Video Port | VDCE | TSIF (0/1) | EMAC | HPI | PCI | USB | VLYNQ | ATA |
| 0x11F0 0000 | 0x11F0 7FFF | 32K | L1D RAM/Cache | L1D RAM/Cache | L1D RAM/Cache | | | | | x | x | x | x | x |
| 0x11F0 8000 | 0x11FF FFFF | 992K | Reserved | Reserved | Reserved | | | | | | | | | |
| 0x1200 0000 | 0x1FFF FFFF | 224M | | | | | | | | | | | | |
| 0x2000 0000 | 0x2000 7FFF | 32K | DDR2 Control Registers | DDR2 Control Registers | DDR2 Control Registers | | | | | | x | | | |
| 0x2000 8000 | 0x2000 FFFF | 32K | EMIFA Control Registers | EMIFA Registers | EMIFA Registers | | | | | | | | | |
| 0x2001 0000 | 0x2001 7FFF | 32K | VLYNQ Control Registers | VLYNQ Registers | VLYNQ Registers | | | | | | | | | |
| 0x2001 8000 | 0x200F FFFF | 928K | Reserved | Reserved | Reserved | | | | | | | | | |
| 0x2010 0000 | 0x2FFF FFFF | 255M | | | | | | | | | | | | |
| 0x3000 0000 | 0x3FFF FFFF | 256M | PCI Data | | PCI Data | | | | | | | | | |
| 0x4000 0000 | 0x403F FFFF | 4M | Reserved | Reserved | Reserved | | | | | | | | | |
| 0x4040 0000 | 0x4043 FFFF | 256K | | | | | | | | | | | | |
| 0x4044 0000 | 0x4047 FFFF | 256K | | | | | | | | | | | | |
| 0x4048 0000 | 0x404B FFFF | 256K | | | | | | | | | | | | |
| 0x404C 0000 | 0x404F FFFF | 256K | | | | | | | | | | | | |
| 0x4050 0000 | 0x405F FFFF | 1M | | | | | | | | | | | | |
| 0x4060 0000 | 0x4063 FFFF | 256K | Reserved | Reserved | Reserved | | | | | | | | | |
| 0x4064 0000 | 0x4067 FFFF | 256K | | | | | | | | | | | | |
| 0x4068 0000 | 0x406B FFFF | 256K | | | | | | | | | | | | |
| 0x406C 0000 | 0x406F FFFF | 256K | | | | | | | | | | | | |
| 0x4070 0000 | 0x41FF FFFF | 25M | | | | | | | | | | | | |
| 0x4200 0000 | 0x43FF FFFF | 32M | EMIFA Data ($\overline{CS2}$)(4) | EMIFA Data ($\overline{CS2}$)(4) | EMIFA Data ($\overline{CS2}$)(4) | | x | x | | | | x | x | |
| 0x4400 0000 | 0x45FF FFFF | 32M | EMIFA Data ($\overline{CS3}$)(4) | EMIFA Data ($\overline{CS3}$)(4) | EMIFA Data ($\overline{CS3}$)(4) | | x | x | | | | x | x | |
| 0x4600 0000 | 0x47FF FFFF | 32M | EMIFA Data ($\overline{CS4}$)(4) | EMIFA Data ($\overline{CS4}$)(4) | EMIFA Data ($\overline{CS4}$)(4) | | x | x | | | | x | x | |
| 0x4800 0000 | 0x49FF FFFF | 32M | EMIFA Data ($\overline{CS5}$)(4) | EMIFA Data ($\overline{CS5}$)(4) | EMIFA Data ($\overline{CS5}$)(4) | | x | x | | | | x | x | |
| 0x4A00 0000 | 0x4BFF FFFF | 32M | Reserved | Reserved | Reserved | | | | | | | | | |
| 0x4C00 0000 | 0x4FFF FFFF | 64M | VLYNQ (Remote Data) | VLYNQ (Remote Data) | VLYNQ (Remote Data) | | x | x | x | x | x | x | | x |
| 0x5000 0000 | 0x7FFF FFFF | 768M | Reserved | Reserved | Reserved | | | | | | | | | |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory | DDR2 Memory | DDR2 Memory | x | x | x | x | x | x | x | x | x |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved | Reserved | Reserved | | | | | | | | | |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved | Reserved | Reserved | | | | | | | | | |

(4) EMIFA $\overline{CS0}$ and $\overline{CS1}$ are ***not*** functionally supported on the DM6467T, and therefore, are ***not*** pinned out.

## Table 3-4. Configuration Memory Map Summary

| START ADDRESS | END ADDRESS | SIZE (Bytes) | ARM/EDMA | C64x+ | MASTER PERIPHERAL ACCESSIBILITY | | |
|---|---|---|---|---|---|---|---|
| | | | | | HPI | PCI | VLYNQ |
| 0x0180 0000 | 0x0180 FFFF | 64K | Reserved | C64x+ Interrupt Controller | | | |
| 0x0181 0000 | 0x0181 0FFF | 4K | | C64x+ Powerdown Controller | | | |
| 0x0181 1000 | 0x0181 1FFF | 4K | | C64x+ Security ID | | | |
| 0x0181 2000 | 0x0181 2FFF | 4K | | C64x+ Revision ID | | | |
| 0x0182 0000 | 0x0182 FFFF | 64K | | C64x+ EMC | | | |
| 0x0183 0000 | 0x0183 FFFF | 64K | | Reserved | | | |
| 0x0184 0000 | 0x0184 FFFF | 64K | | C64x+ Memory System | | | |
| 0x0185 0000 | 0x01BB FFFF | 3520K | | Reserved | | | |
| 0x01BC 0000 | 0x01BC 00FF | 256 | ARM ETB Memory | Reserved | | | |
| 0x01BC 0100 | 0x01BC 01FF | 256 | | | | | |
| 0x01BC 0200 | 0x01BC 0FFF | 3.5K | | | | | |
| 0x01BC 1000 | 0x01BC 17FF | 2K | ARM ETB Registers | | | | |
| 0x01BC 1800 | 0x01BC 18FF | 256 | ARM Ice Crusher | | | | |
| 0x01BC 1900 | 0x01BF FFFF | 255744 | Reserved | | | | |
| 0x01C0 0000 | 0x01C0 FFFF | 64K | EDMA CC | EDMA CC | | | |
| 0x01C1 0000 | 0x01C1 03FF | 1K | EDMA TC0 | EDMA TC0 | | | |
| 0x01C1 0400 | 0x01C1 07FF | 1K | EDMA TC1 | EDMA TC1 | | | |
| 0x01C1 0800 | 0x01C1 0BFF | 1K | EDMA TC2 | EDMA TC2 | | | |
| 0x01C1 0C00 | 0x01C1 0FFF | 1K | EDMA TC3 | EDMA TC3 | | | |
| 0x01C1 1000 | 0x01C1 1FFF | 4K | Reserved | Reserved | | | |
| 0x01C1 2000 | 0x01C1 23FF | 1K | Video Port | | | | |
| 0x01C1 2400 | 0x01C1 27FF | 1K | Reserved | Reserved | | | |
| 0x01C1 2800 | 0x01C1 2FFF | 2K | VDCE | | | | |
| 0x01C1 3000 | 0x01C1 33FF | 1K | TSIF0 | | | | |
| 0x01C1 3400 | 0x01C1 37FF | 1K | TSIF1 | | | | |
| 0x01C1 3800 | 0x01C1 9FFF | 26K | Reserved | Reserved | | | |
| 0x01C1 A000 | 0x01C1 A7FF | 2K | PCI Control Registers | | | | |
| 0x01C1 A800 | 0x01C1 FFFF | 22K | Reserved | Reserved | | | |
| 0x01C2 0000 | 0x01C2 03FF | 1K | UART0 | | x | x | x |
| 0x01C2 0400 | 0x01C2 07FF | 1K | UART1 | | x | x | x |
| 0x01C2 0800 | 0x01C2 0BFF | 1K | UART2 | | x | x | x |
| 0x01C2 0C00 | 0x01C2 0FFF | 1K | Reserved | Reserved | x | x | x |
| 0x01C2 1000 | 0x01C2 13FF | 1K | I2C | | x | x | x |
| 0x01C2 1400 | 0x01C2 17FF | 1K | Timer0 | Timer0 | x | x | x |
| 0x01C2 1800 | 0x01C2 1BFF | 1K | Timer1 | Timer1 | x | x | x |
| 0x01C2 1C00 | 0x01C2 1FFF | 1K | Timer2 (Watchdog) | | x | x | x |
| 0x01C2 2000 | 0x01C2 23FF | 1K | PWM0 | | x | x | x |
| 0x01C2 2400 | 0x01C2 27FF | 1K | PWM1 | | x | x | x |
| 0x01C2 2800 | 0x01C2 5FFF | 14K | Reserved | Reserved | x | x | x |
| 0x01C2 6000 | 0x01C2 63FF | 1K | CRGEN0 | | x | x | x |
| 0x01C2 6400 | 0x01C2 67FF | 1K | CRGEN1 | | x | x | x |
| 0x01C2 6800 | 0x01C3 FFFF | 102K | Reserved | Reserved | x | x | x |
| 0x01C4 0000 | 0x01C4 07FF | 2K | System Module | System Module | x | x | x |
| 0x01C4 0800 | 0x01C4 0BFF | 1K | PLL Controller 1 | | x | x | x |
| 0x01C4 0C00 | 0x01C4 0FFF | 1K | PLL Controller 2 | | x | x | x |
| 0x01C4 1000 | 0x01C4 1FFF | 4K | Power and Sleep Controller | Power and Sleep Controller | x | x | x |
| 0x01C4 2000 | 0x01C4 7FFF | 24K | Reserved | Reserved | x | x | x |
| 0x01C4 8000 | 0x01C4 83FF | 1K | ARM Interrupt Controller | Reserved | x | x | x |
| 0x01C4 8400 | 0x01C6 3FFF | 111K | Reserved | Reserved | x | x | x |
| 0x01C6 4000 | 0x01C6 5FFF | 8K | USB2.0 Registers / RAM | | x | x | x |


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**Table 3-4. Configuration Memory Map Summary (continued)**

| START ADDRESS | END ADDRESS | SIZE (Bytes) | ARM/EDMA | C64x+ | MASTER PERIPHERAL ACCESSIBILITY | | |
|---|---|---|---|---|---|---|---|
| | | | | | HPI | PCI | VLYNQ |
| 0x01C6 6000 | 0x01C6 67FF | 2K | ATA | | x | x | x |
| 0x01C6 6800 | 0x01C6 6FFF | 2K | SPI | | x | x | x |
| 0x01C6 7000 | 0x01C6 77FF | 2K | GPIO | | x | x | x |
| 0x01C6 7800 | 0x01C6 7FFF | 2K | HPI | HPI | x | x | x |
| 0x01C6 8000 | 0x01C7 FFFF | 96K | Reserved | Reserved | x | x | x |
| 0x01C8 0000 | 0x01C8 0FFF | 4K | EMAC Control Registers | Reserved | x | x | x |
| 0x01C8 1000 | 0x01C8 1FFF | 4K | EMAC Control Module Registers | | x | x | x |
| 0x01C8 2000 | 0x01C8 3FFF | 8K | EMAC Control Module RAM | | x | x | x |
| 0x01C8 4000 | 0x01C8 47FF | 2K | MDIO Control Registers | | x | x | x |
| 0x01C8 4800 | 0x01D0 0FFF | 498K | Reserved | Reserved | x | x | x |
| 0x01D0 1000 | 0x01D0 13FF | 1K | McASP0 Registers | McASP0 Registers | x | x | x |
| 0x01D0 1400 | 0x01D0 17FF | 1K | McASP0 Data Port | McASP0 Data Port | x | x | x |
| 0x01D0 1800 | 0x01D0 1BFF | 1K | McASP1 Registers | McASP1 Registers | x | x | x |
| 0x01D0 1C00 | 0x01D0 1FFF | 1K | McASP1 Data Port | McASP1 Data Port | x | x | x |
| 0x01D0 2000 | 0x01DF FFFF | 1016K | Reserved | Reserved | | | |
| 0x01E0 0000 | 0x01FF FFFF | 2M | Reserved | Reserved | | | |
| 0x0200 0000 | 0x021F FFFF | 2M | Reserved | Reserved | | | |
| 0x0220 0000 | 0x023F FFFF | 2M | Reserved | Reserved | | | |
| 0x0240 0000 | 0x0FFF FFFF | 220M | Reserved | Reserved | | | |

## 3.6 Pin Assignments

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. For more information on pin muxing, see Section 4.7, *Multiplexed Pin Configurations*, of this document.

### *3.6.1 Pin Map (Bottom View)*

Figure 3-2 through Figure 3-7 show the bottom view of the package pin assignments in six quadrants (A, B, C, D, E, and F).

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| AC | $V_{SS}$ | $V_{SS}$ | GP[4]/ STC_CLKIN | VP_DOUT1/ BTMODE1 | VP_DOUT6/ DSPBOOT | VP_DOUT5/ PCIEN | VP_DOUT14/ TS1_PSTIN | VP_DOUT9/ TS1_ENAO | AC |
| AB | $V_{SS}$ | AHCLKR0 | GP[3]/ AUDIO_CLK0 | TOUT1U | VP_DOUT0/ BTMODE0 | VP_DOUT3/ BTMODE3 | VP_DOUT7 | VP_DOUT15/ TS1_DIN | AB |
| AA | ACLKX0 | ACLKR0 | AMUTEIN0 | GP[2]/ AUDIO_CLK1 | TOUT1L | TINP0U | VP_DOUT4/ CS2BW | VP_DOUT12/ TS1_WAITO | AA |
| Y | AHCLKX0 | AMUTE0 | AFSR0 | AFSX0 | TOUT2 | TINP1L | TINP0L | VP_DOUT2/ BTMODE2 | Y |
| W | ACLKX1 | AHCLKX1 | AXR0[3] | AXR0[2] | GP[0] | $\overline{\text{RESET}}$ | TOUT0U | TOUT0L | W |
| V | SPI_CLK | AXR1[0] | AXR0[0] | AXR0[1] | GP[1] | $V_{SS}$ | $DV_{DD33}$ | $DV_{DD33}$ | V |
| U | VLYNQ_ CLOCK | $\overline{\text{VLYNQ_}}$ $\overline{\text{SCRUN}}$ | $\overline{\text{SPI_CS1}}$ | SDA | SCL | $V_{SS}$ | $DV_{DD33}$ | $CV_{DD}$ | U |
| T | VLYNQ_TXD1 | VLYNQ_TXD2 | VLYNQ_TXD3 | $\overline{\text{SPI_CS0}}$ | $\overline{\text{SPI_EN}}$ | $V_{SS}$ | $DV_{DD33}$ | $CV_{DD}$ | T |
| R | MTCLK | VLYNQ_RXD2 | VLYNQ_RXD3 | VLYNQ_TXD0 | SPI_SOMI | $V_{SS}$ | $DV_{DD33}$ | $CV_{DD}$ | R |
| P | MTXD7 | GMTCLK | VLYNQ_RXD1 | VLYNQ_RXD0 | SPI_SIMO | $V_{SS}$ | $CV_{DD}$ | $CV_{DD}$ | P |
| N | MTXD3 | MTXD4 | MTXD5 | MTXD6 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | N |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |

| | | |
|---|---|---|
| A | B | C |
| D | E | F |

**Figure 3-2. Pin Map [Section A]**


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| | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|
| AC | VP_CLKIN3/ TS1_CLKO | VP_CLKO3/ TS0_CLKO | TS1_CLKIN | $\overline{\text{UCTS0}}$/ USD0 | VP_CLKIN0 | VP_DIN4/ TS0_DOUT4/ TS1_WAITO | VP_DIN0/ TS0_DOUT0 | VP_DIN8/ TS0_DIN0 | AC |
| AB | VP_DOUT8/ TS1_WAITIN | VP_DOUT11/ TS1_DOUT | $\overline{\text{UDSR0}}$/ TS0_PSTO/ GP[37] | $V_{SS}$ | URXD0/ TS1_DIN | VP_DIN5/ TS0_DOUT5/ TS1_EN_WAITO | VP_DIN1/ TS0_DOUT1 | VP_DIN9/ TS0_DIN1 | AB |
| AA | VP_CLKO2 | VP_DOUT10/ TS1_PSTO | $\overline{\text{UDCD0}}$/ TS0_WAITIN/ GP[38] | $DV_{DD33}$ | $\overline{\text{URTS0}}$/ UIRTX0/ TS1_EN_WAITO | VP_DIN6/ TS0_DOUT6/ TS1_PSTIN | VP_DIN2/ TS0_DOUT2 | VP_DIN10/ TS0_DIN2 | AA |
| Y | VP_DOUT13/ TS1_EN_WAITO | VP_CLKIN2 | $\overline{\text{URIN0}}$/ GP[8]/ TS1_WAITIN | $\overline{\text{UDTR0}}$/ TS0_ENAO/ GP[36] | UTXD0/ URCTX0/ TS1_PSTIN | VP_DIN7/ TS0_DOUT7/ TS1_DIN | VP_DIN3/ TS0_DOUT3 | VP_DIN11/ TS0_DIN3 | Y |
| W | $DV_{DD33}$ | $DV_{DD33}$ | $DV_{DD33}$ | $DV_{DD33}$ | $DV_{DD33}$ | $DV_{DD33}$ | $DV_{DD33}$ | $DV_{DD33}$ | W |
| V | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | V |
| U | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | U |
| T | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | T |
| R | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | R |
| P | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | P |
| N | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | N |
| | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

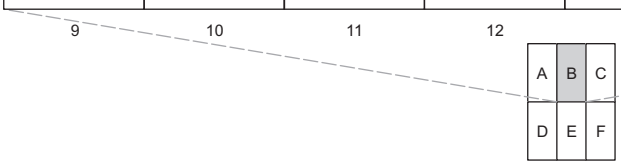
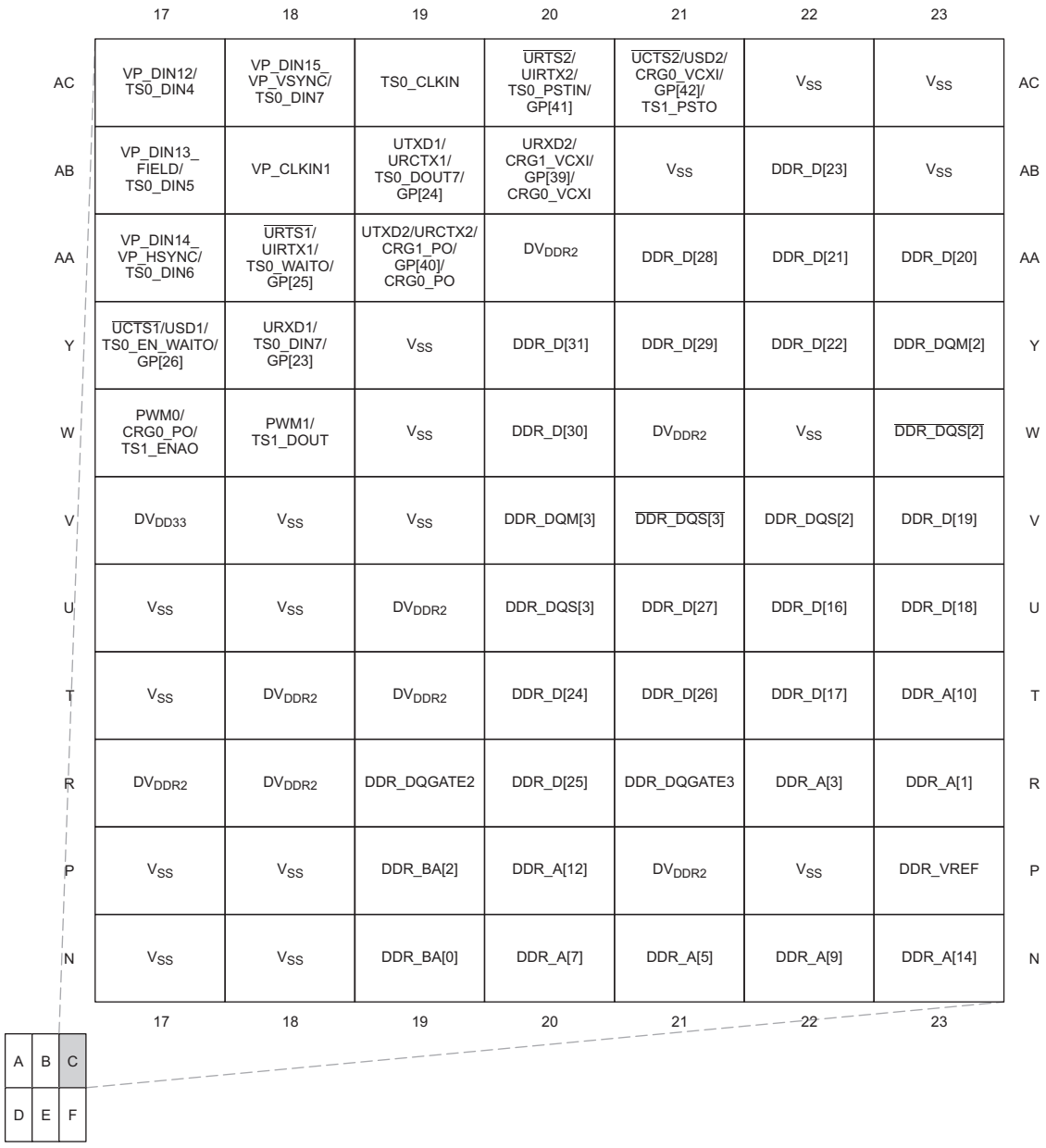



**Figure 3-3. Pin Map [Section B]**



| | 17 | 18 | 19 | 20 | 21 | 22 | 23 | |
|---|---|---|---|---|---|---|---|---|
| AC | VP_DIN12/ TS0_DIN4 | VP_DIN15_ VP_VSYNC/ TS0_DIN7 | TS0_CLKIN | URTS2/ UIRTX2/ TS0_PSTIN/ GP[41] | UCTS2/USD2/ CRG0_VCXI/ GP[42]/ TS1_PSTO | $V_{SS}$ | $V_{SS}$ | AC |
| AB | VP_DIN13_ FIELD/ TS0_DIN5 | VP_CLKIN1 | UTXD1/ URCTX1/ TS0_DOUT7/ GP[24] | URXD2/ CRG1_VCXI/ GP[39]/ CRG0_VCXI | $V_{SS}$ | DDR_D[23] | $V_{SS}$ | AB |
| AA | VP_DIN14_ VP_HSYNC/ TS0_DIN6 | URTS1/ UIRTX1/ TS0_WAITO/ GP[25] | UTXD2/URCTX2/ CRG1_PO/ GP[40]/ CRG0_PO | $DV_{DDR2}$ | DDR_D[28] | DDR_D[21] | DDR_D[20] | AA |
| Y | UCTS1/USD1/ TS0_EN_WAITO/ GP[26] | URXD1/ TS0_DIN7/ GP[23] | $V_{SS}$ | DDR_D[31] | DDR_D[29] | DDR_D[22] | DDR_DQM[2] | Y |
| W | PWM0/ CRG0_PO/ TS1_ENAO | PWM1/ TS1_DOUT | $V_{SS}$ | DDR_D[30] | $DV_{DDR2}$ | $V_{SS}$ | DDR_DQS[2] | W |
| V | $DV_{DD33}$ | $V_{SS}$ | $V_{SS}$ | DDR_DQM[3] | DDR_DQS[3] | DDR_DQS[2] | DDR_D[19] | V |
| U | $V_{SS}$ | $V_{SS}$ | $DV_{DDR2}$ | DDR_DQS[3] | DDR_D[27] | DDR_D[16] | DDR_D[18] | U |
| T | $V_{SS}$ | $DV_{DDR2}$ | $DV_{DDR2}$ | DDR_D[24] | DDR_D[26] | DDR_D[17] | DDR_A[10] | T |
| R | $DV_{DDR2}$ | $DV_{DDR2}$ | DDR_DQGATE2 | DDR_D[25] | DDR_DQGATE3 | DDR_A[3] | DDR_A[1] | R |
| P | $V_{SS}$ | $V_{SS}$ | DDR_BA[2] | DDR_A[12] | $DV_{DDR2}$ | $V_{SS}$ | DDR_VREF | P |
| N | $V_{SS}$ | $V_{SS}$ | DDR_BA[0] | DDR_A[7] | DDR_A[5] | DDR_A[9] | DDR_A[14] | N |
| | 17 | 18 | 19 | 20 | 21 | 22 | 23 | |



**Figure 3-4. Pin Map [Section C]**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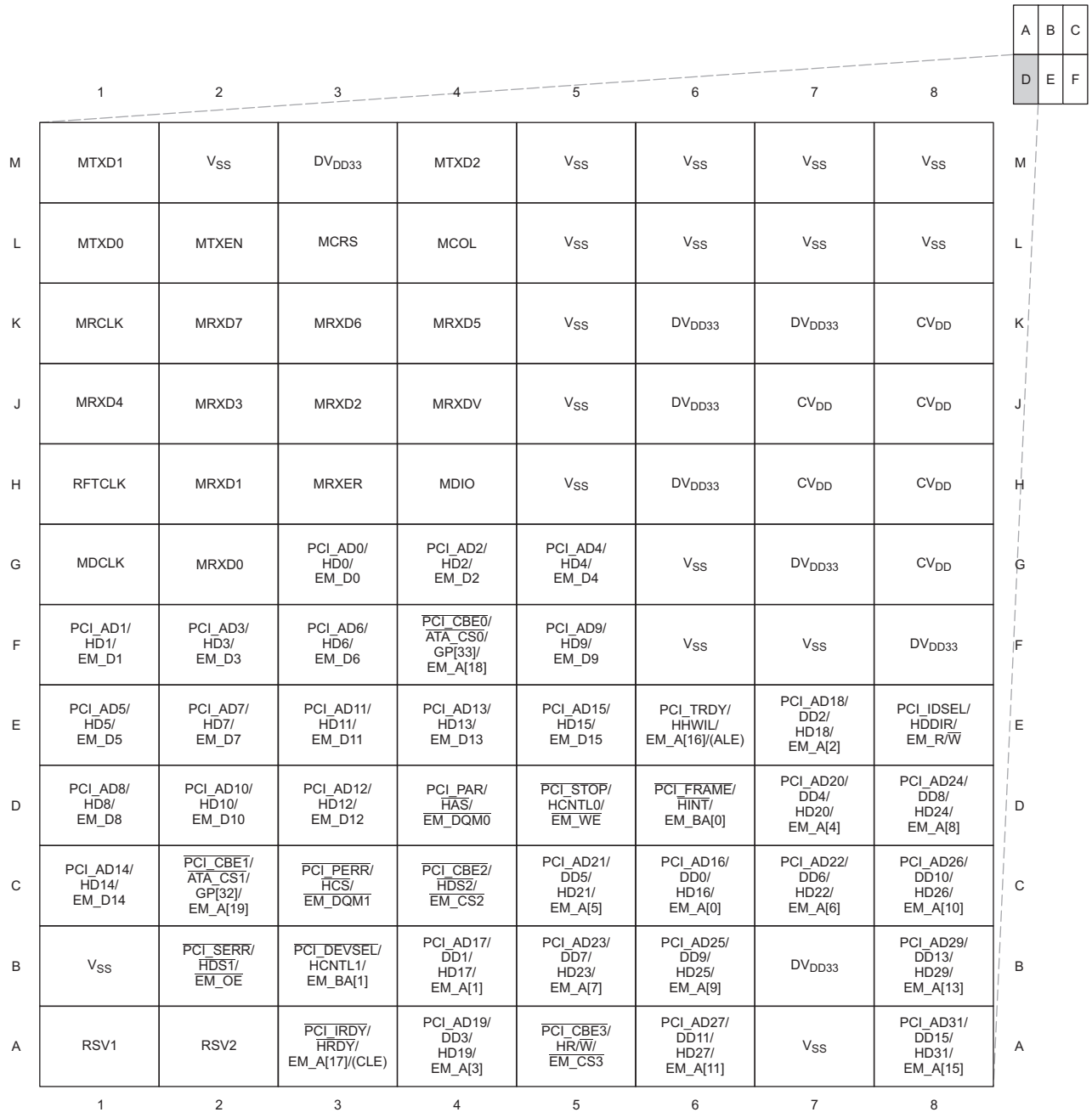

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| M | MTXD1 | $V_{SS}$ | $DV_{DD33}$ | MTXD2 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | M |
| L | MTXD0 | MTXEN | MCRS | MCOL | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | L |
| K | MRCLK | MRXD7 | MRXD6 | MRXD5 | $V_{SS}$ | $DV_{DD33}$ | $DV_{DD33}$ | $CV_{DD}$ | K |
| J | MRXD4 | MRXD3 | MRXD2 | MRXDV | $V_{SS}$ | $DV_{DD33}$ | $CV_{DD}$ | $CV_{DD}$ | J |
| H | RFTCLK | MRXD1 | MRXER | MDIO | $V_{SS}$ | $DV_{DD33}$ | $CV_{DD}$ | $CV_{DD}$ | H |
| G | MDCLK | MRXD0 | PCI_AD0/ HD0/ EM_D0 | PCI_AD2/ HD2/ EM_D2 | PCI_AD4/ HD4/ EM_D4 | $V_{SS}$ | $DV_{DD33}$ | $CV_{DD}$ | G |
| F | PCI_AD1/ HD1/ EM_D1 | PCI_AD3/ HD3/ EM_D3 | PCI_AD6/ HD6/ EM_D6 | PCI_CBE0/ ATA_CS0/ GP[33]/ EM_A[18] | PCI_AD9/ HD9/ EM_D9 | $V_{SS}$ | $V_{SS}$ | $DV_{DD33}$ | F |
| E | PCI_AD5/ HD5/ EM_D5 | PCI_AD7/ HD7/ EM_D7 | PCI_AD11/ HD11/ EM_D11 | PCI_AD13/ HD13/ EM_D13 | PCI_AD15/ HD15/ EM_D15 | PCI_TRDY/ HHWIL/ EM_A[16]/(ALE) | PCI_AD18/ DD2/ HD18/ EM_A[2] | PCI_IDSEL/ HDDIR/ EM_R/W | E |
| D | PCI_AD8/ HD8/ EM_D8 | PCI_AD10/ HD10/ EM_D10 | PCI_AD12/ HD12/ EM_D12 | PCI_PAR/ HAS/ EM_DQM0 | PCI_STOP/ HCNTL0/ EM_WE | PCI_FRAME/ HINT/ EM_BA[0] | PCI_AD20/ DD4/ HD20/ EM_A[4] | PCI_AD24/ DD8/ HD24/ EM_A[8] | D |
| C | PCI_AD14/ HD14/ EM_D14 | PCI_CBE1/ ATA_CS1/ GP[32]/ EM_A[19] | PCI_PERR/ HCS/ EM_DQM1 | PCI_CBE2/ HDS2/ EM_CS2 | PCI_AD21/ DD5/ HD21/ EM_A[5] | PCI_AD16/ DD0/ HD16/ EM_A[0] | PCI_AD22/ DD6/ HD22/ EM_A[6] | PCI_AD26/ DD10/ HD26/ EM_A[10] | C |
| B | $V_{SS}$ | PCI_SERR/ HDS1/ EM_OE | PCI_DEVSEL/ HCNTL1/ EM_BA[1] | PCI_AD17/ DD1/ HD17/ EM_A[1] | PCI_AD23/ DD7/ HD23/ EM_A[7] | PCI_AD25/ DD9/ HD25/ EM_A[9] | $DV_{DD33}$ | PCI_AD29/ DD13/ HD29/ EM_A[13] | B |
| A | RSV1 | RSV2 | PCI_IRDY/ HRDY/ EM_A[17]/(CLE) | PCI_AD19/ DD3/ HD19/ EM_A[3] | PCI_CBE3/ HR/W/ EM_CS3 | PCI_AD27/ DD11/ HD27/ EM_A[11] | $V_{SS}$ | PCI_AD31/ DD15/ HD31/ EM_A[15] | A |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |

**Figure 3-5. Pin Map [Section D]**

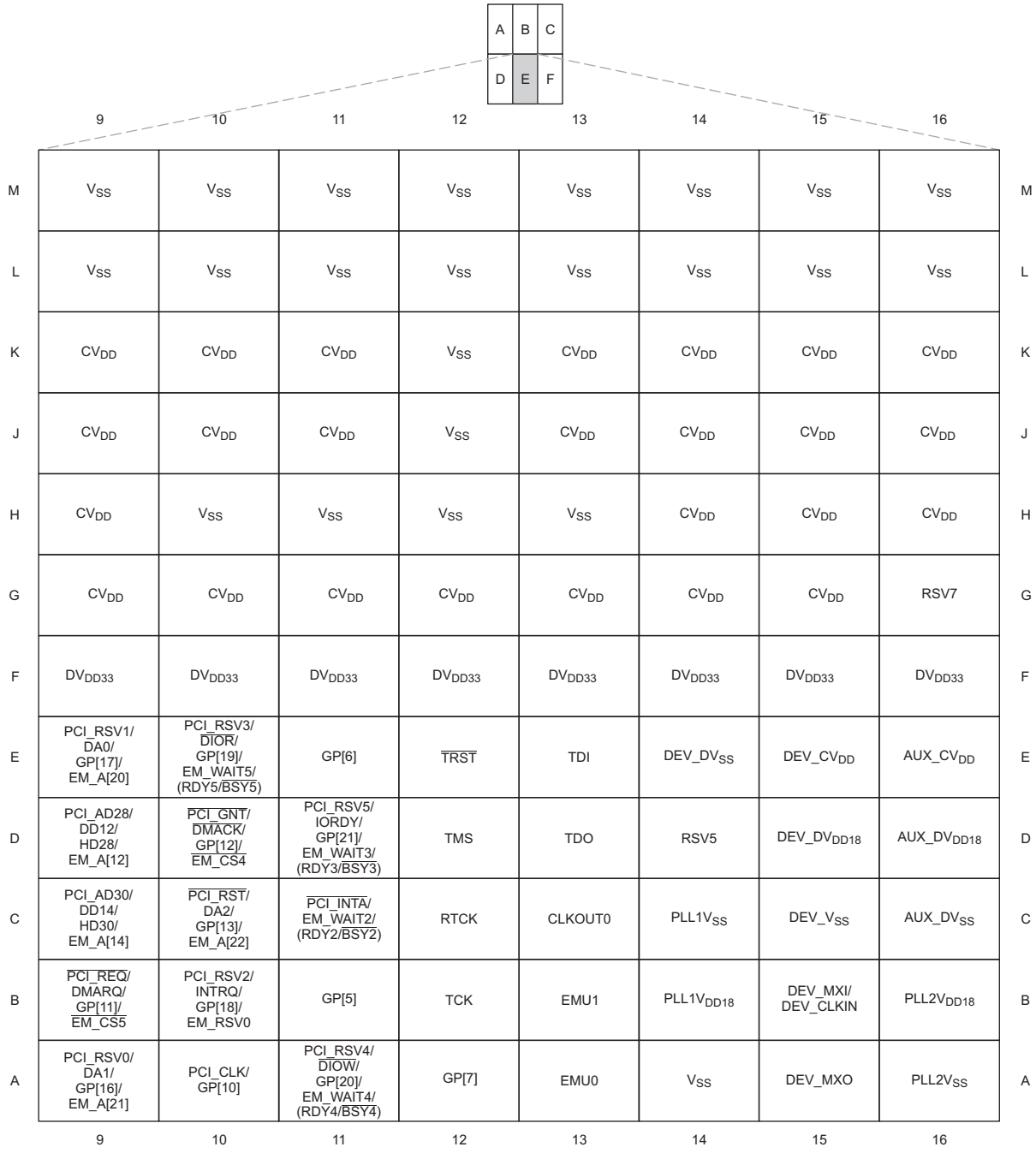


**Figure 3-6. Pin Map [Section E]**


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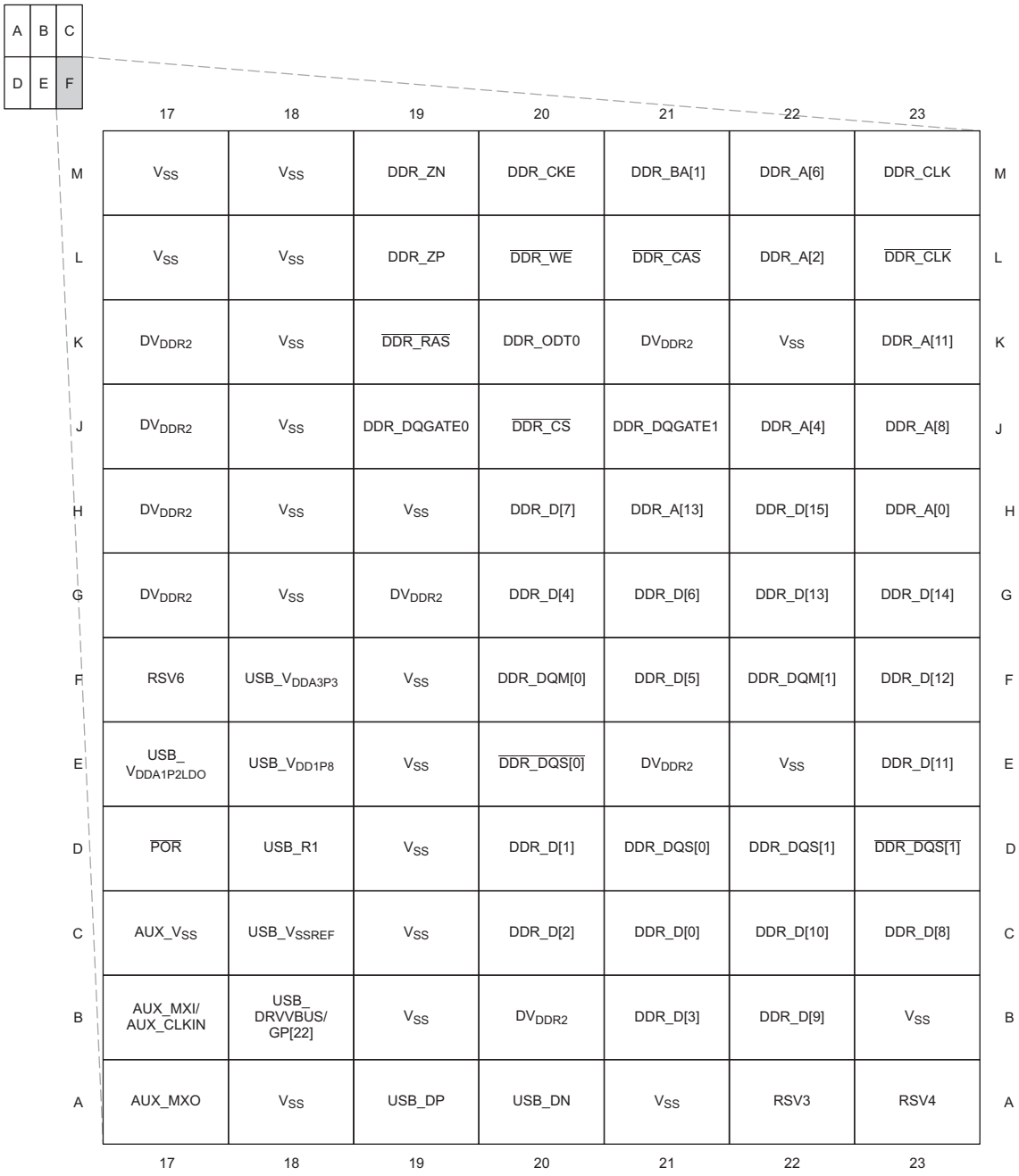


**Figure 3-7. Pin Map [Section F]**

## 3.7 Terminal Functions

The terminal functions tables (Table 3-5 through Table 3-32) identify the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pin, and see the *Device Configurations* section of this data manual.


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## Table 3-5. BOOT Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2)(3) | DESCRIPTION |
|---|---|---|---|---|
| **BOOT** | | | | |
| ARM Boot Mode configuration bits. These pins are multiplexed between ARM boot mode and the Video Port Interface (VPIF). At reset, the boot mode inputs BTMODE[3:0] are sampled to determine the ARM boot configuration. See below the boot modes set by these inputs. For more details on the types of boot modes, see the Section 4.4.1, *Boot Modes*. After reset, these pins are Video port data outputs 3 through 0 (VP_DOUT[3:0]). | | | | |
| | | | | **BTMODE[3:0]** / **ARM Boot Mode** |
| VP_DOUT0/ **BTMODE0** | AB5 | I/O/Z | IPD $DV_{DD33}$ | 0000 — Emulation Boot (PCIEN = 0)<br>0001 — Reserved<br>0010 — HPI Boot (16-Bit width) (if PCIEN = 0) or PCI Boot without auto-initialization (if PCIEN = 1)<br>0011 — HPI Boot (32-Bit width) (if PCIEN = 0) or PCI Boot with auto-initialization (if PCIEN = 1) |
| VP_DOUT1/ **BTMODE1** | AC4 | I/O/Z | IPD $DV_{DD33}$ | 0100 — EMIFA Direct Boot (ROM/NOR) (PCIEN = 0) [error if PCIEN = 1; defaults to UART0]<br>0101 — Reserved<br>0110 — I2C Boot<br>0111 — NAND Flash Boot (PCIEN = 0) [error if PCIEN = 1] |
| VP_DOUT2/ **BTMODE2** | Y8 | I/O/Z | IPD $DV_{DD33}$ | 1000 — UART0 Boot<br>1001 — Reserved<br>1010 — Reserved<br>1011 — Reserved |
| VP_DOUT3/ **BTMODE3** | AB6 | I/O/Z | IPD $DV_{DD33}$ | 1100 - 1101 — Reserved<br>1110 — SPI Boot<br>1111 — Reserved |
| **DEVICE CONTROL** | | | | |
| VP_DOUT4/ **CS2BW** | AA7 | I/O/Z | IPD $DV_{DD33}$ | EMIFA CS2 space data bus width. This pin is multiplexed between EMIFA control and the VPIF. At reset, the input state is sampled to set the EMIFA data bus width for the CS2 (boot) chip select region.<br>For an 8-bit-wide EMIFA data bus, CS2BW = 0.<br>For a 16-bit-wide EMIFA data bus, CS2BW = 1.<br>After reset, this pin is video port data output 4 (VP_DOUT4). |
| VP_DOUT5/ **PCIEN** | AC6 | I/O/Z | IPD $DV_{DD33}$ | PCI Enable. This pin is multiplexed between PCI Control and the VPIF. At reset, the input state is sampled to enable/disable the PCI interface pin multiplexing. **Note:** When PCI boot mode is ***not*** used, for proper device operation out of reset PCIEN ***must*** be "0".<br>0 = PCI pin function is disabled; EMIFA or HPI pin function enabled<br>1 = PCI pin function is enabled<br>After reset, this pin is video port data output 5 (VP_DOUT5).- |
| VP_DOUT6/ **DSPBOOT** | AC5 | I/O/Z | IPD $DV_{DD33}$ | DSP boot source bit. This pin is multiplexed between DSP boot and the VPIF. At reset, the input state is sampled to set the DSP boot source DSPBOOT.<br>The DSP is booted by the ARM when DSPBOOT = 0.<br>The DSP boots from EMIFA when DSPBOOT = 1 (and ARM HPI or PCI boot mode is ***not*** selected).<br>After reset, this pin is video port data output 6 (VP_DOUT6). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-6. Oscillator/PLL Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) | DESCRIPTION |
|---|---|---|---|---|
| **OSCILLATOR, PLL** | | | | |
| DEV_MXI/ DEV_CLKIN | B15 | I | $DEV_DV_{DD18}$ | Crystal input DEV_MXI for DEV oscillator (system oscillator, between 27 MHz and 35 MHz, typically 33 MHz or 33.3 MHz). If the internal oscillator is bypassed, this pin is the 1.8-V external oscillator clock input. |
| DEV_MXO | A15 | O | $DEV_DV_{DD18}$ | Crystal output for DEV oscillator. If the internal oscillator is bypassed, DEV_MXO should be left as a No Connect. |
| $DEV_DV_{DD18}$ | D15 | S | (3) | 1.8-V power supply for DEV oscillator. If the internal oscillator is bypassed, $DEV_DV_{DD18}$ should still be connected to the 1.8-V power supply. |
| $DEV_DV_{SS}$ | E14 | GND | (3) | I/O ground for DEV oscillator. If the internal oscillator is bypassed, $DEV_DV_{SS}$ should be connected to ground $V_{SS}$. |
| $DEV_CV_{DD}$ | E15 | S | (3) | 1.3-V power supply for DEV oscillator. If the internal oscillator is bypassed, $DEV_CV_{DD}$ should be connected to the 1.3-V power supply ($CV_{DD}$). |
| $DEV_V_{SS}$ | C15 | GND | (3) | Ground for DEV oscillator. Connect to crystal load capacitors. ***Do not*** connect to board ground ($V_{SS}$). If the internal oscillator is bypassed, $DEV_V_{SS}$ should still be connected to ground $V_{SS}$. |
| AUX_MXI/ AUX_CLKIN | B17 | I | $AUX_DV_{DD18}$ | Crystal input for Auxiliary (AUX) oscillator (24/48 MHz for USB, and UART2/1/0 and McASP1/0). If the internal oscillator is bypassed, this pin is the 1.8-V external oscillator clock input. When the peripheral ***is not*** used, AUX_MXI should be left as a No Connect. |
| AUX_MXO | A17 | O | $AUX_DV_{DD18}$ | Crystal output for AUX oscillator. If the internal oscillator is bypassed, AUX_MXO should be left as a No Connect. When the peripheral ***is not*** used, AUX_MXO should be left as a No Connect. |
| $AUX_DV_{DD18}$ | D16 | S | (3) | 1.8-V power supply for AUX oscillator. If the internal oscillator is bypassed, $AUX_DV_{DD18}$ should still be connected to the 1.8-V power supply. When the peripheral ***is not*** used, $AUX_DV_{DD18}$ should be connected to the 1.8-V power supply. |
| $AUX_DV_{SS}$ | C16 | GND | (3) | I/O ground for AUX oscillator. If the internal oscillator is bypassed, $AUX_DV_{SS}$ should be connected to ground ($V_{SS}$). When the peripheral ***is not*** used, $AUX_DV_{SS}$ should be connected to ground ($V_{SS}$). |
| $AUX_CV_{DD}$ | E16 | S | (3) | 1.3-V power supply for AUX oscillator. If the internal oscillator is bypassed, $AUX_CV_{DD}$ should be connected to the 1.3-V power supply ($CV_{DD}$). When the peripheral ***is not*** used, $AUX_CV_{DD}$ should be connected to the 1.3-V power supply ($CV_{DD}$). |
| $AUX_V_{SS}$ | C17 | GND | (3) | Ground for AUX oscillator. Connect to crystal load capacitors. ***Do not*** connect to board ground ($V_{SS}$). If the internal oscillator is bypassed, $AUX_V_{SS}$ should still be connected to ground ($V_{SS}$). When the peripheral ***is not*** used, $AUX_V_{SS}$ should be connected to ground ($V_{SS}$). |
| $PLL1V_{DD18}$ | B14 | S | (3) | 1.8-V power supply for PLLs. |
| $PLL2V_{DD18}$ | B16 | | | |
| $PLL1V_{SS}$ | C14 | GND | (3) | Ground for PLLs. |
| $PLL2V_{SS}$ | A16 | | | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) Specifies the operating I/O supply voltage for each signal
(3) For more information, see the *Recommended Operating Conditions* table


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### Table 3-7. Clock Generator Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **CLOCK GENERATOR** | | | | |
| CLKOUT0 | C13 | O/Z | $DV_{DD33}$ | Configurable output clock. |
| GP[3]/ **AUDIO_CLK0** | AB3 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between GPIO and the Audio Clock Selector. For the audio clock selector, this pin is the configurable AUDIO_CLK0 output. |
| GP[2]/ **AUDIO_CLK1** | AA4 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between GPIO and the Audio Clock Selector. For the audio clock selector, this pin is the configurable AUDIO_CLK1 output. |
| GP[4]/ **STC_CLKIN** | AC3 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between GPIO and the TSIF Clock Selector. For TSIF, this pin is the STC_CLKIN which can be used as an external clock source for the TSIF counters or as TSIF output clock. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

### Table 3-8. RESET and JTAG Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **RESET** | | | | |
| $\overline{\text{RESET}}$ | W6 | I | IPU $DV_{DD33}$ | Device reset. |
| $\overline{\text{POR}}$ | D17 | I | IPU $DV_{DD33}$ | Power-on reset. |
| **JTAG** | | | | |
| TMS | D12 | I | IPU $DV_{DD33}$ | JTAG test-port mode select input. For proper device operation, ***do not*** oppose the IPU on this pin. |
| TDO | D13 | O/Z | – $DV_{DD33}$ | JTAG test-port data output. |
| TDI | E13 | I | IPU $DV_{DD33}$ | JTAG test-port data input. |
| TCK | B12 | I | IPU $DV_{DD33}$ | JTAG test-port clock input. |
| RTCK | C12 | O/Z | – $DV_{DD33}$ | JTAG test-port return clock output. |
| $\overline{\text{TRST}}$ | E12 | I | IPD $DV_{DD33}$ | JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see the IEEE 1149.1 JTAG compatibility statement portion of this data manual. |
| EMU1 | B13 | I/O/Z | IPU $DV_{DD33}$ | Emulation pin 1 |
| EMU0 | A13 | I/O/Z | IPU $DV_{DD33}$ | Emulation pin 0 |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-9. Asynchronous External Memory Interface (EMIFA) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **EMIFA BOOT CONFIGURATION** | | | | |
| VP_DOUT4/ **CS2BW** | AA7 | I/O/Z | IPD $DV_{DD33}$ | EMIFA CS2 space data bus width. This pin is multiplexed between EMIFA control and the VPIF. At reset, the input state is sampled to set the EMIFA data bus width for the CS2 (boot) chip select region.<br>For an 8-bit-wide EMIFA data bus, CS2BW = 0.<br>For a 16-bit-wide EMIFA data bus, CS2BW = 1.<br>After reset, this pin is video port data output 4 (VP_DOUT4). |
| VP_DOUT6/ **DSPBOOT** | AC5 | I/O/Z | IPD $DV_{DD33}$ | DSP boot source bit. This pin is multiplexed between DSP boot and the VPIF. At reset, the input state is sampled to set the DSP boot source DSPBOOT.<br>The DSP is booted by the ARM when DSPBOOT = 0.<br>The DSP boots from EMIFA when DSPBOOT=1.<br>After reset, this pin is video port data output 6 (VP_DOUT6). |
| **EMIFA FUNCTIONAL PINS: ASYNC** | | | | |
| PCI_CBE2/ HDS2/ **EM_CS2** | C4 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In EMIFA mode, this pin is Chip Select 2 output EM_CS2 (O/Z). This is the chip select used for EMIFA boot modes. Asynchronous memories (i.e., NOR Flash) or NAND flash. |
| PCI_CBE3/ HR/W **EM_CS3** | A5 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In EMIFA mode, this pin is Chip Select 3 output EM_CS3 (O/Z). Asynchronous memories (i.e., NOR Flash). |
| PCI_GNT/ DACK/ GP[12]/ **EM_CS4** | D10 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA.<br>In EMIFA mode, this pin is Chip Select 4 output EM_CS4 (O/Z). Asynchronous memories (i.e., NOR Flash).<br>This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_REQ/ DMARQ/ GP[11]/ **EM_CS5** | B9 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA.<br>In EMIFA mode, this pin is Chip Select 5 output EM_CS5 (O/Z).<br>This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_IDSEL/ HDDIR/ **EM_R/W** | E8 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, and EMIFA.<br>In EMIFA mode, this pin is the read/write output EM_R/W (O/Z). |
| PCI_SERR/ HDS1/ **EM_OE** | B2 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In EMIFA mode, this pin is the output enable output EM_OE (O/Z). |
| PCI_STOP/ HCNTL0/ **EM_WE** | D5 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In EMIFA mode, this pin is the write enable output EM_WE (O/Z). |
| PCI_PERR/ HCS/ **EM_DQM1** | C3 | I/O/Z | IPU $DV_{DD33}$ | These pins are multiplexed between PCI, HPI, and EMIFA.<br>In EMIFA mode, these pins are EM_DQM[1:0] and act as byte enables (O/Z). |
| PCI_PAR/ HAS/ **EM_DQM0** | D4 | I/O/Z | IPU $DV_{DD33}$ | |
| PCI_INTA/ **EM_WAIT2/** (RDY2/BSY2) | C11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI and EMIFA.<br>In EMIFA mode, this pin is wait state extension input 2 EM_WAIT2 (I).<br>When used for EMIFA (NAND), this pin is the ready/busy 2 input (RDY2/BSY2). |
| PCI_RSV5/IORDY/ GP[21]/**EM_WAIT3/** (RDY3/BSY3) | D11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA.<br>In EMIFA mode, this pin is wait state extension input 3 EM_WAIT3 (I).<br>When used for EMIFA (NAND), this pin is the ready/busy 3 input (RDY3/BSY3). |
| PCI_RSV4/DIOW/ GP[20]/**EM_WAIT4/** (RDY4/BSY4) | A11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA.<br>In EMIFA mode, this pin is wait state extension input 4 EM_WAIT4 (I).<br>When used for EMIFA (NAND), this pin is the ready/busy 4 input (RDY4/BSY4). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 3-9. Asynchronous External Memory Interface (EMIFA) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| PCI_RSV3/DIOR/ GP[19]/**EM_WAIT5**/ (RDY5/BSY5) | E10 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. For EMIFA, this pin is wait state extension input 5 EM_WAIT5 (I). When used for EMIFA (NAND), this pin is the ready/busy 5 input (RDY5/BSY5). |
| PCI_FRAME/ HINT/ **EM_BA[0]** | D6 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. For EMIFA, this is the Bank Address 0 output EM_BA[0] (O/Z). When connected to a 16-bit asynchronous memory, this pin has the same function as EMIF address pin 22 (EM_A[22]). When connected to an 8-bit asynchronous memory, this pin is the lowest order bit of the byte address. |
| PCI_DEVSEL/ HCNTL1/ **EM_BA[1]** | B3 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. For EMIFA, this is the Bank Address 1 output EM_BA[1] (O/Z). When connected to a 16 bit asynchronous memory this pin is the lowest order bit of the 16-bit word address. When connected to an 8-bit asynchronous memory, this pin is the second bit of the address. |
| PCI_RSV2/INTRQ/ GP[18]/**EM_RSV0** | B10 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. In EMIFA mode, this pin is reserved. This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_RST/ DA2/ GP[13]/**EM_A[22]** | C10 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. In EMIFA mode, this pin is address bit 22 output EM_A[22] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_RSV0/DA1/ GP[16]/**EM_A[21]** | A9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. In EMIFA mode, this pin is address bit 21 output EM_A[21] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_RSV1/DA0/ GP[17]/**EM_A[20]** | E9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI ATA, GPIO, and EMIFA. In EMIFA mode, this pin is address bit 20 output EM_A[20] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_CBE1/ ATA_CS1/ GP[32]/**EM_A[19]** | C2 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. In EMIFA mode, this pin is address bit 19 output EM_A[19] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_CBE0/ ATA_CS0/ GP[33]/**EM_A[18]** | F4 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. In EMIFA mode, this pin is address bit 18 output EM_A[18] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_IRDY/ HRDY/ **EM_A[17]**/(CLE) | A3 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In EMIFA mode, this pin is address bit 17 output EM_A[17] (O/Z). When used for EMIFA (NAND), this pin is Command Latch Enable output (CLE). |
| PCI_TRDY/ HHWIL/ **EM_A[16]**/(ALE) | E6 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. For EMIFA, this pin is address bit 16 output EM_A[16] (O/Z). When used for EMIFA (NAND), this pin is Address Latch Enable output (ALE). |
| PCI_AD31/ DD15/ HD31/**EM_A[15]** | A8 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 15 output EM_A[15] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD30/ DD14/ HD30/**EM_A[14]** | C9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 14 output EM_A[14] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD29/ DD13/ HD29/**EM_A[13]** | B8 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 13 output EM_A[13] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD28/ DD12/ HD28/**EM_A[12]** | D9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 12 output EM_A[12] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD27/ DD11/ HD27/**EM_A[11]** | A6 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 11 output EM_A[11] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD26/ DD10/ HD26/**EM_A[10]** | C8 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 10 output EM_A[10] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD25/ DD9/ HD25/**EM_A[9]** | B6 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 9 output EM_A[9] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |

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**Table 3-9. Asynchronous External Memory Interface (EMIFA) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| PCI_AD24/ DD8/ HD24/**EM_A[8]** | D8 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 8 output EM_A[8] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD23/ DD7/ HD23/**EM_A[7]** | B5 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 7 output EM_A[7] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD22/ DD6/ HD22/**EM_A[6]** | C7 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 6 output EM_A[6] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD21/ DD5/ HD21/**EM_A[5]** | C5 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 5 output EM_A[5] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD20/ DD4/ HD20/**EM_A[4]** | D7 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 4 output EM_A[4] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD19/ DD3/ HD19/**EM_A[3]** | A4 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 3 output EM_A[3] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD18/ DD2/ HD18/**EM_A[2]** | E7 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 2 output EM_A[2] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD17/ DD1/ HD17/**EM_A[1]** | B4 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 1 output EM_A[1] (O/Z). This signal is ***not*** available when ATA is enabled (i.e., EMIF NAND Flash mode). |
| PCI_AD16/ DD0/ HD16/**EM_A[0]** | C6 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, HPI, and EMIFA. For EMIFA, this pin is address bit 0 output EM_A[0] (O/Z), which is the least significant bit on a 32-bit word address. When connected to a 16-bit asynchronous memory, this pin is the second bit of the address. For an 8-bit asynchronous memory, this pin is the third bit of the address. |


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**Table 3-9. Asynchronous External Memory Interface (EMIFA) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| PCI_AD15/ HD15/**EM_D15** | E5 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between PCI, HPI, and EMIFA. For EMIFA mode, these pins are the 16-bit bidirectional data bus (EM_D[15:0]) [I/O/Z]. When EMIFA is configured for an 8-bit asynchronous memory, only EM_D[7:0] pins are used. |
| PCI_AD14/ HD14 /**EM_D14** | C1 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD13/ HD13/**EM_D13** | E4 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD12/ HD12/**EM_D12** | D3 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD11/ HD11/**EM_D11** | E3 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD10/ HD10/**EM_D10** | D2 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD9/ HD9/**EM_D9** | F5 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD8/ HD8/**EM_D8** | D1 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD7/ HD7/**EM_D7** | E2 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD6/ HD6/**EM_D6** | F3 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD5/ HD5/**EM_D5** | E1 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD4/ HD4/**EM_D4** | G5 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD3/ HD3/**EM_D3** | F2 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD2/ HD2/**EM_D2** | G4 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD1/ HD1/**EM_D1** | F1 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD0/ HD0/**EM_D0** | G3 | I/O/Z | IPD $DV_{DD33}$ | |
| **EMIFA FUNCTIONAL PINS: NAND** | | | | |
| $\overline{\text{PCI_IRDY}}$/ $\overline{\text{HRDY}}$/ **EM_A[17]**/(CLE) | A3 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In EMIFA mode, this pin is address bit 17 output EM_A[17] (O/Z). When used for EMIFA (NAND), this pin is Command Latch Enable output (CLE). |
| $\overline{\text{PCI_TRDY}}$/ HHWIL/ **EM_A[16]**/(ALE) | E6 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. For EMIFA, this pin is address bit 16 output EM_A[16] (O/Z). When used for EMIFA (NAND), this pin is Address Latch Enable output (ALE). |
| $\overline{\text{PCI_INTA}}$/ **EM_WAIT2**/ (RDY2/$\overline{\text{BSY2}}$) | C11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI and EMIFA. In EMIFA mode, this pin is wait state extension input 2 EM_WAIT2 (I). When used for EMIFA (NAND), this pin is the ready/busy 2 input (RDY2/$\overline{\text{BSY2}}$). |
| IORDY/ GP[21]/**EM_WAIT3**/ (RDY3/$\overline{\text{BSY3}}$) | D11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between ATA, GPIO, and EMIFA. In EMIFA mode, this pin is wait state extension input 3 EM_WAIT3 (I). When used for EMIFA (NAND), this pin is the ready/busy 3 input (RDY3/$\overline{\text{BSY3}}$). |
| $\overline{\text{DIOW}}$/ GP[20]/**EM_WAIT4**/ (RDY4/$\overline{\text{BSY4}}$) | A11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between ATA, GPIO, and EMIFA. In EMIFA mode, this pin is wait state extension input 4 EM_WAIT4 (I). When used for EMIFA (NAND), this pin is the ready/busy 4 input (RDY4/$\overline{\text{BSY4}}$). |
| $\overline{\text{DIOR}}$/ GP[19]/**EM_WAIT5**/ (RDY5/$\overline{\text{BSY5}}$) | E10 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between ATA, GPIO, and EMIFA. For EMIFA, this pin is wait state extension input 5 EM_WAIT5 (I). When used for EMIFA (NAND), this pin is the ready/busy 5 input (RDY5/$\overline{\text{BSY5}}$). |
| $\overline{\text{PCI_SERR}}$/ $\overline{\text{HDS1}}$/ **$\overline{\text{EM_OE}}$** | B2 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In EMIFA mode, this pin is the output enable output $\overline{\text{EM_OE}}$ (O/Z). |

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**Table 3-9. Asynchronous External Memory Interface (EMIFA) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| PCI_STOP/ HCNTL0/ **EM_WE** | D5 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In EMIFA mode, this pin is the write enable output EM_WE (O/Z). |
| PCI_CBE2/ HDS2/ **EM_CS2** | C4 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In EMIFA mode, this pin is Chip Select 2 output EM_CS2 (O/Z). This is the chip select used for EMIFA boot modes. Asynchronous memories (i.e., NOR Flash) or NAND flash. |
| PCI_CBE3/ HR/W **EM_CS3** | A5 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In EMIFA mode, this pin is Chip Select 3 output EM_CS3 (O/Z). Asynchronous memories (i.e., NOR Flash). |
| PCI_AD15/ HD15/**EM_D15** | E5 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between PCI, HPI, and EMIFA. For EMIFA mode, these pins are the 16-bit bidirectional data bus (EM_D[15:0]) [I/O/Z]. When EMIFA is configured for an 8-bit asynchronous memory, only EM_D[7:0] pins are used. |
| PCI_AD14/ HD14 /**EM_D14** | C1 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD13/ HD13/**EM_D13** | E4 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD12/ HD12/**EM_D12** | D3 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD11/ HD11/**EM_D11** | E3 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD10/ HD10/**EM_D10** | D2 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD9/ HD9/**EM_D9** | F5 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD8/ HD8/**EM_D8** | D1 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD7/ HD7/**EM_D7** | E2 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD6/ HD6/**EM_D6** | F3 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD5/ HD5/**EM_D5** | E1 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD4/ HD4/**EM_D4** | G5 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD3/ HD3/**EM_D3** | F2 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD2/ HD2/**EM_D2** | G4 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD1/ HD1/**EM_D1** | F1 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_AD0/ HD0/**EM_D0** | G3 | I/O/Z | IPD $DV_{DD33}$ | |


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**Table 3-10. DDR2 Memory Controller Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **DDR2 Memory Controller** | | | | |
| DDR_CLK | M23 | O/Z | $DV_{DDR2}$ | DDR2 Clock |
| $\overline{\text{DDR_CLK}}$ | L23 | O/Z | $DV_{DDR2}$ | DDR2 Differential clock |
| DDR_CKE | M20 | O/Z | $DV_{DDR2}$ | DDR2 Clock Enable |
| $\overline{\text{DDR_CS}}$ | J20 | O/Z | $DV_{DDR2}$ | DDR2 Active low chip select |
| $\overline{\text{DDR_WE}}$ | L20 | O/Z | $DV_{DDR2}$ | DDR2 Active low Write enable |
| $\overline{\text{DDR_RAS}}$ | K19 | O/Z | $DV_{DDR2}$ | DDR2 Row Access Signal output |
| $\overline{\text{DDR_CAS}}$ | L21 | O/Z | $DV_{DDR2}$ | DDR2 Column Access Signal output |
| DDR_DQM[3] | V20 | O/Z | $DV_{DDR2}$ | DDR2 Data mask outputs<br>DDR_DQM[3]: For upper byte data bus DDR_D[31:24]<br>DDR_DQM[2]: For DDR_D[23:16]<br>DDR_DQM[1]: For DDR_D[15:8]<br>DDR_DQM[0]: For lower byte DDR_D[7:0] |
| DDR_DQM[2] | Y23 | O/Z | $DV_{DDR2}$ | |
| DDR_DQM[1] | F22 | O/Z | $DV_{DDR2}$ | |
| DDR_DQM[0] | F20 | O/Z | $DV_{DDR2}$ | |
| DDR_DQS[3] | U20 | I/O/Z | $DV_{DDR2}$ | Data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR2 memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>DDR_DQS[3] : For upper byte DDR_D[31:24]<br>DDR_DQS[2]: For DDR_D[23:16]<br>DDR_DQS[1]: For DDR_D[15:8]<br>DDR_DQS[0]: For bottom byte DDR_D[7:0] |
| DDR_DQS[2] | V22 | I/O/Z | $DV_{DDR2}$ | |
| DDR_DQS[1] | D22 | I/O/Z | $DV_{DDR2}$ | |
| DDR_DQS[0] | D21 | I/O/Z | $DV_{DDR2}$ | |
| $\overline{\text{DDR_DQS[3]}}$ | V21 | I/O/Z | $DV_{DDR2}$ | Complimentary data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR2 memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>$\overline{\text{DDR_DQS[3]}}$ : For upper byte DDR_D[31:24]<br>$\overline{\text{DDR_DQS[2]}}$: For DDR_D[23:16]<br>$\overline{\text{DDR_DQS[1]}}$: For DDR_D[15:8]<br>DDR_DQS[0]: For bottom byte DDR_D[7:0] |
| $\overline{\text{DDR_DQS[2]}}$ | W23 | I/O/Z | $DV_{DDR2}$ | |
| $\overline{\text{DDR_DQS[1]}}$ | D23 | I/O/Z | $DV_{DDR2}$ | |
| $\overline{\text{DDR_DQS[0]}}$ | E20 | I/O/Z | $DV_{DDR2}$ | |
| DDR_ODT0 | K20 | O/Z | $DV_{DDR2}$ | DDR2 on-die termination control |
| DDR_BA[2] | P19 | O/Z | $DV_{DDR2}$ | Bank address outputs (BA[2:0]). |
| DDR_BA[1] | M21 | | | |
| DDR_BA[0] | N19 | | | |
| DDR_A[14] | N23 | O/Z | $DV_{DDR2}$ | DDR2 address bus |
| DDR_A[13] | H21 | | | |
| DDR_A[12] | P20 | | | |
| DDR_A[11] | K23 | | | |
| DDR_A[10] | T23 | | | |
| DDR_A[9] | N22 | | | |
| DDR_A[8] | J23 | | | |
| DDR_A[7] | N20 | | | |
| DDR_A[6] | M22 | | | |
| DDR_A[5] | N21 | | | |
| DDR_A[4] | J22 | | | |
| DDR_A[3] | R22 | | | |
| DDR_A[2] | L22 | | | |
| DDR_A[1] | R23 | | | |
| DDR_A[0] | H23 | | | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) Specifies the operating I/O supply voltage for each signal
(3) For more information, see the *Recommended Operating Conditions* table

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**Table 3-10. DDR2 Memory Controller Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| DDR_D[31] | Y20 | I/O/Z | $DV_{DDR2}$ | DDR2 data bus can be configured as 32 bits wide or 16 bits wide. |
| DDR_D[30] | W20 | | | |
| DDR_D[29] | Y21 | | | |
| DDR_D[28] | AA21 | | | |
| DDR_D[27] | U21 | | | |
| DDR_D[26] | T21 | | | |
| DDR_D[25] | R20 | | | |
| DDR_D[24] | T20 | | | |
| DDR_D[23] | AB22 | | | |
| DDR_D[22] | Y22 | | | |
| DDR_D[21] | AA22 | | | |
| DDR_D[20] | AA23 | | | |
| DDR_D[19] | V23 | | | |
| DDR_D[18] | U23 | | | |
| DDR_D[17] | T22 | | | |
| DDR_D[16] | U22 | | | |
| DDR_D[15] | H22 | | | |
| DDR_D[14] | G23 | | | |
| DDR_D[13] | G22 | | | |
| DDR_D[12] | F23 | | | |
| DDR_D[11] | E23 | | | |
| DDR_D[10] | C22 | | | |
| DDR_D[9] | B22 | | | |
| DDR_D[8] | C23 | | | |
| DDR_D[7] | H20 | | | |
| DDR_D[6] | G21 | | | |
| DDR_D[5] | F21 | | | |
| DDR_D[4] | G20 | | | |
| DDR_D[3] | B21 | | | |
| DDR_D[2] | C20 | | | |
| DDR_D[1] | D20 | | | |
| DDR_D[0] | C21 | | | |
| DDR_DQGATE0 | J19 | O/Z | $DV_{DDR2}$ | DDR2 strobe gate signal for lower-half data bus |
| DDR_DQGATE1 | J21 | I | $DV_{DDR2}$ | DDR2 strobe gate signal return for lower-half data bus |
| DDR_DQGATE2 | R19 | O/Z | $DV_{DDR2}$ | DDR2 strobe gate signal for upper-half data bus |
| DDR_DQGATE3 | R21 | I | $DV_{DDR2}$ | DDR2 strobe gate signal return for upper-half data bus |
| DDR_VREF | P23 | S | (4) | Reference voltage input for the SSTL_18 IO buffers. |
| DDR_ZP | L19 | O | (4) | Impedance control for DDR2 outputs. This must be connected via a 50-Ω (±5% tolerance) resistor to $V_{SS}$. |
| DDR_ZN | M19 | O | (4) | Impedance control for DDR2 outputs. This must be connected via a 50-Ω (±5% tolerance) resistor to $DV_{DDR2}$. |

(4) For more information, see the *Recommended Operating Conditions* table


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**Table 3-11. Peripheral Component Interconnect (PCI) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **PCI** | | | | |
| **Notes:** When PCI boot mode is ***not*** used, for proper device operation out of reset PCIEN ***must*** be "0".<br>The PCI pin functions are enabled when PCIEN = 1 (PCI mode). This can be done via an external PU on the PCIEN pin (AC6) or by setting the PCIEN bit (bit 2) in the PINMUX0 register to a "1" after device reset. For more details on the PCIEN pin, see Table 3-5, *Boot Terminal Functions*.<br><br>In PCI mode (PCIEN = 1), the internal pullups/pulldowns (IPUs/IPDs) are disabled on all PCI pins and it is recommended to have external pullup resistors on the PCI_RSV[5:0] pins. For more detailed information on external pullup/pulldown resistors, see Section 4.8.1, *Pullup/Pulldown Resistors*.<br><br>Also in PCI mode (PCIEN = 1), the internal pulldowns (IPDs) are disabled on the GP[5:7] pins. It is recommended to have external pullup resistors on the GP[5] pin when PCIEN = 1 and on GP[6:7] pins when PCIEN = 1 *and* VADJEN = 0. | | | | |
| **PCI_CLK**/GP[10] | A10 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI and GPIO.<br>In PCI mode, this pin is the PCI clock input PCI_CLK (I). |
| **PCI_RST** /DA2/ GP[13]/EM_A[22] | C10 | I/O/Z | [IPD] $DV_{DD33}$ | This pin is multiplexed between the PCI, ATA, GPIO, and EMIFA.<br>In PCI mode, this pin is PCI reset PCI_RST (I). |
| **PCI_IDSEL**/ HDDIR/EM_R/W | E8 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, and EMIFA.<br>In PCI mode, this pin is the PCI initialization device select, PCI_IDSEL (I). |
| **PCI_DEVSEL** / HCNTL1/EM_BA[1] | B3 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI device select, PCI_DEVSEL (I/O/Z). |
| **PCI_FRAME** / HINT/EM_BA[0] | D6 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI cycle frame, PCI_FRAME (I/O/Z). |
| **PCI_IRDY** /HRDY/ EM_A[17]/(CLE) | A3 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI initiator ready, PCI_IRDY (I/O/Z). |
| **PCI_ TRDY** /HHWIL/ EM_A[16]/(ALE) | E6 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI target ready, PCI_ TRDY (I/O/Z). |
| **PCI_STOP** / HCNTL0/EM_WE | D5 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI stop, PCI_STOP (I/O/Z). |
| **PCI_SERR** / HDS1/EM_OE | B2 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI system error, PCI_SERR (I/O/Z). |
| **PCI_PERR** / HCS/EM_DQM1 | C3 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI parity error, PCI_PERR (I/O/Z). |
| **PCI_PAR**/ HAS/EM_DQM0 | D4 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI parity, PCI_PAR (I/O/Z). |
| **PCI_INTA** / EM_WAIT2/ (RDY2/BSY2) | C11 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between the PCI and EMIFA.<br>In PCI mode, this pin is the PCI interrupt A, PCI_INTA (O/Z). |
| **PCI_REQ** / DMARQ/ GP[11]/EM_CS5 | B9 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between the PCI, ATA, GPIO, and EMIFA.<br>In PCI mode, this pin is the PCI bus request, PCI_REQ (O/Z). |
| **PCI_GNT** / DMACK/ GP[12]/EM_CS4 | D10 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between the PCI, ATA, GPIO, and EMIFA.<br>In PCI mode, this pin is PCI bus grant, PCI_GNT (I). |
| **PCI_CBE3** / HR/W/EM_CS3 | A5 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI command/byte enable 3, PCI_CBE3 (I/O/Z). |
| **PCI_CBE2** / HDS2/EM_CS2 | C4 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA.<br>In PCI mode, this pin is the PCI command/byte enable 2, PCI_CBE2 (I/O/Z). |
| **PCI_CBE1** / ATA_CS1/ GP[32]/EM_A[19] | C2 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA.<br>In PCI mode, this pin is the PCI command/byte enable 1 PCI_CBE1 (I/O/Z). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-11. Peripheral Component Interconnect (PCI) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **$\overline{\text{PCI_CBE0}}$** / $\overline{\text{ATA_CS0}}$/ GP[33]/$\overline{\text{EM_A}}$[18] | F4 | I/O/Z | [IPU] $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. In PCI mode, this pin is the PCI command/byte enable 0 $\overline{\text{PCI_CBE0}}$ (I/O/Z). |


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**Table 3-11. Peripheral Component Interconnect (PCI) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **PCI_AD31**/DD15/ HD31/EM_A[15] | A8 | I/O/Z | [IPD] $DV_{DD33}$ | These pins are multiplexed between PCI, ATA, HPI, and EMIFA. In PCI mode, these pins are the PCI address/data bus, PCI_AD[31:16] (I/O/Z). |
| **PCI_AD30**/DD14/ HD30/EM_A[14] | C9 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD29**/DD13/ HD29/EM_A[13] | B8 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD28**/DD12/ HD28/EM_A[12] | D9 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD27**/DD11/ HD27/EM_A[11] | A6 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD26**/DD10/ HD26/EM_A[10] | C8 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD25**/DD9/ HD25/EM_A[9] | B6 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD24**/DD8/ HD24/EM_A[8] | D8 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD23**/DD7/ HD23/EM_A[7] | B5 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD22**/DD6/ HD22/EM_A[6] | C7 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD21**/DD5/ HD21/EM_A[5] | C5 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD20**/DD4/ HD20/EM_A[4] | D7 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD19**/DD3/ HD19/EM_A[3] | A4 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD18**/DD2/ HD18/EM_A[2] | E7 | I/O/Z | [IPU] $DV_{DD33}$ | |
| **PCI_AD17**/DD1/ HD17/EM_A[1] | B4 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD16**/DD0/ HD16/EM_A[0] | C6 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD15**/ HD15/EM_D15 | E5 | I/O/Z | [IPD] $DV_{DD33}$ | These pins are multiplexed between PCI, HPI, and EMIFA. For PCI, these pins are PCI data/address bus, PCI_AD [15:0] (I/O/Z). |
| **PCI_AD14**/ HD14/EM_D14 | C1 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD13**/ HD13/EM_D13 | E4 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD12**/ HD12/EM_D12 | D3 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD11**/ HD11/EM_D11 | E3 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD10**/ HD10/EM_D10 | D2 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD9**/ HD9/EM_D9 | F5 | I/O/Z | [IPU] $DV_{DD33}$ | |
| **PCI_AD8**/ HD8/EM_D8 | D1 | I/O/Z | [IPD] $DV_{DD33}$ | |

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**Table 3-11. Peripheral Component Interconnect (PCI) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **PCI_AD7**/ HD7/EM_D7 | E2 | I/O/Z | [IPD] $DV_{DD33}$ | These pins are multiplexed between PCI, HPI, and EMIFA. For PCI, these pins are PCI data/address bus [15:0] (I/O/Z) |
| **PCI_AD6**/ HD6/EM_D6 | F3 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD5**/ HD5/EM_D5 | E1 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD4**/ HD4/EM_D4 | G5 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD3**/ HD3/EM_D3 | F2 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD2**/ HD2/EM_D2 | G4 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD1**/ HD1/EM_D1 | F1 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_AD0**/ HD0/EM_D0 | G3 | I/O/Z | [IPD] $DV_{DD33}$ | |
| **PCI_RSV0**/DA1/ GP[16]/EM_A[21] | A9 | I/O/Z | [IPD] $DV_{DD33}$ | PCI reserved (I)(1) |
| **PCI_RSV1**/DA0/ GP[17]/EM_A[20] | E9 | I/O/Z | [IPD] $DV_{DD33}$ | PCI reserved (O/Z)(1) |
| **PCI_RSV2**/INTRQ/ GP[18]/EM_RSV 0 | B10 | I/O/Z | [IPD] $DV_{DD33}$ | PCI reserved (I)(1) |
| **PCI_RSV3**/$\overline{\text{DIOR}}$/ GP[19]/ EM_WAIT5 | E10 | I/O/Z | [IPU] $DV_{DD33}$ | PCI reserved (O/Z)(1) |
| **PCI_RSV4**/$\overline{\text{DIOW}}$/ GP[20]/ EM_WAIT4 | A11 | I/O/Z | [IPU] $DV_{DD33}$ | PCI reserved (I/O/Z)(1) |
| **PCI_RSV5**/IORDY/ GP[21]/ EM_WAIT3 | D11 | I/O/Z | [IPU] $DV_{DD33}$ | PCI reserved (I/O/Z)(1) |

(1) In PCI mode (PCIEN = 1), it is recommended to have an external pullup resistor on this pin.


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**Table 3-12. EMAC [G]MII and MDIO Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **EMAC [G]MII** | | | | |
| RFTCLK | H1 | I | IPD $DV_{DD33}$ | Gigabit (GMII) reference transmit clock (125 MHz) |
| GMTCLK | P2 | O/Z | - $DV_{DD33}$ | GMII source asynchronous transmit clock |
| MTCLK | R1 | I | IPD $DV_{DD33}$ | [G]MII transmit clock input |
| MTXD7 | P1 | O/Z | - $DV_{DD33}$ | [G]MII transmit data [7:0]. For 1000 GMII operation, MTXD[7:0] are used. For 10/100 MII operation, *only* MTXD[3:0] are used. |
| MTXD6 | N4 | | | |
| MTXD5 | N3 | | | |
| MTXD4 | N2 | | | |
| MTXD3 | N1 | | | |
| MTXD2 | M4 | | | |
| MTXD1 | M1 | | | |
| MTXD0 | L1 | | | |
| MTXEN | L2 | O/Z | - $DV_{DD33}$ | [G]MII transmit data enable output |
| MCOL | L4 | I | IPD $DV_{DD33}$ | [G]MII collision detect (sense) input |
| MCRS | L3 | I | IPD $DV_{DD33}$ | [G]MII carrier sense input |
| MRCLK | K1 | I | IPU $DV_{DD33}$ | [G]MII receive clock |
| MRXD7 | K2 | I | IPU $DV_{DD33}$ | [G]MII receive data [7:0]. For 1000 GMII operation, MRXD[7:0] are used. For 10/100 MII operation, *only* MRXD[3:0] are used. |
| MRXD6 | K3 | | | |
| MRXD5 | K4 | | | |
| MRXD4 | J1 | | | |
| MRXD3 | J2 | | | |
| MRXD2 | J3 | | | |
| MRXD1 | H2 | | | |
| MRXD0 | G2 | | | |
| MRXDV | J4 | I | IPU $DV_{DD33}$ | [G]MII receive data valid input |
| MRXER | H3 | I | IPU $DV_{DD33}$ | [G]MII receive data error input |
| **MDIO** | | | | |
| MDCLK | G1 | O/Z | IPU $DV_{DD33}$ | Management data serial clock output |
| MDIO | H4 | I/O/Z | IPU $DV_{DD33}$ | Management Data IO |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-13. VLYNQ Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **VLYNQ** | | | | |
| VLYNQ_CLOCK | U1 | I/O/Z | IPU $DV_{DD33}$ | VLYNQ serial clock |
| $\overline{\text{VLYNQ_SCRUN}}$ | U2 | I/O/Z | IPU $DV_{DD33}$ | VLYNQ serial clock run request |
| VLYNQ_TXD3 | T3 | O/Z | – $DV_{DD33}$ | VLYNQ transmit bus [3:0] |
| VLYNQ_TXD2 | T2 | | | |
| VLYNQ_TXD1 | T1 | | | |
| VLYNQ_TXD0 | R4 | | | |
| VLYNQ_RXD3 | R3 | I | IPD $DV_{DD33}$ | VLYNQ receive bus [3:0] |
| VLYNQ_RXD2 | R2 | | | |
| VLYNQ_RXD1 | P3 | | | |
| VLYNQ_RXD0 | P4 | | | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 3-14. HPI Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **Host-Port Interface (HPI)** | | | | |
| HPI is enabled by the PINMUX0.HPIEN =1 (*and* PCIEN = 0 *and* ATAEN dependent for 16-/32-bit modes). For more detailed information on the HPI pin muxing, see Section 4.7.3.1, *PCI, HPI, EMIFA, and ATA Pin Muxing*. | | | | |
| PCI_PERR/ **HCS** / EM_DQM1 | C3 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI active-low chip select input, HCS (I). |
| PCI_STOP/ **HCNTL0**/ EM_WE | D5 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI control input 0, HCNTL0 (I) |
| PCI_DEVSEL/ **HCNTL1**/ EM_BA[1] | B3 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI control input 1, HCNTL1 (I). |
| PCI_PAR/ **HAS** / EM_DQM0 | D4 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI address strobe, HAS (I). **NOTE:** The DM6467T HPI ***does not*** support the HAS feature. For proper HPI operation if the pin is routed out, it ***must*** be pulled up via an external resistor. |
| PCI_SERR/ **HDS1** /EM_OE | B2 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI data strobe input 1, HDS1 (I). |
| PCI_CBE2/ **HDS2** /EM_CS2 | C4 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI data strobe input 2, HDS2 (I). |
| PCI_CBE3/ **HR/W** /EM_CS3 | A5 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI host read/write select input, HR/W (I). |
| PCI_TRDY/ **HHWIL**/ EM_A[16]/(ALE) | E6 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI half-word identification input control, HHWIL (I). |
| PCI_AD31/ DD15/ **HD31**/EM_A[15] | A8 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between PCI, ATA, HPI, and EMIFA. In HPI-32 mode, these pins are the HPI upper data bus, HD[31:16] (I/O/Z). In HPI-16 mode, the HD[31:16] pins are ***not*** used by the HPI . |
| PCI_AD30/ DD14/ **HD30**/EM_A[14] | C9 | | | |
| PCI_AD29/ DD13/ **HD29**/EM_A[13] | B8 | | | |
| PCI_AD28/ DD12/ **HD28**/EM_A[12] | D9 | | | |
| PCI_AD27/ DD11/ **HD27**/EM_A[11] | A6 | | | |
| PCI_AD26/ DD10/ **HD26**/ EM_A[10] | C8 | | | |
| PCI_AD25/ DD9/ **HD25**/EM_A[9] | B6 | | | |
| PCI_AD24/ DD8/ **HD24**/EM_A[8] | D8 | | | |

(1) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(2) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-14. HPI Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| PCI_AD23/ DD7/ **HD23**/EM_A[7] | B5 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between PCI, ATA, HPI, and EMIFA.<br>In HPI-32 mode, these pins are the HPI upper data bus, HD[31:16] (I/O/Z).<br>In HPI-16 mode, the HD[31:16] pins are ***not*** used by the HPI . |
| PCI_AD22/ DD6/ **HD22**/EM_A[6] | C7 | | | |
| PCI_AD21/ DD5/ **HD21**/EM_A[5] | C5 | | | |
| PCI_AD20/ DD4/ **HD20**/EM_A[4] | D7 | | | |
| PCI_AD19/ DD3/ **HD19**/EM_A[3] | A4 | | | |
| PCI_AD18/ DD2/ **HD18**/EM_A[2] | E7 | | | |
| PCI_AD17/ DD1/ **HD17**/EM_A[1] | B4 | | | |
| PCI_AD16/ DD0/ **HD16**/EM_A[0] | C6 | | | |
| PCI_AD15/ **HD15**/EM_D15 | E5 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between PCI, HPI, and EMIFA.<br>In HPI-16 mode, these pins are the HPI data bus, HD[15:0] (I/O/Z).<br>In HPI-32 mode, these pins are the HPI lower data bus, HD[15:0] (I/O/Z). |
| PCI_AD14/ **HD14**/EM_D14 | C1 | | | |
| PCI_AD13/ **HD13**/EM_D13 | E4 | | | |
| PCI_AD12/ **HD12**/EM_D12 | D3 | | | |
| PCI_AD11/ **HD11**/EM_D11 | E3 | | | |
| PCI_AD10/ **HD10**/EM_D10 | D2 | | | |
| PCI_AD9/ **HD9**/EM_D9 | F5 | | | |
| PCI_AD8/ **HD8**/EM_D8 | D1 | | | |
| PCI_AD7/ **HD7**/EM_D7 | E2 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between PCI, HPI, and EMIFA.<br>In HPI-16 mode, these pins are the HPI data bus, HD[15:0] (I/O/Z).<br>In HPI-32 mode, these pins are the HPI lower data bus, HD[15:0] (I/O/Z). |
| PCI_AD6/ **HD6**/EM_D6 | F3 | | | |
| PCI_AD5/ **HD5**/EM_D5 | E1 | | | |
| PCI_AD4/ **HD4**/EM_D4 | G5 | | | |
| PCI_AD3/ **HD3**/EM_D3 | F2 | | | |
| PCI_AD2/ **HD2**/EM_D2 | G4 | | | |
| PCI_AD1/ **HD1**/EM_D1 | F1 | | | |
| PCI_AD0/ **HD0**/EM_D0 | G3 | | | |


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**Table 3-14. HPI Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| PCI_IRDY/ **HRDY** / EM_A[17]/(CLE) | A3 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI host ready output from DSP to host, HRDY (O/Z). |
| PCI_FRAME/ **HINT** /EM_BA[0] | D6 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, HPI, and EMIFA. In HPI mode, this pin is the HPI host interrupt output, HINT (O/Z). |

**Table 3-15. USB Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) (4) | DESCRIPTION |
|---|---|---|---|---|
| **USB 2.0** | | | | |
| USB_DP | A19 | A I/O | | USB bidirectional Data Differential signal pair [positive/negative]. When the USB peripheral ***is not*** used, the USB_DP signal should be pulled up (high) and the USB_DN signal should be pulled down (low) via a 10-kΩ resistor. |
| USB_DN | A20 | A I/O | | |
| USB_R1 | D18 | A I/O | (4) | USB current reference output. When the USB peripheral is used, this pin must be connected via a 10-kΩ ±1% resistor to USB_$V_{SSREF}$. When the USB peripheral is ***not*** used, this pin must be connected via a 10-kΩ resistor to USB_$V_{SSREF}$. |
| **USB_DRVVBUS**/ GP[22] | B18 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between USB and GPIO. When this pin is used as USB_DRVVBUS (PINMUX0.VBUSDIS = 0), and the USB Controller is operating as a Host (USBCTL.USBID = 0 *and* Session is in progress), this signal is used by the USB Controler to enable the external VBUS charge pump. |
| USB_$V_{SSREF}$ | C18 | GND | (4) | Ground for reference current. This pin must be connected via a 10-kΩ ±1% resistor to USB_R1. When the USB peripheral ***is not*** used, the USB_$V_{SSREF}$ signal should be connected to $V_{SS}$. |
| USB_$V_{DDA3P3}$ | F18 | S | (4) | Analog 3.3 V power supply for USB PHY. When the USB peripheral ***is not*** used, the USB_$V_{DDA3P3}$ signal should be connected to $DV_{DD33}$. |
| USB_$V_{DD1P8}$ | E18 | S | (4) | 1.8-V I/O power supply for USB PHY. When the USB peripheral ***is not*** used, the USB_$V_{DD1P8}$ signal should be connected to 1.8-V power supply. |
| USB_$V_{DDA1P2LDO}$ | E17 | S | (4) | Core power supply LDO output for USB PHY. This pin must be connected via a 1-µF capacitor to $V_{SS}$. When the USB peripheral ***is not*** used, the USB_$V_{DDA1P2LDO}$ signal should still be connected via a 1-µF capacitor to $V_{SS}$. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal
(4) For more information, see the *Recommended Operating Conditions* table


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**Table 3-16. Video-Port Interface (VPIF) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **VIDEO-PORT INTERFACE (VPIF) – CAPTURE** | | | | |
| VP_CLKIN0 | AC13 | I | IPD $DV_{DD33}$ | VPIF capture channel 0 input clock (I). |
| VP_CLKIN1 | AB18 | I | IPD $DV_{DD33}$ | VPIF capture channel 1 input clock (I). |
| **VP_DIN15_VP_VSYNC/** TS0_DIN7 | AC18 | I | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF0. When used for the VPIF, this pin is capture data bit 15 *or* the vertical sync input, VP_DIN15_VSYNC (I). |
| **VP_DIN14_VP_HSYNC/** TS0_DIN6 | AA17 | I | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF0. When used for the VPIF, this pin is capture data bit 14 *or* the horizontal sync input, VP_DIN14_HSYNC (I). |
| **VP_DIN13_FIELD/** TS0_DIN5 | AB17 | I | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF0. When used for the VPIF, this pin is capture data bit 13 *or* the field indicator input, VP_DIN13_FIELD (I). |
| **VP_DIN12/** TS0_DIN4 | AC17 | I | IPD $DV_{DD33}$ | These pins are multiplexed between the VPIF and TSIF0. When used for the VPIF, these pins are capture data bits, VP_DIN[12:8] (I). |
| **VP_DIN11/** TS0_DIN3 | Y16 | | | |
| **VP_DIN10/** TS0_DIN2 | AA16 | | | |
| **VP_DIN9/** TS0_DIN1 | AB16 | | | |
| **VP_DIN8/** TS0_DIN0 | AC16 | | | |
| **VP_DIN7/** TS0_DOUT7/ TS1_DIN | Y14 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between the VPIF, TSIF0, and TSIF1. When used for the VPIF, these pins are capture data bits, VP_DIN[7:4] (I). |
| **VP_DIN6/** TS0_DOUT6/ TS1_PSTIN | AA14 | | | |
| **VP_DIN5/** TS0_DOUT5/ TS1_EN_WAITO | AB14 | | | |
| **VP_DIN4/** TS0_DOUT4/ TS1_WAITO | AC14 | | | |
| **VP_DIN3/** TS0_DOUT3 | Y15 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between the VPIF and TSIF0. When used for the VPIF, these pins are capture data bits, VP_DIN[3:0] (I). |
| **VP_DIN2/** TS0_DOUT2 | AA15 | | | |
| **VP_DIN1/** TS0_DOUT1 | AB15 | | | |
| **VP_DIN0/** TS0_DOUT0 | AC15 | | | |
| **VIDEO-PORT INTERFACE (VPIF) – DISPLAY** | | | | |
| VP_CLKIN2 | Y10 | I | IPD $DV_{DD33}$ | VPIF display channel 2 source input clock (I). |
| **VP_CLKIN3/** TS1_CLKO | AC9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF1. When used for VPIF, this pin is display channel 3 source clock, VP_CLKIN3 (I). |
| VP_CLKO2 | AA9 | O/Z | - $DV_{DD33}$ | VPIF display channel 2 output clock (O/Z). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-16. Video-Port Interface (VPIF) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **VP_CLKO3/** TS0_CLKO | AC10 | O/Z | - $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF0. When used for VPIF, this pin is the display channel 3 output clock, VP_CLKO3 (O/Z). |
| **VP_DOUT15/** TS1_DIN | AB8 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between the VPIF and TSIF1. When used for the VPIF, these pins are display data bits, VP_DOUT[15:8] (O/Z). |
| **VP_DOUT14/** TS1_PSTIN | AC7 | I/O/Z | | |
| **VP_DOUT13/** TS1_EN_WAITO | Y9 | I/O/Z | | |
| **VP_DOUT12/** TS1_WAITO | AA8 | I/O/Z | | |
| **VP_DOUT11/** TS1_DOUT | AB10 | O/Z | | |
| **VP_DOUT10/** TS1_PSTO | AA10 | O/Z | | |
| **VP_DOUT9/** TS1_ENAO | AC8 | O/Z | | |
| **VP_DOUT8/** TS1_WAITIN | AB9 | O/Z | | |
| **VP_DOUT7** | AB7 | O/Z | IPD $DV_{DD33}$ | This pin is video display data bit 7, VP_DOUT[7] (O/Z). **Note:** For proper device operation, ***do not*** oppose the IPD resistor on this pin at reset (i.e., this pin should be low at the rising edge of RESET or POR). |
| **VP_DOUT6/** DSPBOOT | AC5 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between the VPIF and boot configuration. After reset, these pins are used by the VPIF as display data bits, VP_DOUT[6:0] (O/Z). |
| **VP_DOUT5/** PCIEN | AC6 | | | |
| **VP_DOUT4/** CS2BW | AA7 | | | |
| **VP_DOUT3/** BTMODE3 | AB6 | | | |
| **VP_DOUT2/** BTMODE2 | Y8 | | | |
| **VP_DOUT1/** BTMODE1 | AC4 | | | |
| **VP_DOUT0/** BTMODE0 | AB5 | | | |


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**Table 3-17. Transport Stream Interface 0 (TSIF0) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **TSIF0 PARALLEL INPUT (PINMUX0.PTSIMUX = 10)** | | | | |
| TS0_CLKIN | AC19 | I | IPD $DV_{DD33}$ | TSIF0 receive clock input (I). |
| $\overline{\text{UCTS1}}$/USD1/ **TS0_EN_WAITO**/ GP[26] | Y17 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When TSIF0 input is enabled (PINMUX0.PTSIMUX = 1x), in synchronous mode, this pin is the data enable indicator (I) ***or*** in asynchronous mode, this pin is the wait output (O/Z), TS0_EN_WAITO. |
| $\overline{\text{URTS1}}$/UIRTX1/ **TS0_WAITO**/GP[25] | AA18 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When TSIF0 input is enabled (PINMUX0.PTSIMUX = 1x), in asynchronous mode, this pin is the wait output, TS0_WAITO (O/Z). This TSIF pin function is *not* used in synchronous mode. |
| $\overline{\text{URTS2}}$/UIRTX2/ **TS0_PSTIN**/GP[41] | AC20 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, TSIF0, and GPIO. When TSIF0 input is enabled (PINMUX0.PTSIMUX = 1x), this pin is the packet start input indicator, TS0_PSTIN (I). |
| VP_DIN15_VP_VSYNC/ **TS0_DIN7** | AC18 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between the VPIF and TSIF0. When TSIF0 parallel input mux mode is enabled (PINMUX0.PTSIMUX = 10), these pins are input data bits TS0_DIN[7:0] (I). |
| VP_DIN14_VP_HSYNC/ **TS0_DIN6** | AA17 | | | |
| VP_DIN13_FIELD/ **TS0_DIN5** | AB17 | | | |
| VP_DIN12/ **TS0_DIN4** | AC17 | | | |
| VP_DIN11/ **TS0_DIN3** | Y16 | | | |
| VP_DIN10/ **TS0_DIN2** | AA16 | | | |
| VP_DIN9/ **TS0_DIN1** | AB16 | | | |
| VP_DIN8/ **TS0_DIN0** | AC16 | | | |
| **TSIF0 SERIAL INPUT (PINMUX0.PTSIMUX = 11)** | | | | |
| TS0_CLKIN | AC19 | I | IPD $DV_{DD33}$ | TSIF0 receive clock input (I). |
| $\overline{\text{UCTS1}}$/USD1/ **TS0_EN_WAITO**/ GP[26] | Y17 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When TSIF0 input is enabled (PINMUX0.PTSIMUX = 1x), in synchronous mode, this pin is the data enable indicator (I) ***or*** in asynchronous mode, this pin is the wait output (O/Z), TS0_EN_WAITO. |
| $\overline{\text{URTS2}}$/UIRTX2/ **TS0_PSTIN**/GP[41] | AC20 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, TSIF0, and GPIO. When TSIF0 input is enabled (PINMUX0.PTSIMUX = 1x), in synchronous/asynchronous modes, this pin is the packet start input indicator, TS0_PSTIN (I). |
| URXD1/ **TS0_DIN7**/GP[23] | Y18 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When TSIF0 serial input mux mode is enabled (PINMUX0.PTSIMUX = 11), in synchronous/asynchronous modes, this pin is the serial input data bit (I), TS0_DIN7(I). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-17. Transport Stream Interface 0 (TSIF0) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **TSIF0 PARALLEL OUTPUT (PINMUX0.PTSIMUX = 10)** | | | | |
| VP_CLKO3/ **TS0_CLKO** | AC10 | O/Z | - $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF0. When TSIF0 output is enabled (PINMUX0.PTSOMUX = 1x), this pin is the transmit clock output, TS0_CLKO (O/Z). |
| $\overline{\text{UDTR0}}$/ **TS0_ENAO**/GP[36] | Y12 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When TSIF0 output is enabled (PINMUX0.PTSOMUX = 1x), this pin is the data enable indicator, TS0_ENAO (O/Z) in either synchronous/asynchronous modes. |
| $\overline{\text{UDSR0}}$/ **TS0_PSTO**/ GP[37] | AB11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When TSIF0 output is enabled (PINMUX0.PTSOMUX = 1x), this pin is the packet start output indicator, TS0_PSTO (O/Z) in either synchronous/asynchronous modes. |
| $\overline{\text{UDCD0}}$/ **TS0_WAITIN**/ GP[38] | AA11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When TSIF0 output is enabled (PINMUX0.PTSOMUX = 1x), in asynchronous mode, this pin is the wait input, TS0_WAITIN (I). This TSIF pin function is *not* used in synchronous mode. |
| VP_DIN7/ **TS0_DOUT7**/ TS1_DIN | Y14 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between the VPIF, TSIF0, and TSIF1. When parallel TSIF0 output is enabled (PINMUX0.PTSOMUX = 10), and TSIF1 VPIF_DIN muxing is ***not*** enabled (TSSI_MUX ≠ 11), these pins are the output data bits TS0_DOUT[7:4] (O/Z) in either synchronous/asynchronous modes. |
| VP_DIN6/ **TS0_DOUT6**/ TS1_PSTIN | AA14 | | | |
| VP_DIN5/ **TS0_DOUT5**/ TS1_EN_WAITO | AB14 | | | |
| VP_DIN4/ **TS0_DOUT4**/ TS1_WAITO | AC14 | | | |
| VP_DIN3/ **TS0_DOUT3** | Y15 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between the VPIF and TSIF0. When parallel TSIF0 output is enabled (PINMUX0.PTSOMUX = 10), these pins are the output data bits TS0_DOUT[3:0] (O/Z) in either synchronous/asynchronous modes. |
| VP_DIN2/ **TS0_DOUT2** | AA15 | | | |
| VP_DIN1/ **TS0_DOUT1** | AB15 | | | |
| VP_DIN0/ **TS0_DOUT0** | AC15 | | | |
| **TSIF0 SERIAL OUTPUT (PINMUX0.PTSIMUX = 11)** | | | | |
| VP_CLKO3/ **TS0_CLKO** | AC10 | O/Z | - $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF0. When TSIF0 output is enabled (PINMUX0.PTSOMUX = 1x), this pin is the transmit clock output, TS0_CLKO (O/Z). |
| $\overline{\text{UDTR0}}$/ **TS0_ENAO**/GP[36] | Y12 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When TSIF0 output is enabled (PINMUX0.PTSOMUX = 1x), this pin is the data enable indicator, TS0_ENAO (O/Z) in either synchronous/asynchronous modes. |
| $\overline{\text{UDSR0}}$/ **TS0_PSTO**/GP[37] | AB11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When TSIF0 output is enabled (PINMUX0.PTSOMUX = 1x), this pin is the packet start output indicator, TS0_PSTO (O/Z) in either synchronous/asynchronous modes. |
| $\overline{\text{UDCD0}}$/ **TS0_WAITIN**/GP[38] | AA11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When TSIF0 output is enabled (PINMUX0.PTSOMUX = 1x), in asynchronous mode, this pin is the wait input, TS0_WAITIN (I). This TSIF pin function is *not* used in synchronous mode. |
| UTXD1/URCTX1/ **TS0_DOUT7**/GP[24] | AB19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When serial TSIF0 output is enabled (PINMUX0.PTSOMUX = 11), in synchronous/asynchronous modes, this pin is the serial output data bit, TS0_DOUT[7] (O/Z). |


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**Table 3-18. Transport Stream Interface 1 (TSIF1) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **TSIF1 INPUT – UART0 MUXING (PINMUX0.TSSIMUX = 01)** | | | | |
| TS1_CLKIN | AC11 | I | IPD $DV_{DD33}$ | TSIF1 receive clock input (I). |
| URXD0/ **TS1_DIN** | AB13 | I | IPD $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When TSIF1 input on UART0 muxing is enabled (PINMUX0.TSSIMUX = 01), this pin is the serial data input, TS1_DIN (I). |
| $\overline{\text{URTS0}}$/UIRTX0/ **TS1_EN_WAITO** | AA13 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When TSIF1 input on UART0 muxing is enabled (PINMUX0.TSSIMUX = 01), in synchronous mode, this pin is the data enable indicator (I) ***or*** in asynchronous mode, this pin is the wait output, TS1_EN_WAITO (O/Z). |
| UTXD0/URCTX0/ **TS1_PSTIN** | Y13 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When TSIF1 input on UART0 muxing is enabled (PINUMX0.TSSIMUX = 01), this pin is the packet start indicator, TS1_PSTIN (I). |
| **TSIF1 INPUT – VPIF DOUT MUXING (PINMUX0.TSSIMUX = 10)** | | | | |
| TS1_CLKIN | AC11 | I | IPD $DV_{DD33}$ | TSIF1 receive clock input (I). |
| VP_DOUT15/ **TS1_DIN** | AB8 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between VPIF and TSIF1. When TSIF1 input on VPIF DOUT muxing is enabled (PINMUX0.TSSIMUX = 10), this pin is the serial data input, TS1_DIN (I). |
| VP_DOUT13/ **TS1_EN_WAITO** | Y9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between VPIF and TSIF1. When TSIF1 input on VPIF DOUT muxing is enabled (PINMUX0.TSSIMUX = 10), in synchronous mode, this pin is the data enable indicator (I) ***or*** in asynchronous mode, this pin is the wait output, TS1_EN_WAITO (O/Z). |
| VP_DOUT14/ **TS1_PSTIN** | AC7 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between VPIF and TSIF1. When TSIF1 input on VPIF DOUT muxing is enabled (PINMUX0.TSSIMUX = 10), in synchronous/asynchronous modes, this pin is the packet start indicator, TS1_PSTIN (I). |
| **TSIF1 INPUT – VPIF DIN MUXING (PINMUX0.TSSIMUX = 11)** | | | | |
| TS1_CLKIN | AC11 | I | IPD $DV_{DD33}$ | TSIF1 receive clock input (I). |
| VP_DIN7/ TS0_DOUT7/ **TS1_DIN** | Y14 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between VPIF, TSIF0, and TSIF1. When TSIF1 input on VPIF DIN muxing is enabled (PINMUX0.TSSIMUX = 11), in synchronous/asynchronous modes, this pin is the serial data input, TS1_DIN (I). |
| VP_DIN5/ TS0_DOUT5/ **TS1_EN_WAITO** | AB14 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between VPIF, TSIF0, and TSIF1. When TSIF1 input on VPIF DIN muxing is enabled (PINMUX0.TSSIMUX = 11), in synchronous mode, this pin is the data enable indicator (I) ***or*** in asynchronous mode, this pin is the wait output, TS1_EN_WAITO (O/Z). |
| VP_DIN6/ TS0_DOUT6/ **TS1_PSTIN** | AA14 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between VPIF, TSIF0, and TSIF1. When TSIF1 input on VPIF DIN muxing is enabled (PINMUX0.TSSIMUX = 11), in synchronous/asynchronous modes, this pin is the packet start indicator, TS1_PSTIN (I). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-18. Transport Stream Interface 1 (TSIF1) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **TSIF1 OUTPUT – VPIF DOUT MUXING (PINMUX0.TSSOMUX = 10)** | | | | |
| VP_CLKIN3/ **TS1_CLKO** | AC9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF1. When TSIF1 output is enabled (PINMUX0.TSSOMUX = 1x), in synchronous/asynchronous modes, this pin is the transmit clock output, TS1_CLKO (O/Z). |
| VP_DOUT11/ **TS1_DOUT** | AB10 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF1. When TSIF1 output on VPIF DOUT muxing is enabled (PINMUX0.TSSOMUX = 10), in synchronous/asynchronous modes, this pin is the serial data output, TS1_DOUT (O/Z). |
| VP_DOUT9/ **TS1_ENAO** | AC8 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF1. When TSIF1 output on VPIF DOUT muxing is enabled (PINMUX0.TSSOMUX = 10), in synchronous/asynchronous modes, this pin is the data enable indicator, TS1_ENAO (O/Z). |
| VP_DOUT10/ **TS1_PSTO** | AA10 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF1. When TSIF1 output on VPIF DOUT muxing is enabled (PINMUX0.TSSOMUX = 10), in synchronous/asynchronous modes, this pin is the packet start indicator output, TS1_PSTO (O/Z). |
| VP_DOUT8/ **TS1_WAITIN** | AB9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF1. When TSIF1 output on VPIF DOUT muxing is enabled (PINMUX0.TSSOMUX = 10), in asynchronous mode, this pin is the wait indicator input, TS1_WAITIN (I). This TSIF pin function is *not* used in synchronous mode. |
| **TSIF1 OUTPUT – UART/PWM MUXING (PINMUX0.TSSOMUX = 11)** | | | | |
| VP_CLKIN3/ **TS1_CLKO** | AC9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between the VPIF and TSIF1. When TSIF1 output is enabled (PINMUX0.TSSOMUX = 1x), in synchronous/asynchronous modes, this pin is the transmit clock output, TS1_CLKO (O/Z). |
| PWM1/ **TS1_DOUT** | W18 | I/O/Z | - $DV_{DD33}$ | This pin is multiplexed between PWM1 and TSIF1. When TSIF1 output on UART/PWM is enabled (PINMUX0.TSSOMUX = 11), in synchronous/asynchronous modes, this pin is the serial data output, TS1_DOUT (O/Z). |
| PWM0/ CRG0_PO/ **TS1_ENAO** | W17 | O/Z | - $DV_{DD33}$ | This pin is multiplexed between PWM0, CRGEN0, and TSIF1. When TSIF1 output on UART/PWM is enabled (PINMUX0.TSSOMUX = 11), in synchronous/asynchronous modes, this pin is the data enable indicator output, TS1_ENAO (O/Z) |
| $\overline{\text{UCTS2}}$/USD2/ CRG0_VCX1/ GP[42]/ **TS1_PSTO** | AC21 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN0, GPIO, and TSIF1. When TSIF1 output on UART/PWM is enabled (PINMUX0.TSSOMUX = 11), in synchronous/asynchronous modes, this pin is the packet start indicator output, TS1_PSTO (O/Z). |
| $\overline{\text{URIN0}}$/GP[8]/ **TS1_WAITIN** | Y11 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART0, GPIO, and TSIF1. When TSIF1 output on UART/PWM is enabled (PINMUX0.TSSOMUX = 11), in asynchronous mode, this pin is the wait indicator input, TS1_WAITIN (I). This TSIF pin function is *not* used in synchronous mode. |


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### Table 3-19. I2C Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) | DESCRIPTION |
|---|---|---|---|---|
| I2C | | | | |
| SCL | U5 | I/O/Z | - $DV_{DD33}$ | I2C clock output SCL. For proper device operation, this pin ***must*** be pulled up via external resistor. |
| SDA | U4 | I/O/Z | - $DV_{DD33}$ | I2C bidirectional data signal SDA. For proper device operation, this pin ***must*** be pulled up via external resistor. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) Specifies the operating I/O supply voltage for each signal

### Table 3-20. SPI Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| SPI | | | | |
| SPI_CLK | V1 | I/O/Z | IPD $DV_{DD33}$ | SPI clock |
| $\overline{\text{SPI_EN}}$ | T5 | I/O/Z | IPD $DV_{DD33}$ | SPI device enable |
| $\overline{\text{SPI_CS0}}$ | T4 | I/O/Z | IPD $DV_{DD33}$ | SPI chip select 0 |
| $\overline{\text{SPI_CS1}}$ | U3 | I/O/Z | IPD $DV_{DD33}$ | SPI chip select 1 |
| SPI_SOMI | R5 | I/O/Z | IPD $DV_{DD33}$ | SPI slave out, master in data pin |
| SPI_SIMO | P5 | I/O/Z | IPD $DV_{DD33}$ | SPI slave in, master out data pin |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-21. Multichannel Audio Serial Port (McASP) Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **McASP0** | | | | |
| ACLKR0 | AA2 | I/O/Z | IPD $DV_{DD33}$ | McASP0 receive bit clock |
| AHCLKR0 | AB2 | I/O/Z | IPD $DV_{DD33}$ | McASP0 receive high-frequency master clock |
| AFSR0 | Y3 | I/O/Z | IPD $DV_{DD33}$ | McASP0 receive frame sync |
| ACLKX0 | AA1 | I/O/Z | IPD $DV_{DD33}$ | McASP0 transmit bit clock |
| AHCLKX0 | Y1 | I/O/Z | IPD $DV_{DD33}$ | McASP0 transmit high-frequency master clock |
| AFSX0 | Y4 | I/O/Z | IPD $DV_{DD33}$ | McASP0 transmit frame sync |
| AXR0[3] | W3 | I/O/Z | IPD $DV_{DD33}$ | McASP0 transmit/receive data pins [3:0] |
| AXR0[2] | W4 | | | |
| AXR0[1] | V4 | | | |
| AXR0[0] | V3 | | | |
| AMUTE0 | Y2 | I/O/Z | IPD $DV_{DD33}$ | McASP0 mute output |
| AMUTEIN0 | AA3 | I | IPD $DV_{DD33}$ | McASP0 mute input |
| **McASP1** | | | | |
| ACLKX1 | W1 | I/O/Z | IPD $DV_{DD33}$ | McASP1 transmit bit clock |
| AHCLKX1 | W2 | I/O/Z | IPD $DV_{DD33}$ | McASP1 transmit high-frequency master clock |
| AXR1[0] | V2 | I/O/Z | IPD $DV_{DD33}$ | McASP1 transmit data pin [0] |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 3-22. Clock Recovery Generator (CRGEN) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **CRGEN1 ONLY MODE (PINMUX0.CRGMUX = 001)** | | | | |
| URXD2/ **CRG1_VCXI**/ GP[39]/ CRG0_VCXI | AB20 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When CRGEN1 is enabled (PINMUX0.CRGMUX = 001), this pin is CRGEN1 input clock from external VCXO, CRG1_VCXI (I). |
| UTXD2/ URCTX2/ **CRG1_PO**/ GP[40]/ CRG0_PO | AA19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When CRGEN1 is enabled (PINMUX0.CRGMUX = 001), this pin is CRGEN1 pulse width modulation output, CRG1_PO (O/Z). |
| **CRGEN0 ONLY (UART2/PWM0 MUX) MODE (PINMUX0.CRGMUX = 100)** | | | | |
| $\overline{\text{UCTS2}}$/ USD2/ **CRG0_VCXI**/ GP[42]/ TS1_PSTO | AC21 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN0, GPIO, and TSIF1. When CRGEN0 on UART2/PWM muxing is enabled (PINMUX0.CRGMUX = 10x), this pin is CRGEN0 input clock from external VCXO, CRG0_VCXI (I). |
| PWM0/ **CRG0_PO**/ TS1_ENAO | W17 | O/Z | – $DV_{DD33}$ | This pin is multiplexed between PWM0, CRGEN0, and TSIF1. When CRGEN0 on UART2/PWM muxing is enabled (PINMUX0.CRGMUX = 10x), this pin is CRGEN0 pulse width modulation output, CRG0_PO (O/Z). |
| **CRGEN0 AND CRGEN1 MODE (PINMUX0.CRGMUX = 101)** | | | | |
| URXD2/ **CRG1_VCXI**/ GP[39]/ CRG0_VCXI | AB20 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When CRGEN1 is enabled (PINMUX0.CRGMUX = x01), this pin is CRGEN1 input clock from external VCXO, CRG1_VCXI (I). |
| UTXD2/ URCTX2/ **CRG1_PO**/ GP[40]/ CRG0_PO | AA19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When CRGEN1 is enabled (PINMUX0.CRGMUX = x01), this pin is CRGEN1 pulse width modulation output, CRG1_PO (O/Z). |
| $\overline{\text{UCTS2}}$/ USD2/ **CRG0_VCXI**/ GP[42]/ TS1_PSTO | AC21 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN0, GPIO, and TSIF1. When CRGEN0 on UART2/PWM muxing is enabled (PINMUX0.CRGMUX = 10x), this pin is CRGEN0 input clock from external VCXO, CRG0_VCXI (I). |
| PWM0/ **CRG0_PO**/ TS1_ENAO | W17 | O/Z | – $DV_{DD33}$ | This pin is multiplexed between PWM0, CRGEN0, and TSIF1. When CRGEN0 on UART2/PWM muxing is enabled (PINMUX0.CRGMUX = 10x), this pin is CRGEN0 pulse width modulation output, CRG0_PO (O/Z). |
| **CRGEN0 ONLY (UART2 MUX) MODE (PINMUX0.CRGMUX = 110)** | | | | |
| URXD2/ CRG1_VCXI/ GP[39]/ **CRG0_VCXI** | AB20 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When CRGEN0 on UART2 muxing is enabled (PINMUX0.CRGMUX = 110), this pin is CRGEN0 input clock from external VCXO, CRG0_VCXI (I). |
| UTXD2/ URCTX2/ CRG1_PO/ GP[40]/ **CRG0_PO** | AA19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When CRGEN0 on UART2 muxing is enabled (PINMUX0.CRGMUX = 110), this pin is CRGEN0 pulse width modulation output, CRG0_PO (O/Z). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-23. UART0 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **Actual UART0 pin functions are determined by the PINMUX0 and PINMUX1 register bit settings. For more details, see Section 4.7.3, *Pin Multiplexing*.** | | | | |
| **UART0 WITH MODEM CONTROL (PINMUX1.UART0CTL = 00)** | | | | |
| **URXD0**/ TS1_DIN | AB13 | I | IPD $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 UART functional muxing is selected (PINMUX1.UART0CTL = 0x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 receive data, URXD0 (I). |
| **UTXD0**/ URCTX0/ TS1_PSTIN | Y13 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 UART functional muxing is selected (PINMUX1.UART0CTL = 0x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 transmit data, UTXD0 (O/Z). |
| **$\overline{\text{URTS0}}$** / UIRTX0/ TS1_EN_WAITO | AA13 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 UART functional muxing is selected (PINMUX1.UART0CTL = 0x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is the UART0 request-to-send signal, $\overline{\text{URTS0}}$ (O/Z). |
| **$\overline{\text{UCTS0}}$** / USD0 | AC12 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 UART functional muxing is selected (PINMUX1.UART0CTL = 0x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is the UART0 clear-to-send signal, $\overline{\text{UCTS0}}$ (I). |
| **$\overline{\text{UDTR0}}$** / TS0_ENAO/ GP[36] | Y12 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When UART0 UART with modem functional muxing is selected (PINMUX1.UART0CTL = 00) ***and*** TSIF0 output muxing is ***not*** enabled (PINMUX0.PTSOMUX ≠ 1x), this pin is UART0 data-terminal-ready, $\overline{\text{UDTR0}}$ (O/Z). |
| **$\overline{\text{UDSR0}}$** / TS0_PSTO/ GP[37] | AB11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When UART0 UART with modem functional muxing is selected (PINMUX1.UART0CTL = 00) ***and*** TSIF0 output muxing is ***not*** enabled (PINMUX0.PTSOMUX ≠ 1x), this pin is UART0 data-set-ready, $\overline{\text{UDSR0}}$ (I). |
| **$\overline{\text{UDCD0}}$** / TS0_WAITIN/ GP[38] | AA11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0, TSIF0, and GPIO. When UART0 UART with modem functional muxing is selected (PINMUX1.UART0CTL = 00) ***and*** TSIF0 output muxing is ***not*** enabled (PINMUX0.PTSOMUX ≠ 1x), this pin is UART0 data-carrier-detect, $\overline{\text{UDCD0}}$ (I). |
| **$\overline{\text{URIN0}}$** /GP[8]/ TS1_WAITIN | Y11 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART0, GPIO, and TSIF1. When UART0 UART with modem functional muxing is selected (PINMUX1.UART0CTL = 00) ***and*** TSIF1 output on UART/PWM muxing is ***not*** enabled (PINMUX0.TSSOMUX ≠ 11), this pin is the UART0 ring indicator, $\overline{\text{URIN0}}$ (I). |
| **UART0 WITHOUT MODEM CONTROL (PINMUX1.UART0CTL = 01)** | | | | |
| **URXD0**/ TS1_DIN | AB13 | I | IPD $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 UART functional muxing is selected (PINMUX1.UART0CTL = 0x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 receive data, URXD0 (I). |
| **UTXD0**/ URCTX0/ TS1_PSTIN | Y13 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 UART functional muxing is selected (PINMUX1.UART0CTL = 0x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 transmit data, UTXD0 (O/Z). |
| **$\overline{\text{URTS0}}$** / UIRTX0/ TS1_EN_WAITO | AA13 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 UART functional muxing is selected (PINMUX1.UART0CTL = 0x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 request-to-send signal, $\overline{\text{URTS0}}$ (O/Z). |
| **$\overline{\text{UCTS0}}$** / USD0 | AC12 | I/O/Z | IPU $DV_{DD33}$ | When UART0 UART functional muxing is selected (PINMUX1.UART0CTL = 0x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 clear-to-send signal, $\overline{\text{UCTS0}}$ (I). |

(1) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(2) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(3) Specifies the operating I/O supply voltage for each signal


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**Table 3-23. UART0 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| **UART0 IrDA/CIR FUNCTION (PINMUX1.UART0CTL = 1x)** | | | | |
| **URXD0**/ TS1_DIN | AB13 | I | IPD $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 IrDA/CIR receive data, URXD0 (I). |
| UTXD0/ **URCTX0**/ TS1_PSTIN | Y13 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 IrDA/CIR functional muxing is selected (PINMUX1.UART0CTL = 1x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 CIR transmit data, URCTX0 (O/Z). |
| $\overline{\text{URTS0}}$/ **UIRTX0**/ TS1_EN_WAITO | AA13 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART0 and TSIF1. When UART0 IrDA/CIR functional muxing is selected (PINMUX1.UART0CTL = 1x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 IrDA transmit data, UIRTX0 (O/Z). |
| $\overline{\text{UCTS0}}$/ **USD0** | AC12 | I/O/Z | IPU $DV_{DD33}$ | When UART0 IrDA/CIR functional muxing is selected (PINMUX1.UART0CTL = 1x) ***and*** TSIF1 input on UART0 muxing is ***not*** enabled (PINMUX0.TSSIMUX ≠ 01), this pin is UART0 IrDA transceiver control, USD0 (O/Z). |

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**Table 3-24. UART1 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **UART1 WITH FLOW CONTROL (PINMUX1.UART1CTL = 00)** | | | | |
| **Actual UART1 pin functions are determined by the PINMUX0 and PINMUX1 register bit settings. For more details, see Section 4.7.3, *Pin Multiplexing*.** | | | | |
| **URXD1**/ TS0_DIN7/ GP[23] | Y18 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 UART functional muxing is selected (PINMUX1.UART1CTL = 0x) ***and*** TSIF0 serial input is ***not*** enabled (PINMUX0.PTSIMUX ≠ 11), this pin is UART1 receive data, URXD1 (I). |
| **UTXD1**/ URCTX1/ TS0_DOUT7/ GP[24] | AB19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 UART functional muxing is selected (PINMUX1.UART1CTL = 0x) ***and*** TSIF0 serial output is ***not*** enabled (PINMUX0.PTSIMUX ≠ 11), this pin is UART1 transmit data, UTXD1 (O/Z). |
| **$\overline{\text{URTS1}}$** /UIRTX1/ TS0_WAITO/ GP[25] | AA18 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 UART with flow control muxing is selected (PINMUX1.UART1CTL = 00) ***and*** TSIF0 input is ***not*** enabled (PINMUX0.PTSIMUX ≠ 0x), this pin is UART1 request-to-send, $\overline{\text{URTS1}}$ (O/Z). |
| **$\overline{\text{UCTS1}}$** /USD1 TS0_EN_WAITO/ GP[26] | Y17 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 UART with flow control muxing is selected (PINMUX1.UART1CTL = 00) ***and*** TSIF0 input is ***not*** enabled (PINMUX0.PTSIMUX ≠ 0x), this pin is UART1 clear-to-send, $\overline{\text{UCTS1}}$ (I). |
| **UART1 WITHOUT FLOW CONTROL (PINMUX1.UART1CTL = 01)** | | | | |
| **URXD1**/ TS0_DIN7/ GP[23] | Y18 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 UART functional muxing is selected (PINMUX1.UART1CTL = 0x) ***and*** TSIF0 serial input is ***not*** enabled (PINMUX0.PTSIMUX ≠ 11), this pin is UART1 receive data, URXD1 (I). |
| **UTXD1**/ URCTX1/ TS0_DOUT7/ GP[24] | AB19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 UART functional muxing is selected (PINMUX1.UART1CTL = 0x) ***and*** TSIF0 serial output is ***not*** enabled (PINMUX0.PTSIMUX ≠ 11), this pin is UART1 transmit data, UTXD1 (O/Z). |
| **UART1 IrDA/CIR FUNCTION (PINMUX1.UART1CTL = 10)** | | | | |
| **URXD1**/ TS0_DIN7/ GP[23] | Y18 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 IrDA/CIR functional muxing is selected (PINMUX1.UART1CTL = 10) ***and*** TSIF0 serial input is ***not*** enabled (PINMUX0.PTSIMUX ≠ 11), this pin is UART1 receive data, URXD1 (I). |
| UTXD1/**URCTX1**/ TS0_DOUT7/ GP[24] | AB19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 IrDA/CIR functional muxing is selected (PINMUX1.UART1CTL = 10) ***and*** TSIF0 serial output is ***not*** enabled (PINMUX0.PTSOMUX ≠ 11), this pin is UART1 CIR transmit data, URCTX1 (O/Z). |
| $\overline{\text{URTS1}}$/**UIRTX1**/ TS0_WAITO/ GP[25] | AA18 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 IrDA/CIR functional muxing is selected (PINMUX1.UART1CTL = 10) ***and*** TSIF0 input is ***not*** enabled (PINMUX0.PTSIMUX = 0x), this pin is UART1 IrDA transmit data, UIRTX1 (O/Z). |
| $\overline{\text{UCTS1}}$/**USD1**/ TS0_EN_WAITO/ GP[26] | Y17 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 IrDA/CIR functional muxing is selected (PINMUX1.UART1CTL = 10) ***and*** TSIF0 input is ***not*** enabled (PINMUX0.PTSIMUX = 0x), this pin is UART1 IrDA tranceiver control, USD1 (O/Z). |

(1) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(2) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(3) Specifies the operating I/O supply voltage for each signal


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**Table 3-25. UART2 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **UART2 WITH FLOW CONTROL (PINMUX1.UART2CTL = 00)** | | | | |
| **Actual UART2 pin functions are determined by the PINMUX0 and PINMUX1 register bit settings. For more details, see Section 4.7.3, *Pin Multiplexing*.** | | | | |
| **URXD2**/ CRG1_VCXI/ GP[39]/ CRG0_VCXI | AB20 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When UART2 UART functional muxing is selected (PINMUX1.UART2CTL = 0x) ***and*** CRGEN0/1 are ***not*** enabled (PINMUX0.CRGMUX ≠ x01, 110), this pin is UART2 receive data, URXD2 (I). |
| **UTXD2**/ URCTX2/ CRG1_PO/ GP[40]/ CRG0_PO | AA19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When UART2 UART functional muxing is selected (PINMUX1.UART2CTL = 0x) ***and*** CRGEN0/1 are ***not*** enabled (PINMUX0.CRGMUX ≠ x01, 110), this pin is UART2 transmit data, UTXD2 (O/Z). |
| **$\overline{\text{URTS2}}$** /UIRTX2/ TS0_PSTIN/ GP[41] | AC20 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, TSIF0, and GPIO. When UART2 UART with flow control muxing is selected (PINMUX1.UART2CTL = 00) ***and*** TSIF0 input is ***not*** enabled (PINMUX0.PTSIMUX = 0x), this pin is UART2 request-to-send, $\overline{\text{URTS2}}$ (O/Z). |
| **$\overline{\text{UCTS2}}$** /USD2/ CRG0_VCXI/ GP[42]/ TS1_PSTO | AC21 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN0, GPIO, and TSIF1. When UART2 UART with flow control muxing is selected (PINMUX1.UART2CTL = 00) ***and*** TSIF1 output is ***not*** enabled (PINMUX0.PTSOMUX = 0x), this pin is UART2 clear-to-send, $\overline{\text{UCTS2}}$ (I). |
| **UART2 WITHOUT FLOW CONTROL (PINMUX1.UART2CTL = 01)** | | | | |
| **URXD2**/ CRG1_VCXI/ GP[39]/ CRG0_VCXI | AB20 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When UART2 UART functional muxing is selected (PINMUX1.UART2CTL = 0x) ***and*** CRGEN0/1 are ***not*** enabled (PINMUX0.CRGMUX ≠ x01, 110), this pin is UART2 receive data, URXD2 (I). |
| **UTXD2**/ URCTX2/ CRG1_PO/ GP[40]/ CRG0_PO | AA19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When UART2 UART functional muxing is selected (PINMUX1.UART2CTL = 0x) ***and*** CRGEN0/1 are ***not*** enabled (PINMUX0.CRGMUX ≠ x01, 110), this pin is UART2 transmit data, UTXD2 (O/Z). |
| **UART2 IrDA/CIR FUNCTION (PINMUX1.UART2CTL = 10)** | | | | |
| **URXD2**/ CRG1_VCXI/ GP[39]/ CRG0_VCXI | AB20 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When UART2 IrDA/CIR functional muxing is selected (PINMUX1.UART2CTL = 10) ***and*** CRGEN0/1 are ***not*** enabled (PINMUX0.CRGMUX ≠ x01, 110), this pin is UART2 receive data, URXD2 (I). |
| UTXD2/**URCTX2**/ CRG1_PO/ GP[40]/ CRG0_PO | AA19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When UART2 IrDA/CIR functional muxing is selected (PINMUX1.UART2CTL = 10) ***and*** CRGEN0/1 are ***not*** enabled (PINMUX0.CRGMUX ≠ x01, 110), this pin is the UART2 CIR transmit data, URCTX2 (O/Z). |
| $\overline{\text{URTS2}}$/**UIRTX2**/ TS0_PSTIN/ GP[41] | AC20 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, TSIF0, and GPIO. When UART2 IrDA/CIR functional muxing is selected (PINMUX1.UART2CTL = 10) ***and*** TSIF0 input is ***not*** enabled (PINMUX0.PTSIMUX = 0x), this pin is UART2 IrDA transmit data, UIRTX2 (O/Z). |
| $\overline{\text{UCTS2}}$/**USD2**/ CRG0_VCXI/ GP[42]/ TS1_PSTO | AC21 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN0, GPIO, and TSIF1. When UART2 IrDA/CIR functional muxing is selected (PINMUX1.UART2CTL = 10) ***and*** CRGEN0 on TSIF0 output is ***not*** enabled (PINMUX0.TSSOMUX = 0x), this pin is UART2 IrDA tranceiver control, USD2 (O/Z). |

(1) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(2) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-26. PWM Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) | DESCRIPTION |
|---|---|---|---|---|
| **PWM0** | | | | |
| **PWM0**/ CRG0_PO/ TS1_ENAO | W17 | O/Z | – $DV_{DD33}$ | This pin is multiplexed between PWM0, CRGEN0, and TSIF1. When ***not*** overridden by CRGEN or TSIF1 output muxing (PINMUX0.CRGMUX ≠ 10x ***and*** PINMUX0.TSSOMUX ≠ 11), this pin is the pulse width modulation 0 output, PWM0 (O/Z). |
| **PWM1** | | | | |
| **PWM1**/ TS1_DOUT | W18 | O/Z | – $DV_{DD33}$ | This pin is multiplexed between PWM1 and TSIF1. When ***not*** overridden by TSIF1 output muxing (PINMUX0.TSSOMUX ≠ 11), this pin is the pulse width modulation 1 output, PWM1 (O/Z). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) Specifies the operating I/O supply voltage for each signal


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**Table 3-27. Timer 0, Timer 1, and Timer 2 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **Timer 0** | | | | |
| TINP0L | Y7 | I/O/Z | IPD $DV_{DD33}$ | Timer0 lower input. This pin is the Timer0 input for 64-mode operation. For 32-bit timer operation, this pin is the input for the Timer0 lower 32-bit counter. |
| TINP0U | AA6 | I/O/Z | IPD $DV_{DD33}$ | Timer0 upper input. For 32-bit timer operation, this pin is the input for the Timer0 upper 32-bit counter. Not used for Timer0 64-mode operation. |
| TOUT0L | W8 | I/O/Z | IPD $DV_{DD33}$ | Timer0 lower output. This pin is the Timer0 output for 64-mode operation. For 32-bit timer operation, this pin is the output for the Timer0 lower 32-bit counter. |
| TOUT0U | W7 | I/O/Z | IPD $DV_{DD33}$ | Timer0 upper output. For 32-bit timer operation, this pin is the output for the Timer0 upper 32-bit counter. Not used for Timer0 64-mode operation. |
| **Timer 1** | | | | |
| TINP1L | Y6 | I/O/Z | IPD $DV_{DD33}$ | Timer1 lower input. This pin is the Timer1 input for 64-mode operation. For 32-bit timer operation, this pin is the input for the Timer1 lower 32-bit counter. |
| TOUT1L | AA5 | I/O/Z | IPD $DV_{DD33}$ | Timer1 lower output. This pin is the Timer1 output for 64-mode operation. For 32-bit timer operation, this pin is the output for the Timer1 lower 32-bit counter. |
| TOUT1U | AB4 | I/O/Z | IPD $DV_{DD33}$ | Timer1 upper output. For 32-bit timer operation, this pin is the output for the Timer1 upper 32-bit counter. Not used for Timer1 64-mode operation. |
| **WATCHDOG TIMER (Timer 2)** | | | | |
| TOUT2 | Y5 | I/O/Z | IPD $DV_{DD33}$ | Watchdog timer output. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 3-28. ATA Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **ATA** | | | | |
| ATA is enabled by the PINMUX0.ATAEN =1 (*and* PCIEN = 0). For more detailed information on the ATA pin muxing, see Section 4.7.3.1, *PCI, HPI, EMIFA, and ATA Pin Muxing*. | | | | |
| PCI_CBE0/ **ATA_CS0** / GP[33]/EM_A[18] | F4 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is ATA chip select 0 output, ATA_CS0 (O/Z). |
| PCI_CBE1/ **ATA_CS1** / GP[32]/EM_A[19] | C2 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is ATA chip select 1 output, ATA_CS1 (O/Z). |
| PCI_RSV4/ **DIOW** / GP[20]/EM_WAIT4 | A11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is the ATA write strobe output, DIOW (O/Z). |
| PCI_RSV3/ **DIOR** / GP[19]/EM_WAIT5 | E10 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is the ATA read strobe output, DIOR (O/Z). |
| PCI_RSV5/**IORDY**/ GP[21]/EM_WAIT3 | D11 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is ATA I/O ready, IORDY (I). |
| PCI_RST/ **DA2**/ GP[13]/EM_A[22] | C10 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is ATA address bit 2, DA2 (O/Z). |
| PCI_RSV0/**DA1**/ GP[16]/EM_A[21] | A9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is ATA address bit 1, DA1 (O/Z). |
| PCI_RSV1/**DA0**/ GP[17]/EM_A[20] | E9 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is ATA address bit 0, DA0 (O/Z). |
| PCI_RSV2/**INTRQ**/ GP[18]/EM_RSV0 | B10 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is the ATA interrupt request input, INTRQ (I). |
| PCI_REQ/ **DMARQ**/ GP[11]/EM_CS5 | B9 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is the ATA DMA request input, DMARQ (I). |
| PCI_GNT/ **DMACK** / GP[12]/EM_CS4 | D10 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When ATA is enabled, this pin is the ATA DMA acknowledge output, DMACK (O/Z). |
| PCI_IDSEL/ **HDDIR**/ EM_R/W | E8 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, and EMIFA. When ATA is enabled, this pin is the data direction indicator for external buffer control, HDDIR (O/Z). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 3-28. ATA Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| PCI_AD31/ **DD15**/ HD31/ EM_A[15] | A8 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between PCI, ATA, HPI, and EMIFA. When ATA is enabled, these pins are the ATA 16-bit bidirectional data bus, DD[15:0] (I/O/Z). |
| PCI_AD30/ **DD14**/ HD30/EM_A[14] | C9 | | | |
| PCI_AD29/ **DD13**/ HD29/EM_A[13] | B8 | | | |
| PCI_AD28/ **DD12**/ HD28/EM_A[12] | D9 | | | |
| PCI_AD27/ **DD11**/ HD27/EM_A[11] | A6 | | | |
| PCI_AD26/ **DD10**/ HD26/EM_A[10] | C8 | | | |
| PCI_AD25/ **DD9**/ HD25/EM_A[9] | B6 | | | |
| PCI_AD24/ **DD8**/ HD24/EM_A[8] | D8 | | | |
| PCI_AD23/ **DD7**/ HD23/EM_A[7] | B5 | | | |
| PCI_AD22/ **DD6**/ HD22/EM_A[6] | C7 | | | |
| PCI_AD21/ **DD5**/ HD21/EM_A[5] | C5 | | | |
| PCI_AD20/ **DD4**/ HD20/EM_A[4] | D7 | | | |
| PCI_AD19/ **DD3**/ HD19/EM_A[3] | A4 | | | |
| PCI_AD18/ **DD2**/ HD18/EM_A[2] | E7 | | | |
| PCI_AD17/ **DD1**/ HD17/EM_A[1] | B4 | | | |
| PCI_AD16/ **DD0**/ HD16/EM_A[0] | C6 | | | |

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**Table 3-29. General Purpose Input/Output (GPIO) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **GPIO** | | | | |
| **The DM6467T device does not support GP[47:43], GP[35:34], GP[31:27], GP[15:14], and GP[9] signals (not pinned out). GP[7:0] pins have dedicated ARM926 and DSP interrupts. When PCI is used, GP[19:16] pins are reserved.** | | | | |
| GP[0] | W5 | I/O/Z | IPD $DV_{DD33}$ | GP[0] (I/O/Z). This pin is general-purpose input/output 0. |
| GP[1] | V5 | I/O/Z | IPD $DV_{DD33}$ | GP[1] (I/O/Z). This pin is general-purpose input/output 1. |
| **GP[2]**/ AUDIO_CLK1 | AA4 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between GPIO and the audio clock selector. When audio clock 1 is disabled (PINMUX0.AUDCK1 = 0), this pin is GP[2] (I/O/Z). |
| **GP[3]**/ AUDIO_CLK0 | AB3 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between GPIO and the audio clock selector. When audio clock 0 is disabled (PINMUX0.AUDCK0 = 0), this pin is GP[3] (I/O/Z). |
| **GP[4]**/ STC_CLKIN | AC3 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between GPIO and the TSIF clock selector. When the STC source clock input is disabled (PINMUX0.STCCK = 0), this pin is GP[4] (I/O/Z). |
| **GP[5]** | B11 | I/O/Z | IPD $DV_{DD33}$ | This pin is GP[5] (I/O/Z). |
| **GP[6]** | E11 | I/O/Z | IPD $DV_{DD33}$ | This pin is GP[6] (I/O/Z). |
| **GP[7]** | A12 | I/O/Z | IPD $DV_{DD33}$ | This pin is GP[7] (I/O/Z). |
| $\overline{\text{URIN0}}$/**GP[8]**/ TS1_WAITIN | Y11 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART0, GPIO, and TSIF1. When UART0 UART with modem functional muxing is ***not*** selected (PINMUX1.UART0CTL = 00) ***and*** TSIF1 output on UART/PWM muxing is ***not*** enabled (PINMUX0.TSSOMUX ≠ 11), this pin is GP[8] (I/O/Z). |
| GP[9] | n/a | – | – | GP[9] is ***not*** pinned out on this device. |
| PCI_CLK/**GP[10]** | A10 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI and GPIO. When PCI is disabled (PINMUX0.PCIEN = 0), this pin is GP[10] (I/O/Z). |
| $\overline{\text{PCI_REQ}}$/ DMARQ/ **GP[11]**/$\overline{\text{EM_CS5}}$ | B9 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When 32-bit HPI mode is enabled (PINMUX0.PCIEN = 0, PINMUX0.HPIEN = 1, PINMUX0.ATAEN = 0), this pin is GP[11] (I/O/Z). |
| $\overline{\text{PCI_GNT}}$/ $\overline{\text{DMACK}}$/ **GP[12]**/$\overline{\text{EM_CS4}}$ | D10 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When 32-bit HPI mode is enabled (PINMUX0.PCIEN = 0, PINMUX0.HPIEN = 1, PINMUX0.ATAEN = 0), this pin is GP[12] (I/O/Z). |
| $\overline{\text{PCI_RST}}$/ DA2/ **GP[13]**/EM_A[22] | C10 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between PCI, ATA, GPIO, and EMIFA. When 32-bit HPI mode is enabled (PINMUX0.PCIEN = 0, PINMUX0.HPIEN = 1, PINMUX0.ATAEN = 0), this pin is GP[13] (I/O/Z). |
| GP[14:15] | n/a | – | – | GP[14:15] are ***not*** pinned out on this device. |
| PCI_RSV0/DA1/ **GP[16]**/ EM_A[21] | A9 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between PCI, ATA, GPIO, and EMIFA. When 32-bit HPI mode is enabled (PINMUX0.PCIEN = 0, PINMUX0.HPIEN = 1, PINMUX0.ATAEN = 0), these pins are GP[16:19] (I/0/Z). When PCI mode is enabled (PINMUX0.PCIEN = 1), these pins are reserved. |
| PCI_RSV1/DA0/ **GP[17]**/EM_A[20] | E9 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_RSV2/ $\overline{\text{INTRQ}}$/ **GP[18]**/ EM_RSV0 | B10 | I/O/Z | IPD $DV_{DD33}$ | |
| PCI_RSV3/$\overline{\text{DIOR}}$/ **GP[19]**/ EM_WAIT5 | E10 | I/O/Z | IPU $DV_{DD33}$ | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 3-29. General Purpose Input/Output (GPIO) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| PCI_RSV4/ $\overline{\text{DIOW}}$/ **GP[20]**/ EM_WAIT4 | A11 | I/O/Z | IPU $DV_{DD33}$ | These pins are multiplexed between PCI, ATA, GPIO, and EMIFA. When 32-bit HPI mode is enabled (PINMUX0.PCIEN = 0, PINMUX0.HPIEN = 1, PINMUX0.ATAEN = 0), these pins are GP[20:21] (I/0/Z). |
| PCI_RSV5/ IORDY/ **GP[21]**/ EM_WAIT3 | D11 | I/O/Z | IPU $DV_{DD33}$ | |
| USB_DRVVBUS/ **GP[22]** | B18 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between USB and GPIO. When ***not*** used for USB (PINMUX0.VBUSDIS = 1), this pin is GP[22] (I/O/Z). |
| URXD1/ TS0_DIN7/ **GP[23]** | Y18 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 GPIO muxing ***is*** selected (PINMUX1.UART1CTL = 11) ***and*** TSIF0 serial input is ***not*** enabled (PINMUX0.PTSIMUX ≠ 11), this pin is GP[23] (I/O/Z). |
| UTXD1/ URCTX1/ TS0_DOUT7/ **GP[24]** | AB19 | I/O/Z | IPD $DV_{DD33}$ | This pin is multiplexed between UART1, TSIF0, and GPIO. When UART1 GPIO muxing ***is*** selected (PINMUX1. UART1CTL = 11) ***and*** TSIF0 serial input is ***not*** enabled (PINMUX0.PTSIMUX ≠ 11), this pin is GP[24] (I/O/Z). |
| $\overline{\text{URTS1}}$/ UIRTX1/ TS0_WAITO/ **GP[25]** | AA18 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between UART1, TSIF0, and GPIO. When UART1 GPIO muxing ***is*** selected (PINMUX1.UART1CTL = 11) ***and*** TSIF0 input is ***not*** enabled (PINMUX0.PTSIMUX = 0x), these pins are GP[25:26] (I/O/Z). |
| $\overline{\text{UCTS1}}$/USD1/ TS0_EN_WAITO/ **GP[26]** | Y17 | I/O/Z | IPU $DV_{DD33}$ | |
| GP[27:31] | n/a | – | – | GP[27:31] are ***not*** pinned out on this device. |
| $\overline{\text{PCI_CBE1}}$/ $\overline{\text{ATA_CS1}}$/ **GP[32]**/ EM_A[19] | C2 | I/O/Z | IPU $DV_{DD33}$ | These pins are multiplexed between PCI, ATA, GPIO, and EMIFA. When 32-bit HPI mode is enabled (PINMUX0.PCIEN = 0, PINMUX0.HPIEN = 1, PINMUX0.ATAEN = 0), these pins are GP[32:33] (I/O/Z). |
| $\overline{\text{PCI_CBE0}}$/ $\overline{\text{ATA_CS0}}$/ **GP[33]**/ EM_A[18] | F4 | I/O/Z | IPU $DV_{DD33}$ | |
| GP[34:35] | n/a | – | – | GP[34:35] are ***not*** pinned out on this device. |
| $\overline{\text{UDTR0}}$/ TS0_ENAO/ **GP[36]** | Y12 | I/O/Z | IPU $DV_{DD33}$ | These pins are multiplexed between UART0, TSIF0, and GPIO. When UART0 UART with modem functional muxing is ***not*** selected (PINMUX1.UART0CTL ≠ 00) ***and*** TSIF0 output muxing is ***not*** enabled (PINMUX0.PTSOMUX ≠ 1x), these pins are GP[36:38] (I/O/Z). |
| $\overline{\text{UDSR0}}$/ TS0_PSTO/ **GP[37]** | AB11 | I/O/Z | IPU $DV_{DD33}$ | |
| $\overline{\text{UDCD0}}$/ TS0_WAITIN/ **GP[38]** | AA11 | I/O/Z | IPU $DV_{DD33}$ | |
| URXD2/ CRG1_VCXI/ **GP[39]**/ CRG0_VCXI | AB20 | I/O/Z | IPD $DV_{DD33}$ | These pins are multiplexed between UART2, CRGEN1, GPIO, and CRGEN0. When UART2 UART GPIO muxing ***is*** selected (PINMUX1.UART2CTL = 11) ***and*** CRGEN0/1 are ***not*** enabled (PINMUX0.CRGMUX ≠ x01, 110), these pins are GP[39:40] (I/O/Z). |
| UTXD2/URCTX2/ CRG1_PO/ **GP[40]**/ CRG0_PO | AA19 | I/O/Z | IPD $DV_{DD33}$ | |
| $\overline{\text{URTS2}}$/UIRTX2/ TS0_PSTIN/ **GP[41]** | AC20 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, TSIF0, and GPIO. When UART2 UART without flow control or GPIO muxing ***is*** selected (PINMUX1.UART2CTL = x1) ***and*** TSIF0 input is ***not*** enabled (PINMUX0.PTSIMUX = 0x), this pin is GP[41] (I/O/Z). |
| $\overline{\text{UCTS2}}$/USD2/ CRG0_VCXI/ **GP[42]**/ TS1_PSTO | AC21 | I/O/Z | IPU $DV_{DD33}$ | This pin is multiplexed between UART2, CRGEN0, GPIO, and TSIF1. When UART2 UART without flow control or GPIO muxing ***is*** selected (PINMUX1.UART2CTL = x1) ***and*** CRGEN0 on UART2/PWM muxing is ***not*** enabled (PINMUX0.CRGMUX ≠ 10x) ***and*** TSIF1 output is ***not*** enabled (PINMUX0.TSSOMUX = 0x), this pin is GP[42] (I/O/Z). |

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**Table 3-29. General Purpose Input/Output (GPIO) Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| GP[43:47] | n/a | – | – | GP[43:47] are ***not*** pinned out on this device. |


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**Table 3-30. Reserved Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| **RESERVED** | | | | |
| RSV1 | A1 | | | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |
| RSV2 | A2 | | | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |
| RSV3 | A22 | | | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |
| RSV4 | A23 | | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV5 | D14 | | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV6 | F17 | | | Reserved. For proper device operation, this pin **must** be tied directly to $CV_{DD}$. |
| RSV7 | G16 | | | Reserved. For proper device operation, this pin **must** be tied directly to $CV_{DD}$. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal

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**Table 3-31. Supply Terminal Functions**

| SIGNAL NAME | NO. | TYPE[1] | OTHER | DESCRIPTION |
|---|---|---|---|---|
| **SUPPLY VOLTAGE PINS** | | | | |
| $DV_{DD33}$ | B7 | S | | 3.3-V I/O supply voltage<br>(see the Power-Supply Decoupling section of this data manual) |
| | F8 | | | |
| | F9 | | | |
| | F10 | | | |
| | F11 | | | |
| | F12 | | | |
| | F13 | | | |
| | F14 | | | |
| | F15 | | | |
| | F16 | | | |
| | G7 | | | |
| | H6 | | | |
| | J6 | | | |
| | K6 | | | |
| | K7 | | | |
| | M3 | | | |
| | R7 | | | |
| | T7 | | | |
| | U7 | | | |
| | V7 | | | |
| | V8 | | | |
| | V17 | | | |
| | W9 | | | |
| | W10 | | | |
| | W11 | | | |
| | W12 | | | |
| | W13 | | | |
| | W14 | | | |
| | W15 | | | |
| | W16 | | | |
| | AA12 | | | |
| $DV_{DDR2}$ | B20 | S | | 1.8-V DDR2 I/O supply voltage<br>(see the Power-Supply Decoupling section of this data manual) |
| | E21 | | | |
| | G17 | | | |
| | G19 | | | |
| | H17 | | | |
| | J17 | | | |
| | K17 | | | |
| | K21 | | | |
| | P21 | | | |
| | R17 | | | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal


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**Table 3-31. Supply Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | OTHER | DESCRIPTION |
|---|---|---|---|---|
| $DV_{DDR2}$ | R18 | S | | 1.8-V DDR2 I/O supply voltage (see the Power-Supply Decoupling section of this data manual) |
| | T18 | | | |
| | T19 | | | |
| | U19 | | | |
| | W21 | | | |
| | AA20 | | | |
| $CV_{DD}$ | G8 | S | | 1.3-V core supply voltage (-1G devices) (see the Power-Supply Decoupling section of this data manual) |
| | G9 | | | |
| | G10 | | | |
| | G11 | | | |
| | G12 | | | |
| | G13 | | | |
| | G14 | | | |
| | G15 | | | |
| | H7 | | | |
| | H8 | | | |
| | H9 | | | |
| | H14 | | | |
| | H15 | | | |
| | H16 | | | |
| | J7 | | | |
| | J8 | | | |
| | J9 | | | |
| | J10 | | | |
| | J11 | | | |
| | J13 | | | |
| | J14 | | | |
| | J15 | | | |
| | J16 | | | |
| | K8 | | | |
| | K9 | | | |
| | K10 | | | |
| | K11 | | | |
| | K13 | | | |
| | K14 | | | |
| | K15 | | | |
| | K16 | | | |
| | P7 | | | |
| | P8 | | | |
| | P9 | | | |
| | P10 | | | |
| | P11 | | | |
| | P13 | | | |
| | P14 | | | |
| | P15 | | | |

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**Table 3-31. Supply Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | OTHER | DESCRIPTION |
|---|---|---|---|---|
| $CV_{DD}$ | R8 | S | | 1.3-V core supply voltage (-1G devices)<br>(see the Power-Supply Decoupling section of this data manual) |
| | R9 | | | |
| | R10 | | | |
| | R11 | | | |
| | R13 | | | |
| | R14 | | | |
| | R15 | | | |
| | T8 | | | |
| | T9 | | | |
| | T10 | | | |
| | T11 | | | |
| | T13 | | | |
| | T14 | | | |
| | T15 | | | |
| | U8 | | | |
| | U9 | | | |
| | U10 | | | |
| | U14 | | | |
| | U15 | | | |
| | U16 | | | |
| | V9 | | | |
| | V10 | | | |
| | V11 | | | |
| | V12 | | | |
| | V13 | | | |
| | V14 | | | |
| | V15 | | | |
| | V16 | | | |


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**Table 3-32. Ground Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| GROUND PINS | | | | |
| $V_{SS}$ | A7 | GND | | Ground pins |
| | A14 | | | |
| | A18 | | | |
| | A21 | | | |
| | B1 | | | |
| | B19 | | | |
| | B23 | | | |
| | C19 | | | |
| | D19 | | | |
| | E19 | | | |
| | E22 | | | |
| | F6 | | | |
| | F7 | | | |
| | F19 | | | |
| | G6 | | | |
| | G18 | | | |
| | H5 | | | |
| | H10 | | | |
| | H11 | | | |
| | H12 | | | |
| | H13 | | | |
| | H18 | | | |
| | H19 | | | |
| | J5 | | | |
| | J12 | | | |
| | J18 | | | |
| | K5 | | | |
| | K12 | | | |
| | K18 | | | |
| | K22 | | | |
| | L5 | | | |
| | L6 | | | |
| | L7 | | | |
| | L8 | | | |
| | L9 | | | |
| | L10 | | | |
| | L11 | | | |
| | L12 | | | |
| | L13 | | | |
| | L14 | | | |
| | L15 | | | |
| | L16 | | | |
| | L17 | | | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal

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**Table 3-32. Ground Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | OTHER | DESCRIPTION |
|---|---|---|---|---|
| $V_{SS}$ | L18 | GND | | Ground pins |
| | M2 | | | |
| | M5 | | | |
| | M6 | | | |
| | M7 | | | |
| | M8 | | | |
| | M9 | | | |
| | M10 | | | |
| | M11 | | | |
| | M12 | | | |
| | M13 | | | |
| | M14 | | | |
| | M15 | | | |
| | M16 | | | |
| | M17 | | | |
| | M18 | | | |
| | N5 | | | |
| | N6 | | | |
| | N7 | | | |
| | N8 | | | |
| | N9 | | | |
| | N10 | | | |
| | N11 | | | |
| | N12 | | | |
| | N13 | | | |
| | N14 | | | |
| | N15 | | | |
| | N16 | | | |
| | N17 | | | |
| | N18 | | | |
| | P6 | | | |
| | P12 | | | |
| | P16 | | | |
| | P17 | | | |
| | P18 | | | |
| | P22 | | | |
| | R6 | | | |
| | R12 | | | |
| | R16 | | | |
| | T6 | | | |
| | T12 | | | |
| | T16 | | | |
| | T17 | | | |
| | U6 | | | |
| | U11 | | | |
| | U12 | | | |


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**Table 3-32. Ground Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | OTHER | DESCRIPTION |
|---|---|---|---|---|
| $V_{SS}$ | U13 | GND | | Ground Pins |
| | U17 | | | |
| | U18 | | | |
| | V6 | | | |
| | V18 | | | |
| | V19 | | | |
| | W19 | | | |
| | W22 | | | |
| | Y19 | | | |
| | AB1 | | | |
| | AB12 | | | |
| | AB21 | | | |
| | AB23 | | | |
| | AC1 | | | |
| | AC2 | | | |
| | AC22 | | | |
| | AC23 | | | |

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## 3.8 Device Support

### 3.8.1 Development Support

TI offers an extensive line of development tools for the TMS320DM646x DMSoC platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of TMS320DM646x SoC-based applications:

**Software Development Tools:**

Code Composer Studio™ Integrated Development Environment (IDE): including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any SoC application.

**Hardware Development Tools:**

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the TMS320DM646x DMSoC platform, visit the Texas Instruments web site on the Worldwide Web at www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

### 3.8.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g.,TMS320DM6467TCUT1). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications.

**TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

**TMS** Fully-qualified production device.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.


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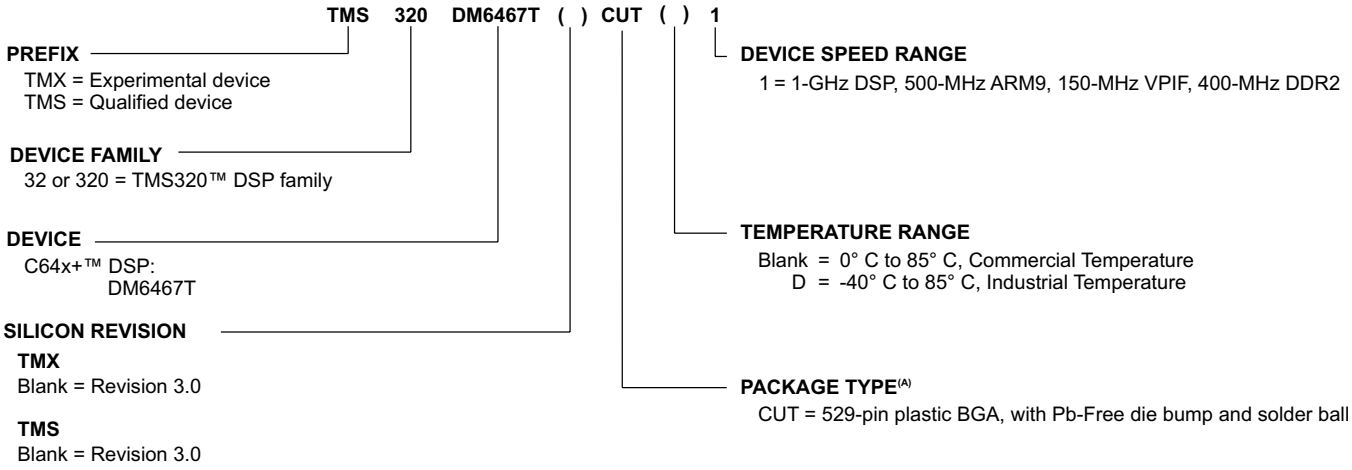
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, CUT), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz or gigahertz (for example, "1" is the default [1-GHz DSP, 500-MHz ARM9, 150-MHz VPIF, 400-MHz DDR2]).

Figure 3-8 provides a legend for reading the complete device name for any TMS320DM6467T DMSoC platform member.




A. BGA = Ball Grid Array

B. For actual device part number (P/Ns) and ordering information, see the TI website (http://www.iti.com)

**Figure 3-8. Device Nomenclature(B)**

## 3.9 Documentation Support

### 3.9.1 Related Documentation From Texas Instruments

The following documents describe the TMS320DM646x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided.

The current documentation that describes the DM646x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

**SPRUEP8** ***TMS320DM646x DMSoC DSP Subsystem Reference Guide.*** Describes the digital signal processor (DSP) subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

**SPRUEP9** ***TMS320DM646x DMSoC ARM Subsystem Reference Guide.*** Describes the ARM subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem and a majority of the peripherals and external memories.

**SPRUEQ0** ***TMS320DM646x DMSoC Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the TMS320DM646x Digital Media System-on-Chip (DMSoC).

**SPRAA84** ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

**SPRU732** ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

**SPRU871** ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

**SPRAAV0** ***Understanding TI's PCB Routing Rule-Based DDR Timing Specification Application Report*** This application report describes the way the DDR high-speed timing requirements are now going to be communicated to system designers. The system designer uses this information to evaluate whether timing specifications are met and can be expected to operate reliably.

## 3.10 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.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# 4 Device Configurations

## 4.1 System Module Registers

The system module includes status and control registers for configuration of the device.Brief descriptions of the various registers are shown in Table 4-1. System Module registers required for device configurations are discussed in the following sections.

**Table 4-1. System Module Register Memory Map**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C4 0000 | PINMUX0 | Pin Multiplexing Control 0 (see Section 4.7.2.1, *PINMUX0 Register*). |
| 0x01C4 0004 | PINMUX1 | Pin Multiplexing Control 1 (see Section 4.7.2.2, *PINMUX1 Register*). |
| 0x01C4 0008 | DSPBOOTADDR | DSP Boot Address. Decoded by bootloader software for host boots. (See Section 4.4.2.1, *DSPBOOTADDR Register*.) |
| 0x01C4 000C | SUSPSRC | Emulator Suspend Source (see Section 4.7.3.12, *Emulation Control*). |
| 0x01C4 0010 | BOOTSTAT | Boot Status (see Section 4.4.2.2, *BOOTSTAT Register*). |
| 0x01C4 0014 | BOOTCFG | Device Boot Configuration (see Section 4.4.2.3, *BOOTCFG Register*). |
| 0x01C4 0018 | – | Reserved |
| 0x01C4 001C - 0x01C4 0020 | – | Reserved |
| 0x01C4 0024 | ARMBOOT | ARM926 Boot Control (see Section 4.4.2.4, *ARMBOOT Register*). |
| 0x01C4 0028 | JTAGID | Device ID Number [see Section 7.29.1, *JTAG ID (JTAGID) Register Description(s)*]. |
| 0x01C4 002C | – | Reserved |
| 0x01C4 0030 | HPICTL | HPI Control (see Section 4.6.2.1, *HPICTL Register*). |
| 0x01C4 0034 | USBCTL | USB Control (see Section 4.6.2.2, *USBCTL Register*). |
| 0x01C4 0038 | VIDCLKCTL | Video Clock Control (see Section 4.3.2.1, *Video Clock Control*). |
| 0x01C4 003C | MSTPRI0 | Bus Master Priority Control 0 (see Section 4.6.1, Switch Central Resource (SCR) Bus Priorities). |
| 0x01C4 0040 | MSTPRI1 | Bus Master Priority Control 1 (see Section 4.6.1, Switch Central Resource (SCR) Bus Priorities). |
| 0x01C4 0044 | MSTPRI2 | Bus Master Priority Control 2 (see Section 4.6.1, Switch Central Resource (SCR) Bus Priorities). |
| 0x01C4 0048 | VDD3P3V_PWDN | $V_{DD}$ 3.3-V I/O Powerdown Control (see Section 4.2, *Power Considerations*). |
| 0x01C4 004C | – | Reserved |
| 0x01C4 0050 | TSIFCTL | TSIF Control Register (see Section 4.3.2.2, *TSIF Control*). |
| 0x01C4 0054 | PWMCTL | PWM Control (see Section 4.6.2.3, *PWM (Trigger Source) Control Register*). |
| 0x01C4 0058 | EDMATCCFG | EDMA TC Configuration (see Section 4.6.2.4, *EDMATCCFG Register*). |
| 0x01C4 005C | CLKCTL | Oscillator and Output Clock Control (see Section 4.3.3, *Clock and Oscillator Control*). |
| 0x01C4 0060 | DSPINT | ARM to DSP Interrupt Status (see Section 4.7.3.11, *ARM/DSP Communications Interrupts*). |
| 0x01C4 0064 | DSPINTSET | ARM to DSP Interrupt Set (see Section 4.7.3.11, *ARM/DSP Communications Interrupts*). |
| 0x01C4 0068 | DSPINTCLR | ARM to DSP Interrupt Clear (see Section 4.7.3.11, *ARM/DSP Communications Interrupts*). |
| 0x01C4 006C | VSCLKDIS | Video and TSIF Clock Disable (see Section 4.3.2.3, *Video and TSIF Clock Disable*). |
| 0x01C4 0070 | ARMINT | DSP to ARM Interrupt Status (see Section 4.7.3.11, *ARM/DSP Communications Interrupts*). |
| 0x01C4 0074 | ARMINTSET | DSP to ARM Interrupt Set (see Section 4.7.3.11, *ARM/DSP Communications Interrupts*). |

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**Table 4-1. System Module Register Memory Map (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C4 0078 | ARMINTCLR | DSP to ARM Interrupt Clear (see Section 4.7.3.11, *ARM/DSP Communications Interrupts*). |
| 0x01C4 007C | ARMWAIT | ARM Memory Wait State Control (see Section 4.4.2.5, *ARMWAIT Register*). |
| 0x01C4 0080 - 0x01C4 03FF | – | Reserved |


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## 4.2 Power Considerations

The DM6467T provides several means of managing power consumption.

As described in the Section 7.3.4, *DM6467T Power and Clock Domains*, the DM6467T has one single power domain—the "Always On" power domain. Within this power domain, the DM6467T utilizes local clock gating via the Power and Sleep Controller (PSC) to achieve power savings. For more details on the PSC, see Section 7.3.5, *Power and Sleep Controller (PSC)* and the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

Some of the DM6467T peripherals support additional power saving features. For more details on power saving features supported, see the peripheral-specific reference guides [listed/linked in the *TMS320DM646x DMSoC Peripherals Overview* Reference Guide (literature number SPRUEQ0).

Most DM6467T 3.3-V I/Os can be powered-down to reduce power consumption. The VDD3P3V_PWDN register in the System Module (see Figure 4-1 ) is used to selectively power down unused 3.3-V I/O pins.

**Note:** To save power, all other I/O buffers are powered down by default. Before using these pins, the user ***must*** program the VDD3P3V_PWDN register to power up the corresponding I/O buffers.

For a list of multiplexed pins on the device and the pin mux group each pin belongs to, see Section 4.7.3, *Pin Multiplexing Details*.

**Note:** The VDD3P3V_PWDN register *only* controls the power to the I/O buffers. The Power and Sleep Controller (PSC) determines the clock/power state of the peripheral.

| 31 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | USBV | CLKOUT | RSV | SPI | VLYNQ | RESERVED | | GMII | MII | MCASP1 | MCASP0 | PCIHPI1 | PCIHPI0 |
| R-000 | | R/W-1 | R/W-0 | R-0 | R/W-1 | R/W-1 | R-00 | | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GPIO | WDTIM | TIM23 | TIM01 | PWM1 | PWM0 | UR2FC | UR2DAT | UR1FC | UR1DAT | UR0MDM | UR0DF | VPIF3 | VPIF2 | VPIF1 | VPIF0 |
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-1. VDD3P3V_PWDN Register [0x01C4 0048]**

**Table 4-2. VDD3P3V_PWDN Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:29 | RESERVED | Reserved. Read returns "0". |
| 28 | USBV | USB_DRVVBUS Powerdown Control.<br>0 = I/O cells powered up.<br>1 = I/O cells powered down.<br>This bit controls the USB_DRVVBUS/GP[22] pin. |
| 27 | CLKOUT | CLKOUT0 Powerdown Control.<br>This bit controls the CLKOUT0 pin. |
| 26 | RSV | Reserved. Read returns "0". |
| 25 | SPI | SPI Powerdown Control.<br>This bit controls the six SPI interface pins: SPI_CLK, SPI_EN, SPI_CS0, SPI_CS1, SPI_SOMI, and SPI_SIMO. |
| 24 | VLYNQ | VLYNQ Powerdown Control.<br>This bit controls the ten VLYNQ interface pins: VLYNQ_CLOCK, VLYNQ_SCRUN, VLYNQ_TXD[3:0], and VLYNQ_RXD[3:0]. |
| 23:22 | RESERVED | Reserved. Read returns "0". |
| 21 | GMII | GMII Powerdown Control.<br>This bit controls the ten pins used by GMII (Gigabit) only: RFTCLK, GMTCLK, MTXD[7:4], and MRXD[7:4]. |
| 20 | MII | MII Powerdown Control.<br>This bit controls the 17 pins used by (G)MII (10/100/1000) and MDIO interfaces: MTCLK, MTXD[3:0], MTXEN, MCOL, MCRS, MRCLK, MRXD[3:0], MRXDV, MRXER, MDCLK, and MDIO. |
| 19 | MCASP1 | McASP1 Powerdown Control.<br>This bit controls the three McASP1 pins: ACLKX1, AHCLKX1, and AXR1[0]. |
| 18 | MCASP0 | McASP0 Powerdown Control.<br>This bit controls the 12 McASP0 pins: ACLKR0, AHCLKR0, AFSR0, ACLKX0, AHCLKX0, AFSX0, AXR0[3:0], AMUTE0, and AMUTEIN0. |
| 17 | PCIHPI1 | PCI/HPI/EMIFA/ATA Powerdown Control.<br>This bit controls the 28 pins used by the ATA or PCI`, HPI, or EMIFA. These pins include: PCI_RST/DA2/GP[13]/EM_A[22], PCI_IDSEL/HDDIR/EM_R/W, PCI_REQ/DMARQ/GP[11]/EM_CS5, PCI_GNT/DMACK/GP[12]/EM_CS4, PCI_CBE1/ATA_CS1/GP[32]/EM_A[19], PCI_CBE0/ATA_CS0/GP[33]/EM_A[18], DIOW/GP[20]/EM_WAIT4/(RDY4/BSY4), IORDY/GP[21]/EM_WAIT3/(RDY3/BSY3), DIOR/GP[19]/EM_WAIT5/(RDY5/BSY5), DA1/GP[16]/EM_A[21], DA0/GP[17]/EM_A[20], INTRQ/GP[18]/RSV , PCI_AD[31:16]/DD[15:0]/HD[31:16]/EM_A[15:0]<br>Defaults to powered up for NOR boot. |
| 16 | PCIHPI0 | PCI/HPI/EMIFA Powerdown Control.<br>This bit controls the 28 pins used by PCI, HPI, or EMIFA but not shared with ATA. These pins include: PCI_CLK/GP[10], PCI_DEVSEL/HCNTL1/EM_BA[1], PCI_FRAME/HINT/EM_BA[0], PCI_IRDY/HRDY/EM_A[17]/(CLE), PCI_TRDY/HHWIL/EM_A[16]/(ALE), PCI_STOP/HCNTL0/EM_WE, PCI_SERR/HDS1/EM_OE, PCI_PERR/HCS/EM_DQM1, PCI_PAR/HAS/EM_DQM0, PCI_INTA/EM_WAIT2/(RDY2/BSY2), PCI_CBE3/HR/W/EM_CS3, PCI_CBE2/HDS2/EM_CS2, PCI_AD[15:0]/HD[15:0]/EM_D[15:0]<br>Defaults to powered up for NOR boot. |
| 15 | GPIO | GPIO Powerdown Control.<br>This bit controls the eight GP[7:0] pins. Defaults to powered up. |
| 14 | WDTIM | WD Timer Powerdown Control.<br>This bit controls the WD Timer pin TOUT2. |
| 13 | TIM23 | Timer1 Powerdown Control.<br>This bit controls the three Timer1 pins TINP1L, TOUT1L, and TOUT1U. |
| 12 | TIM01 | Timer0 Powerdown Control.<br>This bit controls the four Timer0 pins TINP0L, TINP0U, TOUT0L, and TOUT0U. |
| 11 | PWM1 | PWM1 Powerdown Control.<br>This bit controls the PWM1/TS1_DOUT pin. |
| 10 | PWM0 | PWM0 Powerdown Control.<br>This bit controls the PWM0/CRG0_PO/TS1_ENAO pin. |
| 9 | UR2FC | UART2 Flow Control Powerdown Control.<br>This bit controls the URTS2/UIRTX2/TS0_PSTIN/GP[41] and UCTS2/USD2/CRG0_VCXI/GP[42]/TS1_PSTO pins. |


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**Table 4-2. VDD3P3V_PWDN Register Bit Descriptions (continued)**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 8 | UR2DAT | UART2 Data Powerdown Control.<br>This bit controls the URXD2/CRG1_VCXI/GP[39]/CRG0_VCXI and UTXD2/URCTX2/CRG1_PO/GP[40]/CRG0_PO pins. |
| 7 | UR1FC | UART1 Flow Control Powerdown Control.<br>This bit controls the $\overline{\text{URTS1}}$/UIRTX1/TS0_WAITO/GP[25] and $\overline{\text{UCTS1}}$/USD1/TS0_EN_WAITO/GP[26] pins. |
| 6 | UR1DAT | UART1 Data Powerdown Control.<br>This bit controls the URXD1/TS0_DIN7/GP[23] and UTXD1/URCTX1/TS0_DOUT7/GP[24] pins. |
| 5 | UR0MDM | UART0 Modem Control Powerdown Control.<br>This bit controls the $\overline{\text{UDTR0}}$/TS0_ENAO/GP[36], $\overline{\text{UDSR0}}$/TS0_PSTO/GP[37], UDCD0/TS0_WAITIN/GP[38], and URIN0/GP[8]/TS1_WAITIN pins. |
| 4 | UR0DF | UART0 Data and Flow Control Powerdown Control.<br>This bit controls the URXD0/TS1_DIN, $\overline{\text{UTXD0}}$/URCTX0/TS1_PSTIN, $\overline{\text{URTS0}}$/UIRTX0/TS1_EN_WAITO, and $\overline{\text{UCTS0}}$/USD0 pins. |
| 3 | VPIF3 | VPIF MSB Output Powerdown Control.<br>This bit controls the VP_DOUT[15:8]/TS1_xx, VP_CLKIN3/TS1_CLKO, and VP_CLKO3/TS0_CLKO pins. |
| 2 | VPIF2 | VPIF LSB Output Powerdown Control.<br>This bit controls the VP_DOUT[7:0], VP_CLKIN2, and VP_CLKO2 pins. (VP_DOUT[7:0] are boot configuration inputs.) |
| 1 | VPIF1 | VPIF MSB Input Powerdown Control.<br>This bit controls the VP_DIN[15:8]/TS0_DIN[7:0] and VP_CLKIN1 pins. |
| 0 | VPIF0 | VPIF LSB Input Powerdown Control.<br>This bit controls the VP_DIN[3:0]/TS0_DOUT[3:0], VP_DIN[7:4]/TS0_DOUT[7:4]/TS1_xx, and VP_CLKIN0 pins. |

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## 4.3 Clock Considerations

Global device and local peripheral clocks are controlled by the PLL Controllers (PLLC1 and PLLC2) and the Power and Sleep Controller (PSC). In addition, the System Module Video Clock Control (VIDCLKCTL), TSIF Control (TSIFCTL), and Clock and Oscillator Control (CLKCTL) registers configure the clock sources to the VPIF, TSIF, CRGEN peripherals, and the Auxiliary Oscillator.

The selected Video, TSIF, and CRGEN module input clocks are disabled using the System Module Video Source Clock Disable (VSCLKDIS) register. **Note:** To ensure glitch-free operation, the clock should be disabled before changing the clock source frequency or muxing via the VIDCLKCTL and TSIFCTL.

### *4.3.1 Clock Configurations after Device Reset*

After device reset, the user is responsible for programming the PLL Controllers (PLLC1 and PLLC2) and the Power and Sleep Controller (PSC) to bring the device up to the desired clock frequency and the desired peripheral clock state (clock gating *or* not).

For additional power savings, some of the DM6467T peripherals support clock gating within the peripheral boundary. For more details on clock gating and power saving features supported by a specific peripheral, see the peripheral-specific reference/user's guides [listed/linked in the *TMS320DM646x DMSoC Peripherals Overview* Reference Guide (literature number SPRUEQ0)].

#### 4.3.1.1 Device Clock Frequency

The DM6467T defaults to PLL bypass mode. If the ROM bootloader is selected (BTMODE[3:0] ≠ 0100), the bootloader code programs PLLC1 and PLLC2.

Section 4.4.1, *Boot Modes* discusses the different boot modes in more detail.

The user ***must*** adhere to the various clock requirements when programming the PLLC1 and PLLC2:

- PLL multiplier and frequency ranges. For more details on PLL multiplier and frequency ranges, see Section 7.5.1, *PLL1 and PLL2*.

#### 4.3.1.2 Module Clock State

The clock and reset state for each of the modules is controlled by the Power and Sleep Controller (PSC). Table 4-3 shows the default state of each module after a device-level global reset. The DM6467T device has four different module states—Enable, Disable, SyncReset, *or* SwRstDisable. For more information on the definitions of the module states, the PSC, and PSC programming, see Section 7.3.5, *Power and Sleep Controller (PSC)* and the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).


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**Table 4-3. DM6467T Default Module States**

| LPSC # | MODULE NAME | DEFAULT MODULE STATE [PSC Register MDSTATn.STATE] |
|---|---|---|
| 0 | ARM | Enable |
| 1 | DSP C64x+ | If DSPBOOT = 0 then, Enable and Module Local Reset is asserted (MDSTATn.LRST = 0).<br>If DSPBOOT = 1 then, Enable and Module Local Reset is asserted (MDSTATn.LRST = 1). |
| 2 | HDVICP0 | SwRstDisable |
| 3 | HDVICP1 | SwRstDisable |
| 4 | EDMACC | SwRstDisable |
| 5 | EDMATC0 | SwRstDisable |
| 6 | EDMATC1 | SwRstDisable |
| 7 | EDMATC2 | SwRstDisable |
| 8 | EDMATC3 | SwRstDisable |
| 9 | USB2.0 | SwRstDisable |
| 10 | ATA | SwRstDisable |
| 11 | VLYNQ | SwRstDisable |
| 12 | HPI | SwRstDisable |
| 13 | PCI | SwRstDisable |
| 14 | EMAC/MDIO | SwRstDisable |
| 15 | VDCE | SwRstDisable |
| 16 – 17 | Video Port(1) | SwRstDisable |
| 18 | TSIF0 | SwRstDisable |
| 19 | TSIF1 | SwRstDisable |
| 20 | DDR2 Memory Contoller | SwRstDisable |
| 21 | EMIFA | If BTMODE[3:0] ≠ 0100 and DSPBOOT = 0 then, SwRstDisable<br>If BTMODE[3:0] = 0100 or DSPBOOT = 1 then, Enable |
| 22 | McASP0 | SwRstDisable |
| 23 | McASP1 | SwRstDisable |
| 24 | CRGEN0 | SwRstDisable |
| 25 | CRGEN1 | SwRstDisable |
| 26 | UART0 | SwRstDisable |
| 27 | UART1 | SwRstDisable |
| 28 | UART2 | SwRstDisable |
| 29 | PWM0 | SwRstDisable |
| 30 | PWM1 | SwRstDisable |
| 31 | I2C | SwRstDisable |
| 32 | SPI | SwRstDisable |
| 33 | GPIO | SwRstDisable |
| 34 | TIMER0 | SwRstDisable |
| 35 | TIMER1 | SwRstDisable |
| 36 – 44 | Reserved | Reserved |
| 45 | ARM INTC | Enable |

(1) The Video Port Module has a total of five clock inputs that can be controlled by the LPSC. One LPSC can support only a maximum of four clocks; therefore, two LPSCs are assigned to the Video Port. Both Video Port LPSCs should be controlled together and should be set to the same state.

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### 4.3.2 Clock Control

This section describes the following registers: the VPIF (Video)/TSIF clock control and clock disable registers and the Clock and Oscillator control register.

#### 4.3.2.1 Video Clock Control Register

The Video Clock Control (VIDCLKCTL) register allows the user to select/control the clock muxing for the video channels' (i.e., channels 1, 2, and 3) output clock source.

| 31 | 16 |
|---|---|
| RESERVED | |
| R-0000 0000 0000 0000 | |

| 15 | 14 12 | 11 | 10 8 | 7 5 | 4 | 3 0 |
|---|---|---|---|---|---|---|
| RSV | VCH3CLK | RSV | VCH2CLK | RESERVED | VCH1CLK | RESERVED |
| R-0 | R/W-111 | R-0 | R/W-110 | R-000 | R/W-1 | R-0000 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-2. VIDCLKCTL Register [0x01C4 0038]**

**Table 4-4. VIDCLKCTL Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:15 | RESERVED | Reserved. Read returns "0". |
| 14:12 | VCH3CLK | Video Channel 3 Clock Source.<br>This field selects the clock source for the Channel 3 output source clock.<br>000 = CRG0_VCXI (external pin)<br>001 = CRG1_VCXI (external pin)<br>010 = SYSCLK8 (PLLC1)<br>011 = AUXCLK (PLLC1)<br>100 = VP_CLKIN0 (external pin)<br>101 = STC_CLKIN (external pin)<br>110 = VP_CLKIN2 (external pin)<br>111 = VP_CLKIN3 (external pin) |
| 11 | RSV | Reserved. Read returns "0". |
| 10:8 | VCH2CLK | Video Channel 2 Clock Source.<br>This field selects the clock source for the Channel 2 output source clock.<br>000 = CRG0_VCXI (external pin)<br>001 = CRG1_VCXI (external pin)<br>010 = SYSCLK8 (PLLC1)<br>011 = AUXCLK (PLLC1)<br>100 = VP_CLKIN0 (external pin)<br>101 = STC_CLKIN (external pin)<br>110 = VP_CLKIN2 (external pin)<br>111 = Reserved |
| 7:5 | RESERVED | Reserved. Read returns "0". |
| 4 | VCH1CLK | Video Channel 1 Clock Source.<br>This bit selects the clock source for the Channel 1 input clock.<br>0 = VP_CLKIN0 (external pin)<br>1 = VP_CLKIN1 (external pin) |
| 3:0 | RESERVED | Reserved. Read returns "0". |


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### 4.3.2.2 TSIF Control

The TSIF Control (TSIFCTL) registers allows the user to select/control the clock muxing for the counter and serial output of TSIF1 *and*the counter and parallel/serial output for TSIF0.

| 31 | 16 |
|---|---|
| RESERVED | |
| R-0000 0000 0000 0000 | |

| 15 | 14 12 | 11 8 | 7 | 6 4 | 3 | 2 0 |
|---|---|---|---|---|---|---|
| RSV | TSIF1_CNTCLK | TSSO_CLK | RSV | TSIF0_CNTCLK | RSV | TSPO_CLK |
| R-0 | R/W-000 | R/W-0000 | R-0 | R/W-000 | R-0 | R/W-000 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-3. TSIFCTL Register [0x01C4 0050]**

**Table 4-5. TSIFCTL Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:15 | RESERVED | Reserved. Read returns "0". |
| 14:12 | TSIF1_CNTCLK | TSIF1 Counter Clock Source.<br>This field selects the clock source for the TSIF1 module's counter.<br>000 = CRG1_VCXI (external pin)<br>001 = STC_CLKIN (external pin)<br>010 = AUXCLK (PLLC1 output)<br>011 = CRG0_VCXI (external pin)<br>100 = VP_CLKIN2 (external pin)<br>101 = VP_CLKIN3 (external pin)<br>110 = Reserved<br>111 = Reserved |
| 11:8 | TSSO_CLK | TSIF1 Serial Output Clock Source.<br>This field selects the clock source for the TSIF1 output source clock.<br>0000 = CRG1_VCXI (external pin)<br>0001 = STC_CLKIN (external pin)<br>0010 = SYSCLK6 (PLLC1)<br>0011 = SYSCLKBP (PLLC1)<br>0100 = VP_CLKIN0 (external pin)<br>0101 = TS1_CLKIN (external pin)<br>0110 = VP_CLKIN2 (external pin)<br>0111 = Reserved<br>1000 = CRG0_VCXI<br>1001 = Reserved<br>1xx1 = Reserved |
| 7 | RSV | Reserved. Read returns "0". |
| 6:4 | TSIF0_CNTCLK | TSIF0 Counter Clock Source.<br>This field selects the clock source for the TSIF0 module's counter.<br>000 = CRG0_VCXI (external pin)<br>001 = STC_CLKIN (external pin)<br>010 = AUXCLK (PLLC1 output)<br>011 = CRG1_VCXI (external pin)<br>100 = VP_CLKIN0 (external pin)<br>101 = VP_CLKIN1 (external pin)<br>110 = Reserved<br>111 = Reserved |
| 3 | RSV | Reserved. Read returns "0". |
| 2:0 | TSPO_CLK | TSIF0 Parallel/Serial Output Clock Source.<br>This field selects the clock source for the TSIF0 output source clock.<br>000 = CRG0_VCXI (external pin)<br>001 = STC_CLKIN (external pin)<br>010 = SYSCLK5 (PLLC1)<br>011 = SYSCLKBP (PLLC1)<br>100 = VP_CLKIN0 (external pin)<br>101 = VP_CLKIN1 (external pin)<br>110 = TS0_CLKIN (external pin)<br>111 = CRG1_VCXI (external pin) |

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#### 4.3.2.3 Video and TSIF Clock Disable

The Video Source Clock Disable (VSCLKDIS) register allows the user to disable the selected Video (VPIF), TSIF, and CRGEN module input clocks.

**Note:** To ensure glitch-free operation, the clock should be disabled before changing the clock source frequency or muxing via the VIDCLKCTL and TSIFCTL.

| 31 | 16 |
|---|---|
| RESERVED | |
| R-0000 0000 0000 0000 | |

| 15 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | VID3 | VID2 | VID1 | VID0 | TSIFCNT1 | TSIFCNT0 | TSIFTX1 | TSIFTX0 | TSIFRX1 | TSIFRX0 | CRG1 | CRG0 |
| R-0000 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-4. VSCLKDIS Register [0x01C4 006C]**

**Table 4-6. VSCLKDIS Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:12 | RESERVED | Reserved. Read returns "0". |
| 11 | VID3 | VPIF Channel 3 Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 10 | VID2 | VPIF Channel 2 Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 9 | VID1 | VPIF Channel 1 Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 8 | VID0 | VPIF Channel 0 Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 7 | TSIFCNT1 | TSIF1 Counter Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 6 | TSIFCNT0 | TSIF0 Counter Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 5 | TSIFTX1 | TSIF1 Transmit Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 4 | TSIFTX0 | TSIF0 Transmit Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 3 | TSIFRX1 | TSIF1 Receive Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 2 | TSIFRX0 | TSIF0 Receive Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 1 | CRG1 | CRGEN1 Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |
| 0 | CRG0 | CRGEN0 Clock Disable.<br>0 = Clock enabled.<br>1 = Clock disabled. |


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### 4.3.3 Clock and Oscillator Control

The Clock and Oscillator Control (CLKCTL) register allows the user to disable the OSC pwrdwn and pwr disable

| 31 | 26 | 25 | 24 | 23 | 20 | 19 | 16 |
|---|---|---|---|---|---|---|---|
| RESERVED | | OSCPWRDN | OSCDIS | RESERVED | | CLKOUT | |
| R-0000 00 | | R/W-0 | R/W-1 | R-0000 | | R/W-1000 | |

| 15 | 12 | 11 | 8 | 7 | 4 | 3 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | AUD_CLK1 | | RESERVED | | AUD_CLK0 | |
| R-0000 | | R/W-0000 | | R-0000 | | R/W-0000 | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-5. CLKCTL Register [0x01C4 005C]**

**Table 4-7. CLKCTL Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:26 | RESERVED | Reserved. Read returns "0". |
| 25 | OSCPWRDN | Auxiliary Oscillator Powerdown.<br>This bit controls the internal bias resistor conection.<br>0 = Internal bias resistor connected (normal operation)<br>1 = Internal bias resistor disconnected (external bias resistor required or clock input used) |
| 24 | OSCDIS | Auxiliary Oscillator Disable.<br>This bit disables the oscillator.<br>0 = Oscillator enabled (normal operation).<br>1 = Oscillator disabled (clock input used or no Auxiliary clock required). |
| 23:20 | RESERVED | Reserved. Read returns "0". |
| 19:16 | CLKOUT | CLKOUT0 Source(1)<br>This field selects the clock source for the CLKOUT0 output.<br>0000 = Disabled<br>0001 = PLL1 AUXCLK<br>0010 = Reserved<br>0011 = SYSCLK3<br>0100 = SYSCLK4<br>0101 = SYSCLK5<br>0110 = SYSCLK6<br>0111 = Reserved<br>1000 = SYSCLK8<br>1001 = SYSCLK9<br>1010 = AUX_MXI<br>1011 = Reserved<br>1100 = Reserved<br>1101 = Reserved<br>1110 = Reserved<br>1111 = Reserved |
| 15:12 | RESERVED | Reserved. Read returns "0". |

(1) The maximum frequency allowed for the CLKOUT0 pin is 148.5 MHz. Do not configure the CLKOUT bits to any SYSCLKx that is greater than 148.5 MHz. For more details on the CLKOUT0 timings, see Table 7-14, *Switching Characteristics Over Recommended Operating Conditions for CLKOUT0*.

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**Table 4-7. CLKCTL Register Bit Descriptions (continued)**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 11:8 | AUD_CLK1 | AUDIO_CLK1 Source.<br>This field selects the clock source for the AUDIO_CLK1 output.<br>0000 = Disabled<br>0001 = PLL1 AUXCLK<br>0010 = CRG0_VCXI<br>0011 = CRG1_VCXI<br>0100 = VP_CLKIN0<br>0101 = VP_CLKIN1<br>0110 = VP_CLKIN2<br>0111 = VP_CLKIN3<br>1000 = AUX_MXI<br>1001 = STC_CLKIN<br>1010 = Reserved<br>1011 = Reserved<br>1100 = Reserved<br>1101 = Reserved<br>1110 = Reserved<br>1111 = Reserved |
| 7:4 | RESERVED | Reserved. Read returns "0". |
| 3:0 | AUD_CLK0 | AUDIO_CLK0 Source.<br>This field selects the clock source for the AUDIO_CLK0 output.<br>0000 = Disabled<br>0001 = PLL1 AUXCLK<br>0010 = CRG0_VCXI<br>0011 = CRG1_VCXI<br>0100 = VP_CLKIN0<br>0101 = VP_CLKIN1<br>0110 = VP_CLKIN2<br>0111 = VP_CLKIN3<br>1000 = AUX_MXI<br>1001 = STC_CLKIN<br>1010 = Reserved<br>1011 = Reserved<br>1100 = Reserved<br>1101 = Reserved<br>1110 = Reserved<br>1111 = Reserved |


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## 4.4 Boot Sequence

The boot sequence is a process by which the device's memory is loaded with program and data sections, and by which some of the device's internal registers are programmed with predetermined values. The boot sequence is started automatically after each device-level global reset. For more details on device-level global resets, see Section 7.7, *Reset*.

There are several methods by which the memory and register initialization can take place. Each of these methods is referred to as a boot mode. The boot mode to be used is selected at reset. For more information on the bootmode selections, see Section 4.4.1, *Boot Modes*.

The device is booted through multiple means—primary bootloaders within internal ROM or EMIFA, and secondary user bootloaders from peripherals or external memories. Boot modes, pin configurations, and register configurations required for booting the device, are described in the following subsections.

### *4.4.1 Boot Modes*

The DM6467T boot modes are determined by these device boot and configuration pins. For information on how these pins are sampled at device reset, see Section 7.7.1.2, *Latching Boot and Configuration Pins*.

- BTMODE[3:0]
- PCIEN
- CS2BW
- DSPBOOT

The TMS320DM646x DMSoC ARM can boot either from asynchronous EMIF/NOR Flash or from ARM ROM, as determined by the device boot and configuration pins at reset (BTMODE[3:0] and PCIEN). The PCIEN pin configuration is used to select the default configuration of the EMIFA/PCI/HPI pins at reset. This allows the DM646xT DMSoC to be PCI-compliant at reset. When PCIEN = 1, the PCI module controls the multiplexed pins with the appropriate pullup/pulldown configuration. For all other bootmodes (non-PCI bootmodes), the PCIEN ***must*** be cleared to "0".

For a more detailed description of the ROM boot modes supported by the DM646xT DMSoC, see Using the *TMS320DM646x Bootloader* Application Report (literature number SPRAAS0).

### *4.4.2 Boot Mode Registers*

The DSPBOOTADDR, BOOTCMPLT, BOOTCMD, and BOOTCFG registers are used to control boot and device configurations.

#### 4.4.2.1 DSPBOOTADDR Register

The DSPBOOTADDR register contains the upper 22 bits of the DSP reset vector.

| 31 | 10 | 9 | 0 |
|---|---|---|---|
| BOOTADDR[21:0] | | RESERVED | |
| R/W-0100 0010 0010 0000 0000 00 | | R-00 0000 0000 | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-6. DSPBOOTADDR Register**

**Table 4-8. DSPBOOTADDR Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:10 | BOOTADDR[21:0] | Upper 22 bits of the C64x+ DSP boot address. |
| 9:0 | RESERVED | Reserved |

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#### 4.4.2.2 BOOTSTAT Register

The Boot Status (BOOTSTAT) register indicates the status of the device boot process (e.g., boot error, boot complete, or watchdog timer reset).

| 31 | 30 | 20 | 19 | 16 |
|---|---|---|---|---|
| WDRST | RESERVED | | BOOTERR | |
| R/W-0 | R-000 0000 0000 | | R-0000 | |

| 15 | 1 | 0 |
|---|---|---|
| RESERVED | | BC |
| R-0000 0000 0000 000 | | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-7. BOOTSTAT Register**

**Table 4-9. BOOTSTAT Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31 | WDRST | Watchdog Timer Reset.<br>0 = Device reset was not a result of a watchdog timer timeout.<br>1 = Device reset was a result of a watchdog timer timeout.<br>This is a "sticky" bit that can be used to debug WD timeout conditions. The bit is set when a WD timeout occurs (TOUT2). This bit is reset (to "0") by a $\overline{\text{POR}}$ reset only; otherwise it retains its value. It is ***not*** cleared by a Warm Reset or Soft Reset.<br>The bit may be cleared by writing a "1". |
| 30:20 | RESERVED | Reserved. Read returns "0". |
| 19:16 | BOOTERR | Boot Error.<br>0000 = No boot error [**default**].<br>Others = Bootloader detected boot error.<br>The exact meaning of the various error codes will be determined by the bootloader software. |
| 15:1 | RESERVED | Reserved. Read returns "0". |
| 0 | BC | Boot Complete.<br>0 = Host has ***not*** completed the boot sequence [**default**].<br>1 = Host has completed the boot sequence.<br>This bit may be optionally set by a host boot device (such as PCI or HPI) to indicate that it has finished loading code. The ARM926 can poll this bit to determine whether to continue the boot process. |


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#### 4.4.2.3 BOOTCFG Register

The Boot Configuration (BOOTCFG) register is a *read-only* register that indicates the value of the device bootmode and configuration pins latched at the end of reset. During a hard reset (POR or RESET pin active [low]), the values of the CFG pins (i.e., BTMODE[3:0], CS2BW, PCIEN, DSPBOOT) are propagated through the BOOTCFG register to the Boot Controller. When RESET or POR is de-asserted, the value of the pins is latched. The BOOTCFG value *does not* change as a result of a soft reset, instead the value latched at the end of the previous global reset is retained.

| 31 | 18 | 17 | 16 |
|---|---|---|---|
| RESERVED | | DSP_BT | PCIEN |
| R-0000 0000 0000 00 | | R-L | R-L |

| 15 | 9 | 8 | 7 | 4 | 3 | 0 |
|---|---|---|---|---|---|---|
| RESERVED | | CS2_BW | RESERVED | | BOOTMODE | |
| R-0000000 | | R-L | R-0000 | | R-LLLL | |

LEGEND: R = Read only; L = Latched pin value; -*n* = value after reset

**Figure 4-8. BOOTCFG Register**

**Table 4-10. BOOTCFG Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:18 | RESERVED | Reserved. Read returns "0". |
| 17 | DSP_BT | DSP Boot. Latched from DSPBOOT input at the rising edge of RESET or POR.<br>0 = ARM boots C64x+.<br>1 = C64x+ self-boots.<br>This bit will cause the DSP to be released from reset automatically. The C64x+ will boot from EMIFA (default DSPBOOTADDR address 0x4220 0000). If BOOTMODE = 0010 or 0011, or PCIEN = 1, then the C64x+ self-boot will fail since EMIFA will be disabled. |
| 16 | PCIEN | PCI Enable. Latched from PCIEN input at the rising edge of RESET or POR.<br>0 = PCI disabled.<br>1 = PCI enabled.<br>PCIEN = 1 disables the internal pullup and pulldown resistors on the PCI pins and configures the pin muxing for PCI. |
| 15:9 | RESERVED | Reserved. Read returns "0". |
| 8 | CS2_BW | EMIFA EM_CS2 Default Bus Width. Latched from CS2BW input at the rising edge of RESET or POR.<br>0 = Default to 8-bit operation.<br>1 = Default to 16-bit operation.<br>This bit determines the default bus width of the EMIFA EM_CS2 memory space. This ensures that boot from EMIFA (ARM or DSP) will correctly read the attached memory. |
| 7:4 | RESERVED | Reserved. Read returns "0". |
| 3:0 | BOOTMODE | Boot Mode Configuration Bits. Bit values latched from BTMODE[3:0] at the rising edge of RESET or POR.<br>0000 = Emulation boot.<br>0001 = Reserved.<br>0010 = HPI-16 (if PCIEN = 0).<br>PCI without autoinitialization (if PCIEN = 1).<br>0011 = HPI-32 (if PCIEN = 0).<br>PCI with autoinitialization (if PCIEN = 1).<br>0100 = EMIFA direct boot (ROM/NOR) (if PCIEN = 0; error if PCIEN = 1 defaults to UART0).<br>0101 = Reserved.<br>0110 = I2C boot.<br>0111 = NAND Flash boot (if PCIEN = 0; error if PCIEN = 1 defaults to UART0).<br><br>1000 = UART0 boot.<br>1001 = Reserved.<br>1010 = Reserved.<br>1011 = Reserved.<br>1100 = Reserved.<br>1101 = Reserved.<br>1110 = SPI boot.<br>1111 = Reserved. |


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#### 4.4.2.4 ARMBOOT Register

The ARM Boot Configuration (ARMBOOT) register is used to control the ARM926 boot. The ARMBOOT value *does not* change as a result of a soft reset, instead the last value written is retained.

When ROM boot is selected (BTMODE[3:0] ≠ 0100), a jump to the internal TCM ROM (0x0000 8000) is forced into the first fetched instruction word. The embedded ROM boot loader (RBL) code can then perform certain configuration steps, read the BOOTCFG register to determine the desired boot method, and branch to an appropriate secondary loader utility.

If EMIFA boot is selected (BTMODE[3:0] = 0100), a jump to the highest branch address (0x0200 0000) is forced into the first fetched instruction word. This must be modified to address 0x4200 0000 in order to map to the EMIFA. The ARM will then continue executing from external memory using the default EMIFA timings until modified by software. **Note:** that either NOR Flash or ROM ***must*** be connected to the first EMIFA chip select space (EM_CS2). The EMIFA ***does not*** support direct execution from NAND Flash.

| 31 | 5 | 4 | 3 | 1 | 0 |
|---|---|---|---|---|---|
| RESERVED | | ADDRMOD | RESERVED | | TRAMBOOT |
| R-0000 0000 0000 0000 0000 0000 000 | | R/W-C | R-000 | | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset

**Figure 4-9. ARMBOOT Register**

**Table 4-11. ARMBOOT Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:5 | RESERVED | Reserved. Read returns "0". |
| 4 | ADDRMOD | IAHB Address Modification.<br>0 = No address modification.<br>1 = Address bit 30 is tied high to modify IAHB fetch address to point to EMIFA.<br>The default value for this bit is determined by the BOOTMODE configuration bits (BTMODE[3:0]). If BTMODE[3:0] = 0100 [EMIFA direct boot (ROM/NOR)] , then ADDRMOD defaults to "1" so that instruction fetches from the ARM will point to EMIFA $\overline{CS2}$ memory space. For all other BTMODE[3:0] values, ADDRMOD defaults to "0" because ARM will boot from its TCM (ROM or RAM).<br>The ADDRMOD value is ignored when TRAMBOOT is set (1) [address modification is disabled].<br>After branching into the EMIFA $\overline{CS2}$ space, software should clear this bit as part of the reset routine so that subsequent IAHB access addresses are not modified. |
| 3:1 | RESERVED | Reserved. Read returns "0". |
| 0 | TRAMBOOT | ARM TCM RAM Boot.<br>0 = Use BTMODE[3:0] selected boot mode<br>1 = Boot from ITCM RAM<br>This is a "sticky" bit that can be used to force the ARM926 to boot from ITCM RAM. On $\overline{POR}$ reset, this bit will be initialized to "0" because TCM RAM is not initialized; otherwise, the bit retains the value. After initializing ITCM RAM, software can set this bit so that subsequent Warm Reset ($\overline{RESET}$) or Soft Reset will boot from the ITCM. |

#### 4.4.2.5 ARMWAIT Register

The ARM Wait State Control (ARMWAIT) register is used to control ARM926 accesses to its TCM RAM. At normal ARM operating frequency, a wait state ***must*** be inserted when accessing TCM RAM. When the device is operated at low speeds, performance may be increased by removing the wait state. **Note:** TCM ROM *will always* operate with a wait state enabled.

| 31 | 1 | 0 |
|---|---|---|
| RESERVED | | RAMWAIT |
| R-0000 0000 0000 0000 0000 0000 0000 000 | | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-10. ARMWAIT Register**

**Table 4-12. ARMWAIT Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:1 | RESERVED | Reserved. Read returns "0". |
| 0 | RAMWAIT | ARM TCM RAM Wait State Configuration.<br>0 = TCM RAM wait state disabled.<br>1 = TCM RAM wait state enabled. |


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## 4.5 Configurations At Reset

Some device configurations are determined at reset. The following subsections give more details.

### *4.5.1 Device and Peripheral Configurations at Device Reset*

Table 3-5, BOOT Terminal Functions lists the device boot and configuration pins that are latched at device reset for configuring basic device settings for proper device operation. Table 4-13, summarizes the device boot and configuration pins, and the device functions that they affect.

**Table 4-13. Default Functions Affected by Device Boot and Configuration Pins**

| DEVICE BOOT AND CONFIGURATION PINS | BOOT SELECTED | PIN MUX CONTROL | GLOBAL SETTING | PERIPHERAL SETTING |
|---|---|---|---|---|
| BOOTMODE[3:0] | Boot Mode | **PINMUX0/PINMUX1 Registers**: Based on BOOTMODE[3:0], the bootloader code programs PINMUX0 and PINMUX1 registers to select the appropriate pin functions required for boot. | **I/O Pin Power**: Based on BOOTMODE[3:0], the bootloader code programs VDD3P3V_PWDN register to power up the I/O pins required for boot. | **PSC/Peripherals**: Based on BOOTMODE[3:0], the bootloader code programs the PSC to put boot-related peripheral(s) in the Enable State, and programs the peripheral(s) for boot operation. |
| CS2BW | EMIFA Direct Boot Mode | PINMUX0.HPIEN = 0<br>PINMUX0.PCIEN = 0<br>PINMUIX0.ATAEN = 0 | – | The default width of the first EMIFA chip select space (CS2) is determined by the CS2BW value. If CS2BW = 0, the space defaults to 8-bits wide. If CS2BW = 1, it defaults to 16-bits wide. This allows the ARM to make full use of the width of the attached memory device when booting from EMIFA. |
| PCIEN (1) | **Host Boot**: PCIEN selects the type of Host Boot (HPI Boot *or* PCI Boot) | **PINMUX0.PCIEN**: sets this field to control the PCI pin muxing in . (1) (2) | – | **PSC/Peripheral** *(Applicable to Host Boot only)*: Based on the Host Boot type (PCI *or* HPI), the bootloader code programs the PSC to put the corresponding peripheral in the Enable State, and programs the peripheral for boot operation. |

(1) Software can modify all PINMUX0 and PINMUX1 bit fields from their defaults.
(2) In addition to pin mux control, PCIEN also affects the internal pullup/down resistors of the PCI capable pins. When PCIEN = 0, internal pullup/down resistors on the PCI capable pins are enabled. When PCIEN = 1, internal pullup/down resistors on the PCI capable pins are disabled to be compliant to the *PCI Local Bus Specification Revision 2.3*.

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**Table 4-13. Default Functions Affected by Device Boot and Configuration Pins (continued)**

| DEVICE BOOT AND CONFIGURATION PINS | BOOT SELECTED | PIN MUX CONTROL | GLOBAL SETTING | PERIPHERAL SETTING |
|---|---|---|---|---|
| DSPBOOT | Bit = 0, DSP is booted by the ARM<br>Bit =1, DSP boots self from EMIFA | – | – | **Note:** that either NOR Flash or ROM must be connected to the first EMIFA chip select space (CS2).<br>The EMIFA does not support direct execution from NAND Flash. Code within the EMIFA memory should execute a branch to the actual EMIFA address and then disable the Instruction Address Modification logic (by clearing the ADDRMOD bit in the ARMBOOT register of the System Module). |

For proper device operation, external pullup/pulldown resistors may be required on these device boot and configuration pins. For discussion situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.

Note: All DM6467T device configuration inputs (BOOTMODE[3:0], CS2BW, PCIEN, and DSPBOOT) are multiplexed with other functional pins. These pins function as device boot and configuration pins only during device reset. The user must take care of any potential data contention in the system. To help avoid system data contention, the DM6467T puts these configuration pins into a high-impedance state (Hi-Z) when device reset (RESET or POR) is asserted, and continues to hold them in a high-impedance state until the internal global reset is removed; at which point, the default peripheral (VPIF) will now control these pins.

All of the device boot and configuration pin settings are captured in the corresponding bit fields in the BOOTCFG register (see Section 4.4.2.3).

The following subsections provide more details on the device configurations determined at device reset: CS2BW, PCIEN, and DSPBOOT.

### 4.5.2 EMIFA CS2 Bus Width (CS2BW)

The default width of the first EMIFA chip select space (CS2) is determined by the CS2BW value. If CS2BW = 0, the space defaults to 8-bits wide. If CS2BW = 1, it defaults to 16-bits wide. This allows the ARM to make full use of the width of the attached memory device when booting from EMIFA.

**Note:** CS2BW ***only*** selects the default bus width. The EMIFA bus width may be changed at any time via software by accessing the appropriate EMIFA control register.

The default width affects ***only*** the first chip select space (CS2). All other chip select spaces default to 8-bits wide and ***must*** be modified using the appropriate EMIFA control register if 16-bit operation is desired.

### 4.5.3 PCI Enable (PCIEN)

The PCIEN configuration pin determines if the PCI peripheral is used on this device. If PCIEN = 1 indicating the PCI is used, then the PCI multiplexed pins default to PCI functions, and the pins' corresponding internal pullup/pulldown resistors are disabled. If PCIEN = 0 indicating the PCI is not used, then the PCI muxed pins default to non-PCI functions (e.g., EMIFA or HPI pin functions), and the pins' corresponding internal pullup/pulldown resistors are enabled.

The PCIEN setting is captured and stored in the BOOTCFG.PCIEN bit field, and also in the PINMUX0.PCIEN bit field.


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### 4.5.4 DSPBOOT

The DSPBOOT input determines DSP operation at reset. For most applications, the ARM is the master device and controls the reset and boot of the DSP. Under this scenario (DSPBOOT = 0), the DSP will remain disabled (held in reset) after reset. The ARM is responsible for releasing DSP from reset. Before releasing DSP from reset, the ARM must transfer a valid DSP boot image to program memory accessible by the DSP (DSP memory, EMIFA or DDR2), and configure the DSP boot address in DSPBOOTADDR register (in SYSTEM module) from which the DSP will begin execution.

When DSPBOOT = 1, the DSP will boot itself. Under this scenario, DSP will be released from reset without ARM intervention. The DSP boot address is set to an EMIFA address 0x4220 0000h. DSP will begin execution with instruction (L1P) cache enabled.

**Note:** The DSPBOOT operation is overridden when ARM HPI or PCI boot is selected (BTMODE[3:0] = 001x). This is because ARM HPI/PCI boot selection will force the HPIEN or PCIEN bit in PINMUX0 to '1'. This enables UHPI/PCI functions on the EMIFA control and data pins and prevents the DSP from using EMIFA. DSPBOOT is treated as "0" internally when BTMODE[3:0] = 001x, regardless of the value at the configuration pin (The actual pin value should still be latched in the BOOTCFG register of the System Module).

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## 4.6 Configurations After Reset

The following sections provide details on configuring the device after reset.

Multiplexed pin are configured both at and after reset. Section 4.5.1, *Device and Peripheral Configurations at Device Reset*, discusses multiplexed pin control at reset. For more details on multiplexed pins control after reset, see Section 4.7, *Multiplexed Pin Configurations*.

### *4.6.1 Switch Central Resource (SCR) Bus Priorities*

Prioritization within the Switched Central Resource (SCR) is programmable for each master. The register bit fields and default priority levels for DM6467T bus masters are shown in Table 4-14, *DM6467T Default Bus Master Priorities*. The priority levels should be tuned to obtain the best system performance for a particular application. Lower values indicate higher priority. For most masters, their priority values are programmed at the system level by configuring the MSTPRI0, MSTPRI1, and MSTPRI2 registers. Details on the MSTPRI0/1/2 registers are shown in Figure 4-11, Figure 4-12, and Figure 4-13.

**Table 4-14. DM6467T Default Bus Master Priorities**

| Priority Bit Field | Bus Master | Default Priority Level |
|---|---|---|
| VP0P | VPIF Capture | 1 (MSTPRI2 Register) |
| VP1P | VPIF Display | 1 (MSTPRI2 Register) |
| TSIF0P | TSIF0 | 1 (MSTPRI2 Register) |
| TSIF1P | TSIF1 | 1 (MSTPRI2 Register) |
| EDMATC0P | EDMATC0 | 2 (MSTPRI2 Register) |
| EDMATC1P | EDMATC1 | 2 (MSTPRI2 Register) |
| EDMATC2P | EDMATC2 | 2 (MSTPRI2 Register) |
| EDMATC3P | EDMATC3 | 2 (MSTPRI2 Register) |
| HDVICP0P | HDVICP0 (CFG)(1) | 3 (MSTPRI0 Register) |
| HDVICP1P | HDVICP1 (CFG)(1) | 3 (MSTPRI0 Register) |
| ARMINSTP | ARM926 (INST) | 4 (MSTPRI0 Register) |
| ARMDATAP | ARM926 (DATA) | 4 (MSTPRI0 Register) |
| DSPDMAP | C64x+ DSP (DMA) | 4 (MSTPRI0 Register) |
| DSPCFGP | C64x+ DSP (CFG)(1) | 4 (MSTPRI0 Register) |
| VDCEP | VDCE | 4 (MSTPRI1 Register) |
| EMACP | EMAC | 5 (MSTPRI1 Register) |
| USBP | USB2.0 | 5 (MSTPRI1 Register) |
| ATAP | ATA | 5 (MSTPRI1 Register) |
| VLYNQP | VLYNQ | 5 (MSTPRI1 Register) |
| PCIP | PCI | 6 (MSTPRI1 Register) |
| HPIP | HPI | 6 (MSTPRI1 Register) |

(1) The C64x+ DSP (CFG), HDVICP0 (CFG), and HDVICP1 (CFG) priority values are not actually used by the DMSoC infrastructure – which gives equal weight round-robin priority to accesses from these three masters. Therefore, the priority settings for these three masters in the MSTPRI0 register have no effect.


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| 31 | 23 | 22 | 20 | 19 | 18 | 16 |
|---|---|---|---|---|---|---|
| RESERVED | | HDVICP1P(1) | | RSV | HDVICP0P(1) | |
| R-0000 0000 0 | | R/W-011 | | R-0 | R/W-011 | |

| 15 | 14 | 12 | 11 | 8 | 7 | 6 | 4 | 3 | 2 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RSV | DSPDMAP | | RSV | DSPCFGP(1) | RSV | ARMDATAP | | RSV | ARMINSTP | |
| R-0 | R/W-100 | | R-0 | R/W-100 | R-0 | R/W-100 | | R-0 | R/W-100 | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-11. MSTPRI0 Register [0x01C4 003C]**

(1) The DSPCFGP, HDVICP0P, and HDVICP1P priority values are not actually used by the infrastructure, which gives equal weight round-robin priority to accesses from this master; therefore, the settings have no effect.

**Table 4-15. MSTPRI0 Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:23 | RESERVED | Reserved. Read returns "0". |
| 22:20 | HDVICP1P(1) | HDVICP1 master port priority in System Infrastructure. Read returns "011". Writes have no effect. |
| 19 | RSV | Reserved. Read returns "0". |
| 18:16 | HDVICP0P(1) | HDVICP0 master port priority in System Infrastructure. Read returns "011". Writes have no effect. |
| 15 | RSV | Reserved. Read returns "0". |
| 14:12 | DSPDMAP | DSPDMA master port priority in System Infrastructure.<br>000 = Priority 0 (**Highest**) 100 = Priority 4 [**Default**]<br>001 = Priority 1 101 = Priority 5<br>010 = Priority 2 110 = Priority 6<br>011 = Priority 3 111 = Priority 7 (**Lowest**) |
| 11 | RSV | Reserved. Read returns "0". |
| 10:8 | DSPCFGP(1) | DSPCFG master port priority in System Infrastructure. Read returns "100". Writes have no effect. |
| 7 | RSV | Reserved. Read returns "0". |
| 6:4 | ARMDATAP | ARM DATA master port priority in System Infrastructure.<br>000 = Priority 0 (**Highest**) 100 = Priority 4 [**Default**]<br>001 = Priority 1 101 = Priority 5<br>010 = Priority 2 110 = Priority 6<br>011 = Priority 3 111 = Priority 7 (**Lowest**) |
| 3 | RSV | Reserved. Read returns "0". |
| 2:0 | ARMINSTP | ARM INST master port priority in System Infrastructure.<br>000 = Priority 0 (**Highest**) 100 = Priority 4 [**Default**]<br>001 = Priority 1 101 = Priority 5<br>010 = Priority 2 110 = Priority 6<br>011 = Priority 3 111 = Priority 7 (**Lowest**) |

(1) The priorities for these masters are fixed at their default values. Writing alternate values to these fields has no effect..

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| 31 | 30 28 | 27 | 26 24 | 23 | 22 20 | 19 | 18 16 |
|---|---|---|---|---|---|---|---|
| RSV | VDCEP | RSV | PCIP | RSV | HPIP | RSV | VLYNQP |
| R-0 | R/W-100 | R-0 | R/W-110 | R-0 | R/W-110 | R-0 | R/W-101 |

| 15 | 14 12 | 11 | 10 8 | 7 3 | 2 0 |
|---|---|---|---|---|---|
| RSV | ATAP | RSV | USBP | RESERVED | EMACP |
| R-0 | R/W-101 | R-0 | R/W-101 | R-0000 0 | R/W-101 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-12. MSTPRI1 Register [0x01C4 0040]**

**Table 4-16. MSTPRI1 Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31 | RSV | Reserved. Read returns "0". |
| 30:28 | VDCEP | VDCE master port priority in System Infrastructure.<br>000 = Priority 0 (**Highest**)<br>001 = Priority 1<br>010 = Priority 2<br>011 = Priority 3<br>100 = Priority 4 [**Default**]<br>101 = Priority 5<br>110 = Priority 6<br>111 = Priority 7 (**Lowest**) |
| 27 | RSV | Reserved. Read returns "0". |
| 26:24 | PCIP | PCI master port priority in System Infrastructure.<br>000 = Priority 0 (**Highest**)<br>001 = Priority 1<br>010 = Priority 2<br>011 = Priority 3<br>100 = Priority 4<br>101 = Priority 5<br>110 = Priority 6 [**Default**]<br>111 = Priority 7 (**Lowest**) |
| 23 | RSV | Reserved. Read returns "0". |
| 22:20 | HPIP | HPI master port priority in System Infrastructure. Same priority 0–7 selection as above.<br>"110" = Priority 6 [**default**]. |
| 19 | RSV | Reserved. Read returns "0". |
| 18:16 | VLYNQP | VLYNQ master port priority in System Infrastructure. Same priority 0–7 selection as above.<br>"110" = Priority 6 [**default**]. |
| 15 | RSV | Reserved. Read returns "0". |
| 14:12 | ATAP | ATA master port priority in System Infrastructure. Same priority 0–7 selection as above.<br>"101" = Priority 5 [**default**]. |
| 11 | RSV | Reserved. Read returns "0". |
| 10:8 | USBP | USB master port priority in System Infrastructure. Same priority 0–7 selection as above.<br>"101" = Priority 5 [**default**]. |
| 7:3 | RESERVED | Reserved. Read returns "0". |
| 2:0 | EMACP | EMAC master port priority in System Infrastructure. Same priority 0–7 selection as above.<br>"101" = Priority 5 [**default**]. |


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| 31 | 30 28 | 27 | 26 24 | 23 | 22 20 | 19 | 18 16 |
|---|---|---|---|---|---|---|---|
| RSV | TSIF1P | RSV | TSIF0P | RSV | VP1P | RSV | VP0P |
| R-0 | R/W-001 | R-0 | R/W-001 | R-0 | R/W-001 | R-0 | R/W-001 |

| 15 | 14 12 | 11 | 10 8 | 7 | 6 4 | 3 | 2 0 |
|---|---|---|---|---|---|---|---|
| RSV | EDMATC3P | RSV | EDMATC2P | RSV | EDMATC1P | RSV | EDMATC0P |
| R-0 | R/W-010 | R-0 | R/W-010 | R-0 | R/W-010 | R-0 | R/W-010 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-13. MSTPRI2 Register**

**Table 4-17. MSTPRI2 Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31 | RSV | Reserved. Read returns "0". |
| 30:28 | TSIF1P | TSIF1 master port priority in System Infrastructure.<br>000 = Priority 0 (**Highest**) 100 = Priority 4<br>001 = Priority 1 [**Default**] 101 = Priority 5<br>010 = Priority 2 110 = Priority 6<br>011 = Priority 3 111 = Priority 7 (**Lowest**) |
| 27 | RSV | Reserved. Read returns "0". |
| 26:24 | TSIF0P | TSIF0 master port priority in System Infrastructure.<br>000 = Priority 0 (**Highest**) 100 = Priority 4<br>001 = Priority 1 [**Default**] 101 = Priority 5<br>010 = Priority 2 110 = Priority 6<br>011 = Priority 3 111 = Priority 7 (**Lowest**) |
| 23 | RSV | Reserved. Read returns "0". |
| 22:20 | VP1P | VPIF display master port priority in System Infrastructure. Same priority 0–7 selection as above. "001" = Priority 1 [**default**]. |
| 19 | RSV | Reserved. Read returns "0". |
| 18:16 | VP0P | VPIF capture master port priority in System Infrastructure. Same priority 0–7 selection as above. "001" = Priority 1 [**default**]. |
| 15 | RSV | Reserved. Read returns "0". |
| 14:12 | EDMATC3P | EDMATC3 master port priority in System Infrastructure. Same priority 0–7 selection as above. "010" = Priority 2 [**default**]. |
| 11 | RSV | Reserved. Read returns "0". |
| 10:8 | EDMATC2P | EDMATC2 master port priority in System Infrastructure. Same priority 0–7 selection as above. "010" = Priority 2 [**default**]. |
| 7 | RSV | Reserved. Read returns "0". |
| 6:4 | EDMATC1P | EDMATC1 master port priority in System Infrastructure. Same priority 0–7 selection as above. "010" = Priority 2 [**default**]. |
| 3 | RSV | Reserved. Read returns "0". |
| 2:0 | EDMATC0P | EDMATC0 master port priority in System Infrastructure. Same priority 0–7 selection as above. "010" = Priority 2 [**default**]. |

### *4.6.2 Peripheral Selection After Device Reset*

After device reset, most peripheral configurations are done within the peripheral's registers. This section discusses some additional peripheral controls in the System Module. For information on multiplexed pin controls that determine what peripheral pins are brought out to the pins, see Section 4.7, *Multiplexed Pin Configurations*.

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### 4.6.2.1 HPICTL Register

The HPI control register (HPICTL) [0x01C4 0030] controls write access to HPI control and address registers and determines the host time-out value. HPICTL is not reset by a soft reset so that the HPI width will remain correctly configured. Figure 4-14 and Table 4-18 describe in detail the HPICTL register.

| 31 | 18 | 17 | 16 |
|---|---|---|---|
| RESERVED | | RESERVED | |
| R-0000 0000 0000 00 | | R/W-00 | |

| 15 | 14 | 10 | 9 | 8 | 7 | 0 |
|---|---|---|---|---|---|---|
| WIDTH | RESERVED | | CTLMODE | ADDMODE | TIMOUT | |
| R/W-0 | R-000 00 | | R/W-0 | R/W-0 | R/W-1000 0000 | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-14. HPICTL Register [0x01C4 0030]**

**Table 4-18. HPICTL Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:18 | RESERVED | Reserved. Read-only, writes have no effect. |
| 17:16 | RESERVED | Reserved. For proper device operation, the user should *only* write "0" to these bits (default). |
| 15 | WIDTH | HPI Data Width.<br>0 = Half-width (16-bit) data bus<br>1 = Full-width (32-bit) data bus<br>This bit value must be determined before releasing the UHPI from reset to ensure correct UHPI operation. |
| 14:10 | RESERVED | Reserved. Read-only, writes have no effect. |
| 9 | CTLMODE | HPIC Register Write Access.<br>0 = Host<br>1 = DMSoC (if ADDMODE = 1) |
| 8 | ADDMODE | HPIA Register Write Access.<br>0 = Host<br>1 = DMSoC |
| 7:0 | TIMOUT | Host Burst Write Timeout Value.<br>When the HPI time-out counter reaches the value programmed here, the HPI write FIFO content is flushed. For more details on the time-out counter and its use in write bursting, see the *TMS320DM646x DMSoC Host Port Interface (HPI)* User's Guide (literature number SPRUES1). |

### 4.6.2.2 USBCTL Register

The USB interface control register (USBCTL) [0x01C4 0034] is described in Figure 4-15 and Table 4-19.

| 31 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|
| RESERVED | | DATAPOL | VBUSVAL | USBID |
| R-0000 0000 0000 0 | | R/W-1 | R/W-0 | R/W-0 |

| 15 | 9 | 8 | 7 | 5 | 4 | 3 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESERVED | | PHY CLKGD | RESERVED | | PHY PLLON | RESERVED | | PHY PDWN |
| R-0000 000 | | R-0 | R-000 | | R/W-0 | R-000 | | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-15. USBCTL Register [0x01C4 0034]**


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**Table 4-19. USBCTL Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:19 | RESERVED | Reserved. Read returns "0". |
| 18 | DATAPOL | USB Data Polarity.<br>0 = Inverted data.<br>1 = Normal data polarity [default]. |
| 17 | VBUSVAL | VBUS Sense Control.<br>0 = Disabled [default].<br>1 = Session starts. |
| 16 | USBID | USB Mode.<br>0 = Host [default].<br>1 = Peripheral. |
| 15:9 | RESERVED | Reserved. Read returns "0". |
| 8 | PHYCLKGD | USB PHY Power and Clock Good.<br>0 = PHY power is not ramped or PLL is not locked [default].<br>1 = PHY power is good and PLL is locked. |
| 7:5 | RESERVED | Reserved. Read returns "0". |
| 4 | PHYPLLON | USB PHY PLL Suspend Override.<br>0 = Normal PLL operation [default].<br>1 = Override PLL suspend state. |
| 3:1 | RESERVED | Reserved. Read returns "0". |
| 0 | PHYPDWN | USB PHY Power-Down Control.<br>0 = PHY powered on.<br>1 = PHY power off [default]. |

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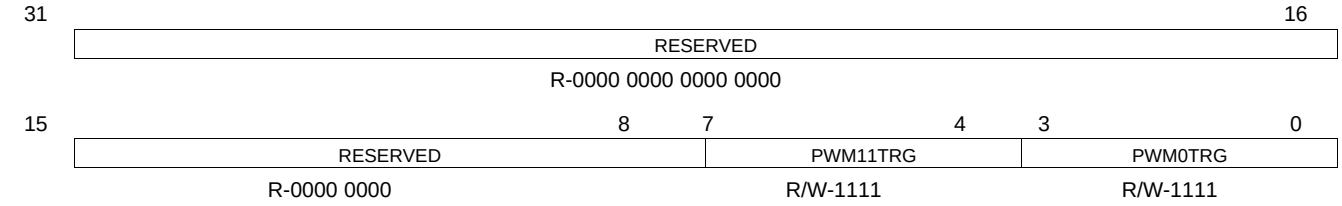
#### 4.6.2.3 PWMCTL (Trigger Source) Control Register

The PWM control register (PWMCTL) [0x01C4 0054] chip-level connections of both PWM0 and PWM1. Figure 4-16 and Table 4-20 describe in detail the PWMCTL register.




LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-16. PWMCTL Register [0x01C4 0054]**

**Table 4-20. PWMCTL Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:8 | RESERVED | Reserved. Read-only, writes have no effect. |
| 7:4 | PWM1TRG | PWM1 Trigger Source<br>0000 = GP[0] 1000 = VPIF Vertical Interrupt 0<br>0001 = GP[1] 1001 = VPIF Vertical Interrupt 1<br>0010 = GP[2] 1010 = VPIF Vertical Interrupt 2<br>0011 = GP[3] 1011 = VPIF Vertical Interrupt 3<br>0100 = GP[4] 1100 = Reserved<br>0101 = GP[5] 1101 = Reserved<br>0110 = GP[6] 1110 = Reserved<br>0111 = GP[7] 1111 = Reserved |
| 3:0 | PWM0TRG | PWM0 Trigger Source<br>same selection as above. |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### 4.6.2.4 EDMATCCFG Register

The EDMA Transfer Controller Default Burst Size Configuration Register (EDMATCCFG) [0x01C4 0058] configures the default burst size (DBS) for EDMA TC0, EDMA TC1, EDMA TC2, and EDMA TC3. Figure 4-17 and Table 4-21 describe in detail the EDMATCCFG register. For more information on the correct usage of DBS, see the *TMS320DM646x DMSoC Enhanced Direct Memory Access (EDMA) Controller* User's Guide (literature number SPRUEQ5).

| 31 | 16 |
|---|---|
| RESERVED | |
| R-0000 0000 0000 0000 | |

| 15 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | TC3DBS | | TC2DBS | | TC1DBS | | TC0DBS | |
| R-0000 0000 | | R/W-01 | | R/W-01 | | R/W-01 | | R/W-01 | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-17. EDMA Transfer Controller Default Burst Size Configuration Register (EDMATCCFG) [0x01C4 0058]**

**Table 4-21. EDMATCCFG Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:8 | RESERVED | Reserved. Read-only, writes have no effect. |
| 7:6 | TC3DBS | EDMA TC3 Default Burst Size.<br>00 = 16 byte<br>01 = 32 byte [default]<br>10 = 64 byte<br>11 = reserved<br>TC3 FIFO size is 256 bytes, regardless of Default Burst Size setting. |
| 5:4 | TC2DBS | EDMA TC2 Default Burst Size.<br>00 = 16 byte<br>01 = 32 byte [default]<br>10 = 64 byte<br>11 = reserved<br>TC2 FIFO size is 256 bytes, regardless of Default Burst Size setting. |
| 3:2 | TC1DBS | EDMA TC1 Default Burst Size.<br>00 = 16 byte<br>01 = 32 byte [default]<br>10 = 64 byte<br>11 = reserved<br>TC1 FIFO size is 256 bytes, regardless of Default Burst Size setting. |
| 1:0 | TC0DBS | EDMA TC0 Default Burst Size.<br>00 = 16 byte<br>01 = 32 byte [default]<br>10 = 64 byte<br>11 = reserved<br>TC0 FIFO size is 256 bytes, regardless of Default Burst Size setting. |

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## 4.7 Multiplexed Pin Configurations

DM6467T makes extensive use of pin multiplexing to accommodate a large number of peripheral function in the smallest possible package, providing the ultimate flexibility for end applications.

The Pin Multiplex Registers PINMUX0 and PINMUX1 in the System Module are responsiblie for controlling all pin multiplexing functions on the DM6467T. The default setting of some of the PINMUX0 and PINMUX1 bit fields are configured by configuration pins latched at reset (see Section 4.5.1, *Device and Peripheral Configurations at Device Reset*). After reset, software may program the PINMUX0 and PINMUX1 registers to switch pin functionalities.

The following peripherals have multiplexed pins: VPIF, TSIF0, TSIF1, CRGEN0, CRGEN1, EMIFA, PCI, HPI, ATA, PWM0, PWM1, UART0, UART1, UART2, Audio Clock Selector, the USB USB_DRVVBUS pin, and GPIO.

### *4.7.1 Pin Muxing Selection At Reset*

This section summarizes pin mux selection at reset.

The configuration pins CS2BW and PCIEN, latched at device reset, determine the default pin muxing. For more details on the default pin muxing at reset, see Section 4.5, *Configurations At Reset*.

### *4.7.2 Pin Muxing Selection After Reset*

The PINMUX0 and PINMUX1 registers in the System Module allow software to select the pin functions. Some pin functions require a combination of PINMUX0/PINMUX1 bit fields. For more details on the combination of the PINMUX bit fields that control each muxed pin, see Section 4.7.3, *Pin Multiplexing Details*.

This section only provides an overview of the PINMUX0 and PINMUX1 registers. For more detailed discussion on how to program each Pin Mux Block, see Section 4.7.3, *Pin Multiplexing Details*.

#### 4.7.2.1 PINMUX0 Register Description

The Pin Multiplexing 0 Register controls the pin function in the EMIFA/ATA/HPI/PCI, TSIF0, TSIF1, CRGEN, Block. The PINMUX0 register format is shown in Figure 4-18 and the bit field descriptions are given in Table 4-22. Some muxed pins are controlled by more than one PINMUX bit field. For the combination of the PINMUX bit fields that control each muxed pin, see Section 4.7.3, *Pin Multiplexing Details*. For more information on the block pin muxing and pin-by-pin muxing control, see specific block muxing section (for example, for CRGEN Pin Mux Control, see Section 4.7.3.7, *CRGEN Signal Muxing*).

| 31 | 30 | 29 | 28 | 27 | 26 24 | 23 22 | 21 20 | 19 18 | 17 16 |
|---|---|---|---|---|---|---|---|---|---|
| VBUSDIS | STCCK | AUDCK1 | AUDCK0 | RSV | CRGMUX | TSSOMUX | TSSIMUX | TSPOMUX | TSPIMUX |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R/W-000 | R/W-00 | R/W-00 | R/W-00 | R/W-00 |

| 15 6 | 5 | 4 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|
| RESERVED | RSV | RESERVED | PCIEN | HPIEN | ATAEN |
| R-0000 0000 00 | R/W-0 | R-0 | R/W-L | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-18. PINMUX0 Register [0x01C4 0000]**


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**Table 4-22. PINMUX0 Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31 | VBUSDIS | This bit disables USB_DRVVBUS output.<br>0 = USB_DRVVBUS function selected.<br>1 = GP[22] function selected. |
| 30 | STCCK | This bit enables STC Source Clock input.<br>0 = GP[4] function selected.<br>1 = STC_CLKIN function selected. |
| 29 | AUDCK1 | This bit enables AUDIO_CLK1 output.<br>0 = GP[2] function selected.<br>1 = AUDIO_CLK1 function selected. |
| 28 | AUDCK0 | This bit enables AUDIO_CLK0 output.<br>0 = GP[3] function selected.<br>1 = AUDIO_CLK0 function selected. |
| 27 | RSV | Reserved. Read returns "0". |
| 26:24 | CRGMUX | CRGEN Pin Mux Control (see Section 4.7.3.7, *CRGEN Signal Muxing*).<br>000 = No CRGEN signals enabled.<br>001 = CRGEN1 selection enabled (muxed with UART2 data).<br>010 = Reserved (no CRGEN signals enabled).<br>011 = Reserved (no CRGEN signals enabled).<br>100 = CRGEN0 selection enabled (muxed with UCTS2 and PWM0).<br>101 = CRGEN0 and CRGEN1 selection enabled.<br>110 = CRGEN0 selection enabled (muxed with UART2 data).<br>111 = Reserved (no CRGEN signals enabled). |
| 23:22 | TSSOMUX | TSIF1 Serial Output Pin Mux Control (see (1), *TSSO Signal Muxing*).<br>0x = No TS1 output signals enabled.<br>10 = TS1 output selection enabled (muxed on VP_DOUT pins).<br>11 = TS1 output selection enabled (muxed on URIN0, UCTS2, PWM0, and PWM1 pins). |
| 21:20 | TSSIMUX | TSIF1 Serial Input Pin Mux Control (see Section 4.7.3.5, *TSIF1 Input Signal Muxing*).<br>00 = No TS1 input signals enabled.<br>01 = TS1 input selection enabled (muxed on UART0 pins).<br>10 = TS1 input selection enabled (muxed on VP_DOUT pins).<br>11 = TS1 input selection enabled (muxed on VP_DIN pins). |
| 19:18 | TSPOMUX | TSIF0 Parallel/Serial Output Pin Mux Control (see Section 4.7.3.4, *TSIF0 Output Signal Muxing*).<br>0x = No TS0 output signals enabled.<br>10 = TS0 parallel output muxing enabled (muxed with VP_DIN pins).<br>11 = TS0 serial output muxing enabled (muxed TS0_DOUT7 with UTXD1). |
| 17:16 | TSPIMUX | TSIF0 Parallel/Serial Input Pin Mux Control (see Section 4.7.3.3, *TSIF0 Input Signal Muxing*).<br>0x = No TS0 signals enabled.<br>10 = TS0 parallel input muxing enabled (muxed with VP_DIN pins).<br>11 = TS0 serial input muxing enabled (muxed TS0_DIN7 with URXD1). |
| 15:6 | RESERVED | Reserved. Read returns "0". |
| 5 | RESERVED | Reserved. Read returns "0". **Note:** For proper device operation, when writing to this bit, only a "0" should be written. |
| 4:3 | RESERVED | Reserved. Read returns "0". |
| 2 | PCIEN | PCI Function Enable (see Section 4.7.3.1, *PCI, HPI, EMIFA and ATA Pin Muxing*).<br>Default value is determined by PCIEN boot configuration pin. |
| 1 | HPIEN | HPI Function Enable (see Section 4.7.3.1, *PCI, HPI, EMIFA and ATA Pin Muxing*). |
| 0 | ATAEN | ATA Function Enable (see Section 4.7.3.1, *PCI, HPI, EMIFA and ATA Pin Muxing*). |

(1) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 4.8.1, *Pullup/Pulldown Resistors*.

### 4.7.2.2 PINMUX1 Register Description

The Pin Multiplexing 1 Register controls the pin function in the UART0, UART1, and UART2 Blocks. The PINMUX1 register format is shown in Figure 4-19 and the bit field descriptions are given in Table 4-23. Some muxed pins are controlled by more than one PINMUX bit field. For the combination of the PINMUX bit fields that control each muxed pin, see Section 4.7.3, *Pin Multiplexing Details*. For the pin-by-pin muxing control of the UART0, UART1, and UART2 Blocks, see Section 4.7.3.8, *UART0 Pin Muxing*; Section 4.7.3.9, *UART1 Pin Muxing*; and Section 4.7.3.10, *UART2 Pin Muxing*.

| 31 | 16 |
|---|---|
| RESERVED | |
| R-0000 0000 0000 0000 | |

| 15 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | UART2CTL | | UART1CTL | | UART0CTL | |
| R-0000 0000 00 | | R/W-00 | | R/W-00 | | R/W-00 | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-19. PINMUX1 Register**

**Table 4-23. PINMUX1 Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:6 | RESERVED | Reserved. Read returns "0". |
| 5:4 | UART2CTL | UART2 Pin Configuration (see Section 4.7.3.10, *UART2 Pin Muxing*).<br>00 = UART function with flow control.<br>01 = UART function without flow control.<br>10 = IrDA/CIR function.<br>11 = GPIO function.<br>(Individual pin functions may be overridden by TSPIMUX, CRGEN0, and CRGEN1 values.) |
| 3:2 | UART1CTL | UART1 Pin Configuration (see Section 4.7.3.9, *UART1 Pin Muxing*).<br>00 = UART function with flow control.<br>01 = UART function without flow control.<br>10 = IrDA/CIR function.<br>11 = GPIO function.<br>(Individual pin functions may be overridden by TSPIMUX and TSPOMUX values.) |
| 1:0 | UART0CTL | UART0 Pin Configuration (see Section 4.7.3.8, *UART0 Pin Muxing*).<br>00 = UART function with modem control.<br>01 = UART function without modem control.<br>1x = IrDA/CIR function.<br>(Individual pin functions may be overridden by TSPOMUX value.) |


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### 4.7.3 Pin Multiplexing Details

This section discusses how to program each Pin Mux Register to select the desired peripheral functions and pin muxing. See the individual pin mux sections for pin muxing details for a specific muxed pin.

For details on PINMUX0 and PINMUX1 registers, see Section 4.7.2, *Pin Muxing Selection After Reset*.

#### 4.7.3.1 PCI, HPI, EMIFA, and ATA Pin Muxing

The PCI, HPI, EMIFA, and ATA signal muxing is determined by the value of the PCIEN, HPIEN, and ATAEN bit fields in the PINMUX0 register. For more details on the actual pin functions, see Table 4-24 and Table 4-25.

**Table 4-24. PCIEN, HPIEN, and ATAEN Encoding**

| PCIEN | HPIEN | ATAEN | PIN FUNCTIONS |
|---|---|---|---|
| 0 | 0 | 0 | EMIFA |
| 0 | 0 | 1 | EMIFA (NAND) and ATA |
| 0 | 1 | 0 | HPI (32-bit) |
| 0 | 1 | 1 | HPI (16-bit) and ATA |
| 1 | x | x | PCI(1) |

(1) In PCI mode (PCIEN = 1), the internal pullups/pulldowns (IPUs/IPDs) are disabled on all PCI pins and it is recommended to have external pullup resistors on the PCI_RSV[5:0] pins. See Table 4-25 for the actual PCI pin functions and any associated footnotes.

**Table 4-25. PCI, HPI, EMIFA, and ATA Pin Muxing**

| PIN FUNCTIONS (WITH PCIEN, HPIEN, ATAEN VALUES) | | | | |
|---|---|---|---|---|
| 1xx(1) | 010 | 011 | 000 | 001 |
| PCI_CLK | GP[10] | GP[10] | GP[10] | GP[10] |
| PCI_IDSEL | – | HDDIR | EM_R/$\overline{W}$ | HDDIR |
| $\overline{\text{PCI_DEVSEL}}$ | HCNTL1 | HCNTL1 | EM_BA[1] | EM_BA[1] |
| $\overline{\text{PCI_FRAME}}$ | $\overline{\text{HINT}}$ | $\overline{\text{HINT}}$ | EM_BA[0] | EM_BA[0] |
| $\overline{\text{PCI_IRDY}}$ | $\overline{\text{HRDY}}$ | $\overline{\text{HRDY}}$ | EM_A[17] | EM_A[17]/(CLE) |
| $\overline{\text{PCI_TRDY}}$ | HHWIL | HHWIL | EM_A[16] | EM_A[16]/(ALE) |
| $\overline{\text{PCI_STOP}}$ | HCNTL0 | HCNTL0 | $\overline{\text{EM_WE}}$ | $\overline{\text{EM_WE}}$ |
| $\overline{\text{PCI_SERR}}$ | $\overline{\text{HDS1}}$ | $\overline{\text{HDS1}}$ | $\overline{\text{EM_OE}}$ | $\overline{\text{EM_OE}}$ |
| $\overline{\text{PCI_PERR}}$ | $\overline{\text{HCS}}$ | $\overline{\text{HCS}}$ | $\overline{\text{EM_DQM1}}$ | $\overline{\text{EM_DQM1}}$ |
| PCI_PAR | $\overline{\text{HAS}}$ | $\overline{\text{HAS}}$ | $\overline{\text{EM_DQM0}}$ | $\overline{\text{EM_DQM0}}$ |
| $\overline{\text{PCI_INTA}}$ | – | – | EM_WAIT2 | EM_WAIT2/(RDY2/$\overline{\text{BSY2}}$) |
| $\overline{\text{PCI_REQ}}$ | GP[11] | DMARQ | $\overline{\text{EM_CS5}}$ | DMARQ |
| $\overline{\text{PCI_GNT}}$ | GP[12] | $\overline{\text{DACK}}$ | $\overline{\text{EM_CS4}}$ | $\overline{\text{DACK}}$ |
| $\overline{\text{PCI_CBE3}}$ | HR/$\overline{W}$ | HR/$\overline{W}$ | $\overline{\text{EM_CS3}}$ | $\overline{\text{EM_CS3}}$ |
| $\overline{\text{PCI_CBE2}}$ | $\overline{\text{HDS2}}$ | $\overline{\text{HDS2}}$ | $\overline{\text{EM_CS2}}$ | $\overline{\text{EM_CS2}}$ |
| $\overline{\text{PCI_CBE1}}$ | GP[32] | $\overline{\text{ATA_CS1}}$ | EM_A[19] | $\overline{\text{ATA_CS1}}$ |
| $\overline{\text{PCI_CBE0}}$ | GP[33] | $\overline{\text{ATA_CS0}}$ | EM_A[18] | $\overline{\text{ATA_CS0}}$ |
| PCI_AD31 | HD31 | DD15 | EM_A[15] | DD15 |
| PCI_AD30 | HD30 | DD14 | EM_A[14] | DD14 |
| PCI_AD29 | HD29 | DD13 | EM_A[13] | DD13 |
| PCI_AD28 | HD28 | DD12 | EM_A[12] | DD12 |
| PCI_AD27 | HD27 | DD11 | EM_A[11] | DD11 |

(1) In PCI mode (PCIEN = 1), the internal pullups/pulldowns (IPUs/IPDs) are disabled on all PCI pins and it is recommended to have external pullup resistors on the PCI_RSV[5:0] pins. For more detailed information on external pullup/pulldown resistors, see Section 4.8.1, *Pullup/Pulldown Resistors*.

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**Table 4-25. PCI, HPI, EMIFA, and ATA Pin Muxing (continued)**

| PIN FUNCTIONS (WITH PCIEN, HPIEN, ATAEN VALUES) | | | | |
|---|---|---|---|---|
| **1xx**(1) | **010** | **011** | **000** | **001** |
| PCI_AD26 | HD26 | DD10 | EM_A[10] | DD10 |
| PCI_AD25 | HD25 | DD9 | EM_A[9] | DD9 |
| PCI_AD24 | HD24 | DD8 | EM_A[8] | DD8 |
| PCI_AD23 | HD23 | DD7 | EM_A[7] | DD7 |
| PCI_AD22 | HD22 | DD6 | EM_A[6] | DD6 |
| PCI_AD21 | HD21 | DD5 | EM_A[5] | DD5 |
| PCI_AD20 | HD20 | DD4 | EM_A[4] | DD4 |
| PCI_AD19 | HD19 | DD3 | EM_A[3] | DD3 |
| PCI_AD18 | HD18 | DD2 | EM_A[2] | DD2 |
| PCI_AD17 | HD17 | DD1 | EM_A[1] | DD1 |
| PCI_AD16 | HD16 | DD0 | EM_A[0] | DD0 |
| PCI_AD15 | HD15 | HD15 | EM_D15 | EM_D15 |
| PCI_AD14 | HD14 | HD14 | EM_D14 | EM_D14 |
| PCI_AD13 | HD13 | HD13 | EM_D13 | EM_D13 |
| PCI_AD12 | HD12 | HD12 | EM_D12 | EM_D12 |
| PCI_AD11 | HD11 | HD11 | EM_D11 | EM_D11 |
| PCI_AD10 | HD10 | HD10 | EM_D10 | EM_D10 |
| PCI_AD9 | HD9 | HD9 | EM_D9 | EM_D9 |
| PCI_AD8 | HD8 | HD8 | EM_D8 | EM_D8 |
| PCI_AD7 | HD7 | HD7 | EM_D7 | EM_D7 |
| PCI_AD6 | HD6 | HD6 | EM_D6 | EM_D6 |
| PCI_AD5 | HD5 | HD5 | EM_D5 | EM_D5 |
| PCI_AD4 | HD4 | HD4 | EM_D4 | EM_D4 |
| PCI_AD3 | HD3 | HD3 | EM_D3 | EM_D3 |
| PCI_AD2 | HD2 | HD2 | EM_D2 | EM_D2 |
| PCI_AD1 | HD1 | HD1 | EM_D1 | EM_D1 |
| PCI_AD0 | HD0 | HD0 | EM_D0 | EM_D0 |
| $\overline{\text{PCI_RST}}$ | GP[13] | DA2 | EM_A[22] | DA2 |
| PCI_RSV0(2) | GP[16] | DA1 | EM_A[21] | DA1 |
| PCI_RSV1(2) | GP[17] | DA0 | EM_A[20] | DA0 |
| PCI_RSV2(2) | GP[18] | INTRQ | EM_RSV0 | INTRQ |
| PCI_RSV3(2) | GP[19] | $\overline{\text{DIOR}}$ | EM_WAIT5/(RDY5/$\overline{\text{BSY5}}$) | $\overline{\text{DIOR}}$ |
| PCI_RSV4(2) | GP[20] | $\overline{\text{DIOW}}$ | EM_WAIT4/(RDY4/$\overline{\text{BSY4}}$) | $\overline{\text{DIOW}}$ |
| PCI_RSV5(2) | GP[21] | IORDY | EM_WAIT3/(RDY3/$\overline{\text{BSY3}}$) | IORDY |

(2) In PCI mode (PCIEN = 1), the internal pullups/pulldowns (IPUs/IPDs) are disabled on all PCI pins and it is recommended to have external pullup resistors on the PCI_RSV[5:0] pins. For more detailed information on external pullup/pulldown resistors, see Section 4.8.1, *Pullup/Pulldown Resistors*.


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#### 4.7.3.2 PWM Signal Muxing

The two PWM outputs will be configured as PWM pin functions by default. The PWM functions may be overridden by the settings of various PINMUX0 bit fields as shown in Table 4-26 and Table 4-27.

**Table 4-26. PWM0 Pin Muxing**

| PIN FUNCTION | | |
|---|---|---|
| **CRGMUX ≠ 10x<br>TSSOMUX ≠ 11** | **CRGMUX = 10x<br>TSSOMUX ≠ 11** | **TSSOMUX = 11** |
| PWM0 | CRG0_PO | TS1_ENAO |

**Table 4-27. PWM1 Pin Muxing**

| PIN FUNCTION | |
|---|---|
| **TSSOMUX ≠ 11** | **TSSOMUX = 11** |
| PWM1 | TS1_DOUT |

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#### 4.7.3.3 TSIF0 Input Signal Muxing (Serial/Parallel)

The TSIF 0 (TS0) input signals have muxing options for both parallel or serial operation as configured by the TPSIMUX bits as shown in Table 4-28.

**Table 4-28. TSIF0 Input Pin Muxing**

| TSPIMUX = 0x (NO TSIF0 SIGNALS ENABLED) | TSPIMUX = 10 (PARALLEL) | TSPIMUX = 11 (SERIAL) |
|---|---|---|
| TS0_CLKIN | TS0_CLKIN | TS0_CLKIN |
| VP_DIN15_VSYNC | TS0_DIN7 | VP_DIN15_VSYNC |
| VP_DIN14_HSYNC | TS0_DIN6 | VP_DIN14_HSYNC |
| VP_DIN13_FIELD | TS0_DIN5 | VP_DIN13_FIELD |
| VP_DIN12 | TS0_DIN4 | VP_DIN12 |
| VP_DIN11 | TS0_DIN3 | VP_DIN11 |
| VP_DIN10 | TS0_DIN2 | VP_DIN10 |
| VP_DIN9 | TS0_DIN1 | VP_DIN9 |
| VP_DIN8 | TS0_DIN0 | VP_DIN8 |
| URXD1 (1) | URXD1 (1) | TS0_DIN7 |
| UTXD1 (1) | UTXD1 (1) | (see Table 4-22—TSPOMUX bit field) (also see Table 4-35) |
| $\overline{\text{URTS1}}$ (1) | TS0_WAITO | TS0_WAITO |
| $\overline{\text{UCTS1}}$ (1) | TS0_EN_WAITO | TS0_EN_WAITO |
| $\overline{\text{URTS2}}$ (2) | TS0_PSTIN | TS0_PSTIN |

(1) Function is determined by UART1CTL bit field value in the PINMUX0 register.
(2) Function is determined by UART2CTL bit field value in the PINMUX0 register.


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#### 4.7.3.4 TSIF0 Output Signal Muxing (Serial/Parallel)

The TSIF 0 (TS0) output signals have muxing options for both parallel or serial operation as configured by the TPSOMUX bits as shown in Table 4-29.

**Table 4-29. TSIF0 Output Pin Muxing**

| TSPOMUX = 0x | | TSPOMUX = 10 (PARALLEL) | TSPOMUX = 11 (SERIAL) |
|---|---|---|---|
| UART0CTL = 00 | UART0CTL ≠ 00 | | |
| VP_CLKO3 | VP_CLKO3 | TS0_CLKO | TS0_CLKO |
| VP_DIN7(1) | VP_DIN7(1) | TS0_DOUT7(1) | VP_DIN7(1) |
| VP_DIN6(1) | VP_DIN6(1) | TS0_DOUT6(1) | VP_DIN6(1) |
| VP_DIN5(1) | VP_DIN5(1) | TS0_DOUT5(1) | VP_DIN5(1) |
| VP_DIN4(1) | VP_DIN4(1) | TS0_DOUT4(1) | VP_DIN4(1) |
| VP_DIN3(1) | VP_DIN3(1) | TS0_DOUT3(1) | VP_DIN3(1) |
| VP_DIN2(1) | VP_DIN2(1) | TS0_DOUT2(1) | VP_DIN2(1) |
| VP_DIN1(1) | VP_DIN1(1) | TS0_DOUT1(1) | VP_DIN1(1) |
| VP_DIN0(1) | VP_DIN0(1) | TS0_DOUT0(1) | VP_DIN0(1) |
| $\overline{\text{UDTR0}}$ | GP[36] | TS0_ENAO | TS0_ENAO |
| $\overline{\text{UDSR0}}$ | GP[37] | TS0_PSTO | TS0_PSTO |
| $\overline{\text{UDCD0}}$ | GP[38] | TS0_WAITIN | TS0_WAITIN |
| URIN0 | GP[8] | GP[8] | GP[8] |
| URXD1(2) | URXD1(2) | URXD1(2) | (see Table 4-22—TSPIMUX bit field) (also see Table 4-35) |
| UTXD1(2) | UTXD1(2) | UTXD1(2) | TS0_DOUT7 |

(1) Function will be overridden by TSIF1 signals if TSSIMUX = 11 (PINMUX0 register).
(2) Function is determined by UART1CTL bit field value in the PINMUX1 register.

#### 4.7.3.5 TSIF1 Input Signal Muxing (Serial Only)

The TSIF 1 (TS1) input signals have three muxing options as configured by the TSSIMUX bits as shown in Table 4-30. When TSSIMUX = 11, the TSSI data and control pins are muxed onto the VP_DIN[7:4] regardless of the value of TSPOMUX.

**Table 4-30. TSIF1 Serial Input Pin Muxing**

| TSSIMUX = 00 | TSSIMUX = 01 | TSSIMUX = 10 | TSSIMUX = 11 |
|---|---|---|---|
| TS1_CLKIN | TS1_CLKIN | TS1_CLKIN | TS1_CLKIN |
| VP_DIN7/TS0_DOUT7 (1) | VP_DIN7/TS0_DOUT7 (1) | VP_DIN7/TS0_DOUT7 (1) | TS1_DIN |
| VP_DIN6/TS0_DOUT6 (1) | VP_DIN6/TS0_DOUT6 (1) | VP_DIN6/TS0_DOUT6 (1) | TS1_PSTIN |
| VP_DIN5/TS0_DOUT5 (1) | VP_DIN5/TS0_DOUT5 (1) | VP_DIN5/TS0_DOUT5 (1) | TS1_EN_WAITO |
| VP_DIN4/TS0_DOUT4 (1) | VP_DIN4/TS0_DOUT4 (1) | VP_DIN4/TS0_DOUT4 (1) | TS1_WAITO |
| VP_DIN3/TS0_DOUT3 (1) | VP_DIN3/TS0_DOUT3 (1) | VP_DIN3/TS0_DOUT3 (1) | Hi-Z |
| VP_DIN2/TS0_DOUT2 (1) | VP_DIN2/TS0_DOUT2 (1) | VP_DIN2/TS0_DOUT2 (1) | Hi-Z |
| VP_DIN1/TS0_DOUT1 (1) | VP_DIN1/TS0_DOUT1 (1) | VP_DIN1/TS0_DOUT1 (1) | Hi-Z |
| VP_DIN0/TS0_DOUT0 (1) | VP_DIN0/TS0_DOUT0 (1) | VP_DIN0/TS0_DOUT0 (1) | Hi-Z |
| VP_DOUT15 | VP_DOUT15 | TS1_DIN | VP_DOUT15 |
| VP_DOUT14 | VP_DOUT14 | TS1_PSTIN | VP_DOUT14 |
| VP_DOUT13 | VP_DOUT13 | TS1_EN_WAITO | VP_DOUT13 |
| VP_DOUT12 | VP_DOUT12 | TS1_WAITO | VP_DOUT12 |
| URXD0 (2) | TS1_DIN | URXD0 (2) | URXD0 (2) |
| UTXD0 (2) | TS1_PSTIN | UTXD0 (2) | UTXD0 (2) |
| $\overline{\text{URTS0}}$ (2) | TS1_EN_WAITO | $\overline{\text{URTS0}}$ (2) | $\overline{\text{URTS0}}$ (2) |
| $\overline{\text{UCTS0}}$ (2) | USD0 | $\overline{\text{UCTS0}}$ (2) | $\overline{\text{UCTS0}}$ (2) |

(1) Function will be determined by TSPOMUX bit field value in the PINMUX0 register.
(2) Function is determined by UART0CTL bit field value in the PINMUX1 register


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#### 4.7.3.6 TSIF1 Output Signal Muxing (Serial Only)

The TSIF 1 (TS1) output signals are muxed with either the VP_DOUT signals or UART0, UART2, and PWM signals as selected by TSSOMUX (PINMUX0 register). The TS1 output pin muxing is shown in Table 4-31.

**Table 4-31. TSIF1 Serial Output Pin Muxing**

| PIN FUNCTION | | |
|---|---|---|
| **TSSOMUX = 0x** | **TSSOMUX = 10** | **TSSOMUX = 11** |
| VP_CLKIN3 | TS1_CLKO | TS1_CLKO |
| VP_DOUT11 | TS1_DOUT | VP_DOUT11 |
| VP_DOUT10 | TS1_PSTO | VP_DOUT10 |
| VP_DOUT9 | TS1_ENAO | VP_DOUT9 |
| VP_DOUT8 | TS1_WAITIN | VP_DOUT8 |
| URIN0/GP[8](1) | URIN0/GP[8](1) | TS1_WAITIN |
| $\overline{\text{UCTS2}}$/GP[42]/CRG0_VCXI(2) | $\overline{\text{UCTS2}}$/GP[42]/CRG0_VCXI(2) | TS1_PSTO |
| PWM0/CRG0_PO(3) | PWM0/CRG0_PO(3) | TS1_ENAO |
| PWM1 | PWM1 | TS1_DOUT |

(1) Function will be determined by UART0CTL bit field value in the PINMUX1 register.
(2) Function will be determined by UART2CTL and CRGMUX bit field values in the PINMUX1 and PINMUX0 registers, respectively.
(3) Function will be determined by CRGMUX bit field value in the PINMUX0 register.

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#### 4.7.3.7 CRGEN Signal Muxing

The two CRGEN modules share pins with UART2 and PWM0. The CRGEN function is selected using the CRGMUX bit field in the PINMUX0 register (see Table 4-32).

**Table 4-32. CRG Pin Muxing**

| PIN FUNCTION | | | | |
|---|---|---|---|---|
| **CRGMUX = 001** | **CRGMUX = 100** | **CRGMUX = 101** | **CRGMUX = 110** | **CRGMUX = other** |
| PWM0(1) | CRG0_PO(1) | CRG0_PO(1) | PWM0(1) | PWM0(1) |
| $\overline{\text{UCTS2}}$ (2) (3) | CRG0_VCXI(3) | CRG0_VCXI(3) | $\overline{\text{UCTS2}}$ (2) (3) | $\overline{\text{UCTS2}}$ (2) (3) |
| CRG1_VCXI | URXD2(2) | CRG1_VCXI | CRG0_VCXI | URXD2(2) |
| CRG1_PO | UTXD2(2) | CRG1_PO | CRG0_PO | UTXD2(2) |

(1) Function will be overridden by TS1_ENAO pin if TSSOMUX = 11 (PINMUX0 register).
(2) Function is determined by UART2CTL bit field value in the PINMUX1 register.
(3) Function will be overridden by TS1_PSTO if TSSOMUX = 11 (PINMUX0 register).


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#### 4.7.3.8 UART0 Pin Muxing

The UART0 module can operate as either a UART or IrDA/CIR interface. The UART0 pin muxing is controlled by the UART0CTL bit field in the PINMUX1 register and the TSPOMUX, TSSIMUX, and TSSOMUX bit fields in the PINMUX0 register. Muxing options are shown in Table 4-33 and Table 4-34. When UART operation is selected, UART0CTL must be set to either '00' for UART with modem signals or '01' for UART without modem signals. When IrDA/CIR operation is selected, UART0CTL must be set to '1x' to use the IrDA/CIR signals and the modem signal become GPIOs. A TSPOMUX setting of '1x' overrides the modem control mux settings. UART0 can still be used as a UART without modem control or in IrDA/CIR mode based on the UART0CTL bit field value. A TSSIMUX setting of '01' overrides the UART data and flow control settings and prevents UART0 from being used. The UART0 modem control pins may be used as either TSIF 0 output or GPIO pins based on the TSPOMUX and UART0CTL settings. A TSSOMUX setting of '11' overrides the RIN function with the TS1_WAITIN function.

**Table 4-33. UART0 Pin Muxing—Part 1**

| TSSIMUX[1] | TSSIMUX[0] | UART0CTL[1] | UART0CTL[0] | PIN FUNCTIONS | | | |
|---|---|---|---|---|---|---|---|
| | | | | URXD0/ TS1_DIN | UTXD0/ URCTX0/ TS1_PSTIN | $\overline{\text{URTS0}}$ / UIRTX0/ TS1_EN_WAITO | $\overline{\text{UCTS0}}$ / USD0 |
| 0 | 0 | 0 | 0 | URXD0 | UTXD0 | $\overline{\text{URTS0}}$ | $\overline{\text{UCTS0}}$ |
| 0 | 0 | 0 | 1 | URXD0 | UTXD0 | $\overline{\text{URTS0}}$ | $\overline{\text{UCTS0}}$ |
| 0 | 0 | 1 | 0 | URXD0 | URCTX0 | UIRTX0 | USD0 |
| 0 | 0 | 1 | 1 | URXD0 | URCTX0 | UIRTX0 | USD0 |
| 0 | 1 | 0 | 0 | TS1_DIN | TS1_PSTIN | TS1_EN_WAITO | – |
| 0 | 1 | 0 | 1 | TS1_DIN | TS1_PSTIN | TS1_EN_WAITO | – |
| 0 | 1 | 1 | 0 | TS1_DIN | TS1_PSTIN | TS1_EN_WAITO | – |
| 0 | 1 | 1 | 1 | TS1_DIN | TS1_PSTIN | TS1_EN_WAITO | – |
| 1 | x | 0 | 0 | URXD0 | UTXD0 | $\overline{\text{URTS0}}$ | $\overline{\text{UCTS0}}$ |
| 1 | x | 0 | 1 | URXD0 | UTXD0 | $\overline{\text{URTS0}}$ | $\overline{\text{UCTS0}}$ |
| 1 | x | 1 | 0 | URXD0 | URCTX0 | UIRTX0 | USD0 |
| 1 | x | 1 | 1 | URXD0 | URCTX0 | UIRTX0 | USD0 |

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**Table 4-34. UART0 Pin Muxing—Part 2**

| TSSOMUX[1] | TSSOMUX[0] | TSPOMUX[1] | TSPOMUX[0] | UART0CTL[1] | UART0CTL[0] | PIN FUNCTIONS | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $\overline{\text{UDTR0}}$ / TS0_ENAO/ GP[36] | $\overline{\text{UDSR0}}$ / TS0_PSTO/ GP[37] | $\overline{\text{UDCD0}}$ / TS0_WAITIN/ GP[38] | URIN0/ GP[8]/ TS1_WAITIN |
| 0 | x | 0 | x | 0 | 0 | $\overline{\text{UDTR0}}$ | $\overline{\text{UDSR0}}$ | $\overline{\text{UDCD0}}$ | URIN0 |
| 0 | x | 0 | x | 0 | 1 | GP[36] | GP[37] | GP[38] | GP[8] |
| 0 | x | 0 | x | 1 | 0 | GP[36] | GP[37] | GP[38] | GP[8] |
| 0 | x | 0 | x | 1 | 1 | GP[36] | GP[37] | GP[38] | GP[8] |
| 0 | x | 1 | x | 0 | 0 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | GP[8] |
| 0 | x | 1 | x | 0 | 1 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | GP[8] |
| 0 | x | 1 | x | 1 | 0 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | GP[8] |
| 0 | x | 1 | x | 1 | 1 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | GP[8] |
| 1 | 0 | 0 | x | 0 | 0 | $\overline{\text{UDTR0}}$ | $\overline{\text{UDSR0}}$ | $\overline{\text{UDCD0}}$ | URIN0 |
| 1 | 0 | 0 | x | 0 | 1 | GP[36] | GP[37] | GP[38] | GP[8] |
| 1 | 0 | 0 | x | 1 | 0 | GP[36] | GP[37] | GP[38] | GP[8] |
| 1 | 0 | 0 | x | 1 | 1 | GP[36] | GP[37] | GP[38] | GP[8] |
| 1 | 0 | 1 | x | 0 | 0 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | GP[8] |
| 1 | 0 | 1 | x | 0 | 1 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | GP[8] |
| 1 | 0 | 1 | x | 1 | 0 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | GP[8] |
| 1 | 0 | 1 | x | 1 | 1 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | GP[8] |
| 1 | 1 | 0 | x | 0 | 0 | $\overline{\text{UDTR0}}$ | $\overline{\text{UDSR0}}$ | $\overline{\text{UDCD0}}$ | TS1_WAITIN |
| 1 | 1 | 0 | x | 0 | 1 | GP[36] | GP[37] | GP[38] | TS1_WAITIN |
| 1 | 1 | 0 | x | 1 | 0 | GP[36] | GP[37] | GP[38] | TS1_WAITIN |
| 1 | 1 | 0 | x | 1 | 1 | GP[36] | GP[37] | GP[38] | TS1_WAITIN |
| 1 | 1 | 1 | x | 0 | 0 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | TS1_WAITIN |
| 1 | 1 | 1 | x | 0 | 1 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | TS1_WAITIN |
| 1 | 1 | 1 | x | 1 | 0 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | TS1_WAITIN |
| 1 | 1 | 1 | x | 1 | 1 | TS0_ENAO | TS0_PSTO | TS0_WAITIN | TS1_WAITIN |


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### 4.7.3.9 UART1 Pin Muxing

The UART1 module can operate as either a UART or IrDA/CIR interface. The UART1 pin muxing options are shown in Table 4-35. When UART operation is selected, UART1CTL must be set to either '00' for UART with flow control or '01' for UART without flow control signals. When IrDA/CIR operation is selected, UART1CTL must be set to '10' to use the IrDA/CIR signals. If UART1 is unused, then setting UART1CTL = 11 muxes GPIO function onto all the pins. The UART1 pin functions may be overridden based on the settings of TSPIMUX and TSPOMUX

**Table 4-35. UART1 Pin Muxing**

| TSPIMUX[1] | TSPIMUX[0] | TSPOMUX[1] | TSPOMUX[0] | UART1CTL[1] | UART1CTL[0] | PIN FUNCTIONS | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | URXD1/ TS0_DIN7/ GP[23] | UTXD1/ URCTX1/ TS0_DOUT7/ GP[24] | $\overline{\text{URTS1}}$ / UIRTX1/ TS0_WAITO/ GP[25] | $\overline{\text{UCTS1}}$ / USD1/ TS0_EN_WAITO/ GP[26] |
| 0 | x | 0 | x | 0 | 0 | URXD1 | UTXD1 | $\overline{\text{URTS1}}$ | $\overline{\text{UCTS1}}$ |
| 0 | x | 0 | x | 0 | 1 | URXD1 | UTXD1 | GP[25] | GP[26] |
| 0 | x | 0 | x | 1 | 0 | URXD1 | URCTX1 | UIRTX1 | USD1 |
| 0 | x | 0 | x | 1 | 1 | GP[23] | GP[24] | GP[25] | GP[26] |
| 0 | x | 1 | 0 | 0 | 0 | URXD1 | UTXD1 | $\overline{\text{URTS1}}$ | $\overline{\text{UCTS1}}$ |
| 0 | x | 1 | 0 | 0 | 1 | URXD1 | UTXD1 | GP[25] | GP[26] |
| 0 | x | 1 | 0 | 1 | 0 | URXD1 | URCTX1 | UIRTX1 | USD1 |
| 0 | x | 1 | 0 | 1 | 1 | GP[23] | GP[24] | GP[25] | GP[26] |
| 0 | x | 1 | 1 | 0 | 0 | URXD1 | TS0_DOUT7 | $\overline{\text{URTS1}}$ | $\overline{\text{UCTS1}}$ |
| 0 | x | 1 | 1 | 0 | 1 | URXD1 | TS0_DOUT7 | GP[25] | GP[26] |
| 0 | x | 1 | 1 | 1 | 0 | URXD1 | TS0_DOUT7 | UIRTX1 | USD1 |
| 0 | x | 1 | 1 | 1 | 1 | GP[23] | TS0_DOUT7 | GP[25] | GP[26] |
| 1 | 0 | 0 | x | 0 | x | URXD1 | UTXD1 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 0 | 0 | x | 1 | 0 | URXD1 | URCTX1 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 0 | 0 | x | 1 | 1 | GP[23] | GP[24] | TS0_WAITO | TS0_EN_WAITO |
| 1 | 0 | 1 | 0 | 0 | x | URXD1 | UTXD1 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 0 | 1 | 0 | 1 | 0 | URXD1 | URCTX1 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 0 | 1 | 0 | 1 | 1 | GP[23] | GP[24] | TS0_WAITO | TS0_EN_WAITO |
| 1 | 0 | 1 | 1 | 0 | x | URXD1 | TS0_DOUT7 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 0 | 1 | 1 | 1 | 0 | URXD1 | TS0_DOUT7 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 0 | 1 | 1 | 1 | 1 | GP[23] | TS0_DOUT7 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 1 | 0 | x | 0 | x | TS0_DIN7 | UTXD1 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 1 | 0 | x | 1 | 0 | TS0_DIN7 | URCTX1 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 1 | 0 | x | 1 | 1 | TS0_DIN7 | GP[24] | TS0_WAITO | TS0_EN_WAITO |
| 1 | 1 | 1 | 0 | 0 | x | TS0_DIN7 | UTXD1 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 1 | 1 | 0 | 1 | 0 | TS0_DIN7 | URCTX1 | TS0_WAITO | TS0_EN_WAITO |
| 1 | 1 | 1 | 0 | 1 | 1 | TS0_DIN7 | GP[24] | TS0_WAITO | TS0_EN_WAITO |
| 1 | 1 | 1 | 1 | x | x | TS0_DIN7 | TS0_DOUT7 | TS0_WAITO | TS0_EN_WAITO |

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### 4.7.3.10 UART2 Pin Muxing

The UART2 module can operate as either a UART or IrDA/CIR interface. The UART2 pin muxing options are shown in Table 4-36 through Table 4-38. When UART operation is selected, UART2CTL must be set to either '00' for UART with flow control or '01' for UART without flow control signals. When IrDA/CIR operation is selected, UART2CTL must be set to '10' to use the IrDA/CIR signals. If UART2 is unused, then setting UART2CTL = 11 muxes GPIO function onto all the pins. The UART2 pin functions may be overridden based on the settings of TSPIMUX, CRGMUX, and TSSOMUX.

**Table 4-36. UART2 Data Pin Muxing**

| CRGMUX[2] | CRGMUX[1] | CRGMUX[0] | UART2CTL[1] | UART2CTL[0] | PIN FUNCTIONS | |
|---|---|---|---|---|---|---|
| | | | | | URXD2/ CRG1_VCXI/ GP[39]/ CRG0_VCXI | UTXD2/ URCTX2/ CRG1_PO/ GP[40]/ CRG0_PO |
| 0 | 0 | 0 | 0 | 0 | URXD2 | UTXD2 |
| 0 | 0 | 0 | 0 | 1 | URXD2 | UTXD2 |
| 0 | 0 | 0 | 1 | 0 | URXD2 | URCTX2 |
| 0 | 0 | 0 | 1 | 1 | GP[39] | GP[40] |
| 0 | 0 | 1 | 0 | 0 | CRG1_VCXI | CRG1_PO |
| 0 | 0 | 1 | 0 | 1 | CRG1_VCXI | CRG1_PO |
| 0 | 0 | 1 | 1 | 0 | CRG1_VCXI | CRG1_PO |
| 0 | 0 | 1 | 1 | 1 | CRG1_VCXI | CRG1_PO |
| 0 | 1 | 0 | 0 | 0 | URXD2 | UTXD2 |
| 0 | 1 | 0 | 0 | 1 | URXD2 | UTXD2 |
| 0 | 1 | 0 | 1 | 0 | URXD2 | URCTX2 |
| 0 | 1 | 0 | 1 | 1 | GP[39] | GP[40] |
| 0 | 1 | 1 | 0 | 0 | URXD2 | UTXD2 |
| 0 | 1 | 1 | 0 | 1 | URXD2 | UTXD2 |
| 0 | 1 | 1 | 1 | 0 | URXD2 | URCTX2 |
| 0 | 1 | 1 | 1 | 1 | GP[39] | GP[40] |
| 1 | 0 | 0 | 0 | 0 | URXD2 | UTXD2 |
| 1 | 0 | 0 | 0 | 1 | URXD2 | UTXD2 |
| 1 | 0 | 0 | 1 | 0 | URXD2 | URCTX2 |
| 1 | 0 | 0 | 1 | 1 | GP[39] | GP[40] |
| 1 | 0 | 1 | 0 | 0 | CRG1_VCXI | CRG1_PO |
| 1 | 0 | 1 | 0 | 1 | CRG1_VCXI | CRG1_PO |
| 1 | 0 | 1 | 1 | 0 | CRG1_VCXI | CRG1_PO |
| 1 | 0 | 1 | 1 | 1 | CRG1_VCXI | CRG1_PO |
| 1 | 1 | 0 | 0 | 0 | CRG0_VCXI | CRG0_PO |
| 1 | 1 | 0 | 0 | 1 | CRG0_VCXI | CRG0_PO |
| 1 | 1 | 0 | 1 | 0 | CRG0_VCXI | CRG0_PO |
| 1 | 1 | 0 | 1 | 1 | CRG0_VCXI | CRG0_PO |
| 1 | 1 | 1 | 0 | 0 | URXD2 | UTXD2 |
| 1 | 1 | 1 | 0 | 1 | URXD2 | UTXD2 |
| 1 | 1 | 1 | 1 | 0 | URXD2 | URCTX2 |
| 1 | 1 | 1 | 1 | 1 | GP[39] | GP[40] |


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### Table 4-37. UART2 Ready-to-Send ( $\overline{\text{URTS2}}$ ) Pin Muxing

| TSPIMUX[1] | TSPIMUX[0] | UART2CTL[1] | UART2CTL[0] | PIN FUNCTION |
|---|---|---|---|---|
| | | | | $\overline{\text{URTS2}}$ / UIRTX2/ TS0_PSTIN/ GP[41] |
| 0 | x | 0 | 0 | $\overline{\text{URTS2}}$ |
| 0 | x | 0 | 1 | GP[41] |
| 0 | x | 1 | 0 | UIRTX2 |
| 0 | x | 1 | 1 | GP[41] |
| 1 | x | x | x | TS0_PSTIN |

### Table 4-38. UART2 Clear-to-Send ( $\overline{\text{UCTS2}}$ ) Pin Muxing

| TSSOMUX ≠ 11 | | | | | PIN FUNCTION | TSSOMUX = 11 | | | | | PIN FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CRGMUX[2] | CRGMUX[1] | CRGMUX[0] | UART2CTL[1] | UART2CTL[0] | $\overline{\text{UCTS2}}$ / USD2/ CRG0_VCXI/ GP[42]/ TS1_PSTO | CRGMUX[2] | CRGMUX[1] | CRGMUX[0] | UART2CTL[1] | UART2CTL[0] | $\overline{\text{UCTS2}}$ / USD2/ CRG0_VCXI/ GP[42]/ TS1_PSTO |
| 0 | 0 | 0 | 0 | 0 | $\overline{\text{UCTS2}}$ | 0 | 0 | 0 | 0 | 0 | TS1_PSTO |
| 0 | 0 | 0 | 0 | 1 | GP[42] | 0 | 0 | 0 | 0 | 1 | TS1_PSTO |
| 0 | 0 | 0 | 1 | 0 | USD2 | 0 | 0 | 0 | 1 | 0 | TS1_PSTO |
| 0 | 0 | 0 | 1 | 1 | GP[42] | 0 | 0 | 0 | 1 | 1 | TS1_PSTO |
| 0 | 0 | 1 | 0 | 0 | $\overline{\text{UCTS2}}$ | 0 | 0 | 1 | 0 | 0 | TS1_PSTO |
| 0 | 0 | 1 | 0 | 1 | GP[42] | 0 | 0 | 1 | 0 | 1 | TS1_PSTO |
| 0 | 0 | 1 | 1 | 0 | USD2 | 0 | 0 | 1 | 1 | 0 | TS1_PSTO |
| 0 | 0 | 1 | 1 | 1 | GP[42] | 0 | 0 | 1 | 1 | 1 | TS1_PSTO |
| 0 | 1 | 0 | 0 | 0 | $\overline{\text{UCTS2}}$ | 0 | 1 | 0 | 0 | 0 | TS1_PSTO |
| 0 | 1 | 0 | 0 | 1 | GP[42] | 0 | 1 | 0 | 0 | 1 | TS1_PSTO |
| 0 | 1 | 0 | 1 | 0 | USD2 | 0 | 1 | 0 | 1 | 0 | TS1_PSTO |
| 0 | 1 | 0 | 1 | 1 | GP[42] | 0 | 1 | 0 | 1 | 1 | TS1_PSTO |
| 0 | 1 | 1 | 0 | 0 | $\overline{\text{UCTS2}}$ | 0 | 1 | 1 | 0 | 0 | TS1_PSTO |
| 0 | 1 | 1 | 0 | 1 | GP[42] | 0 | 1 | 1 | 0 | 1 | TS1_PSTO |
| 0 | 1 | 1 | 1 | 0 | USD2 | 0 | 1 | 1 | 1 | 0 | TS1_PSTO |
| 0 | 1 | 1 | 1 | 1 | GP[42] | 0 | 1 | 1 | 1 | 1 | TS1_PSTO |
| 1 | 0 | 0 | 0 | 0 | CRG0_VCXI | 1 | 0 | 0 | 0 | 0 | TS1_PSTO |
| 1 | 0 | 0 | 0 | 1 | CRG0_VCXI | 1 | 0 | 0 | 0 | 1 | TS1_PSTO |
| 1 | 0 | 0 | 1 | 0 | CRG0_VCXI | 1 | 0 | 0 | 1 | 0 | TS1_PSTO |
| 1 | 0 | 0 | 1 | 1 | CRG0_VCXI | 1 | 0 | 0 | 1 | 1 | TS1_PSTO |
| 1 | 0 | 1 | 0 | 0 | CRG0_VCXI | 1 | 0 | 1 | 0 | 0 | TS1_PSTO |
| 1 | 0 | 1 | 0 | 1 | CRG0_VCXI | 1 | 0 | 1 | 0 | 1 | TS1_PSTO |
| 1 | 0 | 1 | 1 | 0 | CRG0_VCXI | 1 | 0 | 1 | 1 | 0 | TS1_PSTO |
| 1 | 0 | 1 | 1 | 1 | CRG0_VCXI | 1 | 0 | 1 | 1 | 1 | TS1_PSTO |
| 1 | 1 | 0 | 0 | 0 | $\overline{\text{UCTS2}}$ | 1 | 1 | 0 | 0 | 0 | TS1_PSTO |
| 1 | 1 | 0 | 0 | 1 | GP[42] | 1 | 1 | 0 | 0 | 1 | TS1_PSTO |
| 1 | 1 | 0 | 1 | 0 | USD2 | 1 | 1 | 0 | 1 | 0 | TS1_PSTO |
| 1 | 1 | 0 | 1 | 1 | GP[42] | 1 | 1 | 0 | 1 | 1 | TS1_PSTO |
| 1 | 1 | 1 | 0 | 0 | $\overline{\text{UCTS2}}$ | 1 | 1 | 1 | 0 | 0 | TS1_PSTO |
| 1 | 1 | 1 | 0 | 1 | GP[42] | 1 | 1 | 1 | 0 | 1 | TS1_PSTO |
| 1 | 1 | 1 | 1 | 0 | USD2 | 1 | 1 | 1 | 1 | 0 | TS1_PSTO |
| 1 | 1 | 1 | 1 | 1 | GP[42] | 1 | 1 | 1 | 1 | 1 | TS1_PSTO |

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### 4.7.3.11 ARM/DSP Communications Interrupts

The system module includes registers for generating interrupts between the ARM and DSP.

The DSPINT register shows the status of the ARM-to-DSP interrupts. The DSPINT register format is shown in Figure 4-20. Table 4-39 describes the register bit fields. The ARM may generate an interrupt to the DSP by setting one of the four INTDSP[3:0] bits or by setting the INTNMI bit in the DSPINTSET pseudo-register (see Figure 4-21). The interrupt set bit then self-clears and the corresponding INTDSP[3:0] ***or*** INTNMI bit in the DSPINT status register (see Figure 4-20) is automatically set to indicate that the interrupt was generated. After servicing the interrupt, the DSP clears the status bit by writing '1' to the corresponding bit in the DSPINTCLR register (see Figure 4-22). The ARM may poll the status bit to determine when the DSP has completed the interrupt service.

The DSP may generate an interrupt to the ARM in the same manner using the ARMINTSET and ARMINTCLR registers shown/described in Figure 4-24, Table 4-43, and Figure 4-25, Table 4-44, respectively. The DSP can then view the status of the DSP-to-ARM interrupts via the ARMINT register shown/described in Figure 4-23 and Table 4-42.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | |
| R-0000 0000 0000 0000 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | INTNMI | Reserved | | | | INTDSP3 | INTDSP2 | INTDSP1 | INTDSP0 |
| R-0000 000 | | | | | | | R-0 | R-0000 | | | | R-0 | R-0 | R-0 | R-0 |

LEGEND: R = Read only, n = Value at reset

**Figure 4-20. DSPINT Status Register [0x01C4 0060]**

**Table 4-39. DSPINT Status Register Bit Descriptions(1)**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:9 | Reserved | Reserved. A read returns 0. |
| 8 | INTNMI | DSP NMI Status |
| 7:4 | Reserved | Reserved. A read returns 0. |
| 3 | INTDSP3 | ARM-to-DSP Int3 Status |
| 2 | INTDSP2 | ARM-to-DSP Int2 Status |
| 1 | INTDSP1 | ARM-to-DSP Int1 Status |
| 0 | INTDSP0 | ARM-to-DSP Int0 Status |

(1) Read only, writes have no effect.


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| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | |
| R-0000 0000 0000 0000 | | | | | | | | | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | INTNMI | Reserved | | | | INTDSP3 | INTDSP2 | INTDSP1 | INTDSP0 |
| R-0000 000 | | | | | | | R/W-0 | R-0000 | | | | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R = Read, W = Write, n = Value at reset

**Figure 4-21. DSPINTSET Register [0x01C4 0064]**

**Table 4-40. DSPINTSET Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:9 | Reserved | Reserved. A read returns 0. |
| 8 | INTNMI | DSP NMI Set(1) |
| 7:4 | Reserved | Reserved. A read returns 0. |
| 3 | INTDSP3 | ARM-to-DSP Int3 Set(1) |
| 2 | INTDSP2 | ARM-to-DSP Int2 Set(1) |
| 1 | INTDSP1 | ARM-to-DSP Int1 Set(1) |
| 0 | INTDSP0 | ARM-to-DSP Int0 Set(1) |

(1) Writing a '1' generates the interrupt and sets the corresponding bit in the DSPINT status register. The register bit automatically clears to a value of '0'. Writing a '0' has no effect. This register always reads as '0'.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | |
| R-0000 0000 0000 0000 | | | | | | | | | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | INTNMI | Reserved | | | | INTDSP3 | INTDSP2 | INTDSP1 | INTDSP0 |
| R-0000 000 | | | | | | | R/W-0 | R-0000 | | | | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R = Read, W = Write, n = Value at reset

**Figure 4-22. DSPINTCLR Register [0x01C4 0068]**

**Table 4-41. DSPINTCLR Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:9 | Reserved | Reserved. A read returns 0. |
| 8 | INTNMI | DSP NMI Clear(1) |
| 7:4 | Reserved | Reserved. A read returns 0. |
| 3 | INTDSP3 | ARM-to-DSP Int3 Clear(1) |
| 2 | INTDSP2 | ARM-to-DSP Int2 Clear(1) |
| 1 | INTDSP1 | ARM-to-DSP Int1 Clear(1) |
| 0 | INTDSP0 | ARM-to-DSP Int0 Clear(1) |

(1) Writing a '1' clears the corresponding bit in the DSPINT status register. The register bit automatically clears to a value of '0'. Writing a '0' has no effect. This register always reads as '0'.

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| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | |
| R-0000 0000 0000 0000 | | | | | | | | | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | INTARM0 |
| R-0000 0000 0000 000 | | | | | | | | | | | | | | | R-0 |

LEGEND: R = Read only, n = Value at reset

**Figure 4-23. ARMINT Status Register [0x01C4 0070]**

**Table 4-42. ARMINT Status Register Bit Descriptions(1)**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:1 | Reserved | Reserved. A read returns 0. |
| 0 | INTARM0 | DSP-to-ARM Int0 Status |

(1) Read only, writes have no effect.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | |
| R-0000 0000 0000 0000 | | | | | | | | | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | INTARM0 |
| R-0000 0000 0000 000 | | | | | | | | | | | | | | | R/W-0 |

LEGEND: R = Read, W = Write, n = Value at reset

**Figure 4-24. ARMINTSET Register [0x01C4 0074]**

**Table 4-43. ARMINTSET Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:1 | Reserved | Reserved. A read returns 0. |
| 0 | INTARM0 | DSP-to-ARM Int0 Set(1) |

(1) Writing a '1' generates the interrupt and sets the corresponding bit in the ARMINT status register. The register bit automatically clears to a value of '0'. Writing a '0' has no effect. This register always reads as '0'.


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| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | |
| R-0000 0000 0000 0000 | | | | | | | | | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | INTARM0 |
| R-0000 0000 0000 000 | | | | | | | | | | | | | | | R/W-0 |

LEGEND: R = Read, W = Write, n = Value at reset

**Figure 4-25. ARMINTCLR Register [0x01C4 0078]**

**Table 4-44. ARMINTCLR Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:1 | Reserved | Reserved. A read returns 0. |
| 0 | INTARM0 | DSP-to-ARM Int0 Clear(1) |

(1) Writing a '1' clears the corresponding bit in the ARMINT status register. The register bit automatically clears to a value of '0'. Writing a '0' has no effect. This register always reads as '0'.

### 4.7.3.12 Emulation Control

The flexibility of the DM646xT DMSoC architecture allows either the ARM or DSP to control the various peripherals (setup registers, service interrupts, etc.). While this assignment is purely a matter of software convention, during an emulation halt it is necessary for the device to know which peripherals are associated with the halting processor so that only those modules receive the suspend signal. This allows peripherals associated with the other (unhalted) processor to continue normal operation. The SUSPSRC register indicates the emulation suspend source for those peripherals which support emulation suspend.

The SUSPSRC register format is shown in Figure 4-26. Brief details on the peripherals which correspond to the register bits are listed in Table 4-45. When the associated SUSPSRC bit is '0', the peripheral's emulation suspend signal is controlled by the ARM emulator and when set to '1' it is controlled by the DSP emulator.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CRGEN1 SRC | CRGEN0 SRC | TIMR2 SRC | TIMR1 SRC | TIMR0 SRC | GPIO SRC | RSV | PWM1 SRC | PWM0 SRC | SPI SRC | UART2 SRC | UART1 SRC | UART0 SRC | I2C SRC | MCASP1 SRC | MCASP0 SRC |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

| 15 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | HPI SRC | RSV | EMAC SRC | USB SRC | VDCE SRC | TSIF1 SRC | TSIF0 SRC | RSV | VPIF SRC | RESERVED | |
| R-000 | | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R/W-0 | R-0000 | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 4-26. SUSPSRC Register**

**Table 4-45. SUSPSRC Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31 | CRGEN1SRC | Clock Recovery Generator 1 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 30 | CRGEN0SRC | Clock Recovery Generator 0 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 29 | TIMR2SRC | Timer2 (WD Timer) Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 28 | TIMR1SRC | Timer1 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 27 | TIMR0SRC | Timer0 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 26 | GPIOSRC | GPIO Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 25 | RSV | Reserved. Read returns "0". |
| 24 | PWM1SRC | PWM1 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 23 | PWM0SRC | PWM0 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 22 | SPISRC | SPI Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 21 | UART2SRC | UART2 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |


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**Table 4-45. SUSPSRC Register Bit Descriptions (continued)**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 20 | UART1SRC | UART1 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 19 | UART0SRC | UART0 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 18 | I2CSRC | I2C Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 17 | MCASP1SRC | McASP1 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 16 | MCASP0SRC | McASP0 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 15:13 | RESERVED | Reserved. Read returns "0". |
| 12 | HPISRC | HPI Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 11 | RSV | Reserved. Read returns "0". |
| 10 | EMACSRC | Ethernet MAC Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 9 | USBSRC | USB Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 8 | VDCESRC | VDCE Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 7 | TSIF1SRC | TSIF1 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 6 | TSIF0SRC | TSIF0 Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 5 | RSV | Reserved. Read returns "0". |
| 4 | VPIFSRC | Video Port Emulation Suspend Source.<br>0 = ARM emulation suspend.<br>1 = DSP emulation suspend. |
| 3:0 | RESERVED | Reserved. Read returns "0". |

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## 4.8 Debugging Considerations

### 4.8.1 Pullup/Pulldown Resistors

Proper board design should ensure that input pins to the TMS320DM646x DMSoC device always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The TMS320DM646x DMSoC features internal pullup (IPU) and internal pulldown (IPD) resistors on most pins to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor needs to be used in the following situations:

- *Boot and Configuration Pins*: If the pin is both routed out and 3-stated (not driven), an external pullup/pulldown resistor is ***strongly recommended***, even if the IPU/IPD matches the desired value/state.
- *Other Input Pins*: If the IPU/IPD *does not* match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the boot and configuration pins (listed in Table 3-5, *Boot Terminal Functions*), if they are both routed out and 3-stated (not driven), it is ***strongly recommended*** that an external pullup/pulldown resistor be implemented. Although, internal pullup/pulldown resistors exist on these pins and they may match the desired configuration value, providing external connectivity can help ensure that valid logic levels are latched on these device boot and configuration pins. In addition, applying external pullup/pulldown resistors on the boot and configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest $V_{IL}$ level of all inputs connected to the net. For a pullup resistor, this should be above the highest $V_{IH}$ level of all inputs on the net. A reasonable choice would be to target the $V_{OL}$ or $V_{OH}$ levels for the logic family of the limiting device; which, by definition, have margin to the $V_{IL}$ and $V_{IH}$ levels.
- Select a pullup/pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the $DV_{DD}$ rail.

For most systems, a 1-kΩ resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can be used to compliment the IPU/IPD on the boot and configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can also be used as an external PU/PD on the pins that have IPUs/IPDs disabled and require an external PU/PD resistor while still meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current ($I_I$), and the low-/high-level input voltages ($V_{IL}$ and $V_{IH}$) for the DM6467T DMSoC, see Section 6.3, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*.


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For the internal pullup/pulldown resistors for all device pins, see the peripheral/system-specific terminal functions table.

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# 5 System Interconnect

On the DM6467T device, the C64x+ megamodule, the ARM subsystem, the EDMA3 transfer controllers, and the system peripherals are interconnected through a switch fabric architecture. The switch fabric is composed of multiple switched central resources (SCRs) and multiple bridges.

For more detailed information on the DMSoC System Interconnect Architecture, including the device-specific SCRs, bridges, and the system connection matrix, see the *TMS320DM6467 SoC Architecture and Throughput Overview* Application Report (literature number SPRAAW4).


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# 6 Device Operating Conditions

## 6.1 Absolute Maximum Ratings Over Operating Case Temperature Range (Unless Otherwise Noted)(1)

| | | |
|---|---|---|
| Supply voltage ranges: | Core ($CV_{DD}$, $DEV_CV_{DD}$, $AUX_CV_{DD}$)(2) | –0.5 V to 1.5 V |
| | I/O, 3.3V ($DV_{DD33}$, $USB_V_{DDA3P3}$)(2) | -0.3 V to 3.8 V |
| | I/O, 1.8V ($DV_{DDR2}$, $PLL1V_{DD18}$, $PLL2V_{DD18}$, $DEV_DV_{DD18}$, $AUX_DV_{DD18}$, $USB_V_{DD1P8}$)(2) | -0.3 V to 2.6 V |
| Input and Output voltage ranges: | V I/O, 3.3-V pins (except PCI-capable pins) | –0.3 V to 3.8 V<br>–0.3 V to $DV_{DD33}$ + 0.3 V |
| | V I/O, 3.3-V pins PCI-capable pins | –0.5 V to 4.2 V<br>–0.5 V to $DV_{DD33}$ + 0.5 V |
| | V I/O, 1.8 V | –0.3 V to 2.6 V<br>–0.3 V to $DV_{DD18}$ + 0.3 V |
| Operating case temperature ranges, $T_c$: | (default) [-1G] | 0°C to 85°C |
| | (D version) Industrial Temperature [-1G] | -40°C to 85°C |
| Storage temperature range, $T_{stg}$ | (default) | –55°C to 150°C |
| Electrostatic Discharge (ESD) Performance: | ESD-HBM (Human Body Model)(3) | ± 2000 V |
| | ESD-CDM (Charged-Device Model)(4) | ± 500 V |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to $V_{SS}$.
(3) Based on JEDEC JESD22-A114E (*Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*).
(4) Based on JEDEC JESD22-C101C (*Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*).

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## 6.2 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $CV_{DD}$ | Supply voltage, Core ($CV_{DD}$, DEV_$CV_{DD}$, AUX_$CV_{DD}$) (1) | (-1G) | 1.235 | 1.3 | 1.365 | V |
| $DV_{DD}$ | Supply voltage, I/O, 3.3V ($DV_{DD33}$, USB_$V_{DDA3P3}$) | | 3.14 | 3.3 | 3.46 | V |
| | Supply voltage, I/O, 1.8V ($DV_{DDR2}$, PLL1$V_{DD18}$, PLL2$V_{DD18}$, DEV_$DV_{DD18}$, AUX_$DV_{DD18}$, USB_$V_{DD1P8}$ (2)) | | 1.71 | 1.8 | 1.89 | V |
| $V_{SS}$ | Supply ground ($V_{SS}$, PLL1$V_{SS}$, PLL2$V_{SS}$, DEV_$V_{SS}$ (3), AUX_$V_{SS}$ (3), USB_$V_{SSREF}$) | | 0 | 0 | 0 | V |
| DDR_VREF | DDR2 reference voltage (4) | | 0.49$DV_{DDR2}$ | 0.5$DV_{DDR2}$ | 0.51$DV_{DDR2}$ | V |
| DDR_ZP | DDR2 impedance control, connected via 50-Ω (±5% tolerance) resistor to $V_{SS}$ | | | $V_{SS}$ | | V |
| DDR_ZN | DDR2 impedance control, connected via 50-Ω (±5% tolerance) resistor to $DV_{DDR2}$ | | | $DV_{DDR2}$ | | V |
| $V_{IH}$ | High-level input voltage, 3.3 V (except JTAG[TCK], PCI-capable, and I2C pins) | | 2 | | | V |
| | High-level input voltage, JTAG [TCK] | | 2.5 | | | V |
| | High-level input voltage, PCI | | 0.5$DV_{DD33}$ | | | V |
| | High-level input voltage, I2C | | 0.7$DV_{DD33}$ | | | V |
| | High-level input voltage, non-DDR I/O, 1.8 V | | 0.65$DV_{DD18}$ | | | V |
| $V_{IL}$ | Low-level input voltage, 3.3 V (except PCI-capable and I2C pins) | | | | 0.8 | V |
| | Low-level input voltage, PCI | | | | 0.3$DV_{DD33}$ | V |
| | Low-level input voltage, I2C | | 0 | | 0.3$DV_{DD33}$ | V |
| | Low-level input voltage, non-DDR I/O, 1.8 V | | | | 0.35$DV_{DD18}$ | V |
| $T_c$ | Operating case temperature | Default | 0 | | 85 | °C |
| | | D Version | -40 | | 85 | °C |
| $F_{SYSCLK1}$ | DSP Operating Frequency (SYSCLK1) | -1G | 20 | | 1 | GHz |

(1) Future variants of TI SoC devices may operate at voltages ranging from 0.9 V to 1.4 V to provide a range of system power/performance options. TI highly recommends that users design-in a supply that can handle multiple voltages within this range (i.e., 1.0 V, 1.05 V, 1.1 V, 1.14 V, 1.2 V, 1.26 V, 1.3 V, 1.365 V with ± 3% tolerances) by implementing simple board changes such as reference resistor values or input pin configuration modifications. Not incorporating a flexible supply may limit the system's ability to easily adapt to future versions of TI SoC devices.
(2) Oscillator 1.8 V power supply (DEV_$DV_{DD18}$) can be connected to the same 1.8 V power supply as $DV_{DDR2}$.
(3) Oscillator ground (DEV_$V_{SS}$ and AUX_$V_{SS}$) must be kept separate from other grounds and connected directly to the crystal load capacitor ground.
(4) DDR_VREF is expected to equal 0.5$DV_{DDR2}$ of the transmitting device and to track variations in the $DV_{DDR2}$.


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## 6.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

| PARAMETER | | TEST CONDITIONS (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Low/full speed: USB_DN and USB_DP | | 2.8 | | USB_$V_{DDA3P3}$ | V |
| | High speed: USB_DN and USB_DP | | 360 | | 440 | mV |
| | High-level output voltage (3.3V I/O except PCI-capable and I2C pins) | $DV_{DD33}$ = MIN, $I_{OH}$ = MAX | 2.4 | | | V |
| | High-level output voltage (3.3V I/O PCI-capable pins) | $I_{OH}$ = –0.5 mA, $DV_{DD33}$ = 3.3 V | 0.9$DV_{DD33}$ (2) | | | V |
| $V_{OL}$ | Low/full speed: USB_DN and USB_DP | | 0.0 | | 0.3 | V |
| | High speed: USB_DN and USB_DP | | –10 | | 10 | mV |
| | Low-level output voltage (3.3V I/O except PCI-capable and I2C pins) | $DV_{DD33}$ = MIN, $I_{OL}$ = MAX | | | 0.4 | V |
| | Low-level output voltage (3.3V I/O PCI-capable pins) | $I_{OL}$ = 1.5 mA, $DV_{DD33}$ = 3.3 V | | | 0.1$DV_{DD33}$ (2) | V |
| | Low-level output voltage (3.3V I/O I2C pins) | $I_O$ = 3 mA | 0 | | 0.4 | V |
| $V_{LDO}$ | USB_$V_{DDA1P2LDO}$ output voltage | | 1.14 | 1.2 | 1.26 | V |
| $I_I$ (3) | Input current [DC] (except I2C and PCI-capable pins) | $V_I$ = $V_{SS}$ to $DV_{DD33}$ without opposing internal resistor | | | ±20 | µA |
| | | $V_I$ = $V_{SS}$ to $DV_{DD33}$ with opposing internal pullup resistor (4) | 50 | 100 | 250 | µA |
| | | $V_I$ = $V_{SS}$ to $DV_{DD33}$ with opposing internal pulldown resistor (4) | –250 | –100 | –50 | µA |
| | Input current [DC] (I2C) | $V_I$ = $V_{SS}$ to $DV_{DD33}$ | | | ±20 | µA |
| | Input current (PCI-capable pins) [DC](5) | 0 < $V_I$ < $DV_{DD33}$ = 3.3 V without opposing internal resistor | | | ±50 | µA |
| | | 0 < $V_I$ < $DV_{DD33}$ = 3.3 V with opposing internal pullup resistor (4) | 50 | | 250 | µA |
| | | 0 < $V_I$ < $DV_{DD33}$ = 3.3 V with opposing internal pulldown resistor (4) | –250 | | –50 | µA |
| $I_{OH}$ | High-level output current [DC] | GMTCLK, MTXD[7:0], MTXEN | | | –8 | mA |
| | | DDR2; $V_{OH}$ = $DV_{DDR2}$ – 0.4 V | | | –8 | mA |
| | | PCI-capable pins (PCI pin function *only*) | | | –0.5(2) | mA |
| | | All other peripherals | | | –4 | mA |
| $I_{OL}$ | Low-level output current [DC] | GMTCLK, MTXD[7:0], MTXEN | | | 8 | mA |
| | | DDR2; $V_{OL}$ = 0.4 V | | | 8 | mA |
| | | PCI-capable pins (PCI pin function *only*) | | | 1.5(2) | mA |
| | | All other peripherals | | | 4 | mA |
| $I_{OZ}$ (6) | I/O Off-state output current | $V_O$ = $DV_{DD33}$ or $V_{SS}$; internal pull disabled | | | ±20 | µA |
| | | $V_O$ = $DV_{DD33}$ or $V_{SS}$; internal pull enabled | | ±100 | | µA |
| $I_{CDD}$ | Core ($CV_{DD}$, DEV_$CV_{DD}$, AUX_$CV_{DD}$) supply current(7) | $CV_{DD}$ = 1.3 V, DSP clock = 1 GHz ARM Clock = 500 MHz, DDR Clock = 400 MHz | | 1792.22 | | mA |
| $I_{DDD}$ | 3.3V I/O ($DV_{DD33}$, USB_$V_{DDA3P3}$) supply current(7) | $DV_{DD}$ = 3.3 V, DSP clock = 1 GHz ARM Clock = 500 MHz, DDR Clock = 400 MHz | | 25.66 | | mA |

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.
(2) These rated numbers are from the *PCI Local Bus Specification Revision 2.3*. The DC specifications and AC specifications are defined in Table 4-3 (DC Specifications for 3.3V Signaling) and Table 4-4 (AC Specifications for 3.3V Signaling), respectively.
(3) $I_I$ applies to input-only pins and bi-directional pins. For input-only pins, $I_I$ indicates the input leakage current. For bi-directional pins, $I_I$ indicates the input leakage current and off-state (Hi-Z) output leakage current.
(4) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.
(5) PCI input leakage currents include Hi-Z output leakage for all bidirectional buffers with 3-state outputs.
(6) $I_{OZ}$ applies to output-only pins, indicating off-state (Hi-Z) output leakage current.
(7) Measured under the following conditions: 60% DSP CPU utilization; ARM doing typical activity (peripheral configurations, other housekeeping activities); DDR2 Memory Controller at 50% utilization, 50% writes, 32 bits, 50% bit switching at room temperature (25 °C). The actual current draw varies across manufacturing processes and is highly application-dependent. For more details on core and I/O activity, as well as information relevant to board power supply design, see the *TMS320DM6467T Power Consumption Summary* Application Report (literature number SPRAB64).

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## Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted) *(continued)*

| PARAMETER | | TEST CONDITIONS [1] | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{DDD}$ | 1.8V I/O ($DV_{DDR2}$, $PLL1V_{PRW18}$, $PLL2V_{PRW18}$, $DEV_DV_{DD18}$, $AUX_DV_{DD18}$, $USB_V_{DD1P8}$) supply current[7] | $DV_{DD}$ = 1.8 V, DSP clock = 1 GHz ARM Clock = 500 MHz, DDR Clock = 400 MHz | | 214.02 | | mA |
| $C_I$ | Input capacitance | | | | 4 | pF |
| $C_o$ | Output capacitance | | | | 4 | pF |


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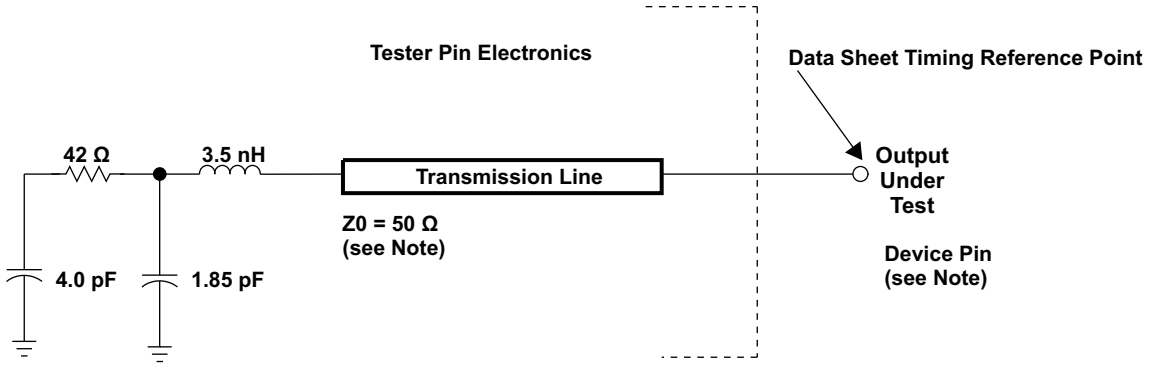
# 7 Peripheral Information and Electrical Specifications

## 7.1 Parameter Information




NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

**Figure 7-1. Test Load Circuit for AC Timing Measurements**

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

### *7.1.1 1.8-V and 3.3-V Signal Transition Levels*

All input and output timing parameters are referenced to $V_{ref}$ for both "0" and "1" logic levels. For 3.3-V I/O, $V_{ref}$ = 1.5 V. For 1.8-V I/O, $V_{ref}$ = 0.9 V.

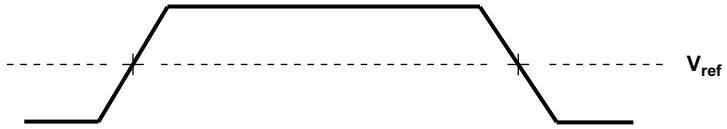



**Figure 7-2. Input and Output Voltage Reference Levels for AC Timing Measurements**

All rise and fall transition timing parameters are referenced to $V_{IL}$ MAX and $V_{IH}$ MIN for input clocks, $V_{OL}$ MAX and $V_{OH}$ MIN for output clocks.

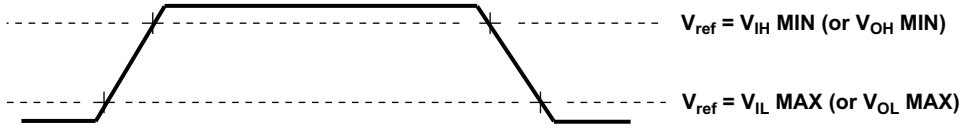



**Figure 7-3. Rise and Fall Transition Time Voltage Reference Levels**

### *7.1.2 3.3-V Signal Transition Rates*

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

### 7.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

For the DDR2 memory controller interface, it is *not* necessary to use the IBIS models to analyze timing characteristics. Section 7.10.2, *DDR2 Interface*, provides a PCB routing rules solution that describes the routing rules to ensure the DDR2 memory controller interface timings are met.

## 7.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.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## 7.3 Power Supplies

For more information regarding TI's power management products and suggested devices to power TI DSPs, visit www.ti.com/processorpower.

### 7.3.1 Power-Supply Sequencing

The DM6467T includes one core supply ($CV_{DD}$), and two I/O supplies—$DV_{DD33}$ and $DV_{DDR2}$. To ensure proper device operation, a specific power-up sequence ***must*** be followed. Some TI power-supply devices include features that facilitate power sequencing—for example, Auto-Track and Slow-Start/Enable features. For more information on TI power supplies and their features, visit www.ti.com/processorpower.

Here is a summary of the power sequencing requirements:

- The power ramp order **must** be $CV_{DD}$ before $DV_{DDR2}$, and $DV_{DDR2}$ before $DV_{DD33}$—meaning during power up, the voltage at the $DV_{DDR2}$ rail should never exceed the voltage at the $CV_{DD}$ rail. Similarly, the voltage at the $DV_{DDD33}$ rail should never exceed the voltage at the $DV_{DDR2}$ rail.
- From the time that power ramp begins, all power supplies ($CV_{DD}$, $DV_{DDR2}$, $DV_{DD33}$) **must** be stable within 200 ms. The term "stable" means reaching the recommended operating condition (see Section 6.2, *Recommended Operating Conditions* table).

### 7.3.2 Power-Supply Design Considerations

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the DM6467T device, the PC board should include separate power planes for core, I/O, and ground; all bypassed with high-quality low-ESL/ESR capacitors.

### 7.3.3 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DM6467T. These caps need to be close to the DM6467T power pins, no more than 1.25 cm maximum distance to be effective. Physically smaller caps, such as 0402, are better but need to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value.

Larger caps for each supply can be placed further away for bulk decoupling. Large bulk caps (on the order of 100 µF) should be furthest away, but still as close as possible. Large caps for each supply should be placed outside of the BGA footprint.

As with the selection of any component, verification of capacitor availability over the product's production lifetime should be considered.

For more details on capacitor usage and placement, see the *Implementing DDR2 PCB Layout on the TMS320DM646x DMSoC* Application Report (literature number SPRAAM1A).

### 7.3.4 DM6467T Power and Clock Domains

The DM6467T includes one single power domain — the "Always On" power domain. The "Always On" power domain is always on when the chip is on. The "Always On" domain is powered by the $CV_{DD}$ pins of the DM6467T. All DM6467T modules lie within the "Always On" power domain. Table 7-1 provides a listing of the DM6467T clock domains.

Two primary reference clocks are required for the DM6467T device. These can either be crystal inputs *or* driven by external oscillators. A 33-MHz or 33.3-MHz crystal is recommended for the system PLLs, which generate the internal clocks for the ARM926, DSP, HDVICPs, peripherals, and the EDMA3. A 24- or 48-MHz crystal is also required if the USB (24-MHz only) or UART (either 24- or 48-MHz) peripherals are to be used. In addition, the 24- or 48-MHz input clock can be used to source the McASPs' clocks. For further description of the DM6467T clock domains, see Table 7-2 and Figure 7-4.

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The DM6467T architecture is divided into the power and clock domains shown in Table 7-1. Table 7-2 further discusses the clock domains and their ratios. Figure 7-4 shows the Clock Domain Block Diagram.

**Table 7-1. DM6467T Power and Clock Domains**

| POWER DOMAIN | CLOCK DOMAIN | PERIPHERAL/MODULE |
|---|---|---|
| Always On | SYSCLK3 | UART0 |
| Always On | SYSCLK3 | UART1 |
| Always On | SYSCLK3 | UART2 |
| Always On | SYSCLK3 | I2C |
| Always On | SYSCLK3 | Timer0 |
| Always On | SYSCLK3 | Timer1 |
| Always On | SYSCLK3 | Timer2 |
| Always On | SYSCLK3 | PWM0 |
| Always On | SYSCLK3 | PWM1 |
| Always On | SYSCLK2 | DDR2 |
| Always On | SYSCLK2 | VPIF |
| Always On | SYSCLK2 | TSIF0 |
| Always On | SYSCLK2 | TSIF1 |
| Always On | SYSCLK2 | VDCE |
| Always On | SYSCLK2 | HDVICP0 |
| Always On | SYSCLK2 | HDVICP1 |
| Always On | SYSCLK2 | EDMA3 |
| Always On | SYSCLK2 | PCI |
| Always On | SYSCLK2 | SCR |
| Always On | SYSCLK3 | GPSC |
| Always On | SYSCLK3 | LPSCs |
| Always On | SYSCLK3 | PLLC1 |
| Always On | SYSCLK3 | PLLC2 |
| Always On | SYSCLK3 | Ice Pick |
| Always On | SYSCLK3 | EMIFA |
| Always On | SYSCLK3 | USB |
| Always On | SYSCLK3 | HPI |
| Always On | SYSCLK3 | VLYNQ |
| Always On | SYSCLK3 | EMAC/MDIO |
| Always On | SYSCLK3 | SPI |
| Always On | SYSCLK3 | McASP0 |
| Always On | SYSCLK3 | McASP1 |
| Always On | SYSCLK3 | CRGEN0 |
| Always On | SYSCLK3 | CRGEN1 |
| Always On | SYSCLK4 | ATA |
| Always On | SYSCLK3 | GPIO |
| Always On | SYSCLK1 | C64x+ CPU |
| Always On | SYSCLK2 | ARM926 |


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**Table 7-2. DM6467T Clock Domains**

| SUBSYSTEM | CLOCK DOMAIN | DOMAIN CLOCK SOURCE | FIXED RATIO vs. SYSCLK1 FREQ | CLOCK MODES FREQUENCY (MHz) | |
|---|---|---|---|---|---|
| | | | | BYPASS MODE [default RATIO] | PLL MODE (-1G)(1) |
| DSP Subsystem | PLLDIV1 | PLLC1 SYSCLK1 | 1:1 | 33.30 MHz | 999 MHz |
| ARM926 Subsystem, EDMA3, HDVICP, PCI, VDCE, VPIF, TSIFs, DDR2 Mem Ctlr | PLLDIV2 | PLLC1 SYSCLK2 | 1:2 | 16.65 MHz | 499.50 MHz |
| Peripherals (GPIO, Timers, I2C, PWMs, HPI, EMAC, EMIFA, VLYNQ, SPI, ARM INTC, USB2.0, UARTs, McASPs, CRGENs, SYSTEM) | PLLDIV3 | PLLC1 SYSCLK3 | 1:4 | 8.33 MHz | 249.75 MHz |
| ATA | PLLDIV4 | PLLC1 SYSCLK4 | 1:6 [default]<br>1:7(2) | 5.55 MHz | 142.71 MHz |
| TSIF0(3) | PLLDIV5 | PLLC1 SYSCLK5 | 1:8 [default]<br>1:10(2) | 4.16 MHz | 99.90 MHz |
| TSIF1(3) | PLLDIV6 | PLLC1 SYSCLK6 | 1:8 [default]<br>1:10(2) | 4.16 MHz | 99.90 MHz |
| VPIF(3) | PLLDIV8 | PLLC1 SYSCLK8 | 1:8 [default]<br>1:7(2) | 4.16 MHz | 142.71 MHz(4) |
| VLYNQ | PLLDIV9 | PLLC1 SYSCLK9 | 1:6 [default]<br>1:10(2) | 5.55 MHz | 99.90 MHz |
| DDR2 PHY | PLLDIV1 | PLLC2 SYSCLK1 | 1:1 | 33.30 MHz | 799.20 MHz |

(1) These table values assume a DEV_MXI/DEV_CLKIN of 33.3 MHz and a PLL1 multiplier equal to 30. Any input crystal with a frequency between 20 MHz and 35 MHz can be used.
(2) To achieve these quoted frequencines, the PLLC1 SYSCLKx (for SYSCLK4, SYSCLK5, SYSCLK6, SYSCLK8, SYSCLK9) default divider values ***must*** be changed based on the input crystal frequency. For the steps to change the PLLC1 SYSCLKx divider values, see the*TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).
(3) These domain clock sources, along with VP_CLKIN[3:0], STC_CLKIN, CRG0_VCXI, and CRG1_VCXI clock signals, go through the clock select logic to determine the clock source enabled as the input to the VPIF and TSIF peripherals.
(4) Use an external clock source for the 54-/74.25-/108-/148.5-MHz VPIF clock.

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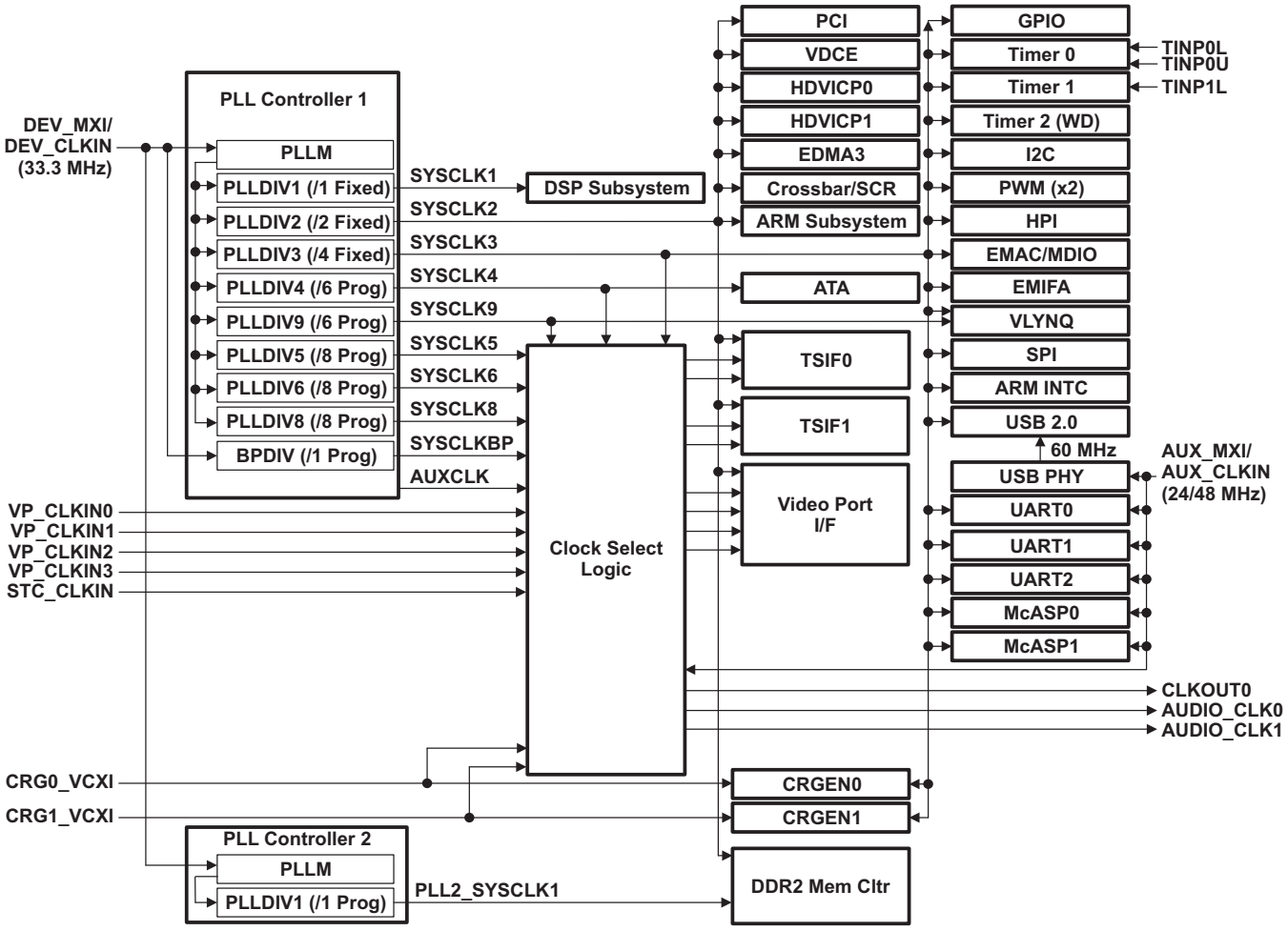


**Figure 7-4. PLL1 and PLL2 Clock Domain Block Diagram**

For further detail on PLL1 and PLL2, see the structure block diagrams shown in Figure 7-5 and Figure 7-6, respectively.

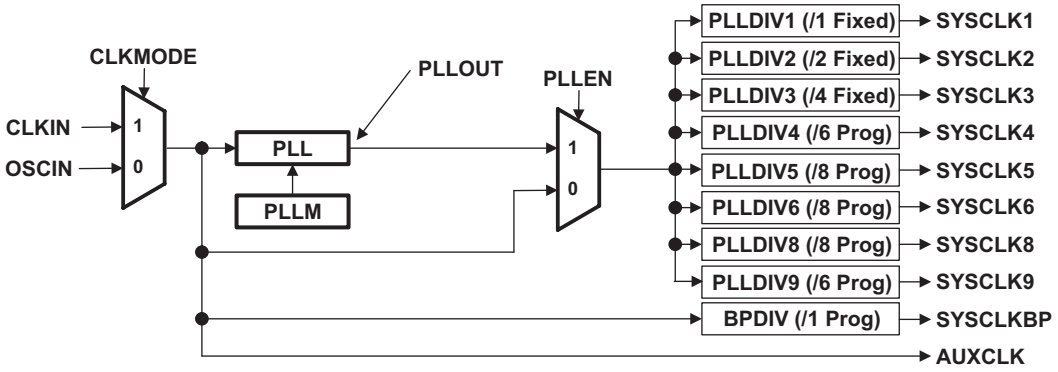


**Figure 7-5. PLL1 Structure Block Diagram**


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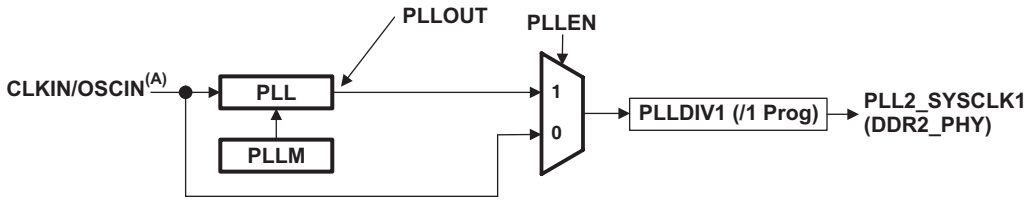


(A) As selected by the PLL2 PLLCTL register

**Figure 7-6. PLL2 Structure Block Diagram**

### 7.3.5 Power and Sleep Controller (PSC)

The Power and Sleep Controller (PSC) controls device power by gating off clocks to individual peripherals/modules. The PSC consists of a Global PSC (GPSC) and a set of Local PSCs (LPSCs). The GPSC contains memory mapped registers, PSC interrupt control, and a state machine for each peripheral/module. An LPSC is associated with each peripheral/module and provides clock and reset control. The GPSC controls all of the DM6467T's LPSCs. The ARM Subsystem does not have an LPSC module. ARM sleep mode is accomplished through the wait for interrupt instruction. The LPSCs for DM6467T are shown in Table 7-3. The PSC Register memory map is given in Table 7-4. For more details on the PSC, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

**Table 7-3. DM6467T LPSC Assignments**

| LPSC NUMBER | PERIPHERAL/MODULE | LPSC NUMBER | PERIPHERAL/MODULE | LPSC NUMBER | PERIPHERAL/MODULE |
|---|---|---|---|---|---|
| 0 | Reserved | 16 | Video Port | 32 | SPI |
| 1 | C64x+ CPU | 17 | Video Port | 33 | GPIO |
| 2 | HDVICP0 | 18 | TSIF0 | 34 | TIMER0 |
| 3 | HDVICP1 | 19 | TSIF1 | 35 | TIMER1 |
| 4 | EDMA CC | 20 | DDR2 Memory Controller | 36 | Reserved |
| 5 | EDMA TC0 | 21 | EMIFA | 37 | Reserved |
| 6 | EDMA TC1 | 22 | McASP0 | 38 | Reserved |
| 7 | EDMA TC2 | 23 | McASP1 | 39 | Reserved |
| 8 | EDMA TC3 | 24 | CRGEN0 | 40 | Reserved |
| 9 | USB2.0 | 25 | CRGEN1 | 41 | Reserved |
| 10 | ATA | 26 | UART0 | 42 | Reserved |
| 11 | VLYNQ | 27 | UART1 | 43 | Reserved |
| 12 | HPI | 28 | UART2 | 44 | Reserved |
| 13 | PCI | 29 | PWM0 | 45 | ARM INTC |
| 14 | EMAC/MDIO | 30 | PWM1 | | |
| 15 | VDCE | 31 | I2C | | |

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**Table 7-4. PSC Registers**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C4 1000 | PID | Peripheral Revision and Class Information Register |
| 0x01C4 1004 - 0x01C4 1017 | – | Reserved |
| 0x01C4 1018 | INTEVAL | Interrupt Evaluation Register |
| 0x01C4 101C - 0x01C4 1039 | – | Reserved |
| 0x01C4 1040 | MERRPR0 | Module Error Pending 0 (mod 0- 31) Register |
| 0x01C4 1044 | MERRPR1 | Module Error Pending 1 (mod 32- 63) Register |
| 0x01C4 1048 - 0x01C4 1049 | – | Reserved |
| 0x01C4 1050 | MERRCR0 | Module Error Clear 0 (mod 0 - 31) Register |
| 0x01C4 1054 | MERRCR1 | Module Error Clear 1 (mod 32 - 63) Register |
| 0x01C4 1058 - 0x01C4 111F | | Reserved |
| 0x01C4 1120 | PTCMD | Power Domain Transition Command Register |
| 0x01C4 1124 - 0x01C4 1127 | – | Reserved |
| 0x01C4 1128 | PTSTAT | Power Domain Transition Status Register |
| 0x01C4 112C - 0x01C4 11FF | – | Reserved |
| 0x01C4 1200 | PDSTAT0 | Power Domain Status 0 Register (Always On) |
| 0x01C4 1204 - 0x01C4 12FF | – | Reserved |
| 0x01C4 1300 | PDCTL0 | Power Domain Control 0 Register (Always On) |
| 0x01C4 1304 - 0x01C4 17FF | – | Reserved |
| 0x01C4 1800 - 0x01C4 1803 | – | Reserved |
| 0x01C4 1804 | MDSTAT1 | Module Status 1 Register (C64x+ CPU) |
| 0x01C4 1808 | MDSTAT2 | Module Status 2 Register (HDVICP0) |
| 0x01C4 180C | MDSTAT3 | Module Status 3 Register (HDVICP1) |
| 0x01C4 1810 | MDSTAT4 | Module Status 4 Register (EDMA CC) |
| 0x01C4 1814 | MDSTAT5 | Module Status 5 Register (EDMA TC0) |
| 0x01C4 1818 | MDSTAT6 | Module Status 6 Register (EDMA TC1) |
| 0x01C4 181C | MDSTAT7 | Module Status 7 Register (EDMA TC2) |
| 0x01C4 1820 | MDSTAT8 | Module Status 8 Register (EDMA TC3) |
| 0x01C4 1824 | MDSTAT9 | Module Status 9 Register (USB) |
| 0x01C4 1828 | MDSTAT10 | Module Status 10 Register (ATA) |
| 0x01C4 182C | MDSTAT11 | Module Status 11 Register (VLYNQ) |
| 0x01C4 1830 | MDSTAT12 | Module Status 12 Register (HPI) |
| 0x01C4 1834 | MDSTAT13 | Module Status 13 Register (PCI) |
| 0x01C4 1838 | MDSTAT14 | Module Status 14 Register (EMAC) |
| 0x01C4 183C | MDSTAT15 | Module Status 15 Register (VDCE) |
| 0x01C4 1840 | MDSTAT16 | Module Status 16 Register (Vdieo Port) |
| 0x01C4 1844 | MDSTAT17 | Module Status 17 Register (Video Port) |
| 0x01C4 1848 | MDSTAT18 | Module Status 18 Register (TSIF0) |
| 0x01C4 184C | MDSTAT19 | Module Status 19 Register (TSIF1) |
| 0x01C4 1850 | MDSTAT20 | Module Status 20 Register (DDR2 Mem Ctlr) |
| 0x01C4 1854 | MDSTAT21 | Module Status 21 Register (EMIFA) |
| 0x01C4 1858 | MDSTAT22 | Module Status 22 Register (McASP0) |
| 0x01C4 185C | MDSTAT23 | Module Status 23 Register (McASP1) |
| 0x01C4 1860 | MDSTAT24 | Module Status 24 Register (CRGEN0) |
| 0x01C4 1864 | MDSTAT25 | Module Status 25 Register (CRGEN1) |
| 0x01C4 1868 | MDSTAT26 | Module Status 26 Register (UART0) |
| 0x01C4 186C | MDSTAT27 | Module Status 27 Register (UART1) |
| 0x01C4 1870 | MDSTAT28 | Module Status 28 Register (UART2) |


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**Table 7-4. PSC Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C4 1874 | MDSTAT29 | Module Status 29 Register (PWM0) |
| 0x01C4 1878 | MDSTAT30 | Module Status 30 Register (PWM1) |
| 0x01C4 187C | MDSTAT31 | Module Status 31 Register (I2C) |
| 0x01C4 1880 | MDSTAT32 | Module Status 32 Register (SPI) |
| 0x01C4 1884 | MDSTAT33 | Module Status 33 Register (GPIO) |
| 0x01C4 1888 | MDSTAT34 | Module Status 34 Register (TIMER0) |
| 0x01C4 188C | MDSTAT35 | Module Status 35 Register (TIMER1) |
| 0x01C4 1890 - 0x01C4 18B3 | – | Reserved |
| 0x01C4 18B4 | MDSTAT45 | Module Status 45 Register (ARM INTC) |
| 0x01C4 18B8 - 0x01C4 19FF | – | Reserved |
| 0x01C4 1A00 - 0x01C4 1A03 | – | Reserved |
| 0x01C4 1A04 | MDCTL1 | Module Control 1 Register (C64x+ CPU) |
| 0x01C4 1A08 | MDCTL2 | Module Control 2 Register (HDVICP0) |
| 0x01C4 1A0C | MDCTL3 | Module Control 3 Register (HDVICP1) |
| 0x01C4 1A10 | MDCTL4 | Module Control 4 Register (EDMA CC) |
| 0x01C4 1A14 | MDCTL5 | Module Control 5 Register (EDMA TC0) |
| 0x01C4 1A18 | MDCTL6 | Module Control 6 Register (EDMA TC1) |
| 0x01C4 1A1C | MDCTL7 | Module Control 7 Register (EDMA TC2) |
| 0x01C4 1A20 | MDCTL8 | Module Control 8 Register (EDMA TC3) |
| 0x01C4 1A24 | MDCTL9 | Module Control 9 Register (USB) |
| 0x01C4 1A28 | MDCTL10 | Module Control 10 Register (ATA) |
| 0x01C4 1A2C | MDCTL11 | Module Control 11 Register (VLYNQ) |
| 0x01C4 1A30 | MDCTL12 | Module Control 12 Register (HPI) |
| 0x01C4 1A34 | MDCTL13 | Module Control 13 Register (PCI) |
| 0x01C4 1A38 | MDCTL14 | Module Control 14 Register (EMAC) |
| 0x01C4 1A3C | MDCTL15 | Module Control 15 Register (VDCE) |
| 0x01C4 1A40 | MDCTL16 | Module Control 16 Register (Video Port) |
| 0x01C4 1A44 | MDCTL17 | Module Control 17 Register (Video Port) |
| 0x01C4 1A48 | MDCTL18 | Module Control 18 Register (TSIF0) |
| 0x01C4 1A4C | MDCTL19 | Module Control 19 Register (TSIF1) |
| 0x01C4 1A50 | MDCTL20 | Module Control 20 Register (DDR2 Mem Ctlr) |
| 0x01C4 1A54 | MDCTL21 | Module Control 21 Register (EMIFA) |
| 0x01C4 1A58 | MDCTL22 | Module Control 22 Register (McASP0) |
| 0x01C4 1A5C | MDCTL23 | Module Control 23 Register (McASP1) |
| 0x01C4 1A60 | MDCTL24 | Module Control 24 Register (CRGEN0) |
| 0x01C4 1A64 | MDCTL25 | Module Control 25 Register (CRGEN1) |
| 0x01C4 1A68 | MDCTL26 | Module Control 26 Register (UART0) |
| 0x01C4 1A6C | MDCTL27 | Module Control 27 Register (UART1) |
| 0x01C4 1A70 | MDCTL28 | Module Control 28 Register (UART2) |
| 0x01C4 1A74 | MDCTL29 | Module Control 29 Register (PWM0) |
| 0x01C4 1A78 | MDCTL30 | Module Control 30 Register (PWM1) |
| 0x01C4 1A7C | MDCTL31 | Module Control 31 Register (I2C) |
| 0x01C4 1A80 | MDCTL32 | Module Control 32 Register (SPI) |
| 0x01C4 1A84 | MDCTL33 | Module Control 33 Register (GPIO) |
| 0x01C4 1A88 | MDCTL34 | Module Control 34 Register (TIMER0) |
| 0x01C4 1A8C | MDCTL35 | Module Control 35 Register (TIMER1) |
| 0x01C4 1A90 - 0x01C4 1AB3 | – | Reserved |

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**Table 7-4. PSC Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C4 1AB4 | MDCTL45 | Module Control 45 Register (ARM INTC) |
| 0x01C4 1AB8 - 0x01C4 1FFF | – | Reserved |


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## 7.4 External Clock Input From DEV_MXI/DEV_CLKIN and AUX_MXI/AUX_CLKIN Pins

The DM6467T device includes two options to provide an external clock input for both the system and auxiliary oscillators:

- Use an on-chip oscillator with external crystal (fundamental parallel resonant mode only, no overtone support).
- Use an external 1.8-V LVCMOS-compatible clock input.

Any input crystal frequency between 27 MHz and 35 MHz can be used for the System Oscillator (DEV_MXI/DEV_CLKIN).

The optimal external clock input frequency for the crystals are 33 MHz or 33.3 MHz for the system oscillator (DEV_MXI/DEV_CLKIN) and 24 MHz for the auxiliary oscillator. Section 7.4.1.1 provides more details on Option 1, using an on-chip oscillator with external crystal for the 33.3-MHz system oscillator. Section 7.4.1.2 provides more details on Option 1, using an on-chip oscillator with external crystal for the 24-MHz auxiliary oscillator. Section 7.4.2.1 provides details on Option 2, using an external 1.8-V LVCMOS-compatible clock input for the 33.3-MHz system oscillator. Section 7.4.2 provides details on Option 2, using an external 1.8-V LVCMOS-compatible clock input for the 24-MHz auxiliary oscillator.

### *7.4.1 Clock Input Option 1—Crystal*

#### 7.4.1.1 33.3-MHz for System Oscillator Clock Input Option 1—Crystal

In this option, a crystal is used as the external clock input to the DM6467T system oscillator.

The 33.3-MHz oscillator provides the reference clock for all DM6467T subsystems and peripherals. The on-chip oscillator requires an external 33.3-MHz crystal connected across the DEV_MXI and DEV_MXO pins, along with two load capacitors, as shown in Figure 7-7. The external crystal load capacitors ***must*** be connected only to the 33.3-MHz oscillator ground pin (DEV_$V_{SS}$). ***Do not*** connect to board ground ($V_{SS}$). The DEV_$DV_{DD18}$ pin can be connected to the same 1.8 V power supply as $DV_{DDR2}$.

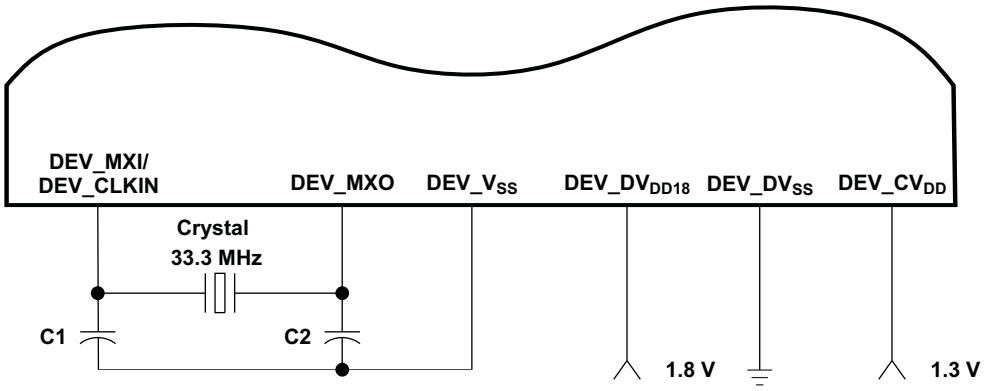


**Figure 7-7. 33.3-MHz System Oscillator**

The load capacitors, C1 and C2, should be chosen such that the equation is satisfied (for typical values, see Table 7-5). $C_L$ in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (DEV_MXI and DEV_MXO) and to the DEV_$V_{SS}$ pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

**Table 7-5. Input Requirements for Crystal on the 27 – 35-MHz System Oscillator**

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Start-Up Time (from power up until oscillating at stable frequency) | | | | 4 | ms |
| | Oscillation Frequency | | 27 | 33 or 33.3 | 35 | MHz |
| | ESR | 27 – 31-MHz | | | 50 | Ω |
| | | 32 – 35-MHz | | | 40 | Ω |
| | Parallel Load Capacitance (C1 and C2) [Max] | | | | 12 – 20 | pF |
| | Frequency Tolerance | | | ± 50 | | ppm |
| | Aging | | | ± 5 | | ppm |
| | Thermal Stability | | | ± 50 | | ppm |
| | Oscillation Mode | | | Fundamental | | n/a |
| | Drive Level (Max) | | | | 0.8 | mW |
| | Shunt Capacitance (Max) | | | | 5 | pF |

### 7.4.1.2 24-MHz Auxiliary Oscillator Clock Input Option 1—Crystal

In this option, a crystal is used as the external clock input to the DM6467T auxiliary oscillator.

The 24-MHz oscillator provides the reference clock for USB and UART peripherals and the internal clock source for the McASP peripherals. The on-chip oscillator requires an external 24-MHz crystal connected across the AUX_MXI and AUX_MXO pins, along with two load capacitors, as shown in Figure 7-8. The external crystal load capacitors ***must*** be connected only to the 24-MHz oscillator ground pin (AUX_$V_{SS}$). ***Do not*** connect to board ground ($V_{SS}$). The AUX_$DV_{DD18}$ pin can be connected to the same 1.8 V power supply as $DV_{DDR2}$.

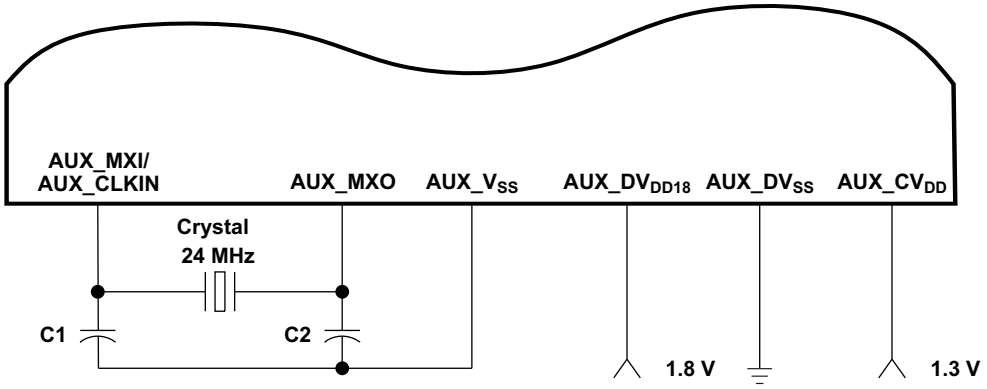


**Figure 7-8. 24-MHz Auxiliary Oscillator**

The load capacitors, C1 and C2, should be chosen such that the equation is satisfied (for typical values, see Table 7-6). $C_L$ in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (AUX_MXI and AUX_MXO) and to the AUX_$V_{SS}$ pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

**Table 7-6. Input Requirements for Crystal on the 24-MHz Auxiliary Oscillator**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| | Start-Up Time (from power up until oscillating at stable frequency of 24 MHz) | | | 4 | ms |
| | Oscillation Frequency | | 24 | | MHz |
| | ESR | | | 60 | Ω |


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**Table 7-6. Input Requirements for Crystal on the 24-MHz Auxiliary Oscillator (continued)**

| | PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| (1) | Frequency Stability | | | ±50 | ppm |
| | Parallel Load Capacitance (C1 and C2) [Max] | | | 12 – 20 | pF |
| | Frequency Tolerance | | ± 50 | | ppm |
| | Aging | | ± 5 | | ppm |
| | Thermal Stability | | ± 50 | | ppm |
| | Oscillation Mode | | Fundamental | | n/a |
| | Drive Level (Max) | | | 0.8 | mW |
| | Shunt Capacitance (Max) | | | 5 | pF |

(1) If the USB is used, a 24-MHz, 50-ppm crystal is recommended.

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### 7.4.2 Clock Input Option 2—1.8-V LVCMOS-Compatible Clock Input

#### 7.4.2.1 33.3-MHz System Oscillator Clock Input Option 2—1.8-V LVCMOS-Compatible Clock Input

In this option, a 1.8-V LVCMOS-Compatible Clock Input is used as the external clock input to the system oscillator. The external connections are shown in Figure 7-9. The DEV_MXI/DEV_CLKIN pin is connected to the 1.8-V LVCMOS-Compatible clock source. The DEV_MXO pin is left unconnected. The DEV_$V_{SS}$ pin is connected to board ground ($V_{SS}$). The DEV_$DV_{DD18}$ pin can be connected to the same 1.8-V power supply as $DV_{DDR2}$.

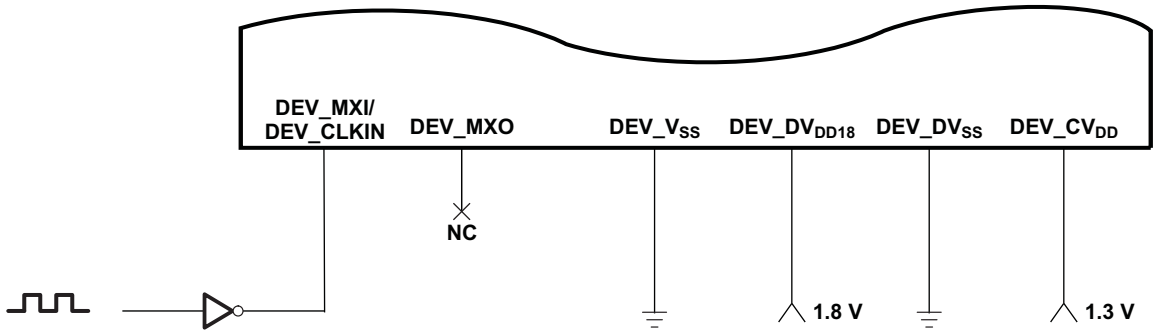


**Figure 7-9. 1.8-V LVCMOS-Compatible Clock Input**

The clock source ***must*** meet the DEV_MXI/DEV_CLKIN timing requirements in Section 7.5.5, *Clock PLL Electrical Data/Timing (Input and Output Clocks)*.

#### 7.4.2.2 24-MHz Auxiliary Oscillator Clock Input Option 2—1.8-V LVCMOS-Compatible Clock Input

In this option, a 1.8-V LVCMOS-Compatible Clock Input is used as the external clock input to the auxiliary oscillator. The external connections are shown in Figure 7-10. The AUX_MXI/AUX_CLKIN pin is connected to the 1.8-V LVCMOS-Compatible clock source. The AUX_MXO pin is left unconnected. The AUX_$V_{SS}$ pin is connected to board ground ($V_{SS}$). The AUX_$DV_{DD18}$ pin can be connected to the same 1.8-V power supply as $DV_{DDR2}$.

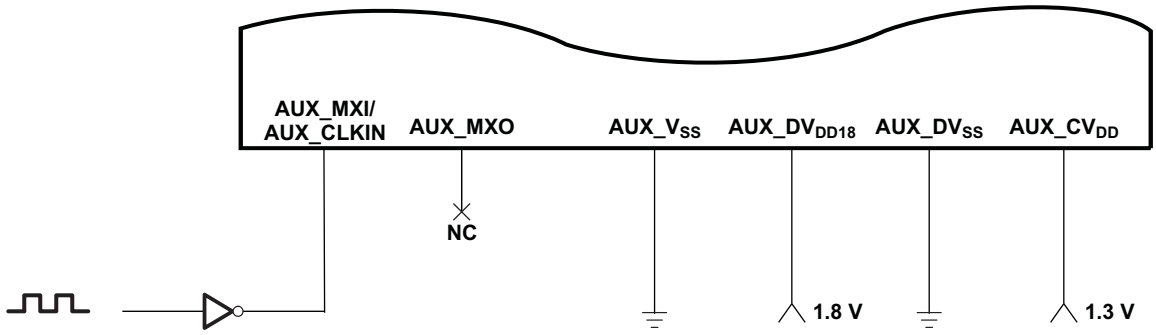


**Figure 7-10. 1.8-V LVCMOS-Compatible Clock Input**

The clock source ***must*** meet the AUX_MXI/AUX_CLKIN timing requirements in Section 7.5.5, *Clock PLL Electrical Data/Timing (Input and Output Clocks)*.


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## 7.5 Clock PLLs

There are two independently controlled PLLs on DM6467T. PLL1 generates the frequencies required for the ARM, DSP, HDVICP0/1, EDMA, and peripherals. PLL2 generates the frequencies required for the DDR2 interface. Any input crystal frequency between 27 MHz and 35 MHz can be used for the System Oscillator (DEV_MXI/DEV_CLKIN). The recommended reference clock for both PLLs is the 33-MHz or 33.3-MHz crystal input. The DM6467T has a third PLL that is embedded within the USB2.0 PHY and the 24-MHz oscillator is its reference clock source. This particular PLL is only usable for USB operation, and is discussed further in the *TMS320DM646x DMSoC Universal Serial Bus (USB) Controller* User's Guide (literature number SPRUER7).

### 7.5.1 PLL1 and PLL2

Both PLL1 and PLL2 power are supplied externally via the 1.8-V PLL power-supply pins ($PLL1V_{DD18}$ and $PLL2V_{DD18}$). An external EMI filter circuit ***must*** be added to $PLL1V_{DD18}$ and $PLL2V_{DD18}$, as shown in Figure 7-11. The 1.8-V supply of the EMI filters must be from the same 1.8-V power plane supplying the device's 1.8-V I/O power-supply pins ($DV_{DDR2}$). TI recommends EMI filter manufacturer Murata, part number NFM18CC222R1C3.

All PLL external components (C1, C2, C3, C4, and the EMI Filters) ***must*** be placed as close to the device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown in Figure 7-11. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (C1, C2, C3, C4, and the EMI Filters).

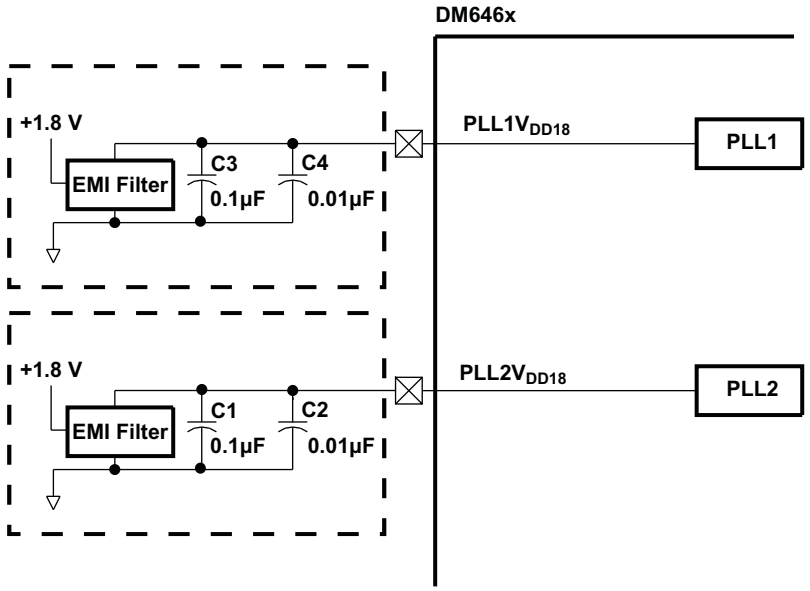


**Figure 7-11. PLL1 and PLL2 External Connection**

The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see Section 7.5.5, *Clock PLL Electrical Data/Timing (Input and Output Clocks)*.

There is an allowable range for PLL multiplier (PLLM). There is a minimum and maximum operating frequency for DEV_MXI/DEV_CLKIN, PLLOUT, AUX_MXI/AUX_CLKIN, and the device clocks (SYSCLKs). The PLL Controllers ***must*** be configured not to exceed any of these constraints documented in this section (certain combinations of external clock inputs, internal dividers, and PLL multiply ratios might not be supported). For these constraints (ranges), see Table 7-7 through Table 7-9 .

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**Table 7-7. PLL1 and PLL2 Multiplier Ranges**

| PLL MULTIPLIER (PLLM) | -1G | |
|---|---|---|
| | MIN | MAX |
| PLL1 Multiplier | x14 | x32 |
| PLL2 Multiplier | x14 | x32 |

**Table 7-8. PLLC1 Clock Frequency Ranges**

| CLOCK SIGNAL NAME | -1G | | UNIT |
|---|---|---|---|
| | MIN | MAX | |
| DEV_MXI/DEV_CLKIN (1) | 20 | 35 | MHz |
| PLLOUT | 400 | 1000 | MHz |
| SYSCLK1 (PLLDIV1 Domain) | | 1000 | MHz |

(1) DEV_MXI/DEV_CLKIN input clock is used for both PLL Controllers (PLLC1 and PLLC2).

**Table 7-9. PLLC2 Clock Frequency Ranges**

| CLOCK SIGNAL NAME | -1G | | UNIT |
|---|---|---|---|
| | MIN | MAX | |
| DEV_MXI/DEV_CLKIN (1) | 20 | 35 | MHz |
| PLLOUT | 400 | 800 | MHz |
| PLL2_SYSCLK1 (to DDR2 PHY) | | 800 | MHz |

(1) DEV_MXI/DEV_CLKIN input clock is used for both PLL Controllers (PLLC1 and PLLC2).

Both PLL1 and PLL2 have stabilization, lock, and reset timing requirements that ***must*** be followed.

The PLL stabilization time is the amount of time that ***must*** be allotted for the internal PLL regulators to become stable after the PLL is powered up (after the PLLCTL.PLLPWRDN bit goes through a 1-to-0 transition). The PLL should *not* be operated until this stabilization time has expired. This stabilization step ***must*** be applied after these resets—a Power-on Reset, a Warm Reset, or a Max Reset, as the PLLCTL.PLLPWRDN bit resets to a "1". For the PLL stabliziation time value, see Table 7-10.

The PLL reset time is the amount of wait time needed for the PLL to properly reset (writing PLLRST = 1) before bringing the PLL out of reset (writing PLLRST = 0). For the PLL reset time value, see Table 7-10.

The PLL lock time is the amount of time needed from when the PLL is taken out of reset (PLLRST = 0 with PLLEN = 0) to when to when the PLL controller can be switched to PLL mode (PLLEN = 1). For the PLL lock time value, see Table 7-10.

**Table 7-10. PLL1 and PLL2 Stabilization, Lock, and Reset Times**

| PLL STABILIZATION/ LOCK/RESET TIME | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| PLL Stabilization Time | 150 | | | µs |
| PLL Lock Time | | | 2000C (1) | ns |
| PLL Reset Time | 128C (1) | | | ns |

(1) C = CLKIN cycle time in ns. For example, when DEV_MXI/DEV_CLKIN or AUX_MXI/AUX_CLKIN frequency is 27 MHz, use C = 37.037 ns.


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For details on the PLL initialization software sequence, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

For more information on the clock domains and their clock ratio restrictions, see Section 7.3.4, *DM6467T Power and Clock Domains*.

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### 7.5.2 PLL Controller Register Description(s)

A summary of the PLL controller registers is shown in Table 7-11. For more details, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

**Table 7-11. PLL and Reset Controller Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| **PLL1 Controller Registers** | | |
| 0x01C4 0800 | PID | Peripheral ID Register |
| 0x01C4 08E4 | RSTYPE | Reset Type Register |
| 0x01C4 0900 | PLLCTL | PLL Controller 1 PLL Control Register |
| 0x01C4 0910 | PLLM | PLL Controller 1 PLL Multiplier Control Register |
| 0x01C4 0918 | PLLDIV1 | PLL Controller 1 Divider 1 Register (SYSCLK1) |
| 0x01C4 091C | PLLDIV2 | PLL Controller 1 Divider 2 Register (SYSCLK2) |
| 0x01C4 0920 | PLLDIV3 | PLL Controller 1 Divider 3 Register (SYSCLK3) |
| 0x01C4 0928 | – | Reserved |
| 0x01C4 092C | BPDIV | PLL Controller 1 Bypass Control-Divider Register (SYSCLKBP) |
| 0x01C4 0938 | PLLCMD | PLL Controller 1 Command Register |
| 0x01C4 093C | PLLSTAT | PLL Controller 1 Status Register (Shows PLLC1 PLLCTL Status) |
| 0x01C4 0940 | ALNCTL | PLL Controller 1 Clock Align Control Register<br>(Indicates Which SYSCLKs Need to be Aligned for Proper Device Operation) |
| 0x01C4 0944 | DCHANGE | PLL Controller 1 PLLDIV Divider Ratio Change Status Register<br>(Indicates if SYSCLK Divide Ratio has been modified) |
| 0x01C4 0948 | CKEN | PLL Controller 1 Clock Enable Control Register |
| 0x01C4 094C | CKSTAT | PLL Controller 1 Clock Status Register (For All Clocks Except SYSCLKx) |
| 0x01C4 0950 | SYSTAT | PLL Controller 1 SYSCLK Status Register (Indicates SYSCLK on/off Status) |
| 0x01C4 0960 | PLLDIV4 | PLL Controller 1 Divider 4 Register (SYSCLK4) |
| 0x01C4 0964 | PLLDIV5 | PLL Controller 1 Divider 5 Register (SYSCLK5) |
| 0x01C4 0968 | PLLDIV6 | PLL Controller 1 Divider 6 Register (SYSCLK6) |
| 0x01C4 096C | – | Reserved |
| 0x01C4 0970 | PLLDIV8 | PLL Controller 1 Divider 8 Register (SYSCLK8) |
| 0x01C4 0974 | PLLDIV9 | PLL Controller 1 Divider 9 Register (SYSCLK9) |
| **PLL2 Controller Registers** | | |
| 0x01C4 0C00 | PID | Peripheral ID Register |
| 0x01C4 0D00 | PLLCTL | PLL Controller 2 PLL Control Register |
| 0x01C4 0D10 | PLLM | PLL Controller 2 PLL Multiplier Control Register |
| 0x01C4 0D18 | PLLDIV1 | PLL Controller 2 Divider 1 Register (PLL2_SYSCLK1 DDR2 PHY) |
| 0x01C4 0D28 | – | Reserved |
| 0x01C4 0D38 | PLLCMD | PLL Controller 2 Command Register |
| 0x01C4 0D3C | PLLSTAT | PLL Controller 2 Status Register (Shows PLLC2 PLLCTL Status) |
| 0x01C4 0D40 | ALNCTL | PLL Controller 2 Clock Align Control Register<br>(Indicates Which SYSCLKs Need to be Aligned for Proper Device Operation) |
| 0x01C4 0D44 | DCHANGE | PLL Controller 2 PLLDIV Divider Ratio Change Status Register<br>(Indicates if SYSCLK Divide Ratio has been modified) |
| 0x01C4 0D48 | CKEN | PLL Controller 2 Clock Enable Control Register |
| 0x01C4 0D4C | CKSTAT | PLL Controller 2 Clock Status Register (For All Clocks Except SYSCLKx) |
| 0x01C4 0D50 | SYSTAT | PLL Controller 2 SYSCLK Status Register (Indicates SYSCLK on/off Status) |
| 0x01C4 0D54 - 0x01C4 0FFF | – | Reserved |


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### 7.5.3 Clock PLL Considerations With External Clock Sources

If the internal oscillator is bypassed, to minimize the clock jitter a single clean power supply should power both the DM6467T device and the external clock oscillator circuit. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see Section 7.5.5, *Clock PLL Electrical Data/Timing (Input and Output Clocks)*.

Rise/fall times, duty cycles (high/low pulse durations), and the load capacitance of the external clock source must meet the device requirements in this data manual (see Section 6.3, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*, and Section 7.5.5, *Clock PLL Electrical Data/Timing (Input and Output Clocks)*.)

### 7.5.4 Output Clocks (CLKOUT0, AUDIO_CLK1, AUDIO_CLK0) - Clock Select Logic

The DM6467T includes a selectable general-purpose clock output (CLKOUT0) [see Figure 7-12] and two selectable audio output clocks (AUDIO_CLK0 and AUDIO_CLK1) for synchronizing external audio devices with the on-chip system or video clocks [see Figure 7-13 and Figure 7-14]. The source for these output clocks is controlled by the CLKCTL register (0x01C4 005C). For more detailed information on the CLKCTL register, see Section 4.3.3, *Clock and Oscillator Control*.

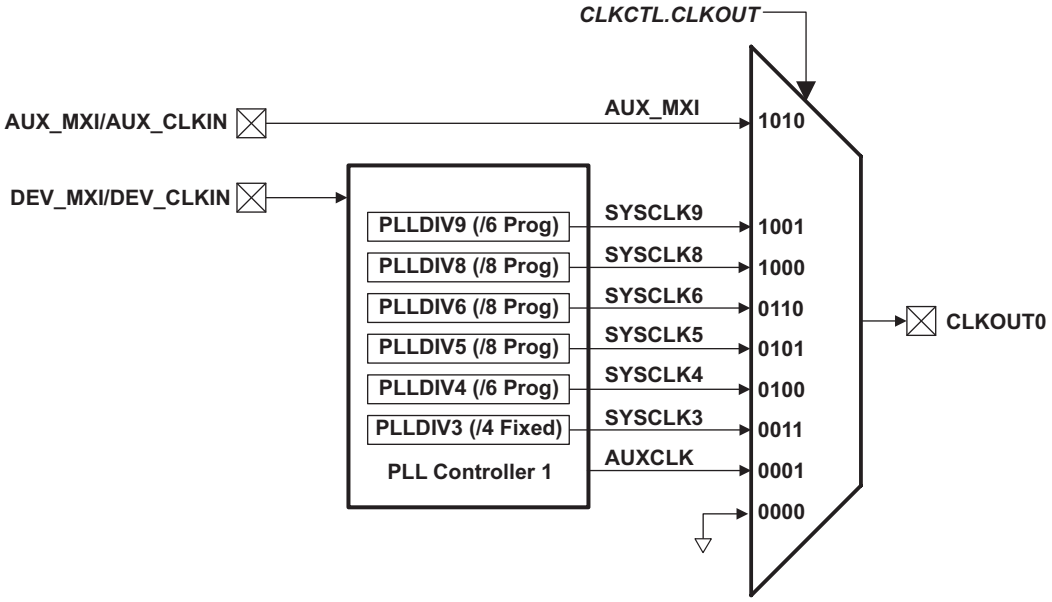


**Figure 7-12. CLKOUT0 Source Selection**

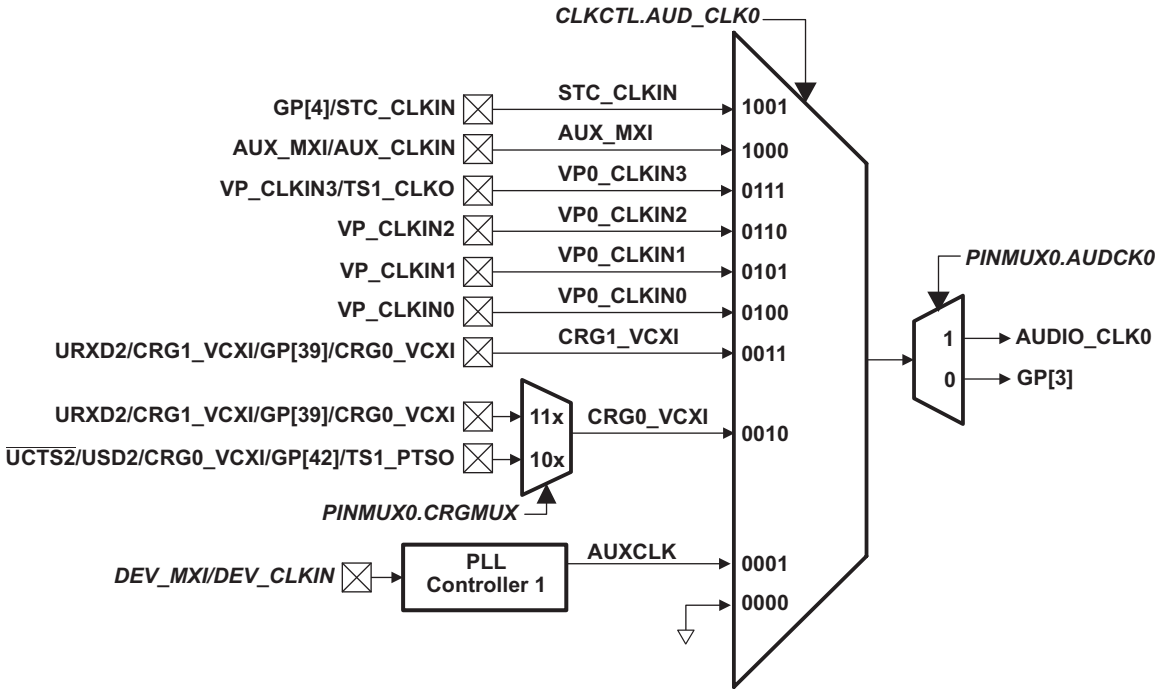


**Figure 7-13. AUDIO_CLK0 Source Selection**

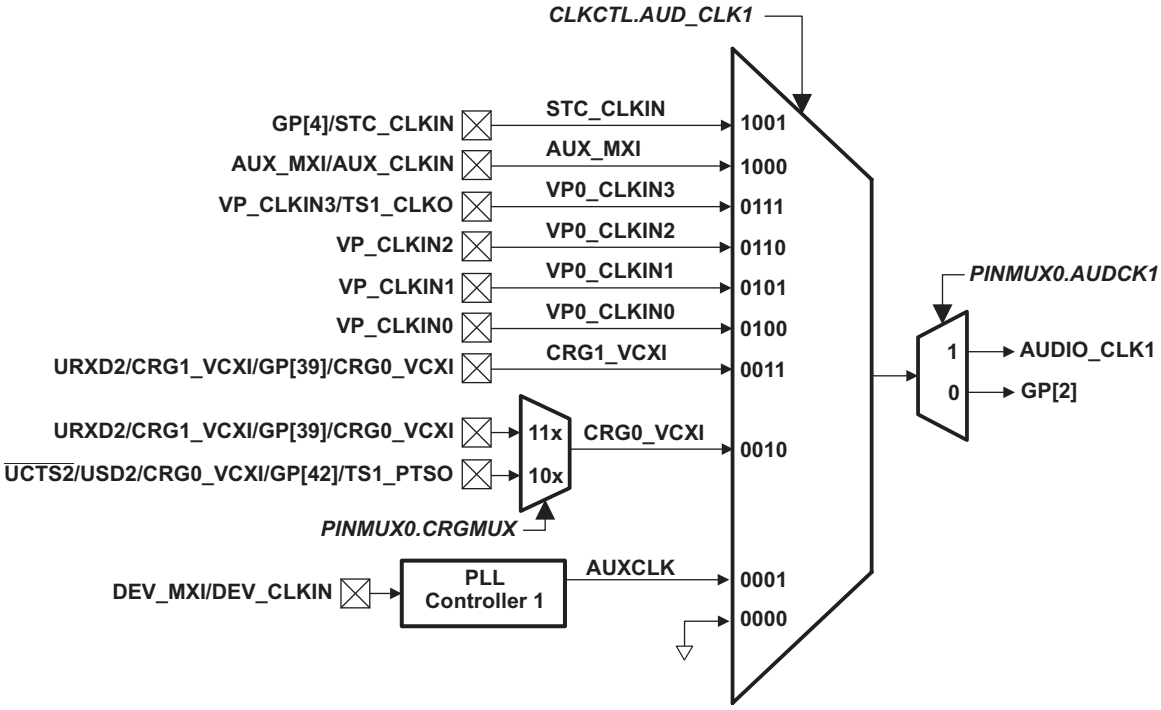


**Figure 7-14. AUDIO_CLK1 Source Selection**


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### 7.5.5 Clock PLL Electrical Data/Timing (Input and Output Clocks)

**Table 7-12. Timing Requirements for DEV_MXI/DEV_CLKIN(1) (2) (3) (4) (see Figure 7-15)**

| NO. | | | -1G | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| 1 | $t_{c(DMXI)}$ | Cycle time, DEV_MXI/DEV_CLKIN | 28.57 | 30.03 | 50 | ns |
| 2 | $t_{w(DMXIH)}$ | Pulse duration, DEV_MXI/DEV_CLKIN high | 0.45C | | 0.55C | ns |
| 3 | $t_{w(DMXIL)}$ | Pulse duration, DEV_MXI/DEV_CLKIN low | 0.45C | | 0.55C | ns |
| 4 | $t_{t(DMXI)}$ | Transition time, DEV_MXI/DEV_CLKIN | | | 7 | ns |
| 5 | $t_{J(DMXI)}$ | Period jitter, DEV_MXI/DEV_CLKIN | | | 0.02C | ns |

(1) The DEV_MXI/DEV_CLKIN frequency and PLL multiply factor should be chosen such that the resulting clock frequency is within the specific range for CPU operating frequency. For example, for a -1G speed device with a 33.3-MHz DEV_CLKIN frequency, the PLL multiply factor should be ≤ 30.
(2) The reference points for the rise and fall transitions are measured at $V_{IL}$ MAX and $V_{IH}$ MIN.
(3) For more details on the PLL multiplier factors, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (Literature Number SPRUEP9).
(4) C = DEV_CLKIN cycle time in ns. For example, when DEV_MXI/DEV_CLKIN frequency is 33.3 MHz, use C = 30.03 ns.

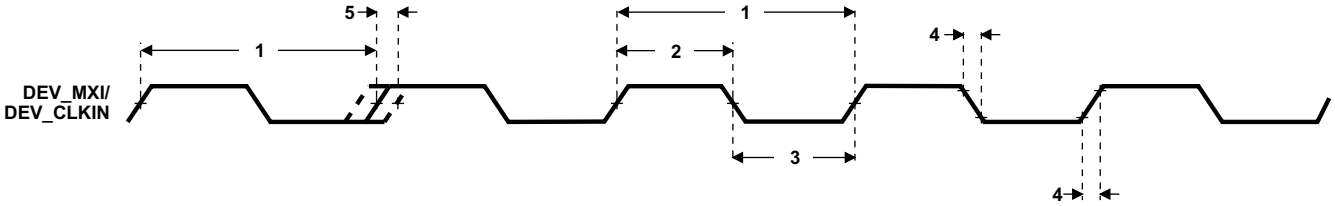


**Figure 7-15. DEV_MXI/DEV_CLKIN Timing**

**Table 7-13. Timing Requirements for AUX_MXI/AUX_CLKIN (1) (2) (3) (see Figure 7-16)**

| NO. | | | -1G | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| 1 | $t_{c(AMXI)}$ | Cycle time, AUX_MXI/AUX_CLKIN | | 41.$\overline{6}$ or 20.8$\overline{3}$ (4) | | ns |
| 2 | $t_{w(AMXIH)}$ | Pulse duration, AUX_MXI/AUX_CLKIN high | 0.45C | | 0.55C | ns |
| 3 | $t_{w(AMXIL)}$ | Pulse duration, AUX_MXI/AUX_CLKIN low | 0.45C | | 0.55C | ns |
| 4 | $t_{t(AMXI)}$ | Transition time, AUX_MXI/AUX_CLKIN | | | 7 | ns |
| 5 | $t_{J(AMXI)}$ | Period jitter, AUX_MXI/AUX_CLKIN | | | 0.02C | ns |
| 6 | $S_f$ | Frequency stability, AUX_MXI/AUX_CLKIN(4) | | | ± 50 | ppm |

(1) The reference points for the rise and fall transitions are measured at $V_{IL}$ MAX and $V_{IH}$ MIN.
(2) For more details on the PLL, see the *TMS320DM646x DMSoC Universal Serial Bus (USB) Controller* User's Guide (Literature Number SPRUER7).
(3) C = DEV_CLKIN cycle time in ns. For example, when AUX_MXI/AUX_CLKIN frequency is 24 MHz, use C = 41.$\overline{6}$ ns and when AUX_MXI/AUX_CLKIN frequency is 48 MHz, use C = 20.8$\overline{3}$ ns.
(4) If the USB is used, a 24-MHz, 50-ppm crystal is recommended.

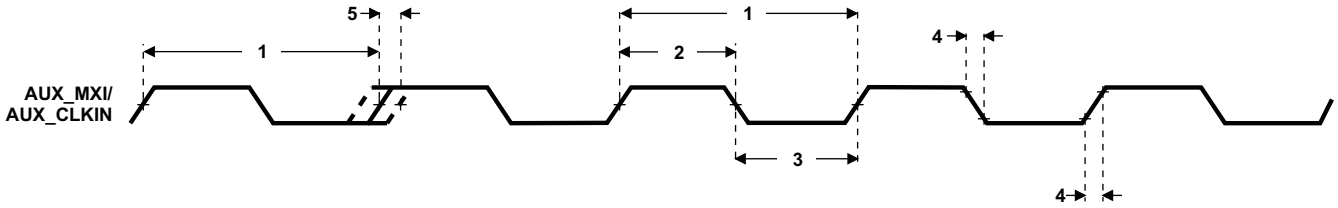


**Figure 7-16. AUX_MXI/AUX_CLKIN Timing**


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**Table 7-14. Switching Characteristics Over Recommended Operating Conditions for CLKOUT0 (1) (2) (see Figure 7-17)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(CLKOUT0)}$ | Cycle time, CLKOUT0 | 6.734 | 296.$\overline{296}$ | ns |
| 2 | $t_{w(CLKOUT0H)}$ | Pulse duration, CLKOUT0 high | 0.4P | 0.6P | ns |
| 3 | $t_{w(CLKOUT0L)}$ | Pulse duration, CLKOUT0 low | 0.4P | 0.6P | ns |
| 4 | $t_{t(CLKOUT0)}$ | Transition time, CLKOUT0 | | 0.05P | ns |

(1) The reference points for the rise and fall transitions are measured at $V_{OL}$ MAX and $V_{OH}$ MIN.
(2) P = 1/CLKOUT0 clock frequency in nanoseconds (ns). For example, when CLKOUT0 frequency is 33.3 MHz, use P = 30.03 ns.

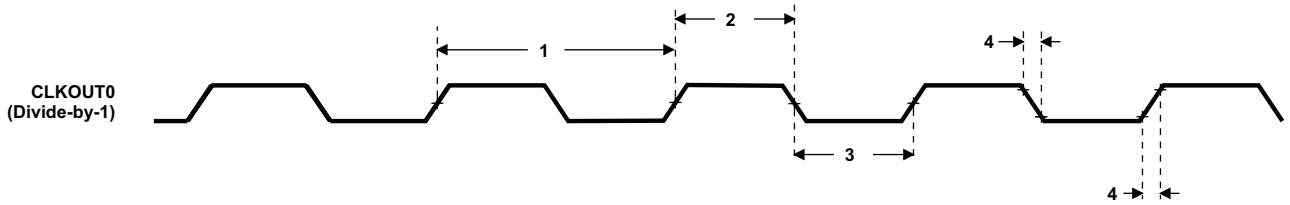


**Figure 7-17. CLKOUT0 Timing**

## 7.6 Enhanced Direct Memory Access (EDMA3) Controller

The EDMA controller handles all data transfers between memories and the device slave peripherals on the DM6467T device. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses. These are summarized as follows:

- Transfer to/from on-chip memories
  - ARM926 TCM
  - DSP L1D memory
  - DSP L2 memory
- Transfer to/from external storage
  - DDR2 SDRAM
  - NAND flash
  - Asynchronous EMIF (EMIFA)
  - ATA
- Transfer to/from peripherals/hosts
  - VLYNQ
  - HPI
  - McASP0/1
  - SPI
  - I2C
  - PWM0/1
  - UART0/1/2
  - PCI

The EDMA supports two addressing modes: constant addressing and increment addressing. On the DM6467T, constant addressing mode is **not** supported by any peripheral or internal memory. For more information on these two addressing modes, see the *TMS320DM646x DMSoC Enhanced Direct Memory Access (EDMA) Controller* User's Guide (literature number SPRUEQ5).

The DM6467T device supports a programmable default burst size feature. The default burst size of each EDMA3 Transfer Controller (TC) is configured via the EDMA Transfer Controller Default Burst Size Configuration register (EDMATCCFG). For more detailed information on the EDMATCCFG register, see Section 4.6.2, *Peripheral Selection After Device Reset*.

### 7.6.1 EDMA3 Channel Synchronization Events

The EDMA supports up to 64 EDMA channels which service peripheral devices and external memory. Table 7-15 lists the source of EDMA synchronization events associated with each of the programmable EDMA channels. For the DM6467T device, the association of an event to a channel is fixed; each of the EDMA channels has one specific event associated with it. These specific events are captured in the EDMA event registers (ER, ERH) even if the events are disabled by the EDMA event enable registers (EER, EERH). For more detailed information on the EDMA module and how EDMA events are enabled, captured, processed, linked, chained, and cleared, etc., see the *TMS320DM646x DMSoC Enhanced Direct Memory Access (EDMA) Controller* User's Guide (literature number SPRUEQ5)

**Table 7-15. DM6467T EDMA Channel Synchronization Events(1)**

| EDMA CHANNEL | EVENT NAME | EVENT DESCRIPTION |
|---|---|---|
| 0-3 | – | Reserved |

(1) In addition to the events shown in this table, each of the 64 channels can also be synchronized with the transfer completion or alternate transfer completion events. For more detailed information on EDMA event-transfer chaining, see the *TMS320DM646x DMSoC Enhanced Direct Memory Access (EDMA) Controller* User's Guide (literature number SPRUEQ5).


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**Table 7-15. DM6467T EDMA Channel Synchronization Events[1] (continued)**

| EDMA CHANNEL | EVENT NAME | EVENT DESCRIPTION |
|---|---|---|
| 4 | AXEVTE0 | McASP0 Transmit Event Even |
| 5 | AXEVTO0 | McASP0 Transmit Event Odd |
| 6 | AXEVT0 | McASP0 Transmit Event |
| 7 | AREVTE0 | McASP0 Receive Event Even |
| 8 | AREVTO0 | McASP0 Receive Event Odd |
| 9 | AREVT0 | McASP0 Receive Event |
| 10 | AXEVTE1 | McASP1 Transmit Event Even |
| 11 | AXEVTO1 | McASP1 Transmit Event Odd |
| 12 | AXEVT1 | McASP1 Transmit Event |
| 13-15 | – | Reserved |
| 16 | SPIXEVT | SPI Transmit Event |
| 17 | SPIREVT | SPI Receive Event |
| 18 | URXEVT0 | UART 0 Receive Event |
| 19 | UTXEVT0 | UART 0 Transmit Event |
| 20 | URXEVT1 | UART 1 Receive Event |
| 21 | UTXEVT1 | UART 1 Transmit Event |
| 22 | URXEVT2 | UART 2 Receive Event |
| 23 | UTXEVT2 | UART 2 Transmit Event |
| 24-27 | – | Reserved |
| 28 | ICREVT | I2C Receive Event |
| 29 | ICXEVT | I2C Transmit Event |
| 30-31 | – | Reserved [Unused] |
| 32 | GPINT0 | GPIO 0 Interrupt Event |
| 33 | GPINT1 | GPIO 1 Interrupt Event |
| 34 | GPINT2 | GPIO 2 Interrupt Event |
| 35 | GPINT3 | GPIO 3 Interrupt Event |
| 36 | GPINT4 | GPIO 4 Interrupt Event |
| 37 | GPINT5 | GPIO 5 Interrupt Event |
| 38 | GPINT6 | GPIO 6 Interrupt Event |
| 39 | GPINT7 | GPIO 7 Interrupt Event |
| 40 | GPBNKINT0 | GPIO Bank 0 Interrupt Event |
| 41 | GPBNKINT1 | GPIO Bank 1 Interrupt Event |
| 42 | GPBNKINT2 | GPIO Bank 2 Interrupt Event |
| 43 | CP_ECDCMP1 | HDVICP1 ECDCMP Interrupt Event |
| 44 | CP_MC1 | HDVICP1 MC Interrupt Event |
| 45 | CP_BS1 | HDVICP1 BS Interrupt Event |
| 46 | CP_CALC1 | HDVICP1 CALC Interrupt Event |
| 47 | CP_LPF1 | HDVICP1 LPF Interrupt Event |
| 48 | TEVTL0 | Timer 0 Event Low Interrupt |
| 49 | TEVTH0 | Timer 0 Event High Interrupt |
| 50 | TEVTL1 | Timer 1 Event Low Interrupt |
| 51 | TEVTH1 | Timer 1 Event High Interrupt |
| 52 | PWM0 | PWM 0 Interrupt Event |
| 53 | PWM1 | PWM 1 Interrupt Event |
| 54-56 | – | Reserved |
| 57 | CP_ME0 | HDVICP0 ME Interrupt Event |
| 58 | CP_IPE0 | HDVICP0 IPE Interrupt Event |

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**Table 7-15. DM6467T EDMA Channel Synchronization Events[(1)] (continued)**

| EDMA CHANNEL | EVENT NAME | EVENT DESCRIPTION |
|---|---|---|
| 59 | CP_ECDCMP0 | HDVICP0 ECDCMP Interrupt Event |
| 60 | CP_MC0 | HDVICP0 MC Interrupt Event |
| 61 | CP_BS0 | HDVICP0 BS Interrupt Event |
| 62 | CP_CALC0 | HDVICP0 CALC Interrupt Event |
| 63 | CP_LPF0 | HDVICP0 LPF Interrupt Event |


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### 7.6.2 EDMA Peripheral Register Description(s)

Table 7-16 lists the EDMA registers, their corresponding acronyms, and DM6467T device memory locations.

**Table 7-16. DM6467T EDMA Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| **Channel Controller Registers** | | |
| 0x01C0 0000 | PID | Peripheral Identification Register |
| 0x01C0 0004 | CCCFG | EDMA3CC Configuration Register |
| 0x01C0 0008 - 0x01C0 00FF | – | Reserved |
| **Global Registers** | | |
| 0x01C0 0100 | DCHMAP0 | DMA Channel 0 Mapping to PaRAM Register |
| 0x01C0 0104 | DCHMAP1 | DMA Channel 1 Mapping to PaRAM Register |
| 0x01C0 0108 | DCHMAP2 | DMA Channel 2 Mapping to PaRAM Register |
| 0x01C0 010C | DCHMAP3 | DMA Channel 3 Mapping to PaRAM Register |
| 0x01C0 0110 | DCHMAP4 | DMA Channel 4 Mapping to PaRAM Register |
| 0x01C0 0114 | DCHMAP5 | DMA Channel 5 Mapping to PaRAM Register |
| 0x01C0 0118 | DCHMAP6 | DMA Channel 6 Mapping to PaRAM Register |
| 0x01C0 011C | DCHMAP7 | DMA Channel 7 Mapping to PaRAM Register |
| 0x01C0 0120 | DCHMAP8 | DMA Channel 8 Mapping to PaRAM Register |
| 0x01C0 0124 | DCHMAP9 | DMA Channel 9 Mapping to PaRAM Register |
| 0x01C0 0128 | DCHMAP10 | DMA Channel 10 Mapping to PaRAM Register |
| 0x01C0 012C | DCHMAP11 | DMA Channel 11 Mapping to PaRAM Register |
| 0x01C0 0130 | DCHMAP12 | DMA Channel 12 Mapping to PaRAM Register |
| 0x01C0 0134 | DCHMAP13 | DMA Channel 13 Mapping to PaRAM Register |
| 0x01C0 0138 | DCHMAP14 | DMA Channel 14 Mapping to PaRAM Register |
| 0x01C0 013C | DCHMAP15 | DMA Channel 15 Mapping to PaRAM Register |
| 0x01C0 0140 | DCHMAP16 | DMA Channel 16 Mapping to PaRAM Register |
| 0x01C0 0144 | DCHMAP17 | DMA Channel 17 Mapping to PaRAM Register |
| 0x01C0 0148 | DCHMAP18 | DMA Channel 18 Mapping to PaRAM Register |
| 0x01C0 014C | DCHMAP19 | DMA Channel 19 Mapping to PaRAM Register |
| 0x01C0 0150 | DCHMAP20 | DMA Channel 20 Mapping to PaRAM Register |
| 0x01C0 0154 | DCHMAP21 | DMA Channel 21 Mapping to PaRAM Register |
| 0x01C0 0158 | DCHMAP22 | DMA Channel 22 Mapping to PaRAM Register |
| 0x01C0 015C | DCHMAP23 | DMA Channel 23 Mapping to PaRAM Register |
| 0x01C0 0160 | DCHMAP24 | DMA Channel 24 Mapping to PaRAM Register |
| 0x01C0 0164 | DCHMAP25 | DMA Channel 25 Mapping to PaRAM Register |
| 0x01C0 0168 | DCHMAP26 | DMA Channel 26 Mapping to PaRAM Register |
| 0x01C0 016C | DCHMAP27 | DMA Channel 27 Mapping to PaRAM Register |
| 0x01C0 0170 | DCHMAP28 | DMA Channel 28 Mapping to PaRAM Register |
| 0x01C0 0174 | DCHMAP29 | DMA Channel 29 Mapping to PaRAM Register |
| 0x01C0 0178 | DCHMAP30 | DMA Channel 30 Mapping to PaRAM Register |
| 0x01C0 017C | DCHMAP31 | DMA Channel 31 Mapping to PaRAM Register |
| 0x01C0 0180 | DCHMAP32 | DMA Channel 32 Mapping to PaRAM Register |
| 0x01C0 0184 | DCHMAP33 | DMA Channel 33 Mapping to PaRAM Register |
| 0x01C0 0188 | DCHMAP34 | DMA Channel 34 Mapping to PaRAM Register |
| 0x01C0 018C | DCHMAP35 | DMA Channel 35 Mapping to PaRAM Register |
| 0x01C0 0190 | DCHMAP36 | DMA Channel 36 Mapping to PaRAM Register |
| 0x01C0 0194 | DCHMAP37 | DMA Channel 37 Mapping to PaRAM Register |

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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 0198 | DCHMAP38 | DMA Channel 38 Mapping to PaRAM Register |
| 0x01C0 019C | DCHMAP39 | DMA Channel 39 Mapping to PaRAM Register |
| 0x01C0 01A0 | DCHMAP40 | DMA Channel 40 Mapping to PaRAM Register |
| 0x01C0 01A4 | DCHMAP41 | DMA Channel 41 Mapping to PaRAM Register |
| 0x01C0 01A8 | DCHMAP42 | DMA Channel 42 Mapping to PaRAM Register |
| 0x01C0 01AC | DCHMAP43 | DMA Channel 43 Mapping to PaRAM Register |
| 0x01C0 01B0 | DCHMAP44 | DMA Channel 44 Mapping to PaRAM Register |
| 0x01C0 01B4 | DCHMAP45 | DMA Channel 45 Mapping to PaRAM Register |
| 0x01C0 01B8 | DCHMAP46 | DMA Channel 46 Mapping to PaRAM Register |
| 0x01C0 01BC | DCHMAP47 | DMA Channel 47 Mapping to PaRAM Register |
| 0x01C0 01C0 | DCHMAP48 | DMA Channel 48 Mapping to PaRAM Register |
| 0x01C0 01C4 | DCHMAP49 | DMA Channel 49 Mapping to PaRAM Register |
| 0x01C0 01C8 | DCHMAP50 | DMA Channel 50 Mapping to PaRAM Register |
| 0x01C0 01CC | DCHMAP51 | DMA Channel 51 Mapping to PaRAM Register |
| 0x01C0 01D0 | DCHMAP52 | DMA Channel 52 Mapping to PaRAM Register |
| 0x01C0 01D4 | DCHMAP53 | DMA Channel 53 Mapping to PaRAM Register |
| 0x01C0 01D8 | DCHMAP54 | DMA Channel 54 Mapping to PaRAM Register |
| 0x01C0 01DC | DCHMAP55 | DMA Channel 55 Mapping to PaRAM Register |
| 0x01C0 01E0 | DCHMAP56 | DMA Channel 56 Mapping to PaRAM Register |
| 0x01C0 01E4 | DCHMAP57 | DMA Channel 57 Mapping to PaRAM Register |
| 0x01C0 01E8 | DCHMAP58 | DMA Channel 58 Mapping to PaRAM Register |
| 0x01C0 01EC | DCHMAP59 | DMA Channel 59 Mapping to PaRAM Register |
| 0x01C0 01F0 | DCHMAP60 | DMA Channel 60 Mapping to PaRAM Register |
| 0x01C0 01F4 | DCHMAP61 | DMA Channel 61 Mapping to PaRAM Register |
| 0x01C0 01F8 | DCHMAP62 | DMA Channel 62 Mapping to PaRAM Register |
| 0x01C0 01FC | DCHMAP63 | DMA Channel 63 Mapping to PaRAM Register |
| 0x01C0 0200 | QCHMAP0 | QDMA Channel 0 Mapping to PaRAM Register |
| 0x01C0 0204 | QCHMAP1 | QDMA Channel 1 Mapping to PaRAM Register |
| 0x01C0 0208 | QCHMAP2 | QDMA Channel 2 Mapping to PaRAM Register |
| 0x01C0 020C | QCHMAP3 | QDMA Channel 3 Mapping to PaRAM Register |
| 0x01C0 0210 | QCHMAP4 | QDMA Channel 4 Mapping to PaRAM Register |
| 0x01C0 0214 | QCHMAP5 | QDMA Channel 5 Mapping to PaRAM Register |
| 0x01C0 0218 | QCHMAP6 | QDMA Channel 6 Mapping to PaRAM Register |
| 0x01C0 021C | QCHMAP7 | QDMA Channel 7 Mapping to PaRAM Register |
| 0x01C0 0220 - 0x01C0 023F | – | Reserved |
| 0x01C0 0240 | DMAQNUM0 | DMA Queue Number Register 0 (Channels 00 to 07) |
| 0x01C0 0244 | DMAQNUM1 | DMA Queue Number Register 1 (Channels 08 to 15) |
| 0x01C0 0248 | DMAQNUM2 | DMA Queue Number Register 2 (Channels 16 to 23) |
| 0x01C0 024C | DMAQNUM3 | DMA Queue Number Register 3 (Channels 24 to 31) |
| 0x01C0 0250 | DMAQNUM4 | DMA Queue Number Register 4 (Channels 32 to 39) |
| 0x01C0 0254 | DMAQNUM5 | DMA Queue Number Register 5 (Channels 40 to 47) |
| 0x01C0 0258 | DMAQNUM6 | DMA Queue Number Register 6 (Channels 48 to 55) |
| 0x01C0 025C | DMAQNUM7 | DMA Queue Number Register 7 (Channels 56 to 63) |
| 0x01C0 0260 | QDMAQNUM | CC QDMA Queue Number |
| 0x01C0 0264 - 0x01C0 0283 | – | Reserved |
| 0x01C0 0284 | QUEPRI | Queue Priority Register |
| 0x01C0 0288 - 0x01C0 02FF | – | Reserved |


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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 0300 | EMR | Event Missed Register |
| 0x01C0 0304 | EMRH | Event Missed Register High |
| 0x01C0 0308 | EMCR | Event Missed Clear Register |
| 0x01C0 030C | EMCRH | Event Missed Clear Register High |
| 0x01C0 0310 | QEMR | QDMA Event Missed Register |
| 0x01C0 0314 | QEMCR | QDMA Event Missed Clear Register |
| 0x01C0 0318 | CCERR | EDMA3CC Error Register |
| 0x01C0 031C | CCERRCLR | EDMA3CC Error Clear Register |
| 0x01C0 0320 | EEVAL | Error Evaluate Register |
| 0x01C0 0324 - 0x01C0 033F | – | Reserved |
| 0x01C0 0340 | DRAE0 | DMA Region Access Enable Register for Region 0 |
| 0x01C0 0344 | DRAEH0 | DMA Region Access Enable Register High for Region 0 |
| 0x01C0 0348 | DRAE1 | DMA Region Access Enable Register for Region 1 |
| 0x01C0 034C | DRAEH1 | DMA Region Access Enable Register High for Region 1 |
| 0x01C0 0350- 0x01C0 035F | – | Reserved |
| 0x01C0 0360 | DRAE4 | DMA Region Access Enable Register for Region 4 |
| 0x01C0 0364 | DRAEH4 | DMA Region Access Enable Register High for Region 4 |
| 0x01C0 0368 | DRAE5 | DMA Region Access Enable Register for Region 5 |
| 0x01C0 036C | DRAEH5 | DMA Region Access Enable Register High for Region 5 |
| 0x01C0 0370 | DRAE6 | DMA Region Access Enable Register for Region 6 |
| 0x01C0 0374 | DRAEH6 | DMA Region Access Enable Register High for Region 6 |
| 0x01C0 0378 | DRAE7 | DMA Region Access Enable Register for Region 7 |
| 0x01C0 037C | DRAEH7 | DMA Region Access Enable Register High for Region 7 |
| 0x01C0 0380 | QRAE0 | QDMA Region Access Enable Register for Region 0 |
| 0x01C0 0384 | QRAE1 | QDMA Region Access Enable Register for Region 1 |
| 0x01C0 0388 - 0x01C0 038F | – | Reserved |
| 0x01C0 0390 | QRAE4 | QDMA Region Access Enable Register for Region 4 |
| 0x01C0 0394 | QRAE5 | QDMA Region Access Enable Register for Region 5 |
| 0x01C0 0398 | QRAE6 | QDMA Region Access Enable Register for Region 6 |
| 0x01C0 039C | QRAE7 | QDMA Region Access Enable Register for Region 7 |
| 0x01C0 03A0 - 0x01C0 03FF | – | Reserved |
| 0x01C0 0400 | Q0E0 | Event Q0 Entry 0 Register |
| 0x01C0 0404 | Q0E1 | Event Q0 Entry 1 Register |
| 0x01C0 0408 | Q0E2 | Event Q0 Entry 2 Register |
| 0x01C0 040C | Q0E3 | Event Q0 Entry 3 Register |
| 0x01C0 0410 | Q0E4 | Event Q0 Entry 4 Register |
| 0x01C0 0414 | Q0E5 | Event Q0 Entry 5 Register |
| 0x01C0 0418 | Q0E6 | Event Q0 Entry 6 Register |
| 0x01C0 041C | Q0E7 | Event Q0 Entry 7 Register |
| 0x01C0 0420 | Q0E8 | Event Q0 Entry 8 Register |
| 0x01C0 0424 | Q0E9 | Event Q0 Entry 9 Register |
| 0x01C0 0428 | Q0E10 | Event Q0 Entry 10 Register |
| 0x01C0 042C | Q0E11 | Event Q0 Entry 11 Register |
| 0x01C0 0430 | Q0E12 | Event Q0 Entry 12 Register |
| 0x01C0 0434 | Q0E13 | Event Q0 Entry 13 Register |
| 0x01C0 0438 | Q0E14 | Event Q0 Entry 14 Register |
| 0x01C0 043C | Q0E15 | Event Q0 Entry 15 Register |

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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 0440 | Q1E0 | Event Q1 Entry 0 Register |
| 0x01C0 0444 | Q1E1 | Event Q1 Entry 1 Register |
| 0x01C0 0448 | Q1E2 | Event Q1 Entry 2 Register |
| 0x01C0 044C | Q1E3 | Event Q1 Entry 3 Register |
| 0x01C0 0450 | Q1E4 | Event Q1 Entry 4 Register |
| 0x01C0 0454 | Q1E5 | Event Q1 Entry 5 Register |
| 0x01C0 0458 | Q1E6 | Event Q1 Entry 6 Register |
| 0x01C0 045C | Q1E7 | Event Q1 Entry 7 Register |
| 0x01C0 0460 | Q1E8 | Event Q1 Entry 8 Register |
| 0x01C0 0464 | Q1E9 | Event Q1 Entry 9 Register |
| 0x01C0 0468 | Q1E10 | Event Q1 Entry 10 Register |
| 0x01C0 046C | Q1E11 | Event Q1 Entry 11 Register |
| 0x01C0 0470 | Q1E12 | Event Q1 Entry 12 Register |
| 0x01C0 0474 | Q1E13 | Event Q1 Entry 13 Register |
| 0x01C0 0478 | Q1E14 | Event Q1 Entry 14 Register |
| 0x01C0 047C | Q1E15 | Event Q1 Entry 15 Register |
| 0x01C0 0480 | Q2E0 | Event Q2 Entry 0 Register |
| 0x01C0 0484 | Q2E1 | Event Q2 Entry 1 Register |
| 0x01C0 0488 | Q2E2 | Event Q2 Entry 2 Register |
| 0x01C0 048C | Q2E3 | Event Q2 Entry 3 Register |
| 0x01C0 0490 | Q2E4 | Event Q2 Entry 4 Register |
| 0x01C0 0494 | Q2E5 | Event Q2 Entry 5 Register |
| 0x01C0 0498 | Q2E6 | Event Q2 Entry 6 Register |
| 0x01C0 049C | Q2E7 | Event Q2 Entry 7 Register |
| 0x01C0 04A0 | Q2E8 | Event Q2 Entry 8 Register |
| 0x01C0 04A4 | Q2E9 | Event Q2 Entry 9 Register |
| 0x01C0 04A8 | Q2E10 | Event Q2 Entry 10 Register |
| 0x01C0 04AC | Q2E11 | Event Q2 Entry 11 Register |
| 0x01C0 04B0 | Q2E12 | Event Q2 Entry 12 Register |
| 0x01C0 04B4 | Q2E13 | Event Q2 Entry 13 Register |
| 0x01C0 04B8 | Q2E14 | Event Q2 Entry 14 Register |
| 0x01C0 04BC | Q2E15 | Event Q2 Entry 15 Register |
| 0x01C0 04C0 | Q3E0 | Event Q3 Entry 0 Register |
| 0x01C0 04C4 | Q3E1 | Event Q3 Entry 1 Register |
| 0x01C0 04C8 | Q3E2 | Event Q3 Entry 2 Register |
| 0x01C0 04CC | Q3E3 | Event Q3 Entry 3 Register |
| 0x01C0 04D0 | Q3E4 | Event Q3 Entry 4 Register |
| 0x01C0 04D4 | Q3E5 | Event Q3 Entry 5 Register |
| 0x01C0 04D8 | Q3E6 | Event Q3 Entry 6 Register |
| 0x01C0 04DC | Q3E7 | Event Q3 Entry 7 Register |
| 0x01C0 04E0 | Q3E8 | Event Q3 Entry 8 Register |
| 0x01C0 04E4 | Q3E9 | Event Q3 Entry 9 Register |
| 0x01C0 04E8 | Q3E10 | Event Q3 Entry 10 Register |
| 0x01C0 04EC | Q3E11 | Event Q3 Entry 11 Register |
| 0x01C0 04F0 | Q3E12 | Event Q3 Entry 12 Register |
| 0x01C0 04F4 | Q3E13 | Event Q3 Entry 13 Register |
| 0x01C0 04F8 | Q3E14 | Event Q3 Entry 14 Register |


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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 04FC | Q3E15 | Event Q3 Entry 15 Register |
| 0x01C0 0500 - 0x01C0 05FF | – | Reserved |
| 0x01C0 0600 | QSTAT0 | Queue 0 Status Register |
| 0x01C0 0604 | QSTAT1 | Queue 1 Status Register |
| 0x01C0 0608 | QSTAT2 | Queue 2 Status Register |
| 0x01C0 060C | QSTAT3 | Queue 3 Status Register |
| 0x01C0 0610 - 0x01C0 061F | – | Reserved |
| 0x01C0 0620 | QWMTHRA | Queue Watermark Threshold A Register for Q[3:0] |
| 0x01C0 0624 - 0x01C0 063F | – | Reserved |
| 0x01C0 0640 | CCSTAT | EDMA3CC Status Register |
| 0x01C0 0644 - 0x01C0 0FFF | – | Reserved |
| **Global Channel Registers** | | |
| 0x01C0 1000 | ER | Event Register |
| 0x01C0 1004 | ERH | Event Register High |
| 0x01C0 1008 | ECR | Event Clear Register |
| 0x01C0 100C | ECRH | Event Clear Register High |
| 0x01C0 1010 | ESR | Event Set Register |
| 0x01C0 1014 | ESRH | Event Set Register High |
| 0x01C0 1018 | CER | Chained Event Register |
| 0x01C0 101C | CERH | Chained Event Register High |
| 0x01C0 1020 | EER | Event Enable Register |
| 0x01C0 1024 | EERH | Event Enable Register High |
| 0x01C0 1028 | EECR | Event Enable Clear Register |
| 0x01C0 102C | EECRH | Event Enable Clear Register High |
| 0x01C0 1030 | EESR | Event Enable Set Register |
| 0x01C0 1034 | EESRH | Event Enable Set Register High |
| 0x01C0 1038 | SER | Secondary Event Register |
| 0x01C0 103C | SERH | Secondary Event Register High |
| 0x01C0 1040 | SECR | Secondary Event Clear Register |
| 0x01C0 1044 | SECRH | Secondary Event Clear Register High |
| 0x01C0 1048 - 0x01C0 104F | – | Reserved |
| 0x01C0 1050 | IER | Interrupt Enable Register |
| 0x01C0 1054 | IERH | Interrupt Enable Register High |
| 0x01C0 1058 | IECR | Interrupt Enable Clear Register |
| 0x01C0 105C | IECRH | Interrupt Enable Clear Register High |
| 0x01C0 1060 | IESR | Interrupt Enable Set Register |
| 0x01C0 1064 | IESRH | Interrupt Enable Set Register High |
| 0x01C0 1068 | IPR | Interrupt Pending Register |
| 0x01C0 106C | IPRH | Interrupt Pending Register High |
| 0x01C0 1070 | ICR | Interrupt Clear Register |
| 0x01C0 1074 | ICRH | Interrupt Clear Register High |
| 0x01C0 1078 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 107C - 0x01C0 107F | – | Reserved |
| 0x01C0 1080 | QER | QDMA Event Register |
| 0x01C0 1084 | QEER | QDMA Event Enable Register |
| 0x01C0 1088 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 108C | QEESR | QDMA Event Enable Set Register |

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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 1090 | QSER | QDMA Secondary Event Register |
| 0x01C0 1094 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 1098 - 0x01C0 1FFF | – | Reserved |
| **Shadow Region 0 Channel Registers** | | |
| 0x01C0 2000 | ER | Event Register |
| 0x01C0 2004 | ERH | Event Register High |
| 0x01C0 2008 | ECR | Event Clear Register |
| 0x01C0 200C | ECRH | Event Clear Register High |
| 0x01C0 2010 | ESR | Event Set Register |
| 0x01C0 2014 | ESRH | Event Set Register High |
| 0x01C0 2018 | CER | Chained Event Register |
| 0x01C0 201C | CERH | Chained Event Register High |
| 0x01C0 2020 | EER | Event Enable Register |
| 0x01C0 2024 | EERH | Event Enable Register High |
| 0x01C0 2028 | EECR | Event Enable Clear Register |
| 0x01C0 202C | EECRH | Event Enable Clear Register High |
| 0x01C0 2030 | EESR | Event Enable Set Register |
| 0x01C0 2034 | EESRH | Event Enable Set Register High |
| 0x01C0 2038 | SER | Secondary Event Register |
| 0x01C0 203C | SERH | Secondary Event Register High |
| 0x01C0 2040 | SECR | Secondary Event Clear Register |
| 0x01C0 2044 | SECRH | Secondary Event Clear Register High |
| 0x01C0 2048 - 0x01C0 204F | – | Reserved |
| 0x01C0 2050 | IER | Interrupt Enable Register |
| 0x01C0 2054 | IERH | Interrupt Enable Register High |
| 0x01C0 2058 | IECR | Interrupt Enable Clear Register |
| 0x01C0 205C | IECRH | Interrupt Enable Clear Register High |
| 0x01C0 2060 | IESR | Interrupt Enable Set Register |
| 0x01C0 2064 | IESRH | Interrupt Enable Set Register High |
| 0x01C0 2068 | IPR | Interrupt Pending Register |
| 0x01C0 206C | IPRH | Interrupt Pending Register High |
| 0x01C0 2070 | ICR | Interrupt Clear Register |
| 0x01C0 2074 | ICRH | Interrupt Clear Register High |
| 0x01C0 2078 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 207C - 0x01C0 207F | – | Reserved |
| 0x01C0 2080 | QER | QDMA Event Register |
| 0x01C0 2084 | QEER | QDMA Event Enable Register |
| 0x01C0 2088 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 208C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2090 | QSER | QDMA Secondary Event Register |
| 0x01C0 2094 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 2098 - 0x01C0 21FF | – | Reserved |
| **Shadow Region 1 Channel Registers** | | |
| 0x01C0 2200 | ER | Event Register |
| 0x01C0 2204 | ERH | Event Register High |
| 0x01C0 2208 | ECR | Event Clear Register |
| 0x01C0 220C | ECRH | Event Clear Register High |


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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 2210 | ESR | Event Set Register |
| 0x01C0 2214 | ESRH | Event Set Register High |
| 0x01C0 2218 | CER | Chained Event Register |
| 0x01C0 221C | CERH | Chained Event Register High |
| 0x01C0 2220 | EER | Event Enable Register |
| 0x01C0 2224 | EERH | Event Enable Register High |
| 0x01C0 2228 | EECR | Event Enable Clear Register |
| 0x01C0 222C | EECRH | Event Enable Clear Register High |
| 0x01C0 2230 | EESR | Event Enable Set Register |
| 0x01C0 2234 | EESRH | Event Enable Set Register High |
| 0x01C0 2238 | SER | Secondary Event Register |
| 0x01C0 223C | SERH | Secondary Event Register High |
| 0x01C0 2240 | SECR | Secondary Event Clear Register |
| 0x01C0 2244 | SECRH | Secondary Event Clear Register High |
| 0x01C0 2248 - 0x01C0 224F | – | Reserved |
| 0x01C0 2250 | IER | Interrupt Enable Register |
| 0x01C0 2254 | IERH | Interrupt Enable Register High |
| 0x01C0 2258 | IECR | Interrupt Enable Clear Register |
| 0x01C0 225C | IECRH | Interrupt Enable Clear Register High |
| 0x01C0 2260 | IESR | Interrupt Enable Set Register |
| 0x01C0 2264 | IESRH | Interrupt Enable Set Register High |
| 0x01C0 2268 | IPR | Interrupt Pending Register |
| 0x01C0 226C | IPRH | Interrupt Pending Register High |
| 0x01C0 2270 | ICR | Interrupt Clear Register |
| 0x01C0 2274 | ICRH | Interrupt Clear Register High |
| 0x01C0 2278 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 227C - 0x01C0 227F | – | Reserved |
| 0x01C0 2280 | QER | QDMA Event Register |
| 0x01C0 2284 | QEER | QDMA Event Enable Register |
| 0x01C0 2288 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 228C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2290 | QSER | QDMA Secondary Event Register |
| 0x01C0 2294 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 2298 - 0x01C0 23FF | – | Reserved |
| 0x01C0 2400 - 0x01C0 25FF | – | Reserved |
| 0x01C0 2600 - 0x01C0 27FF | – | Reserved |
| **Shadow Region 4 Channel Registers** | | |
| 0x01C0 2800 | ER | Event Register |
| 0x01C0 2804 | ERH | Event Register High |
| 0x01C0 2808 | ECR | Event Clear Register |
| 0x01C0 280C | ECRH | Event Clear Register High |
| 0x01C0 2810 | ESR | Event Set Register |
| 0x01C0 2814 | ESRH | Event Set Register High |
| 0x01C0 2818 | CER | Chained Event Register |
| 0x01C0 281C | CERH | Chained Event Register High |
| 0x01C0 2820 | EER | Event Enable Register |
| 0x01C0 2824 | EERH | Event Enable Register High |

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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 2828 | EECR | Event Enable Clear Register |
| 0x01C0 282C | EECRH | Event Enable Clear Register High |
| 0x01C0 2830 | EESR | Event Enable Set Register |
| 0x01C0 2834 | EESRH | Event Enable Set Register High |
| 0x01C0 2838 | SER | Secondary Event Register |
| 0x01C0 283C | SERH | Secondary Event Register High |
| 0x01C0 2840 | SECR | Secondary Event Clear Register |
| 0x01C0 2844 | SECRH | Secondary Event Clear Register High |
| 0x01C0 2848 - 0x01C0 284F | – | Reserved |
| 0x01C0 2850 | IER | Interrupt Enable Register |
| 0x01C0 2854 | IERH | Interrupt Enable Register High |
| 0x01C0 2858 | IECR | Interrupt Enable Clear Register |
| 0x01C0 285C | IECRH | Interrupt Enable Clear Register High |
| 0x01C0 2860 | IESR | Interrupt Enable Set Register |
| 0x01C0 2864 | IESRH | Interrupt Enable Set Register High |
| 0x01C0 2868 | IPR | Interrupt Pending Register |
| 0x01C0 286C | IPRH | Interrupt Pending Register High |
| 0x01C0 2870 | ICR | Interrupt Clear Register |
| 0x01C0 2874 | ICRH | Interrupt Clear Register High |
| 0x01C0 2878 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 287C - 0x01C0 287F | – | Reserved |
| 0x01C0 2880 | QER | QDMA Event Register |
| 0x01C0 2884 | QEER | QDMA Event Enable Register |
| 0x01C0 2888 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 288C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2890 | QSER | QDMA Secondary Event Register |
| 0x01C0 2894 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 2898 - 0x01C0 29FF | – | Reserved |
| **Shadow Region 5 Channel Registers** | | |
| 0x01C0 2A00 | ER | Event Register |
| 0x01C0 2A04 | ERH | Event Register High |
| 0x01C0 2A08 | ECR | Event Clear Register |
| 0x01C0 2A0C | ECRH | Event Clear Register High |
| 0x01C0 2A10 | ESR | Event Set Register |
| 0x01C0 2A14 | ESRH | Event Set Register High |
| 0x01C0 2A18 | CER | Chained Event Register |
| 0x01C0 2A1C | CERH | Chained Event Register High |
| 0x01C0 2A20 | EER | Event Enable Register |
| 0x01C0 2A24 | EERH | Event Enable Register High |
| 0x01C0 2A28 | EECR | Event Enable Clear Register |
| 0x01C0 2A2C | EECRH | Event Enable Clear Register High |
| 0x01C0 2A30 | EESR | Event Enable Set Register |
| 0x01C0 2A34 | EESRH | Event Enable Set Register High |
| 0x01C0 2A38 | SER | Secondary Event Register |
| 0x01C0 2A3C | SERH | Secondary Event Register High |
| 0x01C0 2A40 | SECR | Secondary Event Clear Register |
| 0x01C0 2A44 | SECRH | Secondary Event Clear Register High |


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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 2A48 - 0x01C0 2A4F | – | Reserved |
| 0x01C0 2A50 | IER | Interrupt Enable Register |
| 0x01C0 2A54 | IERH | Interrupt Enable Register High |
| 0x01C0 2A58 | IECR | Interrupt Enable Clear Register |
| 0x01C0 2A5C | IECRH | Interrupt Enable Clear Register High |
| 0x01C0 2A60 | IESR | Interrupt Enable Set Register |
| 0x01C0 2A64 | IESRH | Interrupt Enable Set Register High |
| 0x01C0 2A68 | IPR | Interrupt Pending Register |
| 0x01C0 2A6C | IPRH | Interrupt Pending Register High |
| 0x01C0 2A70 | ICR | Interrupt Clear Register |
| 0x01C0 2A74 | ICRH | Interrupt Clear Register High |
| 0x01C0 2A78 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 2A7C - 0x01C0 2A7F | – | Reserved |
| 0x01C0 2A80 | QER | QDMA Event Register |
| 0x01C0 2A84 | QEER | QDMA Event Enable Register |
| 0x01C0 2A88 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 2A8C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2A90 | QSER | QDMA Secondary Event Register |
| 0x01C0 2A94 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 2A98 - 0x01C0 2BFF | – | Reserved |
| **Shadow Region 6 Channel Registers** | | |
| 0x01C0 2C00 | ER | Event Register |
| 0x01C0 2C04 | ERH | Event Register High |
| 0x01C0 2C08 | ECR | Event Clear Register |
| 0x01C0 2C0C | ECRH | Event Clear Register High |
| 0x01C0 2C10 | ESR | Event Set Register |
| 0x01C0 2C14 | ESRH | Event Set Register High |
| 0x01C0 2C18 | CER | Chained Event Register |
| 0x01C0 2C1C | CERH | Chained Event Register High |
| 0x01C0 2C20 | EER | Event Enable Register |
| 0x01C0 2C24 | EERH | Event Enable Register High |
| 0x01C0 2C28 | EECR | Event Enable Clear Register |
| 0x01C0 2C2C | EECRH | Event Enable Clear Register High |
| 0x01C0 2C30 | EESR | Event Enable Set Register |
| 0x01C0 2C34 | EESRH | Event Enable Set Register High |
| 0x01C0 2C38 | SER | Secondary Event Register |
| 0x01C0 2C3C | SERH | Secondary Event Register High |
| 0x01C0 2C40 | SECR | Secondary Event Clear Register |
| 0x01C0 2C44 | SECRH | Secondary Event Clear Register High |
| 0x01C0 2C48 - 0x01C0 2C4F | – | Reserved |
| 0x01C0 2C50 | IER | Interrupt Enable Register |
| 0x01C0 2C54 | IERH | Interrupt Enable Register High |
| 0x01C0 2C58 | IECR | Interrupt Enable Clear Register |
| 0x01C0 2C5C | IECRH | Interrupt Enable Clear Register High |
| 0x01C0 2C60 | IESR | Interrupt Enable Set Register |
| 0x01C0 2C64 | IESRH | Interrupt Enable Set Register High |
| 0x01C0 2C68 | IPR | Interrupt Pending Register |

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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 2C6C | IPRH | Interrupt Pending Register High |
| 0x01C0 2C70 | ICR | Interrupt Clear Register |
| 0x01C0 2C74 | ICRH | Interrupt Clear Register High |
| 0x01C0 2C78 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 2C7C - 0x01C0 2C7F | – | Reserved |
| 0x01C0 2C80 | QER | QDMA Event Register |
| 0x01C0 2C84 | QEER | QDMA Event Enable Register |
| 0x01C0 2C88 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 2C8C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2C90 | QSER | QDMA Secondary Event Register |
| 0x01C0 2C94 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 2C98 - 0x01C0 2DFF | – | Reserved |
| **Shadow Region 7 Channel Registers** | | |
| 0x01C0 2E00 | ER | Event Register |
| 0x01C0 2E04 | ERH | Event Register High |
| 0x01C0 2E08 | ECR | Event Clear Register |
| 0x01C0 2E0C | ECRH | Event Clear Register High |
| 0x01C0 2E10 | ESR | Event Set Register |
| 0x01C0 2E14 | ESRH | Event Set Register High |
| 0x01C0 2E18 | CER | Chained Event Register |
| 0x01C0 2E1C | CERH | Chained Event Register High |
| 0x01C0 2E20 | EER | Event Enable Register |
| 0x01C0 2E24 | EERH | Event Enable Register High |
| 0x01C0 2E28 | EECR | Event Enable Clear Register |
| 0x01C0 2E2C | EECRH | Event Enable Clear Register High |
| 0x01C0 2E30 | EESR | Event Enable Set Register |
| 0x01C0 2E34 | EESRH | Event Enable Set Register High |
| 0x01C0 2E38 | SER | Secondary Event Register |
| 0x01C0 2E3C | SERH | Secondary Event Register High |
| 0x01C0 2E40 | SECR | Secondary Event Clear Register |
| 0x01C0 2E44 | SECRH | Secondary Event Clear Register High |
| 0x01C0 2E48 - 0x01C0 2E4F | – | Reserved |
| 0x01C0 2E50 | IER | Interrupt Enable Register |
| 0x01C0 2E54 | IERH | Interrupt Enable Register High |
| 0x01C0 2E58 | IECR | Interrupt Enable Clear Register |
| 0x01C0 2E5C | IECRH | Interrupt Enable Clear Register High |
| 0x01C0 2E60 | IESR | Interrupt Enable Set Register |
| 0x01C0 2E64 | IESRH | Interrupt Enable Set Register High |
| 0x01C0 2E68 | IPR | Interrupt Pending Register |
| 0x01C0 2E6C | IPRH | Interrupt Pending Register High |
| 0x01C0 2E70 | ICR | Interrupt Clear Register |
| 0x01C0 2E74 | ICRH | Interrupt Clear Register High |
| 0x01C0 2E78 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 2E7C - 0x01C0 2E7F | – | Reserved |
| 0x01C0 2E80 | QER | QDMA Event Register |
| 0x01C0 2E84 | QEER | QDMA Event Enable Register |
| 0x01C0 2E88 | QEECR | QDMA Event Enable Clear Register |


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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C0 2E8C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2E90 | QSER | QDMA Secondary Event Register |
| 0x01C0 2E94 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 2E98 - 0x01C0 2FFF | – | Reserved |
| 0x01C0 3000 - 0x01C0 3FFF | – | Reserved |
| 0x01C0 4000 - 0x01C0 7FFF | – | Parameter Set RAM (see Table 7-17) |
| 0x01C0 8000 - 0x01C0 FFFF | – | Reserved |
| **Transfer Controller 0 Registers** | | |
| 0x01C1 0000 | PID | Peripheral Identification Register |
| 0x01C1 0004 | TCCFG | EDMA3 TC0 Configuration Register |
| 0x01C1 0008 - 0x01C1 00FF | – | Reserved |
| 0x01C1 0100 | TCSTAT | EDMA3 TC0 Channel Status Register |
| 0x01C1 0104 - 0x01C1 0113 | – | Reserved |
| 0x01C1 0114 - 0x01C1 011F | – | Reserved |
| 0x01C1 0120 | ERRSTAT | EDMA3 TC0 Error Status Register |
| 0x01C1 0124 | ERREN | EDMA3 TC0 Error Enable Register |
| 0x01C1 0128 | ERRCLR | EDMA3 TC0 Error Clear Register |
| 0x01C1 012C | ERRDET | EDMA3 TC0 Error Details Register |
| 0x01C1 0130 | ERRCMD | EDMA3 TC0 Error Interrupt Command Register |
| 0x01C1 0134 - 0x01C1 013F | – | Reserved |
| 0x01C1 0140 | RDRATE | EDMA3 TC0 Read Command Rate Register |
| 0x01C1 0144 - 0x01C1 01FF | – | Reserved |
| 0x01C1 0200 - 0x01C1 023F | – | Reserved |
| 0x01C1 0240 | SAOPT | EDMA3 TC0 Source Active Options Register |
| 0x01C1 0244 | SASRC | EDMA3 TC0 Source Active Source Address Register |
| 0x01C1 0248 | SACNT | EDMA3 TC0 Source Active Count Register |
| 0x01C1 024C | SADST | EDMA3 TC0 Source Active Destination Address Register |
| 0x01C1 0250 | SABIDX | EDMA3 TC0 Source Active B-Index Register |
| 0x01C1 0254 | SAMPPRXY | EDMA3 TC0 Source Active Memory Protection Proxy Register |
| 0x01C1 0258 | SACNTRLD | EDMA3 TC0 Source Active Count Reload Register |
| 0x01C1 025C | SASRCBREF | EDMA3 TC0 Source Active Source Address B-Reference Register |
| 0x01C1 0260 | SADSTBREF | EDMA3 TC0 Source Active Destination Address B-Reference Register |
| 0x01C1 0264 - 0x01C1 027F | – | Reserved |
| 0x01C1 0280 | DFCNTRLD | EDMA3 TC0 Destination FIFO Set Count Reload Register |
| 0x01C1 0284 | DFSRCBREF | EDMA3 TC0 Destination FIFO Set Source Address B-Reference Register |
| 0x01C1 0288 | DFDSTBREF | EDMA3 TC0 Destination FIFO Set Destination Address B-Reference Register |
| 0x01C1 028C - 0x01C1 02FF | – | Reserved |
| 0x01C1 0300 | DFOPT0 | EDMA3 TC0 Destination FIFO Options Register 0 |
| 0x01C1 0304 | DFSRC0 | EDMA3 TC0 Destination FIFO Source Address Register 0 |
| 0x01C1 0308 | DFCNT0 | EDMA3 TC0 Destination FIFO Count Register 0 |
| 0x01C1 030C | DFDST0 | EDMA3 TC0 Destination FIFO Destination Address Register 0 |
| 0x01C1 0310 | DFBIDX0 | EDMA3 TC0 Destination FIFO B-Index Register 0 |
| 0x01C1 0314 | DFMPPRXY0 | EDMA3 TC0 Destination FIFO Memory Protection Proxy Register 0 |
| 0x01C1 0318 - 0x01C1 033F | – | Reserved |
| 0x01C1 0340 | DFOPT1 | EDMA3 TC0 Destination FIFO Options Register 1 |
| 0x01C1 0344 | DFSRC1 | EDMA3 TC0 Destination FIFO Source Address Register 1 |
| 0x01C1 0348 | DFCNT1 | EDMA3 TC0 Destination FIFO Count Register 1 |

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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 034C | DFDST1 | EDMA3 TC0 Destination FIFO Destination Address Register 1 |
| 0x01C1 0350 | DFBIDX1 | EDMA3 TC0 Destination FIFO B-Index Register 1 |
| 0x01C1 0354 | DFMPPRXY1 | EDMA3 TC0 Destination FIFO Memory Protection Proxy Register 1 |
| 0x01C1 0358 - 0x01C1 037F | – | Reserved |
| 0x01C1 0380 | DFOPT2 | EDMA3 TC0 Destination FIFO Options Register 2 |
| 0x01C1 0384 | DFSRC2 | EDMA3 TC0 Destination FIFO Source Address Register 2 |
| 0x01C1 0388 | DFCNT2 | EDMA3 TC0 Destination FIFO Count Register 2 |
| 0x01C1 038C | DFDST2 | EDMA3 TC0 Destination FIFO Destination Address Register 2 |
| 0x01C1 0390 | DFBIDX2 | EDMA3 TC0 Destination FIFO B-Index Register 2 |
| 0x01C1 0394 | DFMPPRXY2 | EDMA3 TC0 Destination FIFO Memory Protection Proxy Register 2 |
| 0x01C1 0398 - 0x01C1 03BF | – | Reserved |
| 0x01C1 03C0 | DFOPT3 | EDMA3 TC0 Destination FIFO Options Register 3 |
| 0x01C1 03C4 | DFSRC3 | EDMA3 TC0 Destination FIFO Source Address Register 3 |
| 0x01C1 03C8 | DFCNT3 | EDMA3 TC0 Destination FIFO Count Register 3 |
| 0x01C1 03CC | DFDST3 | EDMA3 TC0 Destination FIFO Destination Address Register 3 |
| 0x01C1 03D0 | DFBIDX3 | EDMA3 TC0 Destination FIFO B-Index Register 3 |
| 0x01C1 03D4 | DFMPPRXY3 | EDMA3 TC0 Destination FIFO Memory Protection Proxy Register 3 |
| 0x01C1 03D8 - 0x01C1 03FF | – | Reserved |
| **Transfer Controller 1 Registers** | | |
| 0x01C1 0400 | PID | Peripheral Identification Register |
| 0x01C1 0404 | TCCFG | EDMA3 TC1 Configuration Register |
| 0x01C1 0408 - 0x01C1 04FF | – | Reserved |
| 0x01C1 0500 | TCSTAT | EDMA3 TC1 Channel Status Register |
| 0x01C1 0504 - 0x01C1 0513 | – | Reserved |
| 0x01C1 0514 - 0x01C1 051F | – | Reserved |
| 0x01C1 0520 | ERRSTAT | EDMA3 TC1 Error Status Register |
| 0x01C1 0524 | ERREN | EDMA3 TC1 Error Enable Register |
| 0x01C1 0528 | ERRCLR | EDMA3 TC1 Error Clear Register |
| 0x01C1 052C | ERRDET | EDMA3 TC1 Error Details Register |
| 0x01C1 0530 | ERRCMD | EDMA3 TC1 Error Interrupt Command Register |
| 0x01C1 0534 - 0x01C1 053F | – | Reserved |
| 0x01C1 0540 | RDRATE | EDMA3 TC1 Read Command Rate Register |
| 0x01C1 0544 - 0x01C1 05FF | – | Reserved |
| 0x01C1 0600 - 0x01C1 063F | – | Reserved |
| 0x01C1 0640 | SAOPT | EDMA3 TC1 Source Active Options Register |
| 0x01C1 0644 | SASRC | EDMA3 TC1 Source Active Source Address Register |
| 0x01C1 0648 | SACNT | EDMA3 TC1 Source Active Count Register |
| 0x01C1 064C | SADST | EDMA3 TC1 Source Active Destination Address Register |
| 0x01C1 0650 | SABIDX | EDMA3 TC1 Source Active B-Index Register |
| 0x01C1 0654 | SAMPPRXY | EDMA3 TC1 Source Active Memory Protection Proxy Register |
| 0x01C1 0658 | SACNTRLD | EDMA3 TC1 Source Active Count Reload Register |
| 0x01C1 065C | SASRCBREF | EDMA3 TC1 Source Active Source Address B-Reference Register |
| 0x01C1 0660 | SADSTBREF | EDMA3 TC1 Source Active Destination Address B-Reference Register |
| 0x01C1 0664 - 0x01C1 067F | – | Reserved |
| 0x01C1 0680 | DFCNTRLD | EDMA3 TC1 Destination FIFO Set Count Reload Register |
| 0x01C1 0684 | DFSRCBREF | EDMA3 TC1 Destination FIFO Set Source Address B-Reference Register |
| 0x01C1 0688 | DFDSTBREF | EDMA3 TC1 Destination FIFO Set Destination Address B-Reference Register |


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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 068C - 0x01C1 06FF | – | Reserved |
| 0x01C1 0700 | DFOPT0 | EDMA3 TC1 Destination FIFO Options Register 0 |
| 0x01C1 0704 | DFSRC0 | EDMA3 TC1 Destination FIFO Source Address Register 0 |
| 0x01C1 0708 | DFCNT0 | EDMA3 TC1 Destination FIFO Count Register 0 |
| 0x01C1 070C | DFDST0 | EDMA3 TC1 Destination FIFO Destination Address Register 0 |
| 0x01C1 0710 | DFBIDX0 | EDMA3 TC1 Destination FIFO B-Index Register 0 |
| 0x01C1 0714 | DFMPPRXY0 | EDMA3 TC1 Destination FIFO Memory Protection Proxy Register 0 |
| 0x01C1 0718 - 0x01C1 073F | – | Reserved |
| 0x01C1 0740 | DFOPT1 | EDMA3 TC1 Destination FIFO Options Register 1 |
| 0x01C1 0744 | DFSRC1 | EDMA3 TC1 Destination FIFO Source Address Register 1 |
| 0x01C1 0748 | DFCNT1 | EDMA3 TC1 Destination FIFO Count Register 1 |
| 0x01C1 074C | DFDST1 | EDMA3 TC1 Destination FIFO Destination Address Register 1 |
| 0x01C1 0750 | DFBIDX1 | EDMA3 TC1 Destination FIFO B-Index Register 1 |
| 0x01C1 0754 | DFMPPRXY1 | EDMA3 TC1 Destination FIFO Memory Protection Proxy Register 1 |
| 0x01C1 0758 - 0x01C1 077F | – | Reserved |
| 0x01C1 0780 | DFOPT2 | EDMA3 TC1 Destination FIFO Options Register 2 |
| 0x01C1 0784 | DFSRC2 | EDMA3 TC1 Destination FIFO Source Address Register 2 |
| 0x01C1 0788 | DFCNT2 | EDMA3 TC1 Destination FIFO Count Register 2 |
| 0x01C1 078C | DFDST2 | EDMA3 TC1 Destination FIFO Destination Address Register 2 |
| 0x01C1 0790 | DFBIDX2 | EDMA3 TC1 Destination FIFO B-Index Register 2 |
| 0x01C1 0794 | DFMPPRXY2 | EDMA3 TC1 Destination FIFO Memory Protection Proxy Register 2 |
| 0x01C1 0798 - 0x01C1 07BF | – | Reserved |
| 0x01C1 07C0 | DFOPT3 | EDMA3 TC1 Destination FIFO Options Register 3 |
| 0x01C1 07C4 | DFSRC3 | EDMA3 TC1 Destination FIFO Source Address Register 3 |
| 0x01C1 07C8 | DFCNT3 | EDMA3 TC1 Destination FIFO Count Register 3 |
| 0x01C1 07CC | DFDST3 | EDMA3 TC1 Destination FIFO Destination Address Register 3 |
| 0x01C1 07D0 | DFBIDX3 | EDMA3 TC1 Destination FIFO B-Index Register 3 |
| 0x01C1 07D4 | DFMPPRXY3 | EDMA3 TC1 Destination FIFO Memory Protection Proxy Register 3 |
| 0x01C1 07D8 - 0x01C1 07FF | – | Reserved |
| **Transfer Controller 2 Registers** | | |
| 0x01C1 0800 | PID | Peripheral Identification Register |
| 0x01C1 0804 | TCCFG | EDMA3 TC2 Configuration Register |
| 0x01C1 0808 - 0x01C1 08FF | – | Reserved |
| 0x01C1 0900 | TCSTAT | EDMA3 TC2 Channel Status Register |
| 0x01C1 0904 - 0x01C1 0913 | – | Reserved |
| 0x01C1 0914 - 0x01C1 091F | – | Reserved |
| 0x01C1 0920 | ERRSTAT | EDMA3 TC2 Error Status Register |
| 0x01C1 0924 | ERREN | EDMA3 TC2 Error Enable Register |
| 0x01C1 0928 | ERRCLR | EDMA3 TC2 Error Clear Register |
| 0x01C1 092C | ERRDET | EDMA3 TC2 Error Details Register |
| 0x01C1 0930 | ERRCMD | EDMA3 TC2 Error Interrupt Command Register |
| 0x01C1 0934 - 0x01C1 093F | – | Reserved |
| 0x01C1 0940 | RDRATE | EDMA3 TC2 Read Command Rate Register |
| 0x01C1 0944 - 0x01C1 09FF | – | Reserved |
| 0x01C1 0A00 - 0x01C1 0A3F | – | Reserved |
| 0x01C1 0A40 | SAOPT | EDMA3 TC2 Source Active Options Register |
| 0x01C1 0A44 | SASRC | EDMA3 TC2 Source Active Source Address Register |

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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 0A48 | SACNT | EDMA3 TC2 Source Active Count Register |
| 0x01C1 0A4C | SADST | EDMA3 TC2 Source Active Destination Address Register |
| 0x01C1 0A50 | SABIDX | EDMA3 TC2 Source Active B-Index Register |
| 0x01C1 0A54 | SAMPPRXY | EDMA3 TC2 Source Active Memory Protection Proxy Register |
| 0x01C1 0A58 | SACNTRLD | EDMA3 TC2 Source Active Count Reload Register |
| 0x01C1 0A5C | SASRCBREF | EDMA3 TC2 Source Active Source Address B-Reference Register |
| 0x01C1 0A60 | SADSTBREF | EDMA3 TC2 Source Active Destination Address B-Reference Register |
| 0x01C1 0A64 - 0x01C1 0A7F | – | Reserved |
| 0x01C1 0A80 | DFCNTRLD | EDMA3 TC2 Destination FIFO Set Count Reload Register |
| 0x01C1 0A84 | DFSRCBREF | EDMA3 TC2 Destination FIFO Set Source Address B-Reference Register |
| 0x01C1 0A88 | DFDSTBREF | EDMA3 TC2 Destination FIFO Set Destination Address B-Reference Register |
| 0x01C1 0A8C - 0x01C1 0AFF | – | Reserved |
| 0x01C1 0B00 | DFOPT0 | EDMA3 TC2 Destination FIFO Options Register 0 |
| 0x01C1 0B04 | DFSRC0 | EDMA3 TC2 Destination FIFO Source Address Register 0 |
| 0x01C1 0B08 | DFCNT0 | EDMA3 TC2 Destination FIFO Count Register 0 |
| 0x01C1 0B0C | DFDST0 | EDMA3 TC2 Destination FIFO Destination Address Register 0 |
| 0x01C1 0B10 | DFBIDX0 | EDMA3 TC2 Destination FIFO B-Index Register 0 |
| 0x01C1 0B14 | DFMPPRXY0 | EDMA3 TC2 Destination FIFO Memory Protection Proxy Register 0 |
| 0x01C1 0B18 - 0x01C1 0B3F | – | Reserved |
| 0x01C1 0B40 | DFOPT1 | EDMA3 TC2 Destination FIFO Options Register 1 |
| 0x01C1 0B44 | DFSRC1 | EDMA3 TC2 Destination FIFO Source Address Register 1 |
| 0x01C1 0B48 | DFCNT1 | EDMA3 TC2 Destination FIFO Count Register 1 |
| 0x01C1 0B4C | DFDST1 | EDMA3 TC2 Destination FIFO Destination Address Register 1 |
| 0x01C1 0B50 | DFBIDX1 | EDMA3 TC2 Destination FIFO B-Index Register 1 |
| 0x01C1 0B54 | DFMPPRXY1 | EDMA3 TC2 Destination FIFO Memory Protection Proxy Register 1 |
| 0x01C1 0B58 - 0x01C1 0B7F | – | Reserved |
| 0x01C1 0B80 | DFOPT2 | EDMA3 TC2 Destination FIFO Options Register 2 |
| 0x01C1 0B84 | DFSRC2 | EDMA3 TC2 Destination FIFO Source Address Register 2 |
| 0x01C1 0B88 | DFCNT2 | EDMA3 TC2 Destination FIFO Count Register 2 |
| 0x01C1 0B8C | DFDST2 | EDMA3 TC2 Destination FIFO Destination Address Register 2 |
| 0x01C1 0B90 | DFBIDX2 | EDMA3 TC2 Destination FIFO B-Index Register 2 |
| 0x01C1 0B94 | DFMPPRXY2 | EDMA3 TC2 Destination FIFO Memory Protection Proxy Register 2 |
| 0x01C1 0B98 - 0x01C1 0BBF | – | Reserved |
| 0x01C1 0BC0 | DFOPT3 | EDMA3 TC2 Destination FIFO Options Register 3 |
| 0x01C1 0BC4 | DFSRC3 | EDMA3 TC2 Destination FIFO Source Address Register 3 |
| 0x01C1 0BC8 | DFCNT3 | EDMA3 TC2 Destination FIFO Count Register 3 |
| 0x01C1 0BCC | DFDST3 | EDMA3 TC2 Destination FIFO Destination Address Register 3 |
| 0x01C1 0BD0 | DFBIDX3 | EDMA3 TC2 Destination FIFO B-Index Register 3 |
| 0x01C1 0BD4 | DFMPPRXY3 | EDMA3 TC2 Destination FIFO Memory Protection Proxy Register 3 |
| 0x01C1 0BD8 - 0x01C1 0BFF | – | Reserved |
| **Transfer Controller 3 Registers** | | |
| 0x01C1 0C00 | PID | Peripheral Identification Register |
| 0x01C1 0C04 | TCCFG | EDMA3 TC3 Configuration Register |
| 0x01C1 0C08 - 0x01C1 0CFF | – | Reserved |
| 0x01C1 0D00 | TCSTAT | EDMA3 TC3 Channel Status Register |
| 0x01C1 0D04 - 0x01C1 0D1F | – | Reserved |
| 0x01C1 0D20 | ERRSTAT | EDMA3 TC3 Error Status Register |


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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 0D24 | ERREN | EDMA3 TC3 Error Enable Register |
| 0x01C1 0D28 | ERRCLR | EDMA3 TC3 Error Clear Register |
| 0x01C1 0D2C | ERRDET | EDMA3 TC3 Error Details Register |
| 0x01C1 0D30 | ERRCMD | EDMA3 TC3 Error Interrupt Command Register |
| 0x01C1 0D34 - 0x01C1 0D3F | – | Reserved |
| 0x01C1 0D40 | RDRATE | EDMA3 TC3 Read Command Rate Register |
| 0x01C1 0D44 - 0x01C1 0E3F | – | Reserved |
| 0x01C1 0E40 | SAOPT | EDMA3 TC3 Source Active Options Register |
| 0x01C1 0E44 | SASRC | EDMA3 TC3 Source Active Source Address Register |
| 0x01C1 0E48 | SACNT | EDMA3 TC3 Source Active Count Register |
| 0x01C1 0E4C | SADST | EDMA3 TC3 Source Active Destination Address Register |
| 0x01C1 0E50 | SABIDX | EDMA3 TC3 Source Active B-Index Register |
| 0x01C1 0E54 | SAMPPRXY | EDMA3 TC3 Source Active Memory Protection Proxy Register |
| 0x01C1 0E58 | SACNTRLD | EDMA3 TC3 Source Active Count Reload Register |
| 0x01C1 0E5C | SASRCBREF | EDMA3 TC3 Source Active Source Address B-Reference Register |
| 0x01C1 0E60 | SADSTBREF | EDMA3 TC3 Source Active Destination Address B-Reference Register |
| 0x01C1 0E64 - 0x01C1 0E7F | – | Reserved |
| 0x01C1 0E80 | DFCNTRLD | EDMA3 TC3 Destination FIFO Set Count Reload Register |
| 0x01C1 0E84 | DFSRCBREF | EDMA3 TC3 Destination FIFO Set Source Address B-Reference Register |
| 0x01C1 0E88 | DFDSTBREF | EDMA3 TC3 Destination FIFO Set Destination Address B-Reference Register |
| 0x01C1 0E8C - 0x01C1 0EFF | – | Reserved |
| 0x01C1 0F00 | DFOPT0 | EDMA3 TC3 Destination FIFO Options Register 0 |
| 0x01C1 0F04 | DFSRC0 | EDMA3 TC3 Destination FIFO Source Address Register 0 |
| 0x01C1 0F08 | DFCNT0 | EDMA3 TC3 Destination FIFO Count Register 0 |
| 0x01C1 0F0C | DFDST0 | EDMA3 TC3 Destination FIFO Destination Address Register 0 |
| 0x01C1 0F10 | DFBIDX0 | EDMA3 TC3 Destination FIFO B-Index Register 0 |
| 0x01C1 0F14 | DFMPPRXY0 | EDMA3 TC3 Destination FIFO Memory Protection Proxy Register 0 |
| 0x01C1 0F18 - 0x01C1 0F3F | – | Reserved |
| 0x01C1 0F40 | DFOPT1 | EDMA3 TC3 Destination FIFO Options Register 1 |
| 0x01C1 0F44 | DFSRC1 | EDMA3 TC3 Destination FIFO Source Address Register 1 |
| 0x01C1 0F48 | DFCNT1 | EDMA3 TC3 Destination FIFO Count Register 1 |
| 0x01C1 0F4C | DFDST1 | EDMA3 TC3 Destination FIFO Destination Address Register 1 |
| 0x01C1 0F50 | DFBIDX1 | EDMA3 TC3 Destination FIFO B-Index Register 1 |
| 0x01C1 0F54 | DFMPPRXY1 | EDMA3 TC3 Destination FIFO Memory Protection Proxy Register 1 |
| 0x01C1 0F58 - 0x01C1 0F7F | – | Reserved |
| 0x01C1 0F80 | DFOPT2 | EDMA3 TC3 Destination FIFO Options Register 2 |
| 0x01C1 0F84 | DFSRC2 | EDMA3 TC3 Destination FIFO Source Address Register 2 |
| 0x01C1 0F88 | DFCNT2 | EDMA3 TC3 Destination FIFO Count Register 2 |
| 0x01C1 0F8C | DFDST2 | EDMA3 TC3 Destination FIFO Destination Address Register 2 |
| 0x01C1 0F90 | DFBIDX2 | EDMA3 TC3 Destination FIFO B-Index Register 2 |
| 0x01C1 0F94 | DFMPPRXY2 | EDMA3 TC3 Destination FIFO Memory Protection Proxy Register 2 |
| 0x01C1 0F98 - 0x01C1 0FBF | – | Reserved |
| 0x01C1 0FC0 | DFOPT3 | EDMA3 TC3 Destination FIFO Options Register 3 |
| 0x01C1 0FC4 | DFSRC3 | EDMA3 TC3 Destination FIFO Source Address Register 3 |
| 0x01C1 0FC8 | DFCNT3 | EDMA3 TC3 Destination FIFO Count Register 3 |
| 0x01C1 0FCC | DFDST3 | EDMA3 TC3 Destination FIFO Destination Address Register 3 |
| 0x01C1 0FD0 | DFBIDX3 | EDMA3 TC3 Destination FIFO B-Index Register 3 |

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**Table 7-16. DM6467T EDMA Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 0FD4 | DFMPPRXY3 | EDMA3 TC3 Destination FIFO Memory Protection Proxy Register 3 |
| 0x01C1 0FD8 - 0x01C1 0FFF | – | Reserved |

Table 7-17 shows an abbreviation of the set of registers which make up the parameter set for each of 512 EDMA events. Each of the parameter register sets consist of 8 32-bit word entries. Table 7-18 shows the parameter set entry registers with relative memory address locations within each of the parameter sets.


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**Table 7-17. EDMA Parameter Set RAM**

| HEX ADDRESS RANGE | DESCRIPTION |
|---|---|
| 0x01C0 4000 - 0x01C0 401F | Parameters Set 0 (8 32-bit words) |
| 0x01C0 4020 - 0x01C0 403F | Parameters Set 1 (8 32-bit words) |
| 0x01C0 4040 - 0x01C0 405F | Parameters Set 2 (8 32-bit words) |
| 0x01C0 4060 - 0x01C0 407F | Parameters Set 3 (8 32-bit words) |
| 0x01C0 4080 - 0x01C0 409F | Parameters Set 4 (8 32-bit words) |
| 0x01C0 40A0 - 0x01C0 40BF | Parameters Set 5 (8 32-bit words) |
| ... | ... |
| 0x01C0 7FC0 - 0x01C0 7FDF | Parameters Set 510 (8 32-bit words) |
| 0x01C0 7FE0 - 0x01C0 7FFF | Parameters Set 511 (8 32-bit words) |

**Table 7-18. Parameter Set Entries**

| HEX OFFSET ADDRESS WITHIN THE PARAMETER SET | ACRONYM | PARAMETER ENTRY |
|---|---|---|
| 0x0000 | OPT | Option |
| 0x0004 | SRC | Source Address |
| 0x0008 | A_B_CNT | A Count, B Count |
| 0x000C | DST | Destination Address |
| 0x0010 | SRC_DST_BIDX | Source B Index, Destination B Index |
| 0x0014 | LINK_BCNTRLD | Link Address, B Count Reload |
| 0x0018 | SRC_DST_CIDX | Source C Index, Destination C Index |
| 0x001C | CCNT | C Count |

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## 7.7 Reset

The reset controller detects the different type of resets supported on the DM6467T device and manages the distribution of those resets throughout the device.

The DM6467T device has several types of device-level global resets—power-on reset, warm reset, max reset, and system reset. Table 7-19 explains further the types of reset, the reset initiator, and the effects of each reset on the chip. See Section 7.7.9, *Reset Electrical Data/Timing*, for more information on the effects of each reset on the PLL controllers and their clocks.

**Table 7-19. Device-Level Global Reset Types**

| TYPE | INITIATOR | EFFECT(S) |
|---|---|---|
| Power-on Reset (POR) | $\overline{\text{POR}}$ pin | Global chip reset (Cold reset). Activates the POR signal on chip, which resets the entire chip including the emulation logic.<br>The power-on reset ($\overline{\text{POR}}$) pin ***must*** be driven low during power ramp of the device.<br>Device boot and configuration pins are latched. |
| Warm Reset | $\overline{\text{RESET}}$ pin | Resets everything except for the emulation logic. Emulator stays alive during Warm Reset.<br>Device boot and configuration pins are latched. |
| Max Reset | Emulator, WD Timer (Timer 2) | Same as a Warm Reset, except the DM6467T device boot and configuration pins are ***not*** re-latched. |
| System Reset | Emulator | A system reset maintains memory contents and does not reset the test and emulation circuitry. The device boot and configuration pins are also ***not*** re-latched. |
| C64x+ Local Reset (DSP Reset) | Software (register bit) | MMR controls the C64x+ reset input. This is used for control of C64x+ reset by the ARM. The C64x+ Slave DMA port is still alive when in local reset. |

In addition to device-level global resets, the PSC provides the capability to cause local resets to peripherals and/or the C64x+ DSP.

### *7.7.1 Power-on Reset ($\overline{\text{POR}}$ Pin)*

Power-on Reset (POR) is initiated by the $\overline{\text{POR}}$ pin and is used to reset the entire chip, including the test and emulation logic. Power-on Reset is also referred to as a cold reset since the device usually goes through a power-up cycle. During power-up, the $\overline{\text{POR}}$ pin must be asserted (driven low) until the power supplies have reached their normal operating conditions. If an external oscillator is used on the DEV_MXI/DEV_CLKIN pin, the source clock should also be running at the correct frequency prior to de-asserting the $\overline{\text{POR}}$ pin. **Note:** A device power-up cycle is not required to initiate a Power-on Reset.

The following sequence ***must*** be followed during a Power-on Reset.

1. Wait for the power supplies to reach normal operating conditions while keeping the $\overline{\text{POR}}$ pin asserted (driven low).
2. Wait for the input clock source to be stable while keeping the $\overline{\text{POR}}$ pin asserted (low).
3. Once the power supplies and the input clock source are stable, the $\overline{\text{POR}}$ pin ***must*** remain asserted (low) for a minimum of 12 DEV_MXI cycles.

   Within the low period of the $\overline{\text{POR}}$ pin, the following happens:
   - The reset signals flow to the entire chip (including the test and emulation logic), resetting the modules on chip.
   - The PLL Controller clocks start at the frequency of the DEV_MXI clock. The clocks are propagated throughout the chip to reset the chip synchronously. By default, both PLL1 and PLL2 are in reset and unlocked. The PLL Controllers default to PLL Bypass Mode.
4. The $\overline{\text{POR}}$ pin may now be deasserted (driven high).


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When the $\overline{\text{POR}}$ pin is deasserted (high), the configuration pin values are latched and the PLL Controllers changed their system clocks to their default divide-down values. Both PLL Controllers are still in PLL Bypass Mode. Other device initialization also begins.

5. After device initialization is complete, the PLL Controllers pause the system clocks for 10 cycles.

   At this point:
   – The I/O pins are controlled by the default peripherals (default peripherals are determined by PINMUX0 and PINMUX1 registers).
   – The clock and reset of each peripheral is determined by the default settings of the Power and Sleep Controller (PSC).
   – The PLL Controllers are operating in PLL Bypass Mode.
   – The ARM926 begins executing from the default address (either ARM boot ROM or EMIFA).

   After the reset sequence, the boot sequence begins. For more details on the boot sequence, see the Using the *TMS320DM646x Bootloader* Application Report (literature number SPRAAS0).

#### 7.7.1.1 Usage of $\overline{\text{POR}}$ versus $\overline{\text{RESET}}$ Pins

$\overline{\text{POR}}$ and $\overline{\text{RESET}}$ are independent resets.

If the device needs to go through a power-up cycle, $\overline{\text{POR}}$ (*not* $\overline{\text{RESET}}$) ***must*** be used to fully reset the device.

In functional end-system, emulation/debugger logic is typically *not* needed; therefore, the recommendation for functional end-system is to use the $\overline{\text{POR}}$ pin for full device reset. If $\overline{\text{RESET}}$ pin is *not* needed, it can be pulled inactive (high) via an external pullup resistor.

In a debug system, it is typically desirable to allow the reset of the device without crashing an emulation session. In this case, the user can use the $\overline{\text{POR}}$ pin to achieve full device reset and use the $\overline{\text{RESET}}$ pin to achieve a debug reset—which resets the entire device except test and emulation logic.

#### 7.7.1.2 Latching Boot and Configuration Pins

Internal to the chip, the two device reset pins $\overline{\text{RESET}}$ and $\overline{\text{POR}}$ are logically AND'ed together *only* for the purpose of latching device boot and configuration pins. The values on all device and boot configuration pins are latched into the BOOTCFG register when the logical AND of $\overline{\text{RESET}}$ and $\overline{\text{POR}}$ transitions from low to high.

### *7.7.2 Warm Reset ($\overline{\text{RESET}}$ Pin)*

A Warm Reset is activated by driving the $\overline{\text{RESET}}$ pin active-low. This resets everything in the device except the test or emulation logic. An emulator session will stay alive during warm reset.

For more information on $\overline{\text{POR}}$ vs. $\overline{\text{RESET}}$ usage, see Section 7.7.1.1, *Usage of $\overline{\text{POR}}$ versus $\overline{\text{RESET}}$ Pins* and Section 7.7.1.2, *Latching Boot and Configuration Pins*.

The following sequence ***must*** be followed during a Warm Reset:

1. Power supplies and input clock source should already be stable.
2. The $\overline{\text{RESET}}$ pin ***must*** be asserted (low) for a minimum of 12 DEV_MXI cycles.

   Within the low period of the $\overline{\text{RESET}}$ pin, the following happens:
   – The reset signals flow to the entire chip resetting all the modules on chip, except the test and emulation logic.
   – The PLL Controllers are reset thereby, switching back to PLL Bypass Mode and resetting all their registers to default values. Both PLL1 and PLL2 are placed in reset and lose lock.
3. The $\overline{\text{RESET}}$ pin may now be deasserted (driven high).

   When the $\overline{\text{RESET}}$ pin is deasserted (high), the configuration pin values are latched and the PLL Controllers changed their system clocks to their default divide-down values. Both PLL Controllers are still in PLL Bypass Mode. Other device initialization also begins.

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4. After device initialization is complete, the PLL Controllers pause the system clocks for 10 cycles.

   At this point:
   – The I/O pins are controlled by the default peripherals (default peripherals are determined by PINMUX0 and PINMUX1 registers).
   – The clock and reset of each peripheral is determined by the default settings of the Power and Sleep Controller (PSC).
   – The PLL Controllers are operating in PLL Bypass Mode.
   – The ARM926 begins executing from the default address (either ARM boot ROM, TCM RAM, or EMIFA).

After the reset sequence, the boot sequence begins. For more details on the boot sequence, see the Using the *TMS320DM646x Bootloader* Application Report (literature number SPRAAS0).

### 7.7.3 Maximum Reset

A Maximum (Max) Reset is initiated by the emulator or the watchdog timer (Timer 2). The effects are the same as a warm reset, except the device boot and configuration pins are not re-latched. The emulator initiates a maximum reset via the ICEPICK module. This ICEPICK-initiated reset is non-maskable. When the watchdog timer counter reaches zero, this will also initiate a maximum reset to recover from a runaway condition.

To invoke the maximum reset via the ICEPICK module, the user can perform the following from the Code Composer Studio™ IDE menu: Debug→Advanced Resets→System Reset

This is the Max Reset sequence:

1. Max Reset is initiated by the emulator or the watchdog timer.

   During this time, the following happens:
   – The reset signals flow to the entire chip, resetting all the modules on chip except the test and emulation logic.
   – The PLL Controllers are reset —thereby, switching back to PLL Bypass Mode and resetting all their registers to default values. Both PLL1 and PLL2 are placed in reset and lose lock.
2. After device initialization is complete, the PLL Controllers pause the system clocks for 10 cycles.

   At this point:
   – The I/O pins are controlled by the default peripherals (default peripherals are determined by PINMUX0 and PINMUX1 registers).
   – The clock and reset of each peripheral is determined by the default settings of the Power and Sleep Controller (PSC).
   – The PLL Controllers are operating in PLL Bypass Mode.
   – The ARM926 begins executing from the default address (either ARM boot ROM, TCM RAM, or EMIFA).

After the reset sequence, the boot sequence begins. Since the boot and configuration pins are *not* latched with a Max Reset, the previous values (as shown in the BOOTCFG register) are used to select the boot mode. For more details on the boot sequence, see the Using the *TMS320DM646x Bootloader* Application Report (literature number SPRAAS0).

### 7.7.4 System Reset

A System Reset is initiated by the emulator. The following memory contents are maintained:

- L1/L2 RAM: The C64x+ L1/L2 RAM content is retained. The L1/L2 cache content is ***not*** retained because tag information is reset.
- DDR2 Memory Controller: The DDR2 Memory Controller registers are ***not*** reset. In addition, the DDR2 SDRAM memory content is retained if the user places the DDR2 SDRAM in self-refresh mode before invoking the System Reset.


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Test, emulation, clock, and power control logic are unaffected. The emulator initiates a System Reset via the C64x+ emulation logic. This reset can be masked by the emulator.

This is the System Reset sequence:

1. The System Reset is initiated by the emulator.

   During this time, the following happens:
   – The reset signals flow to the entire chip resetting all the modules on chip, except the test and emulation logic.
   – The PLL Controllers are ***not*** reset. Internal system clocks are unaffected. If PLL1/PLL2 were locked before the System Reset, they remain locked.
2. After device initialization is complete, the PLL Controllers pause the system clocks for 10 cycles.

   At this point:
   – The I/O pins are controlled by the default peripherals (default peripherals are determined by PINMUX0 and PINMUX1 registers).
   – The clock and reset of each peripheral (except the DDR2 Memory Controller) is determined by the default settings of the Power and Sleep Controller (PSC).
   – The DDR2 Memory Controller registers retain their previous values. Only the DDR2 Memory Controller state machines are reset by the System Reset.
   – The PLL Controllers are operating in the mode prior to System Reset. The System clocks are unaffected.
   – The ARM926 begins executing from the default address (either ARM boot ROM, TCM RAM, or EMIFA).

After the reset sequence, the boot sequence begins. Since the boot and configuration pins are *not* latched with a System Reset, the previous values (as shown in the BOOTCFG register) are used to select the boot mode. For more details on the boot sequence, see the Using the *TMS320DM646x Bootloader* Application Report (literature number SPRAAS0).

### 7.7.5 C64x+ Local Reset (DSP Local Reset)

With access to the PSC registers, the ARM can perform two types of DSP reset: DSP local reset and DSP module reset. When DSP local reset is asserted, the DSP's internal memories (L1P, L1D, and L2) are still accessible. The local reset only resets the DSP CPU core, not the rest of the DSP subsystem, as the DSP module reset would. Local reset is useful when the DSP module is in the enable state or in the disable state. The DSP module reset takes precedence over local reset. The ARM uses local reset to reset the DSP to initiate the DSP boot process. The intent of module reset is to completely reset the DSP (like hard reset). For more detailed information on DSP local reset and DSP module reset, see the ARM-DSP Integration Chapter in the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

For information on peripheral selection at the rising edge of $\overline{\text{POR}}$ or $\overline{\text{RESET}}$, see Section 4, *Device Configurations* of this data manual.

### 7.7.6 Peripheral Local Reset

The user can configure the local reset and clock state of a peripheral through programming the PSC. Table 7-3, DM6467T LPSC Assignments, identifies the LPSC numbers and the peripherals capable of being locally reset by the PSC. For more detailed information on the programming of these peripherals by the PSC, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

### 7.7.7 Reset Priority

If any of the above reset sources occur simultaneously, the PLLC only processes the highest-priority reset request. The reset request priorities, from high to low, are as follows:

- Power-on Reset

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- Maximum Reset
- Warm Reset
- System Reset

#### 7.7.7.1 Reset Type Status (RSTYPE) Register

The Reset Type Status (RSTYPE) register (0x01C4 08E4) is the only register for the reset controller. This register falls in the same memory range as the PLL1 controller registers (see Table 7-11 for the PLL1 Controller Registers (Including Reset Controller)). For more details on the RSTYPE register and its bit descriptions, see Figure 7-18 and Table 7-20.

| 31 | 16 |
|---|---|
| RESERVED | |
| R-0000 0000 0000 0000 | |

| 15 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|
| RESERVED | | SRST | MRST | WRST | POR |
| R-0000 0000 0000 | | R-0/1 | R-0/1 | R-0/1 | R-0/1 |

LEGEND: R = Read only; -*n* = value after reset

**Figure 7-18. Reset Type Status (RSTYPE) Register [0x01C4 08E4]**

**Table 7-20. RSTYPE Register Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 30:4 | RESERVED | Reserved. Read returns "0". Writes have no effect. |
| 3 | SRST | System Reset.<br>0 = System Reset was ***not*** the last reset to occur.<br>1 = System Reset was the last reset to occur. |
| 2 | MRST | Max Reset.<br>0 = Max Reset was ***not*** the last reset to occur.<br>1 = Max Reset was the last reset to occur. |
| 1 | WRST | Warm Reset.<br>0 = Warm Reset was ***not*** the last reset to occur.<br>1 = Warm Reset was the last reset to occur. |
| 0 | POR | Power-on Reset.<br>0 = Power-on Reset was ***not*** the last reset to occur.<br>1 = Power-on Reset was the last reset to occur. |

### *7.7.8 Pin Behaviors at Reset*

During normal operations, pins are controlled by the respective peripheral selected in the PINMUX0 or PINMUX1 register. During device level global reset, the pin behaves as follows:

**Multiplexed Boot and Configuration Pins**

These pins are forced 3-stated when the device is in reset. This is to ensure the proper boot and configuration values can be latched on these multiplexed pins. This is particularly useful in the case where the boot and configuration values are driven by an external control device. Once the device is out of reset, these pins are controlled by their respective default peripheral.

- **Boot and Configuration Pins Group:** VP_DOUT6/DSPBOOT, VP_DOUT5/PCIEN, VP_DOUT4/CS2BW, VP_DOUT3/BTMODE3, VP_DOUT2/BTMODE2, VP_DOUT1/BTMODE1, and VP_DOUT0/BTMODE0.

For information on whether external pullup/pulldown resistors should be used on the boot and configuration pins, see Section 4.8.1, *Pullup/Pulldown Resistors*.


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### Default Power Down Pins

As discussed in Section 4.2, *Power Considerations*, the VDD3P3V_PWDN register controls power to the 3.3-V pins. The VDD3P3V_PWDN register defaults to powering down some 3.3-V pins to save power. For more details on the VDD3P3V_PWDN register and which 3.3-V pins default to power up or power down, see Section 4.2, *Power Considerations*. The pins that default to power down, are both reset to power down and high-impedance. They remain in that state until configured otherwise by VDD3P3_PWDN and PINMUX0/PINMUX1 programming.

- **Default Power Down Pin Group:** USB_DRVVBUS/GP[22], CLKOUT0, SPI_CLK, SPI_EN, SPI_CS0, SPI_CS1, SPI_MISO, SPI_MOSI, VLYNQ_CLOCK, VLYNQ_SCRUN, VLYNQ_TXD[3:0], VLYNQ_RXD[3:0], RFTCLK, GMTCLK, MTXD[7:4], MRXD[7:4], MTCLK, MTXD[3:0], MTXEN, MCOL, MCRS, MRCLK, MRXD[3:0], MRXDV, MRXER, MDCLK, MDIO, ACLKX1, AHCLKX1, AXR1[0], ACLKR0, AHCLKR0, AFSR0, ACLKX0, AHCLKX0, AFSX0, AXR0[3:0], AMUTE0, AMUTEIN0, PCI_CLK/GP[10], PCI_DEVSEL/HCNTL1/EM_BA[1], PCI_FRAME/HINT/EM_BA[0], PCI_IRDY/HRDY/EM_A[17], PCI_TRDY/HHWIL/EM_A[16], PCI_STOP/HCNTL0/EM_WE, PCI_SERR/HDS1/EM_OE, PCI_PERR/HCS/EM_DQM1, PCI_PAR/HAS/EM_DQM0, PCI_INTA/EM_WAIT2, PCI_CBE3/HR/W/EM_CS3, PCI_CBE2/HDS2/EM_CS2, PCI_AD[15:0]/HD[15:0]/EM_D[15:0], PCI_RST/DA2/GP[13]/EM_A[22], PCI_IDSEL/HDDIR/EM_R/W, PCI_REQ/DMARQ/GP[11]/EM_CS5, PCI_GNT/DMACK/GP[12]/EM_CS4, PCI_CBE1/ATA_CS1/GP[32]/EM_A[19], PCI_CBE0/ATA_CS0/GP[33]/EM_A[18], DIOW/GP[20]/EM_WAIT4, IORDY/GP[21]/EM_WAIT3, DIOR/GP[19]/EM_WAIT5, DA1/GP[16]/EM_A[21], DA0/GP[17]/EM_A[20], INTRQ/GP[18]/RSV , PCI_AD[31:16]/DD[15:0]/HD[31:16]/EM_A[15:0], GP[7], GP[6], GP[5], GP[4]/STC_CLKIN, GP[3]/AUDIO_CLK0, GP[2]/AUDIO_CLK1, GP[1], GP[0], TOUT2, TINP1L, TOUT1L, TOUT1U, TINP0L, TINP0U, TOUT0L, TOUT0U, PWM1/TS1_DOUT, PWM0/CRG0_PO/TS1_ENAO, URTS2/UIRTX2/TS0_PSTIN/GP[41], UCTS2/USD2/CRG0_VCXI/GP[42]/TS1_PSTO, URXD2/CRG1_VCXI/GP[39]/CRG0_VCXI, UTXD2/URCTX2/CRG1_PO/GP[40]/CRG0_PO, URTS1/UIRTX1/TS0_WAITO/GP[25], UCTS1/USD1/TS0_EN_WAITO/GP[26], URXD1/TS0_DIN7/GP[23], UTXD1/URCTX1/TS0_DOUT7/GP[24], UDTR0/TS0_ENAO/GP[36], UDSR0/TS0_PSTO/GP[37], UDCD0/TS0_WAITIN/GP[38], URIN0/GP[8]/TS1_WAITIN, URXD0/TS1_DIN, UTXD0/URCTX0/TS1_PSTIN, URTS0/UIRTX0/TS1_EN_WAITO, UCTS0/USD0, VP_DOUT15/TS1_DIN, VP_DOUT14/TS1_PSTIN, VP_DOUT13/TS1_EN_WAITO, VP_DOUT12/TS1_WAITO, VP_DOUT11/TS1_DOUT, VP_DOUT10/TS1_PSTO, VP_DOUT9/TS1_ENAO, VP_DOUT8/TS1_WAITIN, VP_CLKIN3/TS1_CLKO, VP_CLKO3/TS0_CLKO, VP_DOUT7, VP_DOUT6/DSPBOOT, VP_DOUT5/PCIEN, VP_DOUT4/CS2BW, VP_DOUT3/BTMODE3, VP_DOUT2/BTMODE2, VP_DOUT1/BTMODE1, VP_DOUT0/BTMODE0, VP_CLKIN2, VP_CLKO2, VP_DIN15_VSYNC/TS0_DIN7, VP_DIN14_HSYNC/TS0_DIN6, VP_DIN13_FIELD/TS0_DIN5, VP_DIN12/TS0_DIN4, VP_DIN11/TS0_DIN3, VP_DIN10/TS0_DIN2, VP_DIN9/TS0_DIN1, VP_DIN8/TS0_DIN0, VP_CLKIN1, VP_DIN7/TS0_DOUT7/TS1_DIN, VP_DIN6/TS0_DOUT6/TS1_PSTIN, VP_DIN5/TS0_DOUT5/TS1_EN_WAITO, VP_DIN4/TS0_DOUT4/TS1_WAITO, VP_DIN3/TS0_DOUT3, VP_DIN2/TS0_DOUT2, VP_DIN1/TS0_DOUT1, VP_DIN0/TS0_DOUT0, VP_CLKIN0.

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### All Other Pins

During device reset, all other pins are controlled by the default peripheral. The default peripheral is determined by the default settings of the PINMUX0 or PINMUX1 registers.

Some of the PINMUX0/PINMUX1 settings are determined by configuration pins latched at reset. To determine the reset behavior of these pins, see Section 4.7, *Multiplexed Pin Configurations* and read the rest of the this subsection to understand how that default peripheral controls the pin.

The reset behaviors for all these other pins during all boot modes, ***except PCI Boot***, are categorized as follows (also see Figure 7-19 and Figure 7-20 in Section 7.7.9, *Reset Electrical Data/Timing*):

- **DDR2 Z Group:** DDR_DQS[3:0], DDR_DQS[3:0], DDR_D[31:0], DDR_DQGATE1, DDR_DQGATE3
- **DDR2 Low Group:** DDR_CLK, DDR_CKE, DDR_ODT0, DDR_A[14:0], DDR_DQGATE0, DDR_DQGATE2
- **DDR2 High Group:** DDR_CLK, DDR_CS, DDR_WE, DDR_RAS, DDR_CAS
- **DDR2 Z/High Group:** DDR_DQM[3:0]
- **DDR2 Low/High Group:** DDR_BA[2:0]
- **Z Group:** These pin are 3-stated by default, and these pins remain 3-stated throughout POR or RESET assertion. When POR or RESET is deasserted, these pins remain 3-stated until configured otherwise by their respective peripheral (after the peripheral is enabled by the PSC). PCI_CLK/GP[10], PCI_INTA/EM_WAIT2, DIOW/GP[20]/EM_WAIT4, IORDY/GP[21]/EM_WAIT3, PCI_AD[15:0]/HD[15:0]/EM_D[15:0], RFTCLK, GMTCLK, MTCLK, MTXD[7:0], MTXEN, MCOL, MCRS, MRCLK, MRXD[7:0], MRXDV, MRXER, MDCLK, MDIO, URXD0/TS1_DIN, UTXD0/URCTX0/TS1_PSTIN, URTS0/UIRTX0/TS1_EN_WAITO, UCTS0/USD0, UDTR0/TS0_ENAO/GP[36], UDSR0/TS0_PSTO/GP[37], UDCD0/TS0_WAITIN/GP[38], URIN0/GP[8]/TS1_WAITIN, URXD1/TS0_DIN7/GP[23], UTXD1/URCTX1/TS0_DOUT7/GP[24], URTS1/UIRTX1/TS0_WAITO/GP[25], UCTS1/USD1/TS0_EN_WAITO/GP[26], URXD2/CRG1_VCXI/GP[39]/CRG0_VCXI, UTXD2/URCTX2/CRG1_PO/GP[40]/CRG0_PO, URTS2/UIRTX2/TS0_PSTIN/GP[41], UCTS2/USD2/CRG0_VCXI/GP[42]/TS1_PSTO, ACLKR0, AHCLKR0, AFSR0, ACLKX0, AHCLKX0, AFSX0, AXR0[3:0], AMUTE0, AMUTEIN0, ACLKX1, AHCLKX1, AXR1[0], SCL, SDA, SPI_CLK, SPI_EN, SPI_CS0, SPI_CS1, SPI_MISO, SPI_MOSI, PWM0/CRG0_PO/TS1_ENAO, PWM1/TS1_DOUT, VLYNQ_CLOCK, VLYNQ_SCRUN, VLYNQ_TXD[3:0], VLYNQ_RXD[3:0], USB_DRVVBUS/GP[22], TINP0L, TINP0U, TOUT0L, TOUT0U, TINP1L, TOUT1L, TOUT1U, TOUT2, TS0_CLKIN, TS1_CLKIN, VP_CLKIN0, VP_CLKIN1, VP_DIN15_VSYNC/TS0_DIN7, VP_DIN14_HSYNC/TS0_DIN6, VP_DIN13_FIELD/TS0_DIN5, VP_DIN12/TS0_DIN4, VP_DIN11/TS0_DIN3, VP_DIN10/TS0_DIN2, VP_DIN9/TS0_DIN1, VP_DIN8/TS0_DIN0, VP_DIN7/TS0_DOUT7/TS1_DIN, VP_DIN6/TS0_DOUT6/TS1_PSTIN, VP_DIN5/TS0_DOUT5/TS1_EN_WAITO, VP_DIN4/TS0_DOUT4/TS1_WAITO, VP_DIN3/TS0_DOUT3, VP_DIN2/TS0_DOUT2, VP_DIN1/TS0_DOUT1, VP_DIN0/TS0_DOUT0, VP_CLKIN2, VP_CLKIN3/TS1_CLKO, VP_CLKO2, VP_CLKO3/TS0_CLKO, VP_DOUT15/TS1_DIN, VP_DOUT14/TS1_PSTIN, VP_DOUT13/TS1_EN_WAITO, VP_DOUT12/TS1_WAITO, VP_DOUT11/TS1_DOUT, VP_DOUT10/TS1_PSTO, VP_DOUT9/TS1_ENAO, VP_DOUT8/TS1_WAITIN, VP_DOUT7, GP[0], GP[1], GP[2]/AUDIO_CLK1, GP[3]/AUDIO_CLK0, GP[4]/STC_CLKIN, GP[5], GP[6], GP[7], TIMS, TDO, TDI, TCK, TRST, EMU1, EMU0, DEV_MXI/DEV_CLKIN, AUX_MXI/AUX_CLKIN
- **Low Group:** These pins are low by default, and remain low until configured otherwise by their respective peripheral (after the peripheral is enabled by the PSC). PCI_RST/DA2/GP[13]/EM_A[22], PCI_IDSEL/HDDIR/EM_R/W, PCI_IRDY/HRDY/EM_A[17], PCI_TRDY/HHWIL/EM_A[16], PCI_CBE1/ATA_CS1/GP[32]/EM_A[19], PCI_CBE0/ATA_CS0/GP[33]/EM_A[18], PCI_AD[31:16]/DD[15:0]/HD[31:16]/EM_A[15:0], CLKOUT0, RTCLK,


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- **High Group:** These pins are high by default, and remain high until configured otherwise by their respective peripheral (after the peripheral is enabled by the PSC). PCI_DEVSEL/HCNTL1/EM_BA[1], PCI_FRAME/HINT/EM_BA[0], PCI_STOP/HCNTL0/EM_WE, PCI_SERR/HDS1/EM_OE, PCI_PERR/HCS/EM_DQM1, PCI_PAR/HAS/EM_DQM0, PCI_REQ/DMARQ/GP[11]/EM_CS5, PCI_GNT/DMACK/GP[12]/EM_CS4, PCI_CBE3/HR/W/EM_CS3, PCI_CBE2/HDS2/EM_CS2,

**NOTE:** For **PCI boot mode**, all PCI pins now behave according to Z Group.

For more information on the pin behaviors during device-level global reset, see Figure 7-19 and Figure 7-20 in Section 7.7.9, *Reset Electrical Data/Timing*.

### 7.7.9 Reset Electrical Data/Timing

**Note:** If a configuration pin ***must*** be routed out from the device, the internal pullup/pulldown (IPU/IPD) resistor should ***not*** be relied upon; TI recommends the use of an external pullup/pulldown resistor.

**Table 7-21. Timing Requirements for Reset (see Figure 7-19 and Figure 7-20)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(RESET)}$ | Pulse duration, $\overline{POR}$ low or $\overline{RESET}$ low | 12C(1) | | ns |
| 2 | $t_{su(CONFIG)}$ | Setup time, boot and configuration pins valid before $\overline{POR}$ high or $\overline{RESET}$ high(2) | 12C(1) | | ns |
| 3 | $t_{h(CONFIG)}$ | Hold time, boot and configuration pins valid after $\overline{POR}$ high or $\overline{RESET}$ high(2) | 0 | | ns |

(1) C = 1/DEV_MXI clock frequency in ns. The device clock source ***must*** be stable and at a valid frequency prior to meeting the $t_{w(RESET)}$ requirement.
(2) For the list of boot and configuration pins, see Table 3-5, *Boot Terminal Functions*.

**Table 7-22. Switching Characteristics Over Recommended Operating Conditions During Reset(1) (see Figure 7-20)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 4 | $t_{w(PAUSE)}$ | Pulse duration, SYSCLKs paused (low) | 10C | 10C | ns |
| 23 | $t_{d(RSTH-PAUSE)}$ | Delay time, $\overline{RESET}$ high or $\overline{POR}$ high to SYSCLKs paused (low) | | 1990C | ns |
| 5 | $t_{d(RSTL-BOOTZ)}$ | Delay time, $\overline{RESET}$ low to Boot Configuration Group high impedance | 0 | 20 | ns |
| 6 | $t_{d(RSTL-DDRZZ)}$ | Delay time, $\overline{RESET}$ low to DDR2 Z Group high impedance | 0 | 7P + 20 | ns |
| 7 | $t_{d(RSTL-DDRLL)}$ | Delay time, $\overline{RESET}$ low to DDR2 Low Group low | 0 | 3P + 20 | ns |
| 8 | $t_{d(RSTL-DDRHH)}$ | Delay time, $\overline{RESET}$ low to DDR2 High Group high | 0 | 20 | ns |
| 13 | $t_{d(RSTL-DDRZHZ)}$ | Delay time, $\overline{RESET}$ low to DDR2 Z/High Group high impedance | 0 | 7P + 20 | ns |
| 14 | $t_{d(RSTL-DDRLHL)}$ | Delay time, $\overline{RESET}$ low to DDR2 Low/High Group low | 0 | 20 | ns |
| 17 | $t_{d(RSTL-ZZ)}$ | Delay time, $\overline{RESET}$ low to Z Group high impedance | 0 | 20 | ns |
| 18 | $t_{d(RSTL-LOWL)}$ | Delay time, $\overline{RESET}$ low to Low Group low | 0 | 20 | ns |
| 19 | $t_{d(RSTL-HIGHH)}$ | Delay time, $\overline{RESET}$ low to High Group high | 0 | 20 | ns |
| 9 | $t_{d(RSTL-BOOTV)}$ | Delay time, $\overline{RESET}$ high to Boot Configuration Group valid | | (2) | ns |
| 10 | $t_{d(RSTH-DDRZV)}$ | Delay time, $\overline{RESET}$ high to DDR2 Z Group valid | | (2) | ns |
| 11 | $t_{d(RSTH-DDRLV)}$ | Delay time, $\overline{RESET}$ high to DDR2 Low Group valid | | (2) | ns |
| 12 | $t_{d(RSTH-DDRHV)}$ | Delay time, $\overline{RESET}$ high to DDR2 High Group valid | | (2) | ns |
| 15 | $t_{d(RSTH-DDRZHV)}$ | Delay time, $\overline{RESET}$ high to DDR2 Z/High Group valid high | | (2) | ns |
| 16 | $t_{d(RSTH-DDRLHV)}$ | Delay time, $\overline{RESET}$ high to DDR2 Low/High Group valid high | | (2) | ns |
| 20 | $t_{d(RSTH-ZV)}$ | Delay time, $\overline{RESET}$ high to Z Group valid | | (2) | ns |
| 21 | $t_{d(RSTH-LOWV)}$ | Delay time, $\overline{RESET}$ high to Low Group valid | | (2) | ns |
| 22 | $t_{d(RSTH-HIGHV)}$ | Delay time, $\overline{RESET}$ high to High Group valid | | (2) | ns |

(1) C = 1/DEV_CLKIN clock frequency in ns.
(2) Following $\overline{RESET}$ high or $\overline{POR}$ high, this signal group maintains the state the pins(s) achieved while $\overline{RESET}$ or $\overline{POR}$ was driven low until the peripheral is enabled via the PSC. For example, the DDR2 Z Group goes high impedance following $\overline{RESET}$ low or $\overline{POR}$ low and remains in the high-impedance state following $\overline{RESET}$ high or $\overline{POR}$ high until the DDR2 controller is enabled via the PSC.

Figure 7-19 shows the Power-Up Timing. Figure 7-20 shows the Warm Reset ($\overline{RESET}$) Timing. Max Reset Timing is identical to Warm Reset Timing, except the boot and configuration pins are ***not*** relatched *and* the BOOTCFG register retains its previous value latched before the Max Reset was initiated.


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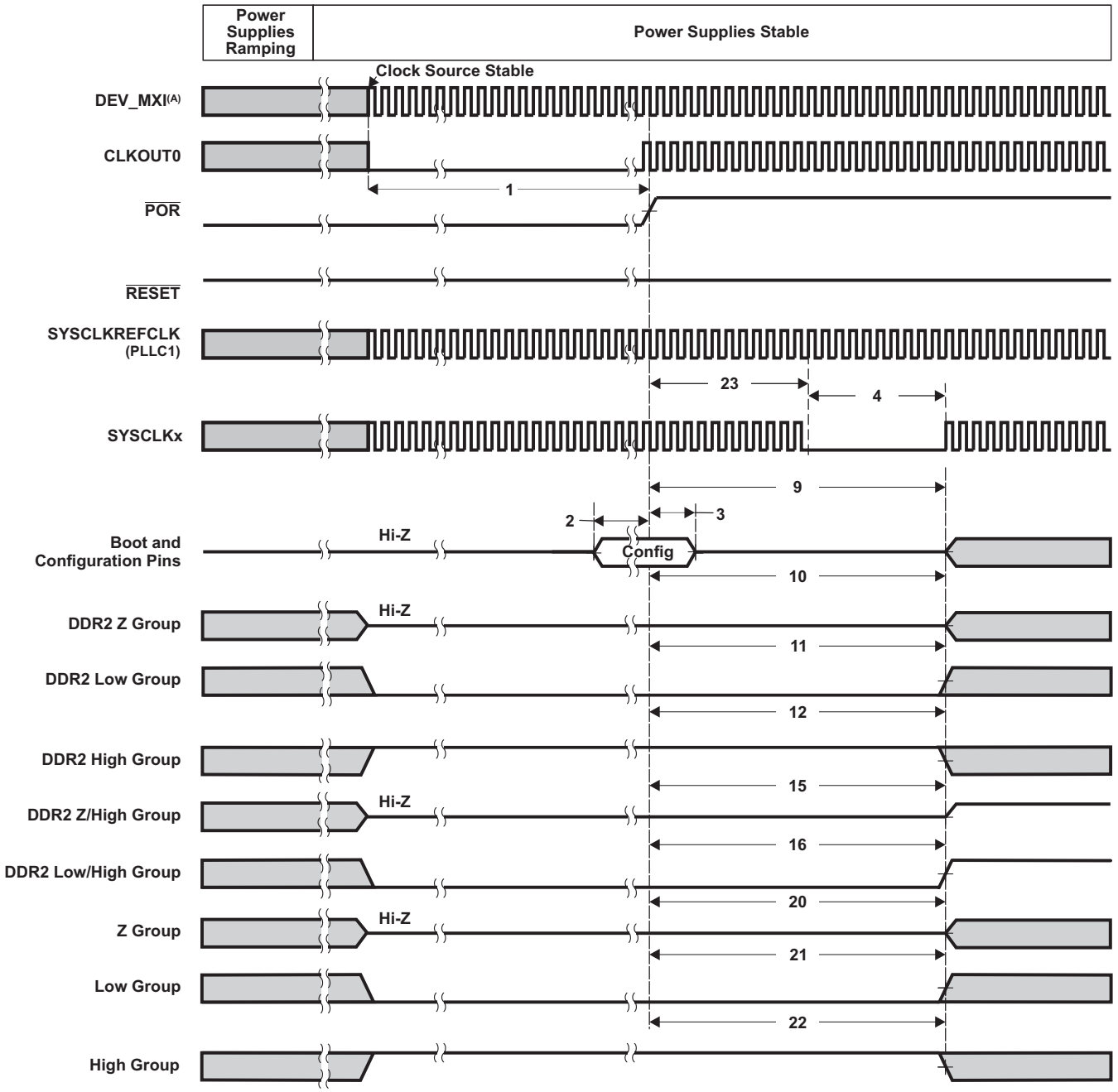
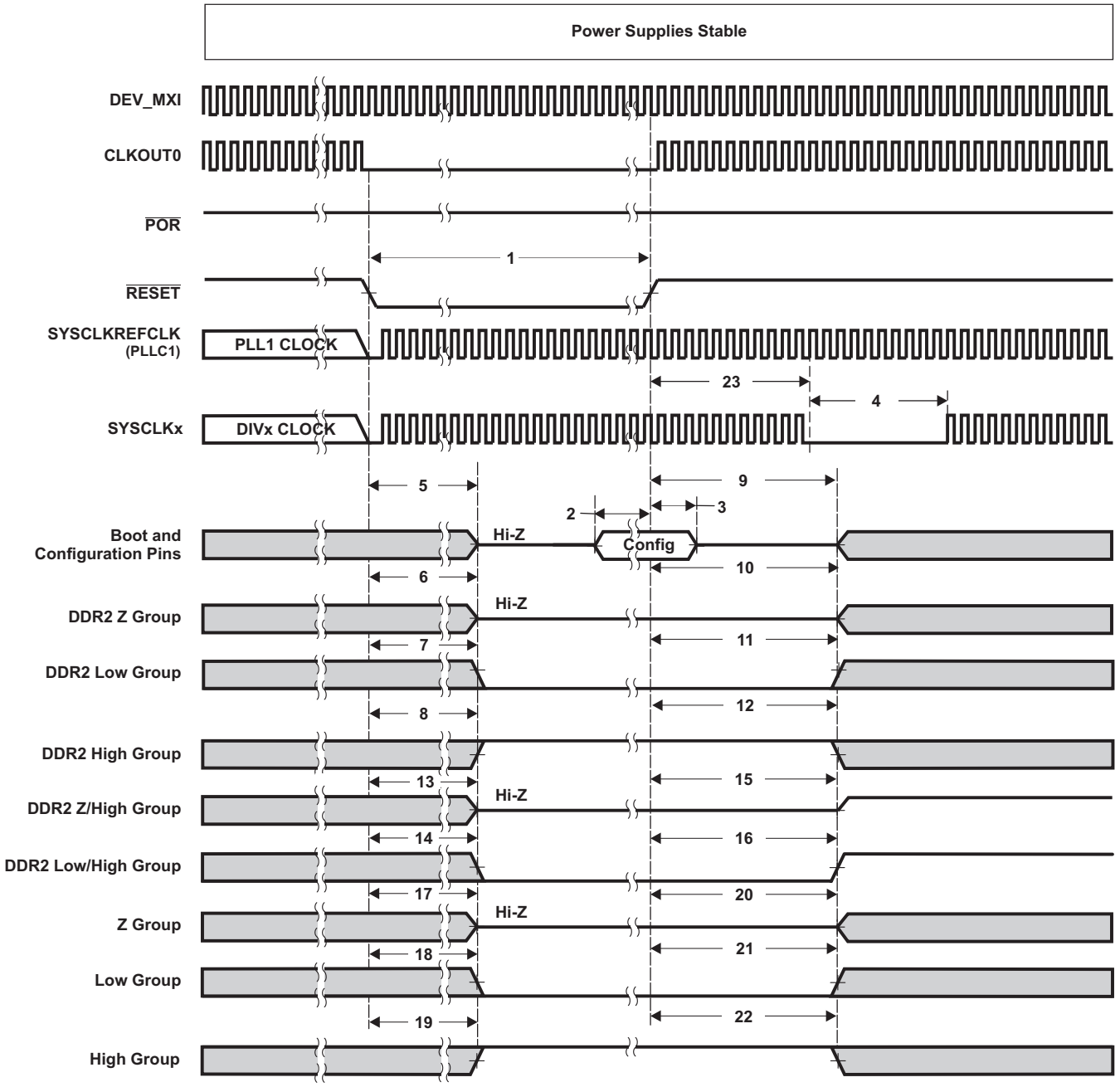



A. Power supplies and DEV_MXI must be stable before the start of $t_{W(RESET)}$.

B. Pin reset behavior depends on which peripheral defaults to controlling the multiplexed pin. For more details on what pin group (e.g., Z Group, Z/Low Group, Z/High Group, etc.) each pin belongs to, see Section 7.7.8, *Pin Behaviors at Reset*.

**Figure 7-19. Power-Up Timing**




A. Pin reset behavior depends on which peripheral defaults to controlling the multiplexed pin. For more details on what pin group (e.g., Z Group, Z/Low Group, Z/High Group, etc.) each pin belongs to, see Section 7.7.8, *Pin Behaviors at Reset*.

**Figure 7-20. Warm Reset ($\overline{\text{RESET}}$) Timing**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## 7.8 Interrupts

The DM6467T device has a large number of interrupts to service the needs of its many peripherals and subsystems. Both the ARM and C64x+ are capable of servicing these interrupts. All of the device interrupts are routed to the ARM interrupt controller with only a limited set routed to the C64x+ interrupt controller. The interrupts can be selectively enabled or disabled in either of the controllers. In typical applications, the ARM handles most of the peripheral interrupts and grants control to the C64x+ for interrupts that are relevant to DSP algorithms. Also, the ARM and DSP can communicate with each other through interrupts.

### *7.8.1 ARM CPU Interrupts*

The ARM926 CPU core supports 2 direct interrupts: FIQ and IRQ. The DM6467T ARM interrupt controller prioritizes up to 64 interrupt requests from various peripherals and subsystems, which are listed in Table 7-23, and interrupts the ARM CPU. Each interrupt is programmable for up to 8 levels of priority. There are 6 levels for IRQ and 2 levels for FIQ. Interrupts at the same priority level are serviced in order by the ARM Interrupt Number, with the lowest number having the highest priority. Table 7-24 shows the ARM interrupt controller registers and memory locations. For more details on ARM interrupt control, see the *TMS320DM646x DMSoC ARM Subsystem* Reference Guide (literature number SPRUEP9).

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**Table 7-23. DM6467T ARM Interrupts**

| ARM INTERRUPT NUMBER | ACRONYM | SOURCE | ARM INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|---|---|---|
| 0 | VP_VERTINT0 | VPIF | 32 | TINTL0 | Timer 0 lower – TINT12 |
| 1 | VP_VERTINT1 | VPIF | 33 | TINTH0 | Timer 0 upper – TINT34 |
| 2 | VP_VERTINT2 | VPIF | 34 | TINTL1 | Timer 1 lower – TINT12 |
| 3 | VP_VERTINT3 | VPIF | 35 | TINTH1 | Timer 1 upper – TINT34 |
| 4 | VP_ERRINT | VPIF | 36 | PWMINT0 | PWM 0 |
| 5 | - | Reserved | 37 | PWMINT1 | PWM 1 |
| 6 | - | Reserved | 38 | VLQINT | VLYNQ |
| 7 | WDINT | WD Timer (TIMER 2) – TINT12 | 39 | I2CINT | I2C |
| 8 | CRGENINT0 | CRGEN 0 | 40 | UARTINT0 | UART 0 |
| 9 | CRGENINT1 | CRGEN 1 | 41 | UARTINT1 | UART 1 |
| 10 | TSINT0 | TSIF 0 | 42 | UARTINT2 | UART 2 |
| 11 | TSINT1 | TSIF 1 | 43 | SPINT0 | SPI |
| 12 | VDCEINT | VDCE | 44 | SPINT1 | SPI |
| 13 | USBINT | USB | 45 | DSP2ARM0 | DSP Controller to ARM |
| 14 | USBDMAINT | USB DMA | 46 | - | Reserved |
| 15 | PCIINT | PCI | 47 | PSCINT | Power and Sleep Controller |
| 16 | CCINT0 | EDMA CC Region 0 | 48 | GPIO0 | GPIO |
| 17 | CCERRINT | EDMA CC Error | 49 | GPIO1 | GPIO |
| 18 | TCERRINT0 | EDMA TC 0 Error | 50 | GPIO2 | GPIO |
| 19 | TCERRINT1 | EDMA TC 1 Error | 51 | GPIO3 | GPIO |
| 20 | TCERRINT2 | EDMA TC 2 Error | 52 | GPIO4 | GPIO |
| 21 | TCERRINT3 | EDMA TC 3 Error | 53 | GPIO5 | GPIO |
| 22 | IDEINT | ATA | 54 | GPIO6 | GPIO |
| 23 | HPIINT | HPI | 55 | GPIO7 | GPIO |
| 24 | MAC_RXTH | EMAC RX Threshold | 56 | GPIOBNK0 | GPIO Bank 0 |
| 25 | MAC_RX | EMAC Receive | 57 | GPIOBNK1 | GPIO Bank 1 |
| 26 | MAC_TX | EMAC Transmit | 58 | GPIOBNK2 | GPIO Bank 2 |
| 27 | MAC_MISC | EMAC Miscellaneous | 59 | DDRINT | DDR2 Memory Controller |
| 28 | AXINT0 | McASP0 Transmit | 60 | EMIFAINT | EMIFA |
| 29 | ARINT0 | McASP0 Receive | 61 | COMMTX | ARMSS |
| 30 | AXINT1 | McASP1 Transmit | 62 | COMMRX | ARMSS |
| 31 | - | Reserved | 63 | EMUINT | E2ICE |


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**Table 7-24. ARM Interrupt Controller Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C4 8000 | FIQ0 | FIQ Interrupt Status 0 [Interrupt Status of INT[31:0] (If Mapped to FIQ)] |
| 0x01C4 8004 | FIQ1 | FIQ Interrupt Status 1 [Interrupt Status of INT[63:32] (If Mapped to FIQ)] |
| 0x01C4 8008 | IRQ0 | IRQ Interrupt Status 0 [Interrupt Status of INT[31:0] (If Mapped to IRQ)] |
| 0x01C4 800C | IRQ1 | IRQ Interrupt Status 1 [Interrupt Status of INT[63:32] (If Mapped to IRQ)] |
| 0x01C4 8010 | FIQENTRY | Entry Address [28:0] for Valid FIQ Interrupt |
| 0x01C4 8014 | IRQENTRY | Entry Address [28:0] for Valid IRQ Interrupt |
| 0x01C4 8018 | EINT0 | Interrupt Enable Register 0 |
| 0x01C4 801C | EINT1 | Interrupt Enable Register 1 |
| 0x01C4 8020 | INCTL | Interrupt Operation Control Register |
| 0x01C4 8024 | EABASE | Interrupt Entry Table Base Address Register |
| 0x01C4 8028 - 0x01C4 802F | - | Reserved |
| 0x01C4 8030 | INTPRI0 | Interrupt 0-7 Priority Select |
| 0x01C4 8034 | INTPRI1 | Interrupt 8-15 Priority Select |
| 0x01C4 8038 | INTPRI2 | Interrupt 16-23 Priority Select |
| 0x01C4 803C | INTPRI3 | Interrupt 24-31 Priority Select |
| 0x01C4 8040 | INTPRI4 | Interrupt 32-39 Priority Select |
| 0x01C4 8044 | INTPRI5 | Interrupt 40-47 Priority Select |
| 0x01C4 8048 | INTPRI6 | Interrupt 48-55 Priority Select |
| 0x01C4 804C | INTPRI7 | Interrupt 56-63 Priority Select |
| 0x01C4 8050 - 0x01C4 83FF | - | Reserved |

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### 7.8.2 DSP Interrupts

The C64x+ DSP interrupt controller combines device events into 12 prioritized interrupts. The source for each of the 12 CPU interrupts is user-programmable and is listed in Table 7-25. Also, the interrupt controller controls the generation of the CPU exception, NMI, and emulation interrupts. Table 7-26 summarizes the C64x+ interrupt controller registers and memory locations. For more details on DSP interrupt control, see the *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (literature number SPRUEP8).

**Table 7-25. DM6467T DSP Interrupts**

| DSP INTERRUPT NUMBER | ACRONYM | SOURCE | DSP INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|---|---|---|
| 0 | EVT0 | C64x+ Int Ctl 0 | 64 | GPIO0 | GPIO |
| 1 | EVT1 | C64x+ Int Ctl 1 | 65 | GPIO1 | GPIO |
| 2 | EVT2 | C64x+ Int Ctl 2 | 66 | GPIO2 | GPIO |
| 3 | EVT3 | C64x+ Int Ctl 3 | 67 | GPIO3 | GPIO |
| 4 | TINTL0 | Timer 0 lower – TINT12 | 68 | GPIO4 | GPIO |
| 5 | TINTH0 | Timer 0 upper – TINT34 | 69 | GPIO5 | GPIO |
| 6 | TINTL1 | Timer 1 lower – TINT12 | 70 | GPIO6 | GPIO |
| 7 | TINTH1 | Timer 1 upper – TINT34 | 71 | GPIO7 | GPIO |
| 8 | – | Reserved | 72 | – | Reserved |
| 9 | EMU_DTDMA | C64x+ EMC | 73 | – | Reserved |
| 10 | – | Reserved | 74 | – | Reserved |
| 11 | EMU_RTDXRX | C64x+ RTDX | 75 | – | Reserved |
| 12 | EMU_RTDXTX | C64x+ RTDX | 76 | – | Reserved |
| 13 | IDMAINT0 | C64x+ EMC 0 | 77 | – | Reserved |
| 14 | IDMAINT1 | C64x+ EMC 1 | 78 | – | Reserved |
| 15 | – | Reserved | 79 | – | Reserved |
| 16 | ARM2DSP0 | ARM to DSP Controller 0 | 80 | – | Reserved |
| 17 | ARM2DSP1 | ARM to DSP Controller 1 | 81 | – | Reserved |
| 18 | ARM2DSP2 | ARM to DSP Controller 2 | 82 | – | Reserved |
| 19 | ARM2DSP3 | ARM to DSP Controller 3 | 83 | – | Reserved |
| 20 | – | Reserved | 84 | CCINT1 | EDMA CC Region 1 |
| 21 | – | Reserved | 85 | CCERRINT | EDMA CC Error |
| 22 | – | Reserved | 86 | TCERRINT0 | EDMA TC0 Error |
| 23 | – | Reserved | 87 | TCERRINT1 | EDMA TC1 Error |
| 24 | – | Reserved | 88 | TCERRINT2 | EDMA TC2 Error |
| 25 | – | Reserved | 89 | TCERRINT3 | EDMA TC3 Error |
| 26 | – | Reserved | 90 | IDEINT | ATA |
| 27 | – | Reserved | 91 | – | Reserved |
| 28 | – | Reserved | 92 | – | Reserved |
| 29 | – | Reserved | 93 | – | Reserved |
| 30 | – | Reserved | 94 | – | Reserved |
| 31 | – | Reserved | 95 | – | Reserved |
| 32 | – | Reserved | 96 | INTERR | C64x+ Interrupt Controller Dropped CPU Interrupt Event |
| 33 | – | Reserved | 97 | EMC_IDMAERR | C64x+ EMC Invalid IDMA Parameters |
| 34 | – | Reserved | 98 | – | Reserved |
| 35 | – | Reserved | 99 | – | Reserved |
| 36 | – | Reserved | 100 | – | Reserved |


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**Table 7-25. DM6467T DSP Interrupts (continued)**

| DSP INTERRUPT NUMBER | ACRONYM | SOURCE | DSP INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|---|---|---|
| 37 | – | Reserved | 101 | – | Reserved |
| 38 | – | Reserved | 102 | – | Reserved |
| 39 | – | Reserved | 103 | – | Reserved |
| 40 | – | Reserved | 104 | – | Reserved |
| 41 | – | Reserved | 105 | – | Reserved |
| 42 | – | Reserved | 106 | – | Reserved |
| 43 | – | Reserved | 107 | – | Reserved |
| 44 | – | Reserved | 108 | – | Reserved |
| 45 | – | Reserved | 109 | – | Reserved |
| 46 | – | Reserved | 110 | – | Reserved |
| 47 | – | Reserved | 111 | – | Reserved |
| 48 | – | Reserved | 112 | – | Reserved |
| 49 | – | Reserved | 113 | PMC_ED | C64x+ PMC |
| 50 | – | Reserved | 114 | – | Reserved |
| 51 | – | Reserved | 115 | – | Reserved |
| 52 | – | Reserved | 116 | UMCED1 | C64x+ UMC 1 |
| 53 | – | Reserved | 117 | UMCED2 | C64x+ UMC 2 |
| 54 | AXINT0 | McASP 0 Transmit | 118 | PDCINT | C64x+ PDC |
| 55 | ARINT0 | McASP 0 Receive | 119 | SYSCMPA | C64x+ SYS |
| 56 | AXINT1 | McASP 1 Transmit | 120 | PMCCMPA | C64x+ PMC |
| 57 | – | Reserved | 121 | PMCDMPA | C64x+ PMC |
| 58 | – | Reserved | 122 | DMCCMPA | C64x+ DMC |
| 59 | – | Reserved | 123 | DMCDMPA | C64x+ DMC |
| 60 | – | Reserved | 124 | UMCCMPA | C64x+ UMC |
| 61 | – | Reserved | 125 | UMCDMPA | C64x+ UMC |
| 62 | – | Reserved | 126 | EMCCMPA | C64x+ EMC |
| 63 | – | Reserved | 127 | EMCBUSERR | C64x+ EMC |

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**Table 7-26. C64x+ Interrupt Controller Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x0180 0000 | EVTFLAG0 | Event flag register 0 |
| 0x0180 0004 | EVTFLAG1 | Event flag register 1 |
| 0x0180 0008 | EVTFLAG2 | Event flag register 2 |
| 0x0180 000C | EVTFLAG3 | Event flag register 3 |
| 0x0180 0020 | EVTSET0 | Event set register 0 |
| 0x0180 0024 | EVTSET1 | Event set register 1 |
| 0x0180 0028 | EVTSET2 | Event set register 2 |
| 0x0180 002C | EVTSET3 | Event set register 3 |
| 0x0180 0040 | EVTCLR0 | Event clear register 0 |
| 0x0180 0044 | EVTCLR1 | Event clear register 1 |
| 0x0180 0048 | EVTCLR2 | Event clear register 2 |
| 0x0180 004C | EVTCLR3 | Event clear register 3 |
| 0x0180 0080 | EVTMASK0 | Event mask register 0 |
| 0x0180 0084 | EVTMASK1 | Event mask register 1 |
| 0x0180 0088 | EVTMASK2 | Event mask register 2 |
| 0x0180 008C | EVTMASK3 | Event mask register 3 |
| 0x0180 00A0 | MEVTFLAG0 | Masked event flag register 0 |
| 0x0180 00A4 | MEVTFLAG1 | Masked event flag register 1 |
| 0x0180 00A8 | MEVTFLAG2 | Masked event flag register 2 |
| 0x0180 00AC | MEVTFLAG3 | Masked event flag register 3 |
| 0x0180 00C0 | EXPMASK0 | Exception mask register 0 |
| 0x0180 00C4 | EXPMASK1 | Exception mask register 1 |
| 0x0180 00C8 | EXPMASK2 | Exception mask register 2 |
| 0x0180 00CC | EXPMASK3 | Exception mask register 3 |
| 0x0180 00E0 | MEXPFLAG0 | Masked exception flag register 0 |
| 0x0180 00E4 | MEXPFLAG1 | Masked exception flag register 1 |
| 0x0180 00E8 | MEXPFLAG2 | Masked exception flag register 2 |
| 0x0180 00EC | MEXPFLAG3 | Masked exception flag register 3 |
| 0x0180 0104 | INTMUX1 | Interrupt mux register 1 |
| 0x0180 0108 | INTMUX2 | Interrupt mux register 2 |
| 0x0180 010C | INTMUX3 | Interrupt mux register 3 |
| 0x0180 0180 | INTXSTAT | Interrupt exception status |
| 0x0180 0184 | INTXCLR | Interrupt exception clear |
| 0x0180 0188 | INTDMASK | Dropped interrupt mask register |


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## 7.9 External Memory Interface (EMIF)

DM6467T supports several memory and external device interfaces, including:

- Asynchronous EMIF (EMIFA) for interfacing to NOR Flash, SRAM, etc.
- NAND Flash
- ATA (see Section 7.20, *ATA Controller*)

### *7.9.1 Asynchronous EMIF (EMIFA)*

The DM6467T Asynchronous EMIF (EMIFA) provides an 8-bit or 16-bit data bus, an address bus width up to 24 bits, and 4 chip selects, along with memory control signals. These signals are multiplexed between these peripherals:

- EMIFA and NAND interfaces
- ATA interface
- Host-Port Interface (HPI)
- PCI
- GPIO

### *7.9.2 NAND (NAND, SmartMedia/SSFDC, xD)*

The EMIFA interface provides both the asynchronous EMIF and NAND interfaces. Four chip selects are provided and each are individually configurable to provide either EMIFA or NAND support. The NAND features supported are as follows.

- NAND flash on up to 4 asynchronous chip selects
- 8- or 16-bit data bus width
- Programmable cycle timings
- Performs ECC calculation
- NAND Mode also supports SmartMedia/SSFDC (Solid State Floppy Disk Controller) and xD memory cards
- ARM ROM supports booting of the DM6467T ARM926 processor from NAND flash located at CS2

The memory map for EMIFA and NAND registers is shown in Table 7-27. For more details on the EMIFA and NAND interfaces, the *TMS320DM646x DMSoC Asynchronous External Memory Interface (EMIF)* User's Guide (literature number SPRUEQ7).

### *7.9.3 EMIFA Peripheral Register Description(s)*

Table 7-27 shows the EMIFA/NAND registers.

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**Table 7-27. EMIFA/NAND Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x2000 8000 | RCSR | Revision Code and Status Register |
| 0x2000 8004 | AWCCR | Asynchronous Wait Cycle Configuration Register |
| 0x2000 8008 - 0x2000 800F | – | Reserved |
| 0x2000 8010 | A1CR | Asynchronous 1 Configuration Register (CS2 Space) |
| 0x2000 8014 | A2CR | Asynchronous 2 Configuration Register (CS3 Space) |
| 0x2000 8018 | A3CR | Asynchronous 3 Configuration Register (CS4 Space) |
| 0x2000 801C | A4CR | Asynchronous 4 Configuration Register (CS5 Space) |
| 0x2000 8020 - 0x2000 803F | – | Reserved |
| 0x2000 8040 | EIRR | EMIF Interrupt Raw Register |
| 0x2000 8044 | EIMR | EMIF Interrupt Mask Register |
| 0x2000 8048 | EIMSR | EMIF Interrupt Mask Set Register |
| 0x2000 804C | EIMCR | EMIF Interrupt Mask Clear Register |
| 0x2000 8050 - 0x2000 805F | – | Reserved |
| 0x2000 8060 | NANDFCR | NAND Flash Control Register |
| 0x2000 8064 | NANDFSR | NAND Flash Status Register |
| 0x2000 8070 | NANDF1ECC | NAND Flash 1 ECC Register (CS2 Space) |
| 0x2000 8074 | NANDF2ECC | NAND Flash 2 ECC Register (CS3 Space) |
| 0x2000 8078 | NANDF3ECC | NAND Flash 3 ECC Register (CS4 Space) |
| 0x2000 807C | NANDF4ECC | NAND Flash 4 ECC Register (CS5 Space) |
| 0x2000 8080 - 0x2000 8FFF | – | Reserved |


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### 7.9.4 EMIFA Electrical Data/Timing

**Table 7-28. Timing Requirements for Asynchronous Memory Cycles for EMIFA Module(1) (see Figure 7-21 and Figure 7-22)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| **READS and WRITES** | | | | | |
| 2 | $t_{w(EM_WAIT)}$ | Pulse duration, EM_WAITx assertion and deassertion | 2E | | ns |
| **READS** | | | | | |
| 12 | $t_{su(EMDV-EMOEH)}$ | Setup time, EM_D[15:0] valid before $\overline{EM_OE}$ high | 5 | | ns |
| 13 | $t_{h(EMOEH-EMDIV)}$ | Hold time, EM_D[15:0] valid after $\overline{EM_OE}$ high | 0 | | ns |
| 14 | $t_{su\ (EMWAIT-EMOEH)}$ | Setup time, EM_WAITx asserted before $\overline{EM_OE}$ high(2) | 4E + 3 | | ns |
| **WRITES** | | | | | |
| 28 | $t_{\ su(EMWAIT-EMWEH)}$ | Setup time, EM_WAITx asserted before $\overline{EM_WE}$ high(2) | 4E + 3 | | ns |

(1) E = SYSCLK3 period in ns for EMIFA. For example, when running the DSP CPU at 1 GHz, use E = 4 ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. Figure 7-23 and Figure 7-24 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

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**Table 7-29. Switching Characteristics Over Recommended Operating Conditions for Asynchronous Memory Cycles for EMIFA Module(1) (2) (see Figure 7-21 and Figure 7-22)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| **READS and WRITES** | | | | | |
| 1 | $t_{d(TURNAROUND)}$ | Turn around time | (TA + 1) * E - 3 | (TA + 1) * E + 3 | ns |
| **READS** | | | | | |
| 3 | $t_{c(EMRCYCLE)}$ | EMIF read cycle time (EW = 0) | (RS + RST + RH + TA + 4) * E - 3 | (RS + RST + RH + TA + 4) * E + 3 | ns |
| | | EMIF read cycle time (EW = 1) | (RS + RST + RH + TA + 4) * E - 3 | 4184 * E + 3 | ns |
| 4 | $t_{su(EMCSL-EMOEL)}$ | Output setup time, $\overline{EM_CS[5:2]}$ low to $\overline{EM_OE}$ low (SS = 0) | (RS + 1) * E - 3 | (RS + 1) * E + 3 | ns |
| | | Output setup time, $\overline{EM_CS[5:2]}$ low to $\overline{EM_OE}$ low (SS = 1) | 3 | | ns |
| 5 | $t_{h(EMOEH-EMCSH)}$ | Output hold time, $\overline{EM_OE}$ high to $\overline{EM_CS[5:2]}$ high (SS = 0) | (RH + 1) * E - 3 | (RH + 1) * E + 3 | ns |
| | | Output hold time, $\overline{EM_OE}$ high to $\overline{EM_CS[5:2]}$ high (SS = 1) | 3 | | ns |
| 6 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, EM_BA[1:0] valid to $\overline{EM_OE}$ low | (RS + 1) * E - 3 | (RS + 1) * E + 3 | ns |
| 7 | $t_{h(EMOEH-EMBAIV)}$ | Output hold time, $\overline{EM_OE}$ high to EM_BA[1:0] invalid | (RH + 1) * E - 3 | (RH + 1) * E + 3 | ns |
| 8 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, EM_A[22:0] valid to $\overline{EM_OE}$ low | (RS + 1) * E - 3 | (RS + 1) * E + 3 | ns |
| 9 | $t_{h(EMOEH-EMBAIV)}$ | Output hold time, $\overline{EM_OE}$ high to EM_A[22:0] invalid | (RH + 1) * E - 3 | (RH + 1) * E + 3 | ns |
| 10 | $t_{w(EMOEL)}$ | $\overline{EM_OE}$ active low width (EW = 0) | (RST + 1) * E - 3 | (RST + 1) * E + 3 | ns |
| | | $\overline{EM_OE}$ active low width (EW = 1) | (RST + 1) * E - 3 | (RST + 4097) * E + 3 | ns |
| 11 | $t_{d(EMWAITH-EMOEH)}$ | Delay time from EM_WAITx deasserted to $\overline{EM_OE}$ high | | 4E + 3 | ns |
| **WRITES** | | | | | |
| 15 | $t_{c(EMWCYCLE)}$ | EMIF write cycle time (EW = 0) | (WS + WST + WH + TA + 4) * E - 3 | (WS + WST + WH + TA + 4) * E + 3 | ns |
| | | EMIF write cycle time (EW = 1) | (WS + WST + WH + TA + 4) * E - 3 | 4184 * E + 3 | ns |
| 16 | $t_{su(EMCSL-EMWEL)}$ | Output setup time, $\overline{EM_CS[5:2]}$ low to $\overline{EM_WE}$ low (SS = 0) | (WS + 1) * E - 3 | (WS + 1) * E + 3 | ns |
| | | Output setup time, $\overline{EM_CS[5:2]}$ low to $\overline{EM_WE}$ low (SS = 1) | 3 | | ns |
| 17 | $t_{h(EMWEH-EMCSH)}$ | Output hold time, $\overline{EM_WE}$ high to $\overline{EM_CS[5:2]}$ high (SS = 0) | (WH + 1) * E - 3 | (WH + 1) * E + 3 | ns |
| | | Output hold time, $\overline{EM_WE}$ high to $\overline{EM_CS[5:2]}$ high (SS = 1) | 3 | | ns |
| 18 | $t_{su(EMRNW-EMWEL)}$ | Output setup time, EM_R/$\overline{W}$ valid to $\overline{EM_WE}$ low | (WS + 1) * E - 3 | (WS + 1) * E + 3 | ns |
| 19 | $t_{h(EMWEH-EMRNW)}$ | Output hold time, $\overline{EM_WE}$ high to EM_R/$\overline{W}$ invalid | (WH + 1) * E - 3 | (WH + 1) * E + 3 | ns |
| 20 | $t_{su(EMBAV-EMWEL)}$ | Output setup time, EM_BA[1:0] valid to $\overline{EM_WE}$ low | (WS + 1) * E - 3 | (WS + 1) * E + 3 | ns |
| 21 | $t_{h(EMWEH-EMBAIV)}$ | Output hold time, $\overline{EM_WE}$ high to EM_BA[1:0] invalid | (WH + 1) * E - 3 | (WH + 1) * E + 3 | ns |
| 22 | $t_{su(EMAV-EMWEL)}$ | Output setup time, EM_A[22:0] valid to $\overline{EM_WE}$ low | (WS + 1) * E - 3 | (WS + 1) * E + 3 | ns |
| 23 | $t_{h(EMWEH-EMAIV)}$ | Output hold time, $\overline{EM_WE}$ high to EM_A[22:0] invalid | (WH + 1) * E - 3 | (WH + 1) * E + 3 | ns |
| 24 | $t_{w(EMWEL)}$ | $\overline{EM_WE}$ active low width (EW = 0) | (WST + 1) * E - 3 | (WST + 1) * E + 3 | ns |
| | | $\overline{EM_WE}$ active low width (EW = 1) | (WST + 1) * E - 3 | (WST + 4097) * E + 3 | ns |
| 25 | $t_{d(EMWAITH-EMWEH)}$ | Delay time from EM_WAITx deasserted to $\overline{EM_WE}$ high | | 4E + 3 | ns |
| 26 | $t_{su(EMDV-EMWEL)}$ | Output setup time, EM_D[15:0] valid to $\overline{EM_WE}$ low | (WS + 1) * E - 3 | (WS + 1) * E + 3 | ns |

(1) RS = Read setup, RST = Read Strobe, RH = Read Hold, WS = Write Setup, WST = Write Strobe, WH = Write Hold, TA = Turn Around, EW = Extend Wait mode, SS = Select Strobe mode. These parameters are programmed via the Asynchronous n Configuration and the Asynchronous Wait Cycle Configuration registers and support the following range of values: TA[0–3], RS[0–15], RST[0–63], RH[0–7], WS[0–15], WST[0–63], WH[0–7], EW[0–1], and MEWC[0–255]. For more information, see the *TMS320DM646x DMSoC Asynchronous External Memory Interface (EMIF)* User's Guide (literature number SPRUEQ7).

(2) E = SYSCLK3 period in ns for EMIFA. For example, when running the DSP CPU at 1 GHz, use E = 4 ns.


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**Table 7-29. Switching Characteristics Over Recommended Operating Conditions for Asynchronous Memory Cycles for EMIFA Module[1] [2] (see Figure 7-21 and Figure 7-22) (continued)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 27 | $t_{h(EMWEH-EMDIV)}$ | Output hold time, $\overline{EM_WE}$ high to EM_D[15:0] invalid | (WH + 1) * E - 3 | (WH + 1) * E + 3 | ns |

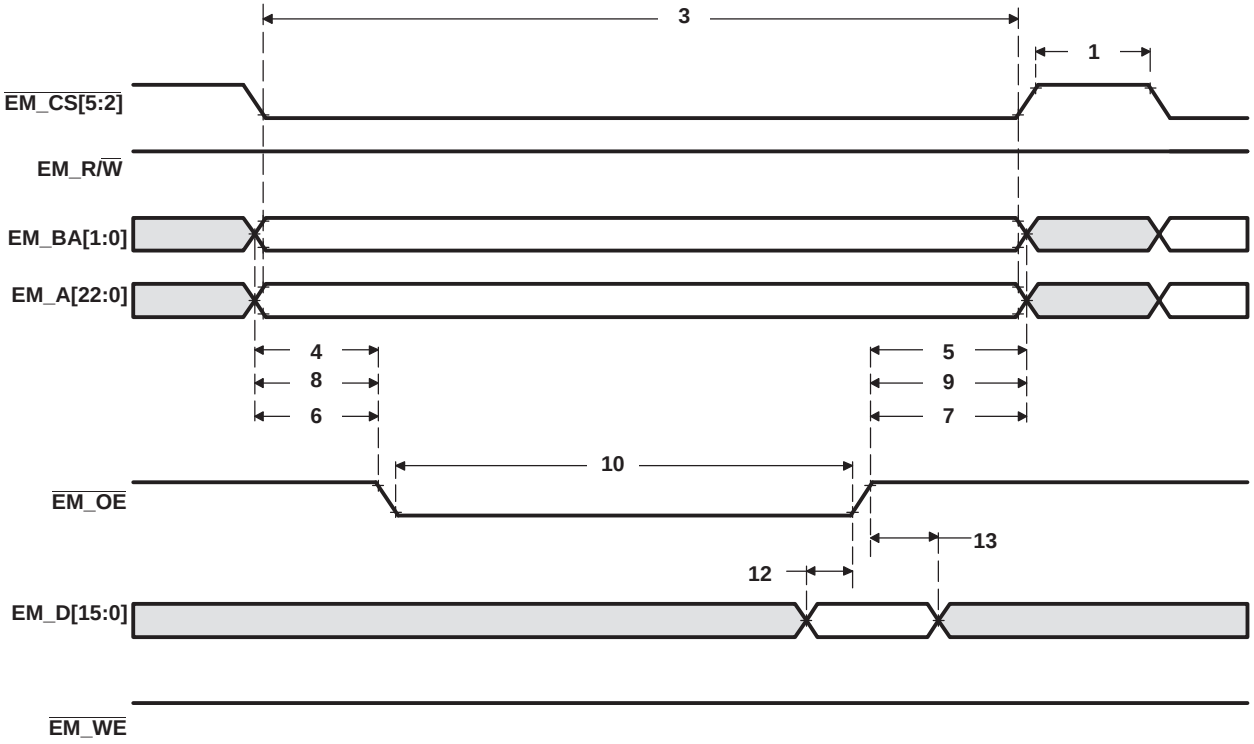


**Figure 7-21. Asynchronous Memory Read Timing for EMIF**

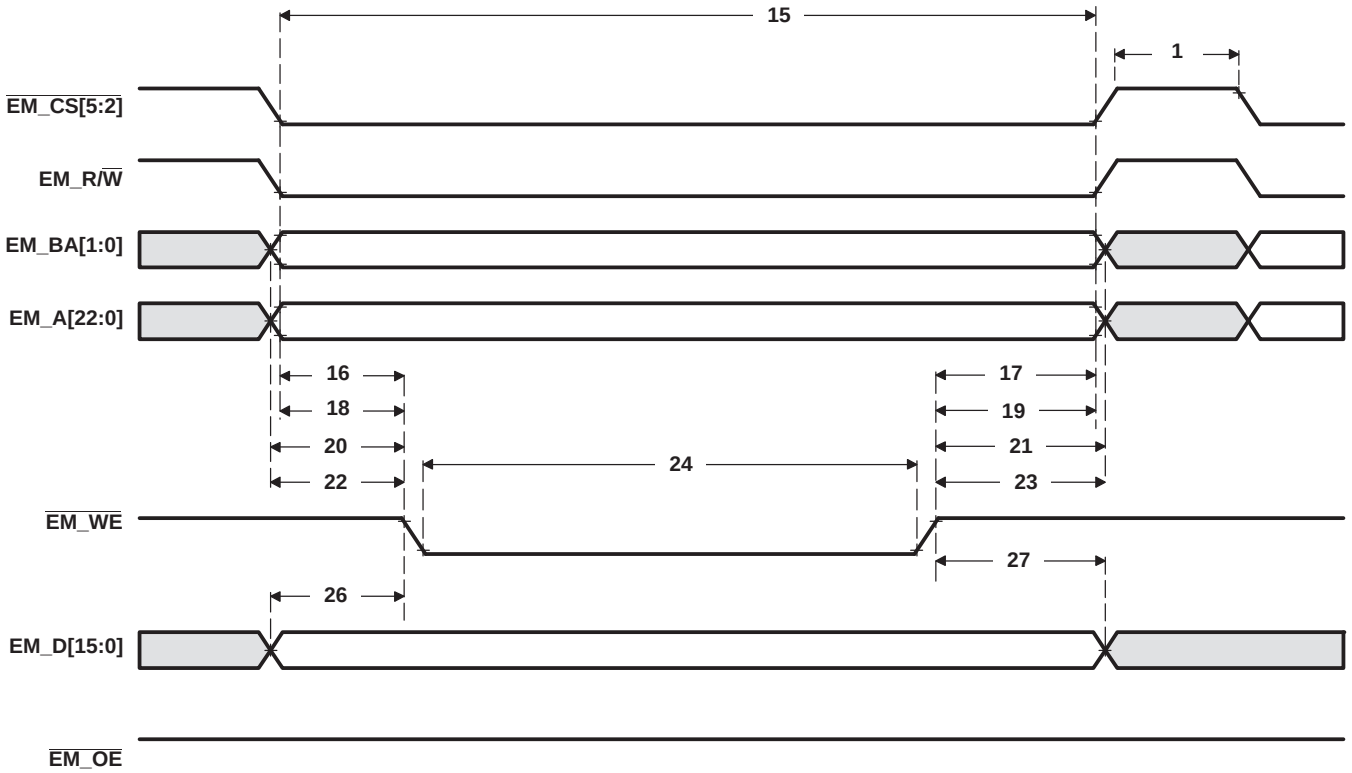


**Figure 7-22. Asynchronous Memory Write Timing for EMIF**

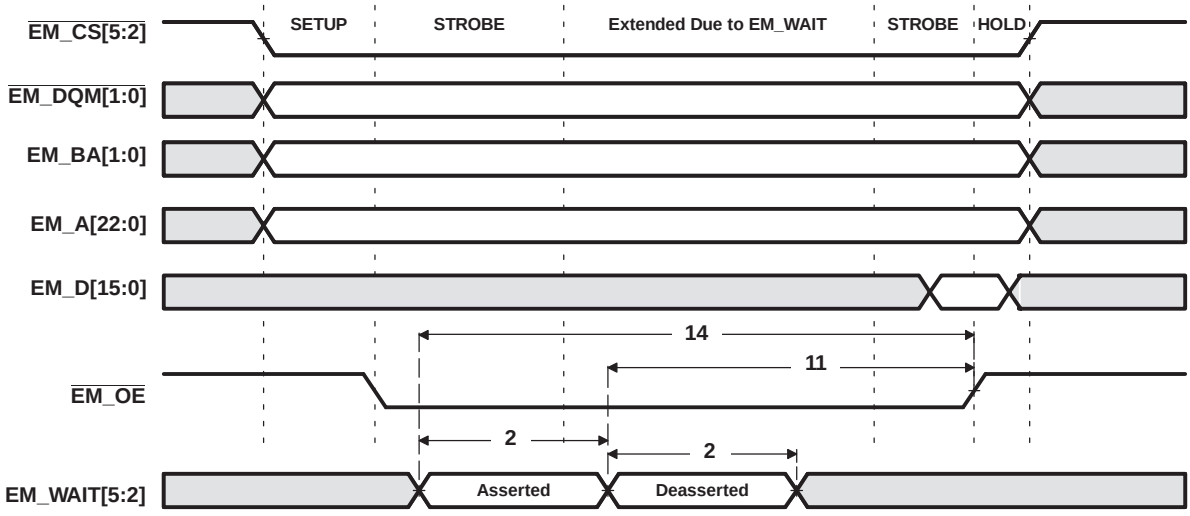


**Figure 7-23. EM_WAITx Read Timing Requirements**


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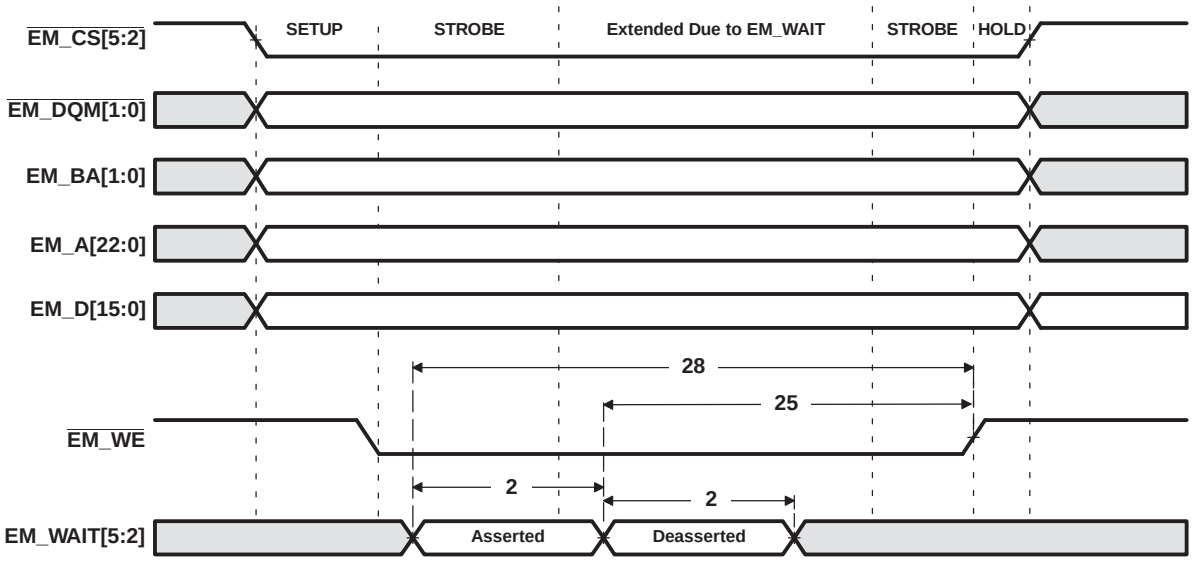


**Figure 7-24. EM_WAITx Write Timing Requirements**

## 7.10 DDR2 Memory Controller

The DDR2 Memory Controller is a dedicated interface to DDR2 SDRAM. It supports JESD79D-2A standard compliant DDR2 SDRAM devices and can interface to either 16-bit or 32-bit DDR2 SDRAM devices. For details on the DDR2 Memory Controller, see the *TMS320DM646x DMSoC DDR2 Memory Controller User's Guide* (literature number SPRUEQ4).

A memory map of the DDR2 Memory Controller registers is shown in Table 7-30.

**Table 7-30. DDR2 Memory Controller Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C4 004C | – | Reserved |
| 0x01C4 2038 | – | Reserved |
| 0x2000 0000 - 0x2000 0003 | – | Reserved |
| 0x2000 0004 | SDRSTAT | SDRAM Status Register |
| 0x2000 0008 | SDBCR | SDRAM Bank Configuration Register |
| 0x2000 000C | SDRCR | SDRAM Refresh Control Register |
| 0x2000 0010 | SDTIMR | SDRAM Timing Register 1 |
| 0x2000 0014 | SDTIMR2 | SDRAM Timing Register 2 |
| 0x2000 0018 - 0x2000 001F | – | Reserved |
| 0x2000 0020 | PBBPR | Peripheral Bus Burst Priority Register |
| 0x2000 0024 - 0x2000 00BF | – | Reserved |
| 0x2000 00C0 | IRR | Interrupt Raw Register |
| 0x2000 00C4 | IMR | Interrupt Masked Register |
| 0x2000 00C8 | IMSR | Interrupt Mask Set Register |
| 0x2000 00CC | IMCR | Interrupt Mask Clear Register |
| 0x2000 00D0 - 0x2000 00E3 | – | Reserved |
| 0x2000 00E4 | DDRPHYCR | DDR2 PHY Control Register |
| 0x2000 00E8 - 0x2000 00EF | – | Reserved |
| 0x2000 00F0 | VTPIOCR | DDR2 VTP IO Control Register |
| 0x2000 00F4 - 0x2000 7FFF | – | Reserved |


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### 7.10.1 DDR2 Memory Controller Electrical Data/Timing

TI only supports board designs that follow the guidelines outlined in this document.

**Table 7-31. Switching Characteristics Over Recommended Operating Conditions for DDR2 Memory Controller(1) (2) (see Figure 7-25)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(DDR_CLK)}$ | Cycle time, DDR_CLK | 2.5 | 8 | ns |
| 2 | $f_{(DDR_CLK)}$ | Frequency, DDR_CLK | 125 | 400 | MHz |

(1) DDR_CLK cycle time = 2 x PLL2 _SYSCLK1 cycle time.
(2) The PLL2 Controller ***must*** be programmed such that the resulting DDR_CLK clock frequency is within the specified range.

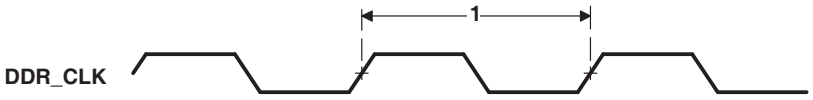


**Figure 7-25. DDR2 Memory Controller Clock Timing**

### 7.10.2 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR2 specification, see *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* Application Report (SPRAAV0).

#### 7.10.2.1 DDR2 Interface Schematic

Figure 7-26 shows the DDR2 interface schematic for a x32 DDR2 memory system. The x16 DDR2 system schematic is identical except that the high word DDR2 device is deleted, see Figure 7-27. The pin numbers for the DM6467T can be obtained from the Section 3.6, *Pin Assignments* of this document.

#### 7.10.2.2 Compatible JEDEC DDR2 Devices

Table 7-32 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-800 speed grade DDR2 devices.

**Table 7-32. Compatible JEDEC DDR2 Devices**

| No. | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 1 | JEDEC DDR2 Device Speed Grade(1) | DDR2-800 | | |
| 2 | JEDEC DDR2 Device Bit Width | x16 | x16 | Bits |
| 3 | JEDEC DDR2 Device Count(2) | 1 | 2 | Devices |
| 4 | JEDEC DDR2 Device Ball Count(3) | 84 | 92 | Balls |

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
(2) 1 DDR2 device is used for 16 bit DDR2 memory system. 2 DDR2 devices are used for 32 bit DDR2 memory system.
(3) 92 ball devices retained for legacy support. New designs will migrate to 84 ball DDR2 devices. Electrrically the 92 and 84 ball DDR2 devices are the same.

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### 7.10.2.3 PCB Stackup

The minimum stackup required for routing the DM6467T is a six layer stack as shown in Table 7-33. Additional layers may be added to the PCB stack up to accommodate other circuity or to reduce the size of the PCB footprint.

**Table 7-33. DM6467T Minimum PCB Stack Up**

| Layer | Type | Description |
|---|---|---|
| 1 | Signal | Top Routing Mostly Horizontal |
| 2 | Plane | Ground |
| 3 | Plane | Power |
| 4 | Signal | Internal Routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom Routing Mostly Vertical |


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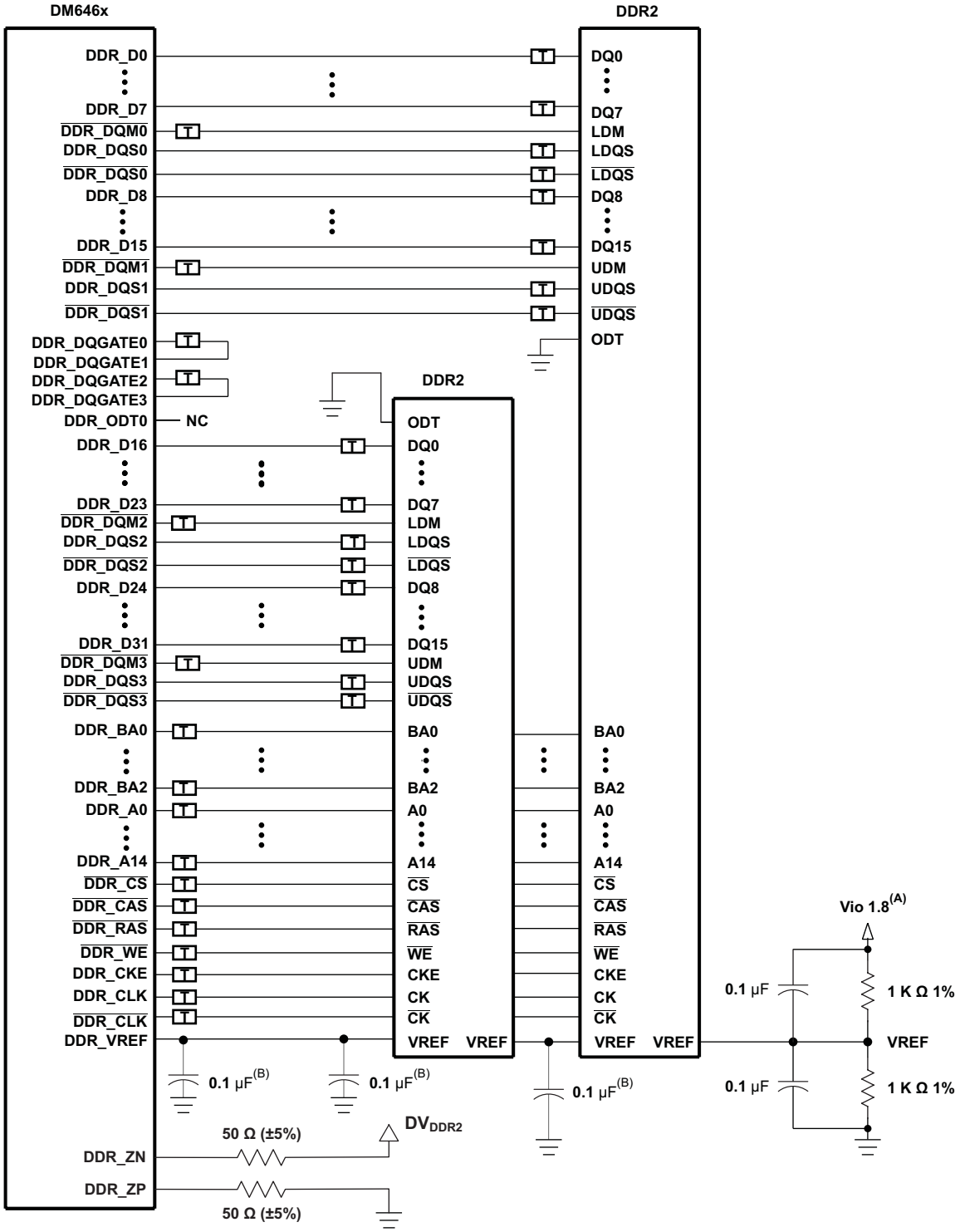
Complete stack up specifications are provided in Table 7-34.

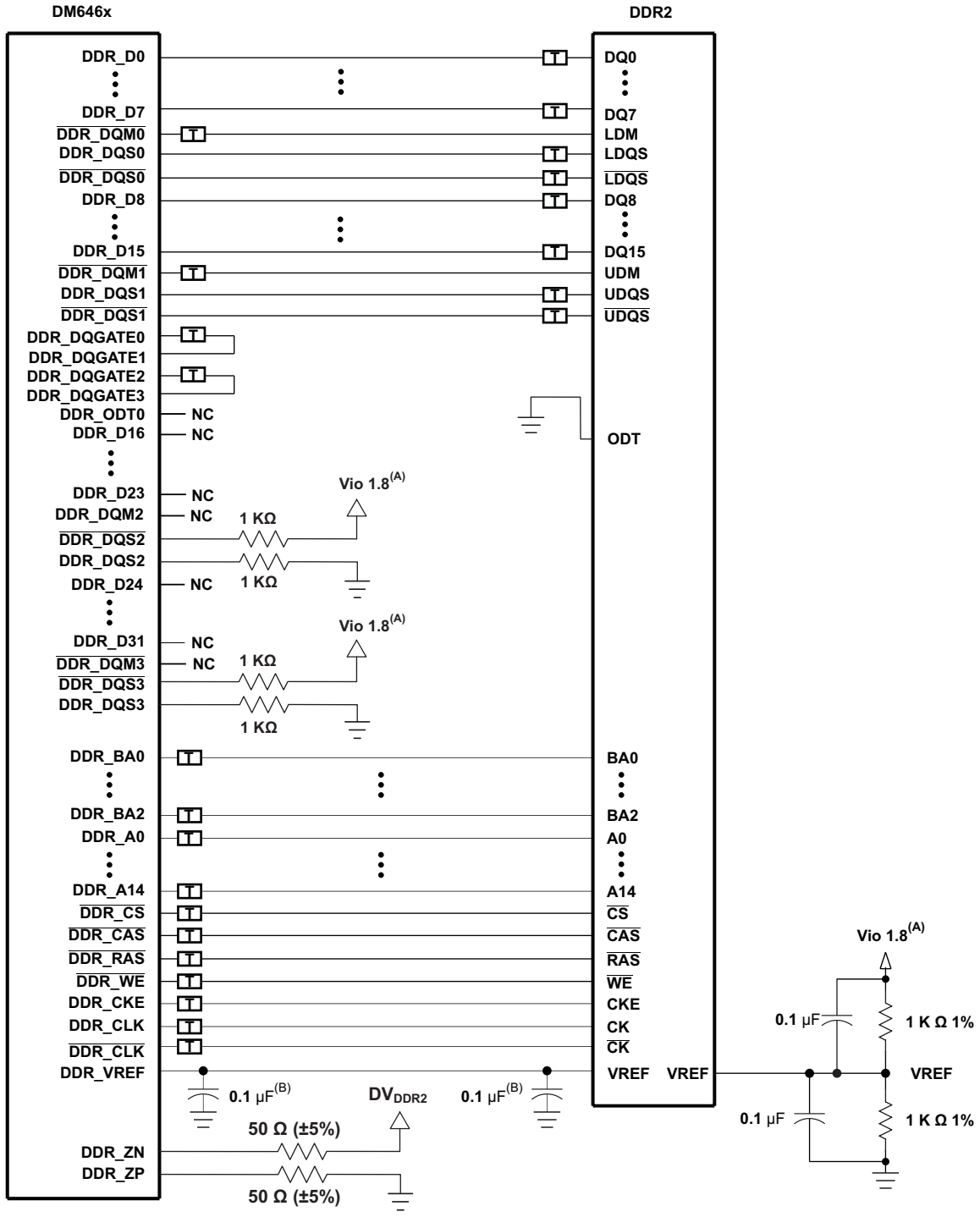



T Terminator, if desired. See terminator comments.

A Vio1.8 is the power supply for the DDR2 memories and DM646x DDR2 interface.

B One of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin.

**Figure 7-26. DM6467T 32-Bit DDR2 High Level Schematic**




T Terminator, if desired. See terminator comments.

A Vio1.8 is the power supply for the DDR2 memories and DM646x DDR2 interface.

B One of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin.

**Figure 7-27. DM6467T 16-Bit DDR2 High Level Schematic**

**Table 7-34. PCB Stack Up Specifications**

| No. | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1 | PCB Routing/Plane Layers | 6 | | | |


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**Table 7-34. PCB Stack Up Specifications (continued)**

| No. | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 2 | Signal Routing Layers | 3 | | | |
| 3 | Full ground layers under DDR2 routing Region | 2 | | | |
| 4 | Number of ground plane cuts allowed within DDR routing region | | | 0 | |
| 5 | Number of ground reference planes required for each DDR2 routing layer | 1 | | | |
| 6 | Number of layers between DDR2 routing layer and reference ground plane | | | 0 | |
| 7 | PCB Routing Feature Size | | 4 | | Mils |
| 8 | PCB Trace Width w | | 4 | | Mils |
| 8 | PCB BGA escape via pad size | | 18 | | Mils |
| 9 | PCB BGA escape via hole size | | 8 | | Mils |
| 10 | DSP Device BGA pad size(1) | | | | |
| 11 | DDR2 Device BGA pad size(2) | | | | |
| 12 | Single Ended Impedance, Zo | 50 | | 75 | Ω |
| 13 | Impedance Control(3) | Z-5 | Z | Z+5 | Ω |

(1) See the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811) for DSP device BGA pad size.
(2) See the DDR2 device manufacturer documenation for the DDR2 device BGA pad size.
(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

### 7.10.2.4 Placement

Figure 7-28 shows the required placement for the DM6467T device as well as the DDR2 devices. The dimensions for Figure 7-28 are defined in Table 7-35. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16 bit DDR memory systems, the high word DDR2 device is omitted from the placement.

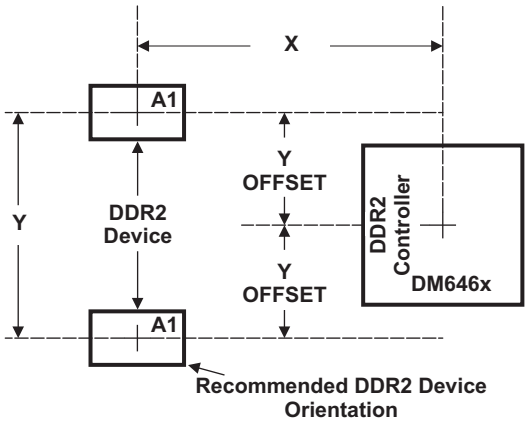


**Figure 7-28. DM6467T and DDR2 Device Placement**

**Table 7-35. Placement Specifications**

| No. | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 1 | X(1) (2) | | 1660 | Mils |
| 2 | Y(1) (2) | | 1280 | Mils |
| 3 | Y Offset(1) (2) (3) | | 650 | Mils |
| 4 | DDR2 Keepout Region(4) | | | |
| 5 | Clearance from non-DDR2 signal to DDR2 Keepout Region(5) | 4 | | w |

(1) See Figure 7-26 for dimension defintions.
(2) Measurements from center of DSP device to center of DDR2 device.
(3) For 16 bit memory systems it is recommended that Y Offset be as small as possible.
(4) DDR2 Keepout region to encompass entire DDR2 routing area
(5) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

### 7.10.2.5 DDR2 Keep Out Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keep out region is defined for this purpose and is shown in Figure 7-29. The size of this region varies with the placement and DDR routing. Additional clearances required for the keep out region are shown in Table 7-35.

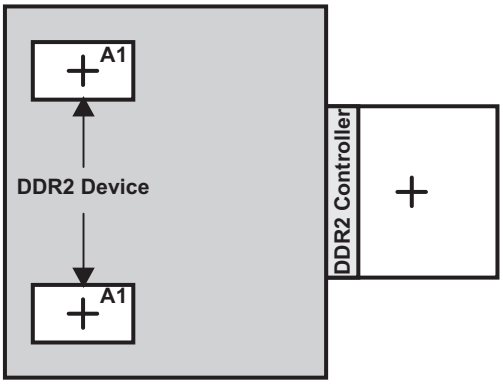


**Figure 7-29. DDR2 Keepout Region**

**NOTE**

The region shown in Figure 7-29 should encompass all the DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keep out region. Non-DDR2 signals may be routed in the region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8-V power plane should cover the entire keep out region.


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#### 7.10.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 7-36 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DSP and DDR2 interfaces. Additional bulk bypass capacitance may be needed for other circuitry.

**Table 7-36. Bulk Bypass Capacitors**

| No. | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 1 | $DV_{DD18}$ Bulk Bypass Capacitor Count(1) | 3 | | Devices |
| 2 | $DV_{DD18}$ Bulk Bypass Total Capacitance | 30 | | µF |
| 3 | DDR#1 Bulk Bypass Capacitor Count(1) | 1 | | Devices |
| 4 | DDR#1 Bulk Bypass Total Capacitance(1) | 10 | | µF |
| 5 | DDR#2 Bulk Bypass Capacitor Count(2) | 1 | | Devices |
| 6 | DDR#2 Bulk Bypass Total Capacitance(1) (2) | 10 | | µF |

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass caps.
(2) Only used on 32-bit wide DDR2 memory systems

#### 7.10.2.7 High-Speed Bypass Capacitors

High-Speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass cap, DSP/DDR power, and DSP/DDR ground connections. Table 7-37 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

#### 7.10.2.8 Net Classes

Table 7-38 lists the clock net classes for the DDR2 interface. Table 7-39 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

**Table 7-37. High-Speed Bypass Capacitors**

| No. | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 1 | HS Bypass Capacitor Package Size(1) | | 0402 | 10 Mils |
| 2 | Distance from HS bypass capacitor to device being bypassed | | 250 | Mils |
| 3 | Number of connection vias for each HS bypass capacitor(2) | 2 | | Vias |
| 4 | Trace length from bypass capacitor contact to connection via | 1 | 30 | Mils |
| 5 | Number of connection vias for each DSP device power or ground balls | 1 | | Vias |
| 6 | Trace length from DSP device power ball to connection via | | 35 | Mils |
| 7 | Number of connection vias for each DDR2 device power or ground balls | 1 | | Vias |
| 8 | Trace length from DDR2 device power ball to connection via | | 35 | Mils |
| 9 | $DV_{DD18}$ HS Bypass Capacitor Count(3) | 20 | | Devices |
| 10 | $DV_{DD18}$ HS Bypass Capacitor Total Capacitance | 1.2 | | µF |
| 11 | DDR#1 HS Bypass Capacitor Count(3) | 8 | | Devices |
| 12 | DDR#1 HS Bypass Capacitor Total Capacitance | 0.4 | | µF |
| 13 | DDR#2 HS Bypass Capacitor Count(3) (4) | 8 | | Devices |
| 14 | DDR#2 HS Bypass Capacitor Total Capacitance(4) | 0.4 | | µF |

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) Only used on 32-bit wide DDR2 memory systems

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**Table 7-38. Clock Net Class Definitions**

| Clock Net Class | DSP Pin Names |
|---|---|
| CK | DDR_CLK/$\overline{\text{DDR_CLK}}$ |
| DQS0 | DDR_DQS0/$\overline{\text{DDR_DQS0}}$ |
| DQS1 | DDR_DQS1/$\overline{\text{DDR_DQS1}}$ |
| DQS2 (1) | DDR_DQS2/$\overline{\text{DDR_DQS2}}$ |
| DQS3 (1) | DDR_DQS3/$\overline{\text{DDR_DQS3}}$ |

(1) Only used on 32-bit wide DDR2 memory systems.

**Table 7-39. Signal Net Class Definitions**

| Clock Net Class | Associated Clock Net Class | DSP Pin Names |
|---|---|---|
| ADDR_CTRL | CK | DDR_BA[2:0], DDR_A[14:0], $\overline{\text{DDR_CS}}$, $\overline{\text{DDR_CAS}}$, $\overline{\text{DDR_RAS}}$, $\overline{\text{DDR_WE}}$, DDR_CKE |
| DQ0 | DQS0 | DDR_D[7:0], DDR_DQM0 |
| DQ1 | DQS1 | DDR_D[15:8], DDR_DQM1 |
| DQ2 (1) | DQS2 | DDR_D[23:16], DDR_DQM2 |
| DQ3 (1) | DQS3 | DDR_D[31:24], DDR_DQM3 |
| DQGATEL | CK, DQS0, DQS1 | DDR_DQGATE0, DDR_DQGATE1 |
| DQGATEH (1) | CK, DQS2, DQS3 | DDR_DQGATE2, DDR_DQGATE3 |

(1) Only used on 32-bit wide DDR2 memory systems.

### 7.10.2.9 DDR2 Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 7-40 shows the specifications for the series terminators.

**Table 7-40. DDR2 Signal Terminations**

| No. | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1 | CK Net Class (1) | 0 | | 10 | Ω |
| 2 | ADDR_CTRL Net Class (1) (2) (3) | 0 | 22 | Zo | Ω |
| 3 | Data Byte Net Classes (DQS0-DQS3, DQ0-DQ3) (1) (2) (3) (4) | 0 | 22 | Zo | Ω |
| 4 | DQGATE Net Classes (DQGATEL, DQGATEH) (1) (2) (3) | 0 | 10 | Zo | Ω |

(1) Only series termination is permitted, parallel or SST specifically disallowed.
(2) Terminator values larger than typical only recommended to address EMI issues.
(3) Termination value should be uniform across net class.
(4) When no termination is used on data lines (0 Ωs), the DDR2 devices must be programmed to operate in 60% strength mode.


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### 7.10.2.10 VREF Routing

VREF is used as a reference by the input buffers of the DDR2 memories as well as the DM6467T's. VREF is intended to be 1/2 the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 7-27. Other methods of creating VREF are not recommended. Figure 7-30 shows the layout guidelines for VREF.

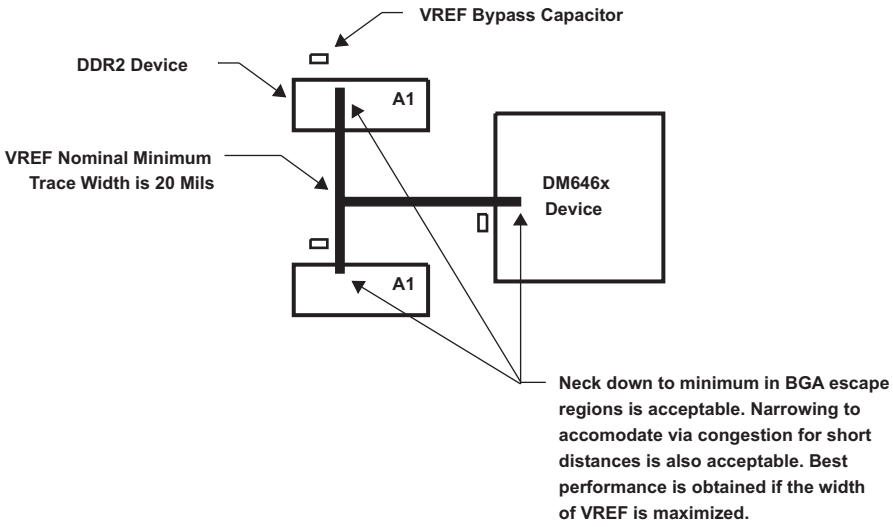


**Figure 7-30. VREF Routing and Topology**

### 7.10.2.11 DDR2 CK and ADDR_CTRL Routing

Figure 7-31 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

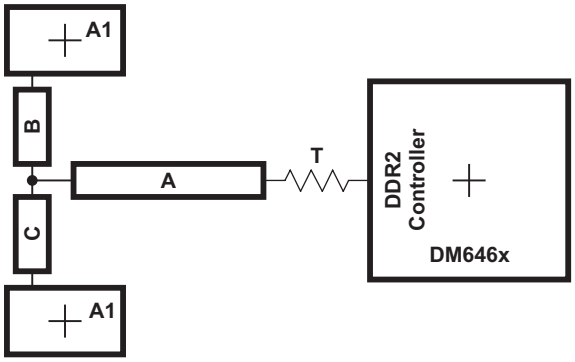


**Figure 7-31. CK and ADDR_CTRL Routing and Topology**

**Table 7-41. CK and ADDR_CTRL Routing Specification (1)**

| No | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1 | Center to center CK-$\overline{CK}$ spacing | | | 2w | |
| 2 | CK A to B/A to C Skew Length Mismatch(1) | | | 25 | Mils |
| 3 | CK B to C Skew Length Mismatch | | | 25 | Mils |
| 4 | Center to center CK to other DDR2 trace spacing(2) | 4w | | | |
| 5 | CK/ADDR_CTRL nominal trace length(3) | CACLM-50 | CACLM | CACLM+50 | Mils |
| 6 | ADDR_CTRL to CK Skew Length Mismatch | | | 100 | Mils |
| 7 | ADDR_CTRL to ADDR_CTRL Skew Length Mismatch | | | 100 | Mils |
| 8 | Center to center ADDR_CTRL to other DDR2 trace spacing(2) | 4w | | | |
| 9 | Center to center ADDR_CTRL to other ADDR_CTRL trace spacing(2) | 3w | | | |
| 10 | ADDR_CTRL A to B/A to C Skew Length Mismatch(1) | | | 100 | Mils |
| 11 | ADDR_CTRL B to C Skew Length Mismatch | | | 100 | Mils |

(1) Series terminator, if used, should be located closest to DSP.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

Figure 7-32 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

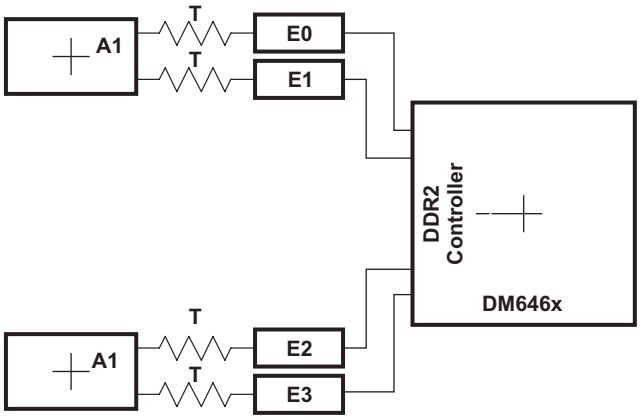


**Figure 7-32. DQS and DQ Routing and Toplogy**


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**Table 7-42. DQS and DQ Routing Specification (1)**

| No. | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1 | Center to center DQS-$\overline{DQS}$ spacing | | | 2w | |
| 2 | DQS E Skew Length Mismatch | | | 25 | Mils |
| 3 | Center to center DQS to other DDR2 trace spacing(2) | 4w | | | |
| 4 | DQS/DQ nominal trace length(1) (3) (4) (5) | DQLM-50 | DQLM | DQLM+50 | Mils |
| 5 | DQ to DQS Skew Length Mismatch(3) (4) (5) | | | 100 | Mils |
| 6 | DQ to DQ Skew Length Mismatch(3) (4) (5) | | | 100 | Mils |
| 7 | DQ to DQ/DQS via count mismatch(3) (4) (5) | | | 1 | Vias |
| 8 | Center to center DQ to other DDR2 trace spacing(2) (6) | 4w | | | |
| 9 | Center to center DQ to other DQ trace spacing(2) (7) (8) | 3w | | | |
| 10 | DQ/DQS E Skew Length Mismatch(3) (4) (5) | | | 100 | Mils |

(1) Series terminator, if used, should be located closest to DDR.
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) A 16 bit DDR memory system will have two sets of data net classes, one for data byte 0, and one for data byte 1, each with an associated DQS (2 DQS's).
(4) A 32 bit DDR memory system will have four sets of data net classes, one each for data bytes 0 through 3, and each associated with a DQS (4 DQS's).
(5) There is no need and it is not recommended to skew match across data bytes, ie from DQS0 and data byte 0 to DQS1 and data byte 1.
(6) DQ's from other DQS domains are considered *other DDR2 trace*.
(7) DQ's from other data bytes are considered *other DDR2 trace*.
(8) DQLM is the longest Manhattan distance of each of the DQS and DQ net classes.

Figure 7-33 shows the routing for the DQGATE net classes. Table 7-43 contains the routing specification.

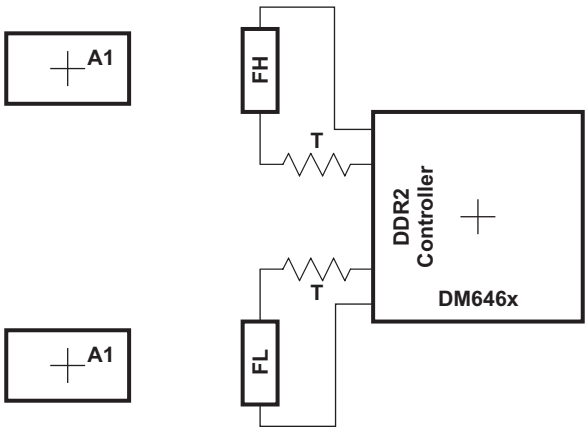


**Figure 7-33. DQGATE Routing**

**Table 7-43. DQGATE Routing Specification**

| No. | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1 | DQGATEL Length F(1) | | CKB0B1 | | |
| 2 | DQGATEH Length F(2) (3) | | CKB2B3 | | |
| 3 | Center to center DQGATE to any other trace spacing | 4w | | | |
| 4 | DQS/DQ nominal trace length | DQLM-50 | DQLM | DQLM+50 | Mils |
| 5 | DQGATEL Skew(4) | | | 100 | Mils |
| 6 | DQGATEH Skew(3) (5) | | | 100 | Mils |

(1) CKB0B1 is the sum of the length of the CK net plus the average length of the DQS0 and DQS1 nets.
(2) CKB2B3 is the sum of the length of the CK net plus the average length of the DQS2 and DQS3 nets.
(3) Only used in 32-bit wide DDR2 memory systems.
(4) Skew from CKB0B1
(5) Skew from CKB2B3


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## 7.11 Video Port Interface (VPIF)

The DM6467T Video Port Interface (VPIF) allows the capture and display of digital video streams. Features include:

- 150-MHz VPIF
- Up to 2 Video Capture Channels (Channel 0 and Channel 1)
  - Two 8-bit Standard-Definition (SD) Video with embedded timing codes (BT.656)
  - Single 16-bit High-Definition (HD) Video with embedded timing codes (BT.1120)
  - Single Raw Video (8-/10-/12-bit)
- Up to 2 Video Display Channels (Channel 2 and Channel 3)
  - Two 8-bit SD Video Display with embedded timing codes (BT.656)
  - Single 16-bit HD Video Display with embedded timing codes (BT.1120)

The VPIF capture channel input data format is selectable based on the settings of the specific Channel Control Register (Channels 0–3). The VPIF Raw Video data-bus width is selectable based on the settings of the Channel 0 Control Register. For more detailed information on these specific Channel Control Registers, see the *TMS320DM6467x DMSoC Video Port Interface (VPIF)* User's Guide (Literature Number SPRUER9).

### 7.11.1 VPIF Bus Master Memory Map

The VPIF peripheral includes a bus master interface that accesses the DM6467T system bus to transfer video-capture and video-display data. Table 7-44 shows the memory map for the VPIF master interface.

**Table 7-44. VPIF Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | VPIF MASTER INTERFACE |
|---|---|---|---|
| 0x0000 0000 | 0x7FFF FFFF | 2G | Reserved |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |

### 7.11.2 VPIF Clock Control (Capture and Display)

The source clocks for the VPIF data channels are selectable based on the settings of the VIDCLKCTL register (0x01C4 0038) (For the VIDCLKCTL register details, see Section 4.3.2.1, *Video Clock Control Register*). The VSCLKDIS register (0x01C4 006C) is used to disable the clock inputs when changing the clock source to ensure glitch-free operation. (For the VSCLKDIS register details, see Section 4.3.2.3, *Video and TSIF Clock Disable*).

For both the VPIF dual 8-bit or 16-bit video-capture modes, Channel 0 is always clocked by VP_CLKIN0 (see Figure 7-34).

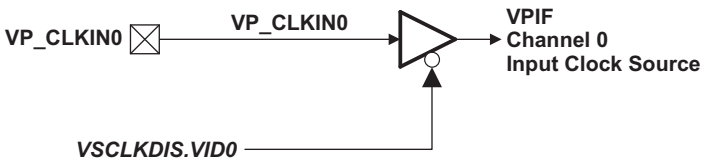



**Figure 7-34. VPIF Capture Channel 0 Source Clock**

Video-Capture Channel 1 is clocked by the VP_CLKIN1 signal, when the dual 8-bit capture mode is enabled. When the 16-bit capture mode or 8-/10-/12-bit raw-capture mode is used, VP_CLKIN0 ***must*** be selected as the clock source (VIDCLKCTL.VCH1CLK = 0) [see Figure 7-35].

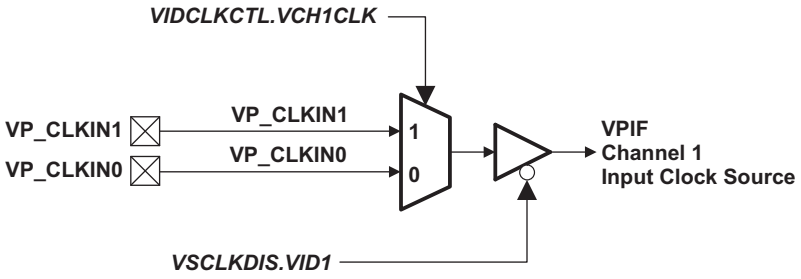
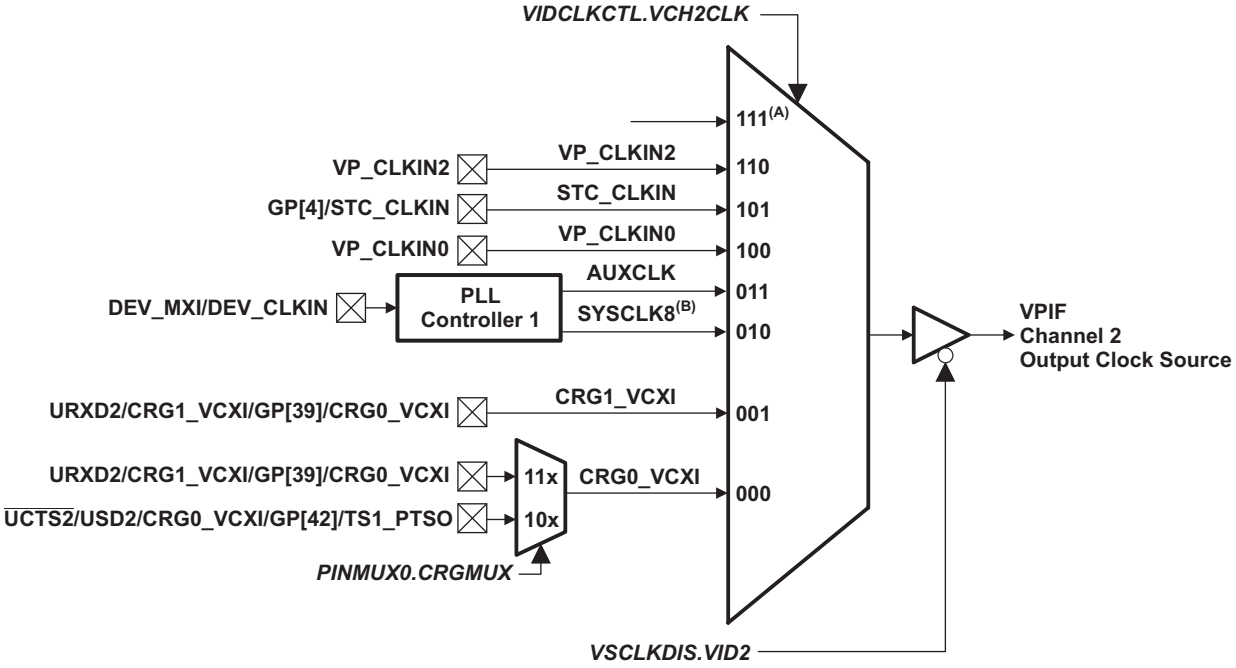



**Figure 7-35. VPIF Capture Channel 1 Source Clock Selection**

For both the dual 8-bit or 16-bit display modes, the VPIF Display Channel 2 outputs data synchronous to VP_CLKO2. The source clock for the VP_CLKO2 output is selectable from a number of external clock inputs or on-chip clock sources (see Figure 7-36).




(A) 111 = Reserved.
(B) For the -1G device, use an external clock source for the 54-/74.25-/108-/148.5-MHz VPIF clock.

**Figure 7-36. VPIF Display Channel 2 Source Clock Selection**

For the dual 8-bit display mode, the VPIF Display Channel 3 outputs data synchronous to VP_CLKO3. The source clock for the VP_CLKO3 output is selectable from a number of external clock inputs or on-chip clock sources (see Figure 7-37). When the 16-bit display mode for Channel 3 is selected, the clock source ***must*** match that of Channel 2 (VIDCLKCTL.VCH3CLK = VCH2CLK).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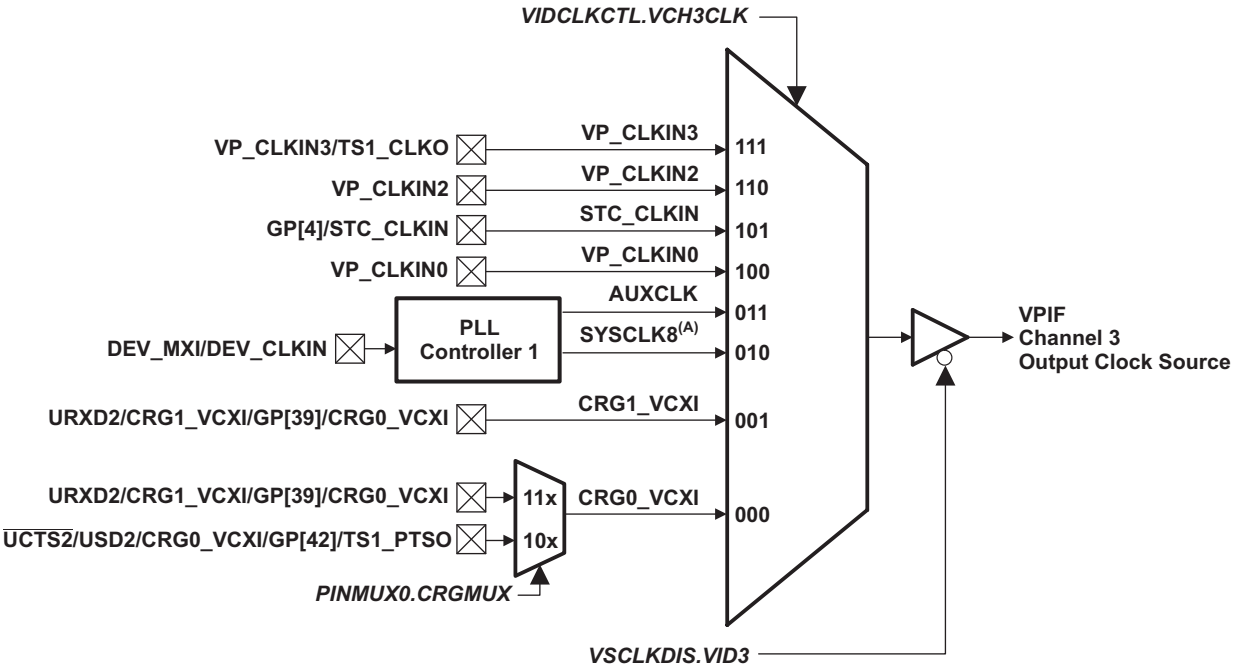


(A) For the -1G device, use an external clock source for the 54-/74.25-/108-/148.5-MHz VPIF clock.

**Figure 7-37. VPIF Display Channel 3 Source Clock Selection**

### 7.11.3 VPIF Register Descriptions

Table 7-45 shows the VPIF registers.

**Table 7-45. Video Port Interface (VPIF) Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 2000 | PID | Peripheral identification register |
| 0x01C1 2004 | CH0_CTRL | Channel 0 control register |
| 0x01C1 2008 | CH1_CTRL | Channel 1 control register |
| 0x01C1 200C | CH2_CTRL | Channel 2 control register |
| 0x01C1 2010 | CH3_CTRL | Channel 3 control register |
| 0x01C1 2014 - 0x01C1 201F | - | Reserved |
| 0x01C1 2020 | INTEN | Interrupt enable |
| 0x01C1 2024 | INTENSET | Interrupt enable set |
| 0x01C1 2028 | INTENCLR | Interrupt enable clear |
| 0x01C1 202C | INTSTAT | Interrupt status |
| 0x01C1 2030 | INTSTATCLR | Interrupt status clear |
| 0x01C1 2034 | EMU_CTRL | Emulation control |
| 0x01C1 2038 | DMA_SIZE | DMA size control |
| 0x01C1 203C - 0x01C1 203F | - | Reserved |
| **CAPTURE CHANNEL 0 REGISTERS** | | |
| 0x01C1 2040 | CH0_TY_STRTADR | Channel 0 Top Field luma buffer start address |
| 0x01C1 2044 | CH0_BY_STRTADR | Channel 0 Bottom Field luma buffer start address |
| 0x01C1 2048 | CH0_TC_STRTADR | Channel 0 Top Field chroma buffer start address |
| 0x01C1 204C | CH0_BC_STRTADR | Channel 0 Bottom Field chroma buffer start address |
| 0x01C1 2050 | CH0_THA_STRTADR | Channel 0 Top Field horizontal ancillary data buffer start address |
| 0x01C1 2054 | CH0_BHA_STRTADR | Channel 0 Bottom Field horizontal ancillary data buffer start address |
| 0x01C1 2058 | CH0_TVA_STRTADR | Channel 0 Top Field vertical ancillary data buffer start address |
| 0x01C1 205C | CH0_BVA_STRTADR | Channel 0 Bottom Field vertical ancillary data buffer start address |
| 0x01C1 2060 | CH0_SUBPIC_CFG | Channel 0 sub-picture configuration |
| 0x01C1 2064 | CH0_IMG_ADD_OFST | Channel 0 image data address offset |
| 0x01C1 2068 | CH0_HA_ADD_OFST | Channel 0 horizontal ancillary data address offset |
| 0x01C1 206C | CH0_HSIZE_CFG | Channel 0 horizontal data size configuration |
| 0x01C1 2070 | CH0_VSIZE_CFG0 | Channel 0 vertical data size configuration (0) |
| 0x01C1 2074 | CH0_VSIZE_CFG1 | Channel 0 vertical data size configuration (1) |
| 0x01C1 2078 | CH0_VSIZE_CFG2 | Channel 0 vertical data size configuration (2) |
| 0x01C1 207C | CH0_VSIZE | Channel 0 vertical image size |
| **CAPTURE CHANNEL 1 REGISTERS** | | |
| 0x01C1 2080 | CH1_TY_STRTADR | Channel 1 Top Field luma buffer start address |
| 0x01C1 2084 | CH1_BY_STRTADR | Channel 1 Bottom Field luma buffer start address |
| 0x01C1 2088 | CH1_TC_STRTADR | Channel 1 Top Field chroma buffer start address |
| 0x01C1 208C | CH1_BC_STRTADR | Channel 1 Bottom Field chroma buffer start address |
| 0x01C1 2090 | CH1_THA_STRTADR | Channel 1 Top Field horizontal ancillary data buffer start address |
| 0x01C1 2094 | CH1_BHA_STRTADR | Channel 1 Bottom Field horizontal ancillary data buffer start address |
| 0x01C1 2098 | CH1_TVA_STRTADR | Channel 1 Top Field vertical ancillary data buffer start address |
| 0x01C1 209C | CH1_BVA_STRTADR | Channel 1 Bottom Field vertical ancillary data buffer start address |
| 0x01C1 20A0 | CH1_SUBPIC_CFG | Channel 1 sub-picture configuration |
| 0x01C1 20A4 | CH1_IMG_ADD_OFST | Channel 1 image data address offset |
| 0x01C1 20A8 | CH1_HA_ADD_OFST | Channel 1 horizontal ancillary data address offset |
| 0x01C1 20AC | CH1_HSIZE_CFG | Channel 1 horizontal data size configuration |


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**Table 7-45. Video Port Interface (VPIF) Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 20B0 | CH1_VSIZE_CFG0 | Channel 1 vertical data size configuration (0) |
| 0x01C1 20B4 | CH1_VSIZE_CFG1 | Channel 1 vertical data size configuration (1) |
| 0x01C1 20B8 | CH1_VSIZE_CFG2 | Channel 1 vertical data size configuration (2) |
| 0x01C1 20BC | CH1_VSIZE | Channel 1 vertical image size |
| **DISPLAY CHANNEL 2 REGISTERS** | | |
| 0x01C1 20C0 | CH2_TY_STRTADR | Channel 2 Top Field luma buffer start address |
| 0x01C1 20C4 | CH2_BY_STRTADR | Channel 2 Bottom Field luma buffer start address |
| 0x01C1 20C8 | CH2_TC_STRTADR | Channel 2 Top Field chroma buffer start address |
| 0x01C1 20CC | CH2_BC_STRTADR | Channel 2 Bottom Field chroma buffer start address |
| 0x01C1 20D0 | CH2_THA_STRTADR | Channel 2 Top Field horizontal ancillary data buffer start address |
| 0x01C1 20D4 | CH2_BHA_STRTADR | Channel 2 Bottom Field horizontal ancillary data buffer start address |
| 0x01C1 20D8 | CH2_TVA_STRTADR | Channel 2 Top Field vertical ancillary data buffer start address |
| 0x01C1 20DC | CH2_BVA_STRTADR | Channel 2 Bottom Field vertical ancillary data buffer start address |
| 0x01C1 20E0 | CH2_SUBPIC_CFG | Channel 2 sub-picture configuration |
| 0x01C1 20E4 | CH2_IMG_ADD_OFST | Channel 2 image data address offset |
| 0x01C1 20E8 | CH2_HA_ADD_OFST | Channel 2 horizontal ancillary data address offset |
| 0x01C1 20EC | CH2_HSIZE_CFG | Channel 2 horizontal data size configuration |
| 0x01C1 20F0 | CH2_VSIZE_CFG0 | Channel 2 vertical data size configuration (0) |
| 0x01C1 20F4 | CH2_VSIZE_CFG1 | Channel 2 vertical data size configuration (1) |
| 0x01C1 20F8 | CH2_VSIZE_CFG2 | Channel 2 vertical data size configuration (2) |
| 0x01C1 20FC | CH2_VSIZE | Channel 2 vertical image size |
| 0x01C1 2100 | CH2_THA_STRTPOS | Channel 2 Top Field horizontal ancillary data insertion start position |
| 0x01C1 2104 | CH2_THA_SIZE | Channel 2 Top Field horizontal ancillary data size |
| 0x01C1 2108 | CH2_BHA_STRTPOS | Channel 2 Bottom Field horizontal ancillary data insertion start position |
| 0x01C1 210C | CH2_BHA_SIZE | Channel 2 Bottom Field horizontal ancillary data size |
| 0x01C1 2110 | CH2_TVA_STRTPOS | Channel 2 Top Field vertical ancillary data insertion start position |
| 0x01C1 2114 | CH2_TVA_SIZE | Channel 2 Top Field vertical ancillary data size |
| 0x01C1 2118 | CH2_BVA_STRTPOS | Channel 2 Bottom Field vertical ancillary data insertion start position |
| 0x01C1 211C | CH2_BVA_SIZE | Channel 2 Bottom Field vertical ancillary data size |
| 0x01C1 2120 - 0x01C1 213F | - | Reserved |
| **DISPLAY CHANNEL 3 REGISTERS** | | |
| 0x01C1 2140 | CH3_TY_STRTADR | Channel 3 Field 0 luma buffer start address |
| 0x01C1 2144 | CH3_BY_STRTADR | Channel 3 Field 1 luma buffer start address |
| 0x01C1 2148 | CH3_TC_STRTADR | Channel 3 Field 0 chroma buffer start address |
| 0x01C1 214C | CH3_BC_STRTADR | Channel 3 Field 1 chroma buffer start address |
| 0x01C1 2150 | CH3_THA_STRTADR | Channel 3 Field 0 horizontal ancillary data buffer start address |
| 0x01C1 2154 | CH3_BHA_STRTADR | Channel 3 Field 1 horizontal ancillary data buffer start address |
| 0x01C1 2158 | CH3_TVA_STRTADR | Channel 3 Field 0 vertical ancillary data buffer start address |
| 0x01C1 215C | CH3_BVA_STRTADR | Channel 3 Field 1 vertical ancillary data buffer start address |
| 0x01C1 2160 | CH3_SUBPIC_CFG | Channel 3 sub-picture configuration |
| 0x01C1 2164 | CH3_IMG_ADD_OFST | Channel 3 image data address offset |
| 0x01C1 2168 | CH3_HA_ADD_OFST | Channel 3 horizontal ancillary data address offset |
| 0x01C1 216C | CH3_HSIZE_CFG | Channel 3 horizontal data size configuration |
| 0x01C1 2170 | CH3_VSIZE_CFG0 | Channel 3 vertical data size configuration (0) |
| 0x01C1 2174 | CH3_VSIZE_CFG1 | Channel 3 vertical data size configuration (1) |
| 0x01C1 2178 | CH3_VSIZE_CFG2 | Channel 3 vertical data size configuration (2) |
| 0x01C1 217C | CH3_VSIZE | Channel 3 vertical image size |

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**Table 7-45. Video Port Interface (VPIF) Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 2180 | CH3_THA_STRTPOS | Channel 3 Top Field horizontal ancillary data insertion start position |
| 0x01C1 2184 | CH3_THA_SIZE | Channel 3 Top Field horizontal ancillary data size |
| 0x01C1 2188 | CH3_BHA_STRTPOS | Channel 3 Bottom Field horizontal ancillary data insertion start position |
| 0x01C1 218C | CH3_BHA_SIZE | Channel 3 Bottom Field horizontal ancillary data size |
| 0x01C1 2190 | CH3_TVA_STRTPOS | Channel 3 Top Field vertical ancillary data insertion start position |
| 0x01C1 2194 | CH3_TVA_SIZE | Channel 3 Top Field vertical ancillary data size |
| 0x01C1 2198 | CH3_BVA_STRTPOS | Channel 3 Bottom Field vertical ancillary data insertion start position |
| 0x01C1 219C | CH3_BVA_SIZE | Channel 3 Bottom Field vertical ancillary data size |
| 0x01C1 21A0 - 0x01C1 21FF | - | Reserved |


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### 7.11.4 VPIF Electrical Data/Timing

**Table 7-46. Timing Requirements for VPIF VP_CLKINx Inputs[1] (see Figure 7-38)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(VKI)}$ | Cycle time, VP_CLKIN0/1/2/3 | 6.6$\overline{6}$ | | ns |
| 2 | $t_{w(VKIH)}$ | Pulse duration, VP_CLKINx high | 0.4C | | ns |
| 3 | $t_{w(VKIL)}$ | Pulse duration, VP_CLKINx low | 0.4C | | ns |
| 4 | $t_{t(VKI)}$ | Transition time, VP_CLKINx | | 5 | ns |

(1) C = VP_CLKINx period in ns.

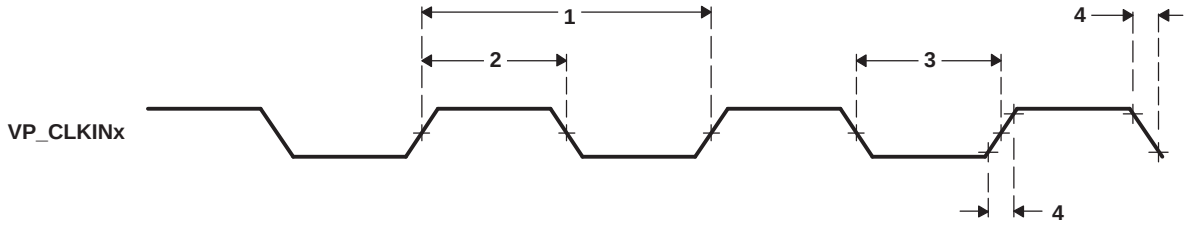


**Figure 7-38. Video Port Capture VP_CLKINx Timing**

**Table 7-47. Timing Requirements for VPIF Channels 0/1 Video Capture Data and Control Inputs (see Figure 7-39)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{su(VDINV-VKIH)}$ | Setup time, VP_DINx valid before VP_CLKIN0/1 high | 1.98 | | ns |
| 2 | $t_{h(VKIH-VDINV)}$ | Hold time, VP_DINx valid after VP_CLKIN0/1 high | 0 | | ns |

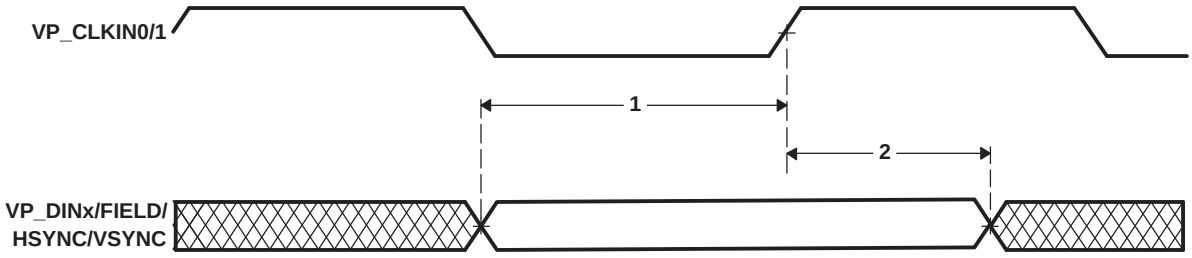


**Figure 7-39. VPIF Channels 0/1 Video Capture Data and Control Input Timing**

**Table 7-48. Switching Characteristics Over Recommended Operating Conditions for Video Data Shown With Respect to VP_CLKO2/3 (1) (see Figure 7-40)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(VKO)}$ | Cycle time, VP_CLKO2/3 | 6.6$\overline{6}$ | | ns |
| 2 | $t_{w(VKOH)}$ | Pulse duration, VP_CLKO2/3 high | 0.4C | | ns |
| 3 | $t_{w(VKOL)}$ | Pulse duration, VP_CLKO2/3 low | 0.4C | | ns |
| 4 | $t_{t(VKO)}$ | Transition time, VP_CLKO2/3 | | 5 | ns |
| 11 | $t_{d(VKOH-VPDOUTV)}$ | Delay time, VP_CLKO2/3 high to VP_DOUTx valid | | 5.15 | ns |
| 12 | $t_{d(VCLKOH-VPDOUTIV)}$ | Delay time, VP_CLKO2/3 high to VP_DOUTx invalid | 1.5 | | ns |

(1) C = VP_CLKO2/3 period in ns.

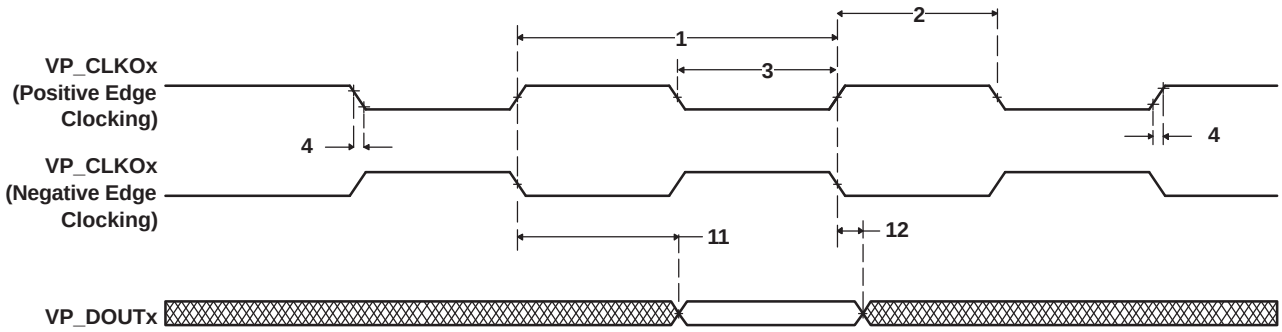


**Figure 7-40. VPIF Channels 2/3 Video Display Data Output Timing With Respect to VP_CLKO2/3**


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## 7.12 Transport Stream Interface (TSIF)

The DM6467T device includes two independent Transport Stream Interfaces (TSIF0 and TSIF1) with corresponding Clock Reference Generator (CRGEN) Modules for System Time-Clock Recovery. The TSIF peripheral supports the following features:

- 1-bit Serial and 8-bit Parallel independent receive and transmit interfaces with both synchronous and asynchronous modes. (**TSIF1 supports Serial mode *only***.)
- Stream input/output (I/O) speed rate configurable by the I/O clock speed
- ATS (absolute time stamp) detection, correction, and addition modes
- Automatically detects PAT and PMT *and* reflects assignment to the internal Packet Identification (PID) table (supported for partial Transfer Stream [TS] mode *only*; stream type and PID should be one-to-one mapping)
- PID filter with 7 PID filter tables and stream type assignments
- BYPASS mode implemented so that not only TS data, but any other data can be received or transmitted by the TSIF module
- Ring buffer control for both writes (8 channels) and reads (1 channel) to/from memory
- Supports “Specific Packet”, indicating boundary of plural program on TS
- Supports Full-TS in *only* one mode–Semi-Automatic-A mode, allowing communication to the C64x+ CPU.
- Supports Partial-TS in these modes–Semi-Automatic-B mode *and* Full-Automatic mode (provided stream type and PID are one-to-one mapping)

For more detailed information on the CRGEN peripheral, see the *TMS320DM646x DMSoC Clock Reference Generator* User's Guide (literature number SPRUEQ1).

### *7.12.1 TSIF Bus Master*

The TSIF peripherals each include a bus master interface that accesses the DM646x system bus to transfer stream receive and transmit data. Table 7-49 shows the memory map for the TSIF master interfaces.

**Table 7-49. TSIF0/1 Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | TSIF0/1 ACCESS |
|---|---|---|---|
| 0x0000 0000 | 0x0FFF FFFF | 256M | Reserved |
| 0x1000 0000 | 0x1000 FFFF | 64K | Reserved |
| 0x1001 0000 | 0x1001 3FFF | 16K | ARM RAM 0 (Data) |
| 0x1001 4000 | 0x1001 7FFF | 16K | ARM RAM 1 (Data) |
| 0x1001 8000 | 0x1001 FFFF | 32K | ARM ROM (Data) |
| 0x1002 0000 | 0x10FF FFFF | 16256K | Reserved |
| 0x1100 0000 | 0x41FF FFFF | 784M | |
| 0x4200 0000 | 0x43FF FFFF | 32M | EMIFA Data ($\overline{CS2}$) |
| 0x4400 0000 | 0x45FF FFFF | 32M | EMIFA Data ($\overline{CS3}$) |
| 0x4600 0000 | 0x47FF FFFF | 32M | EMIFA Data ($\overline{CS4}$) |
| 0x4800 0000 | 0x49FF FFFF | 32M | EMIFA Data ($\overline{CS5}$) |
| 0x4A00 0000 | 0x4BFF FFFF | 32M | Reserved |
| 0x4C00 0000 | 0x4FFF FFFF | 64M | VLYNQ (Remote Data) |
| 0x5000 0000 | 0x7FFF FFFF | 768M | Reserved |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |

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### 7.12.2 TSIF Clock Control

The source clocks for the TSIF counters and output channels are selectable based on the settings of the TSIFCTL register (0x01C4 0050). (For more detailed information on the TSIFCTL register, see Section 4.3.2.2, *TSIF Control*.) The VSCLKDIS register (0x01C4 006C) is used to disable the clock inputs when changing the clock source to ensure glitch-free operation. (For more detailed informaiton on the VSCLKDIS register, see Section 4.3.2.3, *Video and TSIF Clock Disable*.)

TSIF0 outputs data synchronous to TS0_CLKO. The source clock for the TS0_CLKO output is selectable from among a number of external clock inputs or on-chip clock sources (see Figure 7-41).

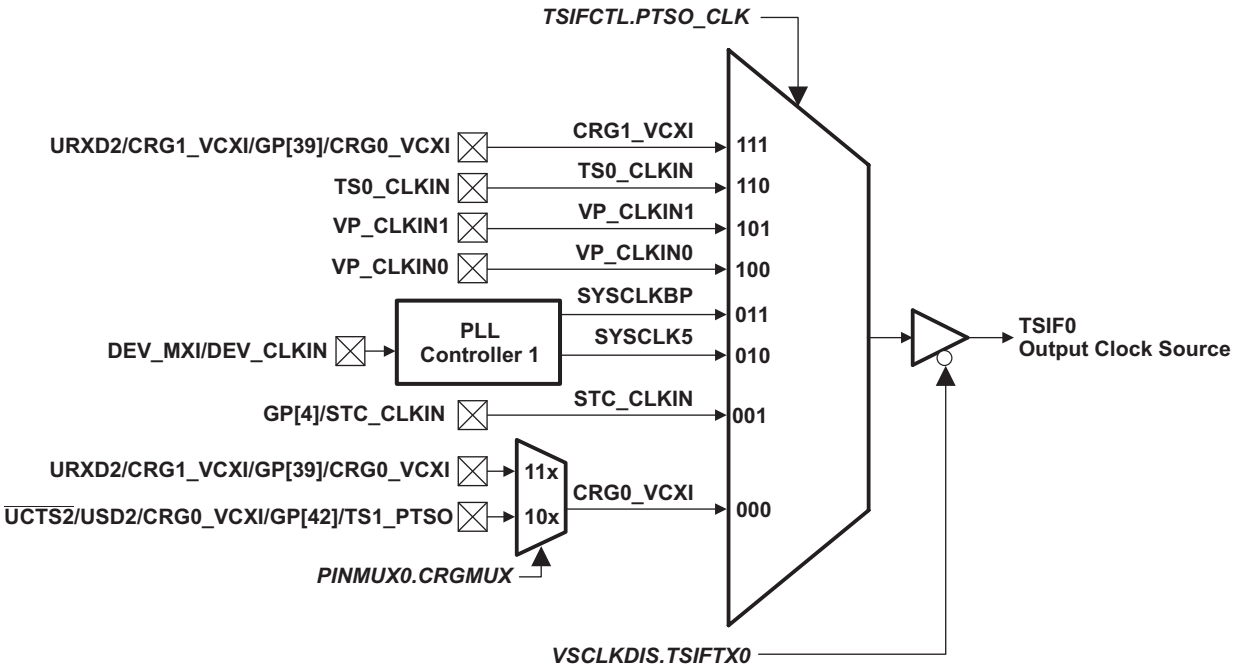


**Figure 7-41. TSIF0 Output Clock Source Selection**

The TSIF0 system time counter may be clocked from a number of external clock inputs or on-chip clock sources (see Figure 7-42).


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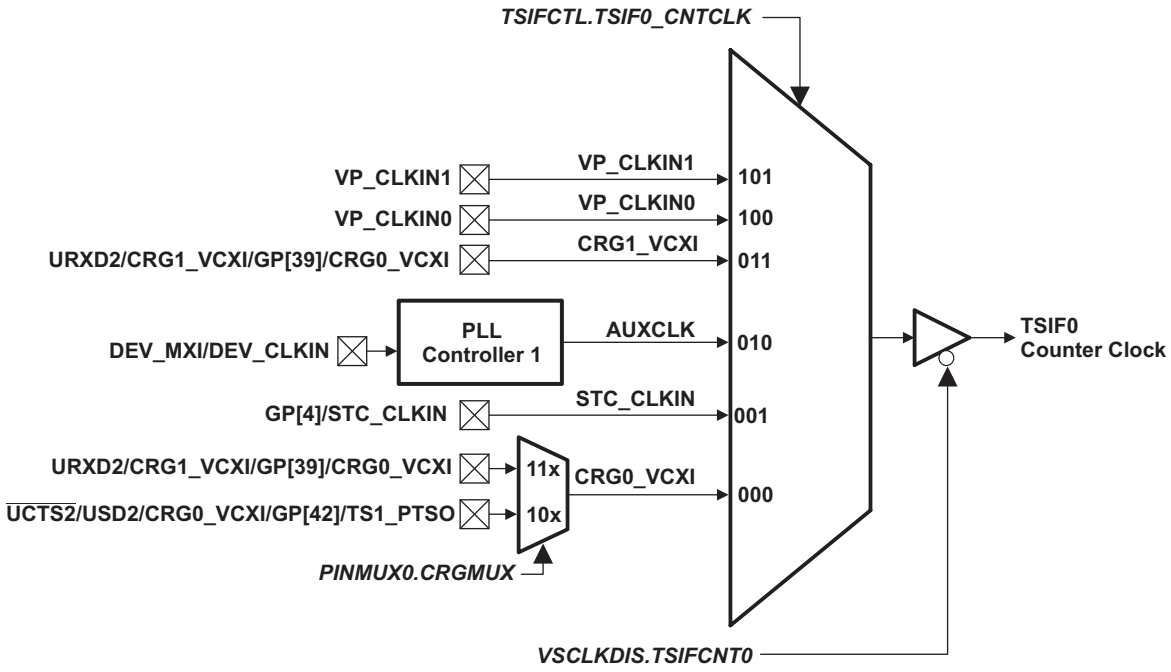
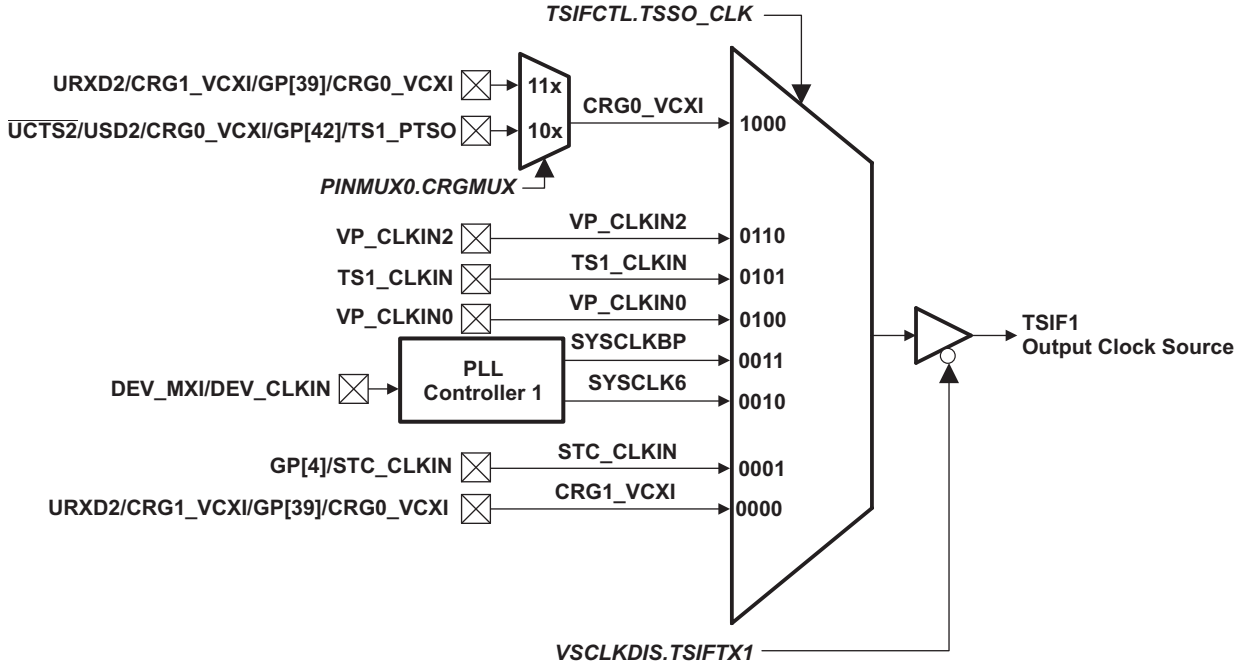



(A) 110, 111 = Reserved.

**Figure 7-42. TSIF0 Counter Clock Selection**

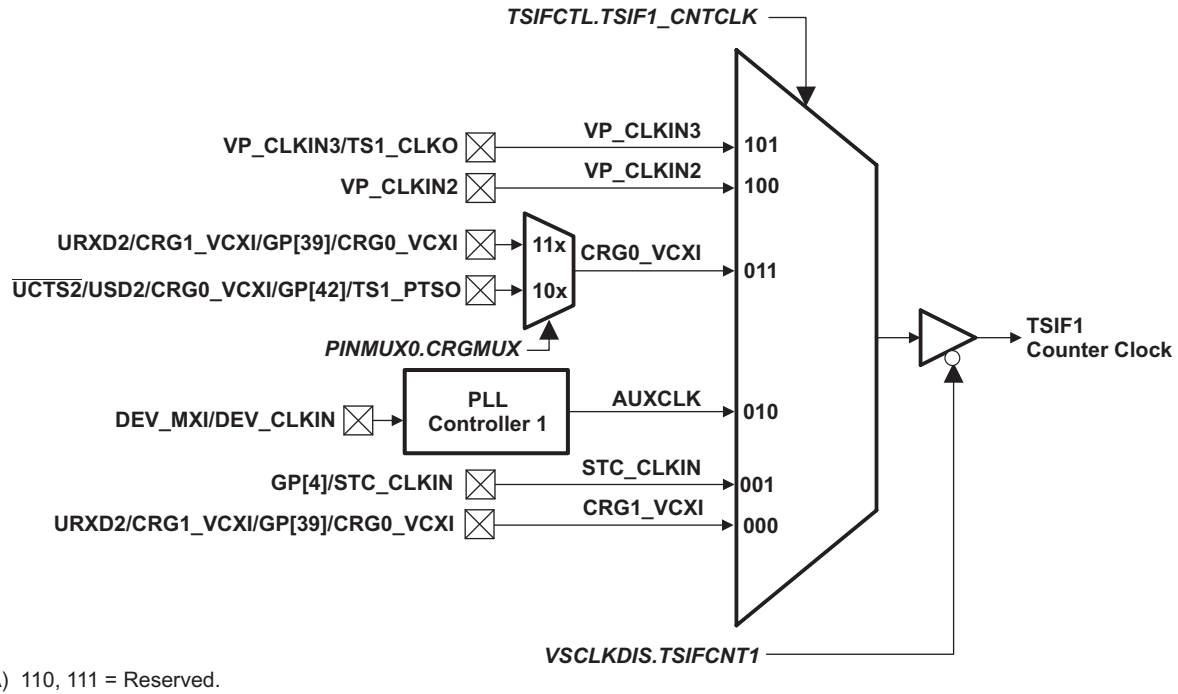
TSIF1 outputs data synchronous to TS1_CLKO. The source clock for the TS1_CLKO output is selectable from among a number of external clock inputs or on-chip clock sources (see Figure 7-43).




(A) 0111, 1001–1xx1 = Reserved.

**Figure 7-43. TSIF1 Output Clock Source Selection**

The TSIF1 system time counter may be clocked from a number of external clock inputs or on-chip clock sources (see Figure 7-44).




(A) 110, 111 = Reserved.

**Figure 7-44. TSIF1 Counter Clock Selection**

### 7.12.3 TSIF Peripheral Register Description(s)

The TSIF0 and TSIF1 registers are shown in Table 7-50 and Table 7-51, respectively.

**Table 7-50. TSIF0 Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 3000 | PID | TSIF0 peripheral identification (PID) register |
| 0x01C1 3004 | CTRL0 | Control register 0 register |
| 0x01C1 3008 | CTRL1 | Control register 1 register |
| 0x01C1 300C | INTEN | Interrupt enable register |
| 0x01C1 3010 | INTEN_SET | Interrupt enable set register |
| 0x01C1 3014 | INTEN_CLR | Interrupt enable clear register |
| 0x01C1 3018 | INTSTAT | Interrupt status register |
| 0x01C1 301C | INTSTAT_CLR | Interrupt status clear register |
| 0x01C1 3020 | EMU_CTRL | Emulation control register |
| 0x01C1 3024 | ASYNC_TX_WAIT | Asynchronous transmit wait time register |
| 0x01C1 3028 | PAT_SEN_CFG | Program association table (PAT) sense configuration register |
| 0x01C1 302C | PAT_STR_ADDR | PAT store address register |
| 0x01C1 3030 | PMT_SEN_CFG | Program map table (PMT) sense configuration register |
| 0x01C1 3034 | PMT_STR_ADDR | PMT store address register |
| 0x01C1 3038 | BSP_IN | Boundary sensing packet (BSP) in register |
| 0x01C1 303C | BSP_STORE_ADDR | BSP in store address register |
| 0x01C1 3040 | PCR_SENSE_CFG | Program clock reference (PCR) sense configuration register |
| 0x01C1 3044 | PID0_FILT_CFG | Packet Identifier (PID) 0 (PID0) filter configuration register |
| 0x01C1 3048 | PID1_FILT_CFG | PID1 filter configuration register |
| 0x01C1 304C | PID2_FILT_CFG | PID2 filter configuration register |
| 0x01C1 3050 | PID3_FILT_CFG | PID3 filter configuration register |
| 0x01C1 3054 | PID4_FILT_CFG | PID4 filter configuration register |


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**Table 7-50. TSIF0 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 3058 | PID5_FILT_CFG | PID5 filter configuration register |
| 0x01C1 305C | PID6_FILT_CFG | PID6 filter configuration register |
| 0x01C1 3060 | BYPASS_CFG | Bypass mode configuration register |
| 0x01C1 3064 | TX_ATS_INIT | Transmit Arrival Time Stamp (ATS) initialization register |
| 0x01C1 3068 | TX_ATS_MON | Transmit ATS monitor register |
| 0x01C1 306C | – | Reserved |
| 0x01C1 3070 | RX_PKT_STAT | Receive packet status register |
| 0x01C1 3074 - 0x01C1 307F | – | Reserved |
| 0x01C1 3080 | STC_INIT_CTRL | System Time Clock (STC) initialization control register |
| 0x01C1 3084 | STC_INIT_VAL | STC initialization value register |
| 0x01C1 3088 | STC_INT0 | STC interrupt entry 0 register |
| 0x01C1 308C | STC_INT1 | STC interrupt entry 1 register |
| 0x01C1 3090 | STC_INT2 | STC interrupt entry 2 register |
| 0x01C1 3094 | STC_INT3 | STC interrupt entry 3 register |
| 0x01C1 3098 | STC_INT4 | STC interrupt entry 4 register |
| 0x01C1 309C | STC_INT5 | STC interrupt entry 5 register |
| 0x01C1 30A0 | STC_INT6 | STC interrupt entry 6 register |
| 0x01C1 30A4 | STC_INT7 | STC interrupt entry 7 register |
| 0x01C1 30A8 - 0x01C1 30BF | – | Reserved |
| 0x01C1 30C0 | WRB_CTRL | Write ring buffer channel control register |
| 0x01C1 30C4 | WRB0_STRT_ADDR | Write ring buffer channel 0 start address register |
| 0x01C1 30C8 | WRB0_END_ADDR | Write ring buffer channel 0 end address register |
| 0x01C1 30CC | WRB0_RDPTR | Write ring buffer channel 0 read pointer register |
| 0x01C1 30D0 | WRB0_SUB | Write ring buffer channel 0 subtraction register |
| 0x01C1 30D4 | WRB0_WRPTR | Write ring buffer channel 0 write pointer register |
| 0x01C1 30D8 - 0x01C1 30DF | – | Reserved |
| 0x01C1 30E0 | WRB1_STRT_ADDR | Write ring buffer channel 1 start address register |
| 0x01C1 30E4 | WRB1_END_ADDR | Write ring buffer channel 1 end address register |
| 0x01C1 30E8 | WRB1_RDPTR | Write ring buffer channel 1 read pointer register |
| 0x01C1 30EC | WRB1_SUB | Write ring buffer channel 1 subtraction register |
| 0x01C1 30F0 | WRB1_WRPTR | Write ring buffer channel 1 write pointer register |
| 0x01C1 30F4 - 0x01C1 30FF | – | Reserved |
| 0x01C1 3100 | WRB2_STRT_ADDR | Write ring buffer channel 2 start address register |
| 0x01C1 3104 | WRB2_END_ADDR | Write ring buffer channel 2 end address register |
| 0x01C1 3108 | WRB2_RDPTR | Write ring buffer channel 2 read pointer register |
| 0x01C1 310C | WRB2_SUB | Write ring buffer channel 2 subtraction register |
| 0x01C1 3110 | WRB2_WRPTR | Write ring buffer channel 2 write pointer register |
| 0x01C1 3114 - 0x01C1 311F | – | Reserved |
| 0x01C1 3120 | WRB3_STRT_ADDR | Write ring buffer channel 3 start address register |
| 0x01C1 3124 | WRB3_END_ADDR | Write ring buffer channel 3 end address register |
| 0x01C1 3128 | WRB3_RDPTR | Write ring buffer channel 3 read pointer register |
| 0x01C1 312C | WRB3_SUB | Write ring buffer channel 3 subtraction register |
| 0x01C1 3130 | WRB3_WRPTR | Write ring buffer channel 3 write pointer register |
| 0x01C1 3134 - 0x01C1 313F | – | Reserved |
| 0x01C1 3140 | WRB4_STRT_ADDR | Write ring buffer channel 4 start address register |
| 0x01C1 3144 | WRB4_END_ADDR | Write ring buffer channel 4 end address register |
| 0x01C1 3148 | WRB4_RDPTR | Write ring buffer channel 4 read pointer register |

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**Table 7-50. TSIF0 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 314C | WRB4_SUB | Write ring buffer channel 4 subtraction register |
| 0x01C1 3150 | WRB4_WRPTR | Write ring buffer channel 4 write pointer register |
| 0x01C1 3154 - 0x01C1 315F | – | Reserved |
| 0x01C1 3160 | WRB5_STRT_ADDR | Write ring buffer channel 5 start address register |
| 0x01C1 3164 | WRB5_END_ADDR | Write ring buffer channel 5 end address register |
| 0x01C1 3168 | WRB5_RDPTR | Write ring buffer channel 5 read pointer register |
| 0x01C1 316C | WRB5_SUB | Write ring buffer channel 5 subtraction register |
| 0x01C1 3170 | WRB5_WRPTR | Write ring buffer channel 5 write pointer register |
| 0x01C1 3174 - 0x01C1 317F | – | Reserved |
| 0x01C1 3180 | WRB6_STRT_ADDR | Write ring buffer channel 6 start address register |
| 0x01C1 3184 | WRB6_END_ADDR | Write ring buffer channel 6 end address register |
| 0x01C1 3188 | WRB6_RDPTR | Write ring buffer channel 6 read pointer register |
| 0x01C1 318C | WRB6_SUB | Write ring buffer channel 6 subtraction register |
| 0x01C1 3190 | WRB6_WRPTR | Write ring buffer channel 6 write pointer register |
| 0x01C1 3194 - 0x01C1 319F | – | Reserved |
| 0x01C1 31A0 | WRB7_STRT_ADDR | Write ring buffer channel 7 start address register |
| 0x01C1 31A4 | WRB7_END_ADDR | Write ring buffer channel 7 end address register |
| 0x01C1 31A8 | WRB7_RDPTR | Write ring buffer channel 7 read pointer register |
| 0x01C1 31AC | WRB7_SUB | Write ring buffer channel 7 subtraction register |
| 0x01C1 31B0 | WRB7_WRPTR | Write ring buffer channel 7 write pointer register |
| 0x01C1 31B4 - 0x01C1 31BF | – | Reserved |
| 0x01C1 31C0 | RRB_CTRL | Read ring buffer channel control register |
| 0x01C1 31C4 | RRB_STRT_ADDR | Read ring buffer channel start address register |
| 0x01C1 31C8 | RRB_END_ADDR | Read ring buffer channel end address register |
| 0x01C1 31CC | RRB_WRPTR | Read ring buffer channel write pointer register |
| 0x01C1 31D0 | RRB_SUB | Read ring buffer channel subtraction register |
| 0x01C1 31D4 | RRB_RDPTR | Read ring buffer channel read pointer register |
| 0x01C1 31D8 | PKT_CNT | Packet counter value register |
| 0x01C1 31DC - 0x01C1 31FF | – | Reserved |

**Table 7-51. TSIF1 Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 3400 | PID | TSIF1 peripheral identification (PID) register |
| 0x01C1 3404 | CTRL0 | Control register 0 register |
| 0x01C1 3408 | CTRL1 | Control register 1 register |
| 0x01C1 340C | INTEN | Interrupt enable register |
| 0x01C1 3410 | INTEN_SET | Interrupt enable set register |
| 0x01C1 3414 | INTEN_CLR | Interrupt enable clear register |
| 0x01C1 3418 | INTSTAT | Interrupt status register |
| 0x01C1 341C | INTSTAT_CLR | Interrupt status clear register |
| 0x01C1 3420 | EMU_CTRL | Emulation control register |
| 0x01C1 3424 | ASYNC_TX_WAIT | Asynchronous transmit wait time register |
| 0x01C1 3428 | PAT_SEN_CFG | Program association table (PAT) sense configuration register |
| 0x01C1 342C | PAT_STR_ADDR | PAT store address register |
| 0x01C1 3430 | PMT_SEN_CFG | Program map table (PMT) sense configuration register |
| 0x01C1 3434 | PMT_STR_ADDR | PMT store address register |
| 0x01C1 3438 | BSP_IN | Boundary sensing packet (BSP) in register |


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**Table 7-51. TSIF1 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 343C | BSP_STORE_ADDR | BSP in store address register |
| 0x01C1 3440 | PCR_SENSE_CFG | Program clock reference (PCR) sense configuration register |
| 0x01C1 3444 | PID0_FILT_CFG | Packet Identifier (PID) 0 (PID0) filter configuration register |
| 0x01C1 3448 | PID1_FILT_CFG | PID1 filter configuration register |
| 0x01C1 344C | PID2_FILT_CFG | PID2 filter configuration register |
| 0x01C1 3450 | PID3_FILT_CFG | PID3 filter configuration register |
| 0x01C1 3454 | PID4_FILT_CFG | PID4 filter configuration register |
| 0x01C1 3458 | PID5_FILT_CFG | PID5 filter configuration register |
| 0x01C1 345C | PID6_FILT_CFG | PID6 filter configuration register |
| 0x01C1 3460 | BYPASS_CFG | Bypass mode configuration register |
| 0x01C1 3064 | TX_ATS_INIT | Transmit Arrival Time Stamp (ATS) initialization register |
| 0x01C1 3468 | TX_ATS_MON | Transmit ATS monitor register |
| 0x01C1 346C | – | Reserved |
| 0x01C1 3470 | RX_PKT_STAT | Receive packet status register |
| 0x01C1 3474 - 0x01C1 347F | – | Reserved |
| 0x01C1 3480 | STC_INIT_CTRL | System Time Clock (STC) initialization control register |
| 0x01C1 3484 | STC_INIT_VAL | STC initialization value register |
| 0x01C1 3488 | STC_INT0 | STC interrupt entry 0 register |
| 0x01C1 348C | STC_INT1 | STC interrupt entry 1 register |
| 0x01C1 3490 | STC_INT2 | STC interrupt entry 2 register |
| 0x01C1 3494 | STC_INT3 | STC interrupt entry 3 register |
| 0x01C1 3498 | STC_INT4 | STC interrupt entry 4 register |
| 0x01C1 349C | STC_INT5 | STC interrupt entry 5 register |
| 0x01C1 34A0 | STC_INT6 | STC interrupt entry 6 register |
| 0x01C1 34A4 | STC_INT7 | STC interrupt entry 7 register |
| 0x01C1 34A8 - 0x01C1 34BF | – | Reserved |
| 0x01C1 34C0 | WRB_CTRL | Write ring buffer channel control register |
| 0x01C1 34C4 | WRB0_STRT_ADDR | Write ring buffer channel 0 start address register |
| 0x01C1 34C8 | WRB0_END_ADDR | Write ring buffer channel 0 end address register |
| 0x01C1 34CC | WRB0_RDPTR | Write ring buffer channel 0 read pointer register |
| 0x01C1 34D0 | WRB0_SUB | Write ring buffer channel 0 subtraction register |
| 0x01C1 34D4 | WRB0_WRPTR | Write ring buffer channel 0 write pointer register |
| 0x01C1 34D8 - 0x01C1 34DF | – | Reserved |
| 0x01C1 34E0 | WRB1_STRT_ADDR | Write ring buffer channel 1 start address register |
| 0x01C1 34E4 | WRB1_END_ADDR | Write ring buffer channel 1 end address register |
| 0x01C1 34E8 | WRB1_RDPTR | Write ring buffer channel 1 read pointer register |
| 0x01C1 34EC | WRB1_SUB | Write ring buffer channel 1 subtraction register |
| 0x01C1 34F0 | WRB1_WRPTR | Write ring buffer channel 1 write pointer register |
| 0x01C1 34F4 - 0x01C1 34FF | – | Reserved |
| 0x01C1 3500 | WRB2_STRT_ADDR | Write ring buffer channel 2 start address register |
| 0x01C1 3504 | WRB2_END_ADDR | Write ring buffer channel 2 end address register |
| 0x01C1 3508 | WRB2_RDPTR | Write ring buffer channel 2 read pointer register |
| 0x01C1 350C | WRB2_SUB | Write ring buffer channel 2 subtraction register |
| 0x01C1 3510 | WRB2_WRPTR | Write ring buffer channel 2 write pointer register |
| 0x01C1 3514 - 0x01C1 351F | – | Reserved |
| 0x01C1 3520 | WRB3_STRT_ADDR | Write ring buffer channel 3 start address register |
| 0x01C1 3524 | WRB3_END_ADDR | Write ring buffer channel 3 end address register |

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**Table 7-51. TSIF1 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 3528 | WRB3_RDPTR | Write ring buffer channel 3 read pointer register |
| 0x01C1 352C | WRB3_SUB | Write ring buffer channel 3 subtraction register |
| 0x01C1 3530 | WRB3_WRPTR | Write ring buffer channel 3 write pointer register |
| 0x01C1 3534 - 0x01C1 353F | – | Reserved |
| 0x01C1 3540 | WRB4_STRT_ADDR | Write ring buffer channel 4 start address register |
| 0x01C1 3544 | WRB4_END_ADDR | Write ring buffer channel 4 end address register |
| 0x01C1 3548 | WRB4_RDPTR | Write ring buffer channel 4 read pointer register |
| 0x01C1 354C | WRB4_SUB | Write ring buffer channel 4 subtraction register |
| 0x01C1 3550 | WRB4_WRPTR | Write ring buffer channel 4 write pointer register |
| 0x01C1 3554 - 0x01C1 355F | – | Reserved |
| 0x01C1 3560 | WRB5_STRT_ADDR | Write ring buffer channel 5 start address register |
| 0x01C1 3564 | WRB5_END_ADDR | Write ring buffer channel 5 end address register |
| 0x01C1 3568 | WRB5_RDPTR | Write ring buffer channel 5 read pointer register |
| 0x01C1 356C | WRB5_SUB | Write ring buffer channel 5 subtraction register |
| 0x01C1 3570 | WRB5_WRPTR | Write ring buffer channel 5 write pointer register |
| 0x01C1 3574 - 0x01C1 357F | – | Reserved |
| 0x01C1 3580 | WRB6_STRT_ADDR | Write ring buffer channel 6 start address register |
| 0x01C1 3584 | WRB6_END_ADDR | Write ring buffer channel 6 end address register |
| 0x01C1 3588 | WRB6_RDPTR | Write ring buffer channel 6 read pointer register |
| 0x01C1 358C | WRB6_SUB | Write ring buffer channel 6 subtraction register |
| 0x01C1 3590 | WRB6_WRPTR | Write ring buffer channel 6 write pointer register |
| 0x01C1 3594 - 0x01C1 359F | – | Reserved |
| 0x01C1 35A0 | WRB7_STRT_ADDR | Write ring buffer channel 7 start address register |
| 0x01C1 35A4 | WRB7_END_ADDR | Write ring buffer channel 7 end address register |
| 0x01C1 35A8 | WRB7_RDPTR | Write ring buffer channel 7 read pointer register |
| 0x01C1 35AC | WRB7_SUB | Write ring buffer channel 7 subtraction register |
| 0x01C1 35B0 | WRB7_WRPTR | Write ring buffer channel 7 write pointer register |
| 0x01C1 35B4 - 0x01C1 35BF | – | Reserved |
| 0x01C1 35C0 | RRB_CTRL | Read ring buffer channel control register |
| 0x01C1 35C4 | RRB_STRT_ADDR | Read ring buffer channel start address register |
| 0x01C1 35C8 | RRB_END_ADDR | Read ring buffer channel end address register |
| 0x01C1 35CC | RRB_WRPTR | Read ring buffer channel write pointer register |
| 0x01C1 35D0 | RRB_SUB | Read ring buffer channel subtraction register |
| 0x01C1 35D4 | RRB_RDPTR | Read ring buffer channel read pointer register |
| 0x01C1 35D8 | PKT_CNT | Packet counter value register |
| 0x01C1 35DC - 0x01C1 35FF | – | Reserved |


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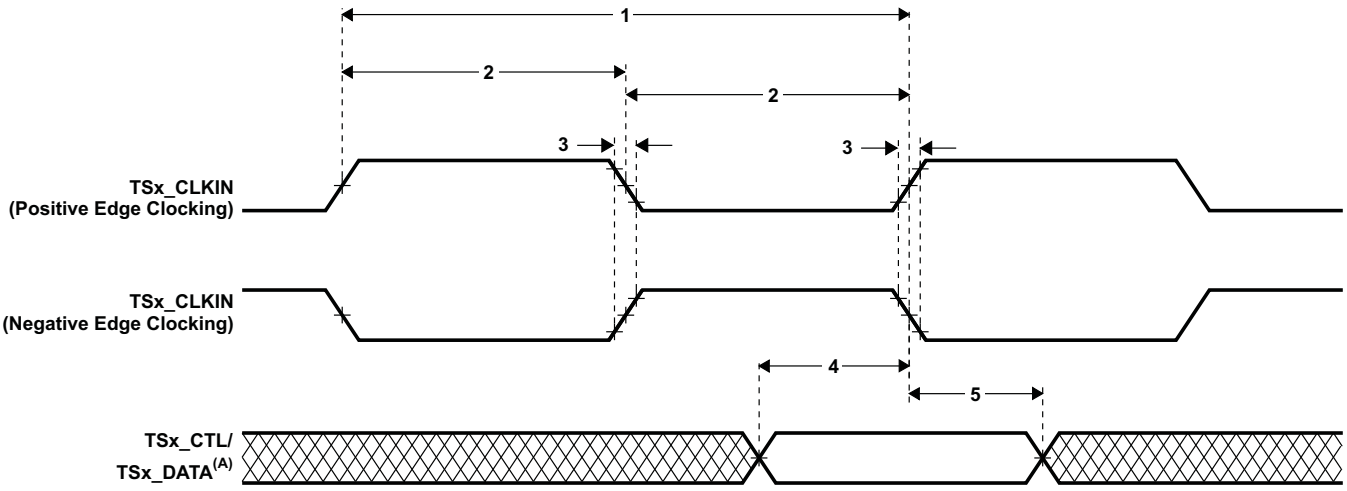
### 7.12.4 Transport Stream Interface (TSIF) Electrical Data/Timing

**Table 7-52. Timing Requirements for TSIF Input (see Figure 7-45)**

| NO. | | | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | SERIAL INPUT | | PARALLEL INPUT(1) | | |
| | | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(TSCLKIN)}$ | Cycle time, TSx_CLKIN | | 10 | | 16.7 | | ns |
| 2 | $t_{w(TSCLKIN)}$ | Pulse duration, TSx_CLKIN high/low(2) | | 0.4C | | 0.4C | | ns |
| 3 | $t_{t(TSCLKIN)}$ | Transition time, TSx_CLKIN | | | 3(3) | | 3(3) | ns |
| 4 | $t_{su(TSDATAIN-TSCLKINV)}$ | Setup time, TSx_CTL/TSx_DATA(4) input valid before TSx_CLKIN edge | All Others | 4 | | 4 | | ns |
| | | | TSx_WAIT IN | 13 | | 13 | | ns |
| 5 | $t_{h(TSCLKINV-TSDATAIN)}$ | Hold time, TSx_CTL/TSx_DATA(4) input valid after TSx_CLKIN edge | | 0 | | 0 | | ns |

(1) TSIF1 supports SERIAL INPUT mode *only*.
(2) C = TSx_CLKIN period (cycle time) in ns.
(3) For a 4-inch transmission line with 4-pF load capacitance at the device pin.
(4) TSx_CTL/TSx_DATA input includes: TS0_EN_WAITO, TS0_WAITIN, TS0_PSTIN, and TS0_DIN[7:0] for a parallel input. For a serial input, TSx_CTL/TSx_DATA input includes: TSx_EN_WAITO, TSx_WAITIN, TSx_PSTIN, and TS0_DIN7 or TS1_DIN.




A. TSx_CTL/TSx_DATA input includes: TS0_EN_WAITO, TS0_WAITIN, TS0_PSTIN, and TS0_DIN[7:0] for a parallel input. For a serial input, TSx_CTL/TSx_DATA input includes: TSx_EN_WAITO, TSx_WAITIN, TSx_PSTIN, and TS0_DIN7 or TS1_DIN.

**Figure 7-45. TSIF Input Timing**

**Table 7-53. Switching Characteristics Over Recommended Operating Conditions for TSIF Output (see Figure 7-46)**

| NO. | | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SERIAL OUTPUT | | PARALLEL OUTPUT(1) | | |
| | | | MIN | MAX | MIN | MAX | |
| 6 | $t_{c(TSCLKO)}$ | Cycle time, TSx_CLKO | 10 | | 16.7 | | ns |
| 7 | $t_{w(TSCLKO)}$ | Pulse duration, TSx_CLKO high/low(2) | 0.4C | | 0.4C | | ns |
| 8 | $t_{t(TSCLKO)}$ | Transition time, TSx_CLKO | | 3(3) | | 3(3) | ns |

(1) TSIF1 supports SERIAL OUTPUT mode *only*.
(2) C = TSx_CLKO period (cycle time) in ns.
(3) For a 4-inch transmission line with 4-pF load capacitance at the device pin.

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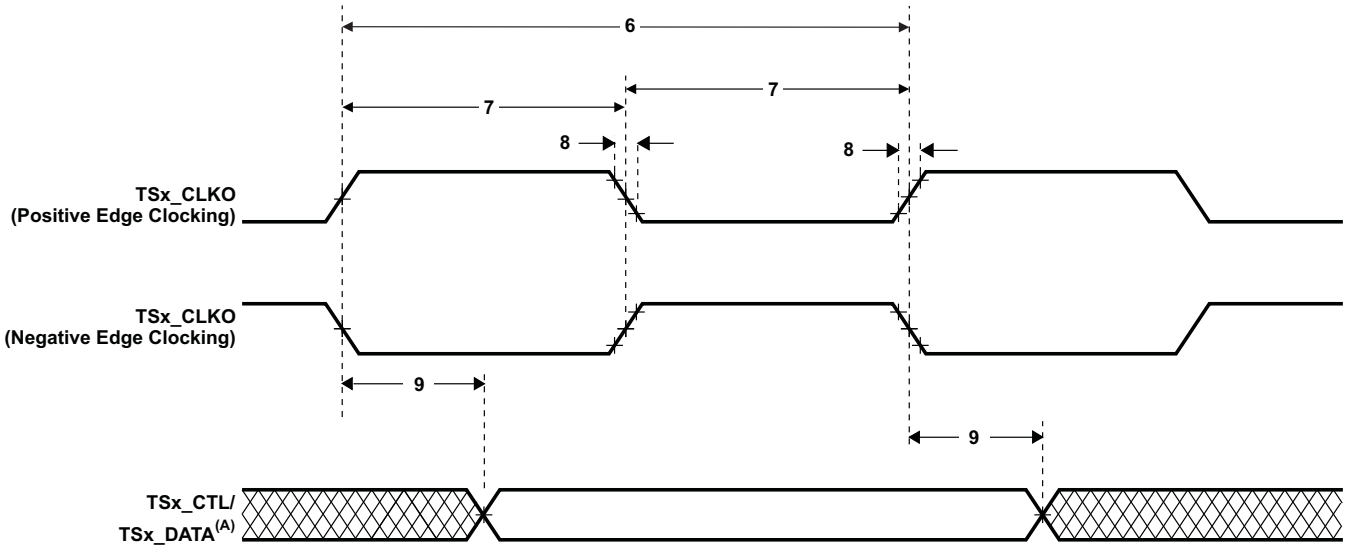
**Table 7-53. Switching Characteristics Over Recommended Operating Conditions for TSIF Output (see Figure 7-46) (continued)**

| NO. | | | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | SERIAL OUTPUT | | PARALLEL OUTPUT(1) | | |
| | | | | MIN | MAX | MIN | MAX | |
| 9 | $t_{d(TSCLKOV-TSDATAO)}$ | Delay time, TSx_CLKO edge to TSx_CTL/TSx_DATA(4) output valid | All Others | 1 | 7.5 | 1 | 7.5 | ns |
| | | | TS0_WAITO, TSx_EN_WAITO | 1 | 16.5 | 1 | 16.5 | ns |

(4) TSx_CTL/TSx_DATA output includes: TS0_ENAO, TS0_WAITO, TS0_PSTO, and TS0_DOUT[7:0] for a parallel output. For a serial output, TSx_CTL/TSx_DATA output includes: TSx_ENAO, TSx_EN_WAITO, TSx_PSTO, and TS0_DOUT7 or TS1_DOUT.




A. TSx_CTL/TSx_DATA output includes: TS0_ENAO, TS0_WAITO, TS0_PSTO, and TS0_DOUT[7:0] for a parallel output. For a serial output, TSx_CTL/TSx_DATA output includes: TSx_ENAO, TSx_EN_WAITO, TSx_PSTO, and TS0_DOUT7 or TS1_DOUT.

**Figure 7-46. TSIF Output Timing**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## 7.13 Clock Recovery Generator (CRGEN)

Each TSIF module has an associated CRGEN module which can adjust the local system time clock based upon the received Program Clock Reference (PCR) packets. CRGEN0 may *only* be used with TSIF 0 and CRGEN 1 may *only* be used with TSIF 1.

Each CRGEN module features:

- Automatic load of received PCR packet values from associated TSIF module
- Local System Time Clock (STC) counter
- PCR/STC difference generator (subtractor)
- Loop Filter (LPF)
- 1-bit sigma/delta modulator digital-to-analog converter (DAC) output for external VCXO control

### *7.13.1 CRGEN Peripheral Register Description(s)*

The CRGEN0 and CRGEN1 registers are shown in Table 7-54 and Table 7-55, respectively.

**Table 7-54. CRGEN0 Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C2 6000 | PID | CRGEN Peripheral Identification Register |
| 0x01C2 6004 | CONTROL | CRGEN control register |
| 0x01C2 6008 | STC_HI | System Time Clock (STC) current value (upper 17 bits) |
| 0x01C2 600C | STC_LO | STC current value (lower 16 bits plus extension) |
| 0x01C2 6010 | STC_VAL_HI | STC value (upper 17 bits) on TSIF0 PCR packet detection |
| 0x01C2 6014 | STC_VAL_LO | STC value (lower 16 bits plus extension) on TSIF0 PCR packet detection |
| 0x01C2 6018 | PCR_HI | Program Clock Reference (PCR) value (upper 17 bits) from TSIF0 Receive packet |
| 0x01C2 601C | PCR_LO | PCR value (lower 16 bits plus extension) from TSIF0 Receive packet |
| 0x01C2 6020 | PCR_PKT_STAT | PCR packet status |
| 0x01C2 6024 | LOOP_FILTER | Loop filter (LPF) interface |
| 0x01C2 6028 | STC_OFFSET_HI | Offset value of the STC counter for the higher (upper) 17 bits. This value is detected in the STC counter with the first PCR loading pulse signal. |
| 0x01C2 602C | STC_OFFSET_LO | Offset value of the STC counter for the lower 16 bits. The role of this register is same as the STC_LO register 0x01C2 600C. |
| 0x01C2 6030 - 0x01C2 603F | - | Reserved |
| 0x01C2 6040 | INTEN | Interrupt enable |
| 0x01C2 6044 | INTEN_SET | Interrupt enable set |
| 0x01C2 6048 | INTEN_CLR | Interrupt enable clear |
| 0x01C2 604C | INTSTAT | Interrupt status |
| 0x01C2 6050 | INTSTAT_CLR | Interrupt status clear |
| 0x01C2 6054 | EMU_CTRL | Emulation control |
| 0x01C2 6058 - 0x01C2 607F | - | Reserved |

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**Table 7-55. CRGEN1 Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C2 6400 | PID | CRGEN Peripheral Identification Register |
| 0x01C2 6404 | CONTROL | CRGEN control register |
| 0x01C2 6408 | STC_HI | System Time Clock (STC) current value (upper 17 bits) |
| 0x01C2 640C | STC_LO | STC current value (lower 16 bits plus extension) |
| 0x01C2 6410 | STC_VAL_HI | STC value (upper 17 bits) on TSIF1 PCR packet detection |
| 0x01C2 6414 | STC_VAL_LO | STC value (lower 16 bits plus extension) on TSIF1 PCR packet detection |
| 0x01C2 6418 | PCR_HI | Program Clock Reference (PCR) value (upper 17 bits) from TSIF1 Receive packet |
| 0x01C2 641C | PCR_LO | PCR value (lower 16 bits plus extension) from TSIF1 Receive packet |
| 0x01C2 6420 | PCR_PKT_STAT | PCR packet status |
| 0x01C2 6424 | LOOP_FILTER | Loop filter (LPF) interface |
| 0x01C2 6428 | STC_OFFSET_HI | Offset value of the STC counter for the higher 17 bits. This value is detected in the STC counter with the first PCR loading pulse signal. |
| 0x01C2 642C | STC_OFFSET_LO | Offset value of the STC counter for the lower 16 bits. The role of this register is same as the STC_LO register 0x01C2 640C. |
| 0x01C2 6430 - 0x01C2 643F | - | Reserved |
| 0x01C2 6440 | INTEN | Interrupt enable |
| 0x01C2 6444 | INTEN_SET | Interrupt enable set |
| 0x01C2 6448 | INTEN_CLR | Interrupt enable clear |
| 0x01C2 644C | INTSTAT | Interrupt status |
| 0x01C2 6450 | INTSTAT_CLR | Interrupt status clear |
| 0x01C2 6454 | EMU_CTRL | Emulation control |
| 0x01C2 6458 - 0x01C2 647F | - | Reserved |


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### 7.13.2 CRGEN Electrical Data/Timing

**Table 7-56. Timing Requirements for CRGx_VCXI Input (see Figure 7-47)**

| NO. | | | -1G | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| 1 | $t_{c(VCXI)}$ | Cycle time, CRGx_VCXI | 29.63 | 37.037 | 44.44 | ns |
| 2 | $t_{w(VCXIH)}$ | Pulse duration, CRGx_VCXI high | 0.4P | | | ns |
| 3 | $t_{w(VCXIL)}$ | Pulse duration, CRGx_VCXI low | 0.4P | | | ns |
| 4 | $t_{t(VCXI)}$ | Transition time, CRGx_VCXI | | | 5 | ns |

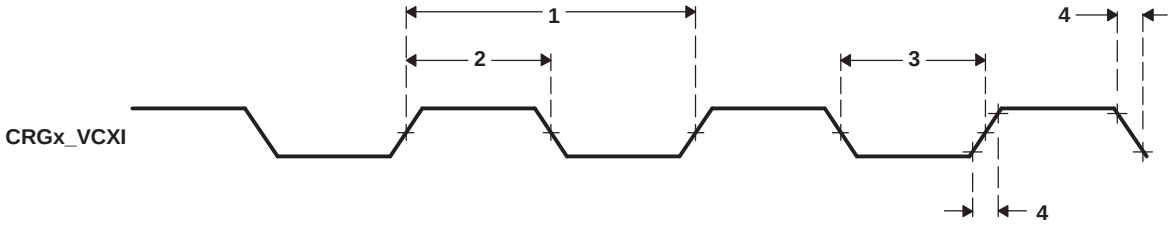


**Figure 7-47. CRGx_VCXI Input Timing**

**Table 7-57. Switching Characteristics Over Recommended Operating Conditions for CRGx_PO Output (see Figure 7-48)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(POH)}$ | Pulse duration, CRGx_PO high | 59.26 | | ns |
| 2 | $t_{w(POL)}$ | Pulse duration, CRGx_PO low | 59.26 | | ns |
| 3 | $t_{t(PO)}$ | Transition time, CRGx_PO | | 5 | ns |

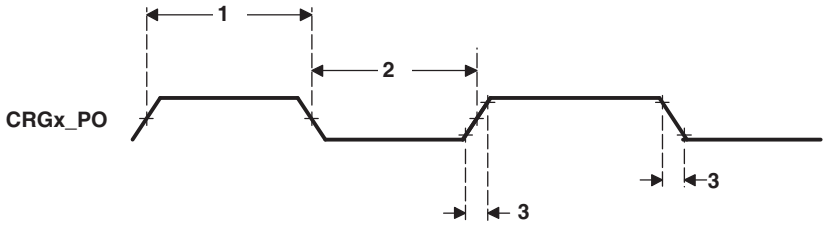


**Figure 7-48. CRGx_PO Output Timing**

## 7.14 Video Data Conversion Engine (VDCE)

The DM6467T Video Data Conversion Engine (VDCE) supports the following features:

- Resize function on horizontal (HRSZ) and vertical (VRSZ) with ratio defined by 256/N (N is a natural number that ranges from 256 to 2048) with 4 taps interpolation. Magnification ratio of horizontal resize and vertical resize can be configured separately (different value can be configured).
- Anti-alias filter (combination of two kinds of low-pass filter) with horizontal 7 taps, and vertical direction.
- Chrominance signal format conversion (CCV) on both directions, one is from 4:2:2 to 4:2:0 and one is from 4:2:0 to 4:2:2. This function also uses 4 taps interpolation. MPEG-1 specific format (half-pixel phased from even pixel position of luminance) is also supported.
- Edge padding for preparation of MC with unrestricted motion vector (required by MPEG-4, H.264, VC-1). All modes (progressive, interlace frame, and interlace field) are supported (macro-block level control that is required in H.264 is ***not*** currently supported).
- VC-1 range mapping in advanced profile (in case of displaying decoded reference image or trans-coding from VC-1 to any other format of video codec).
- 2-bit hardware menu overlay with 256 steps of blending for each color.

### *7.14.1 VDCE Bus Master*

The VDCE includes a bus master interface that accesses the DM646x system bus to transfer data. Table 7-58 shows the memory map for the VDCE interface.

**Table 7-58. VDCE Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | VDCE ACCESS |
|---|---|---|---|
| 0x0000 0000 | 0x0FFF FFFF | 256M | Reserved |
| 0x1000 0000 | 0x1000 FFFF | 64K | Reserved |
| 0x1001 0000 | 0x1001 3FFF | 16K | ARM RAM 0 (Data) |
| 0x1001 4000 | 0x1001 7FFF | 16K | ARM RAM 1 (Data) |
| 0x1001 8000 | 0x1001 FFFF | 32K | ARM ROM (Data) |
| 0x1002 0000 | 0x10FF FFFF | 16256K | Reserved |
| 0x1100 0000 | 0x41FF FFFF | 784M | |
| 0x4200 0000 | 0x43FF FFFF | 32M | EMIFA Data ($\overline{CS2}$) |
| 0x4400 0000 | 0x45FF FFFF | 32M | EMIFA Data ($\overline{CS3}$) |
| 0x4600 0000 | 0x47FF FFFF | 32M | EMIFA Data ($\overline{CS4}$) |
| 0x4800 0000 | 0x49FF FFFF | 32M | EMIFA Data ($\overline{CS5}$) |
| 0x4A00 0000 | 0x4BFF FFFF | 32M | Reserved |
| 0x4C00 0000 | 0x4FFF FFFF | 64M | VLYNQ (Remote Data) |
| 0x5000 0000 | 0x7FFF FFFF | 768M | Reserved |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |


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### 7.14.2 VDCE Register Description(s)

Table 7-59 shows the VDCE registers.

**Table 7-59. VDCE Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 2800 | PID | VDCE peripheral identification register |
| 0x01C1 2804 | CTRL | VDCE control register |
| 0x01C1 2808 | INTEN | Interrupt enable register |
| 0x01C1 280C | INTEN_SET | Interrupt enable set register |
| 0x01C1 2810 | INTEN_CLR | Interrupt enable clear register |
| 0x01C1 2814 | INTSTAT | Interrupt status register |
| 0x01C1 2818 | INTSTAT_CLR | Interrupt status clear register |
| 0x01C1 281C | EMU_CTRL | Emulation control register |
| 0x01C1 2820 | SRD_FRMT | Source/Result data store format register |
| 0x01C1 2824 | REQ_SIZE | Request unit size register |
| 0x01C1 2828 | PROC_SIZE | Processing unit size register |
| 0x01C1 282C - 0x01C1 283F | – | Reserved |
| 0x01C1 2840 | TY_SRCADDR | Luma top field source start address register |
| 0x01C1 2844 | TY_SRCSPSIZE | Luma top field source sub-picture size register |
| 0x01C1 2848 | TY_SRCOFFSET | Luma top field line source address offset size register |
| 0x01C1 284C | BY_SRCADDR | Luma bottom field source start address register |
| 0x01C1 2850 | BY_SRCSPSIZE | Luma bottom field source sub-picture size register |
| 0x01C1 2854 | BY_SRCOFFSET | Luma bottom field line source address offset size register |
| 0x01C1 2858 | TC_SRCADDR | Chroma top field source start address register |
| 0x01C1 285C | TC_SRCSPSIZE | Chroma top field source sub-picture size register |
| 0x01C1 2860 | TC_SRCOFFSET | Chroma top field line source address offset size register |
| 0x01C1 2864 | BC_SRCADDR | Chroma bottom field source start address register |
| 0x01C1 2868 | BC_SRCSPSIZE | Chroma bottom field source sub-picture size register |
| 0x01C1 286C | BC_SRCOFFSET | Chroma bottom field line source address offset size register |
| 0x01C1 2870 | TBMP_SRCADDR | Bitmap top field source start address register |
| 0x01C1 2874 | TBMP_SRCOFFSET | Bitmap top field line source address offset register |
| 0x01C1 2878 | BBMP_SRCADDR | Bitmap bottom field source start address register |
| 0x01C1 287C | BBMP_SRCOFFSET | Bitmap bottom field line source address offset register |
| 0x01C1 2880 | TY_RESADDR | Luma top field result start address register |
| 0x01C1 2884 | TY_RESSPSIZE | Luma top field result sub-picture size register |
| 0x01C1 2888 | TY_RESOFFSET | Luma top field line result address offset size register |
| 0x01C1 288C | BY_RESADDR | Luma bottom field result start address register |
| 0x01C1 2890 | BY_RESSPSIZE | Luma bottom field result sub-picture size register |
| 0x01C1 2894 | BY_RESOFFSET | Luma bottom field line result address offset size register |
| 0x01C1 2898 | TC_RESADDR | Chroma top field result start address register |
| 0x01C1 289C | TC_RESSPSIZE | Chroma top field result sub-picture size register |
| 0x01C1 28A0 | TC_RESOFFSET | Chroma top field result line address offset size register |
| 0x01C1 28A4 | BC_RESADDR | Chroma bottom field result start address register |
| 0x01C1 28A8 | BC_RESSPSIZE | Chroma bottom field result sub-picture size register |
| 0x01C1 28AC | BC_RESOFFSET | Chroma bottom field line result address offset size register |
| 0x01C1 28B0 - 0x01C1 28BF | – | Reserved |
| 0x01C1 28C0 | IMG_Y_SRCSTRTPOS | Luminance source image start position register |
| 0x01C1 28C4 | IMG_Y_SRCSIZE | Luminance source image size register |
| 0x01C1 28C8 | IMG_C_SRCSTRTPOS | Chrominance source image start position register |

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**Table 7-59. VDCE Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C1 28CC | IMG_C_SRCSIZE | Chrominance source image size register |
| 0x01C1 28D0 | IMG_BMP_SRCSTRTPOS | Bitmap source image start position register |
| 0x01C1 28D4 | IMG_BMP_SRCSIZE | Bitmap source image size register |
| 0x01C1 28D8 - 0x01C1 28DF | – | Reserved |
| 0x01C1 28E0 | IMG_Y_RESSTRTPOS | Luminance result image start position register |
| 0x01C1 28E4 | IMG_Y_RESSIZE | Luminance result image size register |
| 0x01C1 28E8 | IMG_C_RESSTRTPOS | Chrominance result image start position register |
| 0x01C1 28EC | IMG_C_RESSIZE | Chrominance result image size register |
| 0x01C1 28F0 | IMG_BMP_RESSTRTPOS | Bitmap result image start position (location) register |
| 0x01C1 28F4 - 0x01C1 28FF | – | Reserved |
| 0x01C1 2900 | RSZ_MODE | Resize mode definition register |
| 0x01C1 2904 | RSZ_HMAG | Horizontal resize magnification ratio control register |
| 0x01C1 2908 | RSZ_VMAG | Vertical resize magnification ratio control register |
| 0x01C1 290C | RSZ_HPHASE | Phase of initial pixel on horizontal resize register |
| 0x01C1 2910 | RSZ_VPHASE | Phase of initial pixel on vertical resize register |
| 0x01C1 2914 | RSZ_AFILTER | Horizontal anti-aliasing (flicker) filter control register |
| 0x01C1 2918 - 0x01C1 291F | – | Reserved |
| 0x01C1 2920 | CCV_MODE | Chrominance conversion mode control register |
| 0x01C1 2924 - 0x01C1 293F | – | Reserved |
| 0x01C1 2940 | BLD_LUT_00 | Look-up table for index 00 register |
| 0x01C1 2944 | BLD_LUT_01 | Look-up table for index 01 register |
| 0x01C1 2948 | BLD_LUT_02 | Look-up table for index 02 register |
| 0x01C1 294C | BLD_LUT_03 | Look-up table for index 03 register |
| 0x01C1 2950 - 0x01C1 295F | – | Reserved |
| 0x01C1 2960 | RGMP_CTRL | Ramp mapping control reigster |
| 0x01C1 2964 - 0x01C1 2983 | – | Reserved |
| 0x01C1 2984 | EPD_LUMA_WIDTH | Edge padding width for luminance register |
| 0x01C1 2988 | EPD_CHROMA_WIDTH | Edge padding width for chrominance register |
| 0x01C1 298C - 0x01C1 291F | – | Reserved |


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## 7.15 Peripheral Component Interconnect (PCI)

The DM6467T DMSoC supports connections to PCI-compliant devices via the integrated PCI master/slave bus interface. The PCI port interfaces to DSP internal resources via the data switched central resource. The data switched central resource is described in more detail in Section 5, *System Interconnect*.

For more detailed information on the PCI port peripheral module, see the *TMS320DM643x DMP Peripheral Component Interconnect (PCI)* User's Guide (literature number SPRU985).

### *7.15.1 PCI Device-Specific Information*

The PCI peripheral on the DM6467T DMSoC conforms to the *PCI Local Bus Specification Revision 2.3*. The PCI peripheral can act both as a PCI bus master and as a target. It supports PCI bus operation of speeds up to 66 MHz and uses a 32-bit data/address bus.

On the DM6467T device, the pins of the PCI peripheral are multiplexed with the pins of the EMIFA, GPIO, HPI, and ATA peripherals. For more detailed information on how to select PCI, see Section 4, Device Configurations.

The DM6467T device provides an initialization mechanism through which the default values for some of the PCI configuration registers can be read from an I2C EEPROM. Table 7-60 shows the registers which can be initialized through the PCI auto-initialization. The default value of these registers when PCI auto-initialization is **not** used. PCI auto-initialization is enabled by selecting PCI boot with auto-initialization. For information on how to select PCI boot with auto-initialization, see Section 4.4.1, Boot Modes. For more information on PCI auto-initialization, see the *TMS320DM646x DMSoC Peripheral Component Interconnect (PCI)* User's Guide (literature number SPRUER2) and the *Using the TMIS320DM646x Bootloader* Application Report (literature number SPRAAS0).

The PCI peripheral is a master peripheral within the DM6467T DMSoC.

**Table 7-60. Default Values for PCI Configuration Registers**

| REGISTER | DEFAULT VALUE (HEX) |
|---|---|
| **0x01C1 A000—Vendor ID/Device ID Register (PCIVENDEV)** | **B002 104Ch** |
| Device ID | B002h |
| Vendor ID | 104Ch |
| **0x01C1 A008—Class Code/Revision ID Register (PCICLREV)** | **1180 0001h** |
| Class Code | 80h |
| Revision ID | 01h |
| **0x01C1 A02C—System Vendor ID/Subsystem ID (PCISUBID)** | **0000 0000h** |
| Subsystem ID | 0000 |
| System Vendor ID | 0000 |
| **0x01C1 A03C—Max Latency/Min Grant/Interrupt Pin/Interrupt Line** | **0000 0100h** |
| Max Latency | 00 |
| Min Grant | 00 |
| Interrupt Pin | 01 |
| Interrupt Line | 00 |

The on-chip Bootloader supports a host boot which allows an external PCI device to load application code into the DMSoC's memory space.

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### 7.15.2 PCI External Master Memory Map

The PCI port includes a local DMA interface that allows external PCI master device intiated transfers to access the DM646x system bus. Table 7-61 shows the memory map for the PCI interface.

**Table 7-61. PCI DMA Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | PCI DMA ACCESS |
|---|---|---|---|
| 0x0000 0000 | 0x01BF FFFF | 28M | Reserved |
| 0x01C0 0000 | 0x0FFF FFFF | 228M | CFG Bus Peripherals |
| 0x1001 0000 | 0x1001 3FFF | 16K | ARM RAM 0 (Data) |
| 0x1001 4000 | 0x1001 7FFF | 16K | ARM RAM 1 (Data) |
| 0x1001 8000 | 0x1001 FFFF | 32K | ARM ROM (Data) |
| 0x1002 0000 | 0x10FF FFFF | 16256K | Reserved |
| 0x1100 0000 | 0x113F FFFF | 4M | |
| 0x1140 0000 | 0x114F FFFF | 1M | |
| 0x1150 0000 | 0x115F FFFF | 1M | |
| 0x1160 0000 | 0x116F FFFF | 1M | |
| 0x1170 0000 | 0x117F FFFF | 1M | |
| 0x1180 0000 | 0x1180 FFFF | 64K | |
| 0x1181 0000 | 0x1181 7FFF | 32K | |
| 0x1181 8000 | 0x1183 7FFF | 128K | C64x+ L2 RAM/Cache |
| 0x1183 8000 | 0x118F FFFF | 800K | Reserved |
| 0x1190 0000 | 0x11DF FFFF | 5M | |
| 0x11E0 0000 | 0x11E0 7FFF | 32K | C64x+ L1P RAM/Cache |
| 0x11E0 8000 | 0x11EF FFFF | 992K | Reserved |
| 0x11F0 0000 | 0x11F0 7FFF | 32K | C64x+ L1D RAM/Cache |
| 0x11F0 8000 | 0x11FF FFFF | 992K | Reserved |
| 0x1200 0000 | 0x4BFF FFFF | 928M | |
| 0x4C00 0000 | 0x4FFF FFFF | 64M | VLYNQ (Remote Data) |
| 0x5000 0000 | 0x7FFF FFFF | 768M | Reserved |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |


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### 7.15.3 PCI Peripheral Register Description(s)

**Table 7-62. PCI Back End Configuration Registers**

| DMSoC ACCESS HEX ADDRESS RANGE | ACRONYM | DMSoC ACCESS REGISTER NAME |
|---|---|---|
| 01C1 A000 - 01C1 A00F | - | Reserved |
| 01C1 A010 | PCISTATSET | PCI Status Set Register |
| 01C1 A014 | PCISTATCLR | PCI Status Clear Register |
| 01C1 A018 - 01C1 A01F | - | Reserved |
| 01C1 A020 | PCIHINTSET | PCI Host Interrupt Enable Set Register |
| 01C1 A024 | PCIHINTCLR | PCI Host Interrupt Enable Clear Register |
| 01C1 A028 - 01C1 A02F | - | Reserved |
| 01C1 A030 | PCIBINTSET | PCI Back End Application Interrupt Enable Set Register |
| 01C1 A034 | PCIBINTCLR | PCI Back End Application Interrupt Enable Clear Register |
| 01C1 A038 | - | Reserved |
| 01C1 A03C - 01C1 A0FF | - | Reserved |
| 01C1 A100 | PCIVENDEVMIR | PCI Vendor ID/Device ID Mirror Register |
| 01C1 A104 | PCICSRMIR | PCI Command/Status Mirror Register |
| 01C1 A108 | PCICLREVMIR | PCI Class Code/Revision ID Mirror Register |
| 01C1 A10C | PCICLINEMIR | PCI BIST/Header Type/Latency Timer/Cacheline Size Mirror Register |
| 01C1 A110 | PCIBAR0MSK | PCI Base Address Mask Register 0 |
| 01C1 A114 | PCIBAR1MSK | PCI Base Address Mask Register 1 |
| 01C1 A118 | PCIBAR2MSK | PCI Base Address Mask Register 2 |
| 01C1 A11C | PCIBAR3MSK | PCI Base Address Mask Register 3 |
| 01C1 A120 | PCIBAR4MSK | PCI Base Address Mask Register 4 |
| 01C1 A124 | PCIBAR5MSK | PCI Base Address Mask Register 5 |
| 01C1 A128 - 01C1 A12B | - | Reserved |
| 01C1 A12C | PCISUBIDMIR | PCI Subsystem Vendor ID/Subsystem ID Mirror Register |
| 01C1 A130 | - | Reserved |
| 01C1 A134 | PCICPBPTRMIR | PCI Capabilities Pointer Mirror Register |
| 01C1 A138 - 01C1 A13B | - | Reserved |
| 01C1 A13C | PCILGINTMIR | PCI Max Latency/Min Grant/Interrupt Pin/Interrupt Line Mirror Register |
| 01C1 A140 - 01C1 A17F | - | Reserved |
| 01C1 A180 | PCISLVCNTL | PCI Slave Control Register |
| 01C1 A184 - 01C1 A1BF | - | Reserved |
| 01C1 A1C0 | PCIBAR0TRL | PCI Slave Base Address 0 Translation Register |
| 01C1 A1C4 | PCIBAR1TRL | PCI Slave Base Address 1 Translation Register |
| 01C1 A1C8 | PCIBAR2TRL | PCI Slave Base Address 2 Translation Register |
| 01C1 A1CC | PCIBAR3TRL | PCI Slave Base Address 3 Translation Register |
| 01C1 A1D0 | PCIBAR4TRL | PCI Slave Base Address 4 Translation Register |
| 01C1 A1D4 | PCIBAR5TRL | PCI Slave Base Address 5 Translation Register |
| 01C1 A1D8 - 01C1 A1DF | - | Reserved |
| 01C1 A1E0 | PCIBAR0MIR | PCI Base Address Register 0 Mirror Register |
| 01C1 A1E4 | PCIBAR1MIR | PCI Base Address Register 1 Mirror Register |
| 01C1 A1E8 | PCIBAR2MIR | PCI Base Address Register 2 Mirror Register |
| 01C1 A1EC | PCIBAR3MIR | PCI Base Address Register 3 Mirror Register |
| 01C1 A1F0 | PCIBAR4MIR | PCI Base Address Register 4 Mirror Register |
| 01C1 A1F4 | PCIBAR5MIR | PCI Base Address Register 5 Mirror Register |
| 01C1 A1F8 - 01C1 A2FF | - | Reserved |
| 01C1 A300 | PCIMCFGDAT | PCI Master Configuration/IO Access Data Register |

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**Table 7-62. PCI Back End Configuration Registers (continued)**

| DMSoC ACCESS HEX ADDRESS RANGE | ACRONYM | DMSoC ACCESS REGISTER NAME |
|---|---|---|
| 01C1 A304 | PCIMCFGADR | PCI Master Configuration/IO Access Address Register |
| 01C1 A308 | PCIMCFGCMD | PCI Master Configuration/IO Access Command Register |
| 01C1 A30C - 01C1 A30F | - | Reserved |
| 01C1 A310 | PCIMSTCFG | PCI Master Configuration Register |

**Table 7-63. DMSoC-to-PCI Address Translation Registers**

| DMSoC ACCESS HEX ADDRESS RANGE | ACRONYM | DMSoC ACCESS REGISTER NAME |
|---|---|---|
| 01C1 A314 | PCIADDSUB0 | PCI Address Substitute 0 Register |
| 01C1 A318 | PCIADDSUB1 | PCI Address Substitute 1 Register |
| 01C1 A31C | PCIADDSUB2 | PCI Address Substitute 2 Register |
| 01C1 A320 | PCIADDSUB3 | PCI Address Substitute 3 Register |
| 01C1 A324 | PCIADDSUB4 | PCI Address Substitute 4 Register |
| 01C1 A328 | PCIADDSUB5 | PCI Address Substitute 5 Register |
| 01C1 A32C | PCIADDSUB6 | PCI Address Substitute 6 Register |
| 01C1 A330 | PCIADDSUB7 | PCI Address Substitute 7 Register |
| 01C1 A334 | PCIADDSUB8 | PCI Address Substitute 8 Register |
| 01C1 A338 | PCIADDSUB9 | PCI Address Substitute 9 Register |
| 01C1 A33C | PCIADDSUB10 | PCI Address Substitute 10 Register |
| 01C1 A340 | PCIADDSUB11 | PCI Address Substitute 11 Register |
| 01C1 A344 | PCIADDSUB12 | PCI Address Substitute 12 Register |
| 01C1 A348 | PCIADDSUB13 | PCI Address Substitute 13 Register |
| 01C1 A34C | PCIADDSUB14 | PCI Address Substitute 14 Register |
| 01C1 A350 | PCIADDSUB15 | PCI Address Substitute 15 Register |
| 01C1 A354 | PCIADDSUB16 | PCI Address Substitute 16 Register |
| 01C1 A358 | PCIADDSUB17 | PCI Address Substitute 17 Register |
| 01C1 A35C | PCIADDSUB18 | PCI Address Substitute 18 Register |
| 01C1 A360 | PCIADDSUB19 | PCI Address Substitute 19 Register |
| 01C1 A364 | PCIADDSUB20 | PCI Address Substitute 20 Register |
| 01C1 A368 | PCIADDSUB21 | PCI Address Substitute 21 Register |
| 01C1 A36C | PCIADDSUB22 | PCI Address Substitute 22 Register |
| 01C1 A370 | PCIADDSUB23 | PCI Address Substitute 23 Register |
| 01C1 A374 | PCIADDSUB24 | PCI Address Substitute 24 Register |
| 01C1 A378 | PCIADDSUB25 | PCI Address Substitute 25 Register |
| 01C1 A37C | PCIADDSUB26 | PCI Address Substitute 26 Register |
| 01C1 A380 | PCIADDSUB27 | PCI Address Substitute 27 Register |
| 01C1 A384 | PCIADDSUB28 | PCI Address Substitute 28 Register |
| 01C1 A388 | PCIADDSUB29 | PCI Address Substitute 29 Register |
| 01C1 A38C | PCIADDSUB30 | PCI Address Substitute 30 Register |
| 01C1 A390 | PCIADDSUB31 | PCI Address Substitute 31 Register |


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**Table 7-64. PCI Hook Configuration Registers**

| DMSoC ACCESS HEX ADDRESS RANGE | ACRONYM | DMSoC ACCESS REGISTER NAME |
|---|---|---|
| 01C1 A394 | PCIVENDEVPRG | PCI Vendor ID and Device ID Program Register |
| 01C1 A398 | – | Reserved |
| 01C1 A39C | PCICLREVPRG | PCI Class Code and Revision ID Program Register |
| 01C1 A3A0 | PCISUBIDPRG | PCI Subsystem Vendor ID and Subsystem ID Program Register |
| 01C1 A3A4 | PCIMAXLGPRG | PCI Max Latency and Min Grant Program Register |
| 01C1 A3A8 | – | Reserved |
| 01C1 A3AC | PCICFGDONE | PCI Configuration Done Register |
| 01C1 A3B0 - 01C1 A3FB | – | Reserved |
| 01C1 A3FC - 01C1 A3FF | – | Reserved |
| 01C1 A400 - 01C1 A7FF | – | Reserved |

**Table 7-65. PCI External Memory Space**

| DMSoC HEX ADDRESS RANGE | ACRONYM | DESCRIPTION |
|---|---|---|
| 3000 0000 - 307F FFFF | – | PCI Master Window 0 |
| 3080 0000 - 30FF FFFF | – | PCI Master Window 1 |
| 3100 0000 - 317F FFFF | – | PCI Master Window 2 |
| 3180 0000 - 31FF FFFF | – | PCI Master Window 3 |
| 3200 0000 - 327F FFFF | – | PCI Master Window 4 |
| 3280 0000 - 32FF FFFF | – | PCI Master Window 5 |
| 3300 0000 - 337F FFFF | – | PCI Master Window 6 |
| 3380 0000 - 33FF FFFF | – | PCI Master Window 7 |
| 3400 0000 - 347F FFFF | – | PCI Master Window 8 |
| 3480 0000 - 34FF FFFF | – | PCI Master Window 9 |
| 3500 0000 - 357F FFFF | – | PCI Master Window 10 |
| 3580 0000 - 35FF FFFF | – | PCI Master Window 11 |
| 3600 0000 - 367F FFFF | – | PCI Master Window 12 |
| 3680 0000 - 36FF FFFF | – | PCI Master Window 13 |
| 3700 0000 - 377F FFFF | – | PCI Master Window 14 |
| 3780 0000 - 37FF FFFF | – | PCI Master Window 15 |
| 3800 0000 - 387F FFFF | – | PCI Master Window 16 |
| 3880 0000 - 38FF FFFF | – | PCI Master Window 17 |
| 3900 0000 - 397F FFFF | – | PCI Master Window 18 |
| 3980 0000 - 39FF FFFF | – | PCI Master Window 19 |
| 3A00 0000 - 3A7F FFFF | – | PCI Master Window 20 |
| 3A80 0000 - 3AFF FFFF | – | PCI Master Window 21 |
| 3B00 0000 - 3B7F FFFF | – | PCI Master Window 22 |
| 3B80 0000 - 3BFF FFFF | – | PCI Master Window 23 |
| 3C00 0000 - 3C7F FFFF | – | PCI Master Window 24 |
| 3C80 0000 - 3CFF FFFF | – | PCI Master Window 25 |
| 3D00 0000 - 3D7F FFFF | – | PCI Master Window 26 |
| 3D80 0000 - 3DFF FFFF | – | PCI Master Window 27 |
| 3E00 0000 - 3E7F FFFF | – | PCI Master Window 28 |
| 3E80 0000 - 3EFF FFFF | – | PCI Master Window 29 |
| 3F00 0000 - 3F7F FFFF | – | PCI Master Window 30 |
| 3F80 0000 - 3FFF FFFF | – | PCI Master Window 31 |

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### 7.15.4 PCI Electrical Data/Timing

Texas Instruments (TI) has performed the simulation and system characterization to ensure that the PCI peripheral meets all AC timing specifications as required by the *PCI Local Bus Specification Revision 2.3*. Therefore, the AC timing specifications are **not** reproduced here. For more information on the AC timing specifications, see Section 4.2.3, *Timing Specification* (66-MHz timing) of the *PCI Local Bus Specification Revision 2.3*. **Note:** The DM6467T PCI peripheral **only** supports 3.3-V signaling and up to 66-MHz operation.


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## 7.16 Ethernet MAC (EMAC)

The Ethernet Media Access Controller (EMAC) module provides an efficient interface between the DM6467T and the networked community. The EMAC supports 10Base-T (10 Mbits/second [Mbps]), and 100BaseTX (100 Mbps), in either half- or full-duplex mode, and 1000BaseT (1000 Mbps) in full-duplex mode, with hardware flow control and quality-of-service (QOS) support.

The EMAC controls the flow of packet data from the DM6467T device to the PHY. The MDIO module controls the PHY configuration and status monitoring.

The EMAC module conforms to the IEEE 802.3-2002 standard, describing the “Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer” specifications. The IEEE 802.3 standard has also been adopted by ISO/IEC and re-designated as ISO/IEC 8802-3:2000(E).

Deviating from this standard, the EMAC module does not use the Transmit Coding Error signal MTXER. Instead of driving the error pin when an underflow condition occurs on a transmitted frame, the EMAC will intentionally generate an incorrect checksum by inverting the frame CRC, so that the transmitted frame will be detected as an error by the network. In addition, the EMAC I/Os operate at 3.3 V and are ***not*** compatible with 2.5-V I/O signaling. Therefore, only Ethernet PHYs with 3.3-V I/O interface should be used.

Both the EMAC and MDIO modules interface to the DM6467T device through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module. The EMAC control module contains the necessary components to allow the EMAC to make efficient use of device memory, plus it controls device interrupts. The EMAC control module incorporates 8K bytes of internal RAM to hold EMAC buffer descriptors.

For more detailed information on the EMAC, see the *TMS320DM646x DMSoC Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module* User's Guide (literature number SPRUEQ6).

### *7.16.1 EMAC Device-Specific Information*

The EMAC module on the DM6467T supports two interface modes: Media Independent Interface (MII) and Gigabit Media Independent Interface (GMII). The MII and GMII interface modes are defined in the IEEE 802.3-2002 standard.

The DM6467T EMAC uses the same pins for the MII and GMII modes of operation. Only one mode can be used at a time. The mode used is selected at device reset based on the GMIIEN bit in the MACCONTROL register. For more detailed information on the EMAC GMIIEN bit, see the *TMS320DM646x DMSoC Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module* User's Guide (literature number SPRUEQ6).

The MII and GMII modes-of-operation pins are as follows:

- MII: MTCLK, MRCLK, MTXD[3:0], MRXD[3:0], MTXEN, MRXDV, MRXER, MCOL, MCRS, MDCLK, and MDIO.
- GMII: RFTCLK, GMTCLK, MTCLK, MRCLK, MTXD[7:0], MRXD[7:0], MTXEN, MRXDV, MRXER, MCOL, MCRS, MDCLK, and MDIO.

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### 7.16.2 EMAC Bus Master Memory Map

The EMAC control module includes a multi-channel DMA engine which is used to transfer receive and transmit packets between the EMAC and DM6467T memory. Table 7-66 shows the memory map for the EMAC DMA.

**Table 7-66. EMAC DMA Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | EMAC DMA ACCESS |
|---|---|---|---|
| 0x0000 0000 | 0x3FFF FFFF | 1G | Reserved |
| 0x4000 0000 | 0x4BFF FFFF | 192M | Reserved |
| 0x4C00 0000 | 0x4FFF FFFF | 64M | VLYNQ (Remote Data) |
| 0x5000 0000 | 0x7FFF FFFF | 768M | Reserved |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |


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### 7.16.3 EMAC Peripheral Register Description(s)

**Table 7-67. Ethernet MAC (EMAC) Control Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C8 0000 | TXIDVER | Transmit identification and version register |
| 0x01C8 0004 | TXCONTROL | Transmit control register |
| 0x01C8 0008 | TXTEARDOWN | Transmit teardown register |
| 0x01C8 000C - 0x01C8 000F | – | Reserved |
| 0x01C8 0010 | RXIDVER | Receive identification and version register |
| 0x01C8 0014 | RXCONTROL | Receive control register |
| 0x01C8 0018 | RXTEARDOWN | Receive teardown register |
| 0x01C8 001C - 0x01C8 007F | – | Reserved |
| 0x01C8 0080 | TXINTSTATRAW | Transmit interrupt status (unmasked) register |
| 0x01C8 0084 | TXINTSTATMASKED | Transmit interrupt status (masked) register |
| 0x01C8 0088 | TXINTMASKSET | Transmit interrupt mask set register |
| 0x01C8 008C | TXINTMASKCLEAR | Transmit interrupt mask clear register |
| 0x01C8 0090 | MACINVECTOR | MAC input vector register |
| 0x01C8 0094 | MACEOIVECTOR | MAC end of interrupt vector register |
| 0x01C8 0098 - 0x01C8 009F | – | Reserved |
| 0x01C8 00A0 | RXINTSTATRAW | Receive interrupt status (unmasked) register |
| 0x01C8 00A4 | RXINTSTATMASKED | Receive interrupt status (masked) register |
| 0x01C8 00A8 | RXINTMASKSET | Receive interrupt mask set register |
| 0x01C8 00AC | RXINTMASKCLEAR | Receive interrupt mask clear register |
| 0x01C8 00B0 | MACINTSTATRAW | MAC interrupt status (unmasked) register |
| 0x01C8 00B4 | MACINTSTATMASKED | MAC interrupt status (masked) register |
| 0x01C8 00B8 | MACINTMASKSET | MAC interrupt mask set register |
| 0x01C8 00BC | MACINTMASKCLEAR | MAC interrupt mask clear register |
| 0x01C8 00C0 - 0x01C8 00FF | – | Reserved |
| 0x01C8 0100 | RXMBPENABLE | Receive multicast/broadcast/promiscuous channel enable register |
| 0x01C8 0104 | RXUNICASTSET | Receive unicast enable set register |
| 0x01C8 0108 | RXUNICASTCLEAR | Receive unicast clear register |
| 0x01C8 010C | RXMAXLEN | Receive maximum length register |
| 0x01C8 0110 | RXBUFFEROFFSET | Receive buffer offset register |
| 0x01C8 0114 | RXFILTERLOWTHRESH | Receive filter low priority frame threshold register |
| 0x01C8 0118 - 0x01C8 011F | – | Reserved |
| 0x01C8 0120 | RX0FLOWTHRESH | Receive channel 0 flow control threshold register |
| 0x01C8 0124 | RX1FLOWTHRESH | Receive channel 1 flow control threshold register |
| 0x01C8 0128 | RX2FLOWTHRESH | Receive channel 2 flow control threshold register |
| 0x01C8 012C | RX3FLOWTHRESH | Receive channel 3 flow control threshold register |
| 0x01C8 0130 | RX4FLOWTHRESH | Receive channel 4 flow control threshold register |
| 0x01C8 0134 | RX5FLOWTHRESH | Receive channel 5 flow control threshold register |
| 0x01C8 0138 | RX6FLOWTHRESH | Receive channel 6 flow control threshold register |
| 0x01C8 013C | RX7FLOWTHRESH | Receive channel 7 flow control threshold register |
| 0x01C8 0140 | RX0FREEBUFFER | Receive channel 0 free buffer count register |
| 0x01C8 0144 | RX1FREEBUFFER | Receive channel 1 free buffer count register |
| 0x01C8 0148 | RX2FREEBUFFER | Receive channel 2 free buffer count register |
| 0x01C8 014C | RX3FREEBUFFER | Receive channel 3 free buffer count register |
| 0x01C8 0150 | RX4FREEBUFFER | Receive channel 4 free buffer count register |
| 0x01C8 0154 | RX5FREEBUFFER | Receive channel 5 free buffer count register |

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**Table 7-67. Ethernet MAC (EMAC) Control Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C8 0158 | RX6FREEBUFFER | Receive channel 6 free buffer count register |
| 0x01C8 015C | RX7FREEBUFFER | Receive channel 7 free buffer count register |
| 0x01C8 0160 | MACCONTROL | MAC control register |
| 0x01C8 0164 | MACSTATUS | MAC status register |
| 0x01C8 0168 | EMCONTROL | Emulation control register |
| 0x01C8 016C | FIFOCONTROL | FIFO control register (transmit and receive) |
| 0x01C8 0170 | MACCONFIG | MAC configuration register |
| 0x01C8 0174 | SOFTRESET | Soft reset register |
| 0x01C8 0178 - 0x01C8 01CF | – | Reserved |
| 0x01C8 01D0 | MACSRCADDRLO | MAC source address low bytes register (lower 16-bits) |
| 0x01C8 01D4 | MACSRCADDRHI | MAC source address high bytes register (upper 32-bits) |
| 0x01C8 01D8 | MACHASH1 | MAC hash address register 1 |
| 0x01C8 01DC | MACHASH2 | MAC hash address register 2 |
| 0x01C8 01E0 | BOFFTEST | Back off test register |
| 0x01C8 01E4 | TPACETEST | Transmit pacing algorithm test register |
| 0x01C8 01E8 | RXPAUSE | Receive pause timer register |
| 0x01C8 01EC | TXPAUSE | Transmit pause timer register |
| 0x01C8 01F0 - 0x01C8 01FF | – | Reserved |
| 0x01C8 0200 - 0x01C8 02FF | (see Table 7-68) | EMAC statistics registers |
| 0x01C8 0300 - 0x01C8 04FF | – | Reserved |
| 0x01C8 0500 | MACADDRLO | MAC address low bytes register (used in receive address matching) |
| 0x01C8 0504 | MACADDRHI | MAC address high bytes register (used in receive address matching) |
| 0x01C8 0508 | MACINDEX | MAC index register |
| 0x01C8 050C - 0x01C8 05FF | – | Reserved |
| 0x01C8 0600 | TX0HDP | Transmit channel 0 DMA head descriptor pointer register |
| 0x01C8 0604 | TX1HDP | Transmit channel 1 DMA head descriptor pointer register |
| 0x01C8 0608 | TX2HDP | Transmit channel 2 DMA head descriptor pointer register |
| 0x01C8 060C | TX3HDP | Transmit channel 3 DMA head descriptor pointer register |
| 0x01C8 0610 | TX4HDP | Transmit channel 4 DMA head descriptor pointer register |
| 0x01C8 0614 | TX5HDP | Transmit channel 5 DMA head descriptor pointer register |
| 0x01C8 0618 | TX6HDP | Transmit channel 6 DMA head descriptor pointer register |
| 0x01C8 061C | TX7HDP | Transmit channel 7 DMA head descriptor pointer register |
| 0x01C8 0620 | RX0HDP | Receive channel 0 DMA head descriptor pointer register |
| 0x01C8 0624 | RX1HDP | Receive channel 1 DMA head descriptor pointer register |
| 0x01C8 0628 | RX2HDP | Receive channel 2 DMA head descriptor pointer register |
| 0x01C8 062C | RX3HDP | Receive channel 3 DMA head descriptor pointer register |
| 0x01C8 0630 | RX4HDP | Receive channel 4 DMA head descriptor pointer register |
| 0x01C8 0634 | RX5HDP | Receive channel 5 DMA head descriptor pointer register |
| 0x01C8 0638 | RX6HDP | Receive channel 6 DMA head descriptor pointer register |
| 0x01C8 063C | RX7HDP | Receive channel 7 DMA head descriptor pointer register |
| 0x01C8 0640 | TX0CP | Transmit channel 0 completion pointer (interrupt acknowledge) register |
| 0x01C8 0644 | TX1CP | Transmit channel 1 completion pointer (interrupt acknowledge) register |
| 0x01C8 0648 | TX2CP | Transmit channel 2 completion pointer (interrupt acknowledge) register |
| 0x01C8 064C | TX3CP | Transmit channel 3 completion pointer (interrupt acknowledge) register |


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**Table 7-67. Ethernet MAC (EMAC) Control Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C8 0650 | TX4CP | Transmit channel 4 completion pointer (interrupt acknowledge) register |
| 0x01C8 0654 | TX5CP | Transmit channel 5 completion pointer (interrupt acknowledge) register |
| 0x01C8 0658 | TX6CP | Transmit channel 6 completion pointer (interrupt acknowledge) register |
| 0x01C8 065C | TX7CP | Transmit channel 7 completion pointer (interrupt acknowledge) register |
| 0x01C8 0660 | RX0CP | Receive channel 0 completion pointer (interrupt acknowledge) register |
| 0x01C8 0664 | RX1CP | Receive channel 1 completion pointer (interrupt acknowledge) register |
| 0x01C8 0668 | RX2CP | Receive channel 2 completion pointer (interrupt acknowledge) register |
| 0x01C8 066C | RX3CP | Receive channel 3 completion pointer (interrupt acknowledge) register |
| 0x01C8 0670 | RX4CP | Receive channel 4 completion pointer (interrupt acknowledge) register |
| 0x01C8 0674 | RX5CP | Receive channel 5 completion pointer (interrupt acknowledge) register |
| 0x01C8 0678 | RX6CP | Receive channel 6 completion pointer (interrupt acknowledge) register |
| 0x01C8 067C | RX7CP | Receive channel 7 completion pointer (interrupt acknowledge) register |
| 0x01C8 0680 - 0x01C8 07FF | – | Reserved |

**Table 7-68. EMAC Statistics Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C8 0200 | RXGOODFRAMES | Good receive frames register |
| 0x01C8 0204 | RXBCASTFRAMES | Broadcast receive frames register (Total number of good broadcast frames received) |
| 0x01C8 0208 | RXMCASTFRAMES | Multicast receive frames register (Total number of good multicast frames received) |
| 0x01C8 020C | RXPAUSEFRAMES | Pause receive frames register |
| 0x01C8 0210 | RXCRCERRORS | Receive CRC errors register (Total number of frames received with CRC errors) |
| 0x01C8 0214 | RXALIGNCODEERRORS | Receive alignment/code errors register (Total number of frames received with alignment/code errors) |
| 0x01C8 0218 | RXOVERSIZED | Receive oversized frames register (Total number of oversized frames received) |
| 0x01C8 021C | RXJABBER | Receive jabber frames register (Total number of jabber frames received) |
| 0x01C8 0220 | RXUNDERSIZED | Receive undersized frames register (Total number of undersized frames received) |
| 0x01C8 0224 | RXFRAGMENTS | Receive Frame Fragments Register |
| 0x01C8 0228 | RXFILTERED | Filtered receive frames register |
| 0x01C8 022C | RXQOSFILTERED | Received QOS filtered frames register |
| 0x01C8 0230 | RXOCTETS | Receive octet frames register (Total number of received bytes in good frames) |
| 0x01C8 0234 | TXGOODFRAMES | Good Transmit Frames Register (Total number of good frames transmitted) |
| 0x01C8 0238 | TXBCASTFRAMES | Broadcast transmit frames register |
| 0x01C8 023C | TXMCASTFRAMES | Multicast transmit frames register |
| 0x01C8 0240 | TXPAUSEFRAMES | Pause transmit frames register |

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**Table 7-68. EMAC Statistics Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C8 0244 | TXDEFERRED | Deferred transmit frames register |
| 0x01C8 0248 | TXCOLLISION | Transmit collision frames register |
| 0x01C8 024C | TXSINGLECOLL | Transmit single collision frames register |
| 0x01C8 0250 | TXMULTICOLL | Transmit multiple collision frames register |
| 0x01C8 0254 | TXEXCESSIVECOLL | Transmit excessive collision frames register |
| 0x01C8 0258 | TXLATECOLL | Transmit late collision frames register |
| 0x01C8 025C | TXUNDERRUN | Transmit underrun error register |
| 0x01C8 0260 | TXCARRIERSENSE | Transmit carrier sense errors register |
| 0x01C8 0264 | TXOCTETS | Transmit octet frames register |
| 0x01C8 0268 | FRAME64 | Transmit and receive 64 octet frames register |
| 0x01C8 026C | FRAME65T127 | Transmit and receive 65 to 127 octet frames register |
| 0x01C8 0270 | FRAME128T255 | Transmit and receive 128 to 255 octet frames register |
| 0x01C8 0274 | FRAME256T511 | Transmit and receive 256 to 511 octet frames register |
| 0x01C8 0278 | FRAME512T1023 | Transmit and receive 512 to 1023 octet frames register |
| 0x01C8 027C | FRAME1024TUP | Transmit and receive 1024 to 1518 octet frames register |
| 0x01C8 0280 | NETOCTETS | Network octet frames register |
| 0x01C8 0284 | RXSOFOVERRUNS | Receive FIFO or DMA start of frame overruns register |
| 0x01C8 0288 | RXMOFOVERRUNS | Receive FIFO or DMA middle of frame overruns register |
| 0x01C8 028C | RXDMAOVERRUNS | Receive DMA start of frame and middle of frame overruns register |
| 0x01C8 0290 - 0x01C8 02FF | – | Reserved |

**Table 7-69. EMAC Control Module Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C8 1000 | CMIDVER | Identification and version register |
| 0x01C8 1004 | CMSOFTRESET | Software reset register |
| 0x01C8 1008 | CMEMCONTROL | Emulation control register |
| 0x01C8 100C | CMINTCTRL | Interrupt control register |
| 0x01C8 1010 | CMRXTHRESHINTEN | Receive threshold interrupt enable register |
| 0x01C8 1014 | CMRXINTEN | Receive interrupt enable register |
| 0x01C8 1018 | CMTXINTEN | Transmit interrupt enable register |
| 0x01C8 101C | CMMISCINTEN | Miscellaneous interrupt enable register |
| 0x01C8 1020 - 0x01C8 103F | – | Reserved |
| 0x01C8 1040 | CMRXTHRESHINTSTAT | Receive threshold interrupt status register |
| 0x01C8 1044 | CMRXINTSTAT | Receive interrupt status register |
| 0x01C8 1048 | CMTXINTSTAT | Transmit interrupt status register |
| 0x01C8 104C | CMMISCINTSTAT | Miscellaneous interrupt status register |
| 0x01C8 1050 - 0x01C8 106F | – | Reserved |
| 0x01C8 1070 | CMRXINTMAX | Receive interrupts per millisecond register |
| 0x01C8 1074 | CMTXINTMAX | Transmit interrupts per millisecond register |
| 0x01C8 1078 - 0x01C8 10FF | – | Reserved |
| 0x01C8 1100 - 0x01C8 1FFF | – | Reserved |

**Table 7-70. EMAC Descriptor Memory**

| HEX ADDRESS RANGE | ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C8 2000 - 0x01C8 3FFF | – | EMAC Control Module Descriptor Memory |


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### 7.16.4 EMAC Electrical Data/Timing

**Table 7-71. Timing Requirements for MRCLK - MII and GMII Operation (see Figure 7-49)**

| NO. | | | -1G | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1000 Mbps (GMII Only) | | 100 Mbps | | 10 Mbps | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(MRCLK)}$ | Cycle time, MRCLK | 8 | | 40 | | 400 | | ns |
| 2 | $t_{w(MRCLKH)}$ | Pulse duration, MRCLK high | 2.8 | | 14 | | 140 | | ns |
| 3 | $t_{w(MRCLKL)}$ | Pulse duration, MRCLK low | 2.8 | | 14 | | 140 | | ns |
| 4 | $t_{t(MRCLK)}$ | Transition time, MRCLK | | 1 | | 3 | | 3 | ns |

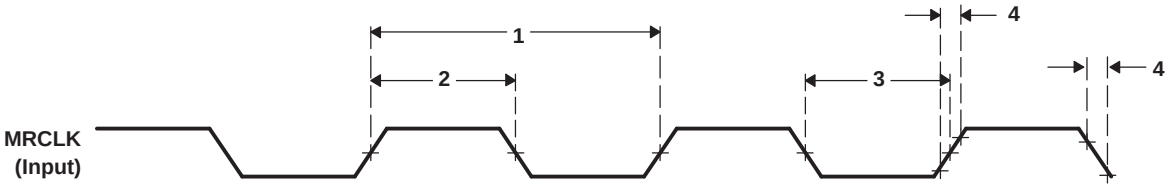


**Figure 7-49. MRCLK Timing (EMAC – Receive) [MII and GMII Operation]**

**Table 7-72. Timing Requirements for MTCLK - MII and GMII Operation (see Figure 7-50)**

| NO. | | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | 100 Mbps | | 10 Mbps | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(MTCLK)}$ | Cycle time, MTCLK | 40 | | 400 | | ns |
| 2 | $t_{w(MTCLKH)}$ | Pulse duration, MTCLK high | 14 | | 140 | | ns |
| 3 | $t_{w(MTCLKL)}$ | Pulse duration, MTCLK low | 14 | | 140 | | ns |
| 4 | $t_{t(MTCLK)}$ | Transition time, MTCLK | | 3 | | 3 | ns |

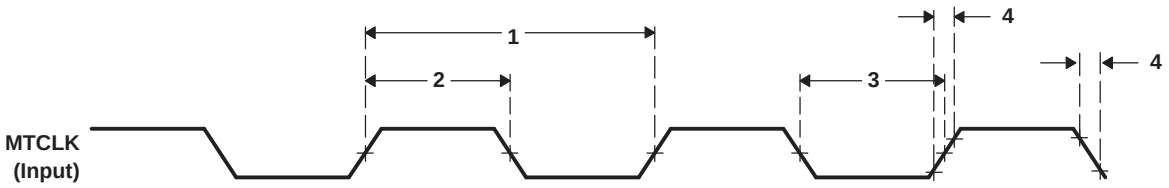


**Figure 7-50. MTCLK Timing (EMAC – Transmit) [MII and GMII Operation]**

**Table 7-73. Timing Requirements for RFTCLK - GMII Operation (see Figure 7-51)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | 1000 Mbps | | |
| | | | MIN | MAX | |
| 1 | $t_{c(RFTCLK)}$ | Cycle time, RFTCLK | 8 | | ns |
| 2 | $t_{w(RFTCLKH)}$ | Pulse duration, RFTCLK high | 2.8 | | ns |
| 3 | $t_{w(RFTCLKL)}$ | Pulse duration, RFTCLK low | 2.8 | | ns |
| 4 | $t_{t(RFTCLK)}$ | Transition time, RFTCLK | | 1 | ns |

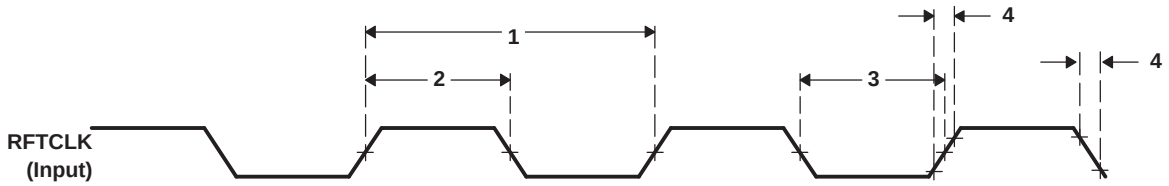


**Figure 7-51. RFTCLK Timing [GMII Operation]**


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**Table 7-74. Switching Characteristics Over Recommended Operating Conditions for GMTCLK - GMII Operation (see Figure 7-52)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | 1000 Mbps | | |
| | | | MIN | MAX | |
| 1 | $t_{c(GMTCLK)}$ | Cycle time, GMTCLK | 8 | | ns |
| 2 | $t_{w(GMTCLKH)}$ | Pulse duration, GMTCLK high | 2.8 | | ns |
| 3 | $t_{w(GMTCLKL)}$ | Pulse duration, GMTCLK low | 2.8 | | ns |
| 4 | $t_{t(GMTCLK)}$ | Transition time, GMTCLK | | 1 | ns |

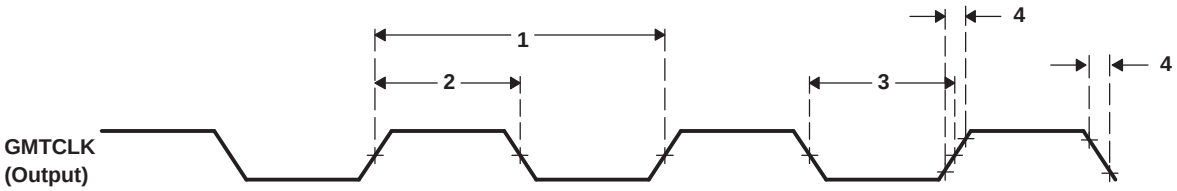


**Figure 7-52. GMTCLK Timing (EMAC – Transmit) [GMII Operation]**

**Table 7-75. Timing Requirements for EMAC MII and GMII Receive 10/100/1000 Mbit/s(1) (see Figure 7-53)**

| NO. | | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | 1000 Mbps | | 100/10 Mbps | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(MRXD-MRCLKH)}$ | Setup time, receive selected signals valid before MRCLK high | 2 | | 8 | | ns |
| 2 | $t_{h(MRCLKH-MRXD)}$ | Hold time, receive selected signals valid after MRCLK high | 0 | | 8 | | ns |

(1) For **MII**, Receive selected signals include: MRXD[3:0], MRXDV, and MRXER.
For **GMII**, Receive selected signals include: MRXD[7:0], MRXDV, and MRXER.

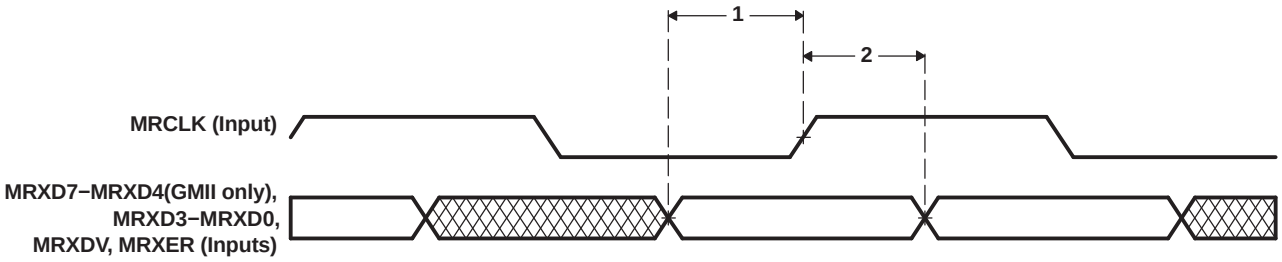


**Figure 7-53. EMAC Receive Interface Timing [MII and GMII Operation]**

**Table 7-76. Switching Characteristics Over Recommended Operating Conditions for EMAC MII and GMII Transmit 10/100 Mbit/s(1) (see Figure 7-54)**

| NO. | PARAMETER | | -1G 100/10 Mbps MIN | -1G 100/10 Mbps MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{d(MTCLKH-MTXD)}$ | Delay time, MTCLK high to transmit selected signals valid | 5 | 25 | ns |

(1) For **MII**, Transmit selected signals include: MTXD[3:0] and MTXEN.
For **GMII**, Transmit selected signals include: MTXD[7:0] and MTXEN.

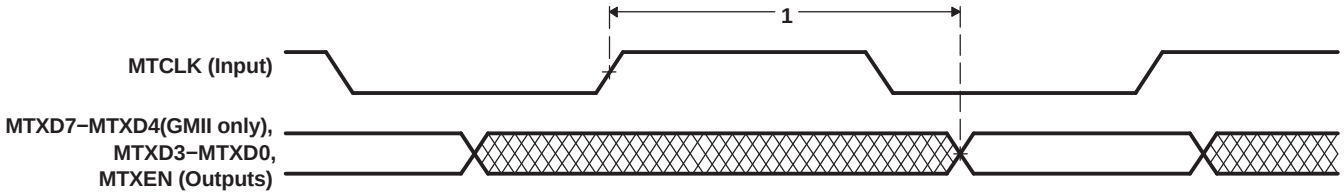


**Figure 7-54. EMAC Transmit Interface Timing [MII and GMII Operation]**

**Table 7-77. Switching Characteristics Over Recommended Operating Conditions for EMAC GMII Transmit 1000 Mbit/s(1) (see Figure 7-55)**

| NO. | PARAMETER | | -1G 1000 Mbps MIN | -1G 1000 Mbps MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{d(GMTCLKH-MTXD)}$ | Delay time, GMTCLK high to transmit selected signals valid | 0.5 | 5 | ns |

(1) For **GMII**, Transmit selected signals include: MTXD[7:0] and MTXEN.

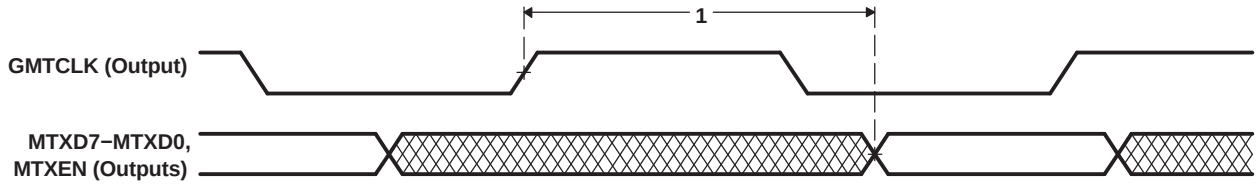


**Figure 7-55. EMAC Transmit Interface Timing [GMII Operation]**


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## 7.17 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The Management Data Input/Output (MDIO) module implements the 802.3 serial management interface to interrogate and control Ethernet PHY(s) using a shared two-wire bus. Host software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. Only one PHY may be connected at any given time.

For more detailed information on the MDIO peripheral, see the *TMS320DM646x DMSoC Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module* User's Guide (literature number SPRUEQ6) . For a list of supported registers and register fields, see Table 7-78, MDIO Registers in this data manual.

### *7.17.1 MDIO Peripheral Register Description(s)*

**Table 7-78. MDIO Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C8 4000 | VERSION | MDIO version register |
| 0x01C8 4004 | CONTROL | MDIO control register |
| 0x01C8 4008 | ALIVE | MDIO PHY alive status register |
| 0x01C8 400C | LINK | MDIO PHY link status register |
| 0x01C8 4010 | LINKINTRAW | MDIO link status change interrupt (unmasked) register |
| 0x01C8 4014 | LINKINTMASKED | MDIO link status change interrupt (masked) register |
| 0x01C8 4018 - 0x01C8 401F | – | Reserved |
| 0x01C8 4020 | USERINTRAW | MDIO user command complete interrupt (unmasked) register |
| 0x01C8 4024 | USERINTMASKED | MDIO user command complete interrupt (masked) register |
| 0x01C8 4028 | USERINTMASKSET | MDIO user command complete interrupt mask set register |
| 0x01C8 402C | USERINTMASKCLEAR | MDIO user command complete interrupt mask clear register |
| 0x01C8 4030 - 0x01C8 407F | – | Reserved |
| 0x01C8 4080 | USERACCESS0 | MDIO user access register 0 |
| 0x01C8 4084 | USERPHYSEL0 | MDIO user PHY select register 0 |
| 0x01C8 4088 | USERACCESS1 | MDIO user access register 1 |
| 0x01C8 408C | USERPHYSEL1 | MDIO user PHY select register 1 |
| 0x01C8 4090 - 0x01C8 47FF | – | Reserved |

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### 7.17.2 Management Data Input/Output (MDIO) Electrical Data/Timing

**Table 7-79. Timing Requirements for MDIO Input (see Figure 7-56 and Figure 7-57)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(MDCLK)}$ | Cycle time, MDCLK | 400 | | ns |
| 2 | $t_{w(MDCLK)}$ | Pulse duration, MDCLK high/low | 180 | | ns |
| 3 | $t_{t(MDCLK)}$ | Transition time, MDCLK | | 5 | ns |
| 4 | $t_{su(MDIO-MDCLKH)}$ | Setup time, MDIO data input valid before MDCLK high | 10 | | ns |
| 5 | $t_{h(MDCLKH-MDIO)}$ | Hold time, MDIO data input valid after MDCLK high | 0 | | ns |

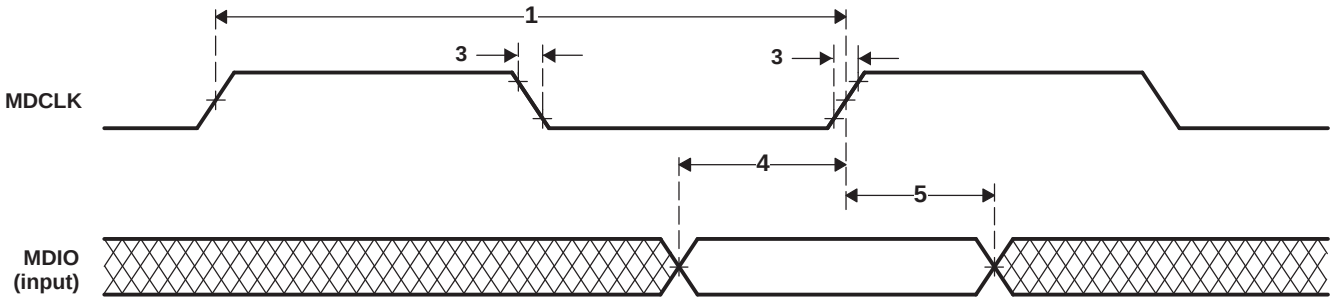


**Figure 7-56. MDIO Input Timing**

**Table 7-80. Switching Characteristics Over Recommended Operating Conditions for MDIO Output (see Figure 7-57)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 7 | $t_{d(MDCLKL-MDIO)}$ | Delay time, MDCLK low to MDIO data output valid | | 100 | ns |

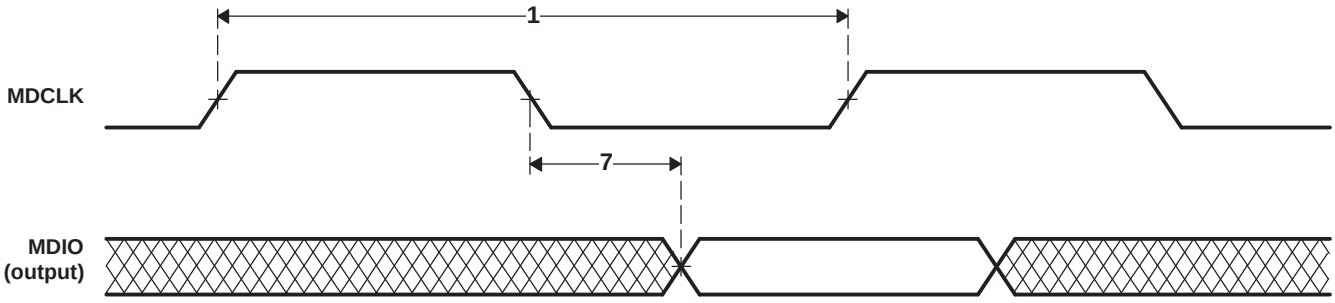


**Figure 7-57. MDIO Output Timing**


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## 7.18 Host-Port Interface (HPI) Peripheral

The HPI is a parallel port through which a host processor can directly access the CPU memory space. The host device functions as a master to the interface, which increases ease of access. The host and CPU can exchange information via internal or external memory. The host also has direct access to memory-mapped peripherals. Connectivity to the CPU memory space is provided through the EDMA3 controller.

### 7.18.1 HPI Device-Specific Information

The DM6467T device includes a user-configurable 32- or 16-bit Host-port interface (HPI32/HPI16).

- Multiplexed (address/data) operation
- Configurable single full-word cycle and dual half-word cycle access modes
- Bursting available utilizing 8-word read and write FIFOs
- HPIA register supports auto-incrementing
- HPID register/FIFOs providing data-path between external host interface and system bus
- Multiple strobes and control signals to allow flexible host connection
- Configurable asynchronous HRDY output to allow HPI to insert wait states to the Host [System Module Register HPICTL.HRDYMODE]
- Software control of data prefetching to the HPID/FIFOs
- DMSoC-to-Host interrupt output signal controlled by HPIC accesses
- Host-to-DMSoC interrupt controlled by HPIC accesses

**NOTE:** The DM6467T HPI ***does not*** support the $\overline{\text{HAS}}$ feature. For proper HPI operation if the $\overline{\text{HAS}}$ pin (D4) is routed out, the $\overline{\text{HAS}}$ pin ***must*** be pulled up via an external resistor.

The DM6467T HPICTL register (0x01C4 0030) is part of the System Module Registers. The HPICTL register controls write access to the HPI peripheral control and address registers as well as determines the host time-out value. The HPICTL System Module Register also determines the operation of the HRDY output which allows the HPI to insert wait states to the Host. For more detailed information on the HPICTL System Module Register, see Section 4.6.2, *Peripheral Selection After Device Reset*.

For more detailed information on the HPI peripheral, see the *TMS320DM646x DMSoC Host Port Interface (HPI)* User's Guide (literature number SPRUES1).

### 7.18.2 HPI Bus Master

The HPI peripheral includes a bus master interface that allows external device initiated transfers to access the DM6467T system bus. Table 7-81 shows the memory map for the HPI master interface.

**Table 7-81. HPI Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | HPI ACCESS |
|---|---|---|---|
| 0x0000 0000 | 0x01BF FFFF | 28M | Reserved |
| 0x01C0 0000 | 0x0FFF FFFF | 228M | CFG Bus Peripherals |
| 0x1000 0000 | 0x1000 FFFF | 64K | Reserved |
| 0x1001 0000 | 0x1001 3FFF | 16K | ARM RAM 0 (Data) |
| 0x1001 4000 | 0x1001 7FFF | 16K | ARM RAM 1 (Data) |
| 0x1001 8000 | 0x1001 FFFF | 32K | ARM ROM (Data) |

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**Table 7-81. HPI Master Memory Map (continued)**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | HPI ACCESS |
|---|---|---|---|
| 0x1002 0000 | 0x10FF FFFF | 16256K | Reserved |
| 0x1100 0000 | 0x113F FFFF | 4M | |
| 0x1140 0000 | 0x114F FFFF | 1M | |
| 0x1150 0000 | 0x115F FFFF | 1M | |
| 0x1160 0000 | 0x116F FFFF | 1M | |
| 0x1170 0000 | 0x117F FFFF | 1M | |
| 0x1180 0000 | 0x1180 FFFF | 64K | |
| 0x1181 0000 | 0x1181 7FFF | 32K | |
| 0x1181 8000 | 0x1183 7FFF | 128K | C64x+ L2 RAM/Cache |
| 0x1183 8000 | 0x118F FFFF | 800K | Reserved |
| 0x1190 0000 | 0x11DF FFFF | 5M | |
| 0x11E0 0000 | 0x11E0 7FFF | 32K | C64x+ L1P RAM/Cache |
| 0x11E0 8000 | 0x11EF FFFF | 992K | Reserved |
| 0x11F0 0000 | 0x11F0 7FFF | 32K | C64x+ L1D RAM/Cache |
| 0x11F0 8000 | 0x11FF FFFF | 992K | Reserved |
| 0x1200 0000 | 0x4BFF FFFF | 928M | |
| 0x4C00 0000 | 0x4FFF FFFF | 64M | VLYNQ (Remote Data) |
| 0x5000 0000 | 0x7FFF FFFF | 768M | Reserved |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |

### *7.18.3 HPI Peripheral Register Description(s)*

**Table 7-82. HPI Control Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|---|---|---|---|
| 01C6 7800 | PID | Peripheral Identification Register | |
| 01C6 7804 | PWREMU_MGMT | HPI power and emulation management register | The ARM/C64x+ has read/write access to the PWREMU_MGMT register. |
| 01C6 7808 - 01C6 782F | - | Reserved | |
| 01C6 7830 | HPIC | HPI control register | The Host and the ARM/C64x+ both have read/write access to the HPIC register. |
| 01C6 7834 | HPIA (HPIAW)(1) | HPI address register (Write) | The Host has read/write access to the HPIA registers. The ARM/C64x+ has only read access to the HPIA registers. |
| 01C6 7838 | HPIA (HPIAR)(1) | HPI address register (Read) | |
| 01C6 783C - 01C6 7FFF | - | Reserved | |

(1) There are two 32-bit HPIA registers: HPIAR for read operations and HPIAW for write operations. The HPI can be configured such that HPIAR and HPIAW act as a single 32-bit HPIA (single-HPIA mode) or as two separate 32-bit HPIAs (dual-HPIA mode) from the perspective of the Host. The ARM/C64x+ can access HPIAW and HPIAR independently. For more details about the HPIA registers and their modes, see the *TMS320DM646x DMSoC Host Port Interface (HPI)* User's Guide (literature number SPRUES1).


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### 7.18.4 HPI Electrical Data/Timing

**Table 7-83. Timing Requirements for Host-Port Interface Cycles(1) (2) (see Figure 7-58 through Figure 7-61)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{su(SELV-HSTBL)}$ | Setup time, select signals(3) valid before $\overline{\text{HSTROBE}}$ low | 5 | | ns |
| 2 | $t_{h(HSTBL-SELV)}$ | Hold time, select signals(3) valid after $\overline{\text{HSTROBE}}$ low | 2 | | ns |
| 3 | $t_{w(HSTBL)}$ | Pulse duration, $\overline{\text{HSTROBE}}$ active low | 15 | | ns |
| 4 | $t_{w(HSTBH)}$ | Pulse duration, $\overline{\text{HSTROBE}}$ inactive high between consecutive accesses | 2M | | ns |
| 11 | $t_{su(HDV-HSTBH)}$ | Setup time, host data valid before $\overline{\text{HSTROBE}}$ high | 5 | | ns |
| 12 | $t_{h(HSTBH-HDV)}$ | Hold time, host data valid after $\overline{\text{HSTROBE}}$ high | 0.15 | | ns |
| 13 | $t_{h(HRDYL-HSTBL)}$ | Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly. | 0 | | ns |

(1) $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.
(2) M = SYSCLK3 period = (CPU clock frequency)/4 in ns. For example, when running parts at 1 GHz, use M = 4 ns.
(3) Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$. For HPI16 mode only, select signals also includes HHWIL.

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**Table 7-84. Switching Characteristics for Host-Port Interface Cycles(1) (2) (3) (see Figure 7-58 through Figure 7-61)**

| NO. | PARAMETER | | | -1G MIN | -1G MAX | UNIT |
|---|---|---|---|---|---|---|
| 5 | $t_{d(HSTBL-HRDYV)}$ | Delay time, HSTROBE low to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: Back-to-back HPIA writes (can be either first or second half-word)<br>*Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word)<br>*Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word)<br>*Case 4*: HPIA write and Write FIFO not empty<br><br>For HPI Read, HRDY can go high (*not ready*) for these HPI Read conditions:<br>*Case 1*: HPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access)<br>*Case 2*: First half-word access of HPID Read without auto-increment<br>For HPI Read, HRDY stays low (*ready*) for these HPI Read conditions:<br>*Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access)<br>*Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access)<br>*Case 3*: HPIC or HPIA read (applies to either half-word access) | | 12 | ns |
| 6 | $t_{en(HSTBL-HD)}$ | Enable time, HD driven from HSTROBE low | | 2 | | ns |
| 7 | $t_{d(HRDYL-HDV)}$ | Delay time, HRDY low to HD valid | | | 0 | ns |
| 8 | $t_{oh(HSTBH-HDV)}$ | Output hold time, HD valid after HSTROBE high | | 1.5 | | ns |
| 14 | $t_{dis(HSTBH-HDV)}$ | Disable time, HD high-impedance from HSTROBE high | | | 12 | ns |
| 15 | $t_{d(HSTBL-HDV)}$ | Delay time, HSTROBE low to HD valid | For HPI Read. Applies to conditions where data is already residing in HPID/FIFO:<br>*Case 1*: HPIC or HPIA read<br>*Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO<br>*Case 3*: Second half-word of HPID read with or without auto-increment | | 12 | ns |

(1) M = SYSCLK3 period = (CPU clock frequency)/4 in ns. For example, when running parts at 1 GHz, use 4 ns.
(2) HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
(3) By design, whenever HCS is driven inactive (high), HPI will drive HRDY active (low).


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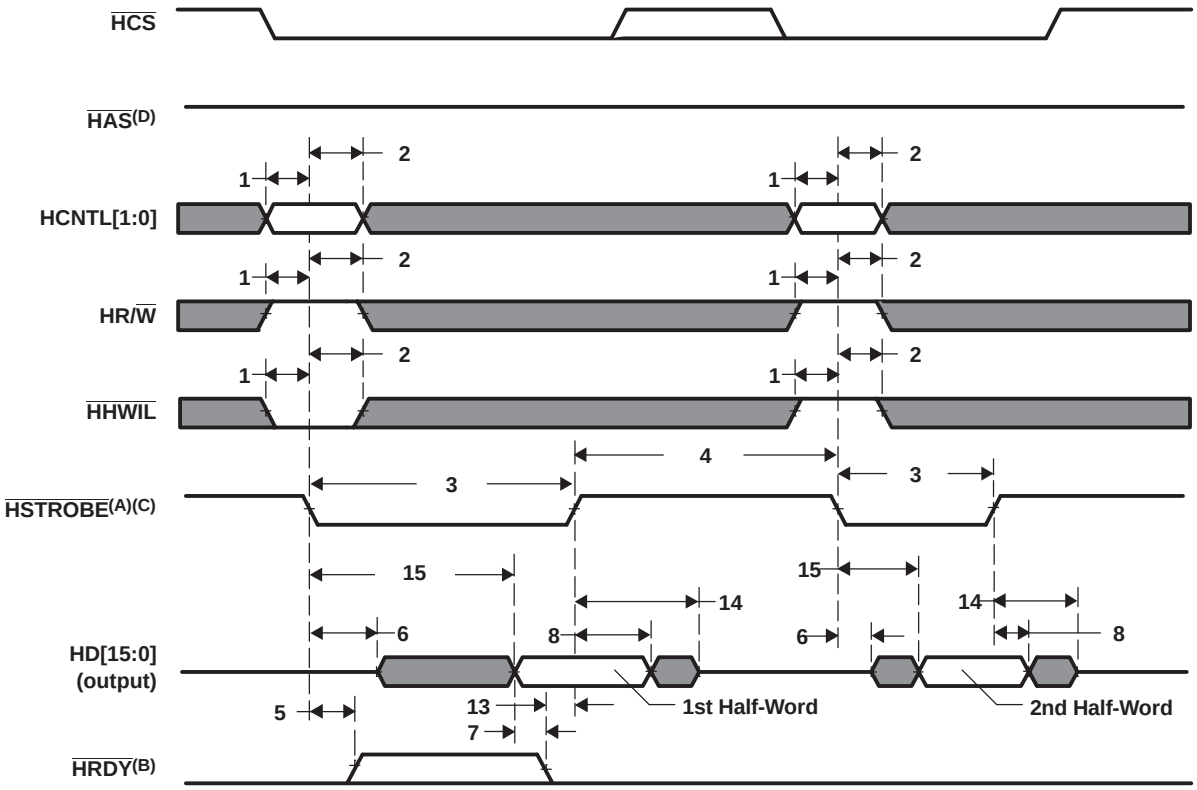
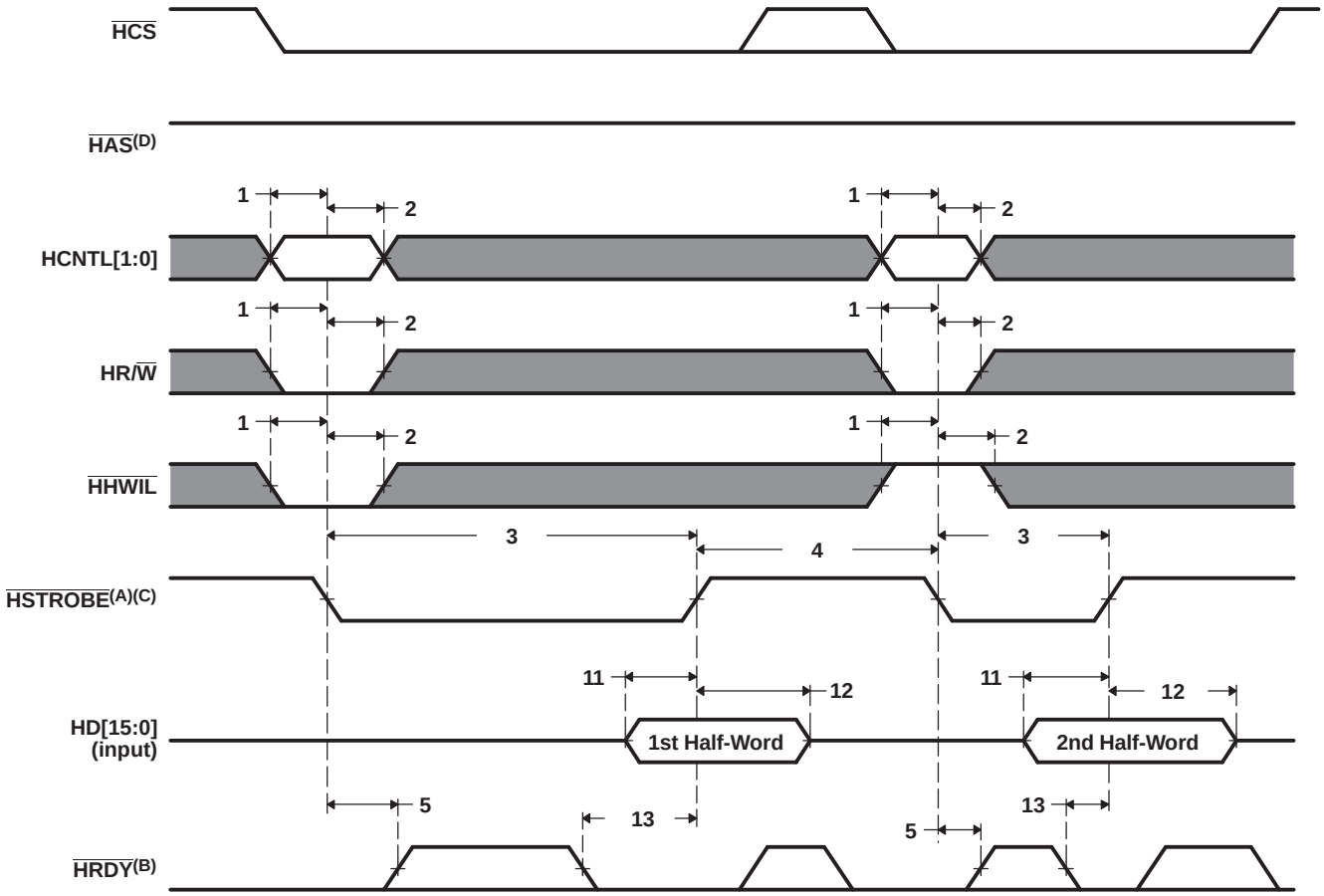



A. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur.
For more detailed information on the HPI peripheral, see the *TMS320DM646x DMSoC Host Port Interface (HPI)* User's Guide (literature number SPRUES1).
C. HCS reflects typical HCS behavior when HSTROBE assertion is caused by HDS1 or HDS2. HCS timing requirements are reflected by parameters for HSTROBE.
D. For proper HPI operation, HAS **must** be pulled up via an external resistor.

**Figure 7-58. HPI16 Read Timing (HAS Not Used, Tied High)**




A. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur.
For more detailed information on the HPI peripheral, see the *TMS320DM646x DMSoC Host Port Interface (HPI)* User's Guide (literature number SPRUES1).

C. HCS reflects typical HCS behavior when HSTROBE assertion is caused by HDS1 or HDS2. HCS timing requirements are reflected by parameters for HSTROBE.

D. For proper HPI operation, HAS **must** be pulled up via an external resistor.

**Figure 7-59. HPI16 Write Timing (HAS Not Used, Tied High)**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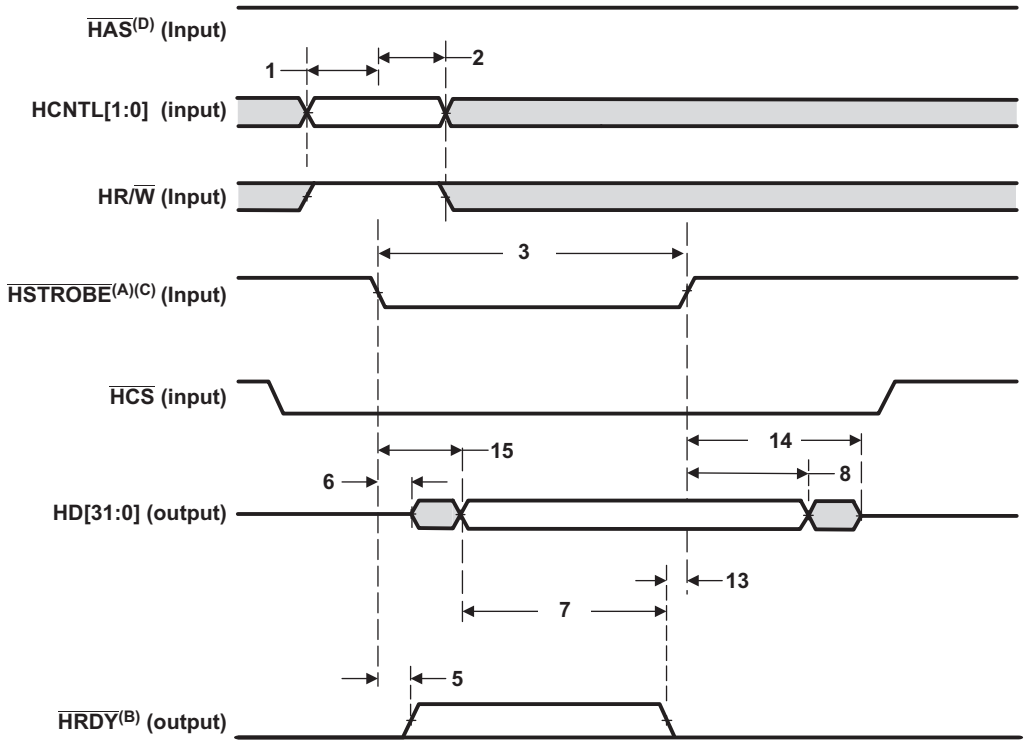
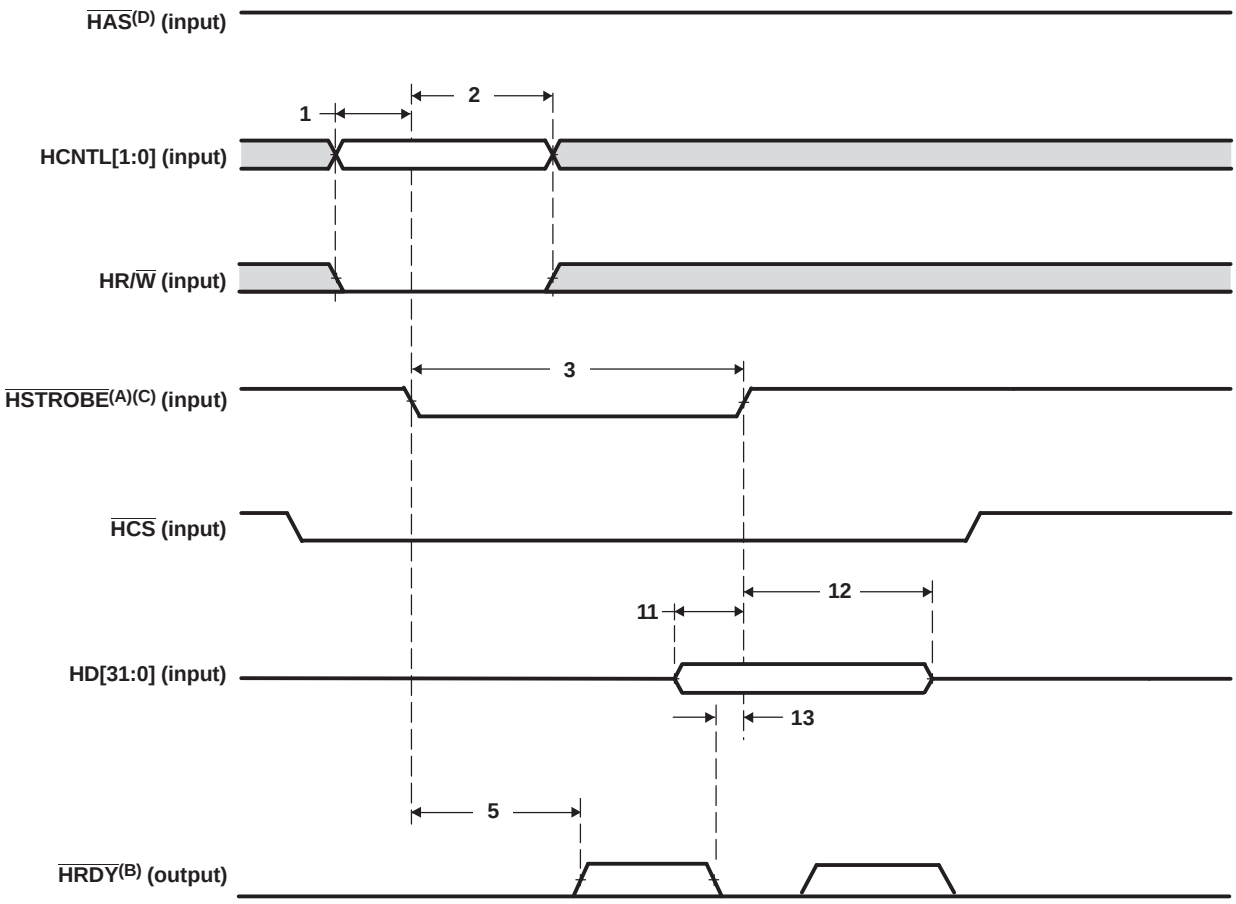



A. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur.
For more detailed information on the HPI peripheral, see the *TMS320DM646x DMSoC Host Port Interface (HPI)* User's Guide (literature number SPRUES1).
C. HCS reflects typical HCS behavior when HSTROBE assertion is caused by HDS1 or HDS2. HCS timing requirements are reflected by parameters for HSTROBE.
D. For Proper HPI operation, HAS **must** be pulled up via an external resistor.

**Figure 7-60. HPI32 Read Timing (HAS Not Used, Tied High)**




A. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur.
For more detailed information on the HPI peripheral, see the *TMS320DM646x DMSoC Host Port Interface (HPI)* User's Guide (literature number SPRUES1).

C. HCS reflects typical HCS behavior when HSTROBE assertion is caused by HDS1 or HDS2. HCS timing requirements are reflected by parameters for HSTROBE.

D. For proper HPI operation, HAS **must** be pulled up via an external resistor.

**Figure 7-61. HPI32 Write Timing (HAS Not Used, Tied High)**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## 7.19 USB 2.0 [see Note]

The DM6467T USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds: high-speed (HS: 480 Mb/s) and full-speed (FS: 12 Mb/s)
- USB 2.0 host at speeds HS, FS, and low speed (LS: 1.5 Mb/s)
- Each endpoint (other than endpoint 0) can support all transfer modes (control, bulk, interrupt, and isochronous)
- 4 Transmit (TX) and 4 Receive (RX) endpoints in addition to endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Connects to a standard UTMI+ PHY with a 60-MHz, 8-bit interface
- External 5-V power supply for VBUS, when operating as Host, enabled directly by the USB controller via a dedicated signal
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

**Note**: USB2.0 is not supported on -1G parts that are dated prior to May 1, 2010. See the TMS320DM6467T Silicon Errata (Literature Number: SPRZ307) for more details on how to decode the date from package markings.

### *7.19.1 USB DMA Master*

The USB2.0 peripheral interface includes a master DMA engine that allows the USB to access the DM6467T system bus. Table 7-85 shows the memory map for the USB2.0 DMA engine.

**Table 7-85. USB2.0 DMA Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | USB2.0 DMA ACCESS |
|---|---|---|---|
| 0x0000 0000 | 0x0FFF FFFF | 256M | Reserved |
| 0x1000 0000 | 0x1000 FFFF | 64K | Reserved |
| 0x1001 0000 | 0x1001 3FFF | 16K | ARM RAM 0 (Data) |
| 0x1001 4000 | 0x1001 7FFF | 16K | ARM RAM 1 (Data) |
| 0x1001 8000 | 0x1001 FFFF | 32K | ARM ROM (Data) |
| 0x1002 0000 | 0x10FF FFFF | 16256K | Reserved |
| 0x1100 0000 | 0x113F FFFF | 4M | |
| 0x1140 0000 | 0x114F FFFF | 1M | |
| 0x1150 0000 | 0x115F FFFF | 1M | |
| 0x1160 0000 | 0x116F FFFF | 1M | |
| 0x1170 0000 | 0x117F FFFF | 1M | |
| 0x1180 0000 | 0x1180 FFFF | 64K | |
| 0x1181 0000 | 0x1181 7FFF | 32K | |
| 0x1181 8000 | 0x1183 7FFF | 128K | C64x+ L2 RAM/Cache |
| 0x1183 8000 | 0x118F FFFF | 800K | Reserved |
| 0x1190 0000 | 0x11DF FFFF | 5M | |
| 0x11E0 0000 | 0x11E0 7FFF | 32K | C64x+ L1P RAM/Cache |
| 0x11E0 8000 | 0x11EF FFFF | 992K | Reserved |
| 0x11F0 0000 | 0x11F0 7FFF | 32K | C64x+ L1D RAM/Cache |
| 0x11F0 8000 | 0x11FF FFFF | 992K | Reserved |
| 0x1200 0000 | 0x4BFF FFFF | 928M | |
| 0x4C00 0000 | 0x4FFF FFFF | 64M | VLYNQ (Remote Data) |
| 0x5000 0000 | 0x7FFF FFFF | 768M | Reserved |

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**Table 7-85. USB2.0 DMA Master Memory Map (continued)**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | USB2.0 DMA ACCESS |
|---|---|---|---|
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |

### *7.19.2 USB2.0 Device-Specific Information*

The DM6467T USBCTL register (0x01C4 00034) is part of the System Module Registers. The USBCTL register controls the USB data polarity, host/peripheral mode, and VBUS sense, along with the PHY power and clock good, PHY PLL suspend override, and PHY power down. For more detailed information on the USBCTL System Module Register, see Section 4.6.2, *Peripheral Selection After Device Reset*

For more detailed information on the USB2.0 peripheral, see the *TMS320DM646x DMSoC Universal Serial Bus (USB) Controller* User's Guide (literature number SPRUER7).


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### 7.19.3 USB2.0 Peripheral Register Description(s)

Table 7-86 shows the USB perripheral register memory mapping.

**Table 7-86. USB2.0 Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C6 4000 | REVR | Revision Register |
| 0x01C6 4004 | CTRLR | Control Register |
| 0x01C6 4008 | STATR | Status Register |
| 0x01C6 400C - 0x01C6 400F | – | Reserved |
| 0x01C6 4010 | RNDISR | RNDIS Register |
| 0x01C6 4014 | AUTOREQ | Auto Request Register |
| 0x01C6 4018 - 0x01C6 401F | – | Reserved |
| 0x01C6 4020 | INTSRCR | USB Interrupt Source Register |
| 0x01C6 4024 | INTSETR | USB Interrupt Source Set Register |
| 0x01C6 4028 | INTCLRR | USB Interrupt Source Clear Register |
| 0x01C6 402C | INTMSKR | USB Interrupt Mask Register |
| 0x01C6 4030 | INTMSKSETR | USB Interrupt Mask Set Register |
| 0x01C6 4034 | INTMSKCLRR | USB Interrupt Mask Clear Register |
| 0x01C6 4038 | INTMASKEDR | USB Interrupt Source Masked Register |
| 0x01C6 403C | EOIR | USB End of Interrupt Register |
| 0x01C6 4040 | INTVECTR | USB Interrupt Vector Register |
| 0x01C6 4044 - 0x01C6 407F | – | Reserved |
| 0x01C6 4080 | TCPPICR | TX CPPI Control Register |
| 0x01C6 4084 | TCPPITDR | TX CPPI Teardown Register |
| 0x01C6 4088 | TCPPIEOIR | TX CPPI DMA Controller End of Interrupt Register |
| 0x01C6 408C | TCPPIIVECTR | TX CPPI DMA Controller Interrupt Vector Register |
| 0x01C6 4090 | TCPPIMSKSR | TX CPPI Masked Status Register |
| 0x01C6 4094 | TCPPIRAWSR | TX CPPI Raw Status Register |
| 0x01C6 4098 | TCPPIIENSETR | TX CPPI Interrupt Enable Set Register |
| 0x01C6 409C | TCPPIIENCLRR | TX CPPI Interrupt Enable Clear Register |
| 0x01C6 40A0 - 0x01C6 40BF | – | Reserved |
| 0x01C6 40C0 | RCPPICR | RX CPPI Control Register |
| 0x01C6 40C4 - 0x01C6 40CF | – | Reserved |
| 0x01C6 40D0 | RCPPIMSKSR | RX CPPI Masked Status Register |
| 0x01C6 40D4 | RCPPIRAWSR | RX CPPI Raw Status Register |
| 0x01C6 40D8 | RCPPIENSETR | RX CPPI Interrupt Enable Set Register |
| 0x01C6 40DC | RCPPIIENCLRR | RX CPPI Interrupt Enable Clear Register |
| 0x01C6 40E0 | RBUFCNT0 | RX Buffer Count 0 Register |
| 0x01C6 40E4 | RBUFCNT1 | RX Buffer Count 1 Register |
| 0x01C6 40E8 | RBUFCNT2 | RX Buffer Count 2 Register |
| 0x01C6 40EC | RBUFCNT3 | RX Buffer Count 3 Register |
| 0x01C6 40F0 - 0x01C6 40FF | – | Reserved |
| **TX/RX CCPI Channel 0 State Block** | | |
| 0x01C6 4100 | TCPPIDMASTATEW0 | TX CPPI DMA State Word 0 |

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**Table 7-86. USB2.0 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C6 4104 | TCPPIDMASTATEW1 | TX CPPI DMA State Word 1 |
| 0x01C6 4108 | TCPPIDMASTATEW2 | TX CPPI DMA State Word 2 |
| 0x01C6 410C | TCPPIDMASTATEW3 | TX CPPI DMA State Word 3 |
| 0x01C6 4110 | TCPPIDMASTATEW4 | TX CPPI DMA State Word 4 |
| 0x01C6 4114 | TCPPIDMASTATEW5 | TX CPPI DMA State Word 5 |
| 0x01C6 4118 | – | Reserved |
| 0x01C6 411C | TCPPICOMPPTR | TX CPPI Completion Pointer |
| 0x01C6 4120 | RCPPIDMASTATEW0 | RX CPPI DMA State Word 0 |
| 0x01C6 4124 | RCPPIDMASTATEW1 | RX CPPI DMA State Word 1 |
| 0x01C6 4128 | RCPPIDMASTATEW2 | RX CPPI DMA State Word 2 |
| 0x01C6 412C | RCPPIDMASTATEW3 | RX CPPI DMA State Word 3 |
| 0x01C6 4130 | RCPPIDMASTATEW4 | RX CPPI DMA State Word 4 |
| 0x01C6 4134 | RCPPIDMASTATEW5 | RX CPPI DMA State Word 5 |
| 0x01C6 4138 | RCPPIDMASTATEW6 | RX CPPI DMA State Word 6 |
| 0x01C6 413C | RCPPICOMPPTR | RX CPPI Completion Pointer |
| **TX/RX CCPI Channel 1 State Block** | | |
| 0x01C6 4140 | TCPPIDMASTATEW0 | TX CPPI DMA State Word 0 |
| 0x01C6 4144 | TCPPIDMASTATEW1 | TX CPPI DMA State Word 1 |
| 0x01C6 4148 | TCPPIDMASTATEW2 | TX CPPI DMA State Word 2 |
| 0x01C6 414C | TCPPIDMASTATEW3 | TX CPPI DMA State Word 3 |
| 0x01C6 4150 | TCPPIDMASTATEW4 | TX CPPI DMA State Word 4 |
| 0x01C6 4154 | TCPPIDMASTATEW5 | TX CPPI DMA State Word 5 |
| 0x01C6 4158 | – | Reserved |
| 0x01C6 415C | TCPPICOMPPTR | TX CPPI Completion Pointer |
| 0x01C6 4160 | RCPPIDMASTATEW0 | RX CPPI DMA State Word 0 |
| 0x01C6 4164 | RCPPIDMASTATEW1 | RX CPPI DMA State Word 1 |
| 0x01C6 4168 | RCPPIDMASTATEW2 | RX CPPI DMA State Word 2 |
| 0x01C6 416C | RCPPIDMASTATEW3 | RX CPPI DMA State Word 3 |
| 0x01C6 4170 | RCPPIDMASTATEW4 | RX CPPI DMA State Word 4 |
| 0x01C6 4174 | RCPPIDMASTATEW5 | RX CPPI DMA State Word 5 |
| 0x01C6 4178 | RCPPIDMASTATEW6 | RX CPPI DMA State Word 6 |
| 0x01C6 417C | RCPPICOMPPTR | RX CPPI Completion Pointer |
| **TX/RX CCPI Channel 2 State Block** | | |
| 0x01C6 4180 | TCPPIDMASTATEW0 | TX CPPI DMA State Word 0 |
| 0x01C6 4184 | TCPPIDMASTATEW1 | TX CPPI DMA State Word 1 |
| 0x01C6 4188 | TCPPIDMASTATEW2 | TX CPPI DMA State Word 2 |
| 0x01C6 418C | TCPPIDMASTATEW3 | TX CPPI DMA State Word 3 |
| 0x01C6 4190 | TCPPIDMASTATEW4 | TX CPPI DMA State Word 4 |
| 0x01C6 4194 | TCPPIDMASTATEW5 | TX CPPI DMA State Word 5 |
| 0x01C6 4198 | – | Rserved |
| 0x01C6 419C | TCPPICOMPPTR | TX CPPI Completion Pointer |
| 0x01C6 41A0 | RCPPIDMASTATEW0 | RX CPPI DMA State Word 0 |
| 0x01C6 41A4 | RCPPIDMASTATEW1 | RX CPPI DMA State Word 1 |
| 0x01C6 41A8 | RCPPIDMASTATEW2 | RX CPPI DMA State Word 2 |
| 0x01C6 41AC | RCPPIDMASTATEW3 | RX CPPI DMA State Word 3 |
| 0x01C6 41B0 | RCPPIDMASTATEW4 | RX CPPI DMA State Word 4 |
| 0x01C6 41B4 | RCPPIDMASTATEW5 | RX CPPI DMA State Word 5 |


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**Table 7-86. USB2.0 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C6 41B8 | RCPPIDMASTATEW6 | RX CPPI DMA State Word 6 |
| 0x01C6 41BC | RCPPICOMPPTR | RX CPPI Completion Pointer |
| **TX/RX CCPI Channel 3 State Block** | | |
| 0x01C6 41C0 | TCPPIDMASTATEW0 | TX CPPI DMA State Word 0 |
| 0x01C6 41C4 | TCPPIDMASTATEW1 | TX CPPI DMA State Word 1 |
| 0x01C6 41C8 | TCPPIDMASTATEW2 | TX CPPI DMA State Word 2 |
| 0x01C6 41CC | TCPPIDMASTATEW3 | TX CPPI DMA State Word 3 |
| 0x01C6 41D0 | TCPPIDMASTATEW4 | TX CPPI DMA State Word 4 |
| 0x01C6 41D4 | TCPPIDMASTATEW5 | TX CPPI DMA State Word 5 |
| 0x01C6 41D8 | – | Rserved |
| 0x01C6 41DC | TCPPICOMPPTR | TX CPPI Completion Pointer |
| 0x01C6 41E0 | RCPPIDMASTATEW0 | RX CPPI DMA State Word 0 |
| 0x01C6 41E4 | RCPPIDMASTATEW1 | RX CPPI DMA State Word 1 |
| 0x01C6 41E8 | RCPPIDMASTATEW2 | RX CPPI DMA State Word 2 |
| 0x01C6 41EC | RCPPIDMASTATEW3 | RX CPPI DMA State Word 3 |
| 0x01C6 41F0 | RCPPIDMASTATEW4 | RX CPPI DMA State Word 4 |
| 0x01C6 41F4 | RCPPIDMASTATEW5 | RX CPPI DMA State Word 5 |
| 0x01C6 41F8 | RCPPIDMASTATEW6 | RX CPPI DMA State Word 6 |
| 0x01C6 41FC | RCPPICOMPPTR | RX CPPI Completion Pointer |
| 0x01C6 4200 - 0x01C6 43FF | – | Reserved |
| **Core Registers** | | |
| 0x01C6 4400 | FADDR | Function Address Register |
| 0x01C6 4401 | POWER | Power Management Register |
| 0x01C6 4402 | INTRTX | Interrupt Register for Endpoint 0 plus TX Endpoints 1 to 4 |
| 0x01C6 4404 | INTRRX | Interrupt Register for RX Endpoints 1 to 4 |
| 0x01C6 4406 | INTRTXE | Interrupt Enable Register for INTRTX |
| 0x01C6 4408 | INTRRXE | Interrupt Enable Register for INTRRX |
| 0x01C6 440A | INTRUSB | Interrupt Register for Common USB Interrupts |
| 0x01C6 440B | INTRUSBE | Interrupt Enable Register for INTRUSB |
| 0x01C6 440C | FRAME | Frame Number Register |
| 0x01C6 440E | INDEX | Index register for selecting the endpoint status and control registers |
| 0x01C6 440F | TESTMODE | Register to enable the USB 2.0 test modes |
| 0x01C6 4410 | TXMAXP | Maximum packet size for peripheral/host TX endpoint (Index register set to select Endpoints 1 - 4 only) |
| 0x01C6 4412 | PERI_CSR0 | Control Status register for Endpoint 0 in Peripheral mode. (Index register set to select Endpoint 0) |
| | HOST_CSR0 | Control Status register for Endpoint 0 in Host mode. (Index register set to select Endpoint 0) |
| | PERI_TXCSR | Control Status register for peripheral TX endpoint. (Index register set to select Endpoints 1 - 4) |
| | HOST_TXCSR | Control Status register for host TX endpoint. (Index register set to select Endpoints 1 - 4) |
| 0x01C6 4414 | RXMAXP | Maximum packet size for peripheral/host RX endpoint (Index register set to select Endpoints 1 - 4 only) |
| 0x01C6 4416 | PERI_RXCSR | Control Status register for peripheral RX endpoint. (Index register set to select Endpoints 1 - 4) |
| | HOST_RXCSR | Control Status register for host RX endpoint. (Index register set to select Endpoints 1 - 4) |

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**Table 7-86. USB2.0 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C6 4418 | COUNT0 | Number of received bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0) |
| | RXCOUNT | Number of bytes in host RX endpoint FIFO. (Index register set to select Endpoints 1 - 4) |
| 0x01C6 441A | HOST_TYPE0 | Defines the speed of Endpoint 0 |
| 0x01C6 441A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint. (Index register set to select Endpoints 1 - 4 only) |
| 0x01C6 441B | HOST_NAKLIMIT0 | Sets the NAK response timeout on Endpoint 0. (Index register set to select Endpoint 0) |
| 0x01C6 441B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint. (Index register set to select Endpoints 1 - 4 only) |
| 0x01C6 441C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint. (Index register set to select Endpoints 1 - 4 only) |
| 0x01C6 441D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint. (Index register set to select Endpoints 1 - 4 only) |
| 0x01C6 441F | CONFIGDATA | Returns details of core configuration (Index register set to select Endpoint 0) |
| 0x01C6 4420 | FIFO0 | TX and RX FIFO Register for Endpoint 0 |
| 0x01C6 4424 | FIFO1 | TX and RX FIFO Register for Endpoint 1 |
| 0x01C6 4428 | FIFO2 | TX and RX FIFO Register for Endpoint 2 |
| 0x01C6 442C | FIFO3 | TX and RX FIFO Register for Endpoint 3 |
| 0x01C6 4430 | FIFO4 | TX and RX FIFO Register for Endpoint 4 |
| 0x01C6 4460 | DEVCTL | Device Control Register |
| 0x01C6 4462 | TXFIFOSZ | TX Endpoint FIFO Size (Index register set to select Endpoints 0 - 4 only) |
| 0x01C6 4463 | RXFIFOSZ | RX Endpoint FIFO Size (Index register set to select Endpoints 0 - 4 only) |
| 0x01C6 4464 | TXFIFOADDR | TX Endpoint FIFO Address (Index register set to select Endpoints 0 - 4 only) |
| 0x01C6 4466 | RXFIFOADDR | RX Endpoint FIFO Address (Index register set to select Endpoints 0 - 4 only) |
| **Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG0** | | |
| 0x01C6 4480 | TXFUNCADDR | Address of the target function that has to be accessed through the associated TX Endpoint |
| 0x01C6 4482 | TXHUBADDR | Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 4483 | TXHUBPORT | Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 4484 | RXFUNCADDR | Address of the target function that has to be accessed through the associated RX Endpoint |
| 0x01C6 4486 | RXHUBADDR | Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 4487 | RXHUBPORT | Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high speed hub |
| **Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG1** | | |
| 0x01C6 4488 | TXFUNCADDR | Address of the target function that has to be accessed through the associated TX Endpoint |
| 0x01C6 448A | TXHUBADDR | Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 448B | TXHUBPORT | Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |


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**Table 7-86. USB2.0 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C6 448C | RXFUNCADDR | Address of the target function that has to be accessed through the associated RX Endpoint |
| 0x01C6 448E | RXHUBADDR | Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high speed hub |
| 0x01C6 448F | RXHUBPORT | Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| **Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG2** | | |
| 0x01C6 4490 | TXFUNCADDR | Address of the target function that has to be accessed through the associated TX Endpoint |
| 0x01C6 4492 | TXHUBADDR | Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 4493 | TXHUBPORT | Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 4494 | RXFUNCADDR | Address of the target function that has to be accessed through the associated RX Endpoint |
| 0x01C6 4496 | RXHUBADDR | Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 4497 | RXHUBPORT | Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| **Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG3** | | |
| 0x01C6 4498 | TXFUNCADDR | Address of the target function that has to be accessed through the associated TX Endpoint |
| 0x01C6 449A | TXHUBADDR | Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 449B | TXHUBPORT | Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full -peed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 449C | RXFUNCADDR | Address of the target function that has to be accessed through the associated RX Endpoint |
| 0x01C6 449E | RXHUBADDR | Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 449F | RXHUBPORT | Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| **Target Endpoint Control Registers (Valid Only in Host Mode) - EPTRG4** | | |
| 0x01C6 44A0 | TXFUNCADDR | Address of the target function that has to be accessed through the associated TX Endpoint |
| 0x01C6 44A2 | TXHUBADDR | Address of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 44A3 | TXHUBPORT | Port of the hub that has to be accessed through the associated TX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| 0x01C6 44A4 | RXFUNCADDR | Address of the target function that has to be accessed through the associated RX Endpoint |
| 0x01C6 44A6 | RXHUBADDR | Address of the hub that has to be accessed through the associated RX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |

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**Table 7-86. USB2.0 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C6 44A7 | RXHUBPORT | Port of the hub that has to be accessed through the associated RX Endpoint. This is used only when full-speed or low-speed device is connected via a USB2.0 high-speed hub. |
| **Control and Status Register for Endpoint 0 - EOCSR0** | | |
| 0x01C6 4502 | PERI_CSR0 | Control Status Register for Endpoint 0 in Peripheral mode |
| | HOST_CSR0 | Control Status Register for Endpoint 0 in Host mode |
| 0x01C6 4508 | COUNT0 | Number of Received Bytes in Endpoint 0 FIFO |
| 0x01C6 450A | HOST_TYPE0 | Defines the Speed of Endpoint 0 |
| 0x01C6 450B | HOST_NAKLIMIT0 | Sets the NAK response timeout on Endpoint 0. |
| 0x01C6 450F | CONFIGDATA | Returns details of core configuration |
| **Control and Status Register for Endpoint 1 - EOCSR1** | | |
| 0x01C6 4510 | TXMAXP | Maximum Packet size for Peripheral/Host TX Endpoint |
| 0x01C6 4512 | PERI_TXCSR | Control Status Register for Peripheral TX Endpoint |
| | HOST_TXCSR | Control Status Register for Host TX Endpoint |
| 0x01C6 4514 | RXMAXP | Maximum Packet Size for Peripheral/Host RX Endpoint |
| 0x01C6 4516 | PERI_RXCSR | Control Status Register for Peripheral RX Endpoint |
| | HOST_RXCSR | Control Status Register for Host RX Endpoint |
| 0x01C6 4518 | RXCOUNT | Number of Bytes in Host RX Endpoint FIFO |
| 0x01C6 451A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint. |
| 0x01C6 451B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint. |
| 0x01C6 451C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint. |
| 0x01C6 451D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint. |
| **Control and Status Register for Endpoint 2 - EOCSR2** | | |
| 0x01C6 4520 | TXMAXP | Maximum Packet Size for Peripheral/Host TX Endpoint |
| 0x01C6 4522 | PERI_TXCSR | Control Status Register for Peripheral TX Endpoint |
| | HOST_TXCSR | Control Status Register for Host TX Endpoint |
| 0x01C6 4524 | RXMAXP | Maximum Packet Size for Peripheral/Host RX Endpoint |
| 0x01C6 4526 | PERI_RXCSR | Control Status Register for Peripheral RX Endpoint |
| | HOST_RXCSR | Control Status Register for Host RX Endpoint |
| 0x01C6 4528 | RXCOUNT | Number of Bytes in Host RX Endpoint FIFO |
| 0x01C6 452A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint. |
| 0x01C6 452B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint. |
| 0x01C6 452C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint. |
| 0x01C6 452D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint. |
| **Control and Status Register for Endpoint 3 - EOCSR3** | | |
| 0x01C6 4530 | TXMAXP | Maximum Packet Size for Peripheral/Host TX Endpoint |
| 0x01C6 4532 | PERI_TXCSR | Control Status Register for Peripheral TX Endpoint |
| | HOST_TXCSR | Control Status Register for Host TX Endpoint |
| 0x01C6 4534 | RXMAXP | Maximum Packet Size for Peripheral/Host RX Endpoint |
| 0x01C6 4536 | PERI_RXCSR | Control Status Register for Peripheral RX Endpoint |
| | HOST_RXCSR | Control Status Register for Host RX Endpoint |
| 0x01C6 4538 | RXCOUNT | Number of Bytes in Host RX Endpoint FIFO |


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**Table 7-86. USB2.0 Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C6 453A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint. |
| 0x01C6 453B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint. |
| 0x01C6 453C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint. |
| 0x01C6 453D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint. |
| **Control and Status Register for Endpoint 4 - EOCSR4** | | |
| 0x01C6 4540 | TXMAXP | Maximum Packet Size for Peripheral/Host TX Endpoint |
| 0x01C6 4542 | PERI_TXCSR | Control Status Register for Peripheral TX Endpoint |
| | HOST_TXCSR | Control Status Register for Host TX Endpoint |
| 0x01C6 4544 | RXMAXP | Maximum Packet Size for Peripheral/Host RX Endpoint |
| 0x01C6 4546 | PERI_RXCSR | Control Status Register for Peripheral RX Endpoint |
| | HOST_RXCSR | Control Status Register for Host RX Endpoint |
| 0x01C6 4548 | RXCOUNT | Number of Bytes in Host RX Endpoint FIFO |
| 0x01C6 454A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host TX endpoint. |
| 0x01C6 454B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint. |
| 0x01C6 454C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host RX endpoint. |
| 0x01C6 454D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host RX endpoint. |

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### 7.19.4 USB2.0 Electrical Data/Timing

**Table 7-87. Switching Characteristics Over Recommended Operating Conditions for USB2.0 (see Figure 7-62)**

| NO. | PARAMETER | | -1G | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | LOW SPEED 1.5 Mbps | | FULL SPEED 12 Mbps | | HIGH SPEED 480 Mbps | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{r(D)}$ | Rise time, USB_DP and USB_DN signals(1) | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 2 | $t_{f(D)}$ | Fall time, USB_DP and USB_DN signals(1) | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 3 | $t_{rfM}$ | Rise/Fall time, matching(2) | 80 | 125 | 90 | 111.11 | – | – | % |
| 4 | $V_{CRS}$ | Output signal cross-over voltage(1) | 1.3 | 2 | 1.3 | 2 | – | – | V |
| 5 | $t_{jr(source)NT}$ | Source (Host) Driver jitter, next transition | | 2 | | 2 | | (3) | ns |
| | $t_{jr(FUNC)NT}$ | Function Driver jitter, next transition | | 25 | | 2 | | (3) | ns |
| 6 | $t_{jr(source)PT}$ | Source (Host) Driver jitter, paired transition(4) | | 1 | | 1 | | (3) | ns |
| | $t_{jr(FUNC)PT}$ | Function Driver jitter, paired transition | | 10 | | 1 | | (3) | ns |
| 7 | $t_{w(EOPT)}$ | Pulse duration, EOP transmitter | 1250 | 1500 | 160 | 175 | – | – | ns |
| 8 | $t_{w(EOPR)}$ | Pulse duration, EOP receiver | 670 | | 82 | | – | | ns |
| 9 | $t_{(DRATE)}$ | Data Rate | | 1.5 | | 12 | | 480 | Mb/s |
| 10 | $Z_{DRV}$ | Driver Output Resistance | – | – | 28 | 49.5 | 40.5 | 49.5 | Ω |
| 11 | USB_R1 | USB reference resistor | 9.9 | 10.1 | 9.9 | 10.1 | 9.9 | 10.1 | kΩ |

(1) Low Speed: $C_L$ = 200 pF, Full Speed: $C_L$ = 50 pF, High Speed: $C_L$ = 50 pF
(2) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(3) For more detailed information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7. Electrical.
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$

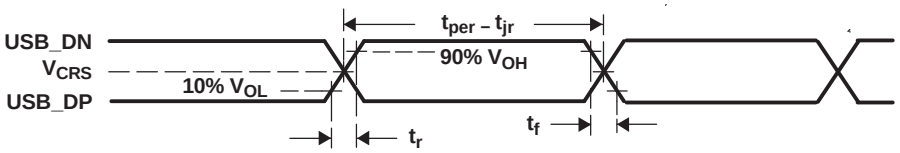
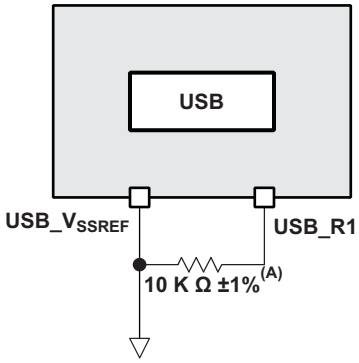



**Figure 7-62. USB2.0 Integrated Transceiver Interface Timing**




A. Place the 10 K Ω ± 1% as close to the device as possible.

**Figure 7-63. USB Reference Resistor Routing**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## 7.20 ATA Controller

The ATA peripheral supports the following features:

- PIO, multiword DMA, and Ultra ATA 33/66/100
- Up to mode 4 timings on PIO mode
- Up to mode 2 timings on multiword DMA
- Up to mode 5 timings on Ultra ATA
- Programmable timing parameters
- Supports TrueIDE mode for Compact Flash

### *7.20.1 ATA Bus Master Memory Map*

The ATA Controller supports multiword DMA transfers between external IDE/ATAPI devices and a system memory bus interface. Table 7-88 shows the memory map for the ATA DMA engine.

**Table 7-88. ATA DMA Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | ATA DMA ACCESS |
|---|---|---|---|
| 0x0000 0000 | 0x0FFF FFFF | 256M | Reserved |
| 0x1000 0000 | 0x1000 FFFF | 64K | Reserved |
| 0x1001 0000 | 0x1001 3FFF | 16K | ARM RAM 0 (Data) |
| 0x1001 4000 | 0x1001 7FFF | 16K | ARM RAM 1 (Data) |
| 0x1001 8000 | 0x1001 FFFF | 32K | ARM ROM (Data) |
| 0x1002 0000 | 0x10FF FFFF | 16256K | Reserved |
| 0x1100 0000 | 0x113F FFFF | 4M | |
| 0x1140 0000 | 0x114F FFFF | 1M | |
| 0x1150 0000 | 0x115F FFFF | 1M | |
| 0x1160 0000 | 0x116F FFFF | 1M | |
| 0x1170 0000 | 0x117F FFFF | 1M | |
| 0x1180 0000 | 0x1180 FFFF | 64K | |
| 0x1181 0000 | 0x1181 7FFF | 32K | |
| 0x1181 8000 | 0x1183 7FFF | 128K | C64x+ L2 RAM/Cache |
| 0x1183 8000 | 0x118F FFFF | 800K | Reserved |
| 0x1190 0000 | 0x11DF FFFF | 5M | |
| 0x11E0 0000 | 0x11E0 7FFF | 32K | C64x+ L1P RAM/Cache |
| 0x11E0 8000 | 0x11EF FFFF | 992K | Reserved |
| 0x11F0 0000 | 0x11F0 7FFF | 32K | C64x+ L1D RAM/Cache |
| 0x11F0 8000 | 0x11FF FFFF | 992K | Reserved |
| 0x1200 0000 | 0x4BFF FFFF | 928M | |
| 0x4C00 0000 | 0x4FFF FFFF | 64M | VLYNQ (Remote Data) |
| 0x5000 0000 | 0x7FFF FFFF | 768M | Reserved |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |

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### 7.20.2 ATA Peripheral Register Description(s)

Table 7-89 shows the ATA registers.

**Table 7-89. ATA Register Memory Map**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| **ATA Bus Master Interface DMA Engine Registers** | | |
| 0x01C6 6000 | BMICP | Primary IDE Channel DMA Control Register |
| 0x01C6 6002 | BMISP | Primary IDE Channel DMA Status Register |
| 0x01C6 6004 | BMIDTP | Primary IDE Channel DMA Descriptor Table Pointer Register |
| 0x01C6 6008 - 0x01C6 603F | – | Reserved |
| **ATA Configuration Registers** | | |
| 0x01C6 6040 | IDETIMP | Primary IDE Channel Timing Register |
| 0x01C6 6042 - 0x01C6 6046 | – | Reserved |
| 0x01C6 6047 | IDESTAT | IDE Controller Status Register |
| 0x01C6 6048 | UDMACTL | Ultra-DMA Control Register |
| 0x01C6 604A | – | Reserved |
| 0x01C6 6050 | MISCCTL | Miscellaneous Control Register |
| 0x01C6 6054 | REGSTB | Task File Register Strobe Timing Register |
| 0x01C6 6058 | REGRCVR | Task File Register Recovery Timing Register |
| 0x01C6 605C | DATSTB | Data Register Access PIO Strobe Timing Register |
| 0x01C6 6060 | DATRCVR | Data Register Access PIO Recovery Timing Register |
| 0x01C6 6064 | DMASTB | Multiword DMA Strobe Timing Register |
| 0x01C6 6068 | DMARCVR | Multiword DMA Recovery Timing Register |
| 0x01C6 606C | UDMASTB | Ultra-DMA Strobe Timing Register |
| 0x01C6 6070 | UDMATRP | Ultra-DMA Ready-to-Pause Timing Register |
| 0x01C6 6074 | UDMATENV | Ultra-DMA Timing Envelope Register |
| 0x01C6 6078 | IORDYTMP | Primary I/O Ready Timer Configuration Register |
| 0x01C6 607C - 0x01C6 67FF | – | Reserved |


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### 7.20.3 ATA Electrical Data/Timing

All ATA AC timing data described in Section 7.20.3.1 – Section 7.20.3.3 is provided at the DM6467T device pins. For more details, see Section 7.1, *Parameter Information*.

The AC timing specifications described in Section 7.20.3.1 – Section 7.20.3.3 assume correct configuration of the ATA memory-mapped control registers for the selected ATA frequency of operation.

#### 7.20.3.1 ATA PIO Data Transfer AC Timing

**Table 7-90. Timings for ATA Module — PIO Data Transfer(1) (2) (see Figure 7-64)**

| NO. | | | -1G | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MODE | MIN | MAX | |
| 1 | $t_0$ | Cycle time | 0-4(3) | (DATSTB + DATRCVR + 2)P -0.5 | | ns |
| 2 | $t_1$ | Address valid to $\overline{\text{DIOW}}$/$\overline{\text{DIOR}}$ setup | 0-4(3) | 12P - 1.6 | | ns |
| 3 | $t_2$ | $\overline{\text{DIOW}}$/$\overline{\text{DIOR}}$ pulse duration low | 0-4(3) | (DATSTB + 1)P - 1 | | ns |
| 4 | $t_{2i}$ | $\overline{\text{DIOW}}$/$\overline{\text{DIOR}}$ recovery time, pulse duration high | 0-2 | – | | ns |
| | | | 3-4(3) | (DATRCVR + 1)P - 1 | | ns |
| 5 | $t_3$ | $\overline{\text{DIOW}}$ data setup time, DD[15:0] valid before $\overline{\text{DIOW}}$ rising edge | 0-4(3) | (DATSTB + 1)P | | ns |
| 6 | $t_4$ | $\overline{\text{DIOW}}$ data hold time, DD[15:0] valid after $\overline{\text{DIOW}}$ rising edge | 0-4(3) | (HWNHLD + 1)P + 1 | | ns |
| 7 | $t_5$ | $\overline{\text{DIOR}}$ data setup time, DD[15:0] valid before $\overline{\text{DIOR}}$ rising edge | 0 | 50 | | ns |
| | | | 1 | 35 | | ns |
| | | | 2-4(3) | 20 | | ns |
| 8 | $t_6$ | $\overline{\text{DIOR}}$ data hold time, DD[15:0] valid after $\overline{\text{DIOR}}$ rising edge | 0-4(3) | 5 | | ns |
| 9 | $t_{6Z}$ | Output data 3-state, DD[15:0] 3-state after $\overline{\text{DIOR}}$ rising edge | 0-4(3) | | 30 | ns |
| 10 | $t_9$ | $\overline{\text{DIOW}}$/$\overline{\text{DIOR}}$ to address valid hold | 0-4(3) | (HWNHLD + 1)P - 2.1 | | ns |
| 11 | $t_{RD}$ | Read data setup time, DD[15:0] valid before IORDY active | 0-4(3) | 0 | | ns |
| 12 | $t_A$ | IORDY setup | 0-4(3) (4) | | 35 | ns |
| 13 | $t_B$ | IORDY pulse width | 0-4(3) | | 1250 | ns |
| 14 | $t_C$ | IORDY assertion to release | 0-4(3) | | 5 | ns |

(1) P = SYSCLK4 period, in ns, for ATA. For example, when running the DSP CPU at 1 GHz, use P = 7 ns.
(2) DATSTB equals the value programmed in the DATSTBxP bit field in the DATSTB register. DATRCVR equals the value programmed in the DATRCVRxP bit field in the DATRCVR register. HWNHLD equals the value programmed in the HWNHLDxP bit field in the MISCCTL register. For more detailed information, see the *TMS320DM646x DMSoC ATA Controller User's Guide* (literature number SPRUEQ3).
(3) The sustained throughput for PIO modes 3 and 4 is limited to the throughput equivalent of PIO mode 2. For more detailed information, see the *TMS320DM646x DMSoC ATA Controller User's Guide* (literature number SPRUEQ3).
(4) The $t_A$ parameter must be met only when the IORDY timer is enabled to allow a device to insert wait states during a transaction. In order to meet the $t_A$ parameter, a minimum frequency for SYSCLK4 is specified for each PIO as follows:
- PIO mode 0, MIN frequency = 15 MHz
- PIO mode 1, MIN frequency = 22 MHz
- PIO mode 2, MIN frequency = 31 MHz
- PIO mode 3, MIN frequency = 45 MHz
- PIO mode 4, MIN frequency = 57 MHz

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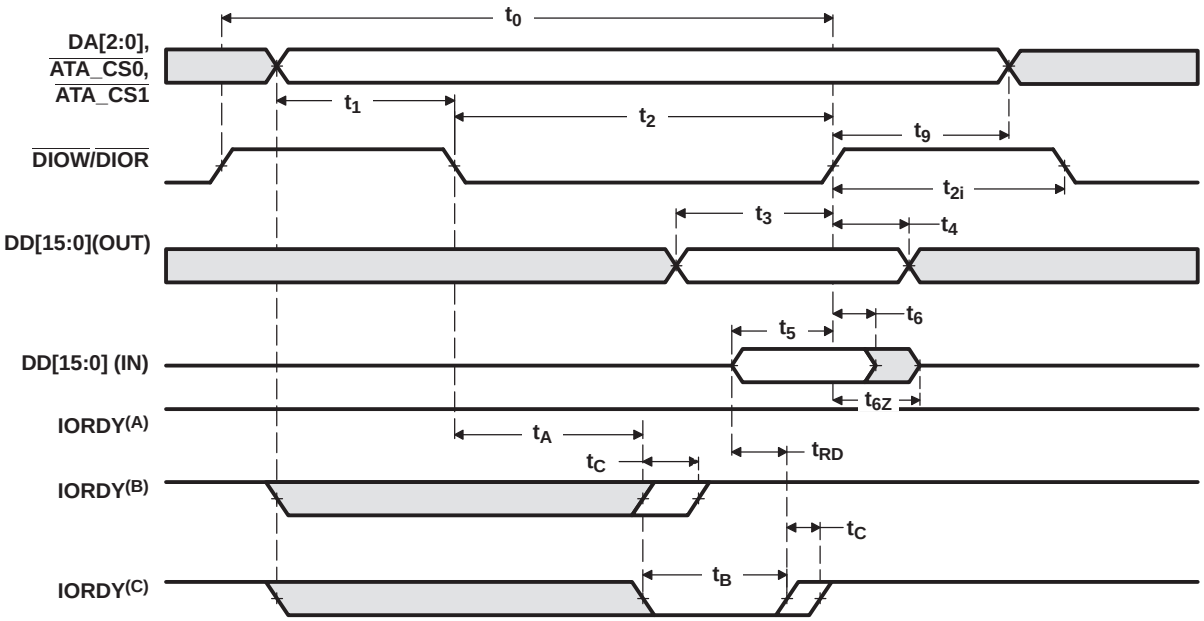


A. IORDY is not negated for transfer (no wait generated)
B. IORDY is negative but is re-asserted before $t_A$ (no wait is generated)
C. IORDY is negative before $t_A$ and remains asserted until $t_B$; data is driven valid at $t_{RD}$ (wait is generated)

**Figure 7-64. ATA PIO Data Transfer Timing**


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### 7.20.3.2 ATA Multiword DMA Timing

**Table 7-91. Timings for ATA Module — Multiword DMA AC Timing(1) (2) (see Figure 7-65)**

| NO. | | | -1G | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MODE | MIN | MAX | |
| 1 | $t_0$ | Cycle time | 0-2 | (DMASTB + DMARCVR + 2)P - 0.5 | | ns |
| 2 | $t_D$ | $\overline{DIOW}$/$\overline{DIOR}$ active low pulse duration | 0-2 | (DMASTB + 1)P - 1 | | ns |
| 3 | $t_E$ | $\overline{DIOR}$ data access, $\overline{DIOR}$ falling edge to DD[15:0] valid | 0 | | 150 | ns |
| | | | 1 | | 60 | ns |
| | | | 2 | | 50 | ns |
| 4 | $t_F$ | $\overline{DIOR}$ data hold time, DD[15:0] valid after $\overline{DIOR}$ rising edge | 0-2 | 5 | | ns |
| 5 | $t_G$ | $\overline{DIOW}$/$\overline{DIOR}$ data setup time, DD[15:0] (**OUT**) valid before $\overline{DIOW}$/$\overline{DIOR}$ rising edge | 0-2 | (DMASTB)P | | ns |
| | | $\overline{DIOW}$/$\overline{DIOR}$ data setup time, DD[15:0] (**IN**) valid before $\overline{DIOW}$/$\overline{DIOR}$ rising edge | 0 | 100 | | ns |
| | | | 1 | 30 | | ns |
| | | | 2 | 20 | | ns |
| 6 | $t_H$ | $\overline{DIOW}$ data hold time, DD[15:0] valid after $\overline{DIOW}$ rising edge | 0-2 | (HWNHLD + 1)P + 1 | | ns |
| 7 | $t_I$ | $\overline{DMACK}$ to $\overline{DIOW}$/$\overline{DIOR}$ setup | 0-2 | (DMARCVR + 1)P - 1.7 | | ns |
| 8 | $t_J$ | $\overline{DIOW}$/$\overline{DIOR}$ to $\overline{DMACK}$ hold | 0-2 | 5P - 5.9 | | ns |
| 9 | $t_{KR}$ | $\overline{DIOR}$ negated pulse width | 0-2 | (DMARCVR + 1)P - 1 | | ns |
| 10 | $t_{KW}$ | $\overline{DIOW}$ negated pulse width | 0-2 | (DMARCVR + 1)P - 1 | | ns |
| 11 | $t_{LR}$ | $\overline{DIOR}$ to DMARQ delay | 0 | | 120 | ns |
| | | | 1 | | 45 | ns |
| | | | 2 | | 35 | ns |
| 12 | $t_{LW}$ | $\overline{DIOW}$ to DMARQ delay | 0-1 | | 40 | ns |
| | | | 2 | | 35 | ns |
| 13 | $t_M$ | $\overline{ATA_CSx}$ valid to $\overline{DIOW}$/$\overline{DIOR}$ setup | 0-2 | (DATRCVR)P - 1.7 | | ns |
| 14 | $t_N$ | $\overline{ATA_CSx}$ valid after $\overline{DIOW}$/$\overline{DIOR}$ rising edge hold | 0-2 | 5P - 1.7 | | ns |
| 15 | $t_Z$ | $\overline{DMACK}$ to read data (DD[15:0]) released | 0 | | 20 | ns |
| | | | 1-2 | | 25 | ns |

(1) P = SYSCLK4 period, in ns, for ATA. For example, when running the DSP CPU at 1 GHz, use P = 7 ns.
(2) DMASTB equals the value programmed in the DMASTBxP bit field in the DMASTB register. DMARCVR equals the value programmed in the DMARCVRxP bit field in the DMARCVR register. HWNHLD equals the value programmed in the HWNHLDxP bit field in the MISCCTL register. For more detailed information, see the *TMS320DM646x DMSoC ATA Controller User's Guide* (literature number SPRUEQ3).

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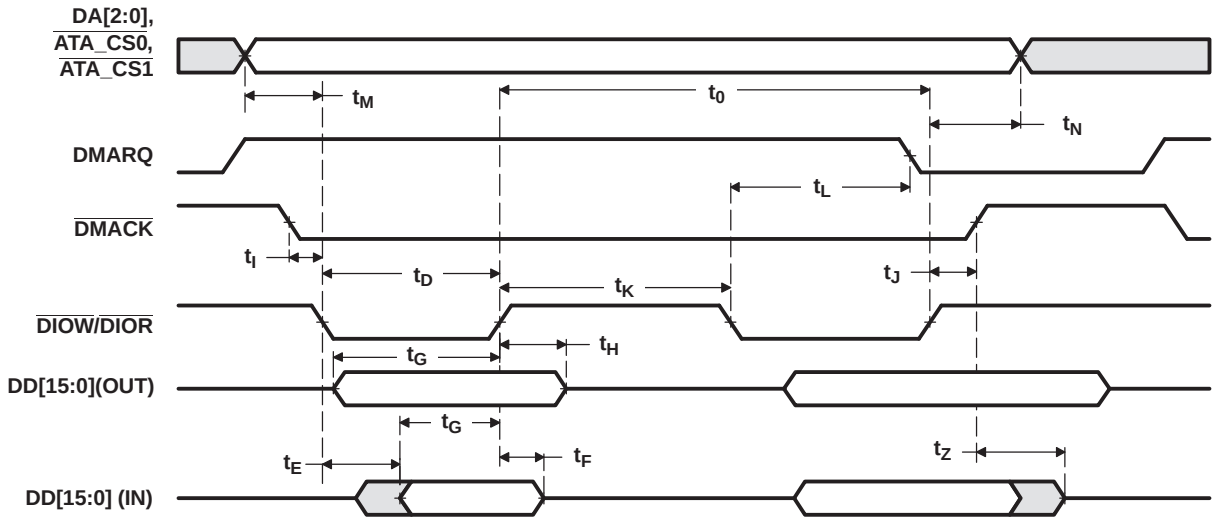


**Figure 7-65. ATA Multiword DMA Timing**


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### 7.20.3.3 ATA Ultra DMA Timing

**Table 7-92. Timings for ATA Module — Ultra DMA AC Timing(1) (2) (see Figure 7-66 through Figure 7-75)**

| NO. | | | -1G | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MODE | MIN | MAX | |
| 28 | $f_{(SYSCLK4)}$ | Operating frequency, SYSCLK4 | 0-5 | 25 | | MHz |
| 1 | $t_{2CYCTYP}$ | Typical sustained average two cycle time | 0 | 240 | | ns |
| | | | 1 | 160 | | ns |
| | | | 2 | 120 | | ns |
| | | | 3 | 90 | | ns |
| | | | 4 | 60 | | ns |
| | | | 5 | 40 | | ns |
| 2 | $t_{CYC}$ | Cycle time, Strobe edge to Strobe edge | 0-5 | (UDMASTB + 1)P | | ns |
| 3 | $t_{2CYC}$ | Two cycle time, rising to rising edge or falling to falling edge | 0-5 | 2(UDMASTB + 1)P | | ns |
| 4 | $t_{DS}$ | Data setup, data valid before STROBE edge | 0 | 15 | | ns |
| | | | 1 | 10 | | ns |
| | | | 2-3 | 7 | | ns |
| | | | 4 | 5 | | ns |
| | | | 5 | 4 | | ns |
| 5 | $t_{DH}$ | Data hold, data valid after STROBE edge | 0-4 | 5 | | ns |
| | | | 5 | 4.6 | | ns |
| 6 | $t_{DVS}$ | Data valid **INPUT** setup time, data valid before STROBE | 0 | 70 | | ns |
| | | | 1 | 48 | | ns |
| | | | 2 | 31 | | ns |
| | | | 3 | 20 | | ns |
| | | | 4 | 6.7 | | ns |
| | | | 5 | 4.8 | | ns |
| | | Data valid **OUTPUT** setup time, data valid before STROBE | 0-5 | (UDMASTB)P - 3.1 | | ns |
| 7 | $t_{DVH}$ | Data valid **INPUT** hold time, data valid after STROBE | 0-4 | 6.2 | | ns |
| | | | 5 | 4.8 | | ns |
| | | Data valid **OUTPUT** hold time, data valid after STROBE | 0-5 | 1P - 2 | | ns |
| 10 | $t_{CVS}$ | CRC word valid setup time at host, CRC valid before $\overline{DMACK}$ negation | 0-5 | P | | ns |
| 11 | $t_{CVH}$ | CRC word valid hold time at sender, CRC valid after $\overline{DMACK}$ negation | 0-5 | 2P | | ns |
| 12 | $t_{ZFS}$ | Time from STROBE output released-to-driving until the first transition of critical timing | 0-4 | 0 | | ns |
| | | | 5 | 35 | | ns |
| 13 | $t_{DZFS}$ | Time from data output released-to-driving until the first transition of critical timing | 0 | 70 | | ns |
| | | | 1 | 48 | | ns |
| | | | 2 | 31 | | ns |
| | | | 3 | 20 | | ns |
| | | | 4 | 6.7 | | ns |
| | | | 5 | 25 | | ns |

(1) P = SYSCLK4 period, in ns, for ATA. For example, when running the DSP CPU at 1 GHz, use P = 7 ns.
(2) UDMASTB equals the value programmed in the UDMSTBxP bit field in the UDMASTB register. UDMATRP equals the value programmed in the UDMTRPxP bit field in the UDMATRP register. TENV equals the value programmed in the UDMATNVxP bit field in the UDMATENV register. For more detailed information, see the *TMS320DM646x DMSoC ATA Controller User's Guide* (literature number SPRUEQ3).

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**Table 7-92. Timings for ATA Module — Ultra DMA AC Timing[1] [2] (see Figure 7-66 through Figure 7-75) (continued)**

| NO. | | | -1G | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MODE | MIN | MAX | |
| 14 | $t_{FS}$ | First STROBE time | 0 | | 230 | ns |
| | | | 1 | | 200 | ns |
| | | | 2 | | 170 | ns |
| | | | 3 | | 130 | ns |
| | | | 4 | | 120 | ns |
| | | | 5 | | 90 | ns |
| 15 | $t_{LI}$ | Limited interlock time | 0-2 | 0 | 150 | ns |
| | | | 3-4 | 0 | 100 | ns |
| | | | 5 | 0 | 75 | ns |
| 16 | $t_{MLI}$ | Interlock time with minimum | 0-5 | 20 | | ns |
| 17 | $t_{UI}$ | Unlimited interlock time | 0-5 | 0 | | ns |
| 18 | $t_{AZ}$ | Maximum time allowed for output drivers to release | 0-5 | | 10 | ns |
| 19 | $t_{ZAH}$ | Minimum delay time required for output | 0-5 | 20 | | ns |
| 20 | $t_{ZAD}$ | Minimum delay time for driver to assert or negate (from released) | 0-5 | 0 | | ns |
| 21 | $t_{ENV}$ | Envelope time, $\overline{\text{DMACK}}$ to STOP and $\overline{\text{DMACK}}$ to HDMARDY during in-burst initiation and from $\overline{\text{DMACK}}$ to STOP during data out burst initiation | 0-5 | (TENV + 1)P - 0.5 | (TENV + 1)P + 1.4 | ns |
| 22 | $t_{RFS}$ | Ready-to-final-STROBE time | 0 | | 75 | ns |
| | | | 1 | | 70 | ns |
| | | | 2-4 | | 60 | ns |
| | | | 5 | | 50 | ns |
| 23 | $t_{RP}$ | Ready to pause time, **(HDMARDY ($\overline{\text{DIOR}}$) to STOP ($\overline{\text{DIOW}}$))** | 0-5 | (UDMATRP + 1)P - 0.8 | | ns |
| | | Ready to pause time, **(DDMARDY (IORDY) to DMARQ)** | 0 | 160 | | ns |
| | | | 1 | 125 | | ns |
| | | | 2-4 | 100 | | ns |
| | | | 5 | 85 | | ns |
| 24 | $t_{IORDYZ}$ | Maximum time before releasing IORDY | 0-5 | | 20 | ns |
| 25 | $t_{ZIORDY}$ | Minimum time before driving IORDY | 0-5 | 0 | | ns |
| 26 | $t_{ACK}$ | Setup and hold time for $\overline{\text{DMACK}}$ (before assertion or negation) | 0-5 | 20 | | ns |
| 27 | $t_{SS}$ | STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst) | 0-5 | 50 | | ns |


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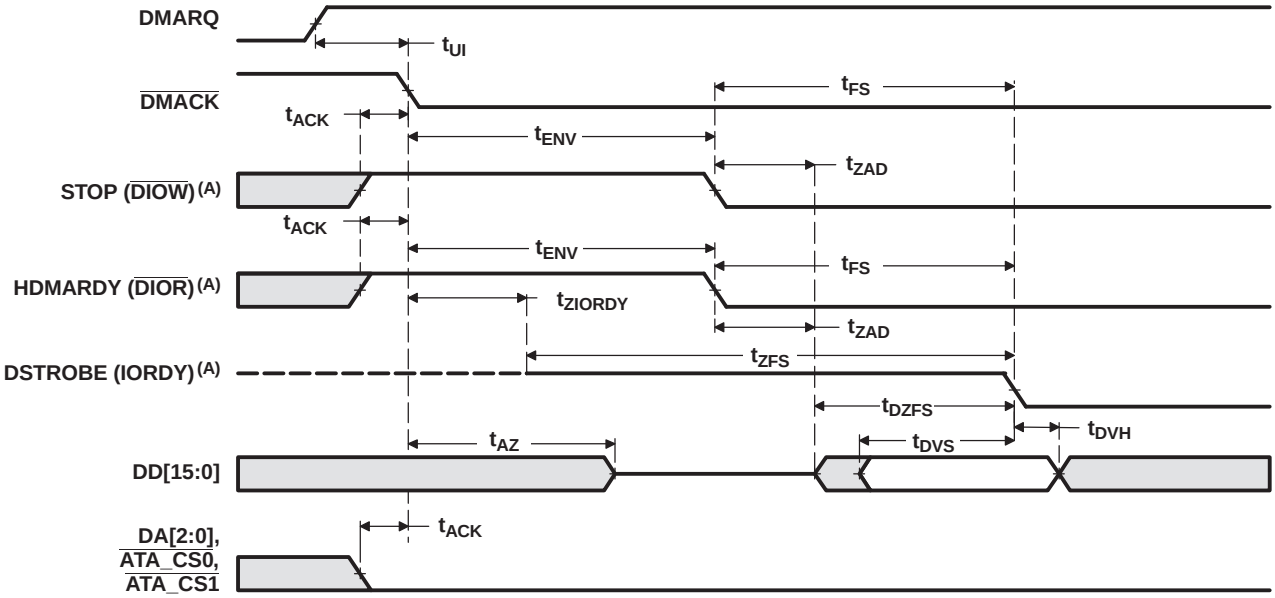
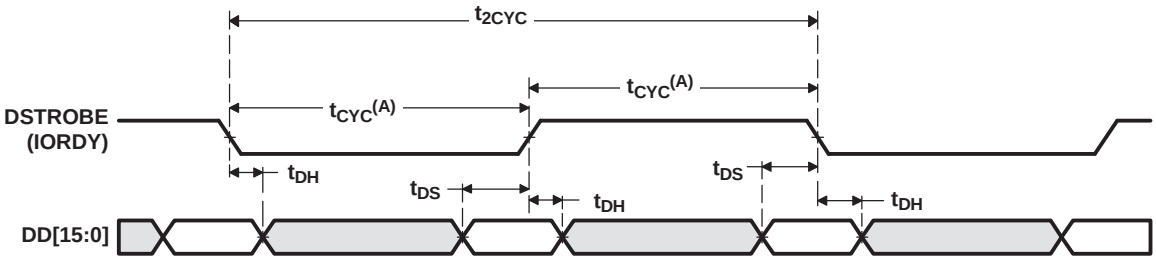



A. The definitions for the DIOW:STOP, DIOR:HDMARDY, and IORDY:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

**Figure 7-66. ATA Initiating an Ultra DMA Data-In Burst Timing**




A. While DSTROBE (IORDY) timing is $t_{CYC}$ at the device, it may be different at the host due to propagation delay differences on the cable.

**Figure 7-67. ATA Sustained Ultra DMA Data-In Data Transfer Timing**

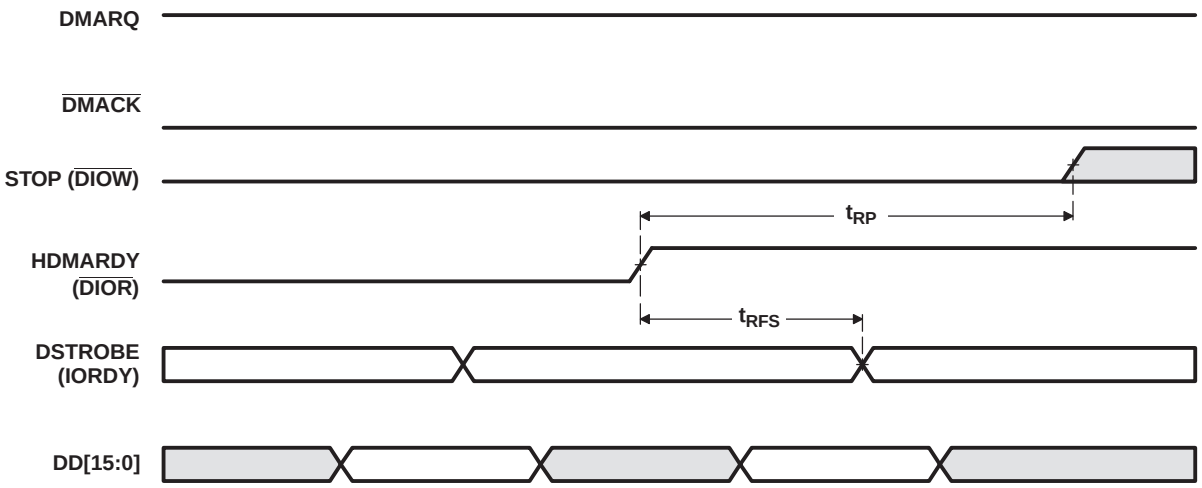



**Figure 7-68. ATA Host Pausing an Ultra DMA Data-In Burst Timing**

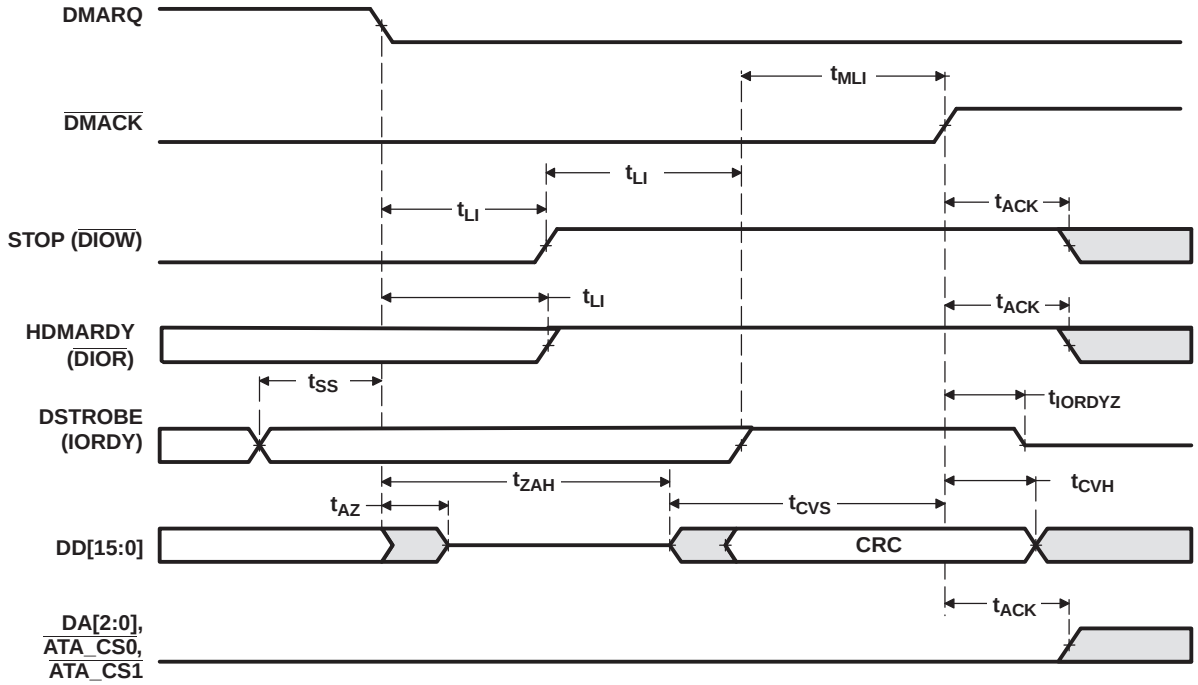



**Figure 7-69. ATA Device Terminating an Ultra DMA Data-In Burst Timing**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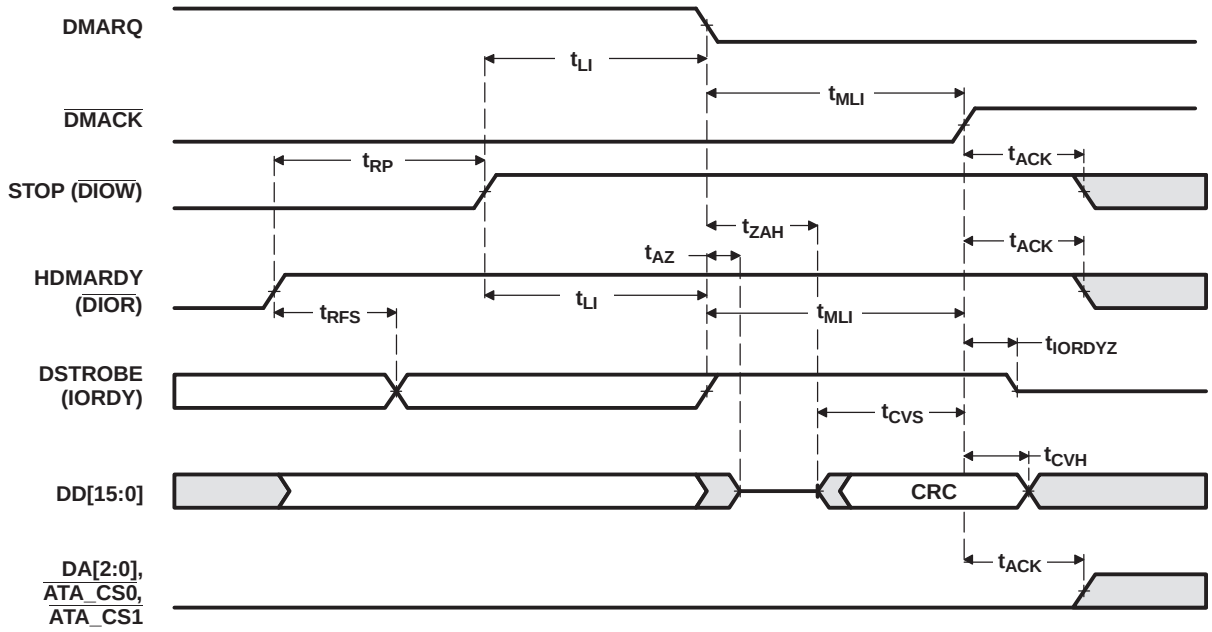
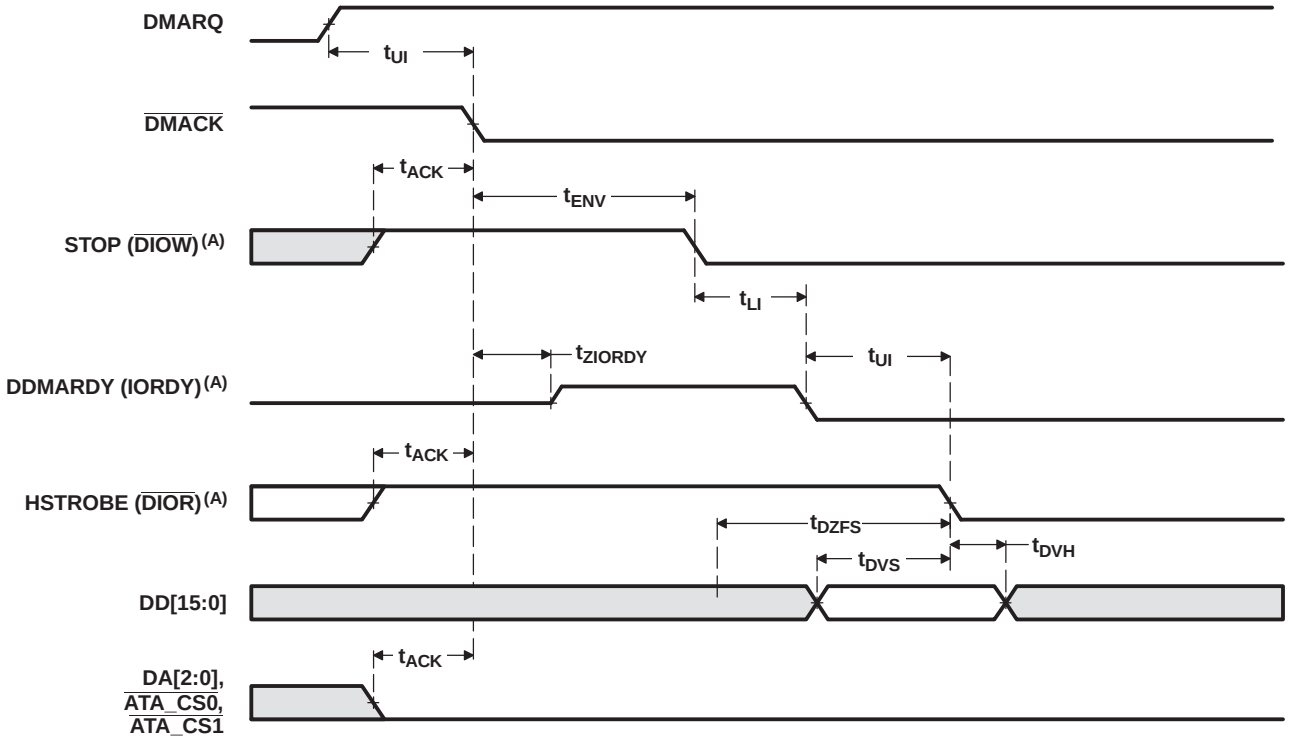
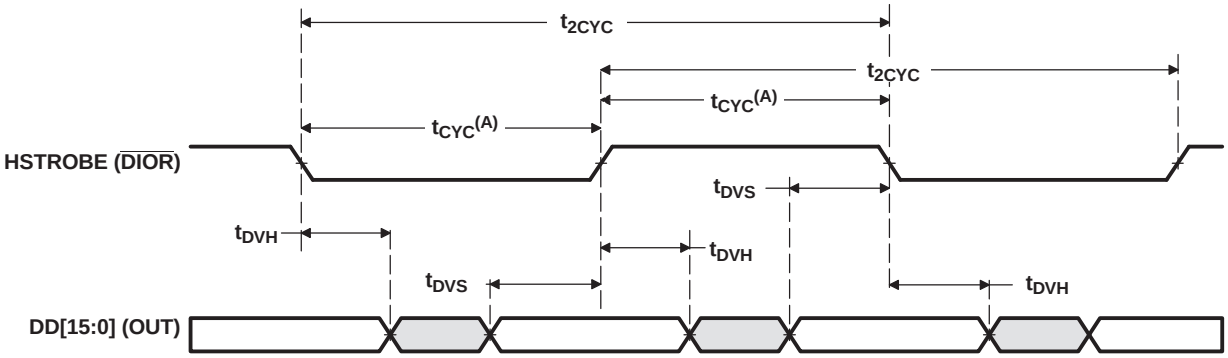



**Figure 7-70. ATA Host Terminating an Ultra DMA Data-In Burst Timing**




A. The definitions for the DIOW:STOP, IORDY:DDMARDY, and DIOR:HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

**Figure 7-71. ATA Initiating an Ultra DMA Data-Out Burst Timing**




A. While HSTROBE (DIOR) timing is $t_{CYC}$ at the host, it may be different at the device due to propagation delay differences on the cable.

**Figure 7-72. ATA Sustained Ultra DMA Data-Out Transfer Timing**

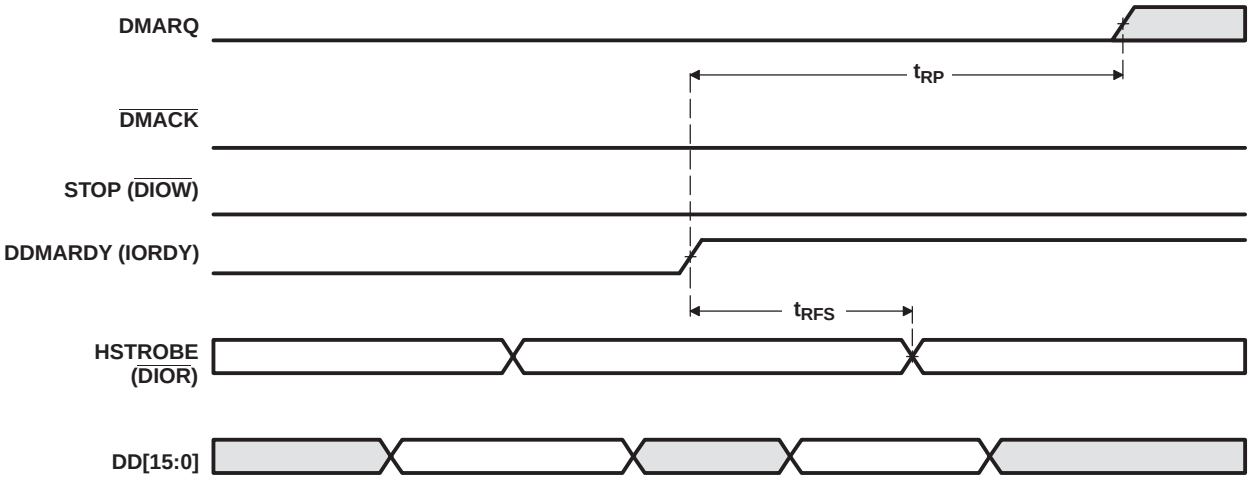



**Figure 7-73. ATA Device Pausing an Ultra DMA Data-Out Burst Timing**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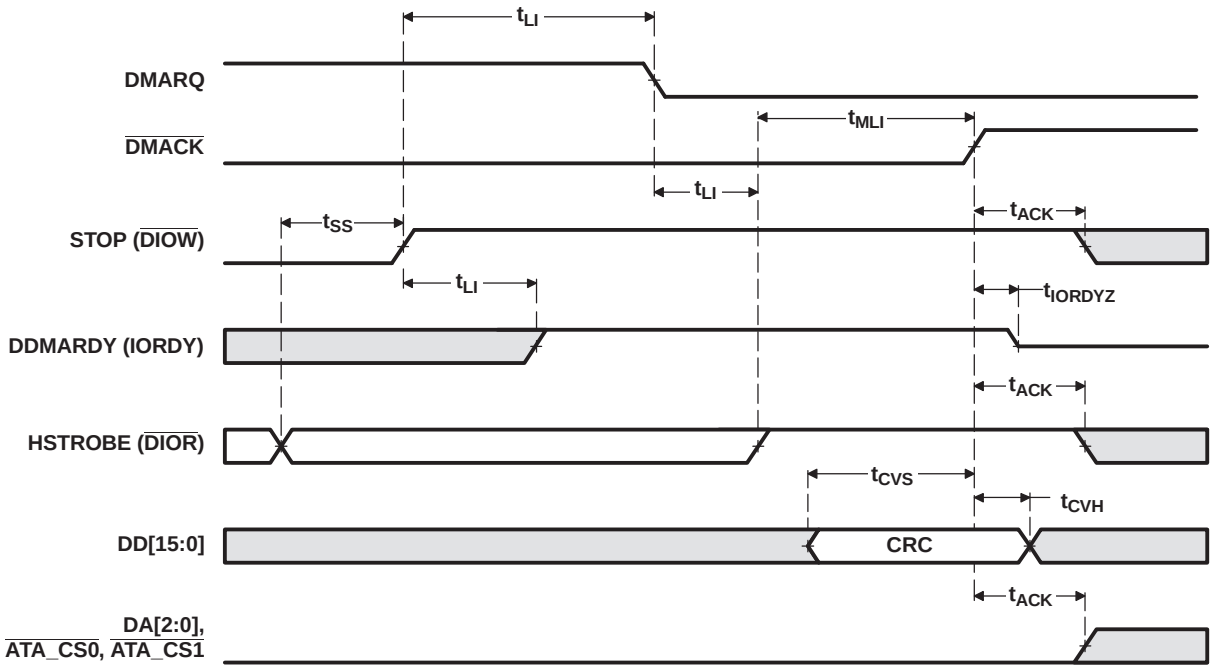



**Figure 7-74. ATA Host Terminating an Ultra DMA Data-Out Burst Timing**

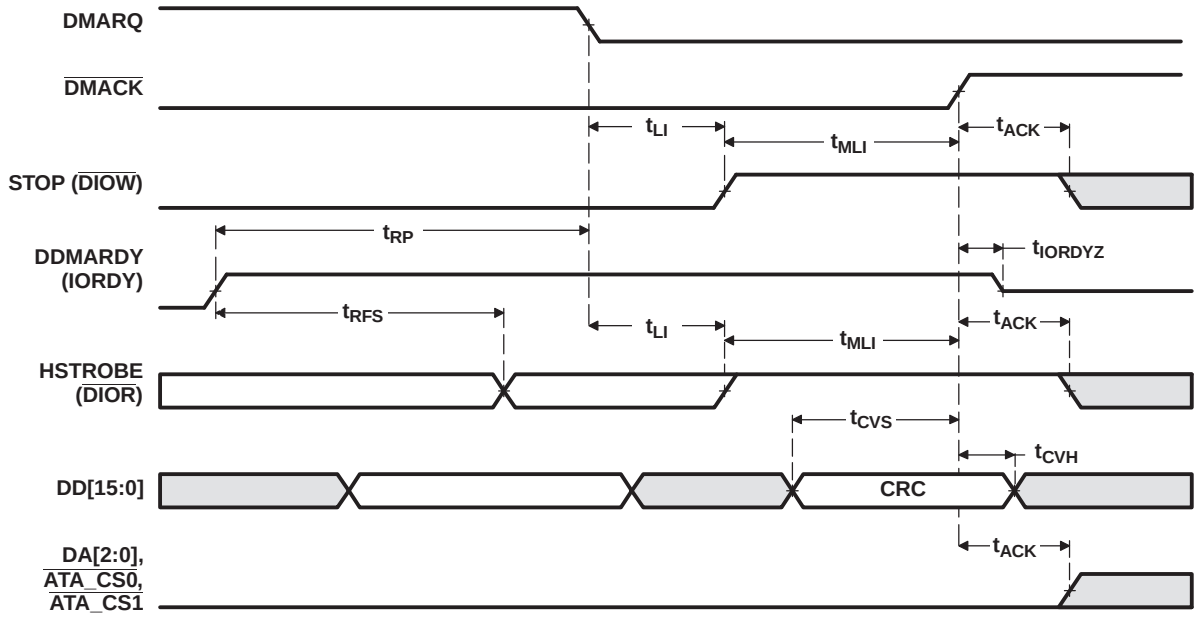



**Figure 7-75. ATA Device Terminating an Ultra DMA Data-Out Burst Timing**

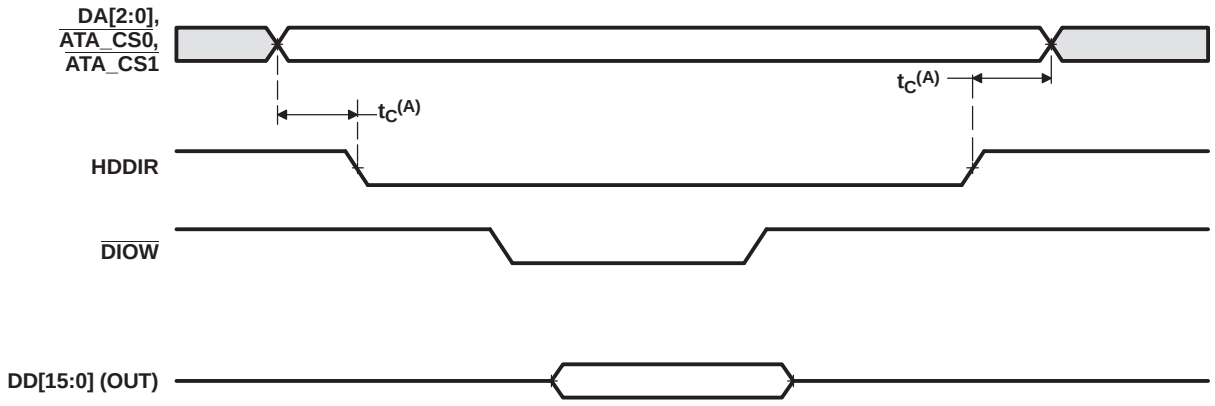
### 7.20.3.4 ATA HDDIR Timing

Figure 7-76 through Figure 7-79 show the behavior of HDDIR for the different types of transfers.

**Table 7-93. Timing Requirements for HDDIR(1)**

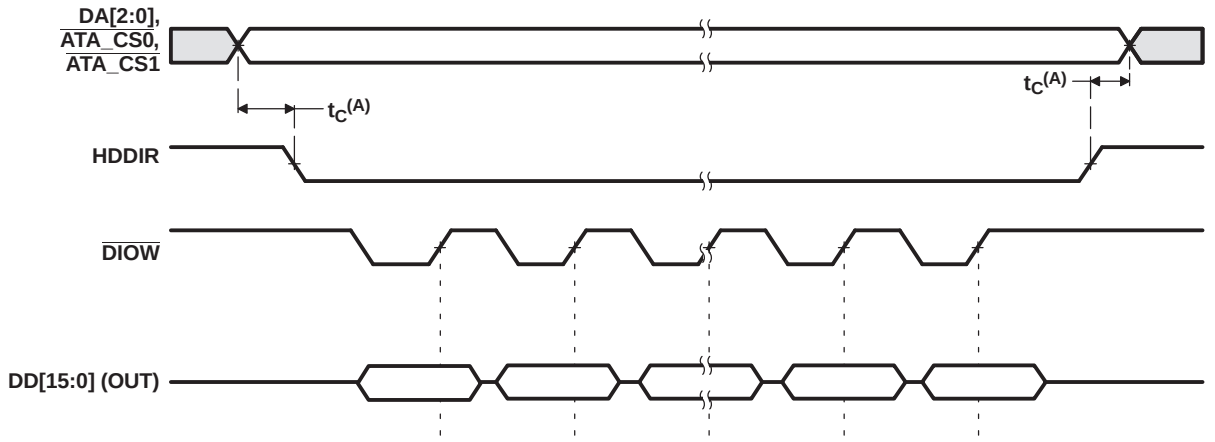
| NO. | | -1G | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| 1 | $t_c$ Cycle time, $\overline{ATA_CS[1:0]}$ to HDDIR low | E - 3.1 | | ns |

(1) E = ATA clock cycle




A. $t_C \geq$ one cycle

**Figure 7-76. ATA HDDIR Taskfile Write/Single PIO Write Timing**




A. $t_C \geq$ one cycle

**Figure 7-77. ATA HDDIR PIO Postwrite Start Timing**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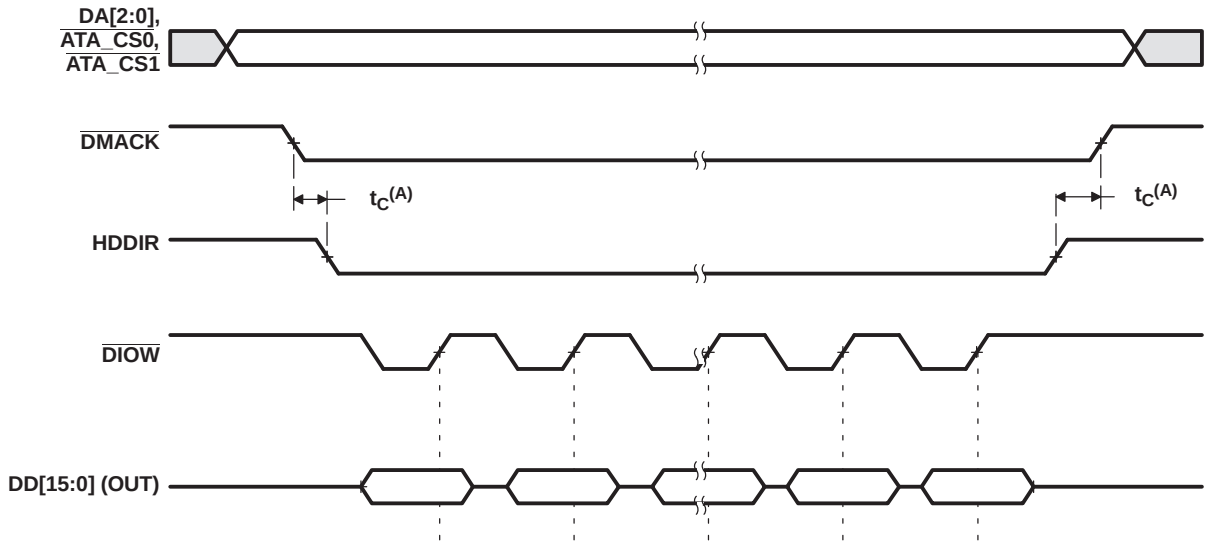
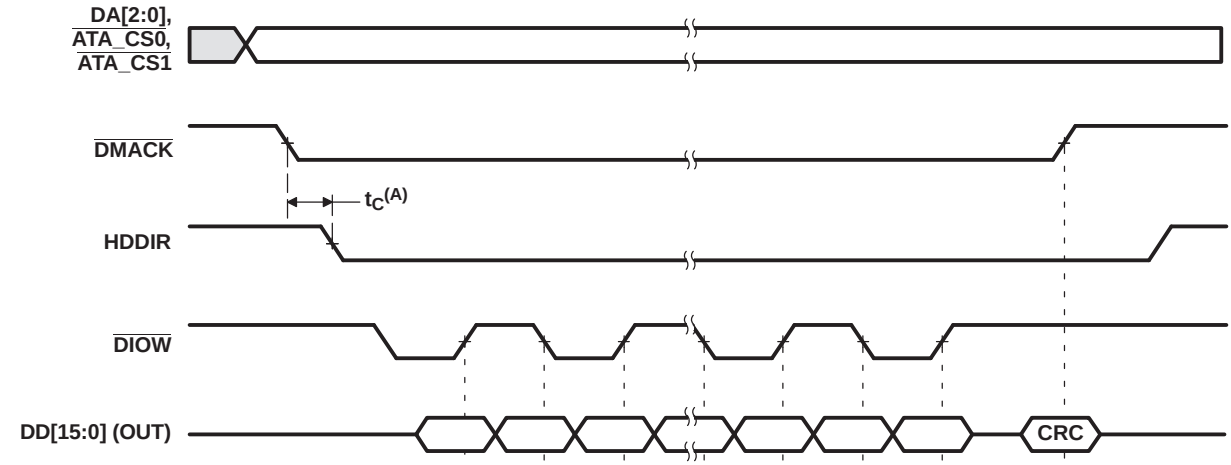



A. $t_C \geq$ one cycle

**Figure 7-78. ATA HDDIR Multiword DMA Write Transfer Timing**




A. $t_C \geq$ one cycle

**Figure 7-79. ATA HDDIR Ultra DMA Write Transfer Timing**

## 7.21 VLYNQ

The DM6467T VLYNQ peripheral provides a high speed serial communications interface with the following features.

- Low Pin Count
- Scalable Performance/Support
- Simple Packet Based Transfer Protocol for Memory Mapped Access
  - Write Request/Data Packet
  - Read Request Packet
  - Read Response Data Packet
  - Interrupt Request Packet
- Supports both Symmetric and Asymmetric Operation
  - Tx pins on first device connect to Rx pins on second device and vice versa
  - Data pin widths are automatically detected after reset
  - Request packets, response packets, and flow control information are all multiplexed and sent across the same physical pins
  - Supports both Host/Peripheral and Peer-to-Peer communication
- Simple Block Code Packet Formatting (8-bit/10-bit)
- In Band Flow Control
  - No extra pins needed
  - Allows receiver to momentarily throttle back transmitter when overflow is about to occur
  - Uses built in special code capability of block code to seamlessly interleave flow control information with user data
  - Allows system designer to balance cost of data buffering versus performance
- Multiple outstanding transactions
- Automatic packet formatting optimizations
- Internal loop-back mode

### *7.21.1 VLYNQ Bus Master Memory Map*

The VLYNQ peripheral includes a bus master interface that allows external device initiated transfers to access the DM6467T system bus. Table 7-94 shows the memory map for the VLYNQ master interface.

**Table 7-94. VLYNQ Master Memory Map**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | HPI ACCESS |
|---|---|---|---|
| 0x0000 0000 | 0x01BF FFFF | 28M | Reserved |
| 0x01C0 0000 | 0x0FFF FFFF | 228M | CFG Bus Peripherals |
| 0x1000 0000 | 0x1000 FFFF | 64K | Reserved |
| 0x1001 0000 | 0x1001 3FFF | 16K | ARM RAM 0 (Data) |
| 0x1001 4000 | 0x1001 7FFF | 16K | ARM RAM 1 (Data) |
| 0x1001 8000 | 0x1001 FFFF | 32K | ARM ROM (Data) |


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**Table 7-94. VLYNQ Master Memory Map (continued)**

| START ADDRESS | END ADDRESS | SIZE (BYTES) | HPI ACCESS |
|---|---|---|---|
| 0x1002 0000 | 0x10FF FFFF | 16256K | Reserved |
| 0x1100 0000 | 0x113F FFFF | 4M | |
| 0x1140 0000 | 0x114F FFFF | 1M | |
| 0x1150 0000 | 0x115F FFFF | 1M | |
| 0x1160 0000 | 0x116F FFFF | 1M | |
| 0x1170 0000 | 0x117F FFFF | 1M | |
| 0x1180 0000 | 0x1180 FFFF | 64K | |
| 0x1181 0000 | 0x1181 7FFF | 32K | |
| 0x1181 8000 | 0x1183 7FFF | 128K | C64x+ L2 RAM/Cache |
| 0x1183 8000 | 0x118F FFFF | 800K | Reserved |
| 0x1190 0000 | 0x11DF FFFF | 5M | |
| 0x11E0 0000 | 0x11E0 7FFF | 32K | C64x+ L1P RAM/Cache |
| 0x11E0 8000 | 0x11EF FFFF | 992K | Reserved |
| 0x11F0 0000 | 0x11F0 7FFF | 32K | C64x+ L1D RAM/Cache |
| 0x11F0 8000 | 0x11FF FFFF | 992K | Reserved |
| 0x1200 0000 | 0x41FF FFFF | 768M | |
| 0x4200 0000 | 0x43FF FFFF | 32M | EMIFA Data ($\overline{CS2}$) |
| 0x4400 0000 | 0x45FF FFFF | 32M | EMIFA Data ($\overline{CS3}$) |
| 0x4600 0000 | 0x47FF FFFF | 32M | EMIFA Data ($\overline{CS4}$) |
| 0x4800 0000 | 0x49FF FFFF | 32M | EMIFA Data ($\overline{CS5}$) |
| 0x4A00 0000 | 0x7FFF FFFF | 864M | Reserved |
| 0x8000 0000 | 0x9FFF FFFF | 512M | DDR2 Memory Controller |
| 0xA000 0000 | 0xBFFF FFFF | 512M | Reserved |
| 0xC000 0000 | 0xFFFF FFFF | 1G | Reserved |

### 7.21.2 VLYNQ Peripheral Register Description(s)

**Table 7-95. VLYNQ Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x2001 0000 | REVID | VLYNQ Revision Register |
| 0x2001 0004 | CTRL | VLYNQ Local Control Register |
| 0x2001 0008 | STAT | VLYNQ Local Status Register |
| 0x2001 000C | INTPRI | VLYNQ Local Interrupt Priority Vector Status/Clear Register |
| 0x2001 0010 | INTSTATCLR | VLYNQ Local Unmasked Interrupt Status/Clear Register |
| 0x2001 0014 | INTPENDSET | VLYNQ Local Interrupt Pending/Set Register |
| 0x2001 0018 | INTPTR | VLYNQ Local Interrupt Pointer Register |
| 0x2001 001C | XAM | VLYNQ Local Transmit Address Map Register |
| 0x2001 0020 | RAMS1 | VLYNQ Local Receive Address Map Size 1 Register |
| 0x2001 0024 | RAMO1 | VLYNQ Local Receive Address Map Offset 1 Register |
| 0x2001 0028 | RAMS2 | VLYNQ Local Receive Address Map Size 2 Register |
| 0x2001 002C | RAMO2 | VLYNQ Local Receive Address Map Offset 2 Register |
| 0x2001 0030 | RAMS3 | VLYNQ Local Receive Address Map Size 3 Register |
| 0x2001 0034 | RAMO3 | VLYNQ Local Receive Address Map Offset 3 Register |
| 0x2001 0038 | RAMS4 | VLYNQ Local Receive Address Map Size 4 Register |
| 0x2001 003C | RAMO4 | VLYNQ Local Receive Address Map Offset 4 Register |
| 0x2001 0040 | CHIPVER | VLYNQ Local Chip Version Register |

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**Table 7-95. VLYNQ Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x2001 0044 | AUTNGO | VLYNQ Local Auto Negotiation Register |
| 0x2001 0048 | – | Reserved |
| 0x2001 004C | – | Reserved |
| 0x2001 0050 - 0x2001 005C | – | Reserved |
| 0x2001 0060 | – | Reserved |
| 0x2001 0064 | – | Reserved |
| 0x2001 0068 - 0x2001 007C | – | Reserved *for future use* |
| 0x2001 0080 | RREVID | VLYNQ Remote Revision Register |
| 0x2001 0084 | RCTRL | VLYNQ Remote Control Register |
| 0x2001 0088 | RSTAT | VLYNQ Remote Status Register |
| 0x2001 008C | RINTPRI | VLYNQ Remote Interrupt Priority Vector Status/Clear Register |
| 0x2001 0090 | RINTSTATCLR | VLYNQ Remote Unmasked Interrupt Status/Clear Register |
| 0x2001 0094 | RINTPENDSET | VLYNQ Remote Interrupt Pending/Set Register |
| 0x2001 0098 | RINTPTR | VLYNQ Remote Interrupt Pointer Register |
| 0x2001 009C | RXAM | VLYNQ Remote Transmit Address Map Register |
| 0x2001 00A0 | RRAMS1 | VLYNQ Remote Receive Address Map Size 1 Register |
| 0x2001 00A4 | RRAMO1 | VLYNQ Remote Receive Address Map Offset 1 Register |
| 0x2001 00A8 | RRAMS2 | VLYNQ Remote Receive Address Map Size 2 Register |
| 0x2001 00AC | RRAMO2 | VLYNQ Remote Receive Address Map Offset 2 Register |
| 0x2001 00B0 | RRAMS3 | VLYNQ Remote Receive Address Map Size 3 Register |
| 0x2001 00B4 | RRAMO3 | VLYNQ Remote Receive Address Map Offset 3 Register |
| 0x2001 00B8 | RRAMS4 | VLYNQ Remote Receive Address Map Size 4 Register |
| 0x2001 00BC | RRAMO4 | VLYNQ Remote Receive Address Map Offset 4 Register |
| 0x2001 00C0 | RCHIPVER | VLYNQ Remote Chip Version Register (values on the device_id and device_rev pins of remote VLYNQ) |
| 0x2001 00C4 | RAUTNGO | VLYNQ Remote Auto Negotiation Register |
| 0x2001 00C8 | RMANNGO | VLYNQ Remote Manual Negotiation Register |
| 0x2001 00CC | RNGOSTAT | VLYNQ Remote Negotiation Status Register |
| 0x2001 00D0 - 0x2001 00DC | – | Reserved |
| 0x2001 00E0 | RINTVEC0 | VLYNQ Remote Interrupt Vectors 3 - 0 (sourced from vlynq_int_i[3:0] port of remote VLYNQ) |
| 0x2001 00E4 | RINTVEC1 | VLYNQ Remote Interrupt Vectors 7 - 4 (sourced from vlynq_int_i[7:4] port of remote VLYNQ) |
| 0x2001 00E8 - 0x2001 00FC | – | Reserved *for future use* |
| 0x2001 0100 - 0x2001 0FFF | – | Reserved |
| **VLYNQ Remote Devices** | | |
| 0x4C00 0000 - 0x4FFF FFFF | VLYNQREMOTE | 64 MB Remote Data Region. Translated into one of four mapped registers on the remote device. |


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### 7.21.3 VLYNQ Electrical Data/Timing

**Table 7-96. Timing Requirements for VLYNQ_CLOCK Input (see Figure 7-80)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(VCLK)}$ | Cycle time, VLYNQ_CLOCK | 9.6 | | ns |
| 2 | $t_{w(VCLKH)}$ | Pulse duration, VLYNQ_CLOCK high | 3 | | ns |
| 3 | $t_{w(VCLKL)}$ | Pulse duration, VLYNQ_CLK low | 3 | | ns |
| 4 | $t_{t(VCLK)}$ | Transition time, VLYNQ_CLOCK | | 3 | ns |

**Table 7-97. Switching Characteristics Over Recommended Operating Conditions for VLYNQ_CLOCK Output (see Figure 7-80)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(VCLK)}$ | Cycle time, VLYNQ_CLOCK | 9.6 | | ns |
| 2 | $t_{w(VCLKH)}$ | Pulse duration, VLYNQ_CLOCK high | 4 | | ns |
| 3 | $t_{w(VCLKL)}$ | Pulse duration, VLYNQ_CLOCK low | 4 | | ns |
| 4 | $t_{t(VCLK)}$ | Transition time, VLYNQ_CLOCK | | 3 | ns |

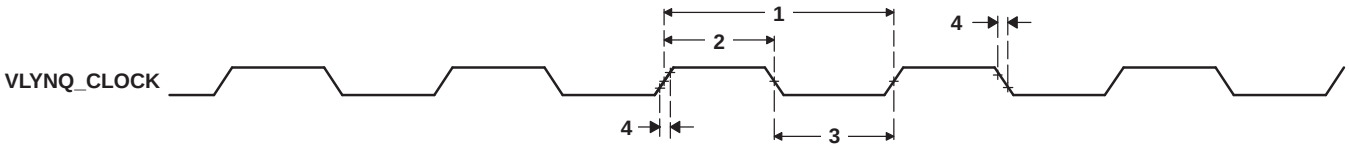


**Figure 7-80. VLYNQ_CLOCK Timing for VLYNQ**

**Table 7-98. Switching Characteristics Over Recommended Operating Conditions for Transmit Data for the VLYNQ Module (see Figure 7-81)**

| NO. | PARAMETER | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | FAST MODE | | SLOW MODE | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(VCLKH-TXDI)}$ | Delay time, VLYNQ_CLOCK high to VLYNQ_TXD[3:0] invalid | 1 | | 2.21 | | ns |
| 2 | $t_{d(VCLKH-TXDV)}$ | Delay time, VLYNQ_CLOCK high to VLYNQ_TXD[3:0] valid | | 7.14 | | 8.5 | ns |

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**Table 7-99. Timing Requirements for Receive Data for the VLYNQ Module(1) (see Figure 7-81)**

| NO. | | | | -1G | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 3 | $t_{su(RXDV-VCLKH)}$ | Setup time, VLYNQ_RXD[3:0] valid before VLYNQ_CLOCK high | RTM disabled, RTM sample = 3 | 0.2 | | ns |
| | | | RTM enabled | (1) | | ns |
| 4 | $t_{h(VCLKH-RXDV)}$ | Hold time, VLYNQ_RXD[3:0] valid after VLYNQ_CLOCK high | RTM disabled, RTM sample = 3 | 2 | | ns |
| | | | RTM enabled | (1) | | ns |

(1) The VLYNQ receive timing manager (RTM) is a serial receive logic designed to eliminate setup and hold violations that could occur in traditional input signals. RTM logic automatically selects the setup and hold timing from one of eight data flops (see Table 7-100). When RTM logic is disabled, the setup and hold timing from the default data flop (3) is used.

**Table 7-100. RTM RX Data Flop Hold/Setup Timing Constraints**

| RX Data Flop | HOLD (Y) | SETUP (X) |
|---|---|---|
| 0 | 0.62 | 1.3 |
| 1 | 1.43 | 0.8 |
| 2 | 1.66 | 0.4 |
| 3 | 2.12 | 0.2 |
| 4 | 2.5 | 0 |
| 5 | 3.18 | -0.3 |
| 6 | 3.87 | -0.5 |
| 7 | 4.25 | -0.7 |

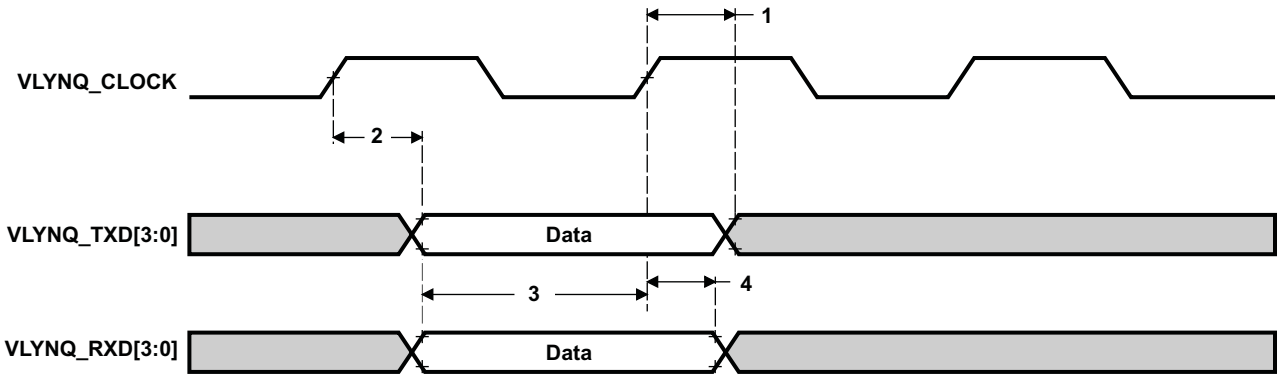


**Figure 7-81. VLYNQ Transmit/Receive Timing**


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## 7.22 Multichannel Audio Serial Port (McASP0/1) Peripherals

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT).

### *7.22.1 McASP Device-Specific Information*

The DM6467T device includes two multichannel audio serial port (McASP) interface peripherals (McASP0 and McASP1). The McASP0 module consists of a transmit and receive section. These sections can operate completely independently with different data formats, separate master clocks, bit clocks, and frame syncs or alternatively, the transmit and receive sections may be synchronized. The McASP0 module also includes a pool of 4 shift registers that may be configured to operate as either transmit data or receive data.

The transmit section of the McASP0 can transmit data in either a time-division-multiplexed (TDM) synchronous serial format or in a digital audio interface (DIT) format where the bit stream is encoded for S/PDIF, AES-3, IEC-60958, CP-430 transmission. The receive section of the McASP0 peripheral supports the TDM synchronous serial format.

The McASP0 module can support one transmit data format (either a TDM format or DIT format) and one receive format at a time. All transmit shift registers use the same format and all receive shift registers use the same format. However, the transmit and receive formats need not be the same. Both the transmit and receive sections of the McASP also support burst mode which is useful for non-audio data (for example, passing control information between two DSPs).

The McASP0 peripheral has additional capability for flexible clock generation, and error detection/handling, as well as error management.

The DM6467T McASP1 module is a reduced feature version of the McASP peripheral. The McASP1 module provides a single transmit-only shift register and can transmit data in DIT format only.

For more detailed information on and the functionality of the McASP peripheral, see the *TMS320DM646x DMSoC Multichannel Audio Serial Port (McASP)* User's Guide (literature number SPRUER1).

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### 7.22.2 McASP0 and McASP1 Peripheral Register Description(s)

**Table 7-101. McASP0 Control Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 01D0 1000 | PID | Peripheral Identification register [Register value: 0x0010 0101] |
| 01D0 1004 | – | Reserved |
| 01D0 1008 | – | Reserved |
| 01D0 100C | – | Reserved |
| 01D0 1010 | PFUNC | Pin function register |
| 01D0 1014 | PDIR | Pin direction register |
| 01D0 1018 | – | Reserved |
| 01D0 101C | – | Reserved |
| 01D0 1020 | – | Reserved |
| 01D0 1024 – 01D0 1040 | – | Reserved |
| 01D0 1044 | GBLCTL | Global control register |
| 01D0 1048 | AMUTE | Mute control register |
| 01D0 104C | DLBCTL | Digital Loop-back control register |
| 01D0 1050 | DITCTL | DIT mode control register |
| 01D0 1054 – 01D0 105C | – | Reserved |
| 01D0 1060 | RGBLCTL | Alias of GBLCTL containing only Receiver Reset bits, allows transmit to be reset independently from receive. |
| 01D0 1064 | RMASK | Receiver format UNIT bit mask register |
| 01D0 1068 | RFMT | Receive bit stream format register |
| 01D0 106C | AFSRCTL | Receive frame sync control register |
| 01D0 1070 | ACLKRCTL | Receive clock control register |
| 01D0 1074 | AHCLKRCTL | High-frequency receive clock control register |
| 01D0 1078 | RTDM | Receive TDM slot 0–31 register |
| 01D0 107C | RINTCTL | Receiver interrupt control register |
| 01D0 1080 | RSTAT | Status register – Receiver |
| 01D0 1084 | RSLOT | Current receive TDM slot register |
| 01D0 1088 | RCLKCHK | Receiver clock check control register |
| 01D0 108C | REVTCTL | Receiver DMA event control register |
| 01D0 1090 – 01D0 109C | – | Reserved |
| 01D0 10A0 | XGBLCTL | Alias of GBLCTL containing only Transmitter Reset bits, allows transmit to be reset independently from receive. |
| 01D0 10A4 | XMASK | Transmit format UNIT bit mask register |
| 01D0 10A8 | XFMT | Transmit bit stream format register |
| 01D0 10AC | AFSXCTL | Transmit frame sync control register |
| 01D0 10B0 | ACLKXCTL | Transmit clock control register |
| 01D0 10B4 | AHCLKXCTL | High-frequency Transmit clock control register |
| 01D0 10B8 | XTDM | Transmit TDM slot 0–31 register |
| 01D0 10BC | XINTCTL | Transmit interrupt control register |
| 01D0 10C0 | XSTAT | Status register – Transmitter |
| 01D0 10C4 | XSLOT | Current transmit TDM slot |
| 01D0 10C8 | XCLKCHK | Transmit clock check control register |
| 01D0 10CC | XEVTCTL | Transmit DMA event control register |


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**Table 7-101. McASP0 Control Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 01D0 10D0 – 01D0 10FC | – | Reserved |
| 01D0 1100 | DITCSRA0 | Left (even TDM slot) channel status register file |
| 01D0 1104 | DITCSRA1 | Left (even TDM slot) channel status register file |
| 01D0 1108 | DITCSRA2 | Left (even TDM slot) channel status register file |
| 01D0 110C | DITCSRA3 | Left (even TDM slot) channel status register file |
| 01D0 1110 | DITCSRA4 | Left (even TDM slot) channel status register file |
| 01D0 1114 | DITCSRA5 | Left (even TDM slot) channel status register file |
| 01D0 1118 | DITCSRB0 | Right (odd TDM slot) channel status register file |
| 01D0 111C | DITCSRB1 | Right (odd TDM slot) channel status register file |
| 01D0 1120 | DITCSRB2 | Right (odd TDM slot) channel status register file |
| 01D0 1124 | DITCSRB3 | Right (odd TDM slot) channel status register file |
| 01D0 1128 | DITCSRB4 | Right (odd TDM slot) channel status register file |
| 01D0 112C | DITCSRB5 | Right (odd TDM slot) channel status register file |
| 01D0 1130 | DITUDRA0 | Left (even TDM slot) user data register file |
| 01D0 1134 | DITUDRA1 | Left (even TDM slot) user data register file |
| 01D0 1138 | DITUDRA2 | Left (even TDM slot) user data register file |
| 01D0 113C | DITUDRA3 | Left (even TDM slot) user data register file |
| 01D0 1140 | DITUDRA4 | Left (even TDM slot) user data register file |
| 01D0 1144 | DITUDRA5 | Left (even TDM slot) user data register file |
| 01D0 1148 | DITUDRB0 | Right (odd TDM slot) user data register file |
| 01D0 114C | DITUDRB1 | Right (odd TDM slot) user data register file |
| 01D0 1150 | DITUDRB2 | Right (odd TDM slot) user data register file |
| 01D0 1154 | DITUDRB3 | Right (odd TDM slot) user data register file |
| 01D0 1158 | DITUDRB4 | Right (odd TDM slot) user data register file |
| 01D0 115C | DITUDRB5 | Right (odd TDM slot) user data register file |
| 01D0 1160 – 01D0 117C | – | Reserved |
| 01D0 1180 | SRCTL0 | Serializer 0 control register |
| 01D0 1184 | SRCTL1 | Serializer 1 control register |
| 01D0 1188 | SRCTL2 | Serializer 2 control register |
| 01D0 118C | SRCTL3 | Serializer 3 control register |
| 01D0 1190 – 01D0 11FC | – | Reserved |
| 01D0 1200 | XBUF0 | Transmit Buffer for Serializer 0 |
| 01D0 1204 | XBUF1 | Transmit Buffer for Serializer 1 |
| 01D0 1208 | XBUF2 | Transmit Buffer for Serializer 2 |
| 01D0 120C | XBUF3 | Transmit Buffer for Serializer 3 |
| 01D0 1210 – 01D0 127C | – | Reserved |
| 01D0 1280 | RBUF0 | Receive Buffer for Serializer 0 |
| 01D0 1284 | RBUF1 | Receive Buffer for Serializer 1 |
| 01D0 1288 | RBUF2 | Receive Buffer for Serializer 2 |
| 01D0 128C | RBUF3 | Receive Buffer for Serializer 3 |
| 01D0 1290 – 01D0 13FF | – | Reserved |

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**Table 7-102. McASP0 Data Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|---|---|---|---|
| 01D0 1400 – 01D0 17FF | RBUF0/XBUF0 | McASP0 receive buffers or McASP0 transmit buffers via the Peripheral Data Bus. | (Used when RSEL or XSEL bits = 0 [these bits are located in the RFMT or XFMT registers, respectively].) |


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**Table 7-103. McASP1 Control Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 01D0 1800 | PID | Peripheral Identification register [Register value: 0x0010 0101] |
| 01D0 1804 | – | Reserved |
| 01D0 1808 | – | Reserved |
| 01D0 180C | – | Reserved |
| 01D0 1810 | PFUNC | Pin function register |
| 01D0 1814 | PDIR | Pin direction register |
| 01D0 1818 | – | Reserved |
| 01D0 181C | – | Reserved |
| 01D0 1820 | – | Reserved |
| 01D0 1824 – 01D0 1843 | – | Reserved |
| 01D0 1844 | GBLCTL | Global control register |
| 01D0 1848 | – | Reserved |
| 01D0 184C | DLBCTL | Digital Loop-back control register |
| 01D0 1850 | DITCTL | DIT mode control register |
| 01D0 1854 – 01D0 185F | – | Reserved |
| 01D0 1860 | RGBLCTL | Alias of GBLCTL containing only Receiver Reset bits, allows transmit to be reset independently from receive. |
| 01D0 1864 | – | Reserved |
| 01D0 1868 | – | Reserved |
| 01D0 186C | – | Reserved |
| 01D0 1870 | – | Reserved |
| 01D0 1874 | – | Reserved |
| 01D0 1878 | – | Reserved |
| 01D0 187C | RINTCTL | Receiver interrupt control register |
| 01D0 1880 | RSTAT | Status register – Receiver |
| 01D0 1884 | – | |
| 01D0 1888 | – | |
| 01D0 188C | – | |
| 01D0 1890 – 01D0 189F | – | Reserved |
| 01D0 18A0 | XGBLCTL | Alias of GBLCTL containing only Transmitter Reset bits, allows transmit to be reset independently from receive. |
| 01D0 18A4 | XMASK | Transmit format UNIT bit mask register |
| 01D0 18A8 | XFMT | Transmit bit stream format register |
| 01D0 18AC | AFSXCTL | Transmit frame sync control register |
| 01D0 18B0 | ACLKXCTL | Transmit clock control register |
| 01D0 18B4 | AHCLKXCTL | High-frequency Transmit clock control register |
| 01D0 18B8 | XTDM | Transmit TDM slot 0–31 register |
| 01D0 18BC | XINTCTL | Transmit interrupt control register |
| 01D0 18C0 | XSTAT | Status register – Transmitter |
| 01D0 18C4 | XSLOT | Current transmit TDM slot |
| 01D0 18C8 | XCLKCHK | Transmit clock check control register |
| 01D0 18CC | XEVTCTL | Transmit DMA event control register |

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**Table 7-103. McASP1 Control Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 01D0 18D0 – 01D0 18FF | – | Reserved |
| 01D0 1900 | DITCSRA0 | Left (even TDM slot) channel status register file |
| 01D0 1904 | DITCSRA1 | Left (even TDM slot) channel status register file |
| 01D0 1908 | DITCSRA2 | Left (even TDM slot) channel status register file |
| 01D0 190C | DITCSRA3 | Left (even TDM slot) channel status register file |
| 01D0 1910 | DITCSRA4 | Left (even TDM slot) channel status register file |
| 01D0 1914 | DITCSRA5 | Left (even TDM slot) channel status register file |
| 01D0 1918 | DITCSRB0 | Right (odd TDM slot) channel status register file |
| 01D0 191C | DITCSRB1 | Right (odd TDM slot) channel status register file |
| 01D0 1920 | DITCSRB2 | Right (odd TDM slot) channel status register file |
| 01D0 1924 | DITCSRB3 | Right (odd TDM slot) channel status register file |
| 01D0 1928 | DITCSRB4 | Right (odd TDM slot) channel status register file |
| 01D0 192C | DITCSRB5 | Right (odd TDM slot) channel status register file |
| 01D0 1930 | DITUDRA0 | Left (even TDM slot) user data register file |
| 01D0 1934 | DITUDRA1 | Left (even TDM slot) user data register file |
| 01D0 1938 | DITUDRA2 | Left (even TDM slot) user data register file |
| 01D0 193C | DITUDRA3 | Left (even TDM slot) user data register file |
| 01D0 1940 | DITUDRA4 | Left (even TDM slot) user data register file |
| 01D0 1944 | DITUDRA5 | Left (even TDM slot) user data register file |
| 01D0 1948 | DITUDRB0 | Right (odd TDM slot) user data register file |
| 01D0 194C | DITUDRB1 | Right (odd TDM slot) user data register file |
| 01D0 1950 | DITUDRB2 | Right (odd TDM slot) user data register file |
| 01D0 1954 | DITUDRB3 | Right (odd TDM slot) user data register file |
| 01D0 1958 | DITUDRB4 | Right (odd TDM slot) user data register file |
| 01D0 195C | DITUDRB5 | Right (odd TDM slot) user data register file |
| 01D0 1960 – 01D0 197F | – | Reserved |
| 01D0 1980 | SRCTL0 | Serializer 0 control register |
| 01D0 1984 – 01D0 19FF | – | Reserved |
| 01D0 1A00 | XBUF0 | Transmit Buffer for Serializer 0 |
| 01D0 1A04 – 01D0 13FF | – | Reserved |

**Table 7-104. McASP1 Data Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|---|---|---|---|
| 01D0 1C00 – 01D0 1FFF | XBUF1 | McASP1 transmit buffers via the Peripheral Data Bus. | (Used when XSEL bits = 0 [these bits are located in the XFMT register].) |


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## 7.22.3 McASP0 and McASP1 Electrical Data/Timing

### 7.22.3.1 Multichannel Audio Serial Port (McASP0) Timing

**Table 7-105. Timing Requirements for McASP0 (see Figure 7-82 and Figure 7-83)(1)**

| NO. | | | | -1G | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{c(AHCKRX)}$ | Cycle time, AHCLKR/X | | 20.8 | | ns |
| 2 | $t_{w(AHCKRX)}$ | Pulse duration, AHCLKR/X high or low | | 8.3 | | ns |
| 3 | $t_{c(CKRX)}$ | Cycle time, ACLKR/X | ACLKR/X ext | 37 | | ns |
| 4 | $t_{w(CKRX)}$ | Pulse duration, ACLKR/X high or low | ACLKR/X ext | 15 | | ns |
| 5 | $t_{su(FRX-CKRX)}$ | Setup time, AFSR/X input valid before ACLKR/X latches data | ACLKR/X int | 15 | | ns |
| | | | ACLKR/X ext | 3 | | ns |
| 6 | $t_{h(CKRX-FRX)}$ | Hold time, AFSR/X input valid after ACLKR/X latches data | ACLKR/X int | 0 | | ns |
| | | | ACLKR/X ext | 3 | | ns |
| 7 | $t_{su(AXR-CKRX)}$ | Setup time, AXR input valid before ACLKR/X latches data | ACLKR int | 15 | | ns |
| | | | ACLKX int | 14 | | ns |
| | | | ACLKR/X ext | 3 | | ns |
| 8 | $t_{h(CKRX-AXR)}$ | Hold time, AXR input valid after ACLKR/X latches data | ACLKR/X int | 3 | | ns |
| | | | ACLKR/X ext | 3 | | ns |

(1) ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1

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**Table 7-106. Switching Characteristics Over Recommended Operating Conditions for McASP0 (1) (2) (3) (see Figure 7-82 and Figure 7-83)**

| NO. | PARAMETER | | | -1G | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 9 | $t_{c(AHCKRX)}$ | Cycle time, AHCLKR/X | | 41.7 | | ns |
| 10 | $t_{w(AHCKRX)}$ | Pulse duration, AHCLKR/X high or low | | AH - 2.5 | | ns |
| 11 | $t_{c(CKRX)}$ | Cycle time, ACLKR/X | ACLKR/X int | 41.7 | | ns |
| 12 | $t_{w(CKRX)}$ | Pulse duration, ACLKR/X high or low | ACLKR/X int | A - 2.5 | | ns |
| 13 | $t_{d(CKRX-FRX)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid | ACLKR int | -2 | 5 | ns |
| | | | ACLKX int | -1 | 5 | ns |
| | | | ACLKR ext | 0 | 15 | ns |
| | | | ACLKX ext | 0 | 16 | ns |
| 14 | $t_{d(CKX-AXRV)}$ | Delay time, ACLKX transmit edge to AXR output valid | ACLKX int | -2 | 5 | ns |
| | | | ACLKX ext | 0 | 16 | ns |
| 15 | $t_{dis(CKRX-AXRHZ)}$ | Disable time, AXR high impedance following last data bit from ACLKR/X transmit edge | ACLKR/X int | -3 | 8 | ns |
| | | | ACLKR/X ext | -3 | 15 | ns |

(1) A = (ACLKR/X period)/2 in ns. For example, when ACLKR/X period is 25 ns, use A = 12.5 ns.
(2) AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(3) ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1


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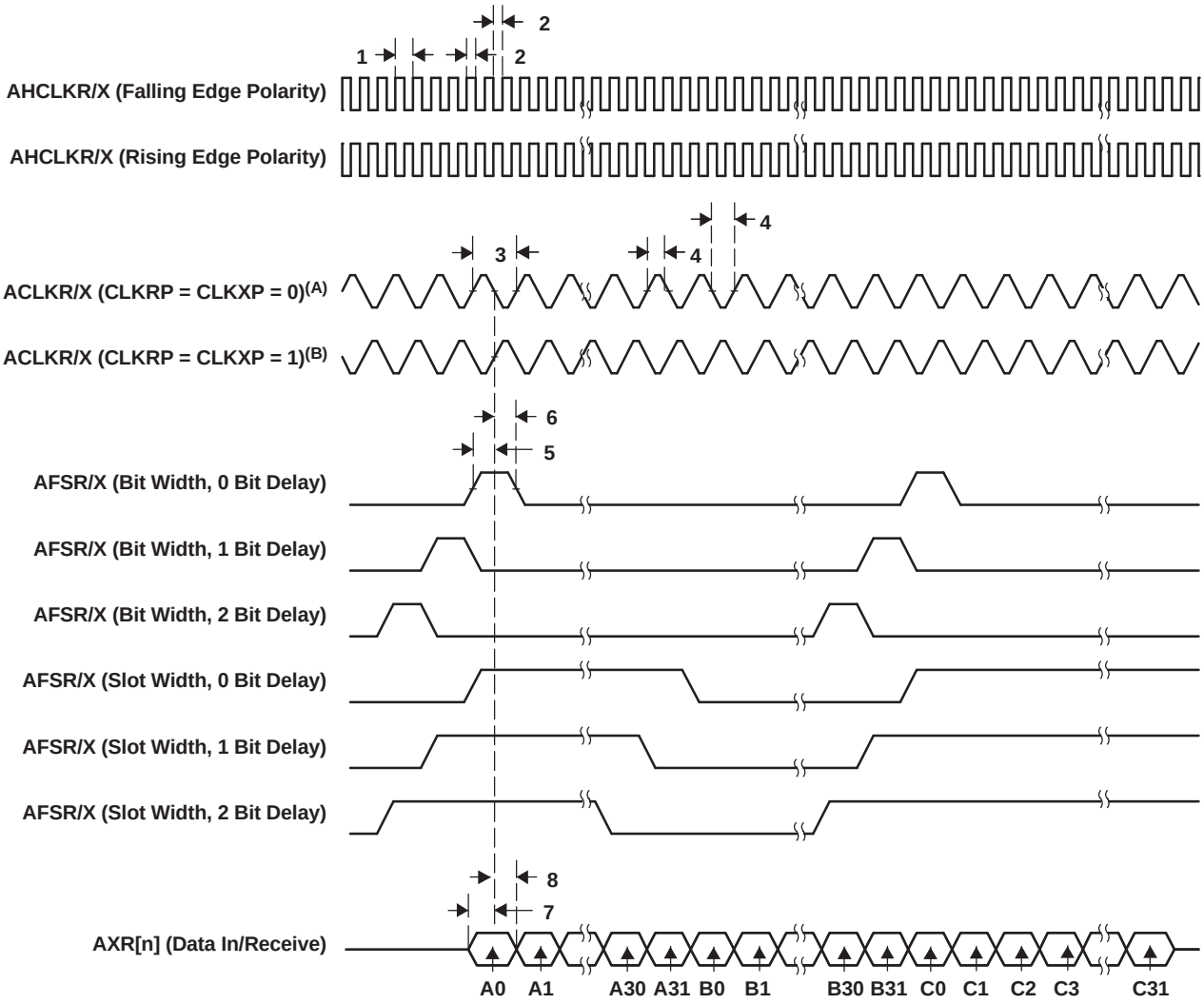
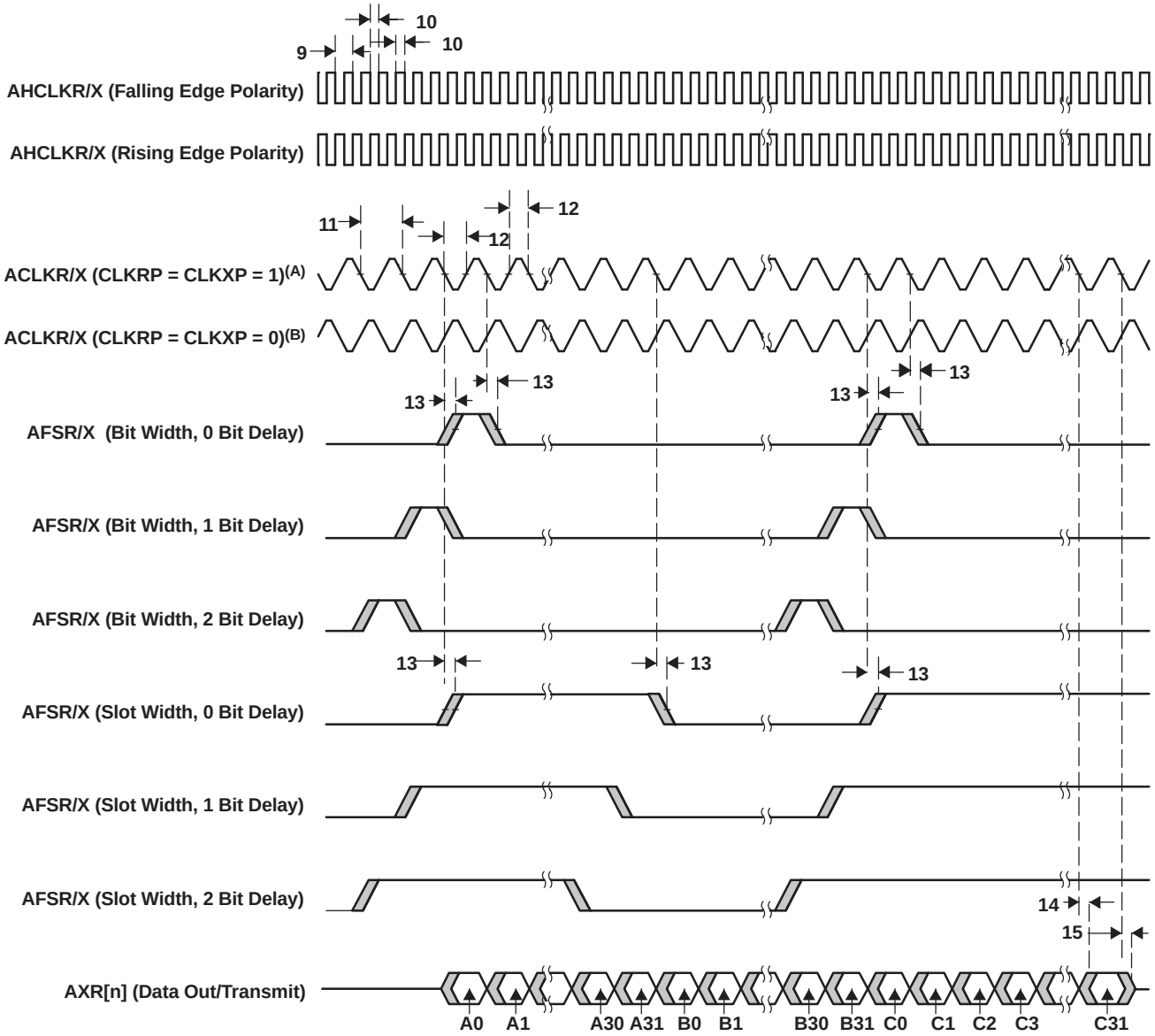



A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

**Figure 7-82. McASP0 and McASP1 Input Timings**




A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

**Figure 7-83. McASP0 and McASP1 Output Timings**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### 7.22.3.2 Multichannel Audio Serial Port (McASP1) DIT Timing

**Table 7-107. Timing Requirements for McASP1 (see Figure 7-82 and Figure 7-83)(1)**

| NO. | | | | -1G | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{c(AHCKRX)}$ | Cycle time, AHCLKX | | 20.8 | | ns |
| 2 | $t_{w(AHCKRX)}$ | Pulse duration, AHCLKX high or low | | 8.3 | | ns |
| 3 | $t_{c(CKRX)}$ | Cycle time, ACLKX | ACLKX ext | 37 | | ns |
| 4 | $t_{w(CKRX)}$ | Pulse duration, ACLKX high or low | ACLKX ext | 15 | | ns |

(1) ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

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**Table 7-108. Switching Characteristics Over Recommended Operating Conditions for McASP1 (1) (2) (3) (see Figure 7-82 and Figure 7-83)**

| NO. | PARAMETER | | | -1G | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 9 | $t_{c(AHCKRX)}$ | Cycle time, AHCLKX | | 41.7 | | ns |
| 10 | $t_{w(AHCKRX)}$ | Pulse duration, AHCLKX high or low | | AH - 2.5 | | ns |
| 11 | $t_{c(CKRX)}$ | Cycle time, ACLKX | | 41.7 | | ns |
| 12 | $t_{w(CKRX)}$ | Pulse duration, ACLKX high or low | ACLKR/X int | A - 2.5 | | ns |
| 14 | $t_{d(CKX-AXRV)}$ | Delay time, ACLKX transmit edge to AXR output valid | ACLKX int | -1 | 5 | ns |
| | | | ACLKX ext | 0 | 16 | ns |
| 15 | $t_{dis(CKRX-AXRHZ)}$ | Disable time, AXR high impedance following last data bit from ACLKX transmit edge | ACLKX int | -3 | 8 | ns |
| | | | ACLKX ext | -3 | 15 | ns |

(1) A = (ACLKX period)/2 in ns. For example, when ACLKX period is 25 ns, use A = 12.5 ns.
(2) AH = (AHCLKX period)/2 in ns. For example, when AHCLKX period is 25 ns, use AH = 12.5 ns.
(3) ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1


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## 7.23 Serial Peripheral Interface (SPI)

The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2-to-16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the TMS320DM646x DMSoC and external peripherals. Typical applications inlcude a interface to external I/O or peripheral expansion via devices such as shift regisers, display drivers, SPI EEPROMs, and Analog-to-Digital Converters (ADCs).

### 7.23.1 SPI Device-Specific Information

The DM6467T SPI supports the following features:

- Master/slave operation
- 2 chip selects for interfacing/control to multiple SPI slave devices
- 3-, 4-, 5-wire interface [The DM6467T supports 3-pin mode, 2 4-pin modes, and the 5-pin mode.]
- 16-bit shift register
- Receive buffer register
- 8-bit clock prescaler
- Programmable SPI clock frequency range, character length, and clock phase and polarity

### 7.23.2 SPI Peripheral Register Description(s)

Table 7-109 shows the SPI registers.

**Table 7-109. SPI Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 01C6 6800 | SPIGCR0 | SPI Global Control Register 0 |
| 01C6 6804 | SPIGCR1 | SPI Global Control Register 1 |
| 01C6 5808 | SPIINT | SPI Interrupt Register |
| 01C6 680C | SPIILVL | SPI Interrupt Level Register |
| 01C6 6810 | SPIFLG | SPI Flag Status Register |
| 01C6 6814 | SPIPC0 | SPI Pin Control Register 0 |
| 01C6 6818 | – | Reserved |
| 01C6 681C | SPIPC2 | SPI Pin Control Register 2 |
| 01C6 6820 – 01C6 6838 | – | Reserved |
| 01C6 683C | SPIDAT1 | SPI Shift Register 1 |
| 01C6 6840 | SPIBUF | SPI Buffer Register |
| 01C6 6844 | SPIEMU | SPI Emulation Register |
| 01C6 6848 | SPIDELAY | SPI Delay Register |
| 01C6 684C | SPIDEF | SPI Default Chip Select Register |
| 01C6 6850 | SPIFMT0 | SPI Data Format Register 0 |
| 01C6 6854 | SPIFMT1 | SPI Data Format Register 1 |
| 01C6 6858 | SPIFMT2 | SPI Data Format Register 2 |
| 01C6 685C | SPIFMT3 | SPI Data Format Register 3 |
| 01C6 6860 | INTVEC0 | SPI Interrupt Vector Register 0 |
| 01C6 6864 | INTVEC1 | SPI Interrupt Vector Register 1 |
| 01C6 6868 – 01C6 6FFF | – | Reserved |

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### 7.23.3 SPI Electrical Data/Timing

#### Master Mode — General

**Table 7-110. General Switching Characteristics in Master Mode(1)**

| NO. | PARAM2ETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(CLK)}$ | Cycle time, SPI_CLK | 2P | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse width, SPI_CLK high | P | | ns |
| 3 | $t_{w(CLKL)}$ | Pulse width, SPI_CLK low | P | | ns |
| 4 | $t_{osu(SIMO-CLK)}$ | Output setup time, SPI_SIMO valid (1st bit) before initial SPI_CLK rising edge, 3-/4-/5-pin mode, polarity = 0, phase = 0 | 2P | | ns |
| | | Output setup time, SPI_SIMO valid (1st bit) before initial SPI_CLK rising edge, 3-/4-/5-pin mode, polarity = 0, phase = 1 | 0.5T + 2P | | |
| | | Output setup time, SPI_SIMO valid (1st bit) before initial SPI_CLK falling edge, 3-/4-/5-pin mode, polarity = 1, phase = 0 | 2P | | |
| | | Output setup time, SPI_SIMO valid (1st bit) before initial SPI_CLK falling edge, 3-/4-/5-pin mode, polarity = 1, phase = 1 | 0.5T + 2P | | |
| 5 | $t_{d(CLK-SIMO)}$ | Delay time, SPI_CLK transmit rising edge to SPI_SIMO output valid (subsequent bit driven), 3-/4-/5-pin mode, polarity = 0, phase = 0 | | 5 | ns |
| | | Delay time, SPI_CLK transmit falling edge to SPI_SIMO output valid (subsequent bit driven), 3-/4-/5-pin mode, polarity = 0, phase = 1 | | 5 | |
| | | Delay time, SPI_CLK transmit falling edge to SPI_SIMO output valid (subsequent bit driven), 3-/4-/5-pin mode, polarity = 1, phase = 0 | | 5 | |
| | | Delay time, SPI_CLK transmit rising edge to SPI_SIMO output valid (subsequent bit driven), 3-/4-/5-pin mode, polarity = 1, phase = 1 | | 5 | |
| 6 | $t_{oh(CLK-SIMO)}$ | Output hold time, SPI_SIMO valid (except final bit) after receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 0 | 0.5T – 4 | | ns |
| | | Output hold time, SPI_SIMO valid (except final bit) after receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 1 | 0.5T – 4 | | |
| | | Output hold time, SPI_SIMO valid (except final bit) after receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 0 | 0.5T – 4 | | |
| | | Output hold time, SPI_SIMO valid (except final bit) after receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 1 | 0.5T – 4 | | |

(1) T = period of SPI_CLK; P = period of SPI core clock


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**Table 7-111. General Input Timing Requirements in Master Mode**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 7 | $t_{su(SOMI-CLK)}$ | Setup time, SPI_SOMI valid before receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 0 | 4 | | ns |
| | | Setup time, SPI_SOMI valid before receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 1 | 4 | | |
| | | Setup time, SPI_SOMI valid before receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 0 | 4 | | |
| | | Setup time, SPI_SOMI valid before receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 1 | 4 | | |
| 8 | $t_{h(CLK-SOMI)}$ | Hold time, SPI_SOMI valid after receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 0 | 2 | | ns |
| | | Hold time, SPI_SOMI valid after receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 1 | 2 | | |
| | | Hold time, SPI_SOMI valid after receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 0 | 2 | | |
| | | Hold time, SPI_SOMI valid after receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 1 | 2 | | |

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### Slave Mode — General

**Table 7-112. General Switching Characteristics in Slave Mode (For 3-/4-/5-Pin Modes)(1)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 13 | $t_{d(CLK-SOMI)}$ | Delay time, transmit rising edge of SPI_CLK to SPI_SOMI output valid, 3-/4-/5-pin mode, polarity = 0, phase = 0 | | 15 | ns |
| | | Delay time, transmit falling edge of SPI_CLK to SPI_SOMI output valid, 3-/4-/5-pin mode, polarity = 0, phase = 1 | | 15 | |
| | | Delay time, transmit falling edge of SPI_CLK to SPI_SOMI output valid, 3-/4-/5-pin mode, polarity = 1, phase = 0 | | 15 | |
| | | Delay time, transmit rising edge of SPI_CLK to SPI_SOMI output valid, 3-/4-/5-pin mode, polarity = 1, phase = 1 | | 15 | |
| 14 | $t_{oh(CLK-SOMI)}$ | Output hold time, SPI_SOMI valid (except final bit) after receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 0 | 0.5T – 4 | | ns |
| | | Output hold time, SPI_SOMI valid (except final bit) after receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 1 | 0.5T – 4 | | |
| | | Output hold time, SPI_SOMI valid (except final bit) after receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 0 | 0.5T – 4 | | |
| | | Output hold time, SPI_SOMI valid (except final bit) after receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 1 | 0.5T – 4 | | |

(1) T = period of SPI_CLK


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**Table 7-113. General Input Timing Requirements in Slave Mode(1)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 9 | $t_{c(CLK)}$ | Cycle time, SPI_CLK | 2P | | ns |
| 10 | $t_{w(CLKH)}$ | Pulse width, SPI_CLK high | P | | ns |
| 11 | $t_{w(CLKL)}$ | Pulse width, SPI_CLK low | P | | ns |
| 15 | $t_{su(SIMO-CLK)}$ | Setup time, SPI_SIMO data valid before receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 0 | 2P | | ns |
| | | Setup time, SPI_SIMO data valid before receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 1 | 2P | | |
| | | Setup time, SPI_SIMO data valid before receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 0 | 2P | | |
| | | Setup time, SPI_SIMO data valid before receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 1 | 2P | | |
| 16 | $t_{h(CLK-SIMO)}$ | Hold time, SPI_SIMO data valid after receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 0 | 2 | | ns |
| | | Hold time, SPI_SIMO data valid after receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 0, phase = 1 | 2 | | |
| | | Hold time, SPI_SIMO data valid after receive rising edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 0 | 2 | | |
| | | Hold time, SPI_SIMO data valid after receive falling edge of SPI_CLK, 3-/4-/5-pin mode, polarity = 1, phase = 1 | 2 | | |

(1) P = period of SPI core clock

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### Master Mode — Additional

**Table 7-114. Additional Output Switching Characteristics of 4-Pin Enable Option in Master Mode(1) (2)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 17 | $t_{d(EN-CLK)}$ | Delay time, slave assertion of $\overline{\text{SPI_EN}}$ active to first SPI_CLK rising edge from master, 4-pin mode, polarity = 0, phase = 0 | | 3P + 6 | ns |
| | | Delay time, slave assertion of $\overline{\text{SPI_EN}}$ active to first SPI_CLK rising edge from master, 4-pin mode, polarity = 0, phase = 1 | | 0.5T + 3P + 6 | |
| | | Delay time, slave assertion of $\overline{\text{SPI_EN}}$ active to first SPI_CLK falling edge from master, 4-pin mode, polarity = 1, phase = 0 | | 3P + 6 | |
| | | Delay time, slave assertion of $\overline{\text{SPI_EN}}$ active to first SPI_CLK falling edge from master, 4-pin mode, polarity = 1, phase = 1 | | 0.5T + 3P + 6 | |

(1) T = period of SPI_CLK; P = period of SPI core clock
(2) Figure 7-86 shows only polarity = 0, phase = 0 as an example. In this case, the Master SPI is ready with new data before $\overline{\text{SPI_EN}}$ assertion.

**Table 7-115. Additional Input Timing Requirements of 4-Pin Enable Option in Master Mode(1) (2)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 18 | $t_{d(CLK-EN)}$ | Delay time, max delay for slave to deassert $\overline{\text{SPI_EN}}$ after final SPI_CLK falling edge, 4-pin mode,polarity = 0, phase = 0 | | 0.5T + P | ns |
| | | Delay time, max delay for slave to deassert $\overline{\text{SPI_EN}}$ after final SPI_CLK falling edge, 4-pin mode,polarity = 0, phase = 1 | | P | |
| | | Delay time, max delay for slave to deassert $\overline{\text{SPI_EN}}$ after final SPI_CLK rising edge, 4-pin mode,polarity = 1, phase = 0 | | 0.5T + P | |
| | | Delay time, max delay for slave to deassert $\overline{\text{SPI_EN}}$ after final SPI_CLK rising edge, 4-pin mode,polarity = 1, phase = 1 | | P | |

(1) T = period of SPI_CLK; P = period of SPI core clock
(2) Figure 7-86 shows only polarity = 0, phase = 0 as an example. In this case, the Master SPI is ready with new data before $\overline{\text{SPI_EN}}$ deassertion.


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**Table 7-116. Additional Output Switching Characteristics of 4-Pin Chip-Select Option in Master Mode(1)(2)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 19 | $t_{osu(CS-CLK)}$ (3) | Output setup time, SPI_CS[n] active before first SPI_CLK rising edge, polarity = 0, phase = 0, SPIDELAY.C2TDELAY = 0 | | (C2TDELAY + 2) * P - 6 | ns |
| | | Output setup time, SPI_CS[n] active before first SPI_CLK rising edge, polarity = 0, phase = 1, SPIDELAY.C2TDELAY = 0 | | (C2TDELAY + 2) * P - 6 | |
| | | Output setup time, SPI_CS[n] active before first SPI_CLK falling edge, polarity = 1, phase = 0, SPIDELAY.C2TDELAY = 0 | | (C2TDELAY + 2) * P - 6 | |
| | | Output setup time, SPI_CS[n] active before first SPI_CLK falling edge, polarity = 1, phase = 1, SPIDELAY.C2TDELAY = 0 | | (C2TDELAY + 2) * P - 6 | |
| 20 | $t_{d(CLK-CS)}$ | Delay time, final SPI_CLK falling edge to master deasserting SPI_CS[n], polarity = 0, phase = 0, SPIDELAY.T2CDELAY = 0, SPIDAT1.CSHOLD not enabled | (T2CDELAY + 1) * P - 6 | | ns |
| | | Delay time, final SPI_CLK falling edge to master deasserting SPI_CS[n], polarity = 0, phase = 1, SPIDELAY.T2CDELAY = 0, SPIDAT1.CSHOLD not enabled | (T2CDELAY + 1) * P - 6 | | |
| | | Delay time, final SPI_CLK rising edge to master deasserting SPI_CS[n], polarity = 1, phase = 0, SPIDELAY.T2CDELAY = 0, SPIDAT1.CSHOLD not enabled | (T2CDELAY + 1) * P - 6 | | |
| | | Delay time, final SPI_CLK rising edge to master deasserting SPI_CS[n], polarity = 1, phase = 1, SPIDELAY.T2CDELAY = 0, SPIDAT1.CSHOLD not enabled | (T2CDELAY + 2) * P - 6 | | |

(1) P = period of SPI core clock
(2) Figure 7-86 shows only polarity = 0, phase = 0 as an example.
(3) The Master SPI is ready with new data before SPI_CS[n] assertion.

**Table 7-117. Additional Output Switching Characteristics of 5-Pin Option in Master Mode(1)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 32 | $t_{d(CLK-CS)}$ (2) | Delay time, final SPI_CLK falling edge to master deasserting SPI_CS[n], polarity = 0, phase = 0, SPIDELAY.T2CDELAY = 0, SPIDAT1.CSHOLD not enabled | (T2CDELAY + 2) * P - 6 | | ns |
| | | Delay time, final SPI_CLK rising edge to master deasserting SPI_CS[n], polarity = 0, phase = 1, SPIDELAY.T2CDELAY[4:0] = 0, SPIDAT1.CSHOLD not enabled | (T2CDELAY + 2) * P - 6 | | |
| | | Delay time, final SPI_CLK rising edge to master deasserting SPI_CS[n], polarity = 1, phase = 0, SPIDELAY.T2CDELAY = 0, SPIDAT1.CSHOLD not enabled | (T2CDELAY + 2) * P - 6 | | |
| | | Delay time, final SPI_CLK falling edge to master deasserting SPI_CS[n], polarity = 1, phase = 1, SPIDELAY.T2CDELAY = 0, SPIDAT1.CSHOLD not enabled | (T2CDELAY + 2) * P - 6 | | |
| 22 | $t_{osu(CS-CLK)}$ (2) (3) | Output setup time, SPI_CS[n] active before first SPI_CLK rising edge, polarity = 0, phase = 0, SPIDELAY.C2TDELAY = 0 | (C2TDELAY + 2) * P - 6 | | ns |
| | | Output setup time, SPI_CS[n] active before first SPI_CLK rising edge, polarity = 0, phase = 1, SPIDELAY.C2TDELAY = 0 | (C2TDELAY + 2) * P - 6 | | |
| | | Output setup time, SPI_CS[n] active before first SPI_CLK falling edge, polarity = 1, phase = 0, SPIDELAY.C2TDELAY = 0 | (C2TDELAY + 2) * P - 6 | | |
| | | Output setup time, SPI_CS[n] active before first SPI_CLK falling edge, polarity = 1, phase = 1, SPIDELAY.C2TDELAY = 0 | (C2TDELAY + 2) * P - 6 | | |
| 23 | $t_{d(CLK-EN)}$ (2) | Delay time, SPI_EN assertion low to first SPI_CLK rising edge, polarity = 0, phase = 0, SPI_EN was initially deasserted and SPI_CLK delayed | | 0.5T + P | ns |
| | | Delay time, SPI_EN assertion low to first SPI_CLK rising edge, polarity = 0, phase = 1, SPI_EN was initially deasserted and SPI_CLK delayed | | P | |
| | | Delay time, SPI_EN assertion low to first SPI_CLK falling edge, polarity = 1, phase = 0, SPI_EN was initially deasserted and SPI_CLK delayed | | 0.5T + P | |
| | | Delay time, SPI_EN assertion low to first SPI_CLK falling edge, polarity = 1, phase = 1, SPI_EN was initially deasserted and SPI_CLK delayed | | P | |

(1) T = period of SPI_CLK; P = period of SPI core clock
(2) Figure 7-86 shows only polarity = 0, phase = 0 as an example.
(3) SPI_EN is immediately asserted, the SPI Master is ready with new data before SPI_CS[n] assertion.


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**Table 7-118. Additional Input Timing Requirements of 5-Pin Option in Master Mode(1)**

| NO. | | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 21 | $t_{d(CSL-ENA)}$ | Delay time, max delay for slave SPI to drive SPI_ENA valid after master asserts SPI_CS[n] to delay the master from beginning the next transfer | | 0.5P | | 0.5D | ns |
| 31 | $t_{d(CLK-ENA)}$ (2) (3) | Delay time, max delay for slave to deassert SPI_ENA after final SPI_CLK falling edge, 5-pin mode, polarity = 0, phase = 0 | | 0.5T | | 0.5T | ns |
| | | Delay time, max delay for slave to deassert SPI_ENA after final SPI_CLK falling edge, 5-pin mode, polarity = 0, phase = 1 | | 0 | | 0 | |
| | | Delay time, max delay for slave to deassert SPI_ENA after final SPI_CLK rising edge, 5-pin mode, polarity = 1, phase = 0 | | 0.5T | | 0.5T | |
| | | Delay time, max delay for slave to deassert SPI_ENA after final SPI_CLK rising edge, 5-pin mode, polarity = 1, phase = 1 | | 0 | | 0 | |

(1) T = period of SPI_CLK; P = period of SPI core clock; D = period of 24-MHz clock
(2) SPI master is ready with new data before SPI_ENA deassertion.
(3) Figure 7-86 shows only polarity = 0, phase = 0 as an example.

### Slave Mode — Additional

**Table 7-119. Additional Output Switching Characteristics of 4-Pin Enable Option in Slave Mode(1)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| SPI24 | $t_{d(CLK-EN)}$ (2) | Delay time, final SPI_CLK falling edge to slave deasserting SPI_EN, polarity = 0, phase = 0 | P – 6 | 3P + 15 | ns |
| | | Delay time, final SPI_CLK falling edge to slave deasserting SPI_EN, polarity = 0, phase = 1 | 0.5T + P – 6 | 0.5T + 3P + 15 | |
| | | Delay time, final SPI_CLK rising edge to slave deasserting SPI_EN, polarity = 1, phase = 0 | P – 6 | 3P + 15 | |
| | | Delay time, final SPI_CLK rising edge to slave deasserting SPI_EN, polarity = 1, phase = 1 | 0.5T + P – 6 | 0.5T + 3P + 15 | |

(1) T = period of SPI_CLK; P = period of SPI core clock
(2) Figure 7-87 shows only polarity = 0, phase = 0 as an example.

**Table 7-120. Additional Output Switching Characteristics of 4-Pin Chip-Select Option in Slave Mode(1)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 27 | $t_{d(CSL-SOMI)}$ | Delay time, master asserting SPI_CS[n] to slave driving SPI_SOMI data valid | | P + 6 | ns |
| 28 | $t_{dis(CSH-SOMI)}$ | Disable time, master deasserting SPI_CS[n] to slave driving SPI_SOMI high impedance | | P + 6 | ns |

(1) T = period of SPI_CLK; P = period of SPI core clock

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**Table 7-121. Additional Input Timing Requirements of 4-Pin Chip-Select Option in Slave Mode(1)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 25 | $t_{su(CSL-CLK)}$ | Setup time, $\overline{SPI_CS[n]}$ asserted at slave to first SPI_CLK edge (rising or falling) at slave | 2P + 6 | | ns |
| 26 | $t_{d(CLK-CSH)}$ (2) | Delay time, final falling edge SPI_CLK to $\overline{SPI_CS[n]}$ deasserted, polarity = 0, phase = 0 | 0.5T + P + 6 | | ns |
| | | Delay time, final falling edge SPI_CLK to $\overline{SPI_CS[n]}$ deasserted, polarity = 0, phase = 1 | P + 6 | | |
| | | Delay time, final rising edge SPI_CLK to $\overline{SPI_CS[n]}$ deasserted, polarity = 1, phase = 0 | 0.5T + P + 6 | | |
| | | Delay time, final rising edge SPI_CLK to $\overline{SPI_CS[n]}$ deasserted, polarity = 1, phase = 1 | P + 6 | | |

(1) T = period of SPI_CLK; P = period of SPI core clock
(2) Figure 7-87 shows only polarity = 0, phase = 0 as an example.

**Table 7-122. Additional Output Switching Characteristics of 5-Pin Option in Slave Mode(1)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| SPI33 | $t_{en(CSL-SOMI)}$ | Enable time, master asserting $\overline{SPI_CS[n]}$ to slave driving SPI_SOMI valid | | P + 6 | ns |
| SPI34 | $t_{dis(CSH-SOMI)}$ | Disable time, master deasserting $\overline{SPI_CS[n]}$ to slave driving SPI_SOMI high impedance | | P + 6 | ns |
| SPI29 | $t_{en(CSL-EN)}$ | Enable time, master asserting $\overline{SPI_CS[n]}$ to slave driving $\overline{SPI_EN}$ | | 6 | ns |
| SPI30 | $t_{dis(CLK-ENZ)}$ (2) | Disable time, final clock receive falling edge of SPI_CLK to slave drive $\overline{SPI_EN}$ high impedance, polarity = 0, phase = 0, SPIINT0.ENABLE HIGHZ = 1 | | 1.5P + 6 | ns |
| | | Disable time, final clock receive rising edge of SPI_CLK to slave drive $\overline{SPI_EN}$ high impedance, polarity = 0, phase = 1, SPIINT0.ENABLE HIGHZ = 1 | | 1.5P + 6 | |
| | | Disable time, final clock receive rising edge of SPI_CLK to slave drive $\overline{SPI_EN}$ high impedance, polarity = 1, phase = 0, SPIINT0.ENABLE HIGHZ = 1 | | 1.5P + 6 | |
| | | Disable time, final clock receive falling edge of SPI_CLK to slave drive $\overline{SPI_EN}$ high impedance, polarity = 1, phase = 1, SPIINT0.ENABLE HIGHZ = 1 | | 1.5P + 6 | |
| 37 | $t_{dis(CSH-ENH)}$ (2) | Disable time, $\overline{SPI_CS[n]}$ deassertion to slave drive $\overline{SPI_EN}$ high impedance, polarity = 0, phase = 0, SPIINT0.ENABLE HIGHZ = 1 | | P + 6 | ns |
| | | Disable time, $\overline{SPI_CS[n]}$ deassertion to slave drive $\overline{SPI_EN}$ high impedance, polarity = 0, phase = 1, SPIINT0.ENABLE HIGHZ = 1 | | P + 6 | |
| | | Disable time, $\overline{SPI_CS[n]}$ deassertion to slave drive $\overline{SPI_EN}$ high impedance, polarity = 1, phase = 0, SPIINT0.ENABLE HIGHZ = 1 | | P + 6 | |
| | | Disable time, $\overline{SPI_CS[n]}$ deassertion to slave drive $\overline{SPI_EN}$ high impedance, polarity = 1, phase = 1, SPIINT0.ENABLE HIGHZ = 1 | | P + 6 | |

(1) T = period of SPI_CLK; P = period of SPI core clock
(2) Figure 7-87 shows only polarity = 0, phase = 0 as an example.


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**Table 7-122. Additional Output Switching Characteristics of 5-Pin Option in Slave Mode(1) (continued)**

| NO. | PARAMETER | | -1G MIN | -1G MAX | UNIT |
|---|---|---|---|---|---|
| 38 | $t_{d(CLK-ENZ)}$ (2) | Delay time, final clock receive edge on SPI_CLK to slave deasserting SPI_EN, polarity = 0, phase = 0, SPIINT0.ENABLE HIGHZ = 0 | | 3P + 15 | ns |
| | | Delay time, final clock receive edge on SPI_CLK to slave deasserting SPI_EN, polarity = 0, phase = 1, SPIINT0.ENABLE HIGHZ = 0 | | 0.5T + 3P + 15 | |
| | | Delay time, final clock receive edge on SPI_CLK to slave deasserting SPI_EN, polarity = 1, phase = 0, SPIINT0.ENABLE HIGHZ = 0 | | 3P + 15 | |
| | | Delay time, final clock receive edge on SPI_CLK to slave deasserting SPI_EN, polarity = 1, phase = 1, SPIINT0.ENABLE HIGHZ = 0 | | 0.5T + 3P + 15 | |
| 39 | $t_{d(CSH-ENH)}$ (2) | Delay time, SPI_CS[n] deassertion to slave deasserting SPI_EN, polarity = 0, phase = 0, SPIINT0.ENABLE HIGHZ = 0 | | 6 | ns |
| | | Delay time, SPI_CS[n] deassertion to slave deasserting SPI_EN, polarity = 0, phase = 1, SPIINT0.ENABLE HIGHZ = 0 | | 6 | |
| | | Delay time, SPI_CS[n] deassertion to slave deasserting SPI_EN, polarity = 1, phase = 0, SPIINT0.ENABLE HIGHZ = 0 | | 6 | |
| | | Delay time, SPI_CS[n] deassertion to slave deasserting SPI_EN polarity = 1, phase = 1, SPIINT0.ENABLE HIGHZ = 0 | | 6 | |

**Table 7-123. Additional Input Timing Requirements of 5-Pin Option in Slave Mode(1)**

| NO. | | | -1G MIN | -1G MAX | UNIT |
|---|---|---|---|---|---|
| 35 | $t_{d(CSL-CLK)}$ | Delay time, SPI_CS[n] asserted at slave to first clock edge (rising or falling) of SPI_CLK at slave | P | | ns |
| 36 | $t_{d(CLK-CSH)}$ (2) | Delay time, SPI_CLK falling edge to SPI_CS[n] deasserted, polarity = 0, phase = 0 | 0.5T + P + 6 | | ns |
| | | Delay time, SPI_CLK falling edge to SPI_CS[n] deasserted, polarity = 0, phase = 1 | P + 6 | | |
| | | Delay time, SPI_CLK rising edge to SPI_CS[n] deasserted, polarity = 1, phase = 0 | 0.5T + P + 6 | | |
| | | Delay time, SPI_CLK rising edge to SPI_CS[n] deasserted, polarity = 1, phase = 1 | P + 6 | | |

(1) T = period of SPI_CLK; P = period of SPI core clock
(2) Figure 7-87 shows only polarity = 0, phase = 0 as an example.

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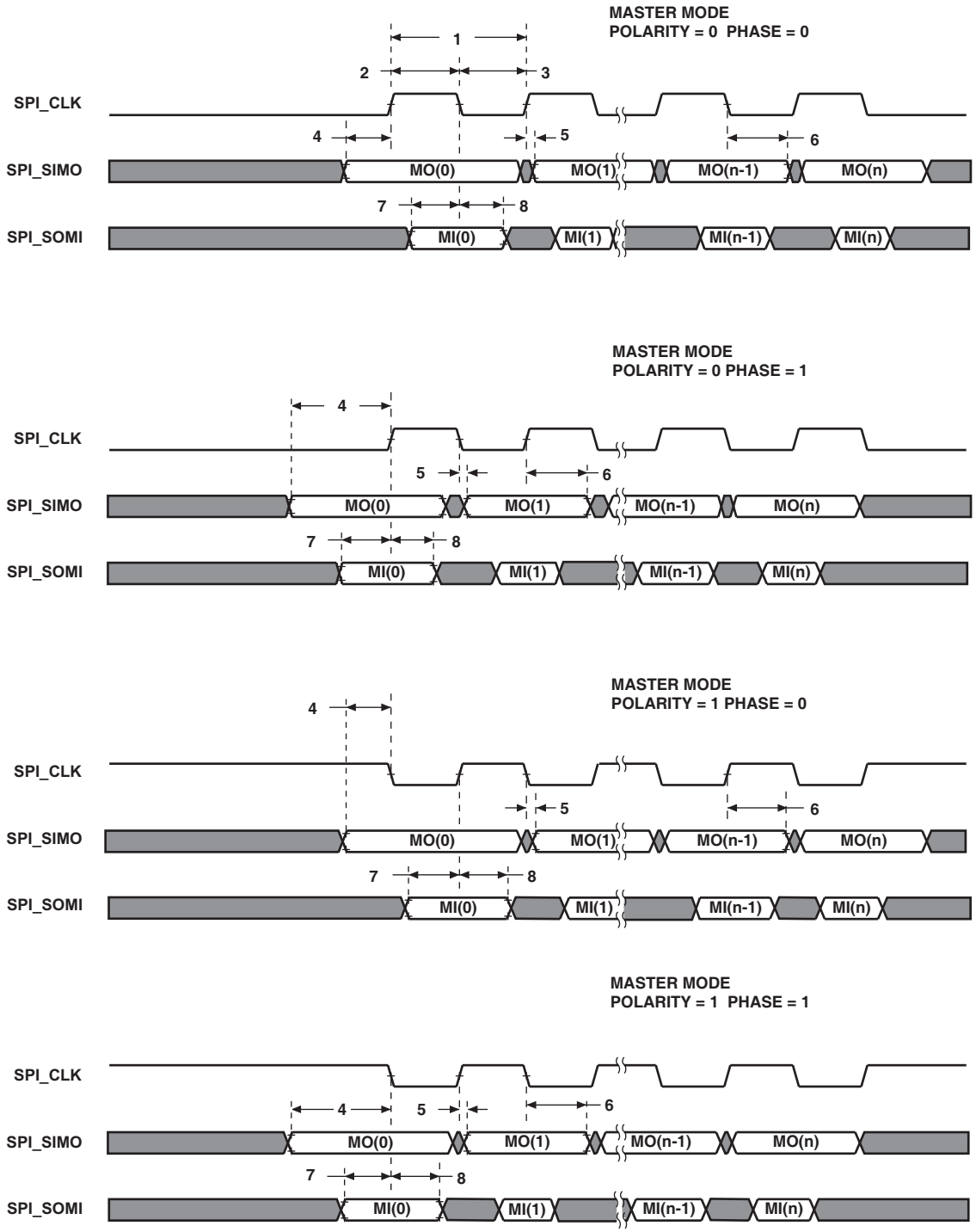


**Figure 7-84. SPI Timings—Master Mode**


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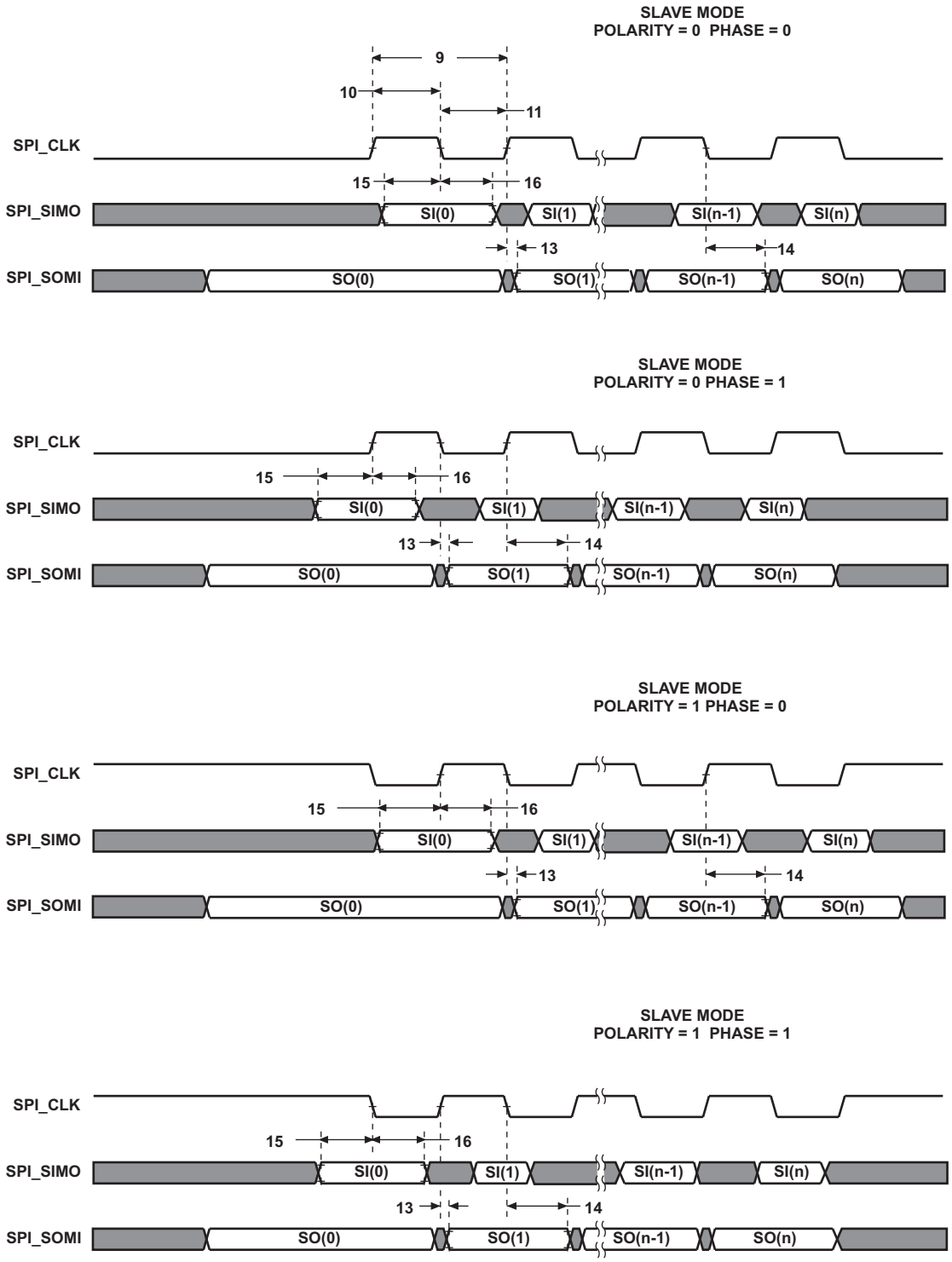
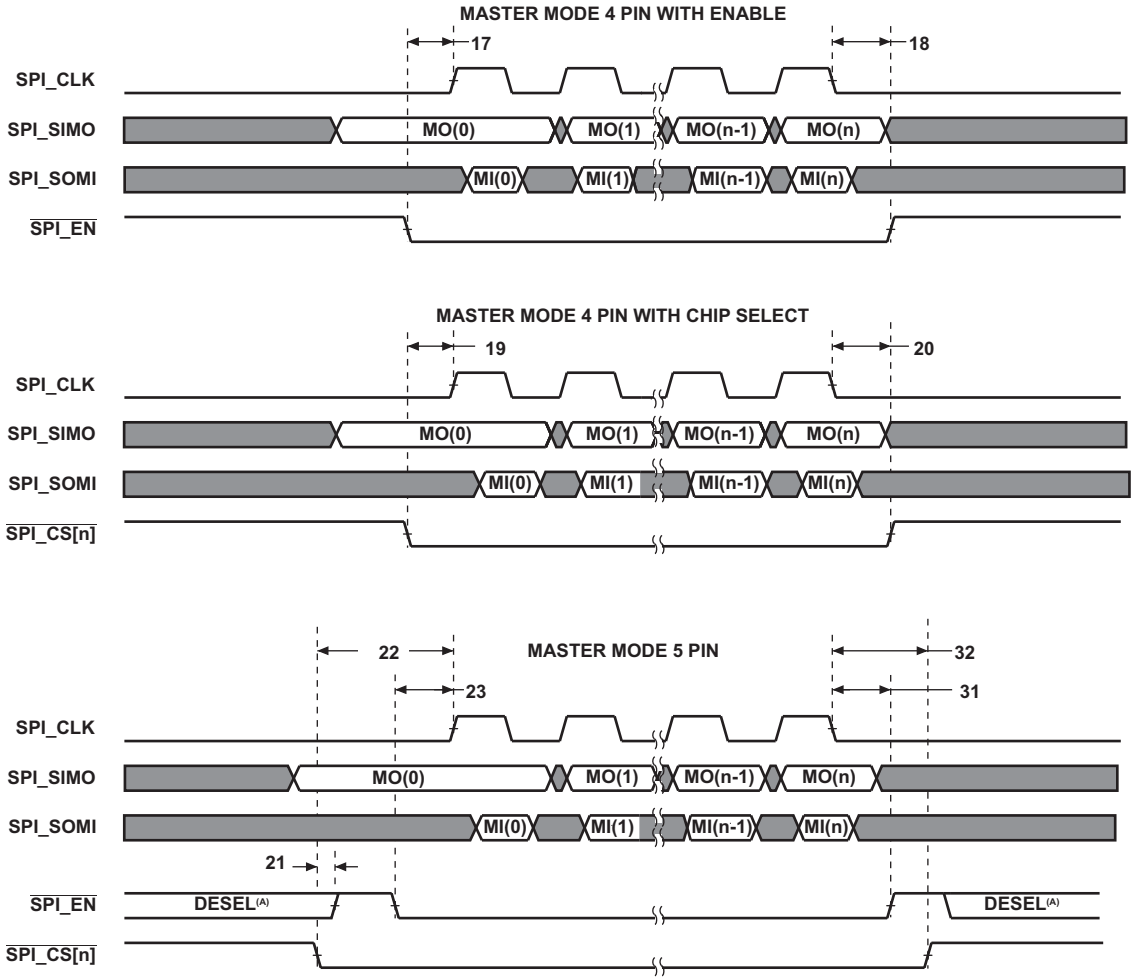



A. The first bit of transmit data becomes valid on the SPI_SOMI pin when software writes to the SPIDAT0/1 register(s). See the *TMS320DM646x DMSoC Serial Peripheral Interface (SPI)* User's Guide (literature number SPRUER4).

**Figure 7-85. SPI Timings—Slave Mode**




A. Deselected is programmable either high or 3-state (requires external pullup)

**Figure 7-86. SPI Timings—Master Mode (4-Pin and 5-Pin)**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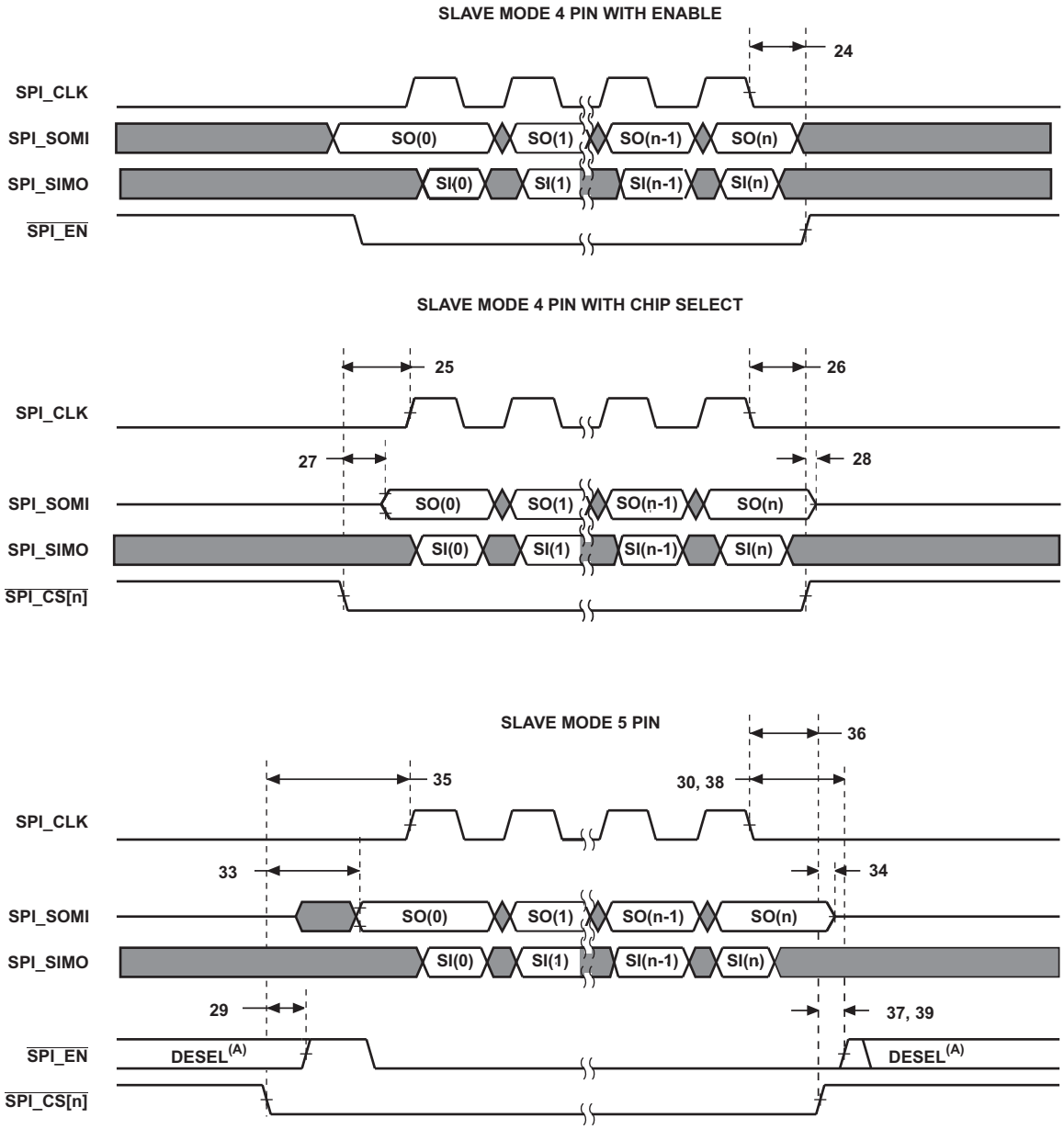


A. Deselected is programmable either high or 3-state (requires external pullup)

**Figure 7-87. SPI Timings—Slave Mode (4-Pin and 5-Pin)**

## 7.24 Universal Asynchronouse Receiver/Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU.

### *7.24.1 UART Device-Specific Information*

DM6467T provides up to 3 UART peripheral interfaces depending on the selected pin multiplexing.

Each UART has the following features:

- Selectable UART/IrDA (SIR/MIR)/CIR modes
- Dual 64 entry FIFOs for received and transmitted data payload
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Frequency prescaler values from 0 to 16 383 it generate the appropriate baud rates
- Two DMA requests and one interrupt request to the system

UART functions include:

- Baud-rate up to 1.8432 Mbit/s
- Software/Hardware flow control
  - Programmable Xon/Xoff characters
  - Programmable Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$
- Programmable serial interfaces characteristics
  - 5, 6, 7, or 8-bit characters
  - Even, odd, mark, space, or no parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
- Additional Modem control functions ($\overline{\text{UDTR0}}$, $\overline{\text{UDSR0}}$, $\overline{\text{UDCD0}}$, and $\overline{\text{URIN0}}$) [UART0 ***only***]

IR-IrDA functions include:

- Both slow infrared (SIR, baud-rate up to 115.2 Kbit/s) and medium infrared (MIR, baud-rate up to 0.576 Mbits/s) supported
- Supports framing error, cyclic redundancy check (CRC) error, and abort pattern (SIR, MIR) detection
- 8-entry status FIFO (with selectable trigger levels) available to monitor frame length and frame errors

IR-CIR functions include:

- Consumer Infrared (CIR) remote control mode with programmable data encoding


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### 7.24.2 UART Peripheral Register Description(s)

Table 7-124 shows the UART register name summary. Table 7-125, Table 7-126, and Table 7-127 show the UART0/1/2 registers, respectively along with their configuration requirements.

**Table 7-124. UART Register Summary**

| ACRONYM | REGISTER NAME | ACRONYM | REGISTER NAME |
|---|---|---|---|
| RHR | Receive Holding Register | RXFLH | Receive Frame Length High Register |
| THR | Transmit Holding Register | BLR | BOF Control Register |
| IER | Interrupt Enable Register | ACREG | Auxilliary Control Register |
| IIR | Interrupt Identification Register | SCR | Supplementary Control Register |
| FCR | FIFO Control Register | SSR | Supplementary Status Register |
| LCR | Line Control Register | EBLR | BOF Length Register |
| MCR | Modem Control Register | MVR | Module Version Register |
| LSR | Line Status Register | SYSC | System Configuration Register |
| MSR | Modem Status Register | SYSS | System Status Register |
| SPR | Scratchpad Register | WER | Wake-up Enable Register |
| TCR | Transmission Control Register | CFPS | Carrier Frequency Prescaler Register |
| TLR | Trigger Level Register | DLL | Divisor Latch Low Register |
| MDR1 | Mode Definition Register 1 | DLH | Divisor Latch High Register |
| MDR2 | Mode Definition Register 2 | UASR | UART Autobauding Status Register |
| SFLSR | Status FIFO Line Status Register | EFR | Enhanced Feature Register |
| RESUME | Resume Register | XON1 | UART XON1 Character Register |
| SFREGL | Status FIFO Register Low | XON2 | UART XON2 Character Register |
| SFREGH | Status FIFO Register High | XOFF1 | UART XOFF1 Character Register |
| TXFLL | Transmit Frame Length Low Register | XOFF2 | UART XOFF2 Character Register |
| TXFLH | Transmit Frame Length High Register | ADDR1 | IrDA Address 1 Register |
| RXFLL | Receive Frame Length Low Register | ADDR2 | IrDA Address 2 Register |

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**Table 7-125. UART0 – UART/IrDA/CIR Register Program Map**

| HEX ADDRESS RANGE | REGISTER | | | | | |
|---|---|---|---|---|---|---|
| | LCR[7] = 0 | | LCR[7] = 1 & LCR[7:0] ≠ 0xBF | | LCR[7:0] = 0xBF | |
| | READ | WRITE | READ | WRITE | READ | WRITE |
| 0x01C2 0000 | RHR | THR | DLL | DLL | DLL | DLL |
| 0x01C2 0004 | IER(1) | IER(1) | DLH | DLH | DLH | DLH |
| 0x01C2 0008 | IIR | FCR(2) | IIR | FCR(2) | EFR | EFR |
| 0x01C2 000C | LCR | LCR | LCR | LCR | LCR | LCR |
| 0x01C2 0010 | MCR(2) | MCR(2) | MCR(2) | MCR(2) | XON1/ADDR1 | XON1/ADDR1 |
| 0x01C2 0014 | LSR | – | LSR | – | XON2/ADR2 | XON2/ADDR2 |
| 0x01C2 0018 | MSR/TCR(3) | TCR(3) | MSR/TCR(3) | TCR(3) | XOFF1/TCR(3) | XOFF1/TCR(3) |
| 0x01C2 001C | SPR/TLR(3) | SPR/TLR(3) | SPR/TLR(3) | SPR/TLR(3) | XOFF2/TLR(3) | XOFF2/TLR(3) |
| 0x01C2 0020 | MDR1 | MDR1 | MDR1 | MDR1 | MDR1 | MDR1 |
| 0x01C2 0024 | MDR2 | MDR2 | MDR2 | MDR2 | MDR2 | MDR2 |
| 0x01C2 0028 | SFLSR | TXFLL | SFLSR | TXFLL | SFLSR | TXFLL |
| 0x01C2 002C | RESUME | TXFLH | RESUME | TXFLH | RESUME | TXFLH |
| 0x01C2 0030 | SFREGL | RXFLL | SFREGL | RXFLL | SFREGL | RXFLL |
| 0x01C2 0034 | SFREGH | RXFLH | SFREGH | RXFLH | SFREGH | RXFLH |
| 0x01C2 0038 | BLR | BLR | UASR | – | UASR | – |
| 0x01C2 003C | ACREG | ACREG | – | – | – | – |
| 0x01C2 0040 | SCR | SCR | SCR | SCR | SCR | SCR |
| 0x01C2 0044 | SSR | – | SSR | – | SSR | – |
| 0x01C2 0048 | EBLR | EBLR | – | – | – | – |
| 0x01C2 004C | – | – | – | – | – | – |
| 0x01C2 0050 | MVR | – | MVR | – | MVR | – |
| 0x01C2 0054 | SYSC | SYSC | SYSC | SYSC | SYSC | SYSC |
| 0x01C2 0058 | SYSS | – | SYSS | – | SYSS | – |
| 0x01C2 005C | WER | WER | WER | WER | WER | WER |
| 0x01C2 0060 | CFPS | CFPS | CFPS | CFPS | CFPS | CFPS |
| 0x01C2 0064 - 0x01C2 007F | – | – | – | – | – | – |

(1) In UART modes, IER.[7:4] can only be written when ENHANCED_EN in EFR = 1. In IrDA/CIR modes, ENHANCED_EN in EFR has no impact on the access to IER.[7:4].
(2) MCR.[7:5] and the TX_FIFO_TRIG bits in FCR can only be written to when the ENHANCED_EN bit in EFR = 1.
(3) Transmission control register (TCR) and trigger level register (TLR) are accessible only when the ENHANCED_EN bit in the EFR =1 and the TCR_TLR bit in the MCR = 1.


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**Table 7-126. UART1 – UART/IrDA/CIR Register Program Map**

| HEX ADDRESS RANGE | REGISTER | | | | | |
|---|---|---|---|---|---|---|
| | LCR[7] = 0 | | LCR[7] = 1 & LCR[7:0] ≠ 0xBF | | LCR[7:0] = 0xBF | |
| | READ | WRITE | READ | WRITE | READ | WRITE |
| 0x01C2 0400 | RHR | THR | DLL | DLL | DLL | DLL |
| 0x01C2 0404 | IER(1) | IER(1) | DLH | DLH | DLH | DLH |
| 0x01C2 0408 | IIR | FCR(2) | IIR | FCR(2) | EFR | EFR |
| 0x01C2 040C | LCR | LCR | LCR | LCR | LCR | LCR |
| 0x01C2 0410 | MCR(2) | MCR(2) | MCR(2) | MCR(2) | XON1/ADDR1 | XON1/ADDR1 |
| 0x01C2 0414 | LSR | – | LSR | – | XON2/ADR2 | XON2/ADDR2 |
| 0x01C2 0418 | MSR/TCR(3) | TCR(3) | MSR/TCR(3) | TCR(3) | XOFF1/TCR(3) | XOFF1/TCR(3) |
| 0x01C2 041C | SPR/TLR(3) | SPR/TLR(3) | SPR/TLR(3) | SPR/TLR(3) | XOFF2/TLR(3) | XOFF2/TLR(3) |
| 0x01C2 0420 | MDR1 | MDR1 | MDR1 | MDR1 | MDR1 | MDR1 |
| 0x01C2 0424 | MDR2 | MDR2 | MDR2 | MDR2 | MDR2 | MDR2 |
| 0x01C2 0428 | SFLSR | TXFLL | SFLSR | TXFLL | SFLSR | TXFLL |
| 0x01C2 042C | RESUME | TXFLH | RESUME | TXFLH | RESUME | TXFLH |
| 0x01C2 0430 | SFREGL | RXFLL | SFREGL | RXFLL | SFREGL | RXFLL |
| 0x01C2 0434 | SFREGH | RXFLH | SFREGH | RXFLH | SFREGH | RXFLH |
| 0x01C2 0438 | BLR | BLR | UASR | – | UASR | – |
| 0x01C2 043C | ACREG | ACREG | – | – | – | – |
| 0x01C2 0440 | SCR | SCR | SCR | SCR | SCR | SCR |
| 0x01C2 0444 | SSR | – | SSR | – | SSR | – |
| 0x01C2 0448 | EBLR | EBLR | – | – | – | – |
| 0x01C2 044C | – | – | – | – | – | – |
| 0x01C2 0450 | MVR | – | MVR | – | MVR | – |
| 0x01C2 0454 | SYSC | SYSC | SYSC | SYSC | SYSC | SYSC |
| 0x01C2 0458 | SYSS | – | SYSS | – | SYSS | – |
| 0x01C2 045C | WER | WER | WER | WER | WER | WER |
| 0x01C2 0460 | CFPS | CFPS | CFPS | CFPS | CFPS | CFPS |
| 0x01C2 0464 - 0x01C2 047F | – | – | – | – | – | – |

(1) In UART modes, IER.[7:4] can only be written when ENHANCED_EN in EFR = 1. In IrDA/CIR modes, ENHANCED_EN in EFR has no impact on the access to IER.[7:4].
(2) MCR.[7:5] and the TX_FIFO_TRIG bits in FCR can only be written to when the ENHANCED_EN bit in EFR = 1.
(3) Transmission control register (TCR) and trigger level register (TLR) are accessible only when the ENHANCED_EN bit in the EFR =1 and the TCR_TLR bit in the MCR = 1.

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**Table 7-127. UART2 – UART/IrDA/CIR Register Program Map**

| HEX ADDRESS RANGE | REGISTER | | | | | |
|---|---|---|---|---|---|---|
| | LCR[7] = 0 | | LCR[7] = 1 & LCR[7:0] ≠ 0xBF | | LCR[7:0] = 0xBF | |
| | READ | WRITE | READ | WRITE | READ | WRITE |
| 0x01C2 0800 | RHR | THR | DLL | DLL | DLL | DLL |
| 0x01C2 0804 | IER(1) | IER(1) | DLH | DLH | DLH | DLH |
| 0x01C2 0808 | IIR | FCR(2) | IIR | FCR(2) | EFR | EFR |
| 0x01C2 080C | LCR | LCR | LCR | LCR | LCR | LCR |
| 0x01C2 0810 | MCR(2) | MCR(2) | MCR(2) | MCR(2) | XON1/ADDR1 | XON1/ADDR1 |
| 0x01C2 0814 | LSR | – | LSR | – | XON2/ADR2 | XON2/ADDR2 |
| 0x01C2 0818 | MSR/TCR(3) | TCR(3) | MSR/TCR(3) | TCR(3) | XOFF1/TCR(3) | XOFF1/TCR(3) |
| 0x01C2 081C | SPR/TLR(3) | SPR/TLR(3) | SPR/TLR(3) | SPR/TLR(3) | XOFF2/TLR(3) | XOFF2/TLR(3) |
| 0x01C2 0820 | MDR1 | MDR1 | MDR1 | MDR1 | MDR1 | MDR1 |
| 0x01C2 0824 | MDR2 | MDR2 | MDR2 | MDR2 | MDR2 | MDR2 |
| 0x01C2 0828 | SFLSR | TXFLL | SFLSR | TXFLL | SFLSR | TXFLL |
| 0x01C2 082C | RESUME | TXFLH | RESUME | TXFLH | RESUME | TXFLH |
| 0x01C2 0830 | SFREGL | RXFLL | SFREGL | RXFLL | SFREGL | RXFLL |
| 0x01C2 0834 | SFREGH | RXFLH | SFREGH | RXFLH | SFREGH | RXFLH |
| 0x01C2 0838 | BLR | BLR | UASR | – | UASR | – |
| 0x01C2 083C | ACREG | ACREG | – | – | – | – |
| 0x01C2 0840 | SCR | SCR | SCR | SCR | SCR | SCR |
| 0x01C2 0844 | SSR | – | SSR | – | SSR | – |
| 0x01C2 0848 | EBLR | EBLR | – | – | – | – |
| 0x01C2 084C | – | – | – | – | – | – |
| 0x01C2 0850 | MVR | – | MVR | – | MVR | – |
| 0x01C2 0854 | SYSC | SYSC | SYSC | SYSC | SYSC | SYSC |
| 0x01C2 0858 | SYSS | – | SYSS | – | SYSS | – |
| 0x01C2 085C | WER | WER | WER | WER | WER | WER |
| 0x01C2 0860 | CFPS | CFPS | CFPS | CFPS | CFPS | CFPS |
| 0x01C2 0864 - 0x01C2 087F | – | – | – | – | – | – |

(1) In UART modes, IER.[7:4] can only be written when ENHANCED_EN in EFR = 1. In IrDA/CIR modes, ENHANCED_EN in EFR has no impact on the access to IER.[7:4].
(2) MCR.[7:5] and the TX_FIFO_TRIG bits in FCR can only be written to when the ENHANCED_EN bit in EFR = 1.
(3) Transmission control register (TCR) and trigger level register (TLR) are accessible only when the ENHANCED_EN bit in the EFR =1 and the TCR_TLR bit in the MCR = 1.


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### 7.24.3 UART Electrical Data/Timing [Receive/Transmit]

**Table 7-128. Timing Requirements for UARTx Receive[1] (see Figure 7-88)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 4 | $t_{w(URXDB)}$ | Pulse duration, receive data bit (URXDx) [15/30/100 pF] | 0.96U | 1.05U | ns |
| 5 | $t_{w(URXSB)}$ | Pulse duration, receive start bit [15/30/100 pF] | 0.96U | 1.05U | ns |

(1) U = UART baud time = 1/programmed baud rate.

**Table 7-129. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit[1] (see Figure 7-88)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $f_{(baud)}$ | Maximum programmable baud rate | | 128 | kHz |
| 2 | $t_{w(UTXDB)}$ | Pulse duration, transmit data bit (UTXDx) [15/30/100 pF] | U - 2 | U + 2 | ns |
| 3 | $t_{w(UTXSB)}$ | Pulse duration, transmit start bit [15/30/100 pF] | U - 2 | U + 2 | ns |

(1) U = UART baud time = 1/programmed baud rate.

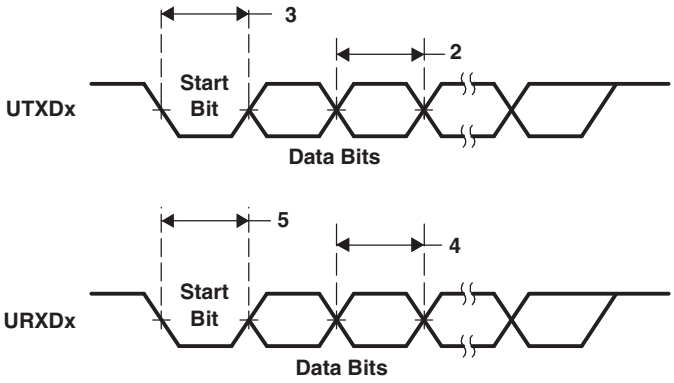


**Figure 7-88. UART Transmit/Receive Timing**

### 7.24.4 IrDA Interface Receive/Transmit Timings

**Table 7-130. Signaling Rate and Pulse Duration Specification in Receive Mode**

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | | UNIT |
|---|---|---|---|---|
| | MAX | NOM | MIN | |
| **SIR MODE** | | | | |
| 2.4 Kbit/s (Kbps) | 1.41 | 78.1 | 88.55 | µs |
| 9.6 Kbps | 1.41 | 19.5 | 22.13 | µs |
| 19.2 Kbps | 1.41 | 9.75 | 11.07 | µs |
| 38.4 Kbps | 1.41 | 4.87 | 5.96 | µs |
| 57.6 Kbps | 1.41 | 3.25 | 4.34 | µs |
| 115.2 Kbps | 1.41 | 1.62 | 2.23 | µs |
| **MIR MODE** | | | | |
| 0.576 Mbit/s (Mbps) | 297.2 | 416 | 518.8 | ns |

**Table 7-131. Timing Requirements for IrDA Receive**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{r(URXD)}$ | Rise time, receive data bit URXDx | | 200 | ns |
| 2 | $t_{f(URXD)}$ | Fall time, receive data bit URXDx | | 200 | ns |

**Table 7-132. Signaling Rate and Pulse Duration Specification in Transmit Mode**

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | | UNIT |
|---|---|---|---|---|
| | MAX | NOM | MIN | |
| **SIR MODE** | | | | |
| 2.4 Kbit/s (Kbps) | 78.10 | 78.1 | 78.10 | µs |
| 9.6 Kbps | 19.50 | 19.5 | 19.50 | µs |
| 19.2 Kbps | 9.75 | 9.75 | 9.75 | µs |
| 38.4 Kbps | 4.87 | 4.87 | 4.87 | µs |
| 57.6 Kbps | 3.25 | 3.25 | 3.25 | µs |
| 115.2 Kbps | 1.62 | 1.62 | 1.62 | µs |
| **MIR MODE** | | | | |
| 0.576 Mbit/s (Mbps) | 414.0 | 416.0 | 419.0 | ns |


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## 7.25 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module provides an interface between DM6467T and other devices compliant with Philips Semiconductors Inter-IC bus ($I^2C$-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 2 to 8-bit data to/from the DMSoC through the I2C module. The I2C port *does not* support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Standard and Fast Modes from 10 – 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- Slew-Rate Limited Open-Drain Output Buffers

For more detailed information on the I2C peripheral, see the *TMS320DM646x DMSoC Inter-Integrated Circuit (I2C) Module* User's Guide (literature number SPRUER0).

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### 7.25.1 I2C Peripheral Register Description(s)

**Table 7-133. I2C Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x1C2 1000 | ICOAR | I2C Own Address Register |
| 0x1C2 1004 | ICIMR | I2C Interrupt Mask Register |
| 0x1C2 1008 | ICSTR | I2C Interrupt Status Register |
| 0x1C2 100C | ICCLKL | I2C Clock Divider Low Register |
| 0x1C2 1010 | ICCLKH | I2C Clock Divider High Register |
| 0x1C2 1014 | ICCNT | I2C Data Count Register |
| 0x1C2 1018 | ICDRR | I2C Data Receive Register |
| 0x1C2 101C | ICSAR | I2C Slave Address Register |
| 0x1C2 1020 | ICDXR | I2C Data Transmit Register |
| 0x1C2 1024 | ICMDR | I2C Mode Register |
| 0x1C2 1028 | ICIVR | I2C Interrupt Vector Register |
| 0x1C2 102C | ICEMDR | I2C Extended Mode Register |
| 0x1C2 1030 | ICPSC | I2C Prescaler Register |
| 0x1C2 1034 | ICPID1 | I2C Peripheral Identification Register 1 |
| 0x1C2 1038 | ICPID2 | I2C Peripheral Identification Register 2 |


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### 7.25.2 I2C Electrical Data/Timing

**Table 7-134. Timing Requirements for I2C Timings(1) (see Figure 7-89)**

| NO. | | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | STANDARD MODE | | FAST MODE | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| 2 | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| 3 | $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | µs |
| 4 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| 5 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| 6 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100(2) | | ns |
| 7 | $t_{h(SDA-SCLL)}$ | Hold time, SDA valid after SCL low | 0(3) | | 0(3) | 0.9(4) | µs |
| 8 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| 9 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | $20 + 0.1C_b$(5) | 300 | ns |
| 10 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | $20 + 0.1C_b$(5) | 300 | ns |
| 11 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | $20 + 0.1C_b$(5) | 300 | ns |
| 12 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | $20 + 0.1C_b$(5) | 300 | ns |
| 13 | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | µs |
| 14 | $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| 15 | $C_b$ (5) | Capacitive load for each bus line | | 400 | | 400 | pF |

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) A Fast-mode $I^2C$-bus™ device can be used in a Standard-mode $I^2C$-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r$ max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode $I^2C$-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

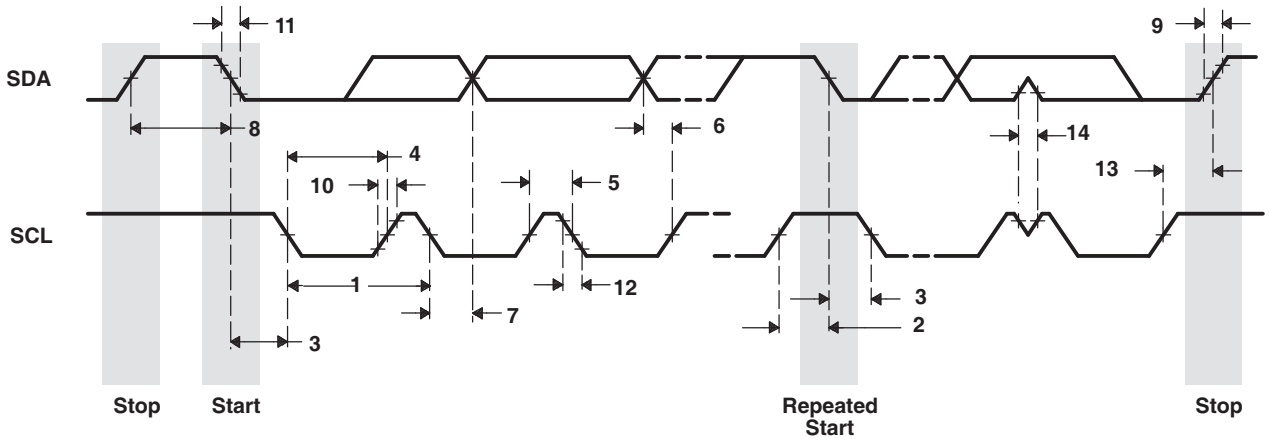


**Figure 7-89. I2C Receive Timings**

**Table 7-135. Switching Characteristics for I2C Timings[1] (see Figure 7-90)**

| NO. | PARAMETER | | -1G | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | STANDARD MODE | | FAST MODE | | |
| | | | MIN | MAX | MIN | MAX | |
| 16 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| 17 | $t_{d(SCLH-SDAL)}$ | Delay time, SCL high to SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| 18 | $t_{d(SDAL-SCLL)}$ | Delay time, SDA low to SCL low (for a START and a repeated START condition) | 4 | | 0.6 | | µs |
| 19 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| 20 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| 21 | $t_{d(SDAV-SCLH)}$ | Delay time, SDA valid to SCL high | 250 | | 100 | | ns |
| 22 | $t_{v(SCLL-SDAV)}$ | Valid time, SDA valid after SCL low | 0 | | 0 | 0.9 | µs |
| 23 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| 24 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | $20 + 0.1C_b$ (2) | 300 | ns |
| 25 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | $20 + 0.1C_b$ (2) | 300 | ns |
| 26 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | $20 + 0.1C_b$ (2) | 300 | ns |
| 27 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | $20 + 0.1C_b$ (2) | 300 | ns |
| 28 | $t_{d(SCLH-SDAH)}$ | Delay time, SCL high to SDA high (for STOP condition) | 4 | | 0.6 | | µs |
| 29 | $C_p$ | Capacitance for each I2C pin | | 10 | | 10 | pF |

(1) $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.
(2) $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

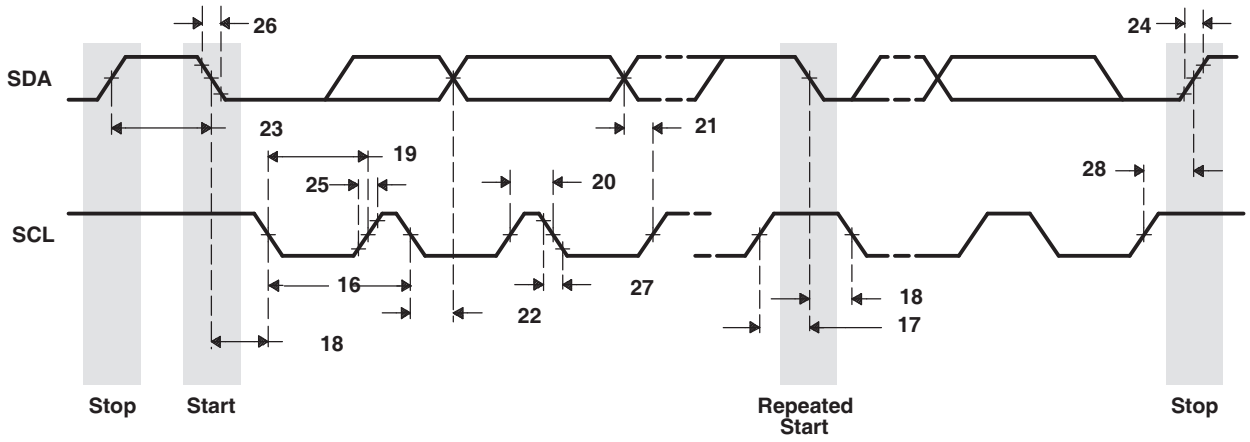


**Figure 7-90. I2C Transmit Timings**


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## 7.26 Pulse Width Modulator (PWM)

The PWM provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components.

### 7.26.1 PWM Device-Specific Information

The 2 DM6467T Pulse Width Modulator (PWM) peripherals support the following features:

- 32-bit period counter
- 32-bit first-phase duration counter
- 32-bit repeat count for one-shot operation. One-shot operation generates N+1 periods of waveform, N being the repeat count register value.
- Configurable to operate in either one-shot or continuous mode
- Programmable buffered period and first-phase duration registers
- One-shot operation triggerable by VPIF or GPIO with programmable edge transitions. (low-to-high or high-to-low).
- One-shot operation generates N+1 periods of waveform, N being the repeat count register value
- Configurable PWM output pin inactive state
- Interrupt and EDMA synchronization events
- Emulation support for stop or free-run operation

### 7.26.2 PWM Peripheral Register Description(s)

Table 7-136 and Table 7-137 show the register memory maps for PWM0/1.

**Table 7-136. PWM0 Register**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C2 2000 | PID | PWM0 Peripheral Identification Register |
| 0x01C2 2004 | PCR | PWM0 Peripheral Control Register |
| 0x01C2 2008 | CFG | PWM0 Configuration Register |
| 0x01C2 200C | START | PWM0 Start Register |
| 0x01C2 2010 | RPT | PWM0 Repeat Count Register |
| 0x01C2 2014 | PER | PWM0 Period Register |
| 0x01C2 2018 | PH1D | PWM0 First-Phase Duration Register |
| 0x01C2 201C - 0x01C2 23FF | - | Reserved |

**Table 7-137. PWM1 Register Memory Map**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C2 2400 | PID | PWM1 Peripheral Identification Register |
| 0x01C2 2404 | PCR | PWM1 Peripheral Control Register |
| 0x01C2 2408 | CFG | PWM1 Configuration Register |
| 0x01C2 240C | START | PWM1 Start Register |
| 0x01C2 2410 | RPT | PWM1 Repeat Count Register |
| 0x01C2 2414 | PER | PWM1 Period Register |
| 0x01C2 2418 | PH1D | PWM1 First-Phase Duration Register |
| 0x01C2 241C -0x01C2 27FF | - | Reserved |

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### 7.26.3 PWM0/1 Electrical Data/Timing

**Table 7-138. Switching Characteristics Over Recommended Operating Conditions for PWM0/1 Outputs[1] (see Figure 7-91 and Figure 7-92)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(PWMH)}$ | Pulse duration, PWMx high | 37 | | ns |
| 2 | $t_{w(PWML)}$ | Pulse duration, PWMx low | 37 | | ns |
| 3 | $t_{t(PWM)}$ | Transition time, PWMx | | 5 | ns |
| 4 | $t_{d(VPIF-PWMV)}$ | Delay time, VPIF (VSYNC) or GPIO trigger event to PWMx valid | 4P | 6P + 20 | ns |

(1) P = SYSCLK3 period in ns.

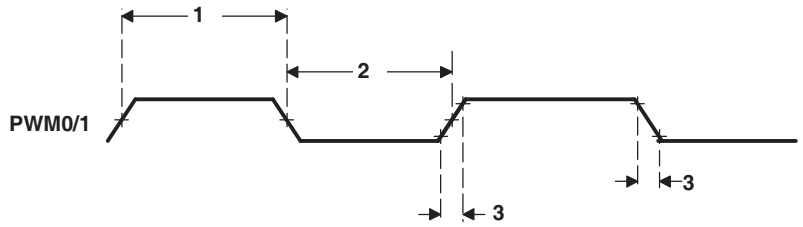


**Figure 7-91. PWM Output Timing**

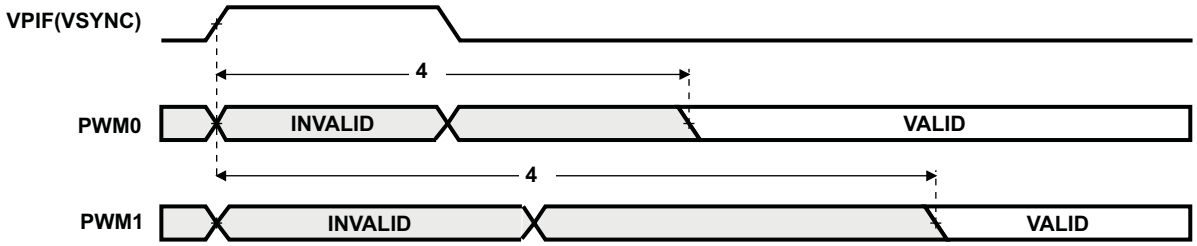


**Figure 7-92. PWM Output Delay Timing**


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## 7.27 Timers

The timers support four modes of operation: a 64-bit general-purpose (GP) timer, dual-unchained 32-bit GP timers, dual-chained 32-bit timers, or a watchdog timer. The GP timer mode can be used to generate periodic interrupts or EDMA synchronization events. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

### *7.27.1 Timers Device-Specific Information*

The DM6467T device has 3 64-bit general-purpose timers which have the following features:

- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode (Timer 0 and 1)
  - Dual 32-bit general-purpose timer mode (Timer 0 and 1)
  - Watchdog timer mode (Timer 2) [mainly controlled by the ARM]
- 2 possible clock sources:
  - Internal clock
  - External clock input via timer input pin TINP0U, TINP0L, and TINP1L, (Timer 0 and 1 only)
- 2 operation modes:
  - One-time operation (timer runs for one period then stops)
  - Continuous operation (timer automatically resets after each period)
- Generates interrupts to the DSP and the ARM CPUs
- Generates sync event to EDMA
- Causes device global reset upon watchdog timer timeout (Timer 2 only)

For more detailed information, see the *TMS320DM646x DMSoC 64-Bit Timer* User's Guide (literature number SPRUER5).

### *7.27.2 Timer Peripheral Register Description(s)*

Table 7-139, Table 7-140, and Table 7-141 show the registers for Timer 0, Timer 1, and Timer 2 (Watchdog).

**Table 7-139. Timer 0 Registers**

| HEX ADDRESS RANGE | ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C2 1400 | PID12 | Timer 0 Peripheral Identification Register 12 |
| 0x01C2 1404 | EMUMGT | Timer 0 Emulation Management |
| 0x01C2 1410 | TIM12 | Timer 0 Counter Register 12 |
| 0x01C2 1414 | TIM34 | Timer 0 Counter Register 34 |
| 0x01C2 1418 | PRD12 | Timer 0 Period Register 12 |
| 0x01C2 141C | PRD34 | Timer 0 Period Register 34 |
| 0x01C2 1420 | TCR | Timer 0 Control Register |
| 0x01C2 1424 | TGCR | Timer 0 Global Control Register |
| 0x01C2 1428 - 0x01C2 17FF | - | Reserved |

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**Table 7-140. Timer 1 Registers**

| HEX ADDRESS RANGE | ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C2 1800 | PID12 | Timer 1 Peripheral Identification Register 12 |
| 0x01C2 1804 | EMUMGT | Timer 1 Emulation Management |
| 0x01C2 1810 | TIM12 | Timer 1 Counter Register 12 |
| 0x01C2 1814 | TIM34 | Timer 1 Counter Register 34 |
| 0x01C2 1818 | PRD12 | Timer 1 Period Register 12 |
| 0x01C2 181C | PRD34 | Timer 1 Period Register 34 |
| 0x01C2 1820 | TCR | Timer 1 Control Register |
| 0x01C2 1824 | TGCR | Timer 1 Global Control Register |
| 0x01C2 1828 - 0x01C2 1BFF | - | Reserved |

**Table 7-141. Timer 2 (Watchdog) Registers**

| HEX ADDRESS RANGE | ACRONYM | DESCRIPTION |
|---|---|---|
| 0x01C2 1C00 | PID12 | Timer 2 Peripheral Identification Register 12 |
| 0x01C2 1C04 | EMUMGT | Timer 2 Emulation Management |
| 0x01C2 1C10 | TIM12 | Timer 2 Counter Register 12 |
| 0x01C2 1C14 | TIM34 | Timer 2 Counter Register 34 |
| 0x01C2 1C18 | PRD12 | Timer 2 Period Register 12 |
| 0x01C2 1C1C | PRD34 | Timer 2 Period Register 34 |
| 0x01C2 1C20 | TCR | Timer 2 Control Register |
| 0x01C2 1C24 | TGCR | Timer 2 Global Control Register |
| 0x01C2 1C28 | WDTCR | Timer 2 Watchdog Timer Control Register |
| 0x01C2 1C2C - 0x01C2 1FFF | - | Reserved |


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### 7.27.3 Timer Electrical Data/Timing

**Table 7-142. Timing Requirements for Timer Input[1] (see Figure 7-93)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(TINPH)}$ | Pulse duration, TINPxL/TINP0U high | 2P | | ns |
| 2 | $t_{w(TINPL)}$ | Pulse duration, TINPxL/TINP0U low | 2P | | ns |

(1) P = DEV_MXI/DEV_CLKIN cycle time in ns. For example, when DEV_MXI/DEV_CLKIN frequency is 27 MHz, use P = 37.0$\overline{37}$ ns.

**Table 7-143. Switching Characteristics Over Recommended Operating Conditions for Timer Output[1] (see Figure 7-93)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 3 | $t_{w(TOUTH)}$ | Pulse duration, TOUTxL/TOUTxU/TOUT2 high | P | | ns |
| 4 | $t_{w(TOUTL)}$ | Pulse duration, TOUTxL/TOUTxU/TOUT2 low | P | | ns |

(1) P = DEV_MXI/DEV_CLKIN cycle time in ns. For example, when DEV_MXI/DEV_CLKIN frequency is 27 MHz, use P = 37.0$\overline{37}$ ns.

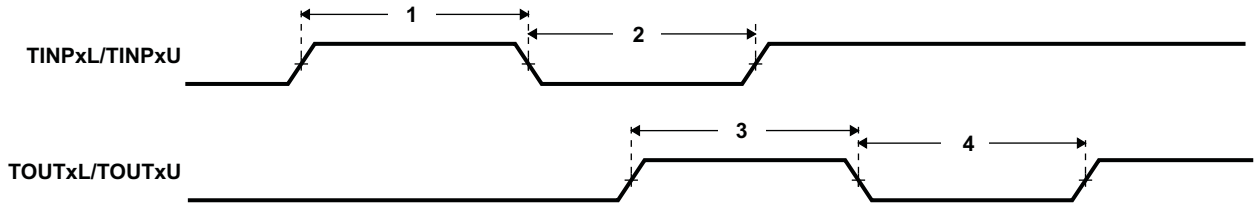


**Figure 7-93. Timer Timing**

## 7.28 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register can control the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts and EDMA events in different interrupt/event generation modes. The GPIO peripheral provides generic connections to external devices. The GPIO pins are grouped into banks of 16 pins per bank (i.e., bank 0 consists of GP[0:15]).

### *7.28.1 GPIO Device-Specific Information*

The DM6467T GPIO peripheral supports the following:

- Up to 33 3.3-V GPIO pins, GP[0:47; not all pinned out]
- Interrupts:
  - Up to 8 unique GP[0:7] interrupts from Bank 0
  - 3 GPIO bank (aggregated) interrupt signals from each of the 3 banks of GPIOs
  - Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO signal
- DMA events:
  - Up to 8 unique GPIO DMA events from Bank 0
  - 3 GPIO bank (aggregated) DMA event signals from each of the 3 banks of GPIOs
- Set/clear functionality: Software writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple software processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to anther process during GPIO programming).
- Separate Input/Output registers
- Output register in addition to set/clear so that, if preferred by software, some GPIO output signals can be toggled by direct write to the output register(s).
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic be implemented.

Although, the DM6467T device implements three GPIO banks, not all GPIOs from all banks are available externally (pinned out). The following GPIOs are ***not*** pinned out on the DM6467T device:

- **BANK 0**
  - GP[9]
  - GP[14]
  - GP[15]
- **BANK 1**
  - GP[27:31]
- **BANK 2**
- GP[34]
- GP[35]
- GP[43:47]

For more detailed information on GPIOs, see the *TMS320DM646x DMSoC General-Purpose Input/Output (GPIO)* User's Guide (literature number SPRUEQ8).


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### 7.28.2 GPIO Peripheral Register Description(s)

Table 7-144 shows the GPIO peripheral registers.

**Table 7-144. GPIO Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01C6 7000 | PID | Peripheral Identification Register |
| 0x01C6 7004 | - | Reserved |
| 0x01C6 7008 | BINTEN | GPIO interrupt per-bank enable |
| **GPIO Banks 0 and 1** | | |
| 0x01C6 700C | - | Reserved |
| 0x01C6 7010 | DIR01 | GPIO Banks 0 and 1 Direction Register (GP[0:31]) |
| 0x01C6 7014 | OUT_DATA01 | GPIO Banks 0 and 1 Output Data Register (GP[0:31]) |
| 0x01C6 7018 | SET_DATA01 | GPIO Banks 0 and 1 Set Data Register (GP[0:31]) |
| 0x01C6 701C | CLR_DATA01 | GPIO Banks 0 and 1 Clear data for banks 0 and 1 (GP[0:31]) |
| 0x01C6 7020 | IN_DATA01 | GPIO Banks 0 and 1 Input Data Register (GP[0:31]) |
| 0x01C6 7024 | SET_RIS_TRIG01 | GPIO Banks 0 and 1 Set Rising Edge Interrupt Register (GP[0:31]) |
| 0x01C6 7028 | CLR_RIS_TRIG01 | GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register (GP[0:31]) |
| 0x01C6 702C | SET_FAL_TRIG01 | GPIO Banks 0 and 1 Set Falling Edge Interrupt Register (GP[0:31]) |
| 0x01C6 7030 | CLR_FAL_TRIG01 | GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register (GP[0:31]) |
| 0x01C6 7034 | INSTAT01 | GPIO Banks 0 and 1 Interrupt Status Register (GP[0:31]) |
| **GPIO Bank 2** | | |
| 0x01C6 7038 | DIR2 | GPIO Bank 2 Direction Register (GP[32:47]) |
| 0x01C6 703C | OUT_DATA2 | GPIO Bank 2 Output Data Register (GP[32:47]) |
| 0x01C6 7040 | SET_DATA2 | GPIO Bank 2 Set Data Register (GP[32:47]) |
| 0x01C6 7044 | CLR_DATA2 | GPIO Bank 2 Clear Data Register (GP[32:47]) |
| 0x01C6 7048 | IN_DATA2 | GPIO Bank 2 Input Data Register (GP[32:47]) |
| 0x01C6 704C | SET_RIS_TRIG2 | GPIO Bank 2 Set Rising Edge Interrupt Register (GP[32:47]) |
| 0x01C6 7050 | CLR_RIS_TRIG2 | GPIO Bank 2 Clear Rising Edge Interrupt Register (GP[32:47]) |
| 0x01C6 7054 | SET_FAL_TRIG2 | GPIO Bank 2 Set Falling Edge Interrupt Register (GP[32:47]) |
| 0x01C6 7058 | CLR_FAL_TRIG2 | GPIO Bank 2 Clear Falling Edge Interrupt Register (GP[32:47]) |
| 0x01C6 705C | INSTAT2 | GPIO Bank 2 Interrupt Status Register (GP[32:47]) |
| 0x01C6 7060 - 0x01C6 77FF | - | Reserved |

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### 7.28.3 GPIO Peripheral Input/Output Electrical Data/Timing

**Table 7-145. Timing Requirements for GPIO Inputs(1) (see Figure 7-94)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(GPIH)}$ | Pulse duration, GP[x] input high | 2C(2) | | ns |
| 2 | $t_{w(GPIL)}$ | Pulse duration, GP[x] input low | 2C(2) | | ns |

(1) The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have DM6467T recognize the GP[x] input changes through software polling of the GPIO register, the GP[x] input duration must be extended to allow DM6467T enough time to access the GPIO register through the internal bus.
(2) C = SYSCLK3 period in ns. For example, when running parts at 1 GHz, use C = 4 ns.

**Table 7-146. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 7-94)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 3 | $t_{w(GPOH)}$ | Pulse duration, GP[x] output high | C(1) (2) | | ns |
| 4 | $t_{w(GPOL)}$ | Pulse duration, GP[x] output low | C(1) (2) | | ns |

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
(2) C = SYSCLK3 period in ns. For example, when running parts at 1 GHz, use C = 4 ns.

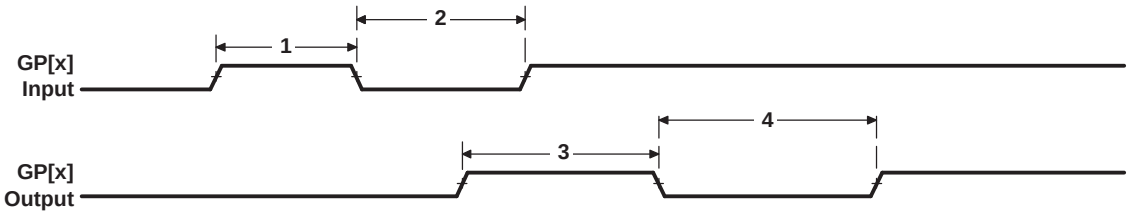


**Figure 7-94. GPIO Port Timing**


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## 7.29 IEEE 1149.1 JTAG

The JTAG [3] interface is used for BSDL testing and emulation of the DM6467T device.

$\overline{\text{TRST}}$ only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality.

$\overline{\text{RESET}}$ must be released only in order for boundary-scan JTAG to read the variant field of IDCODE correctly. Other boundary-scan instructions work correctly independent of current state of $\overline{\text{RESET}}$.

DM6467T includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the device's internal emulation logic will always be properly initialized.

JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of a pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the device after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary scan operations.

### *7.29.1 JTAG ID (JTAGID) Register Description(s)*

**Table 7-147. JTAG ID Register**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|---|---|---|---|
| 0x01C4 0028 | JTAGID | JTAG Identification Register | Read-only. Provides 32-bit JTAG ID of the device. |

(3) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. For the DM6467T device, the JTAG ID register resides at address location 0x01C4 0028. The register hex value for DM6467T is: 0x1B77 002F. For the actual register bit names and their associated bit field descriptions, see Figure 7-95 and Table 7-148.

| 31-28 | 27-12 | 11-1 | 0 |
|---|---|---|---|
| VARIANT (4-Bit) | PART NUMBER (16-Bit) | MANUFACTURER (11-Bit) | LSB |
| R-0001 | R-1011 0111 0111 0000 | R-0000 0010 111 | R-1 |

LEGEND: R = Read, W = Write, n = value at reset

**Figure 7-95. JTAG ID Register Description - DM6467T Register Value - 0x1B77 002F**

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**Table 7-148. JTAG ID Register Selection Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:28 | VARIANT | Variant (4-Bit) value. DM6467T value: 0001 [Silicon Revision 3.0 and later]. |
| 27:12 | PART NUMBER | Part Number (16-Bit) value. DM6467T value: 1011 0111 0111 0000. |
| 11-1 | MANUFACTURER | Manufacturer (11-Bit) value. DM6467T value: 0000 0010 111. |
| 0 | LSB | LSB. This bit is read as a "1" for DM6467T. |

### 7.29.2 JTAG Test-Port Electrical Data/Timing

**Table 7-149. Timing Requirements for JTAG Test Port(1) (2) (see Figure 7-96)**

| NO. | | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 20 | | ns |
| 2 | $t_{w(TCKH)}$ | Pulse duration, TCK high | 0.4T | | ns |
| 3 | $t_{w(TCKL)}$ | Pulse duration, TCK low | 0.4T | | ns |
| 4 | $t_{c(RTCK)}$ | Cycle time, RTCK | 20 | | ns |
| 5 | $t_{w(RTCKH)}$ | Pulse duration, RTCK high | 0.4R | | ns |
| 6 | $t_{w(RTCKL)}$ | Pulse duration, RTCK low | 0.4R | | ns |
| 7 | $t_{su(TDIV-RTCKH)}$ | Setup time, TDI/TMS/$\overline{TRST}$ valid before RTCK high | 12 | | ns |
| 8 | $t_{h(RTCKH-TDIV)}$ | Hold time, TDI/TMS/$\overline{TRST}$ valid after RTCK high | 0 | | ns |
| 9 | $t_{su(EMUV-TCKH)}$ | Setup time, EMU[1:0] valid before TCK high | 1.5 | | ns |
| 10 | $t_{h(TCKH-EMUV)}$ | Hold time, EMU[1:0] valid after TCK high | 4 | | ns |

(1) T = TCK cycle time in ns. For example, when TCK frequency is 20 MHz, use T = 50 ns.
(2) R = RTCLK cycle time in ns. For example, when RTCK frequency is 20 MHz, use T = 50 ns.

**Table 7-150. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port(1) (see Figure 7-96)**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 11 | $t_{d(RTCKL-TDOV)}$ | Delay time, RTCK low to TDO valid | -1 | 8 | ns |
| 12 | $t_{d(TCKH-EMUV)}$ | Delay time, TCK high to EMU[1:0] valid | 2.5 | T - 2.5 | ns |

(1) T = TCK cycle time in ns. For example, when TCK frequency is 20 MHz, use T = 50 ns.


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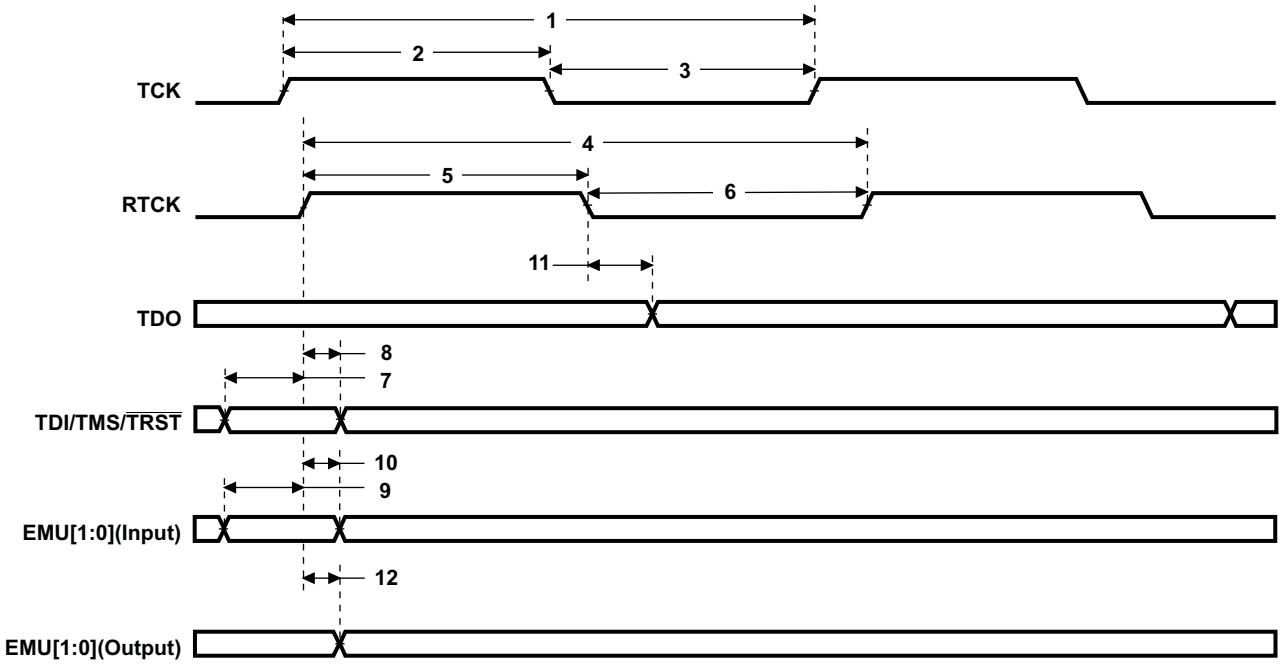


**Figure 7-96. JTAG Test-Port Timing**

# 8 Mechanical Packaging and Orderable Information

The following table(s) show the thermal resistance characteristics for the PBGA–CUT mechanical package.

## 8.1 Thermal Data for CUT

**Table 8-1. Thermal Resistance Characteristics (PBGA Package) [CUT]**

| NO. | | | °C/W(1) | AIR FLOW (m/s)(2) |
|---|---|---|---|---|
| 1 | $R\Theta_{JC}$ | Junction-to-case | 1.5 | N/A |
| 2 | $R\Theta_{JB}$ | Junction-to-board | 9.9 | N/A |
| 3 | $R\Theta_{JA}$ | Junction-to-free air | 19.2 | 0.00 |
| 4 | $R\Theta_{JMA}$ | Junction-to-moving air | 14.8 | 0.50 |
| 5 | | | 13.8 | 1.00 |
| 6 | | | 12.7 | 2.00 |
| 7 | | | 11.9 | 3.00 |
| 8 | $Psi_{JT}$ | Junction-to-package top | 0.3 | 0.00 |
| 9 | | | 0.4 | 0.50 |
| 10 | | | 0.4 | 1.00 |
| 11 | | | 0.4 | 2.00 |
| 12 | | | 0.5 | 3.00 |
| 13 | $Psi_{JB}$ | Junction-to-board | 9.0 | 0.00 |
| 14 | | | 8.0 | 0.50 |
| 15 | | | 7.7 | 1.00 |
| 16 | | | 7.3 | 2.00 |
| 17 | | | 7.0 | 3.00 |

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.

(2) m/s = meters per second

## 8.2 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS320DM6467TCUT1 | ACTIVE | FCBGA | CUT | 529 | 84 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 85 | TMS320 DM6467TCUT1 | Samples |
| TMS320DM6467TCUT9 | ACTIVE | FCBGA | CUT | 529 | 84 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 85 | TMS320 DM6467TCUT9 | Samples |
| TMS320DM6467TCUTD1 | ACTIVE | FCBGA | CUT | 529 | 84 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | -40 to 85 | TMS320 DM6467TCUTD1 | Samples |
| TMS320DM6467TCUTL1 | ACTIVE | FCBGA | CUT | 529 | 84 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | | TMS320 DM6467TCUTL1 | Samples |
| TMS320DM6467TZUT1 | OBSOLETE | FCBGA | ZUT | 529 | | TBD | Call TI | Call TI | 0 to 85 | TMS320 DM6467TZUT1 | |
| TMS320DM6467TZUT9 | LIFEBUY | FCBGA | ZUT | 529 | | TBD | Call TI | Call TI | 0 to 85 | TMS320 DM6467TZUT9 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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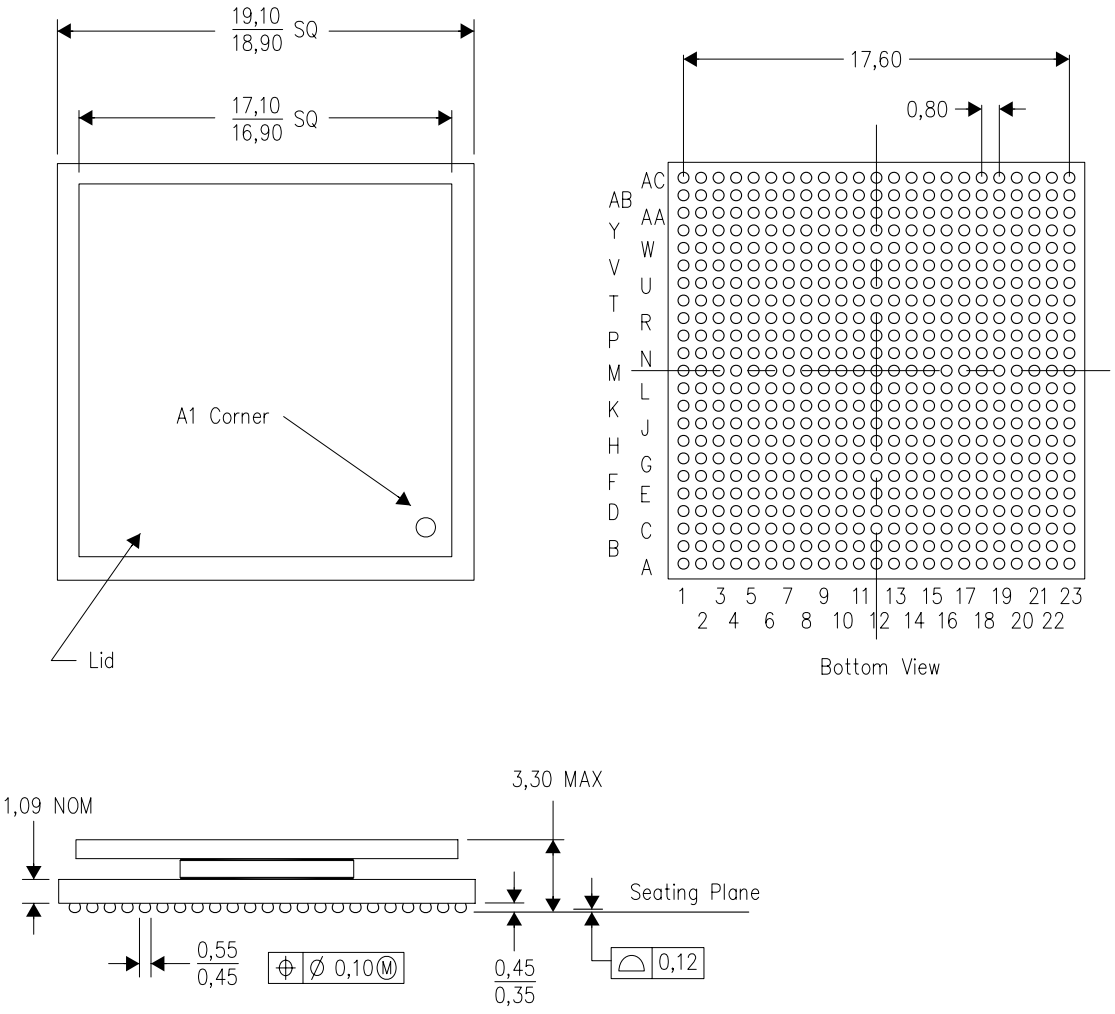
CUT (S–PBGA–N529) PLASTIC BALL GRID ARRAY




4207942/C 02/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Thermally enhanced package with lid.
D. Flip chip application only.
E. Pb–free die bump and solder ball.

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