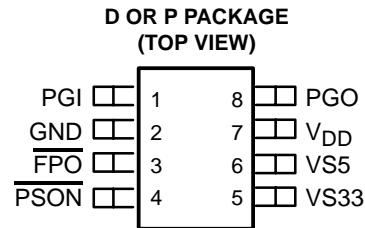


- Overvoltage Protection and Lockout for 12 V, 5 V, 3.3 V
- Undervoltage Protection and Lockout for 5 V and 3.3 V
- Fault Protection Output With Open-Drain Output Stage
- Open-Drain Power Good Output Signal for Power Good Input, 3.3 V and 5 V
- Power Good Delay; 300-ms TPS3510, 150-ms TPS3511
- 75-ms Delay for 5-V and 3.3-V Power Supply Short-Circuit Turnon Protection
- 2.3-ms PSON Control to FPO Turnoff Delay
- 38-ms PSON Control Debounce
- 73- $\mu$ s Width Noise Deglitches
- Wide Supply Voltage Range From 4 V to 15 V



### description

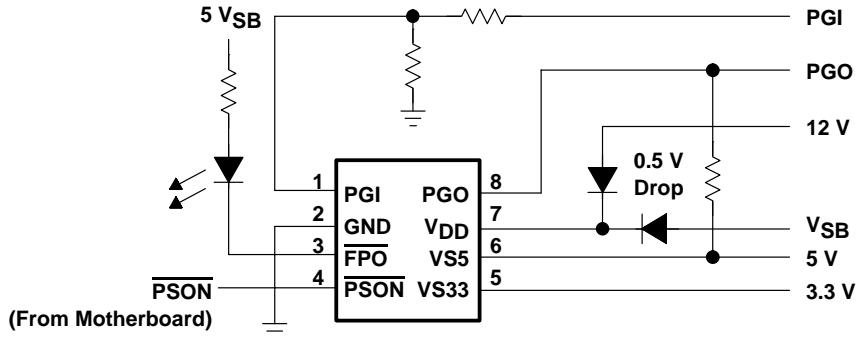
The TPS3510/1 is designed to minimize external components of personal-computer switching power supply systems. It provides protection circuits, power good indicator, fault protection output (FPO) and PSON control.

Overvoltage protection (OVP) monitors 3.3 V, 5 V, and 12 V (12-V signal detects via VDD pin). Undervoltage protection (UVP) monitors 3.3 V and 5 V. When an OV or UV condition is detected, the power good output (PGO) is set to low and FPO is latched high. PSON from low to high resets the protection latch. UVP function is enabled 75 ms after PSON is set low and debounced. Furthermore, there is a 2.3-ms delay (and an additional 38-ms debounce) at turnoff. There is no delay during turnon.

Power good feature monitors PGI, 3.3 V and 5 V and issues a power good signal when the output is ready.

The TPS3510/1 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### typical application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TPS3510, TPS3511 PC POWER SUPPLY SUPERVISORS

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FUNCTION TABLE

PGI	<u>PSON</u>	UV CONDITION (3.3 V OR 5 V)	OV CONDITION (3.3 V, 5 V, OR 12 V)	<u>FPO</u>	PGO
<0.95 V	L	no	no	L	L
<0.95 V	L	no	yes	H	L
<0.95 V	L	yes	no	L	L
0.95 V < PGI < 1.15 V	L	no	no	L	L
0.95 V < PGI < 1.15 V	L	no	yes	H	L
0.95 V < PGI < 1.15 V	L	yes	no	H	L
PGI > 1.15 V	L	no	no	L	H
PGI > 1.15 V	L	no	yes	H	L
PGI > 1.15 V	L	yes	no	H	L
x	H	x	x	H	L

x = don't care

FPO = L means: fault IS NOT latched

FPO = H means: fault IS latched

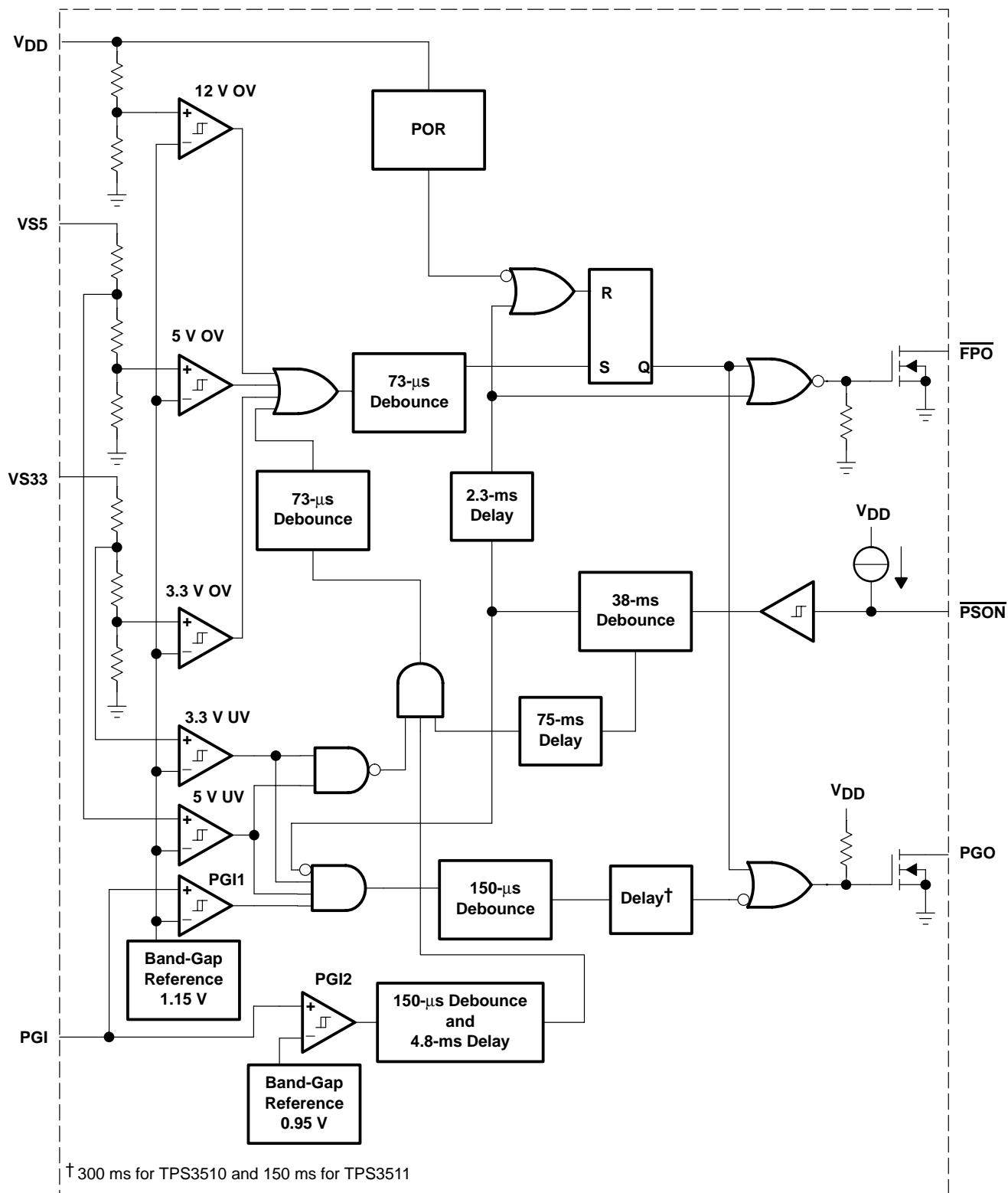
PGO = L means: fault

PGO = H means: NO fault



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functional block diagram

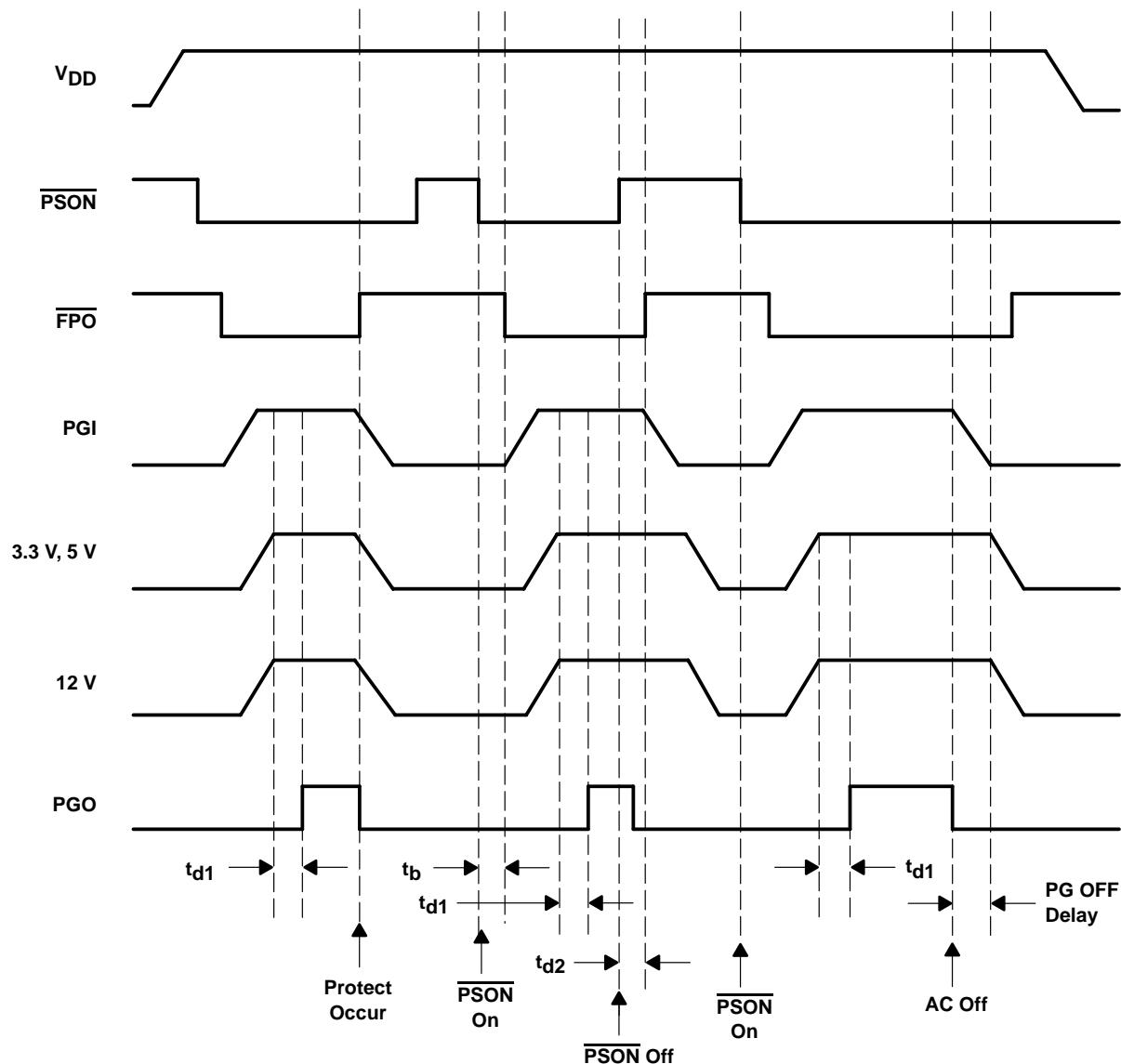


† 300 ms for TPS3510 and 150 ms for TPS3511

# TPS3510, TPS3511 PC POWER SUPPLY SUPERVISORS

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## timing diagram



## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
FPO	3	O	Inverted fault protection output, open drain output stage
GND	2		Ground
PGI	1	I	Power good input
PGO	8	O	Power good output, open drain output stage
PSON	4	I	ON/OFF control
V <sub>DD</sub>	7	I	Supply voltage/12 V overvoltage protection input pin
VS33	5	I	3.3 V over/undervoltage protection
VS5	6	I	5 V over/undervoltage protection

## detailed description

### power good and power good delay

A PC power supply is commonly designed to provide a power-good signal, which is defined by the computer manufacturers. PGO is a power-good signal and should be asserted high by the PC power supply to indicate that the 5-V and 3.3-V outputs are above the under-voltage threshold limit. At this time the converter should be able to provide enough power to ensure continuous operation within the specification. Conversely, when either the 5-V or the 3.3-V output voltages fall below the under-voltage threshold, or when ac power has been removed for a time sufficiently long so that power supply operation is no longer ensured, PGO should be de-asserted to a low state.

Figure 1 represents the timing characteristics of the power good (PGO), dc enable ( $\overline{\text{PSON}}$ ), and the 5 V/3.3 V supply rails.

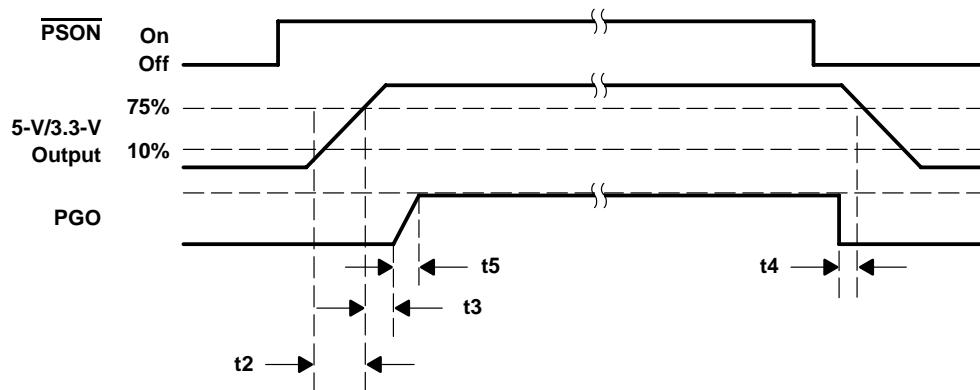


Figure 1. Timing of  $\overline{\text{PSON}}$  and PGO

Although there is no requirement to meet specific timing parameters, the following signal timings are recommended:

$$2 \text{ ms} \leq t2 \leq 20 \text{ ms}, 100 \text{ ms} < t3 < 2000 \text{ ms}, t4 > 1 \text{ ms}, t5 \leq 10 \text{ ms}$$

Furthermore motherboards should be designed to comply with the previously recommended timing. If timings other than these are implemented or required, this information should be clearly specified.

The TPS3510/1 family of power-supply supervisors provides a power-good output (PGO) for the 3.3-V and 5-V supply voltage rails and a separate power-good input (PGI). An internal timer is used to generate a power-good delay. If the voltage signals at PGI, VS33, and VS5 rise above the under-voltage threshold, the open-drain power-good output (PGO) goes high after a delay of 150 ms or 300 ms. When the PGI voltage or either the 3.3-V and 5-V power rails drops below the under-voltage threshold, PGO is disabled immediately (after 150- $\mu$ s debounce).

### power supply remote on/off ( $\overline{\text{PSON}}$ ) and fault protect output ( $\overline{\text{FPO}}$ )

Since the latest personal computer generation focuses on easy turnon and power saving functions, the PC power supply requires two characteristics. One is a dc power supply remote on/off function, the other is standby voltage to achieve very low power consumption of the PC system. Thus the main power needs to be shut down.

The power supply remote on/off ( $\overline{\text{PSON}}$ ) is an active low signal that turns on all of the main power rails including 3.3 V, 5 V, -5 V, 12 V, and -12 V power rails. When this signal is held high by the PC motherboard or left open circuited, the signal of the fault protect output ( $\overline{\text{FPO}}$ ) also goes high. Thus, the main power rails should not deliver current and should be held at 0 V.

# TPS3510, TPS3511 PC POWER SUPPLY SUPERVISORS

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## power supply remote on/off (PSON) and fault protect output (FPO)(continued)

When the FPO signal is held high due to an occurring fault condition, the fault status is latched and the outputs of the main power rails should not deliver current but are held at 0 V. Toggling the power supply remote on/off (PSON) from low to high resets the fault-protection latch. During this fault condition only the standby power is not affected.

When PSON goes from high to low or low to high, the 38-ms debounce block is active to avoid a glitch on the input that disables/enables the FPO output. During this period the under-voltage function is disabled for 75 ms to prevent turnon failure. At turnoff, there is an additional delay of 2.3 ms from PSON to FPO.

Power should be delivered to the rails only if the PSON signal is held at ground potential, thus FPO is active-low. The FPO pin can be connected to 5 V (or up to 15 V) through a pullup resistor.

## undervoltage protection

The TPS3510/1 provides under-voltage protection (UVP) for the 3.3-V and 5-V rails. When an undervoltage condition appears at either one of the 3.3-V (VS33) or 5-V (VS5) input pins for more than 146  $\mu$ s, the FPO output goes high and PGO goes low. Also, this fault condition is latched until PSON is toggled from low to high or  $V_{DD}$  is removed.

The need for undervoltage protection is often overlooked in off-line switching power supply system design. But it is very important in battery-powered or hand-held equipment since the TTL or CMOS logic often results in malfunction.

In flyback or forward-type off-line switching power supplies, usually designed for low power, the overload protection design is very simple. Most of these types of power supplies are only sensing the input current for an overload condition. The trigger point needs to be set much higher than the maximum load in order to prevent false turnon.

However, this causes one critical problem. If the connected load is larger than the maximum allowable load but smaller than the trigger point, the system always becomes overheated with failure and damage occurring.

## overvoltage protection

The overvoltage protection (OVP) of TPS3510/1 monitors 3.3 V, 5 V, and 12 V (12 V is sensed via the  $V_{DD}$  pin). When an overvoltage condition appears at one of the 3.3-V, 5-V, or 12-V input pins for more than 73  $\mu$ s, the FPO output goes high and PGO goes low. Also, this fault condition is latched until PSON is toggled from low to high or  $V_{DD}$  is removed. During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage of the system. To protect the system under these abnormal conditions, it is common practice to provide overvoltage protection within the power supply.

Because TTL and CMOS circuits are very vulnerable to overvoltages, it is becoming industry standard to provide overvoltage protection on all 3.3-V and 5-V outputs. However, not only the 3.3-V and 5-V rails for the logic circuits on the motherboard need to be protected, but also the 12-V peripheral devices such as the hard disk, floppy disk, and CD-ROM players etc., need to be protected.

## short-circuit power supply turnon

During safety testing the power supply might have tied the output voltage direct to ground. If this happens during the normal operating, this is called a short-circuit or over-current condition. When it happens before the power supply turns on, this is called a short-circuit power supply turnon. It can happen during the design period, in the production line, at quality control inspection or at the end user. The TPS3510/1 provides an undervoltage protection function with a 75-ms delay after PSON is set low.



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**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage, $V_{DD}$ (see Note1)	16 V
Output voltage $V_O$ : FPO	16 V
PGO	8 V
All other pins (see Note 1)	–0.3 V to 16 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Soldering temperature	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING
P	1092 mW	8.74 mW/°C	699 mW	568 mW
D	730 mW	5.84 mW/°C	467 mW	379 mW

**recommended operating conditions at specified temperature range**

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$		4		15	V
Input voltage, $V_I$	PSON, VS5, VS33			7	V
	PGI			$V_{DD} + 0.3$ V (max = 7 V)	
Output voltage, $V_O$	FPO			15	V
	PGO			7	
Output sink current, $I_{O,sink}$	FPO			20	mA
	PGO			10	
Supply voltage rising time, $t_r$	See Note 2		1		ms
Operating free-air temperature range, $T_A$		–40		85	°C

NOTE 2:  $V_{DD}$  rising and falling slew rate must be less than 14 V/ms.

# TPS3510, TPS3511 PC POWER SUPPLY SUPERVISORS

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## electrical characteristics over recommended operating conditions (unless otherwise noted)

### overvoltage protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage threshold	VS33		3.7	3.9	4.1	V
	VS5		5.7	6.1	6.5	
	V <sub>DD</sub>		13.2	13.8	14.4	
I <sub>LKG</sub>	Leakage current (FPO)	V(FPO) = 5 V		5	μA	
V <sub>OL</sub>	Low-level output voltage (FPO)	V <sub>DD</sub> = 5 V, I <sub>sink</sub> = 20 mA		0.7	V	
Noise deglitch time OVP		V <sub>DD</sub> = 5 V	35	73	110	μs

### PGI and PGO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>PGI</sub>	Input threshold voltage (PGI)	PGI1		1.1	1.15	1.2	
		PGI2		0.9	0.95	1	
V <sub>IT</sub>	Undervoltage threshold	VS33		2	2.2	2.4	
		VS5		3.3	3.5	3.7	
I <sub>LKG</sub>	Leakage current (PGO)	PGO = 5 V		5	μA		
V <sub>OL</sub>	Low-level output voltage (PGO)	V <sub>DD</sub> = 4 V, I <sub>sink</sub> = 10 mA		0.4	V		
Short-circuit protection delay		3.3 V, 5 V		49	75	114	
t <sub>d1</sub>	Delay time	TP3510	PGI to PGO	200	300	450	
		TP3511		100	150	225	
				3.2	4.8	7.2	
Noise deglitch time		PGI to PGO	V <sub>DD</sub> = 5 V	88	150	225	
		PGI to FPO		180	296	445	
		UVP to FPO		82	146	220	

### PSON control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>I</sub>	Input pullup current	PSON = 0 V		120		μA
V <sub>IH</sub>	High-level input voltage			2.4		V
V <sub>IL</sub>	Low-level input voltage				1.2	V
t <sub>b</sub>	Debounce time (PSON)	V <sub>DD</sub> = 5 V	24	38	57	ms
t <sub>d2</sub>	Delay time (PSON to FPO)	V <sub>DD</sub> = 5 V	t <sub>b</sub> +1.1	t <sub>b</sub> +2.3	t <sub>b</sub> +4	ms

### total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>DD</sub>	Supply current	PSON = 5 V		1	mA	

TYPICAL CHARACTERISTICS

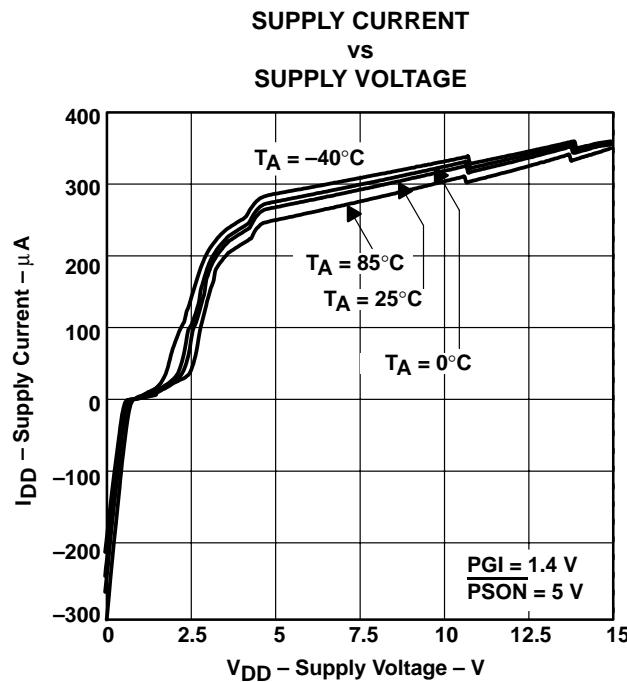


Figure 2

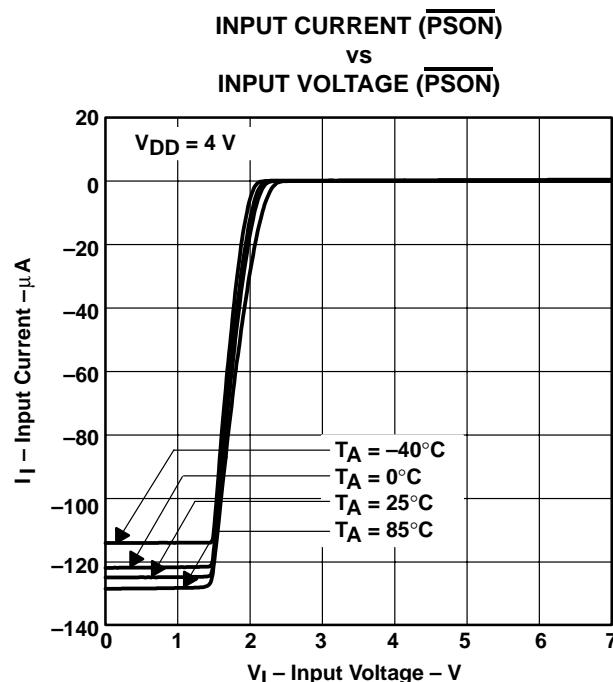


Figure 3

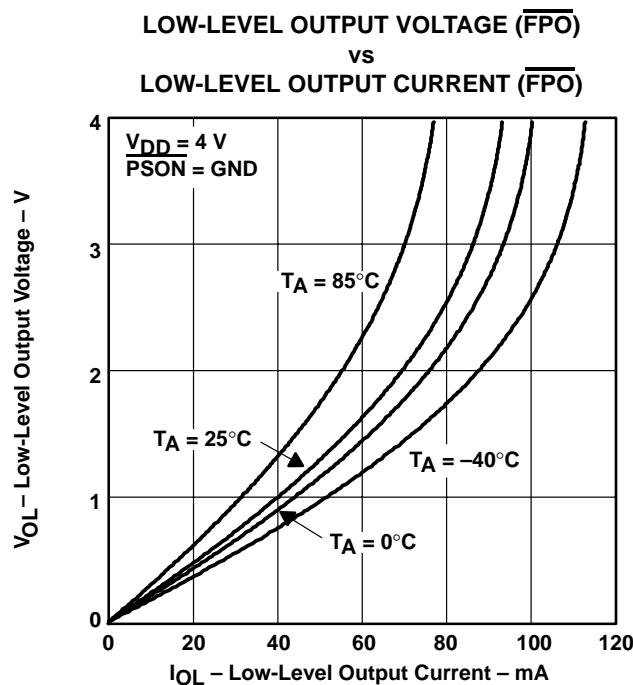


Figure 4

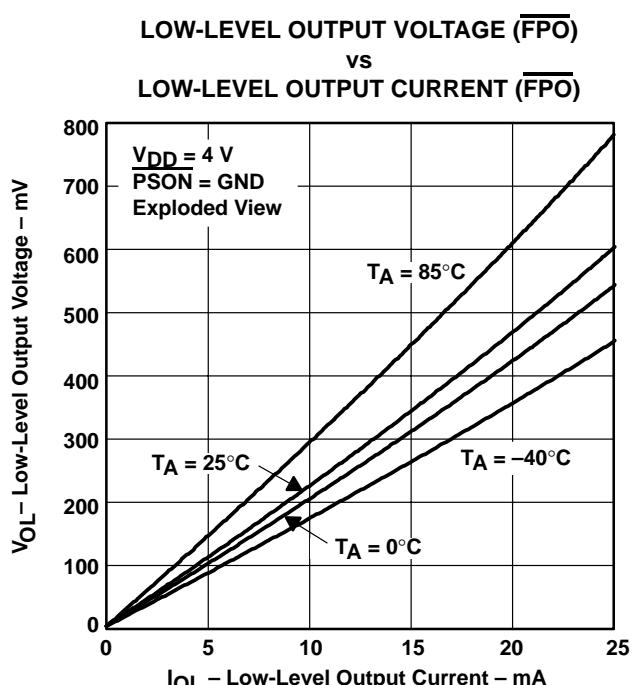


Figure 5

# TPS3510, TPS3511 PC POWER SUPPLY SUPERVISORS

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## TYPICAL CHARACTERISTICS

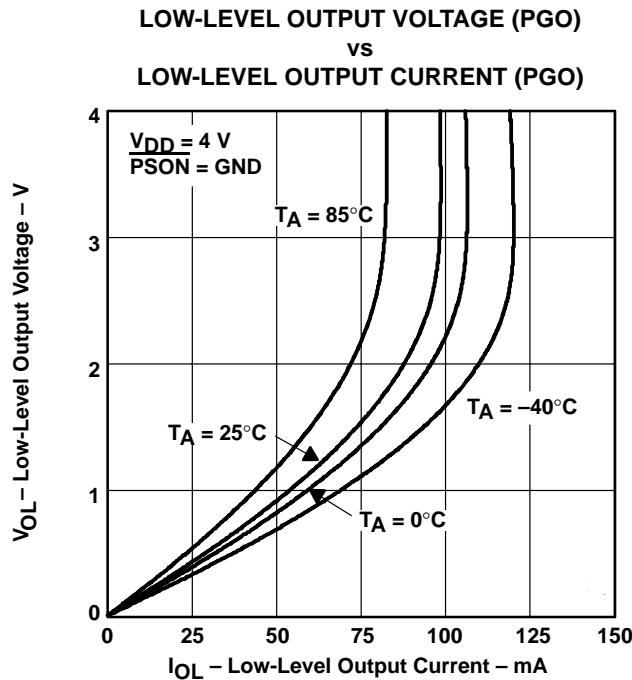


Figure 6

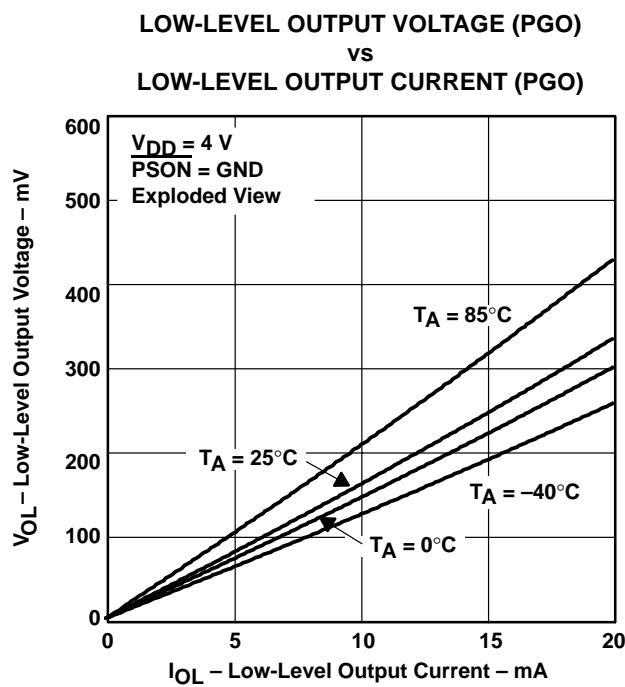


Figure 7

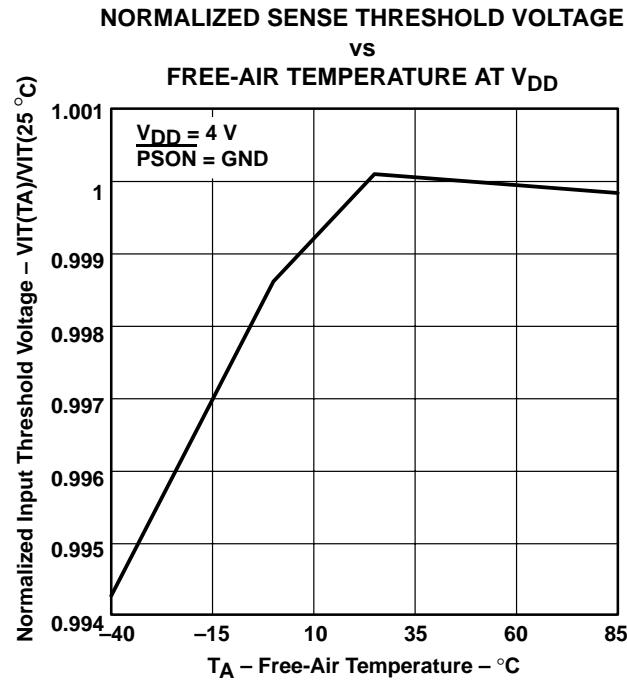


Figure 8

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS3510D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3510DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3510DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3510DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3510P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS3510PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS3511D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3511DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3511DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3511DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3511P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS3511PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

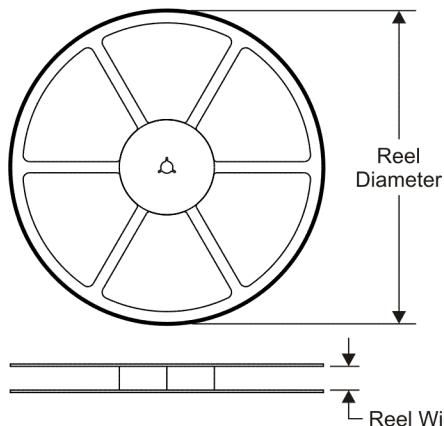
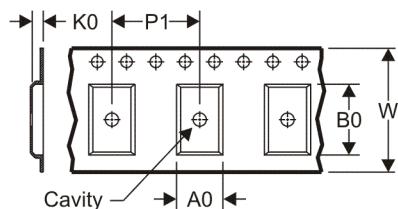
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

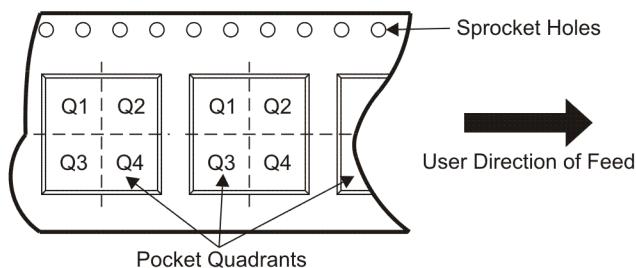
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


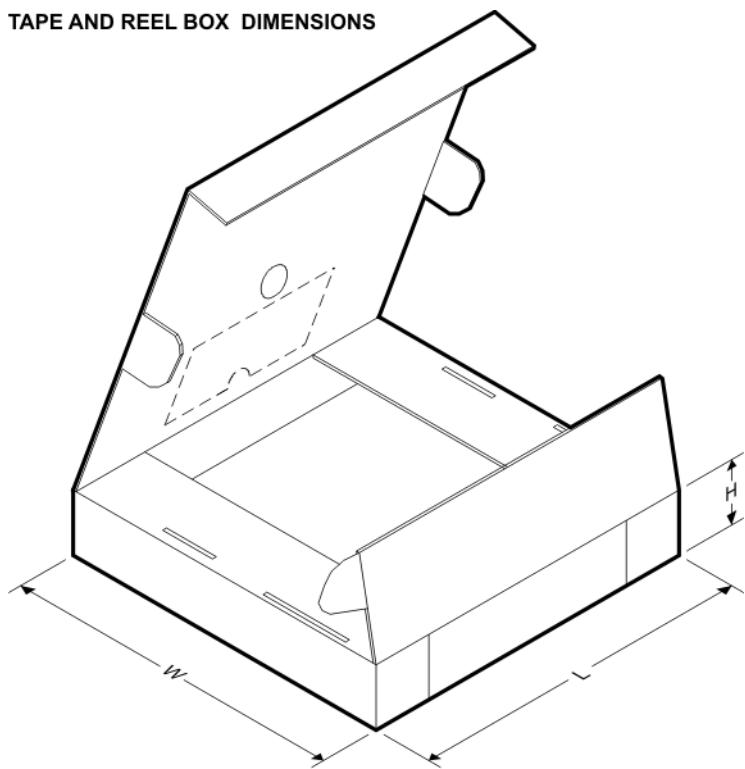
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3510DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3511DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

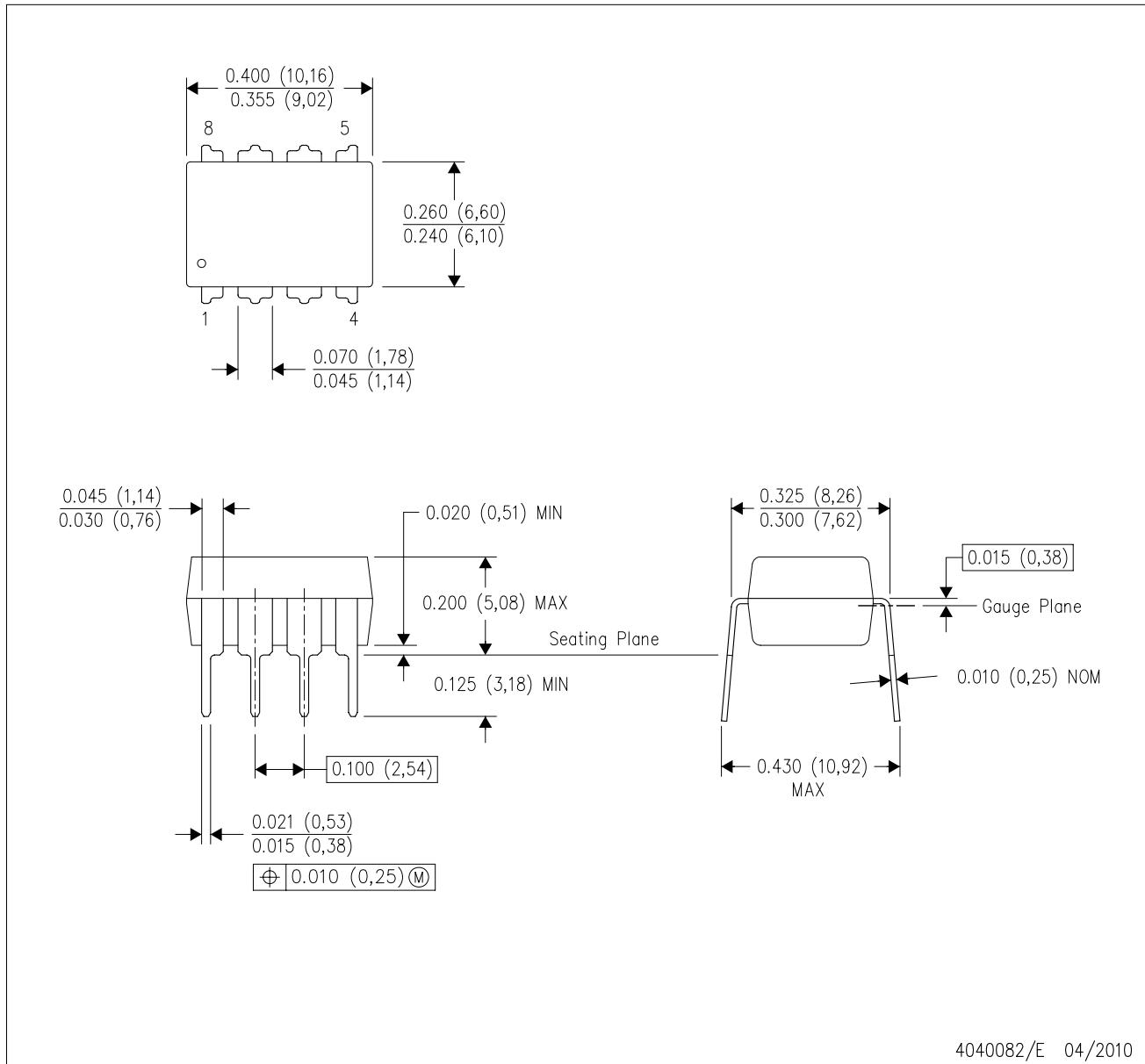


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3510DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS3511DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

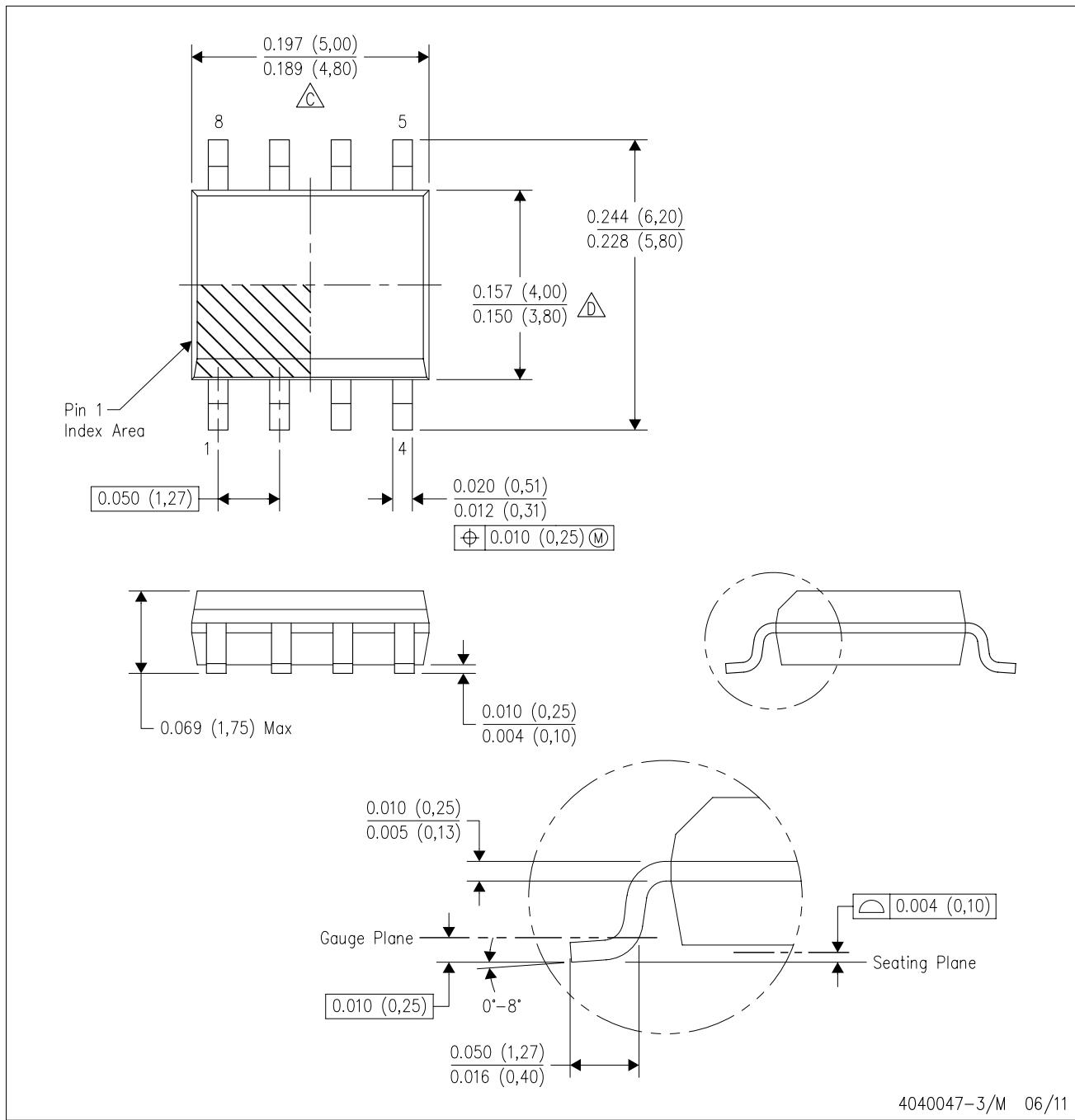


NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 variation BA.

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D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

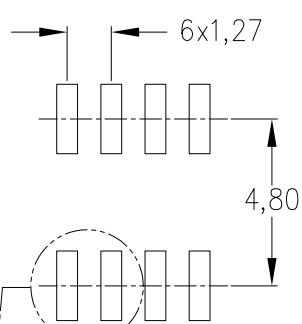
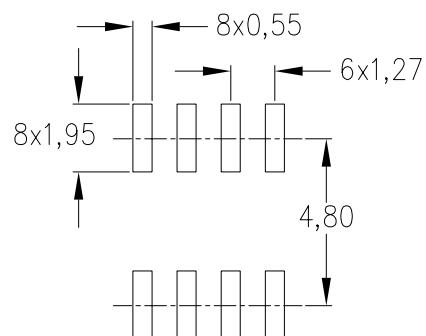
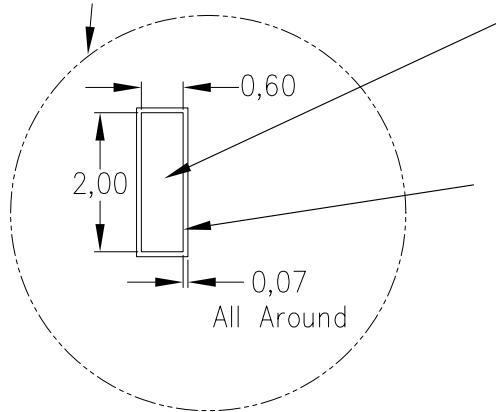
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-2/D 06/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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