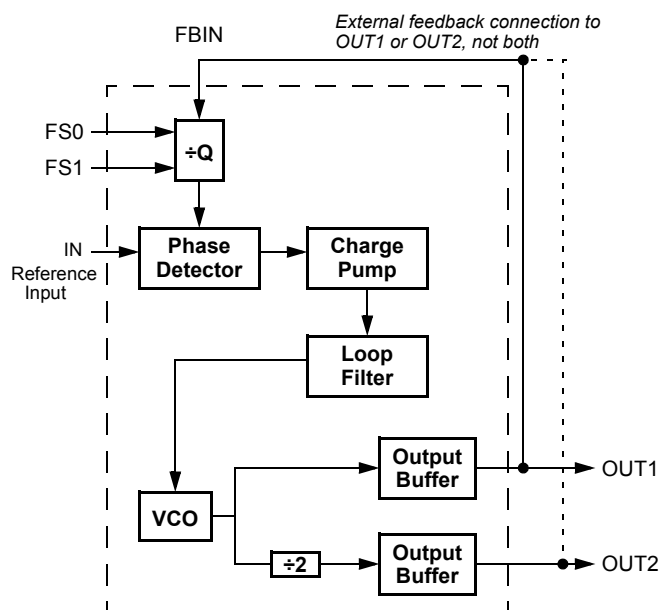# Frequency Multiplier and Zero Delay Buffer

## Features

- 90 ps typical jitter OUT2
- 200 ps typical jitter OUT1
- 65 ps typical output-to-output skew
- 90 ps typical propagation delay
- Voltage range: 3.3 V ± 5%, or 5 V ± 10%
- Output frequency range: 5 MHz to 133 MHz
- Two outputs
- Configuration options allow various multiplications of the reference frequency – refer to Configuration Options to determine the specific option which meets your multiplication needs
- Available in 8-pin SOIC package

## Configuration Options

| FBIN | FS0 | FS1 | OUT1 | OUT2 |
|------|-----|-----|------|------|
| OUT1 | 0 | 0 | 2 × REF | REF |
| OUT1 | 1 | 0 | 4 × REF | 2 × REF |
| OUT1 | 0 | 1 | REF | REF/2 |
| OUT1 | 1 | 1 | 8 × REF | 4 × REF |
| OUT2 | 0 | 0 | 4 × REF | 2 × REF |
| OUT2 | 1 | 0 | 8 × REF | 4 × REF |
| OUT2 | 0 | 1 | 2 × REF | REF |
| OUT2 | 1 | 1 | 16 × REF | 8 × REF |

## Logic Block Diagram

# Contents

## Pinouts

**Figure 1. 8-pin SOIC pinout**

```
FBIN  ▭   1        8   ▭  OUT2
IN    ▭   2        7   ▭  VDD
GND   ▭   3        6   ▭  OUT1
FS0   ▭   4        5   ▭  FS1
```
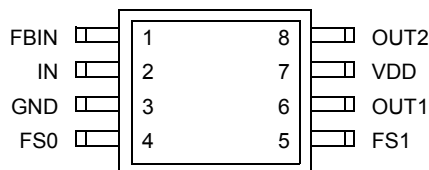
## Pin Definitions

| Pin Name | Pin No. | Pin Type | Pin Description |
|---|---|---|---|
| IN | 2 | I | Reference Input: The output signals are synchronized to this signal. |
| FBIN | 1 | I | Feedback Input: This input must be fed by one of the outputs (OUT1 or OUT2) to ensure proper functionality. If the trace between FBIN and the output pin being used for feedback is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations are synchronized to the REF signal input (IN). |
| OUT1 | 6 | O | Output 1: The frequency of the signal provided by this pin is determined by the feedback signal connected to FBIN, and the FS0:1 inputs (see Configuration Options on page 1). |
| OUT2 | 8 | O | Output 2: The frequency of the signal provided by this pin is one-half of the frequency of OUT1. See Configuration Options on page 1. |
| VDD | 7 | P | Power Connections: Connect to 3.3V or 5V. This pin should be bypassed with a 0.1-$\mu$F decoupling capacitor. Use ferrite beads to help reduce noise for optimal jitter performance. |
| GND | 3 | P | Ground Connection: Connect all grounds to the common system ground plane. |
| FS0:1 | 4, 5 | I | Function Select Inputs: Tie to $V_{DD}$ (HIGH, 1) or GND (LOW, 0) as desired per Configuration Options on page 1. |

## Overview

The CY2302 is a two-output zero delay buffer and frequency multiplier. It provides an external feedback path allowing maximum flexibility when implementing the Zero Delay feature. This is explained further in the sections of this datasheet titled, How to Implement Zero Delay, and Inserting Other Devices in Feedback Path.

The CY2302 is a pin-compatible upgrade of the Cypress W42C70-01. The CY2302 addresses some application dependent problems experienced by users of the older device.

**Figure 2. Schematic/Suggested Layout**
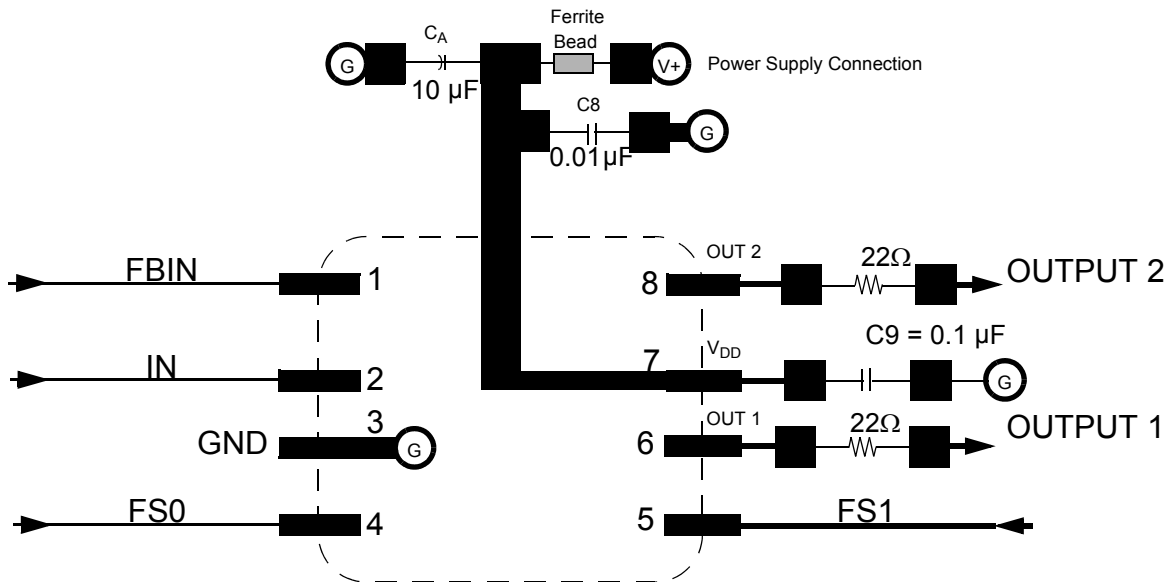


### How to Implement Zero Delay

Typically, Zero Delay Buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described as follows.

External feedback is the trait that allows for this compensation. The PLL on the ZDB causes the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feedback and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may also be implemented by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

### Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) that is put into the feedback path.

Referring to Figure 2, if the traces between the ASIC/Buffer and the destination of the clock signal(s) (A) are equal in length to the

trace between the buffer and the FBIN pin, the signals at the destination(s) device is driven HIGH at the same time when the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is more complex however, as any propagation delay from the ZDB output to the ASIC/Buffer output must be accounted for.

**Figure 3. Six Output Buffer in the Feedback Path**
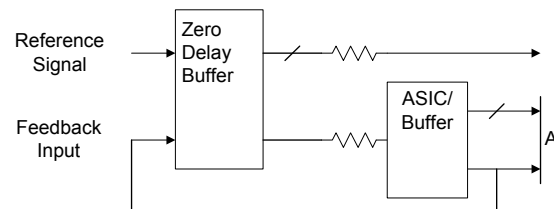


### Phase Alignment

In cases where OUT1 (i.e., the higher frequency output) is connected to FBIN input pin the output OUT2 rising edges may be either 0 or 180° phase aligned to the IN input waveform (as set randomly when the input and/or power is supplied). If OUT2 is desired to be rising-edge aligned to the IN input's rising edge, then connect the OUT2 (i.e., the lowest frequency output) to the FBIN pin. This set-up provides a consistent input-output phase relationship.

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| Parameter | Description | Rating | Unit |
|---|---|---|---|
| $V_{DD}$, $V_{IN}$ | Voltage on any pin with respect to GND | –0.5 to +7.0 | V |
| $T_{STG}$ | Storage temperature | –65 to +150 | °C |
| $T_A$ | Ambient operating temperature, commercial | 0 to +70 | °C |
| | Ambient operating temperature, industrial | –40 to +85 | °C |
| $T_B$ | Ambient temperature under bias | –55 to +125 | °C |
| $P_D$ | Power dissipation | 0.5 | W |

## DC Electrical Characteristics

$T_A$ = 0 °C to 70 °C or –40 °C to 85 °C, $V_{DD}$ = 3.3 V ±5%

| Parameter | Description | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Unloaded, 100 MHz | – | 17 | 35 | mA |
| $V_{IL}$ | Input low voltage | – | – | – | 0.8 | V |
| $V_{IH}$ | Input high voltage | – | 2.0 | – | – | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 12 mA | – | – | 0.4 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -12 mA | 2.4 | – | – | V |
| $I_{IL}$ | Input low current | $V_{IN}$ = 0V | –40 | – | 5 | μA |
| $I_{IH}$ | Input high current | $V_{IN}$ = $V_{DD}$ | – | – | 5 | μA |

## DC Electrical Characteristics

$T_A$ = 0 °C to 70 °C or –40 °C to 85 °C, $V_{DD}$ = 5 V ±10%

| Parameter | Description | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Unloaded, 100 MHz | – | 37 | 50 | mA |
| $V_{IL}$ | Input low voltage | – | – | – | 0.8 | V |
| $V_{IH}$ | Input high voltage | – | 2.0 | – | – | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 12 mA | – | – | 0.4 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -12 mA | 2.4 | – | – | V |
| $I_{IL}$ | Input low current | $V_{IN}$ = 0 V | –80 | – | 5 | μA |
| $I_{IH}$ | Input high current | $V_{IN}$ = $V_{DD}$ | – | – | 5 | μA |

## AC Electrical Characteristics

$T_A$ = 0 °C to +70 °C or –40 °C to 85 °C, $V_{DD}$ = 3.3 V ± 5% [1]

| Parameter | Description | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency [2] | – | 5 | – | 133 | MHz |
| $f_{OUT}$ | Output Frequency | OUT1 15-pF load | 10 | – | 133 | MHz |
| $t_R$ | Output Rise Time | 0.8 V to 2.0 V, 15-pF load | – | – | 3.5 | ns |
| $t_F$ | Output Fall Time | 2.0 V to 0.8 V, 15-pF load | – | – | 2.5 | ns |
| $t_{ICLKR}$ | Input Clock Rise Time [3] | – | – | – | 10 | ns |
| $t_{ICLKF}$ | Input Clock Fall Time [3] | – | – | – | 10 | ns |
| $t_D$ | Duty Cycle | 15-pF load[4] | 40 | 50 | 60 | % |
| $t_{LOCK}$ | PLL Lock Time | Power supply stable | – | – | 1.0 | ms |
| $t_{JC}$ | Jitter, Cycle-to-Cycle | OUT1, $f_{OUT}$ >30 MHz | – | 200 | 300 | ps |
| | | OUT2, $f_{OUT}$ >30 MHz | – | 90 | 300 | ps |
| $t_{DC}$ | Die Out Time[5] | – | 100 | – | – | Clock Cycles |
| $t_{SKEW}$ | Output-output Skew[6] | – | – | 65 | 250 | ps |
| $t_{PD}$ | Propagation Delay[6] | – | –350 | 90 | 350 | ps |

**Notes**
1. All AC specifications are measured with a 50Ω transmission line, load terminated with 50 Ω to 1.4 V.
2. Input frequency is limited by output frequency range and input to output frequency multiplication factor (which is determined by circuit configuration).
3. Longer input rise and fall time degrades skew and jitter performance.
4. Duty cycle is measured at 1.4 V.
5. 33 MHz reference input suddenly stopped (0 MHz). Number of cycles provided prior to output falling to <16 MHz.
6. Skew is measured at 1.4 V on rising edges.

## AC Electrical Characteristics

$T_A$ = 0 °C to +70 °C or –40 °C to 85 °C, $V_{DD}$ = 5.0 V ± 10% [7]

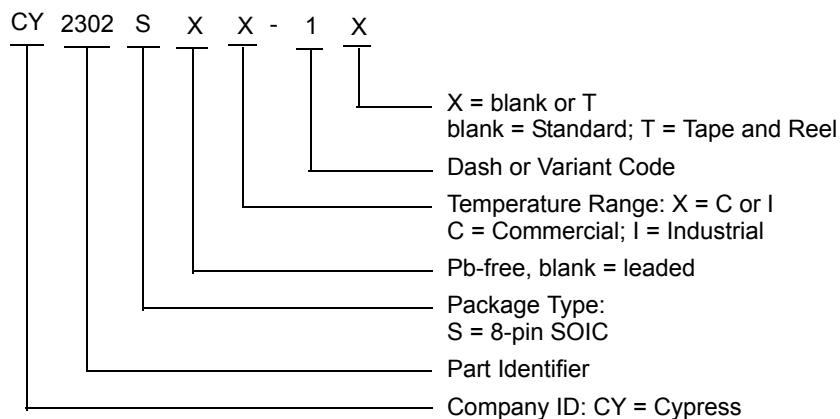| Parameter | Description | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency [8] | – | 5 | – | 133 | MHz |
| $f_{OUT}$ | Output Frequency | OUT1 15-pF load | 10 | – | 133 | MHz |
| $t_R$ | Output Rise Time | 0.8 V to 2.0 V, 15-pF load | – | – | 2.5 | ns |
| $t_F$ | Output Fall Time | 2.0 V to 0.8 V, 15-pF load | – | – | 1.5 | ns |
| $t_{ICLKR}$ | Input Clock Rise Time [9] | – | – | – | 10 | ns |
| $t_{ICLKF}$ | Input Clock Fall Time [9] | – | – | – | 10 | ns |
| $t_D$ | Duty Cycle | 15-pF load [10, 11] | 40 | 50 | 60 | % |
| $t_{LOCK}$ | PLL Lock Time | Power supply stable | – | – | 1.0 | ms |
| $t_{JC}$ | Jitter, Cycle-to-Cycle | OUT1, $f_{OUT}$ >30 MHz | – | 200 | 300 | ps |
| | | OUT2, $f_{OUT}$ >30 MHz | – | 90 | 300 | ps |
| $t_{DC}$ | Die out time [12] | – | 100 | – | – | Clock cycles |
| $t_{SKEW}$ | Output-output Skew [13] | – | – | 65 | 250 | ps |
| $t_{PD}$ | Propagation Delay [13] | – | –350 | 90 | 350 | ps |

**Notes**
7. All AC specifications are measured with a 50Ω transmission line, load terminated with 50 Ω to 1.4 V.
8. Input frequency is limited by output frequency range and input to output frequency multiplication factor (which is determined by circuit configuration).
9. Longer input rise and fall time degrades skew and jitter performance.
10. Duty cycle is measured at 1.4 V.
11. Duty Cycle measured at 120 MHz. For 133 MHz, degrades to 35/65 worst case.
12. 33 MHz reference input suddenly stopped (0 MHz). Number of cycles provided prior to output falling to <16 MHz.
13. Skew is measured at 1.4 V on rising edges.

## Ordering Information

| Ordering Code | Package Type | Temperature Grade |
|---|---|---|
| **Pb-free** | | |
| CY2302SXC-1 | 8-pin SOIC | Commercial (0 °C to 70 °C) |
| CY2302SXC-1T | 8-pin SOIC – Tape and Reel | Commercial (0 °C to 70 °C) |
| CY2302SXI-1 | 8-pin SOIC | Industrial (–40 °C to 85 °C) |
| CY2302SXI-1T | 8-pin SOIC – Tape and Reel | Industrial (–40 °C to 85 °C) |

## Ordering Code Definitions

CY  2302  S  X  X  -  1  X

X = blank or T
blank = Standard; T = Tape and Reel

Dash or Variant Code

Temperature Range: X = C or I
C = Commercial; I = Industrial

Pb-free, blank = leaded

Package Type:
S = 8-pin SOIC

Part Identifier

Company ID: CY = Cypress

## Package Diagram

**Figure 4. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066**



1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.

2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME

3. REFERENCE JEDEC MS-012

4. PACKAGE WEIGHT 0.07gms

| PART # | |
|---|---|
| S08.15 | STANDARD PKG |
| SZ08.15 | LEAD FREE PKG |
| SW8.15 | LEAD FREE PKG |
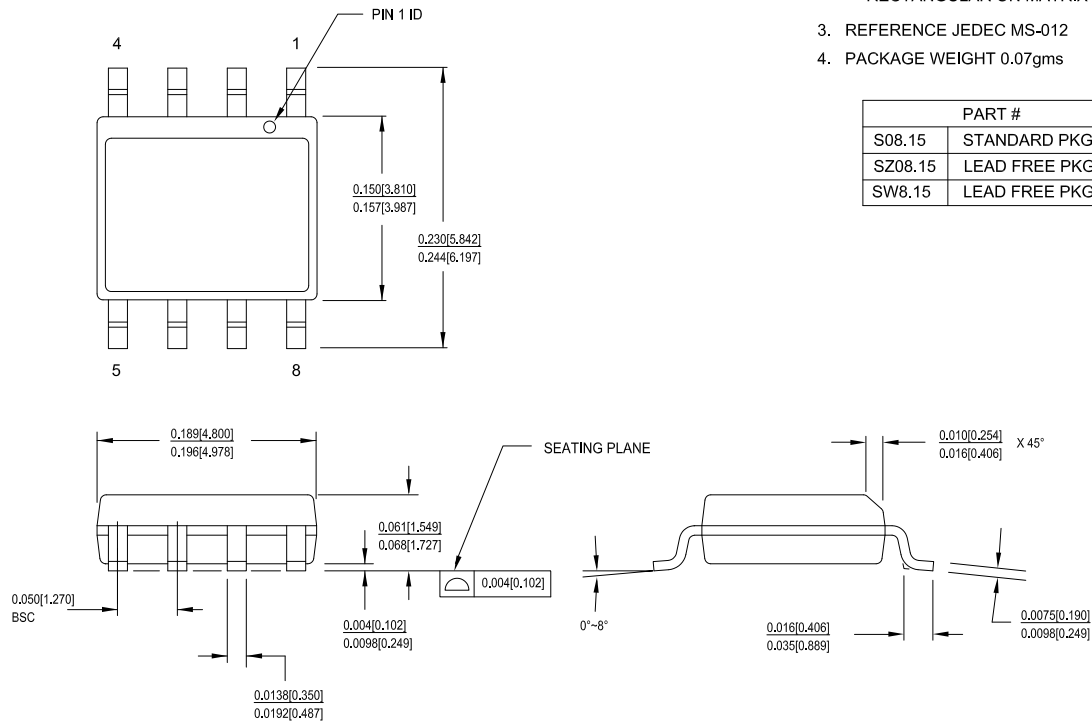
51-85066 *F

## Acronyms

| Acronym | Description |
|---------|-------------|
| FBK | Feedback |
| PLL | Phase Locked Loop |
| MUX | Multiplexer |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-----------------|--------|-----------------|
| °C | degree Celsius | µW | microwatt |
| dB | decibel | mA | milliampere |
| fC | femtocoulomb | mm | millimeter |
| fF | femtofarad | ms | millisecond |
| Hz | hertz | mV | millivolt |
| KB | 1024 bytes | nA | nanoampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | nV | nanovolt |
| kΩ | kilohm | Ω | ohm |
| MHz | megahertz | ppm | parts per million |
| MΩ | megaohm | pA | picoampere |
| µA | microampere | pF | picofarad |
| µF | microfarad | pp | peak-to-peak |
| µH | microhenry | ps | picosecond |
| µs | microsecond | sps | samples per second |
| µV | microvolt | σ | sigma: one standard deviation |
| µVrms | microvolts root-mean-square | | |

## Document History Page

<table>
<tr><td colspan="5">Document Title: CY2302, Frequency Multiplier and Zero Delay Buffer<br>Document Number: 38-07154</td></tr>
<tr><th>Revision</th><th>ECN</th><th>Orig. of Change</th><th>Submission Date</th><th>Description of Change</th></tr>
<tr><td>**</td><td>110264</td><td>SZV</td><td>12/18/01</td><td>Change from Spec number: 38-00794 to 38-07154</td></tr>
<tr><td>*A</td><td>394695</td><td>RGL</td><td>See ECN</td><td>Added typical char data<br>Added Pb-free devices<br>Added phase alignment paragraph</td></tr>
<tr><td>*B</td><td>2761988</td><td>KVM</td><td>09/10/09</td><td>Added temperature values to Absolute Maximum Ratings table.<br><br>Removed CY2302SI-1T from the Ordering Information table.<br>Added temperature values to Ordering Information table.</td></tr>
<tr><td>*C</td><td>2894970</td><td>KVM</td><td>03/23/2010</td><td>Updated Ordering Information:<br>Removed inactive parts.<br><br>Updated Package Diagram.</td></tr>
<tr><td>*D</td><td>2907904</td><td>KVM</td><td>04/08/2010</td><td>Updated Ordering Information:<br>Removed inactive parts.</td></tr>
<tr><td>*E</td><td>3204657</td><td>BASH</td><td>03/24/2011</td><td>Added Ordering Code Definitions under Ordering Information.<br><br>Added Acronyms and Units of Measure.</td></tr>
<tr><td>*F</td><td>4348705</td><td>CINM</td><td>04/16/2014</td><td>Updated Package Diagram:<br>spec 51-85066 – Changed revision from *D to *F.<br><br>Updated in new template.<br><br>Completing Sunset Review.</td></tr>
</table>

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

| | | |
|---|---|---|
| **Products** | | **PSoC® Solutions** |
| Automotive | cypress.com/go/automotive | psoc.cypress.com/solutions |
| Clocks & Buffers | cypress.com/go/clocks | PSoC 1 \| PSoC 3 \| PSoC 4 \| PSoC 5LP |
| Interface | cypress.com/go/interface | |
| Lighting & Power Control | cypress.com/go/powerpsoc | **Cypress Developer Community** |
| | cypress.com/go/plc | Community \| Forums \| Blogs \| Video \| Training |
| Memory | cypress.com/go/memory | |
| PSoC | cypress.com/go/psoc | **Technical Support** |
| Touch Sensing | cypress.com/go/touch | cypress.com/go/support |
| USB Controllers | cypress.com/go/USB | |
| Wireless/RF | cypress.com/go/wireless | |

All products and company names mentioned in this document may be the trademarks of their respective holders.