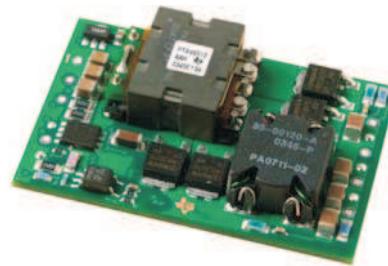


DUAL COMPLEMENTARY-OUTPUT DC/DC CONVERTER FOR DSL

Check for Samples: [PTB48510](#), [PTB48511](#)

FEATURES

- Dual Complementary Outputs (± 5 V, ± 12 V, or ± 15 V)
- Input Voltage Range: 36 V to 75 V
- On/Off Enable for Sequencing
- 1500 V_{DC} Isolation
- Overcurrent Protection
- Overvoltage Protection (PTB48511 only)
- Over Temperature Shutdown
- Undervoltage Lockout
- Temperature Range: -40°C to 85°C
- Industry Standard Outline
- Fixed Frequency Operation
- Synchronizes with PTB48500
- Powers Line Drivers for AC-7 and Other xDSL Chipsets
- Safety Approvals:
 - EN 60950
 - UL/cUL 60950



DESCRIPTION

The PTB4851x series of isolated DC/DC converter modules produce a complementary pair of regulated supply voltages for powering line-driver devices in xDSL telecom applications. The modules operate from a standard telecom (-48 V) central office (CO) supply and can provide up to a 72 W of power in a balanced load configuration.

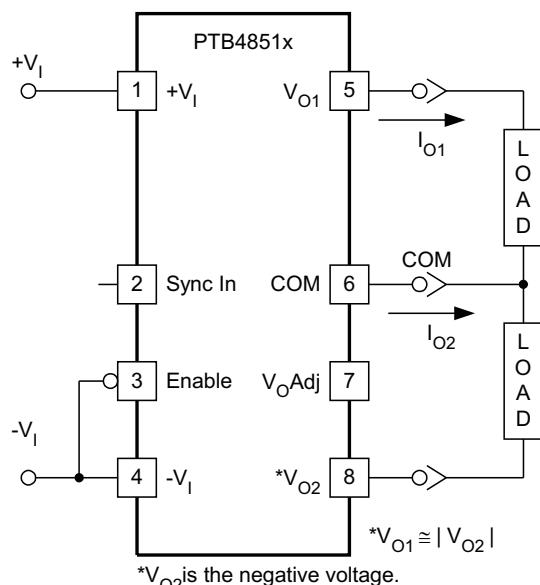
The A-suffix module (± 5 V) is designed to power the line driver devices for the AC-7 ADSL chipset. Other voltage options powers other analog applications requiring a complementary supply with relatively balanced loads.

Both the PTB48510 and PTB48511 include an “on/off” enable control, output current limit, over-temperature protection, and input under-voltage lockout (UVLO). The PTB48511 adds output overvoltage protection (OVP).

The control inputs, *Enable* and *Sync In*, are compatible with the *EN Out* and *Sync Out* signals of the PTB48500 DC/DC converter. This allows the power-up and switching frequency of the PTB4851x modules to be directly controlled from a PTB48500. Together the PTB48500 and PTB4851x converters meet all the system power and sequencing requirements of the AC- ADSL chipset.

The PTB4851x uses double-sided surface mount technology construction. The package size is based on the industry standard outline and does not require a heatsink. Both through-hole and surface mount pin configurations are available.

STAND-ALONE APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PTB48510
PTB48511

SLTS219F –FEBRUARY 2004–REVISED MARCH 2007

www.ti.com

ORDERING INFORMATION

BASE DEVICE NUMBER. (PTB4851xxx)		OUTPUT VOLTAGE (PTB4851xx)		PACKAGE OPTIONS (PT4851xx)		
ORDER PREFIX	DESCRIPTION	CODE	VOLTAGE (V)	CODE	DESCRIPTION	PACKAGE REFERENCE ⁽¹⁾
PTB48510xxx	Basic model	A	± 5	AH	Horizontal T/H	ERK
PTB48511xxx	Adds output overvoltage protection ⁽²⁾	B	± 12	AS	SMD, Standard ⁽³⁾	ERL
		C	± 15 ⁽⁴⁾			

(1) Reference the applicable package reference drawing for the dimensions and PC board layout

(2) Output overvoltage protection

(3) Standard option specifies 63/37, Sn/Pb pin solder material

(4) ± 15 -V output is not available with the PTB48511**Environmental and General Specifications**(Unless otherwise stated, all voltages are with respect to V_{I2})

			VALUE	UNIT
V_I	Input Voltage Range	Over output load range	36 to 75	V_{DC}
	Isolation Voltage	Input-output/input/case	1500	V
	Capacitance	Input to output	1500	pF
	Resistance	Input to output	10	$m\Omega$
T_A	Operating Temperature Range	Over V_I Range	-40 to 85	$^{\circ}C$
OTP	Over-Temperature Protection	Shutdown threshold	115 ⁽¹⁾	
		Hysteresis	10	
T_{reflow}	Solder Reflow Temperature	Surface temperature of module body or pins	235 ⁽²⁾	
T_s	Storage Temperature		-55 to 125	
Mechanical Shock	Per Mil-STD-883D, Method 2002.3 1 ms, 1/2 Sine, mounted	T/H	500	G
		SMD	250	
Mechanical Vibration Mil-STD-883D	Mil-STD-883D, Method 2007.2 20-2000 Hz	T/H	10	G
		SMD	5	
Weight			28	grams
Flammability	Meets UL 94V-O			

(1) This parameter is assured by design.

(2) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, $T_A = 25^\circ\text{C}$, $V_I = 48\text{ V}$, $C_I = 0\text{ }\mu\text{F}$, $C_O = 0\text{ }\mu\text{F}$, $I_{O1} = I_{O2} = 3.25\text{ A}$ maximum)

PARAMETER	TEST CONDITIONS	PTB4851xA			UNIT
		MIN	TYP	MAX	
P_O	Output Power	Total output power from V_{O1} or V_{O2}	0	65 ⁽¹⁾	W
I_{O1}, I_{O2}	Output Current	Over V_I range, $I_{O1} \leq 0.1\text{ A}$ or $I_{O2} \leq 0.1\text{ A}$	0	6.5 ⁽²⁾	A
$I_{O1} - I_{O2}$	Output Load Imbalance	$I_{O1} \leq 0.1\text{ A}$ or $I_{O2} \leq 0.1\text{ A}$	0	1 ⁽³⁾	A
V_{O1}, V_{O2}	Output Voltage	Includes set point, line, load, $I_{O1} \leq 0.1\text{ A}$ or $I_{O2} \leq 0.1\text{ A}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	4.75 ⁽²⁾	5	5.25 ⁽²⁾ V
$\Delta R_{\text{Reg,temp}}$	Temperature Variation	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $I_{O1} \leq 0.1\text{ A}$ or $I_{O2} \leq 0.1\text{ A}$	V_{O1} V_{O2}	± 1 ± 1	$\%V_O$
$\Delta R_{\text{Reg,line}}$	Line Regulation	Over V_I range, balanced load	V_{O1} or V_{O2}	± 0.1	
$\Delta R_{\text{Reg,load}}$	Load Regulation	Over I_{O1}, I_{O2} range, balanced load	V_{O1} or V_{O2}	± 0.2	± 0.4 $\%V_O$
η	Efficiency			86%	
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth, $C_O = 10\text{-}\mu\text{F}$ tantalum capacitor		20	30 ⁽⁴⁾ mV _{pp}
t_{tr}	Transient Response	0.11 A/ μs load step, 50% to 75% I_{O1} or I_{O2} maximum		30	μs
ΔV_{tr}		V_{O1} or V_{O2} overshoot/undershoot		± 1.0	$\%V_O$
$I_{O\text{trip}}$	Overcurrent Threshold	$V_I = 36\text{ V}$, reset followed by auto-recovery	6.8	7.5	10 A
$V_{O1(\text{trip})}, V_{O2(\text{trip})}$	Overvoltage Threshold	Outputs latched off ⁽⁵⁾	PTB48510 PTB48511	NA 5.9	NA 7 V
	Short Circuit Current	Continuous overcurrent trip, $I_{O1} = I_{O2}$	$I_{O1(\text{pk})}$	12.5	A
			$I_{O2(\text{pk})}$ Duty	10%	
$V_{O1(\text{adj})}, V_{O2(\text{adj})}$	Output Voltage Adjust Range	V_{O1} or V_{O2} adjust simultaneously		3.5	5.5 V
f_S	Switching Frequency	Over V_I and I_O ranges	440	470 ⁽⁶⁾	500 kHz
$V_I \text{ on}$	Undervoltage lockout	V_I increasing		33	V
$V_I \text{ off}$		V_I decreasing		32	
V_{IH}	On/Off Enable (pin 3) High-level input voltage	Referenced to V_I (pin 4)		3.6	V
V_{IL}	Low-level input voltage		-0.2	0.8	
I_{IL}	Low-level input current			-1	
$I_I \text{ standby}$	Standby Input Current	Pin 3 connected		2	mA
t_{ON}	Start-up Time	$I_{O1} \leq 0.1\text{ A}$ or $I_{O2} \leq 0.1\text{ A}$, V_{O1} or V_{O2} rising 0 to 0.95 (typ)	6	10	22 ms
C_I	Internal Input Capacitance			3	μF
C_O	External Output Capacitance	Capacitance from either output to COM (pin 6)	0	5000 ⁽⁸⁾	μF
MTBF	Reliability	Per Telcordia SR-332 50% stress, $T_A = 40^\circ\text{C}$, ground benign	PTB48510A PTB48511A	2.7 2.5	10^6 hrs

- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
- (2) Under balanced load conditions, load current flowing out of V_{O1} is balanced to within $\pm 0.1\text{ A}$ of that flowing into V_{O2} .
- (3) A load imbalance is the difference in current flowing from V_{O1} to V_{O2} . The module can operate with a higher imbalance but with reduced specifications.
- (4) Output voltage ripple is measured with a 10- μF tantalum capacitor connected from V_{O1} (pin 5) or V_{O2} (pin 8), to COM (pin 6).
- (5) If the overvoltage threshold is exceeded by either regulated output the module will shut down, turning both outputs off. This is a latched condition, which can only be reset by removing and then re-applying the module's input power.
- (6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
- (7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to V_I . The open-circuit voltage is 5 V maximum. If it is left open circuit the converter operates when input power is applied.
- (8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, $T_A = 25^\circ\text{C}$, $V_I = 48\text{ V}$, $C_I = 0\text{ }\mu\text{F}$, $C_O = 0\text{ }\mu\text{F}$, $I_{O1} = I_{O2} = 3.25\text{ A}$ maximum)

PARAMETER	TEST CONDITIONS	PTB4851xB			UNIT
		MIN	TYP	MAX	
P_O	Output Power	0	72 ⁽¹⁾	72 ⁽¹⁾	W
I_{O1} or I_{O2}	Output Current	0	3 ⁽²⁾	3 ⁽²⁾	A
$I_{O1} - I_{O2}$	Output Load Imbalance	0	1 ⁽³⁾	1 ⁽³⁾	A
V_{O1} or V_{O2}	Output Voltage	11.6 ⁽²⁾	12	12.4 ⁽²⁾	V
ΔR_{temp}	Temperature Variation	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $I_{O1} \leq 0.1\text{ A}$ or $I_{O2} \leq 0.1\text{ A}$	V_{O1} or V_{O2}	± 1	% V_O
ΔR_{line}	Line Regulation	Over V_I range, balanced load	V_{O1} or V_{O2}	± 0.05	% V_O
ΔR_{load}	Load Regulation	Over I_{O1} or I_{O2} range, balanced load	V_{O1} or V_{O2}	± 0.1	% V_O
η	Efficiency			89%	
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth, $C_O = 10\text{ }\mu\text{F}$ tantalum capacitor		20	80 ⁽⁴⁾
t_{tr}	Transient Response	0.1 A/ μs load step, 50% to 75% I_{O1} or I_{O2} maximum		30	μs
ΔV_{tr}		V_{O1} or V_{O2} overshoot/undershoot		± 1	% V_O
$I_{O\text{trip}}$	Overcurrent Threshold	$V_I = 36\text{ V}$, reset followed by auto-recovery		3.3	A
$V_{O1(\text{trip})}$, $V_{O2(\text{trip})}$	Overvoltage Threshold	Outputs latched off ⁽⁵⁾	PTB48510A	NA	NA
			PTB48511A	14	15.8
	Short Circuit Current	Continuous overcurrent trip, $I_{O1} = I_{O2}$	$I_{O1(\text{pk})}$	6	A
			Duty	10%	
$V_{O1(\text{adj})}$, $V_{O2(\text{adj})}$	Output Voltage Adjust Range	V_{O1} and V_{O2} adjust simultaneously		6.5	13.4
f_S	Switching Frequency	Over V_I and I_O ranges		440	480 ⁽⁶⁾
V_I on	Under-Voltage Lockout	V_I increasing		33	V
V_I off		V_I decreasing		32	
V_{IH}	On/Off Enable (pin 3)	Referenced to V_I (pin 4)		3.6	V
V_{IL}	High-level input voltage			-0.2	
I_{IL}	Low-level input voltage			-1	
I_I standby	Standby Input Current	Pin 3 open circuit		2	mA
t_{ON}	Start-up Time	$I_{O1} \leq 1\text{ A}$ or $I_{O2} \leq 1\text{ A}$, V_{O1} or V_{O2} rising 0 to 0.95 (typ)		6	ms
C_I	Internal Input Capacitance			3	μF
C_O	External Output Capacitance	Capacitance from either output to COM (pin 6)		0	3000 ⁽⁸⁾
MTBF	Reliability	Per Telcordia SR-332 50% stress, $T_A = 40^\circ\text{C}$, ground benign	PTB48510B	2.8	10^6 Hrs
			PTB48511B	2.5	

- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
- (2) Under balanced load conditions, load current flowing out of V_{O1} is balanced to within $\pm 0.1\text{ A}$ of that flowing into V_{O2} .
- (3) A load imbalance is the difference in current flowing from V_{O1} to V_{O2} . The module can operate with a higher imbalance but with reduced specifications.
- (4) Output voltage ripple is measured with a $10\text{ }\mu\text{F}$ tantalum capacitor connected from V_{O1} (pin 5) or V_{O2} (pin 8), to COM (pin 6).
- (5) If the overvoltage threshold is exceeded by either regulated output the module will shut down, turning both outputs off. This is a latched condition, which can only be reset by removing and then re-applying the module's input power.
- (6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
- (7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to V_I . The open-circuit voltage is 5 V maximum. If it is left open circuit the converter operates when input power is applied.
- (8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, $T_A = 25^\circ\text{C}$, $V_I = 48\text{ V}$, $C_I = 0\text{ }\mu\text{F}$, $C_O = 0\text{ }\mu\text{F}$, $I_{O1} = I_{O2} = 3.25\text{ A}$ maximum)

PARAMETER	TEST CONDITIONS	PTB4851xC			UNIT
		MIN	TYP	MAX	
P_O	Output Power	0	66 ⁽¹⁾	66 ⁽¹⁾	W
I_{O1} or I_{O2}	Output Current	0	2.2 ⁽²⁾	2.2 ⁽²⁾	A
$I_{O1} - I_{O2}$	Output Load Imbalance	0	1 ⁽³⁾	1 ⁽³⁾	A
V_{O1} or V_{O2}	Output Voltage	14.5 ⁽²⁾	15	15.5 ⁽²⁾	V
ΔR_{temp}	Temperature Variation	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $I_{O1} \leq 0.1\text{ A}$ or $I_{O2} \leq 0.1\text{ A}$	V_{O1} or V_{O2}	± 1	% V_O
ΔR_{line}	Line Regulation	Over V_I range, balanced load	V_{O1} or V_{O2}	± 0.05	% V_O
ΔR_{load}	Load Regulation	Over I_{O1} or I_{O2} range, balanced load	V_{O1} or V_{O2}	± 0.1	% V_O
η	Efficiency	$I_{O1} = I_{O2}$		90%	
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth, $C_O = 10\text{ }\mu\text{F}$ tantalum capacitor		50 100 ⁽⁴⁾	mV _{pp}
t_{tr}	Transient Response	0.1 A/ μs load step, 50% to 75% I_{O1} or I_{O2} maximum		30	μs
ΔV_{tr}		V_{O1} or V_{O2} overshoot/undershoot		± 1	% V_O
I_{trip}	Over Current Threshold	$V_I = 36\text{ V}$, reset followed by auto-recovery		2.45 3 3.85	A
	Short Circuit Current	Continuous overcurrent trip, $I_{O1} = I_{O2}$	$I_{O1(\text{pk})}$ $I_{O2(\text{pk})}$	4.5	A
			Duty	10%	
$V_{O1(\text{adj})}$, $V_{O2(\text{adj})}$	Output Voltage Adjust Range	V_{O1} and V_{O2} adjust simultaneously		7.2 16.7	V
f_S	Switching Frequency	Over V_I and I_O ranges		440 480 ⁽⁵⁾ 520	kHz
V_I on	Under-Voltage Lockout	V_I increasing		33	V
V_I off		V_I decreasing		32	
	On/Off Enable (pin 3)	Referenced to $-V_I$ (pin 4)			V
V_{IH}	High-level input voltage			3.6 75 ⁽⁶⁾	
V_{IL}	Low-level input voltage			-0.2 0.8	
I_{IL}	Low-level input current			-1	mA
I_I standby	Standby Input Current	Pin 3 open circuit		2	mA
t_{ON}	Start-up Time	$I_{O1} \leq 1\text{ A}$ or $I_{O2} \leq 1\text{ A}$, V_{O1} or V_{O2} or rising 0 to 0.95 (typ)		6 12 18	ms
C_I	Internal Input Capacitance			3	μF
C_O	External Output Capacitance	Capacitance from either output to COM (pin 6)		0 3000 ⁽⁷⁾	μF
MTBF	Reliability	Per Telcordia SR-332 50% stress, $T_A = 40^\circ\text{C}$, ground benign		2.8	10^6 hrs

- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
- (2) Under balanced load conditions, load current flowing out of V_{O1} is balanced to within $\pm 0.1\text{ A}$ of that flowing into V_{O2} .
- (3) A load imbalance is the difference in current flowing from V_{O1} to V_{O2} . The module can operate with a higher imbalance but with reduced specifications.
- (4) Output voltage ripple is measured with a 10- μF tantalum capacitor connected from V_{O1} (pin 5) or V_{O2} (pin 8), to COM (pin 6).
- (5) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
- (6) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to V_I . The open-circuit voltage is 5 V maximum. If it is left open circuit the converter operates when input power is applied.
- (7) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
+V _I ⁽¹⁾	1	The positive input supply for the module with respect to V _I (or ground return). When powering the module from a -48 V telecom central office supply, this input is connected to the primary system ground.
Sync In	2	This pin is used when the PTB4851x and PTB4850x DC/DC converter modules are used together. Connecting this pin to the <i>Sync Out</i> of the PTB4850x module allows the PTB4851x to be synchronized to the same switch conversion frequency as the PTB4850x.
Enable ⁽²⁾	3	This is an open-collector (open-drain) negative logic input that enables the module output. This pin is referenced to -V _I . A logic 0 at this pin enables the module's outputs, and a high impedance disables the outputs. If this feature is not used the pin should be connected to -V _I . Note: Connecting this input directly to the <i>EN Out</i> pin of the PTB4850x enables the output voltages from both converters (PTB4850x and PTB4851x) to power up in sequence.
-V _I	4	The negative input supply for the module, and the 0 VDC reference for the <i>Enable</i> , and <i>Sync In</i> signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.
V _{O1}	5	The positive output supply voltage, which is referenced to the COM node. The voltage at V _{O1} has the same magnitude, but is the complement to that at V _{O2} .
V _{O2}	8	The negative output supply voltage, which is referenced to the COM node. The voltage at V _{O2} has the same magnitude, but is the complement to that at V _{O1} .
COM	6	The secondary return reference for the module's regulated output voltages. This node is dc isolated from the input supply pins.
V _{OAdj}	7	Using a single resistor, this pin allows the magnitude of both V _{O1} and V _{O2} to be adjusted together, either higher or lower than their preset value. If not used, this pin should be left open circuit.

(1) Shaded functions indicate signals that are referenced to -V_I

(2) Denotes negative logic: Open = Output Off, -V_I = Normal operation.

TYPICAL CHARACTERISTICS

PTB4851xA CHARACTERISTIC DATA at $V_I = 48$ V ⁽¹⁾ ⁽²⁾

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

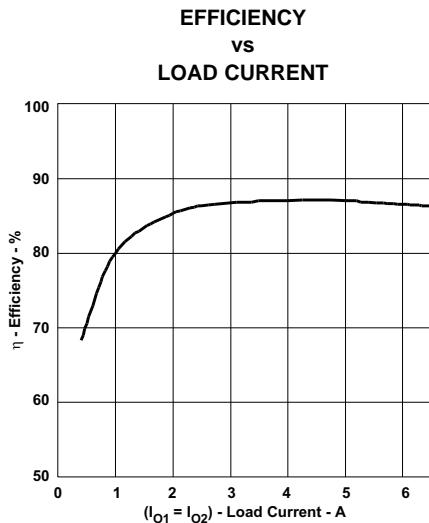


Figure 1. ⁽¹⁾

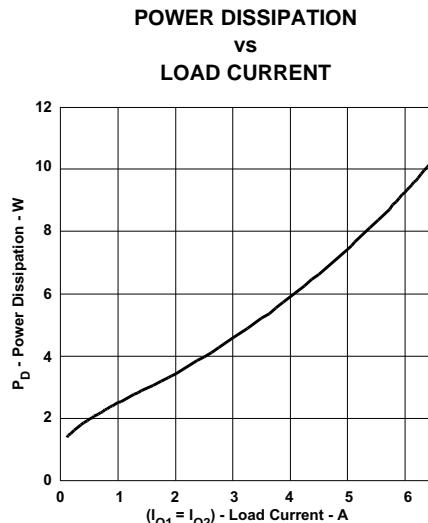


Figure 2. ⁽¹⁾

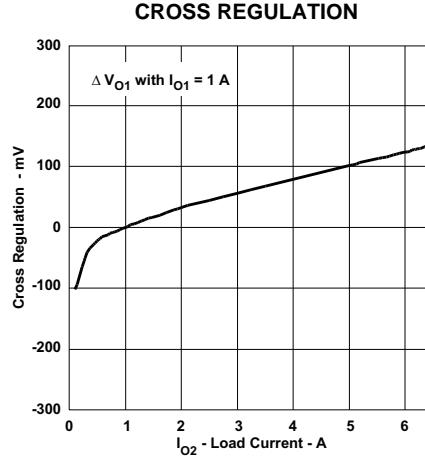


Figure 3.

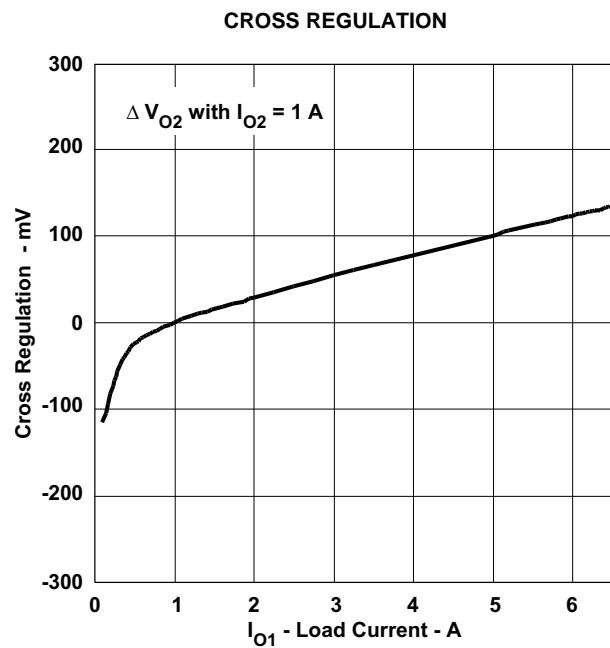


Figure 4.

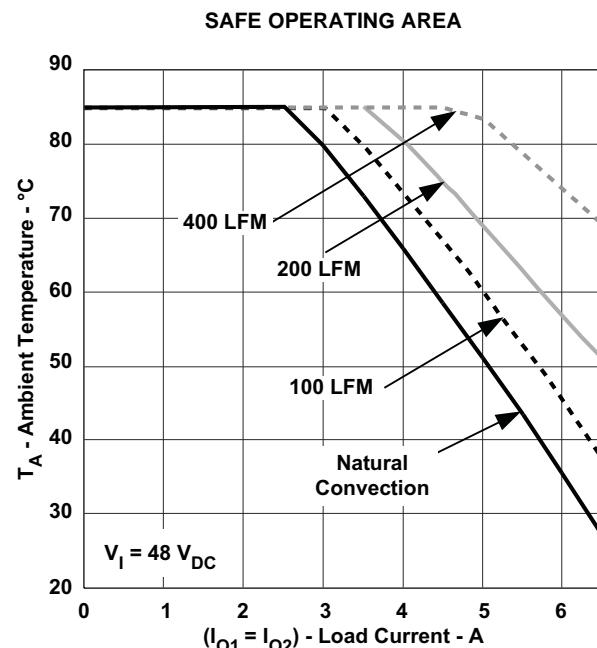


Figure 5. ⁽¹⁾ ⁽²⁾

- (1) Under a balanced load, current flowing out of V_{O1} is equal to that flowing into V_{O2} .
- (2) SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. \times 4 in. double-sided PCB with 1 oz. copper.

TYPICAL CHARACTERISTICS (Continued)

PTB4851xB CHARACTERISTIC DATA at $V_I = 48$ V ⁽¹⁾ ⁽²⁾

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

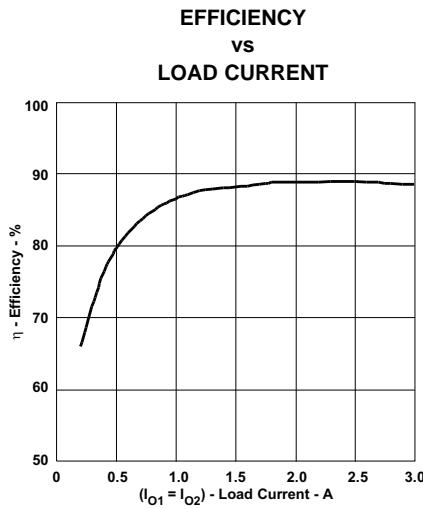
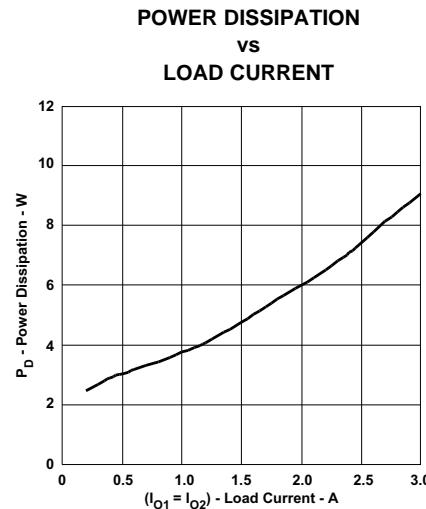
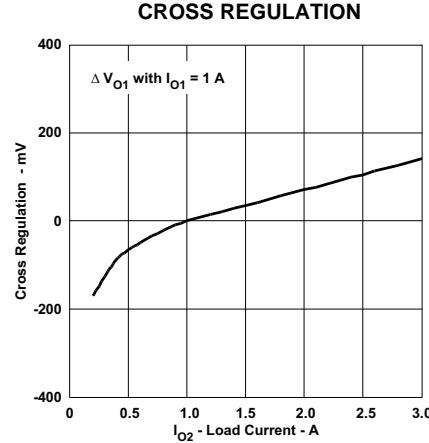
Figure 6. ⁽¹⁾Figure 7. ⁽¹⁾

Figure 8.

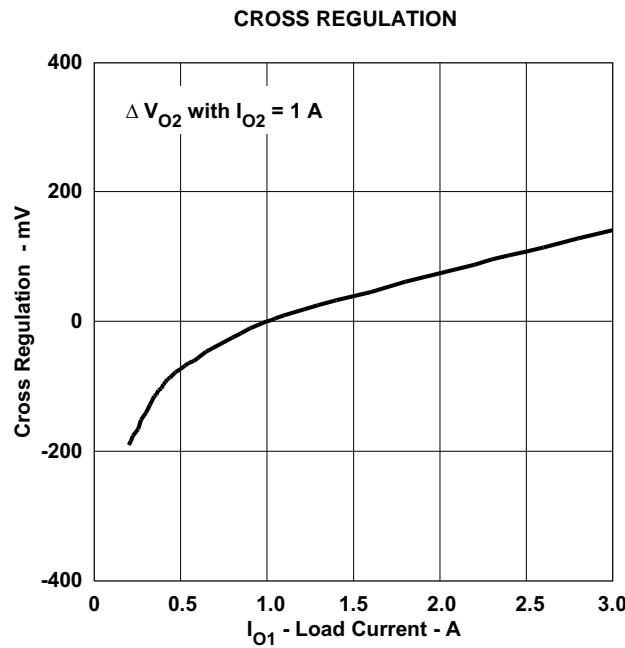
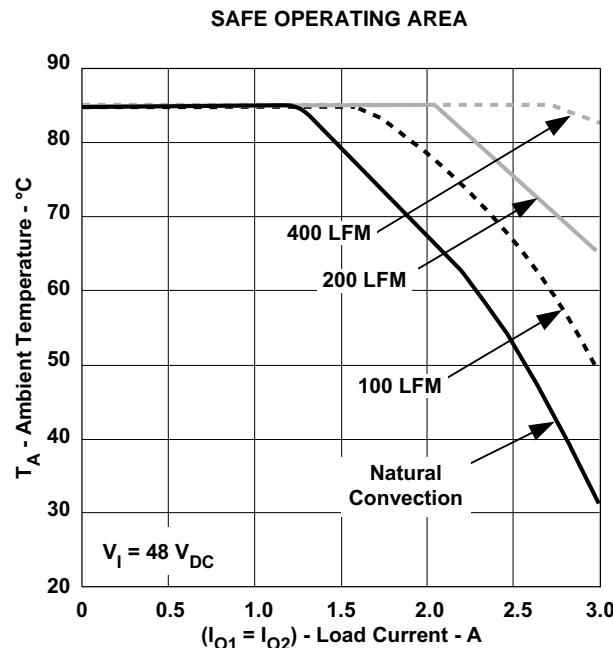


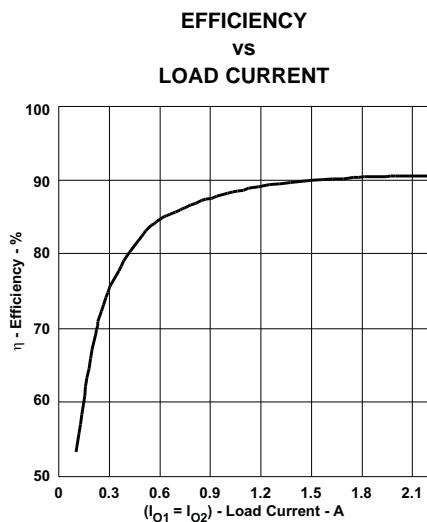
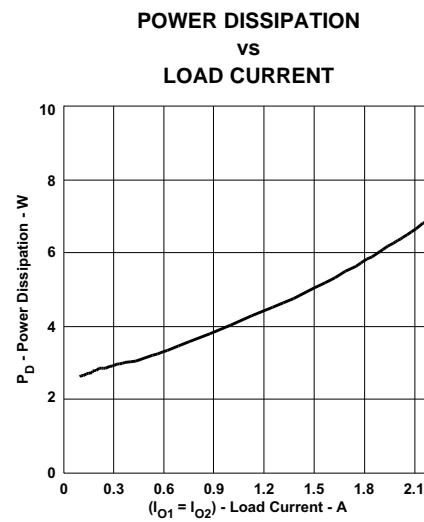
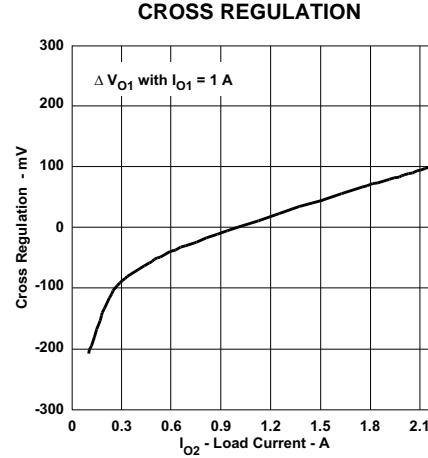
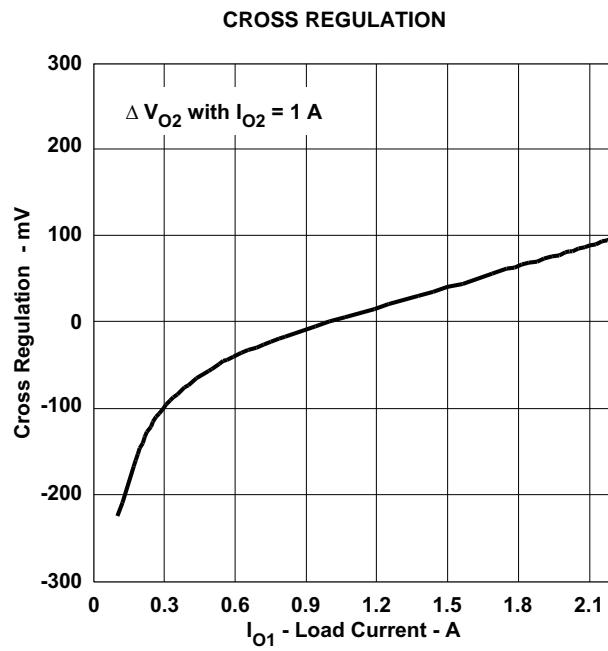
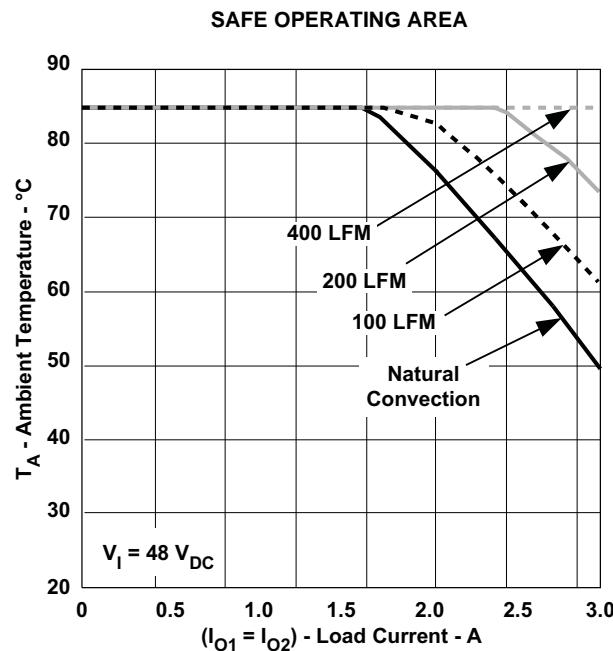
Figure 9.

Figure 10. ⁽¹⁾ ⁽²⁾

- (1) Under a balanced load, current flowing out of V_{O1} is equal to that flowing into V_{O2} .
 (2) SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. \times 4 in. double-sided PCB with 1 oz. copper.

TYPICAL CHARACTERISTICS (Continued)
PTB4851xC CHARACTERISTIC DATA at $V_I = 48$ V ⁽¹⁾ ⁽²⁾

Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.


Figure 11. ⁽¹⁾

Figure 12. ⁽¹⁾

Figure 13.

Figure 14.

Figure 15. ⁽¹⁾ ⁽²⁾

- (1) Under a balanced load, current flowing out of V_{O1} is equal to that flowing into V_{O2} .
- (2) SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. \times 4 in. double-sided PCB with 1 oz. copper.

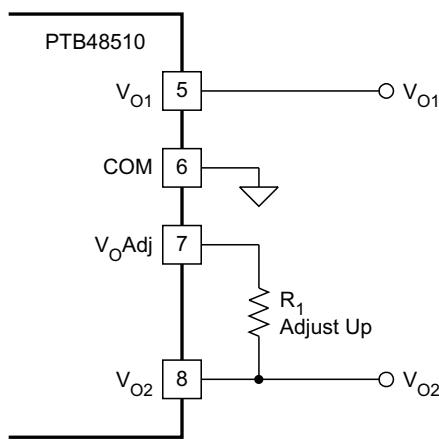
APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE OF THE PTB4851x SERIES OF DC/DC CONVERTERS

The PTB48510 and PTB48511 DC/DC converters produce a balanced pair of complimentary output voltages. They are identified V_{O1} and V_{O2} , respectively. The magnitude of both output voltages can be adjusted together as a pair, higher or lower, by up to $\pm 10\%$ of their nominal. The adjustment method uses a single external resistor.¹ The value of the resistor determines the adjustment magnitude, and its placement determines whether the magnitude is increased or decreased. The resistor values can be calculated using the appropriate formula (see below). The formula constants are given in [Table 1](#). The placement of each resistor is as follows.

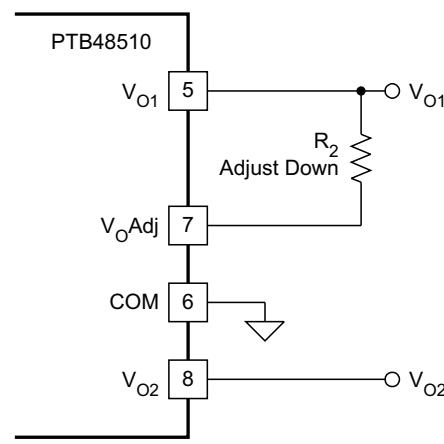
Adjust Up: To increase the magnitude of both output voltages, place a resistor R_1 between V_{O1Adj} (pin 7) and the V_{O2} (pin 8) voltage rail; see [Figure 16](#).

Adjust Down: To decrease the magnitude of both output voltages, add a resistor (R_2), between V_{O1Adj} (pin 7) and the V_{O1} (pin 5) voltage rail; see [Figure 17](#).



UDG-07041

Figure 16. Adjust Up Resistor Placement



UDG-07042

Figure 17. Adjust Down Resistor Placement

ADJUST RESISTOR CALCULATION

The value of the adjust resistor is calculated using one of the following equations. Use the equation for R_1 to adjust up, or (R_2) to adjust down.

$$R_1 [\text{Adjust Up}] = \frac{V_r R_o}{2(V_a - V_o)} - R_s \text{ k}\Omega \quad (1)$$

$$(R_2) [\text{Adjust Down}] = \frac{R_o(2V_a - V_r)}{2(V_o - V_a)} - R_s \text{ k}\Omega \quad (2)$$

Where:

V_o = Magnitude of the original V_{O1} or V_{O2}

V_a = Magnitude of the adjusted voltage

V_r = The reference voltage from [Table 1](#)

R_o = The resistance value in [Table 1](#)

R_s = The series resistance from [Table 1](#)

Table 1. Adjustment Range and Formula Parameters

PARAMETERS	PTB4851xA	PTB4851xB	PTB48510C
$V_O(\text{nom})$ (V)	5	12	15
$V_a(\text{min})$ (V)	3.5	6.5	7.2
$V_a(\text{max})$ (V)	5.5	13.4	16.7
V_r (V)	2.495	2.495	2.495
R_n (k Ω)	7.5	18.2	22.1
R_s (k Ω)	9.09	16.9	16.9

NOTES:

1. A 0.05 W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/ $^{\circ}\text{C}$ or better. Place the resistor in either the R_1 or (R_2) location, as close to the converter as possible.
2. Never connect capacitors to the V_o *Adj* pin. Capacitance added to this pin can affect the stability of the regulated output.
3. **The overvoltage protection (PTB4851x)** is nominally set to 25% above the original output voltage set-point. Increasing the magnitude of the output voltages reduces the margin between the output voltage and the overvoltage (OV) protection threshold. This could make the module more sensitive to OV faults, as a result of random noise and load transients.

Note: An OV fault is a latched condition that shuts down the converter's outputs. The fault can be cleared by cycling the Enable pin, or by momentarily removing input power to the module.

CONFIGURING THE PTB4850x and PTB4851x DC/DC CONVERTERS FOR DSL APPLICATIONS

When operated as a pair, the PTB4850x and PTB4851x converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB4851x produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB4851x may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. [Figure 19](#) shows the required cross-connects between the two converters to enable these two features.

SWITCHING FREQUENCY SYNCHRONIZATION

Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter's switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

POWER-UP SEQUENCING

The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be assured if the PTB4850x and PTB4851x are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the *EN Out* pin of the PTB4850x is directly connected to the *activelow Enable* input of the PTB4851x (see [Figure 19](#)). This allows the PTB4850x to momentarily hold off the outputs from the PTB4851x until the logic-level voltages have risen first. [Figure 19](#) shows the power-up waveforms of all four supply voltages from the schematic of [Figure 19](#).

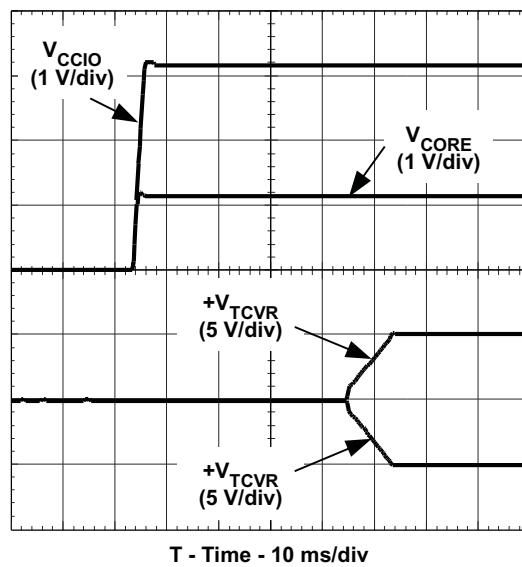
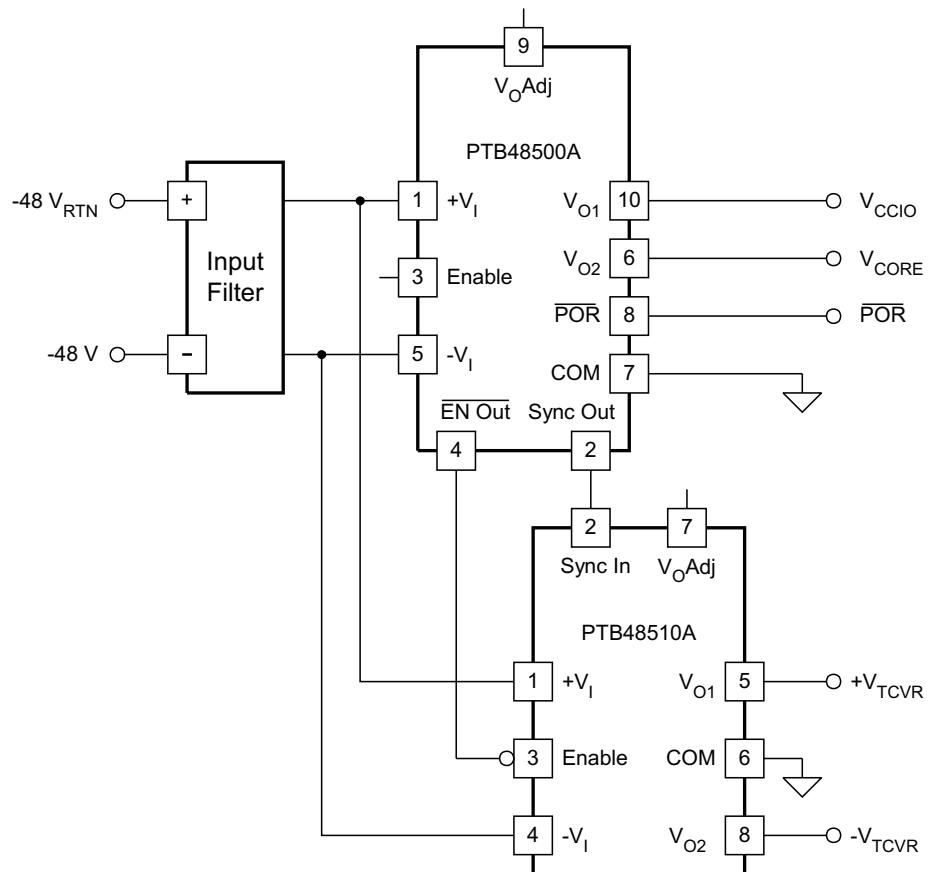


Figure 18. Power-Up Sequencing Waveforms



UDG-07043

Figure 19. Example of PTB4850x and PTB4851x Modules Configured for DSL Applications

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTB48510AAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48510BAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48510BAS	NRND	Surface Mount Module	ERL	8	9	TBD	SNPB	Level-1-235C-UNLIM/Level-3-260C-168HRS	-40 to 85		
PTB48510BAZ	NRND	Surface Mount Module	ERL	8	9	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTB48510CAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48510CAZ	NRND	Surface Mount Module	ERL	8	9	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTB48511AAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48511AAS	OBsolete	Surface Mount Module	ERL	8		TBD	Call TI	Call TI	-40 to 85		
PTB48511BAH	NRND	Through-Hole Module	ERK	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		
PTB48511BAZ	NRND	Surface Mount Module	ERL	8	9	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

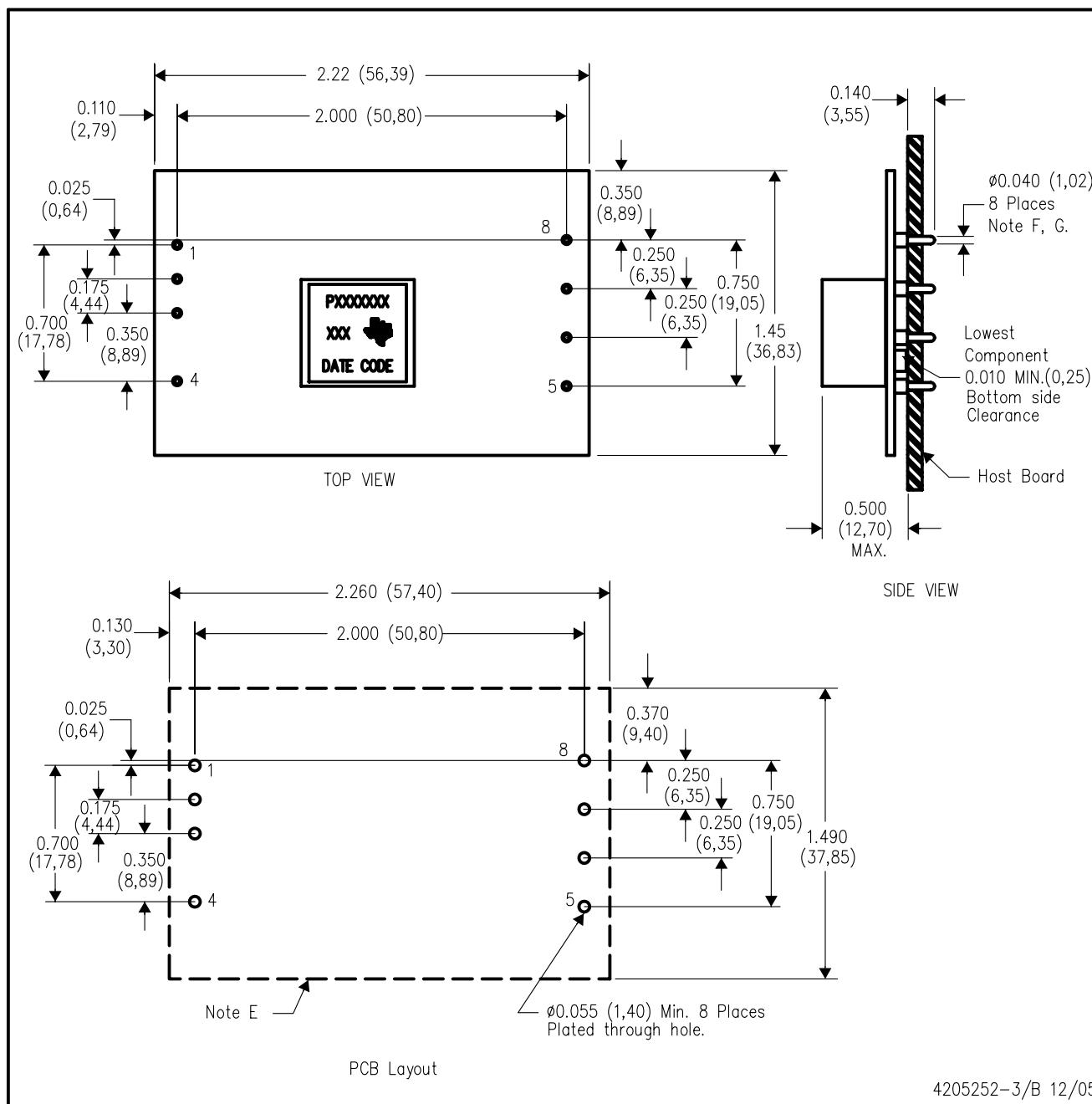
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

ERK (R-PDSS-T8)

DOUBLE SIDED MODULE



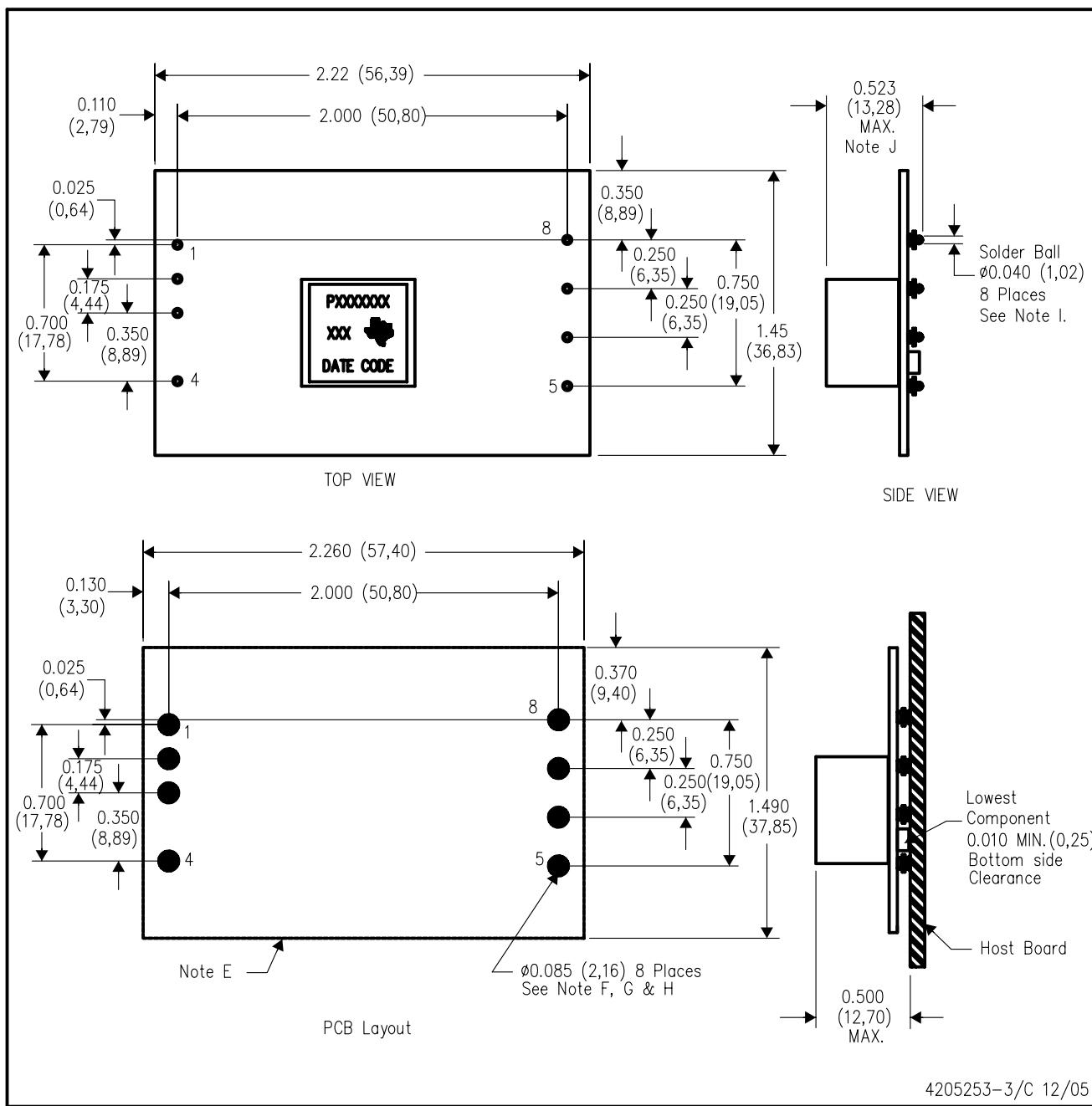
- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.020 (± 0.51 mm).
 - D. 3 place decimals are ± 0.010 (± 0.25 mm).
 - E. Recommended keep out area for user components.

- F. Pins are 0.040" (1.02) diameter with 0.070" (1.78) diameter standoff shoulder.
- G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

MECHANICAL DATA

ERL (R-PDSS-B8)

DOUBLE SIDED MODULE



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity
	TI E2E Community
	e2e.ti.com