NCP1568

Product Preview

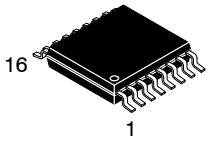
Ac-Dc Active Clamp Flyback PWM IC

ON Semiconductor®

www.onsemi.com

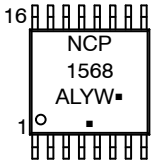
The NCP1568 is a highly integrated Ac−Dc PWM controller designed to implement an active clamp flyback topology. NCP1568 employs a proprietary variable frequency algorithm to enable zero voltage switching (ZVS) of the MOSFETs across line & load conditions. The ZVS feature allows high frequency operation increasing power density of a power converter while achieving high efficiency. Further, it simplifies EMI filter design and can be easily designed to avoid interference with other sensitive circuits in the system. The NCP1568 features a HV startup circuit, a strong low side driver, and a 5V logic level driver for active clamp FET. The NCP1568 is suitable for a variety of applications including Ac−Dc adapters, industrial, telecom, lighting and other applications where power density is an important requirement.

The NCP1568 also features multimode operation and transitions from ACF mode to Discontinuous Conduction Mode (DCM) to meet regulatory requirements from around the world. The NCP1568 further implements quiet skip technique in standby mode resulting in excellent standby power while eliminating acoustic noise. The combination of flexible control scheme and user programmable features allow the use of NCP1568 with Super−Junction MOSFETs (Si) and Gallium Nitride (GaN) FETs.



TSSOP−16
DT SUFFIX
CASE 948F

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 36 of this data sheet.

Features

- Topology & Control Scheme
  - Active Clamp Flyback Topology Aids in ZVS
  - Proprietary Multi−mode Operation to Enhance Light Load Efficiency
  - Proprietary Adaptive ZVS Allows High Frequency Operation while Reducing EMI
  - Inbuilt Adaptive Dead−time for Both Main & Active Clamp FETs
  - Peak Current−mode Control with Inbuilt Slope Compensation with Options
  - Flexible Control Scheme and Programmability Allow for Configuration with Either External Silicon or GaN FETs
- DCM & Light Load Operation
  - Customer Programmable Optional Transition to DCM
  - Integrated Frequency Foldback with Minimum Frequency Clamp for Highest Performance in Standby Mode
  - Minimum Frequency Clamp & Quiet Skip Eliminates Audible Noise
  - Standby Power < 30 mW
- HV & Startup Circuits
  - 700 V Startup Circuit
  - AC Line Brownout Detect and Integrated X2 Capacitor Discharge
- Drivers
  - 1.25 A/2.5 A Source/sink for Low Side
  - 100 mA/200 mA Active Clamp Driver Output
- Oscillator
  - Programmable Frequency from 100 kHz to 1 MHz
  - Internal Soft−start Timer with 4 Options
- Protection
  - Dedicated FLT Pin Compatible with a Thermistor
  - Adjustable Over Power Protection (OPP)
  - Option for Auto−recovery & Latched in Various Faults
  - Internal Thermal Shutdown

Applications

- USB Power Delivery
- Notebook Adapters
- High Density Chargers
- Industrial Power Supplies

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

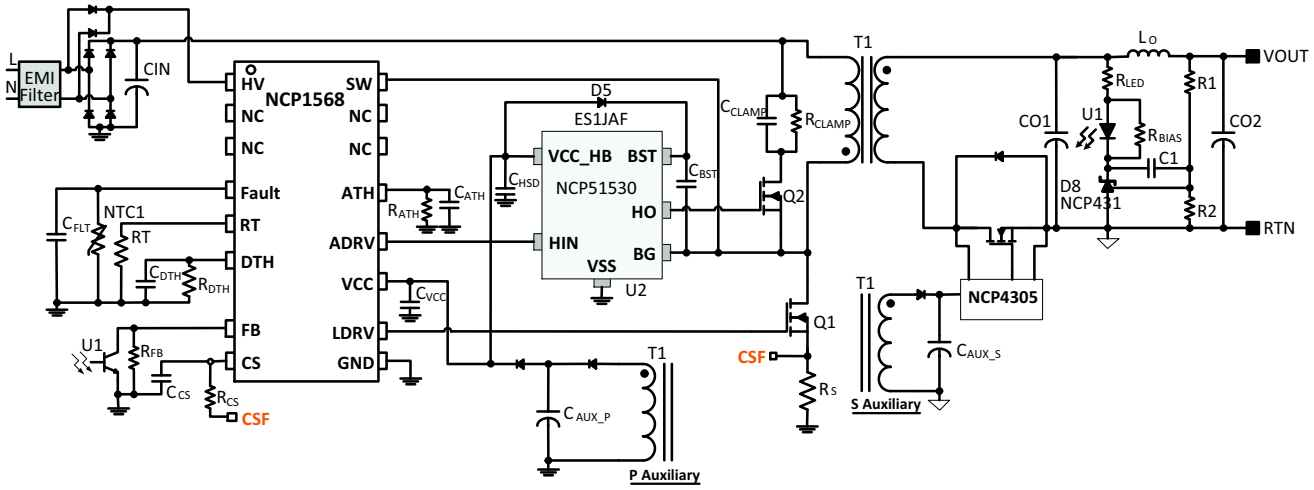


Figure 1. Typical Application for the NCP1568 Active Clamp Flyback

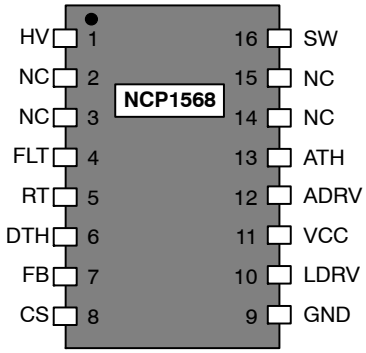


Figure 2. Pinout

Table 1. PIN FUNCTIONAL DESCRIPTION

Pin out Controller Option	Name	Function
1	HV	Input to the HV startup circuit. Information derived from HV pin is also used for BO detection, AC line presences detect, over power protection, and X2 discharge.
2,3,14,15	NC	Removed for creepage and clearance compliance.
4	FLT	The controller enters fault mode if the voltage of this pin is pulled above or below the fault thresholds.
5	RT	A resistor from the RT pin to ground sets the minimum frequency of the internal oscillator.
6	DTH	A resistor to ground sets the ACF to DCM transition threshold
7	FB	Feedback input allows direct connection to an opto−coupler and is pulled up with an internal resistor
8	CS	Current sense input. A CS resistor connected between the source of the power FET and the GND provides primary current information to the IC.
9	GND	Ground reference.
10	LDRV	Low−side drive output. Clamped to 12 V output.
11	VCC	Supply input. At startup, an internal HV current charges the VCC capacitor. Once the power stage is enabled, an auxiliary winding supplies current to the VCC cap and internal HV current source is turned−off.
12	ADRV	ADRV is the 5 V alternate ground based high side driver signal for the controller option
13	ATH	A resistor to ground sets the DCM to ACF transition threshold
16	SW	Connect to SW node.

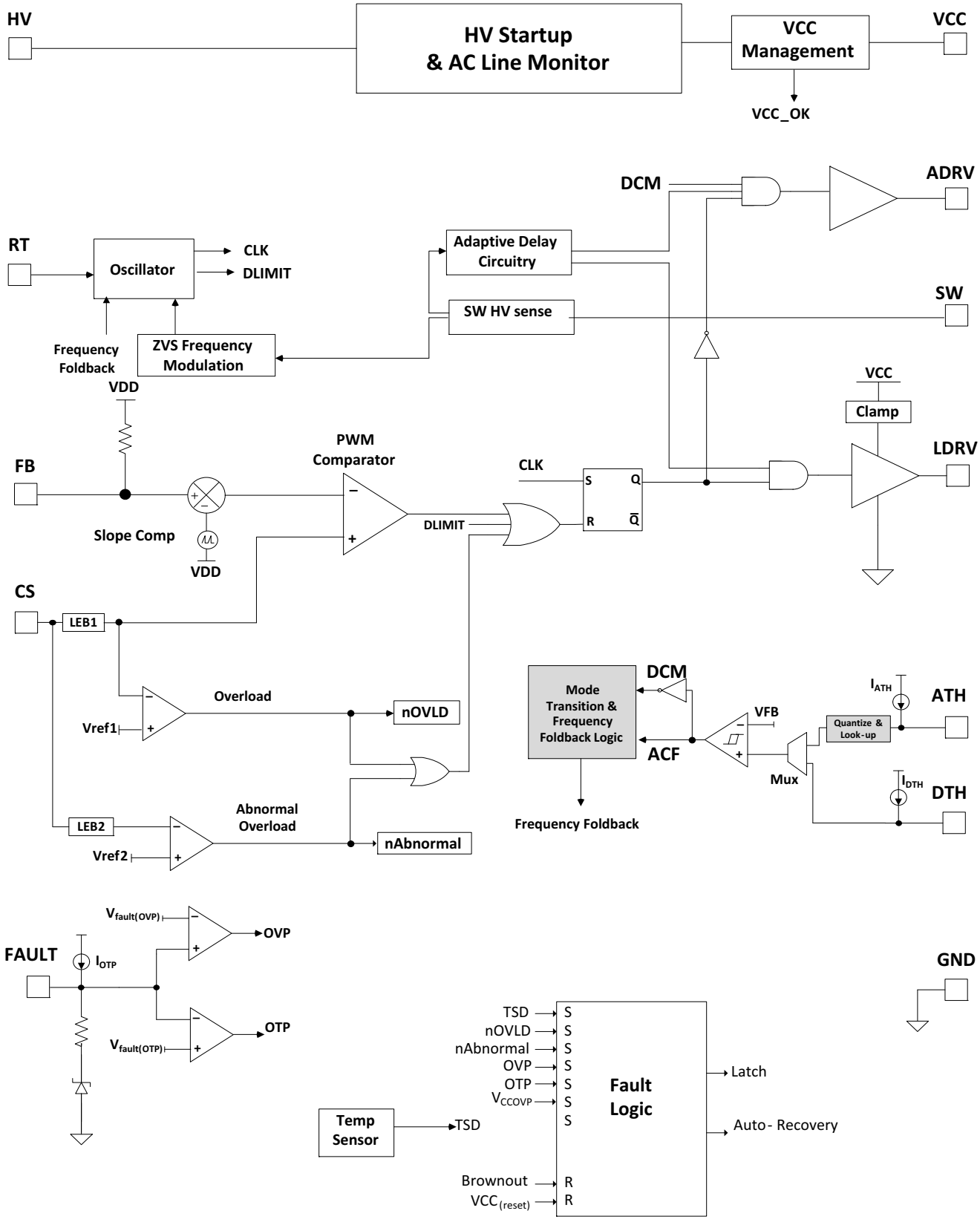


Figure 3. Block Diagram

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage Startup Circuit Input Voltage	$V_{HV(MAX)}$	−0.3 to 700	V
High Voltage Startup Circuit Input Current	$I_{HV(MAX)}$	20	mA
Supply Input Voltage	$V_{CC(MAX)}$	−0.3 to 30	V
Supply Input Current	$I_{CC(MAX)}$	30	mA
Supply Input Voltage Slew Rate	dV_{CC}/dt	25	mV/μs
.SW Pin to GND	$V_{SW(MAX)}$	−1 to 700	V
SW Pin Circuit Input Current	$I_{SW(MAX)}$	1	mA
ADRV Pin to GND	V_{ADRV}	−0.3 V to 5.5	V
ADRV Driver Maximum Current	$I_{ADRV(SRC)}$ $I_{ADRV(SNK)}$	130 190	mA
Low Side Driver Voltage (Note 1)	V_{DRV}	−0.3 V to $V_{DRV(high)}$	V
Maximum Input Voltage ATH	$V_{ATH(MAX)}$	0.3 V to 5.5	V
Maximum Input Current ATH	$I_{ATH(MAX)}$	10	mA
Maximum Input Voltage DTH	$V_{DTH(MAX)}$	0.3 V to 5.5	V
Maximum Input Current DTH	$I_{DTH(MAX)}$	10	mA
Current Sense Input Voltage	V_{CS}	−0.3 to 5.5	V
Current Sense Input Current	I_{CS}	10	mA
Maximum Input Voltage (Other Pins: FB, RT, FLT)	V_{MAX}	−0.3 to 30	V
Maximum Input Current (Other Pins: FB, RT, FLT)	I_{MAX}	27	mA
Operating Junction Temperature	T_J	−40 to 125	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
Power Dissipation (T_A = 25°C, 1 Oz Cu, 0.231 Sq Inch Printed Circuit Copper Clad) TBD Suffix, Plastic Package TSSOP16	$P_{D(MAX)}$	833	mW
Thermal Resistance, Junction to Ambient 1 Oz Cu Printed Circuit Copper Clad) TBD Suffix, Plastic Package TSSOP16	$R_{\theta JA}$	150	°C/W
ESD Capability (Note 3) Human Body Model per JEDEC Standard JESD22−A114E. Charge Device Model per JEDEC Standard JESD22−C101E.		 2000 1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.
2. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.
3. Low Conductivity Board. As mounted on 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper trances and heat spreading area. As specified for a JEDEC51−1 conductivity test PCB. Test conditions were under natural convection of zero airflow.
4. HV Pin is rated to the maximum voltage of the part, or 600 V.

Table 3. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min	Typ	Max	Units
Vcc operating voltage V_{CC}	V_{CC}	9.7	16	27	V
Operating Junction temperature	Jc	−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1 nF for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
START−UP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	15.0	15.5	16.0	
Minimum Operating Voltage After Turn−On	V_{CC} decreasing	$V_{CC(off)}$	8.5	9.0	9.5	
Operating Hysteresis	$V_{CC(on)}$	$V_{CC(HYS)}$	5.5	–	–	
Internal Latch/Logic Reset Level	− $V_{CC(off)}$	$V_{CC(reset)}$	5.0	5.5	6.5	
V_{CC} Level at Which I_{start1} Transitions to I_{start2}	V_{CC} decreasing	$V_{CC(inhibit)}$	0.27	0.70	1.03	
VCC Charge Voltage During Line Removal	V_{CC} increasing, I_{HV} = 500 μA V_{CC} increasing	$V_{CC(X2\_reg)}$	16.0	17.0	18.0	
$V_{CC(off)}$ to Drive Turn−Off Timeout Delay	V_{cc} decreasing	$t_{delay(VCC\_off)}$	52.5	60.0	67.5	μs
Startup Delay	Delay from $V_{CC(on)}$ to first LDRV pulse	$t_{delay(start)}$	40	50	70	μs
Start−Up Time	C_{VCC} = 0.47 μF, V_{CC} = 0 V to $V_{CC(on)}$	$t_{start-up}$	–	2.5	5.5	ms
Minimum HV Pin Voltage for Rated Start−Up Current Source	V_{cc} = $V_{CC(on)}$ − 0.5 V	$V_{HV(MIN)}$	–	–	40	V
Inhibit Current Sourced from V_{CC} Pin	V_{cc} = 0 V	I_{start1}	0.2	0.5	0.65	mA
Start−Up Current Sourced from V_{CC} Pin	V_{cc} = $VCC_{(on)}$ − 0.5 V	I_{start2}	2.5	3.75	5	mA
Start−Up Circuit Off−State Leakage Current	V_{hv} = 162.5 V V_{hv} = 325 V V_{hv} = 700 V	$I_{HV(off1)}$ $I_{HV(off2)}$ $I_{HV(off3)}$	– – –	– – –	15 20 50	μA
Switch Pin Off−State Leakage Current	FLT = 0 V V_{hv} = 162 V V_{hv} = 325 V V_{hv} = 700 V	 $I_{SW(off1)}$ $I_{SW(off2)}$ $I_{SW(off3)}$	 – – –	 – – –	 3 4 5	μA
Switch Pin Active Current Draw	V_{ATH} = V_{DTH} = 0 V V_{HV} = 162 V V_{HV} = 325 V V_{HV} = 700 V	 $I_{SW(on1)}$ $I_{SW(on2)}$ $I_{SW(on3)}$	 102 121 122	 120 121 122	 148 149 150	μA
Supply Current						mA
FLT PIN OTP	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{CC1A}	0.10	0.19	0.30	
FLT PIN OVP	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{CC1B}	0.10	0.19	0.30	
Latch Fault	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{CC1C}	0.10	0.15	0.30	
Skip Mode (Excluding FB & FLT Current)	V_{FB} = 0 V	I_{CC2}	0.18	0.27	0.41	
Operating Current 500 kHz	F_{sw} = 500 kHz, A_{DRV} = L_{DRV} =100 pF	I_{CC3}	3.50	4.70	5.20	
Operating Current 100 kHz	F_{sw} = 100 kHz, VCC = 20 V	I_{CC4}	2.60	3.60	4.20	
Operating Current 500 kHz	F_{sw} = 500 kHz, VCC = 10 V	I_{CC5}	7.20	8.20	9.20	
V_{CC} Overvoltage Protection Threshold	Latched event	$V_{CC(OVP)}$	27	28	29	V
V_{CC} Overvoltage Protection Timeout Delay		$t_{delay(VCC\_OVP)}$	52.5	60.0	67.5	μs
BROWNOUT DETECTION						
System Start−Up Threshold	V_{HV} increasing DC level	$V_{HV(start)}$	109	112	115	V
Brownout Threshold	V_{HV} decreasing DC level	$V_{HV(stop)}$	95	98	101	V
Hysteresis		$V_{HV(HYS)}$	9	14	–	V
Brownout Detection Blanking Time	V_{HV} decreasing	$t_{HV(stop)}$	40	50	60	ms
System Start−Up Threshold Filter	Rising AC waveform	$t_{delay(HV\_start)}$	80	100	120	μs
Brownout Detection Blanking Time Filter	Falling AC waveform	$t_{delay(HV\_stop)}$	200	300	400	μs

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1 nF for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
X2 CAPACITOR DISCHARGE						
Line Voltage Removal Detection Timer		$t_{line(removal)}$	65	96	135	ms
Discharge Timer Duration		$t_{line(discharge)}$	29	32	35	ms
Line Detection Timer Duration		$t_{line(detect)}$	29	32	35	ms
V_{CC} Discharge Current	V_{CC} = 20 V	$I_{CC(discharge)}$	13	18	23	mA
HV Discharge Level		$V_{HV(discharge)}$	–	–	30	V
SOFT−START						
Soft−Start Time	Ramp time for CS from 0 to I_{limit}	$t_{soft-start1}$		8		ms
Forced DCM Time at the Beginning of Soft Start	RT = 33 kΩ (303 kHz)	t_{DCM_SS}		600		μs
Time at which FB is Compared to DTH threshold	Time from the End of Soft Start to the ACF/DCM Assessment	t_{MODE_Sam1}		16		ms
OSCILLATOR						
Minimum Oscillator Frequency in ACF Mode	VSW = 15 V, RT = 100 kΩ	$F_{osc\_ACF\_100}$	95	100	105	kHz
Minimum Oscillator Frequency in ACF Mode	VSW = 15 V, RT = 20 kΩ	$F_{osc\_ACF\_500}$	450	500	550	kHz
Frequency Modulation Bounds	VSW = Modulated RT = 100 kΩ, 4.20 * F_{osc_ACF} RT = 42.2 kΩ, 4.20 * F_{osc_ACF}	 $F_{osc1\_ACF\_M}$ $F_{osc2\_ACF\_M}$	 399 950	 420 1000	 441 1050	kHz
Oscillator Frequency at Low/High Line in DCM Mode	RT = 20 kΩ, FB = DCM to ACF Trip Threshold −5 mV	$F_{osc\_DCM\_2}$	225	250	275	kHz
Oscillator Frequency Range	RT = 100 kΩ to 10 kΩ	F_{Range}	100		1000	kHz
Maximum Duty Cycle	F_{osc}= 100 kHz, RT = 100 kΩ F_{osc} = 250 kHz ,RT = 40 kΩ F_{osc}= 500 kHz, RT = 20 kΩ, T_{min_OFF} F_{osc} = 1 MHz, RT = 10 kΩ T_{min_OFF}	D_{Max_100} D_{Max_400} $D_{Max\_500\_OFF}$ $D_{Max\_1000\_OFF}$	78 78 70 58	80 80 72 60	82 82 74 62	%
Minimum OFF Time for ADRV	Measured at 50% of Drive Voltage From Falling Edge to Rising Edge of LDRV	T_{min_OFF}		400		ns
RT Pin Voltage	RT = 10 kΩ	V_{RT}	1.7	2	2.3	V
TRANSITION MODE						
ACF to DCM Transition	ADRV LEM soft stop time	$t_{ACF\_DCM\_Trans}$		0.5		ms
DCM to ACF Transition	ADRV LEM soft start time	$t_{DCM\_ACF\_Trans}$		0.5		ms
DCM Forced Switching Time from ATH trip	V_{FB} = V_{ATH} + 100 mV	T_{DCMT}		100		μs
DCM to ACF Blanking time after transition	Time the DCM to ACF Comparator is blanked	$t_{DCM\_ACF\_HOLD}$		4		ms
ATH FUNCTION						
Current Sourced From ATH	ATH = 2 V	I_{ATH}	9.85	10	10.15	μA
ATH BIN 0	50 mV	ATH_BIN0_OPT0	ACF	ACF	ACF	–
ATH BIN 1	180 mV	ATH_BIN1_OPT1	1.092	1.12	1.148	V
ATH BIN 2	220 mV	ATH_BIN2_OPT1	1.17	1.2	1.23	V
ATH BIN 3	270 mV	ATH_BIN3_OPT1	1.248	1.28	1.312	V
ATH BIN 4	330 mV	ATH_BIN4_OPT1	1.326	1.36	1.394	V
ATH BIN 5	390 mV	ATH_BIN5_OPT1	1.404	1.44	1.476	V

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1 nF for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
ATH FUNCTION						
ATH BIN 6	460 mV	ATH_BIN6_OPT1	1.482	1.52	1.558	V
ATH BIN 7	540 mV	ATH_BIN7_OPT1	1.56	1.6	1.64	V
ATH BIN 8	630 mV	ATH_BIN8_OPT1	1.638	1.68	1.722	V
ATH BIN 9	740 mV	ATH_BIN9_OPT1	1.716	1.76	1.804	V
ATH BIN 10	870 mV	ATH_BIN10_OPT1	1.794	1.84	1.886	V
ATH BIN 11	1.02 V	ATH_BIN11_OPT1	1.872	1.92	1.968	V
ATH BIN 12	1.19 V	ATH_BIN12_OPT1	1.95	2	2.05	V
ATH BIN 13	1.39 V	ATH_BIN13_OPT1	2.028	2.08	2.132	V
ATH BIN 14	1.63 V	ATH_BIN14_OPT1	2.106	2.16	2.214	V
ATH BIN 15	1.91 V	ATH_BIN15_OPT1	2.184	2.24	2.296	V
DTH FUNCTION						
DTH pin Pullup Current	RT = 100 kΩ	I_{DTH}		16.0		μA
DTH Trip Voltage	VDTH = 500 mV FB Decreasing VDTH = 1.5 V FB Decreasing VDTH = 3.0 V FB Decreasing	V_{FB_DTH1} V_{FB_DTH1} V_{FB_DTH1}		0.50 1.5 3.0		V
SLOPE COMPENSATION						
Duty Cycle at which Ramp Compensation Begins	Both ACF & DCM Mode	D_{Slope_Start}	40	42.5	45	%
Slope of Compensating Ramp		S_{RAMP}	125	135	145	mV/μs
CM MODE FREQUENCY FOLDBACK						
Feedback Voltage Below which CS Detected Peak Current is Frozen (at the FB Pin)		$V_{FB(lpk\_freeze)}$		800		mV
CS Pin Peak Current Floor Threshold Set when FB is Lower than $\mathbf{V_{FB(lpk\_freeze)}}$	RT = 100 kΩ RT = 33.3 kΩ RT = 20 kΩ	$V_{CS(lpk\_freeze)\_0}$ $V_{CS(lpk\_freeze)\_1}$ $V_{CS(lpk\_freeze)\_2}$	203 341 454	208 348 489	212 355 499	mV
Minimum Oscillator Frequency	Operating Mode = DCM, V_{FB} = 400 mV	$F_{osc(min)}$	25	31	35	kHz
Oscillator Frequency at Low/High Line in DCM Mode	RT = 20 kΩ FB = DCM to ACF Trip Threshold −5 mV	$F_{osc\_DCM\_2}$	225	250	275	kHz
Feedback Voltage at which Minimum Switching Frequency is Reached (at the FB Pin)	Fsw = $F_{osc(min)}$	$V_{Fosc(min)}$	390	400	410	mV
Feedback Voltage at which Skip Cycle Comparator Trips (at the FB Pin)	Feedback Falling	$V_{FB(skip)}$	370	400	430	mV
Skip Cycle Comparator Hysteresis	Feedback Rising (Positive)	$V_{FB(skip)\_hys}$	65	70	75	mV
Skip Wakeup Time	FB > ($V_{FB(skip)}$ + $V_{FB(skip)\_hys}$ +100 mV)	T_{Skip_wake}		24		μs
FEEDBACK						
Open Pin Voltage		$V_{FB(open)}$	4.9	5.0	5.1	V
VFB to Internal Current Set Point Division Ratio	VFB = 4 V	K_{FB}	3.80	4.00	4.20	
Internal Pull−Up Resistor	V_{FB} = 0.4 V	R_{FB}	75	97	125	kΩ
Internal Pull−Up Current	V_{FB} = 0.4 V	I_{FB_0}	91	100.0	108	μA

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1 nF for typical values T_J = 25°C, for min/max values, T_J is –40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
FLT PROTECTION						
Overvoltage Protection (OVP) Threshold	V_{FLT} Increasing	$V_{FLT\ (OVP)}$	2.79	3.00	3.21	V
OVP Detection Delay	V_{FLT} Increasing	$t_{delay(OVP)}$	22.5	30.0	37.5	μs
Over Temperature Protection (OTP) Threshold	V_{FLT} Decreasing (Note 5)	$V_{FLT(OTP\_in)}$	0.38	0.40	0.42	V
Over Temperature Protection (OTP) Exiting Threshold	V_{FLT} Increasing (Note 5)	$V_{FLT(OTP\_out)}$	0.874	0.920	0.966	V
Over Temperature Protection (OTP) Exiting Threshold on Startup	V_{FLT} Increasing with first VCC Power on	$V_{FLT(OTP\_out\_1st)}$	0.38	0.40	0.42	V
OTP Detection Delay	V_{FLT} Decreasing	$t_{delay(OTP)}$	22.5	30.0	37.5	μs
OTP Pull−Up Current Source	$V_{FLT} = V_{FLT\ (OTP\_in)}$ + 0.2 V	$I_{FLT(OTP)}$	42.5	45.5	48.5	μA
FLT Input Clamp Voltage		$V_{FLT\ (clamp)}$	1.58	1.7	1.82	V
FLT Input Clamp Series Resistor		$R_{FLT\ (clamp)}$	1.48	1.5	2.2	kΩ
OVER POWER PROTECTION						
Current Flowing Out of the CS Pin for Line OPP	V_{HV}_peak = 92V V_{HV}_peak = 110 V V_{HV}_peak = 127 V V_{HV}_peak = 145 V V_{HV}_peak = 162V V_{HV}_peak = 186 V V_{HV}_peak = 224V V_{HV}_peak = 268 V V_{HV}_peak = 312 V V_{HV}_peak = 356 V V_{HV}_peak = 401 V	$I_{gm\_prp\_LV4}$ $I_{gm\_prp\_LV5}$ $I_{gm\_prp\_LV6}$ $I_{gm\_prp\_LV7}$ $I_{gm\_prp\_LV8}$ $I_{gm\_prp\_LV9}$ $I_{gm\_prp\_LV10}$ $I_{gm\_prp\_LV11}$ $I_{gm\_prp\_LV12}$ $I_{gm\_prp\_LV13}$ $I_{gm\_prp\_LV14}$		17 21 24 27 31 34 40 49 57 66 74		μA
HV Update Time	HV is sampled every 33 ms to check for update	T_{UPDATE}		33		ms
CURRENT LIMIT PROTECTION						
Count of OCP Events Before Fault is Declared	$V_{CS} > V_{ILIM(OCP)}$	N_{OCP_0}		5		k #
Count of SCP Events Before Fault is Declared	$V_{CS} > V_{ILIM(SCP)}$	N_{SCP_0}	5	5	5	#
Restart Timer for Auto − Recovery		T_{auto_retry}	1479	1600	1775	ms
CS Pin Internal Pull−up Current	V_{CS} = 0.8 V	I_{bias}	.5	1	3	μA
CURRENT SENSE						
Cycle by Cycle Current Limit Threshold Over Current Protection (OCP)	DCM threshold	$V_{ILIM(OCP)\_DCM}$	768	800	832	mV
Cycle by Cycle Current Limit Threshold ACF	RT = 100 kΩ					mV
90 VAC 127 VDC		$V_{(OCP)\_ACF\_90}$	765	800	835	
102 VAC 145 VDC		$V_{(OCP)\_ACF\_102}$	668	700	733	
115 VAC 165 VDC		$V_{(OCP)\_ACF\_115}$	590	620	651	
132 VAC 187 VDC		$V_{(OCP)\_ACF\_132}$	590	620	651	
158 VAC 224 VDC		$V_{(OCP)\_ACF\_158}$	551	580	610	
190 VAC 268 VDC		$V_{(OCP)\_ACF\_190}$	512	540	569	
221 VAC 312 VDC		$V_{(OCP)\_ACF\_221}$	482	510	538	
252 VAC 357 VDC		$V_{(OCP)\_ACF\_252}$	482	510	538	
284 VAC 401 VDC		$V_{(OCP)\_ACF\_284}$	482	510	538	
Cycle by Cycle Current Limit Threshold Over Current Protection (OCP) During LEM	In Transition Mode (ACF to DCM or DCM to ACF)	$V_{ILIM(OCP)\_Trans}$	1.15	1.2	1.24	V

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1 nF for typical values T_J = 25°C, for min/max values, T_J is –40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Short Circuit Protection (SCP) Threshold	Both ACF & DCM	$V_{ILIM(SCP)}$	1.15	1.2	1.24	V
Short Circuit Protection (SCP) Threshold During LEM	In Transition Mode (ACF to DCM or DCM to ACF)	$VI_{LIM(SCP)\_Trans}$	1.32	1.4	1.48	V
OCP Leading Edge Blanking Delay		$T_{LEB(OCP)}$		178	200	ns
SCP Leading Edge Blanking Delay		$T_{LEB(SCP)}$		126	150	ns
OCP Propagation Delay	CS ramped from 0 to 1 V at dv/dt = 20 V/μs to LDRV 8.5 V falling edge	$T_{PROP(OCP)}$		50	75	ns
SCP Propagation Delay	CS ramped from 0 to 1 V at dv/dt = 20 V/μs to LDRV 8.5 V falling edge	$T_{PROP(SCP)}$		50	75	ns
CS Switch Discharge Resistance	Measured with 5 mA Pull Up Current	$R_{DS(ON)\_CS}$			100	Ω
DEAD−TIME MANAGEMENT IN ACF MODE						
Resonant Mode to Energy Storage Voltage Threshold	Falling Edge of SW pin Voltage	$D_{T\_R\_E\_VTH}$	8	10	12	V
Energy Storage to Resonant Mode Voltage Threshold	Rising Edge of SW pin Voltage	$D_{T\_E\_R\_VTH}$	8	10	12	V
Dead−Time from Energy Storage to Resonant Mode	$V_{SW} > D_{T\_E\_R\_VTH}$ to ADRV 2.5 V	$D_{T\_E\_R1}$	33	37	49	ns
LEM ZVS Rising Edge Enable Time	Time during LEM for VSW > 12 V to ADRV output enable	T_{LEM_HSA}		400		ns
Maximum Dead−Time	Measured from ADRV falling edge to LDRV rising edge	$D_{T\_Max\_1}$	399	418	441	ns
ZVS Reference Time for Frequency Modulation	Measured from ADRV Falling Edge to D_{T_Max}	$T_{\_ZVS\_1}$	340	360	380	ns
LOW SIDE DRIVER						
LDRV Rise Time	V_{LDRV} = 2.4 V to 8.5 V	T_{LS_rise}	7.4	9.9	13.5	ns
LDRV Fall Time	V_{LDRV} = 8.5 V to 2.4 V	T_{LS_fall}	2.1	3	4.5	ns
LDRV Source Current	$V_{CC} = V_{CC(off)}$ + 0.5 V, V_{LDRV} = 6 V	I_{LS_src}	0.91	1.3	1.7	A
LDRV Sink Current	$V_{CC} = V_{CC(off)}$ + 0.5 V,V_{LDRV} = 6V	I_{LS_snk}	1.75	2.5	3.25	A
LDRV Clamp Voltage	$V_{CC} = V_{CC(off)}$ + 0.5 V V_{CC} = 18 V, R_{DRV} = 10 kΩ	$V_{LDRV(High1)}$ $V_{LDRV(High2)}$	8.0 10	– 12	– 14	V
Low State Voltage	V_{CC} = 18 V, R_{DRV} = 10 kΩ	$V_{LDRV(low)}$	0	0	0.25	V
ADRV						
ADRV Rise Time	V_{ADRV} = 20% V to 80% of 5 V	T_{ADRV_rise}		2	10	ns
ADRV Fall Time	V_{ADRV} = 80% V to 20% of 5 V	T_{ADRV_fall}		4	5	ns
ADRV Source Current	V_{ADRV} = 2.5 V	I_{ADRV_SRC}	106	136	159	mA
ADRV Sink Current	V_{ADRV} = 2.5 V	I_{ADRV_SNK}	154	200	210	mA
Minimum Pulse Width Allowed		$MIN_{\_PW\_GD}$	210	244	295	ns
ADRV Clamp Voltage	R_{DRV} = 10 kΩ	$V_{ADRV(low)}$	4.5	5	5.5	V
THERMAL SHUTDown						
Thermal Shutdown	Temperature Increasing	T_{SHDN}		150		°C
Thermal Shutdown Hysteresis	Temperature Decreasing	$T_{SHDN(HYS)}$		40		°C

5. On first startup the $V_{FLT(OTP\_out)}$ is set to $V_{FLT(OTP\_out\_1st)}$. If the FLT voltage decreases below $V_{FLT(OTP\_out)}$ after the first soft start the $V_{FLT(OTP\_out)}$ changed to 900 mV.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Introduction

The NCP1568 implements active clamp flyback converter utilizing current−mode architecture where the main switch turn off event is dictated by the peak current. This IC is an ideal candidate for high frequency high−density adapters, open−frame power supplies to name a few. The NCP1568 incorporates advanced control and power management techniques as well as multimode operation to meet stringent regulatory requirement. The NCP1568 is also enhanced with non−dissipative overpower protection (OPP), brownout protection, and frequency modulation in both ACF and DCM mode of operation for optimized efficiency over the entire power range. Accounting for the needs of extremely low standby power requirements, the controller features minimized current consumption and includes a built−in X2 capacitor discharge circuit.

High Voltage Startup

The NCP1568 integrates a high voltage startup circuit accessible through the HV pin. The HV pin also provides access to the brown−out detection circuit as well as line voltage detectors that detect the ac line voltage range and the presence or absence of an ac line. The brown−out detector detects ac line interruptions and the line voltage detector determines the rectified voltage peaks at quantized voltage levels. Depending on the detected input voltage range, device parameters are internally adjusted to optimize the system performance. The HV pin connects to both line and neutral through two diodes to achieve full−wave rectification as shown in Figure 4. A low value resistor in series with the HV pin can be used to limit current in the event of a pin short or surge. The series resistance of the HV pin should not exceed 3 kΩ, as the function of the brown−out and line detection circuits will be hampered. Further, placing a capacitor from the HV pin to ground greater than 22 pF can potentially cause misidentification of line removal.

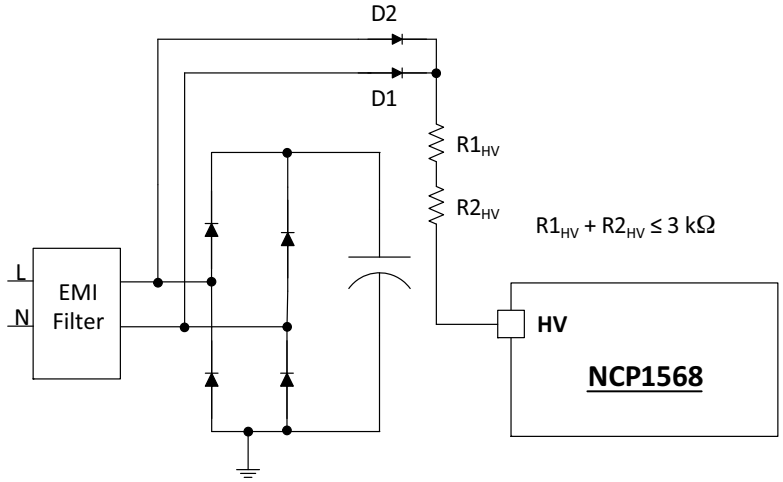


Figure 4. Typical HV Pin Connection

The HV startup regulator consists of constant current sources that supply current from the ac input terminals (V_{in}) to the supply capacitor on the V_{CC} pin (C_{CC}). When the ac input voltage is greater than $V_{HV(discharge)}$ current is sourced from the HV pin to the V_{CC} pin at I_{start1}, typically 0.5 mA until the voltage on the V_{CC} pin exceeds $V_{CC(inhibit)}$ typically 700 mV. Once the $V_{CC(inhibit)}$ threshold has been exceeded, the startup circuit current increases to I_{start2}, typically 3.25 mA. NCP1568 will continue to source I_{start2} from the HV pin to the V_{CC} pin when the voltage is below $V_{CC(on)}$ and the voltage on the HV pin is above $V_{HV(MIN)}$. I_{start2} is disabled if the V_{CC} pin falls below $V_{CC(inhibit)}$. In this condition the startup current is reduced to I_{start1}. The internal high voltage startup circuits eliminate the need for external startup components. In addition, these current sources reduce no load power and increase the system efficiency as the HV startup circuit has negligible power consumption in the normal, light load, and standby operations. During a typical startup, the V_{CC} is charged up to $V_{CC(on)}$ in tstart−up with a 0.47 μF capacitor.

Once the V_{CC} capacitor C_{CC} is charged to the startup threshold, $V_{CC(on)}$, the HV pin startup current sources are disabled and a controller waits for the HV pin sensed brown−out threshold to be exceeded. If the input startup voltage is not met, the startup current sources remain disabled until V_{CC} falls below the minimum operating voltage threshold, $V_{CC(off)}$ after the $tdelay_{(VCC\_off)}$ expires. Once the threshold is reached, the current sources are again enabled to charge V_{CC} back up to $V_{CC(on)}$. Figure 5 shows a typical startup sequence. If the ac input voltage fails to meet the brown−out threshold or a fault is detected on the FLT pin, the part will continue to operate by providing current to V_{CC} capacitor as needed in in Dynamic Self Supply (DSS) until all faults are cleared. Once the $V_{CC(on)}$ threshold is exceeded and the brownout is identified the part will charge up to VCC on and the soft start sequence will

begin. A dedicated comparator monitors V_{CC} and latches the controller into a low power state if V_{CC} exceeds $V_{CC(OVP)}$ for $t_{delay(VCC\_OVP)}$. To reset the OVP fault, the V_{CC} voltage must by less than $V_{CC(reset)}$.

The C_{CC} provides power to the controller during power up. The capacitor must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is ramping up. Otherwise, V_{CC} will collapse and the controller will turn off. The operating IC bias current, I_{CC4}, the high side driver current, and gate charge load at the low side and high side drive outputs must be considered to correctly size C_{CC}. The increase in current consumption due to external gate charge is calculated using the following equation. Since the switching frequency is ramped from 25 kHz to the desired switching frequency, a trapezoidal shape is assumed for the frequency both in the DCM mode, the LEM operation, and ACF mode. The high side driver has no gate drive losses during DCM operation, thus the frequency is set to zero and the switch only has the average of the applied switching time from LEM and ACF operations.

(eq. 1)

$$f_{SW} = \frac{\left(FSW_{MIN} + \frac{FSW_{DCM\_MAX} - FSW_{MIN}}{2}\right) \cdot T_{DCM} + \left(FSW_{DCM\_MAX} + \frac{FSW_{ACF\_MAX} - FSW_{DCM\_MAX}}{2}\right) \cdot \left(T_{SS} - T_{DCM}\right)}{T_{SS}} \rightarrow$$

$$147.1\ kHz = \frac{\left(31.25\ kHz + \frac{100\ kHz - 31.25\ kHz}{2}\right) \cdot 550\ \mu s + \left(100\ kHz + \frac{100\ kHz - 100\ kHz}{2}\right) \cdot \left(16\ ms - 550\ \mu s\right)}{16\ ms}$$

Assuming a typical gate charge of 17 nC for the high side and low side MOSFETs.

(eq. 2)

$$I_{ICC(gate\_Charge\_Total)} = fsw\_ls \cdot Q_{g\_ls} + fsw\_hs \cdot Q_{g\_hs} \rightarrow$$
$$4.96\ mA = 147.1\ kHz \cdot 17 \cdot nC + 144.8\ kHz \cdot 17 \cdot nC \rightarrow$$

Equation 2 has fsw as the average soft start switching frequency of the low side or high side MOSFET and Qg is the gate charge of the external MOSFETs.

Once the C_{CC} is charged to the startup threshold, a delay of $t_{delay(start)}$ is used to stabilize all internal power supplies and ensure biasing is up before operation and level setting can continue. After $t_{delay(start)}$ expires, the IC will not start switching until and timers expire as shown in Figure 6.

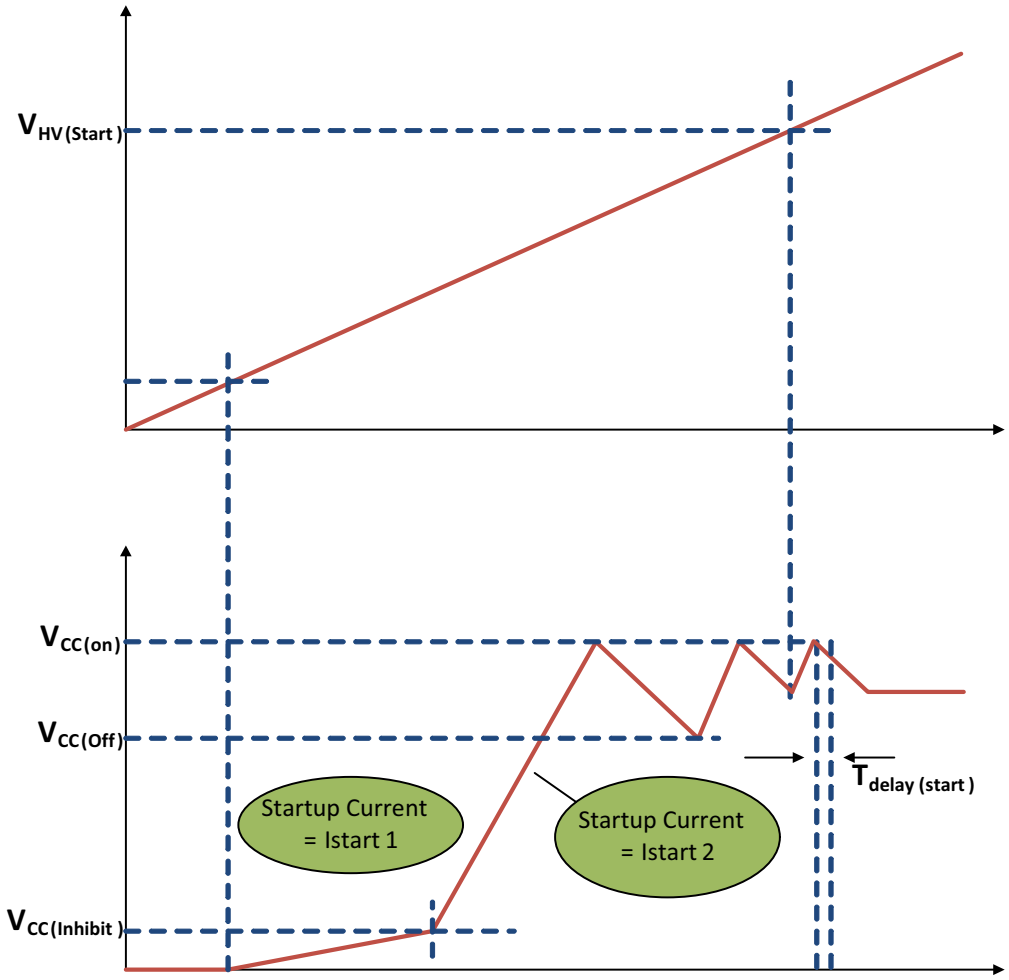


Figure 5. Startup Timing Diagram

The V_{CC} capacitor value must account for the startup delay time, soft start time, and all of the currents provided during that time. Equation 3 shows the calculated capacitance to soft start without the V_{CC} voltage dipping below the $V_{CC(OFF)}$ threshold. The capacitance value provided by the equation should be increased by 20% to allow for capacitor tolerances. Further increases may be made by the designer to account for operating temperature range.

$$C_{VCC\_MIN} = \frac{\left(T_{Delay(Start)}\right) \cdot \left(I_{CC1} + I_{DRVQ}\right) + \left(T_{Soft\_start1} + T_{MODE\_SAM1}\right) \cdot \left(I_{CC3} + I_{DRV} + I_{CC(gate\ charge)}\right)}{V_{CCON} - V_{CCOFF}} \quad \text{(eq. 3)}$$

$$24.4\ \mu F = \frac{(0.05\ ms) \cdot (0.15\ mA + 0.200\ mA) + (4\ ms + 8\ ms) \cdot (4.27\ mA + 4\ mA + 4.96\ mA)}{15.5\ V - 9.0\ V}$$

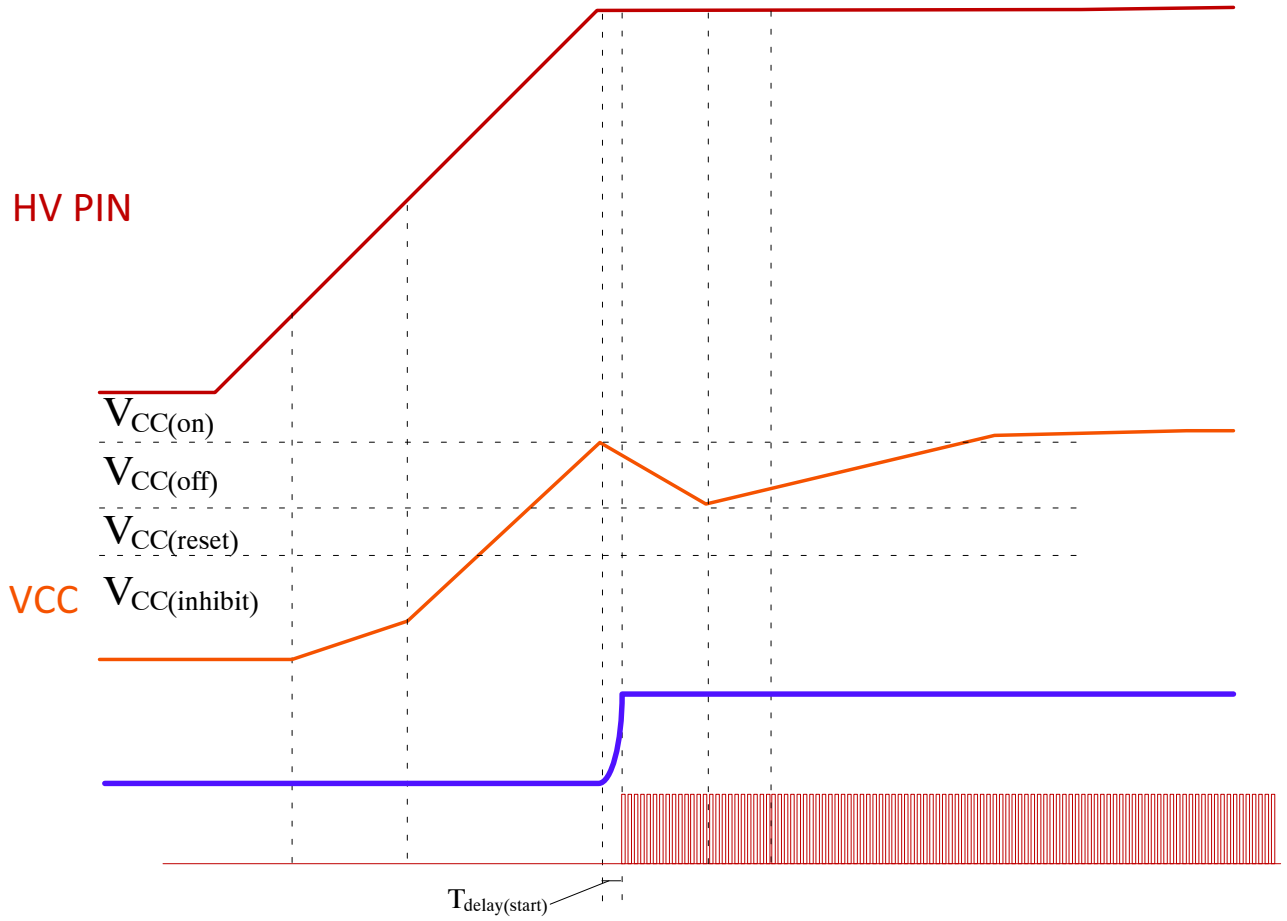


Figure 6. Normal Startup Timing Diagram and Delays

HV Currents and No load Operation

When considering no load operation it is important to understand that the NCP1568 has a static loss on the HV pin due to off state leakage currents. The DC leakage currents on the pin are shown in the datasheet as $I_{HV(Off1)}$, $I_{HV(Off2)}$, $I_{HV(Off3)}$.

Brown−Out Detection

The HV pin provides access to the brownout and line voltage detectors. Once V_{CC} reaches $V_{CC(on)}$ the HV pin to VCC Pin current sources (I_{start1} and I_{start2}) are turned off. Once the current sources are turned off the line voltage is assessed to determine if the brownout level has been exceeded. The line is not assessed any time the NCP1568 is sourcing current to the VCC Pin. The startup sequence is initiated once V_{HV} is above the brown−out threshold ($V_{HV(start)}$) for $t_{delay(HV\_start)}$ and the VCC voltage has been charged back up to $V_{CC(on)}$ by I_{start2}. Every time the HV voltage drops below the $V_{BO(stop)}$ the $t_{dealy(HV\_stop)}$ typically 300 μs timer starts and if the voltage has not exceeded the $V_{BO(start)}$ the $T_{HV(stop)}$ timer is initiated. The timer, $T_{HV(stop)}$, typically 50 ms, is set long enough to ignore a two cycle drop−out. If the timer $T_{HV(stop)}$ expires, a brownout condition is established and drive pulses are terminated. If the HV voltage is greater than $V_{BO(start)}$ for $t_{dealy(HV\_start)}$ the $T_{HV(stop)\ timer}$ is reset and normal operation continues. Figure 7, and Figure 8 show typical brown−out waveforms and the state flow diagram.

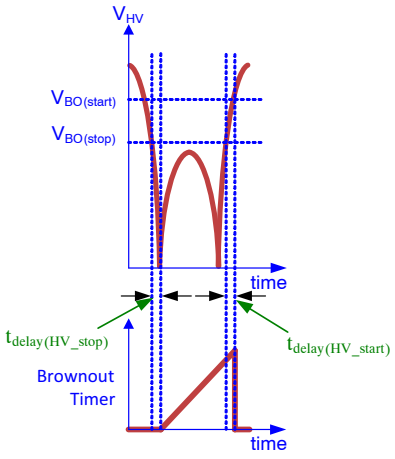


Figure 7. Brownout Filter Timing

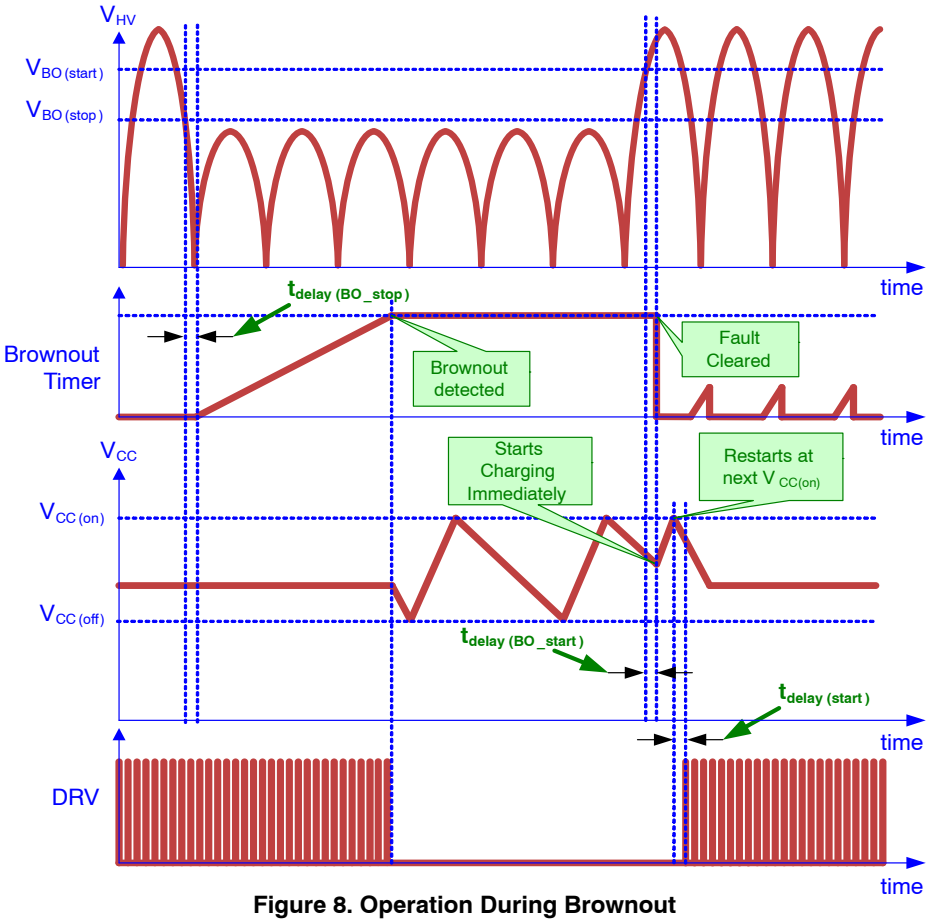


Figure 8. Operation During Brownout

Line Detection

The input voltage range is detected based on the peak voltage measured at the HV pin. Many aspects of the NCP1568's performance are modified based on the line voltage. Some key features that are changed with line voltage are: Over Power Protection (OPP), current limit, and ACF to DCM transition thresholds. Please refer to appropriate sections for more information. The controller compares a divided version of V_{HV} to internal line select thresholds. The thresholds can be trimmed with 4 bits as shown in the electrical table.

The default power−up mode of the controller is low line. No line changes are applied until after the soft start has completed and soft start wait or the forced ACF period has ended to ensure a repeatable reliable soft start free from glitches. Once soft start wait has completed, the system is free to apply changes to parameters based on line voltage. On each line cycle the increasing voltage is sensed and the controller updates the measured high voltage level continuously. The continuous updating is used to determine slope and levels. The HV detector uses internal comparators and a divided down version of the HV voltage to digitally track the progress of the line as it increases and decreases. During the first line cycle measured, the HV detector increases the maximum values it measures upon each increasing voltage reference trip level. The values will continue to be updated until the maximum voltage is reached. The HV detector will continue to measure voltages as they decrease. When the HV detector measures a 2 level decrease, it knows a maximum was detected. The internal digital detection then holds the current value and adds 2 levels to obtain the peak value. The new value is then referred to as the Held Maximum HV Value (HMHVV). To update the HMHVV, the peak measurement current HV Value (CHVV) must be repeated twice. If a large increase or decrease in voltage occurs, the HV detector is only allowed to increment or decrement the HMHVV one level every 100 ms. An analog front filter of 253 μs $t_{delayline}$ is used to ensure glitches high or low are not used to change levels. Note that some line dependent functions use the CHVV and some functions use the HMHVV, please refer to the appropriate section for the value used.

Line Removal (X2 capacitor discharge)

Safety agency standards require the input filter capacitors to be discharged once the ac line voltage is removed. A resistor network is the most common method to meet this requirement. Unfortunately, the resistor network consumes power across all operating modes and it is a major contributor of input power losses during light−load and no−load conditions.

The NCP1568 eliminates the need for external discharge resistors by integrating input filter capacitor (X2) discharge circuitry. A novel approach is used to reconfigure the high

voltage startup circuit to discharge the input filter capacitors upon removal of the ac line voltage. The line removal detection circuitry is always active to ensure safety compliance.

Line removal is detected by digitally sampling the voltage at the HV pin and monitoring the slope. A timer, $t_{line(removal)}$ (typically 80 ms), is used to detect when the slope of the input signal is negative or conversely not positive, or below the resolution level. The timer is reset anytime a positive slope is detected. Once the $t_{line(removal)}$ timer expires, a line removal condition is acknowledged, switching is stopped, and an X2 capacitor discharge cycle begins.

Once the X2 condition is acknowledged, I_{start2} (typically 3.5 mA) is turned on and will remain on for the discharge cycle to discharge the input filter capacitance and the $t_{line(discharge)}$ timer is started. When the X2 removal is acknowledged, the I_{start2} current, X2 discharge circuitry consisting of Vcc monitors, and a pull down current $I_{CC(discharge)}$ (typically 18 mA) is enabled. If V_{CC} is above $V_{CC(on)}$, it is first discharged to $V_{CC(on)}$ by the $I_{CC(discharge)}$ current. Once the voltage decreases below $V_{CC(ON)}$, $I_{CC(discharge)}$ is turned off, and I_{start2} charges V_{CC} until the voltage increases to the $V_{CC(X2\_reg)}$ level on the V_{CC} pin. Once the $V_{CC(X2\_reg)}$ level is exceeded, the $I_{CC(discharge)}$ is turned on once again to discharge the V_{CC} pin. The process continues until the $t_{line(discharge)}$ timer expires. Once the timer expires, $I_{CC(discharge)}$ remains on until the V_{CC} voltage decreases to $V_{CC(on)}$, at which time it starts a second timer, $t_{line(detect)}$ (typically 32 ms). The $t_{line(detect)}$ timer is used to ensure the IC does not overheat and to allow the HV pin to monitor the input voltage to determine if AC voltage has been applied again. Once the detection phase is complete, $t_{line(discharge)}$ is again activated if line voltage activity is not detected, and the X2 capacitor continues to discharge. The discharging process is cyclic and continues until the AC line is detected again or the voltage across the X2 capacitor is lower than $V_{HV(discharge)}$ (30 V maximum). If AC line voltage is detected, V_{CC} is charged up to $V_{CC(on)}$ from the HV pin via I_{start2} and the soft start process will begin. **It is important to note that the HV pin cannot be connected to any dc voltage due to this feature, i.e. directly to the bulk capacitor without disabling the feature.**

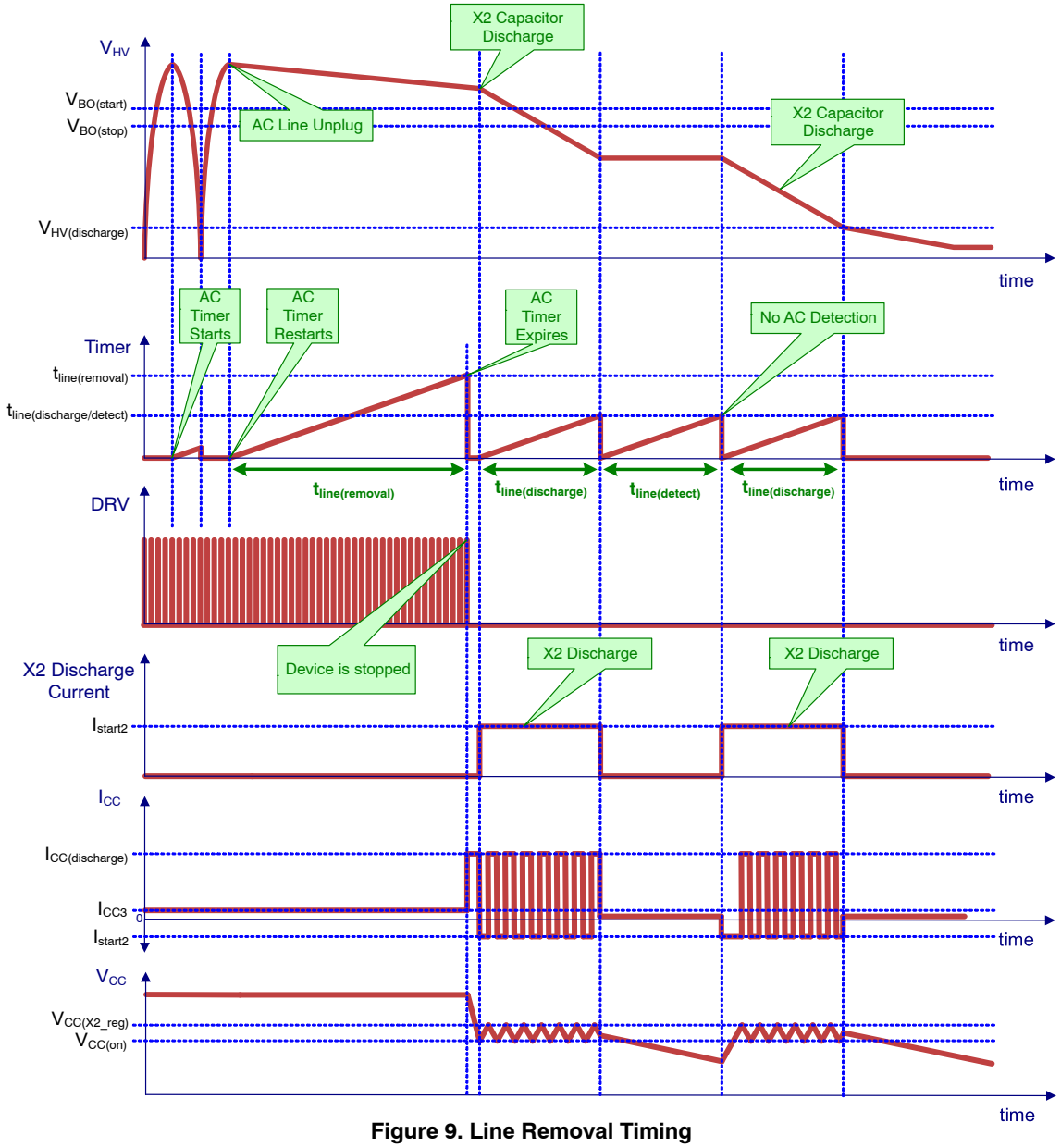


Figure 9. Line Removal Timing

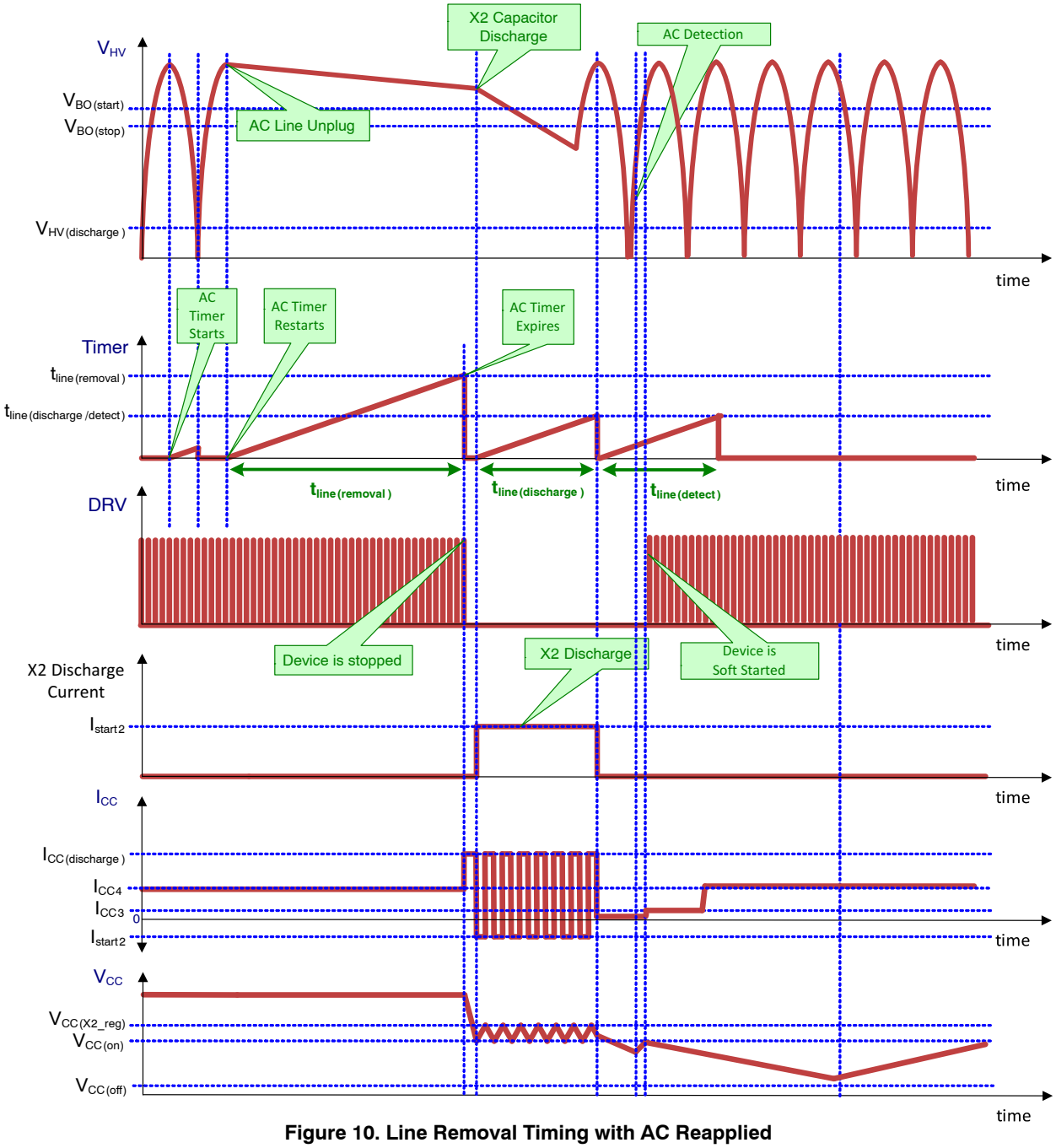


Figure 10. Line Removal Timing with AC Reapplied

PWM Architecture

The NCP1568 implements peak current mode control architecture for pulse width modulation. Peak current mode control simplifies the loop compensation and typically will result in a simple Type II compensator. With relatively simple compensation schemes, aggressive bandwidths can be achieved compared to a standard voltage mode control. Further, it inherently provides current limiting while also providing a line feed−forward resulting in excellent line transient response. However, peak current mode control is susceptible to sub−harmonic oscillation for duty cycles greater than 50%. Sub−harmonic oscillation is characterized by alternating narrow and wide pulse−widths. To prevent subharmonic oscillation, NCP1568 also features additional slope compensation.

The NCP1568 features multi−mode operation to optimize efficiency across line and load conditions. Below are the modes of operation:

1. Active Clamp Operation with variable frequency
2. Transition from ACF Mode to DCM Mode and vice−versa.
3. Discontinuous Conduction Mode with Frequency Foldback
4. Skip Mode

Multi−Mode Algorithm

Multi−mode algorithm is implemented in the NCP1568 to optimize the efficiency across load conditions. The magnetizing current is in continuous conduction mode (CCM) in the active clamp operation. Therefore, when the power supply is in standby condition the active clamp flyback topology will work at high peak currents and the primary side clamp FET along with the main FET will form a synchronous buck−boost structure with magnetizing current traversing both the first and the third quadrants.

At light load, in an ACF topology, high peak currents will result in high conduction losses, core losses, and copper losses while achieving ZVS. At light load, ZVS will not offset the three large loss contributors and the efficiency will be lower compared to DCM operation.

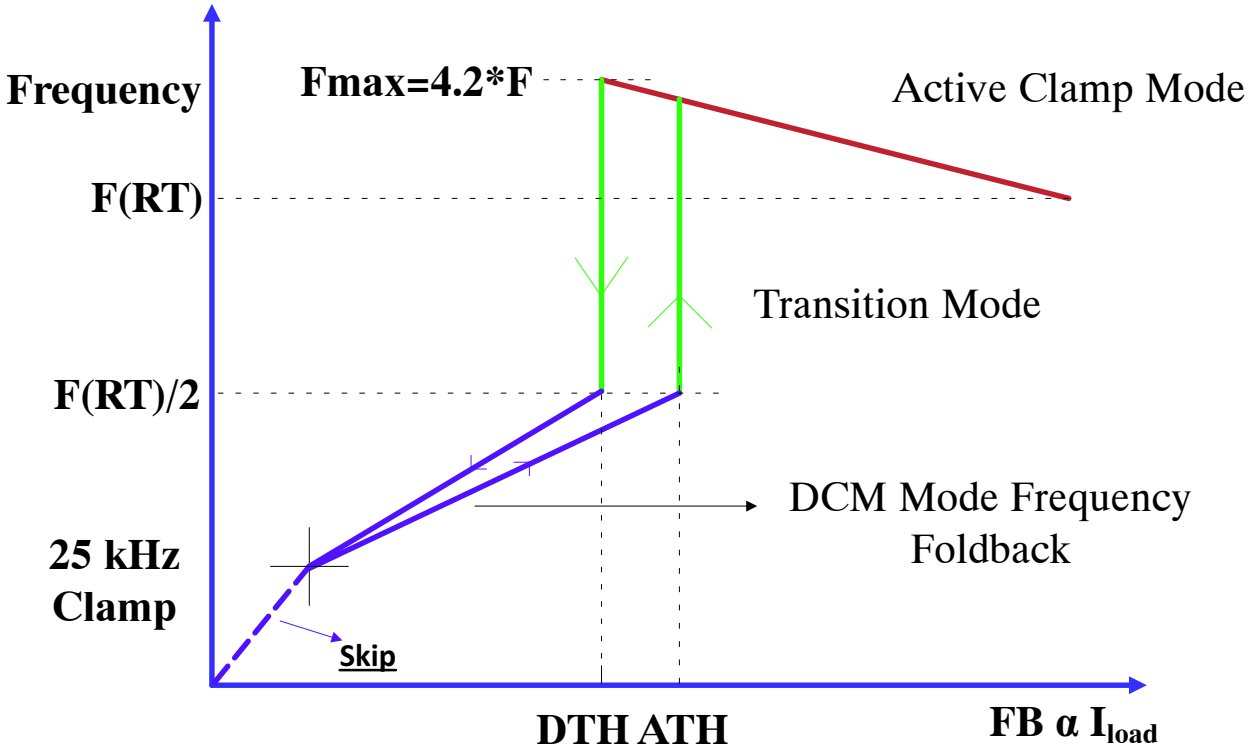


Figure 11. Frequency Transition from No Load to Full Load and DCM To ACF Operation

Oscillator

In NCP1568 the RT resistor sets the minimum frequency of operation for the internal oscillator. Typically, for an active clamp flyback topology minimum frequency is selected to be at its lowest input voltage, lowest intended output voltage and maximum load current.

An internal amplifier forces 2 V on the RT pin, the current sourced from the resistor on the RT pin is used by the internal oscillator to set the minimum switching frequency. The frequency set by the RT resistor follows the equation noted below:

$$F_{OSC} = \frac{1}{RT \cdot 100\ pF} \rightarrow 100\ kHz = \frac{1}{100\ k\Omega \cdot 100\ pF} \quad \text{(eq. 4)}$$

Where F_{OSC} is the frequency set by the RT resistor value. The frequency programmed at the RT pin sets the minimum ACF switching frequency. The curve below shows the RT resistor vs. the oscillator frequency from 10 kΩ to 100 kΩ. The minimum RT resistor value is 10 kΩ.

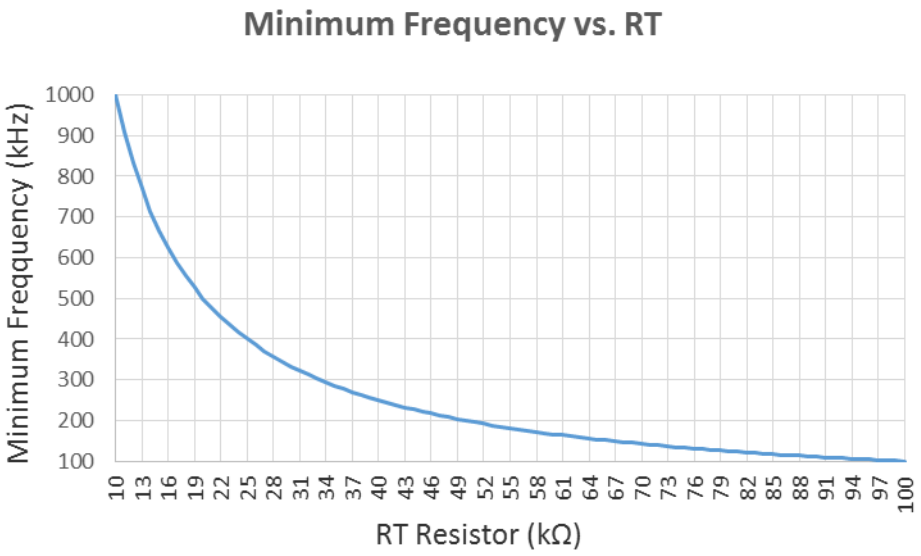


Figure 12. Minimum Oscillator Frequency vs. RT

On and Off Time Restrictions

The NCP1568 has internally set options to have a minimum off time of 400 ns or 750 ns shown in Figure 12 that is always imposed in ACF mode. The minimum off time is to ensure that enough time remains in each switching cycle to fully execute a successful high side pulse. The minimum off time is constant, but the IC also has a maximum duty cycle of 80% to allow refreshing of the high side switch and avoided transformer saturation. The maximum duty cycle is therefore not constant, as the minimum off time must be maintained to continue ACF operation past a certain operating frequency. With a constant off time of 400 ns, the maximum duty cycle is governed by the minimum off time past 500 kHz. The resulting frequency vs duty cycle plot is shown in Figure 13. Equation 5 shows the maximum duty ratio.

(eq. 5)

$$\begin{bmatrix} \text{Duty\_Ratio} = 80\% \\ \text{Duty\_Ratio} = 1 - \text{FSW} \cdot 0.4 \cdot \mu\text{s} \end{bmatrix} \begin{bmatrix} \text{FSW} < 400\ \text{kHz} \\ \text{FSW} > 410\ \text{kHz} \end{bmatrix}$$

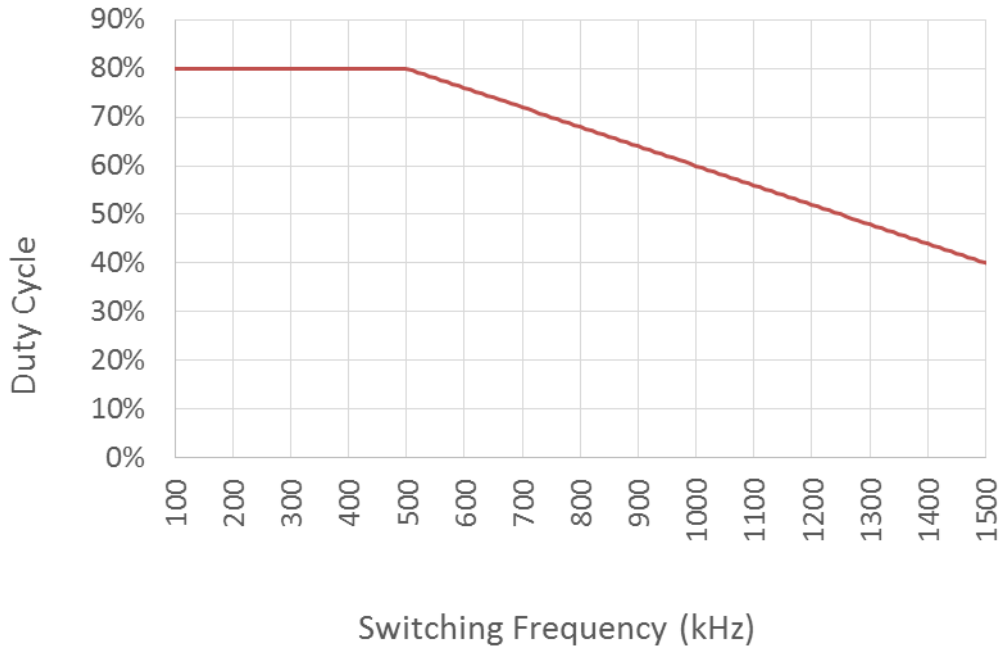


Figure 13. Switching Duty Ratio

ACF Oscillator Operation

In order to minimize the power loss in an ACF, as load is decreased and as input voltage is increased, the frequency of the operation needs to be increased such that the additional circulating current is kept to a minimum. The negative current needed for ZVS is typically in the order of −0.5 A for super junction FETs. The current could be lower for wide band gap devices such as GaN as their Coss is typically lower. Keeping the negative magnetization current relatively constant is accomplished digitally by adjusting the frequency of the oscillator until a predetermined dead−time is seen across the line and load conditions.

A time reference is established in the NCP1568 and an error signal is accumulated based on the time it takes to transition and achieve ZVS. If the switch node transitions fast and ZVS occurs before the reference time, then there is more than enough energy to reset the node quickly then the frequency is increased or the off time reduced such that less energy is available for resetting the switch node and as such will result in less required on time for the low side switch and a smaller Δ IM. The smaller Δ IM results in fewer losses in the system. If the switch node ZVS occurs coincident with the time reference, no frequency adjustment is necessary. If the ZVS occurs after the reference, the frequency is too high and needs to be reduced to ensure good ZVS. Finally, if the ZVS never occurs and instead reaches a maximum allowable time limit ($D_{T\_Max\_1}$), the current switching cycle will start the LDRV, but the maximum frequency reduction will be applied to the following switching cycle.

The net result is that the duty ratio would be maintained, the load current would be supported, and the frequency would adjust with load to provide enough energy to achieve ZVS.

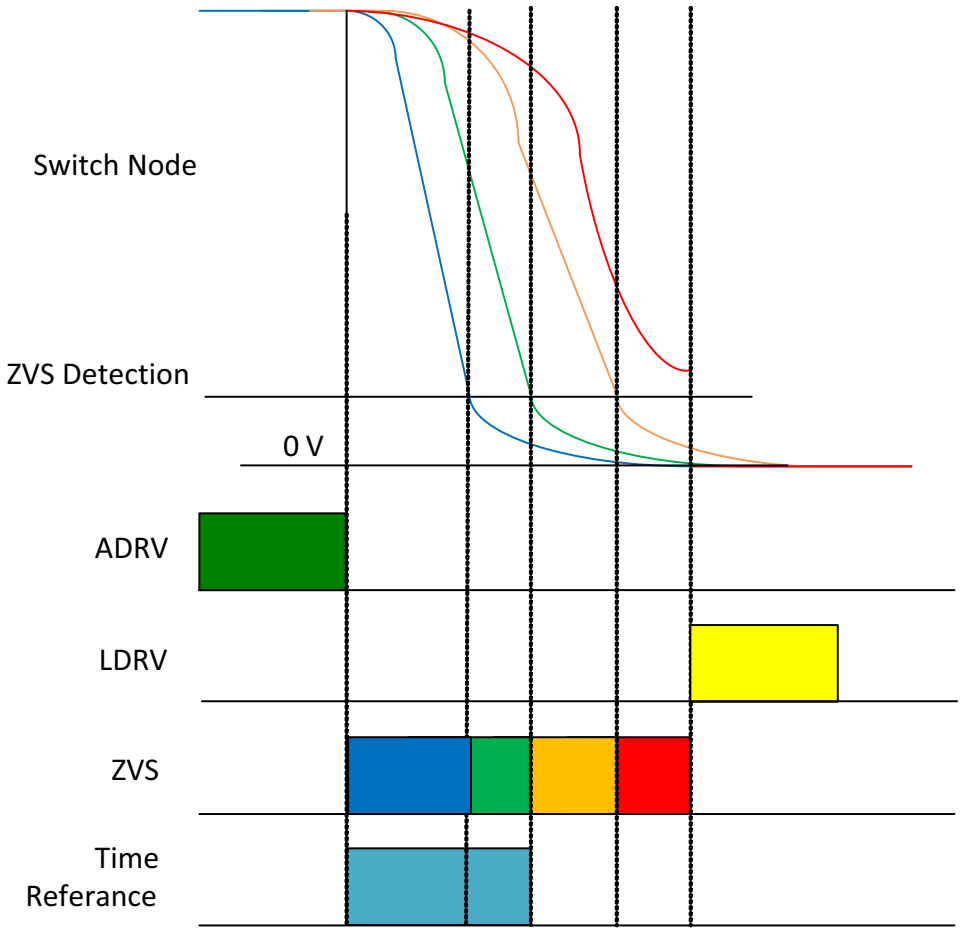


Figure 14. Time Referenced Digital Modulation of Operating Frequency Regulating the ZVS Point

DCM Oscillator Operation

In DCM mode of operation, the frequency is dependent on the DCM to ACF threshold setting, the FB voltage and the frequency change option. The maximum oscillator frequency can be 1/2, 1/3, or 1/4 of the minimum frequency set by the RT resistor. A frequency foldback proportional to the FB pin is also implemented in the DCM mode. Please refer to the frequency foldback section for a description. The options for frequency foldback highest frequency are shown in Table 5.

Table 5. MAXIMUM DCM FREQUENCY FOLDBACK OPTIONS

Option	DCM Maximum Frequency (kHz)
1	FOSC/2
2	FOSC/3
3	FOSC/4
4	FOSC

Frequency Foldback

The combination of mandated agency stand−by power and light load efficiency targets at various load points necessitates the need to change the frequency of operation when the IC is in DCM mode. In DCM operation the frequency is the highest once the FB reaches a settable V_{DTH} threshold, the frequency of operation is reduced as FB voltage falls with its lowest point at the $V_{FB(skip)}$ skip threshold. Since the DCM to ACF threshold is programmable, the VCO must change slopes based on the selected V_{DTH} threshold as shown in Figure 15. In frequency foldback mode the NCP1568 works with peak current setting the on time employing variable frequency control from the $V_{TH\_DCM\_ACF}$ threshold to the $V_{FB(Ipk\_freeze)}$ threshold for the outer loop. Once the FB voltage reaches $V_{FB(Ipk\_freeze)}$ on the FB pin, the peak current floor is frozen to the $V_{CS(\ Ipk\_freeze)}$ value. The IC can produce a peak current that is greater than the $V_{CS(\ Ipk\_freeze)}$ if the PWM comparator requires a longer on time to satisfy the control loop as shown in Figure 15. Freezing the peak current to a minimum accelerates the slope of the frequency foldback. The peak current is frozen and the oscillator frequency is changed to maintain output voltage regulation. As the load decreases, the frequency will keep decreasing until it stops at the minimum frequency clamp of $F_{OSC(min)}$ 25 kHz. The minimum frequency occurs at the $V_{FB(skip)}$ threshold, typically at 400 mV on the FB pin. At this threshold, skip cycle operation is enabled.

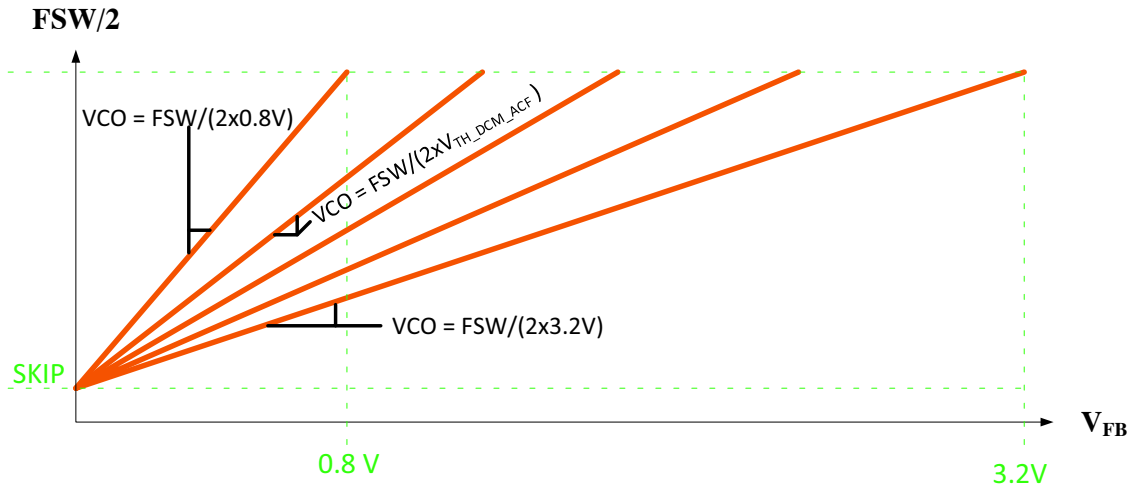


Figure 15. VCO Frequency Change with V_{DTH} Voltage Selection

Minimum Frequency Clamp and Skip Mode

The minimum switching frequency clamp prevents the switching frequency from dropping below $F_{OSC(min)}$ (25 kHz typical). When the switching cycle is longer than 40 μs, a new switching cycle is initiated. Since the NCP1568 forces a minimum peak current and a minimum frequency, the power delivery cannot be continuously controlled to zero load. Instead, the circuit starts skipping pulses when the FB voltage drops below the skip level, $V_{FB(skip)}$, and recovers operation when VFB exceeds $V_{FB(skip)} + V_{FB(skip)\_hys}$. The skip−mode method provides an efficient method of control during light loads.

Optional Quiet−Skip

There is an option in NCP1568 to enable quiet skip. Quiet skip is suitable for high output voltage and fixed output operation. To avoid acoustic noise, the quiet skip circuit prevents the burst frequency during skip mode from entering the audible range by limiting the time between pulse bursts to a maximum of 800 Hz. The pulse burst frequency is achieved via a timer (T_{Quiet}) that is activated during the rising edge of the first pulse of Quiet−Skip. The start of the next burst cycle is prevented from starting until this timer has expired.

When the output power decreases, the switching frequency decreases. Once the switching frequency decreases to 25 kHz, the skip−in threshold is reached and burst mode is entered. When FB is lower than $V_{FB(skip)}$ switching the IC finishes its current switching cycle then enters into Quiet−Skip. An internal flag is then set to indicate burst mode operation.

Once switching stops, FB will gradually rise and crosses the skip−exit threshold which is $V_{FB(skip)}$ + $V_{FB(skip)hys}$, drive pulses will resume, but the burst mode flag remains set as shown in Figure 16. When at this point, a 1250 μs (typ) timer, T_{Quiet}, is started together with a count−to−3 counter. The next time the FB voltage drops below the skip−in threshold $V_{FB(skip)}$, drive pulses stop at the end of the current pulse as long as 3 drive pulses have been counted (if not, they do not stop until the end of the 3rd pulse). The skip−exit threshold does not start pulses as they are not allowed to start again until the timer expires and the FB exceeds the skip−exit threshold. When the IC is below the $V_{FB(skip)}$ threshold, the IC draws I_{CC2} (typically 210 μA).

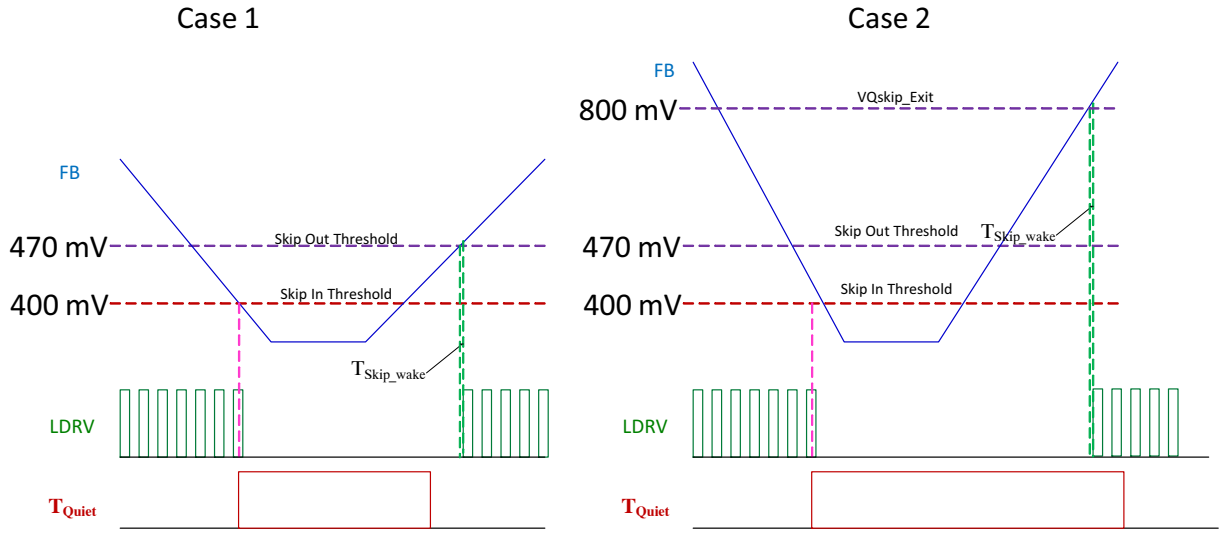


Figure 16. Skip Threshold

During no−load, there will be a minimum of 3 drive pulses, and the burst−cycle period will likely be much longer than 1250 μs. The quiet skip operation helps to reduce power consumption at no−load conditions.

Frequency foldback is still active while the burst mode flag is set. When FB raises, the frequency is modulated according to the ATH pin set VCO curves and the RT resistor. Figure 16 shows the VCO curve for three cases; it is possible for the burst mode flag to be set with the controller operating in frequency foldback mode, i.e. the drive pulses never stop.

In order to clear the burst mode flag, the FB voltage must rise higher than V_{Qskip_Exit0} (typically 800 mV). If this occurs before T_{Quiet} expires, the drive pulses will resume immediately, i.e. the controller won't wait for the timer to expire. Figure 16 provides an example of Quiet−Skip functionality.

The T_{Skip_wake} time (typically 24 μs) is the duration required to initialize and stabilize the IC once the FB pin has crossed the $V_{FB(skip)}$ + $V_{FB(skip)hys}$ and the T_{Quiet} timer has expired. The IC must also wait for T_{Skip_wake} if the time T_{Quiet} has not expired, but the FB voltage has exceeded the Qskip exit as shown in Figure 16.

DCM TO ACF Transition (ADRV Soft−Start)

Once all of the criteria to transition from DCM to ACF Mode have been met, the NCP1568 soft−starts ADRV employing leading edge modulation (LEM). The ADRV soft−start slowly discharges the energy stored in the clamp capacitor in DCM operation to the output. During the ADRV soft−start time, $T_{DCM\_ACF\_Trans1}$, ADRV pulses will increase from a minimum of approximately 250 ns to 1−D in a linear fashion.

Figure 17 shows leading edge modulation of ADRV during the DCM to ACF transition. The secondary current shape starts to resemble that of resonant current during the LEM period and eventually resonant current can be seen throughout the 1−D cycle as the ADRV soft−start is finished.

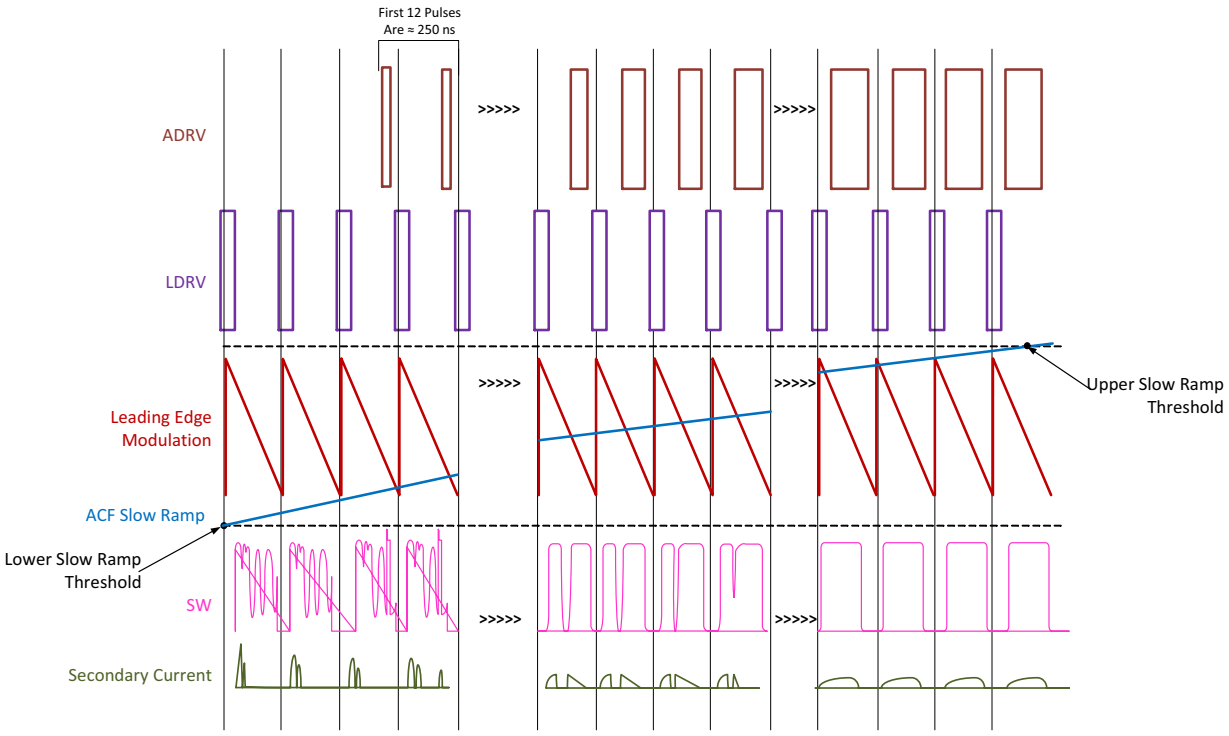


Figure 17. Leading Edge Modulation of ADRV during DCM to ACF

Transition Hard Switch Avoidance

Before the high side switch begins the LEM process, the switch node demagnetizes and rings as a classic flyback would. During the start of LEM, the switch node demagnetization is interrupted by the switch node pulling up to the clamp capacitor voltage. The time the switch node is pulled up to the clamp capacitor voltage steadily increases and the demagnetization switch node signature continues to increase the amplitude of resonation. Either the LEM finishes with no ringing to ground and is in full ACF Mode of operation or the switch node is clamped on a falling edge ring to ground by the body diode of the low side MOSFET. When the body diode of the low side MOSFET is conducting, turning on the high side switch creates a disturbance to the system, drains the energy in the clamp capacitor, and causes large spikes on the primary and secondary side of the transformer. To avoid disturbing the system, an option to avoid hard switching during LEM is available. This option is primarily useful for Si FETs.

ACF to DCM Transition (ADRV soft−stop)

In ACF Mode, when the system determines it is time to move from ACF operation to DCM operation by comparing an externally set voltage threshold via the DTH pin against FB voltage, an internal timer T_{Trans} is initiated. During this time, the active clamp FET (ADRV) duty cycle is decreased in a controlled fashion over multiple cycles. At the same time, a non−linear frequency foldback to half the frequency (1/2*Fosc) set by the RT resistor is also implemented.

A leading edge modulation technique employed to soft stop the active clamp FET. The soft−stop time $T_{ACF\_DCM\_trans}$ is typically around 500 μs a diagram of the soft stop shown in the Figure 18.

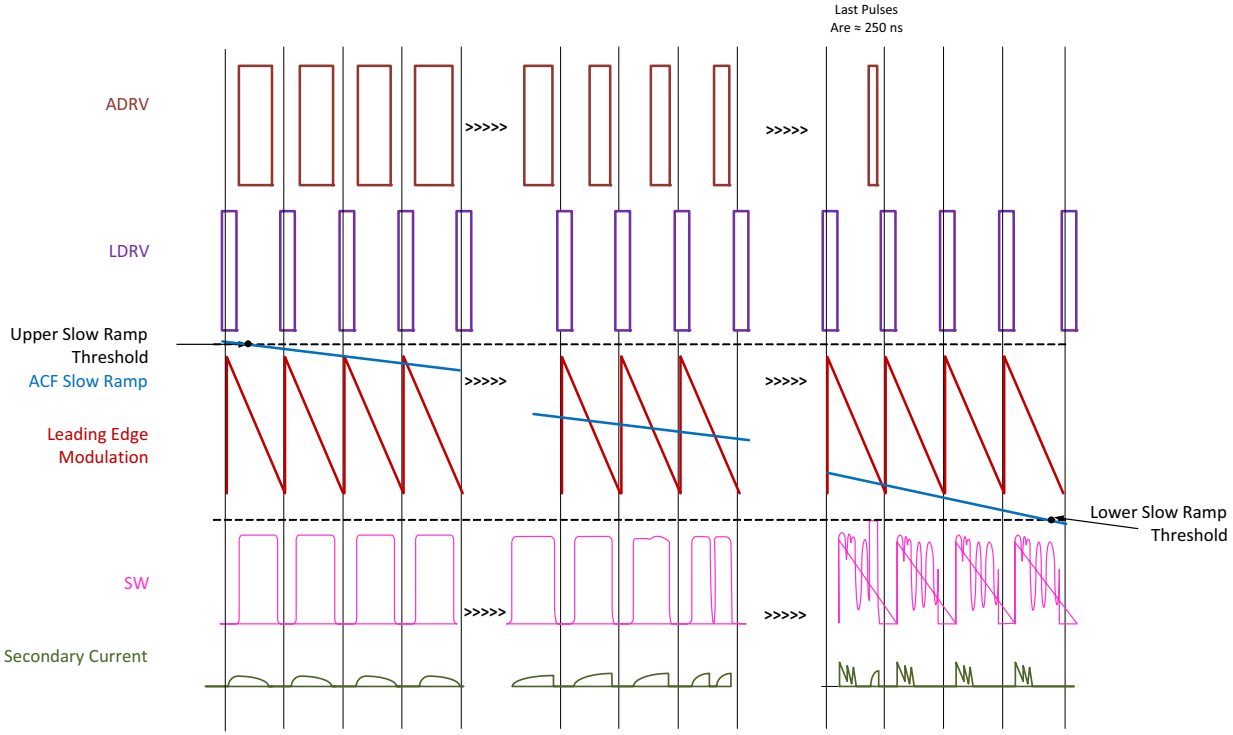


Figure 18. ACF to DCM Transition Waveforms

ATH Pin Functionality

The function of the ATH pin is to set the DCM to ACF threshold. The threshold is set with a fixed current and a resistor to create an analog voltage. The analog voltage is quantized into bins; each bin is mapped to a precise internal reference voltage which is compared against feedback to transition into ACF operation.

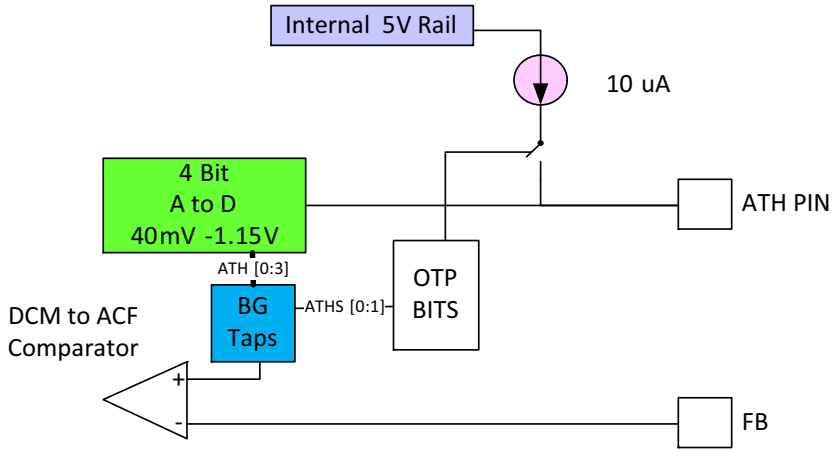


Figure 19. ATH Setting Threshold System Diagram

ATH Pin Turn On and Sourcing Current

The ATH pin current is sourced once V_{CC} exceeds the V_{CC} on threshold. The sourced current is 10 μA +/− 1.5%. Current is sourced from the pin during all normal operating conditions, DCM operation, ACF operation, and skip. Turn on timing for the ATH pin current source is shown in Figure 20.

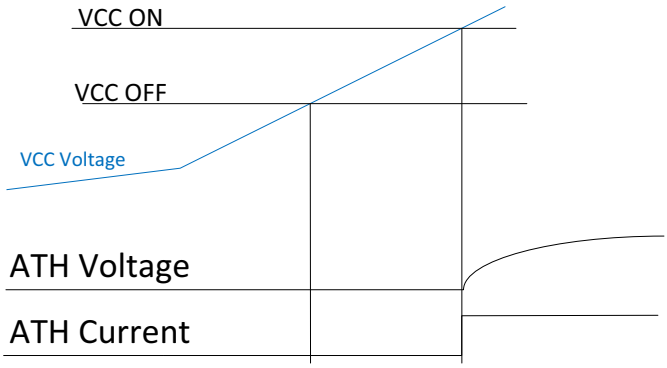


Figure 20. ATH Setting Threshold

Resistor Setting Range

Once a bin is selected, the selected bin maps to a set internal voltage. The voltage measured on the ATH pin only serves to select a digital bin and its tolerance does not affect the internally selected voltage. The mapped reference taps have a tolerance of 2.5%. Table 6 includes the DCM to ACF binning thresholds and resistor map.

Table 6. ATH RESISTOR SET VALUES

R96 Resistor (kΩ)	Internal reference for FB trip point (V)
	2.24
190.6	2.24
161.2	2.16
139.6	2.08
118	2
102.2	1.92
86.4	1.84
74.8	1.76
63.2	1.68
53.4	1.6
46.4	1.52
39.2	1.44
33	1.36
27.4	1.28
22	1.2
18.2	1.12
	ACF ONLY

DTH Pin Functionality

The DTH pin is a real time pin that is observed continuously once soft start has completed and forced ACF time (please refer to soft−start section) has expired. Once V_{CC} has exceeded the V_{CC}(on) threshold, the DTH pin will begin sourcing 16 μA. The pin will be specified with a maximum capacitance of 1 nF to ground. The resistance range that will be applied to the DTH pin can range from 0 Ω to 187.5 kΩ to set a voltage threshold between 0 V and 3 V. The most common anticipated ACF to DCM thresholds are shown in Figure 21. The DTH current source is turned off in DCM mode.

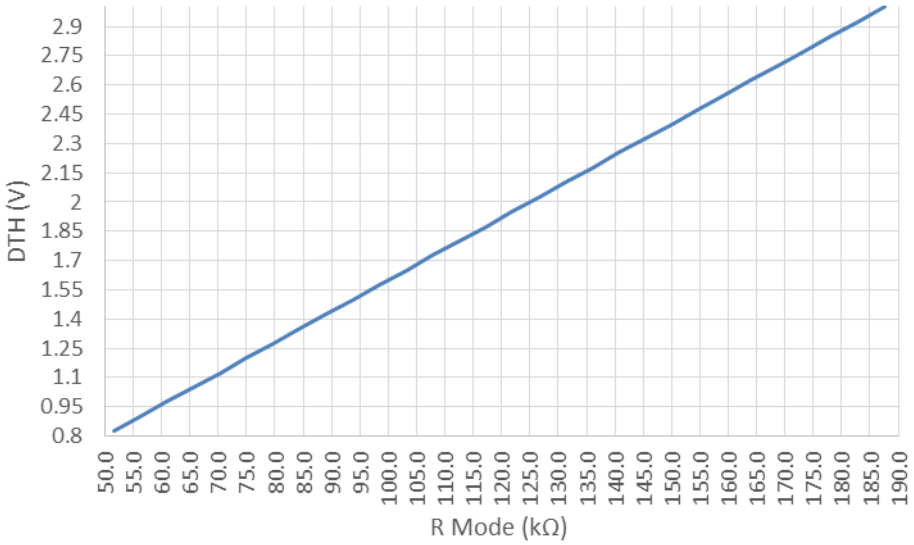


Figure 21. Setting Threshold for DTH PIN

Soft Start

The soft−start of the NCP1568 is initiated once all of the criteria has been satisfied for the V_{CC} to reach $V_{CC(on)}$, V_{HV}>$V_{HV(Start)}$, no other faults are present and $t_{delay(start)}$ is expired. Before the first pulses of the LDRV is initiated, the FB voltage is held high by the internal pull up current source tied to an internal 5 V source. During normal operation, the optocoupler regulates this node but it is not regulated until the output voltage is greater than the reference voltage and the forward diode drop of the optocoupler. The IC will want to transition to ACF Mode immediately on the first switching pulse as the FB voltage will be higher than any threshold that can be set by the ATH pin. The IC's natural tendency is to transition to ACF Mode when heavy loads are applied to the output. Thus, all of the criteria are met to enter the ACF soft start, but the boot pin for the high voltage level shifter and driver is not charged. The NCP1568 works in DCM operation for the first part of the soft start T_{DCM_SS} (typically 580 μs) to make sure that boot capacitor is charged. During the soft−start, the PWM pulse width is gradually increased by ramping the internal current limit reference to its final value. Once, it reaches its maximum value, the IC then operates in ACF mode.The IC must wait for an additional time referred to as T_{MODE_Sam} (typically twice the soft start time). After T_{MODE_Sam} expires, the ACF detection circuits and logic are no longer manipulated but are allowed to transition as the state diagram would normally indicate.

Forced DCM

The forced DCM operation allows a sufficient number of low side pulses to charge the high side drivers boot capacitor and to allow the driver sufficient time to preform internal startup sequences. The maximum current provided to the output for the first few switching cycles is regulated by the minimum on−time. Minimum on−time is a sum of LEB, propagation delay of CS comparator, gate drive, and the MOSFET turn off. To reduce primary and secondary start up current stress, the frequency is ramped to half the oscillator frequency set by RT during the first 580 μs (typ).

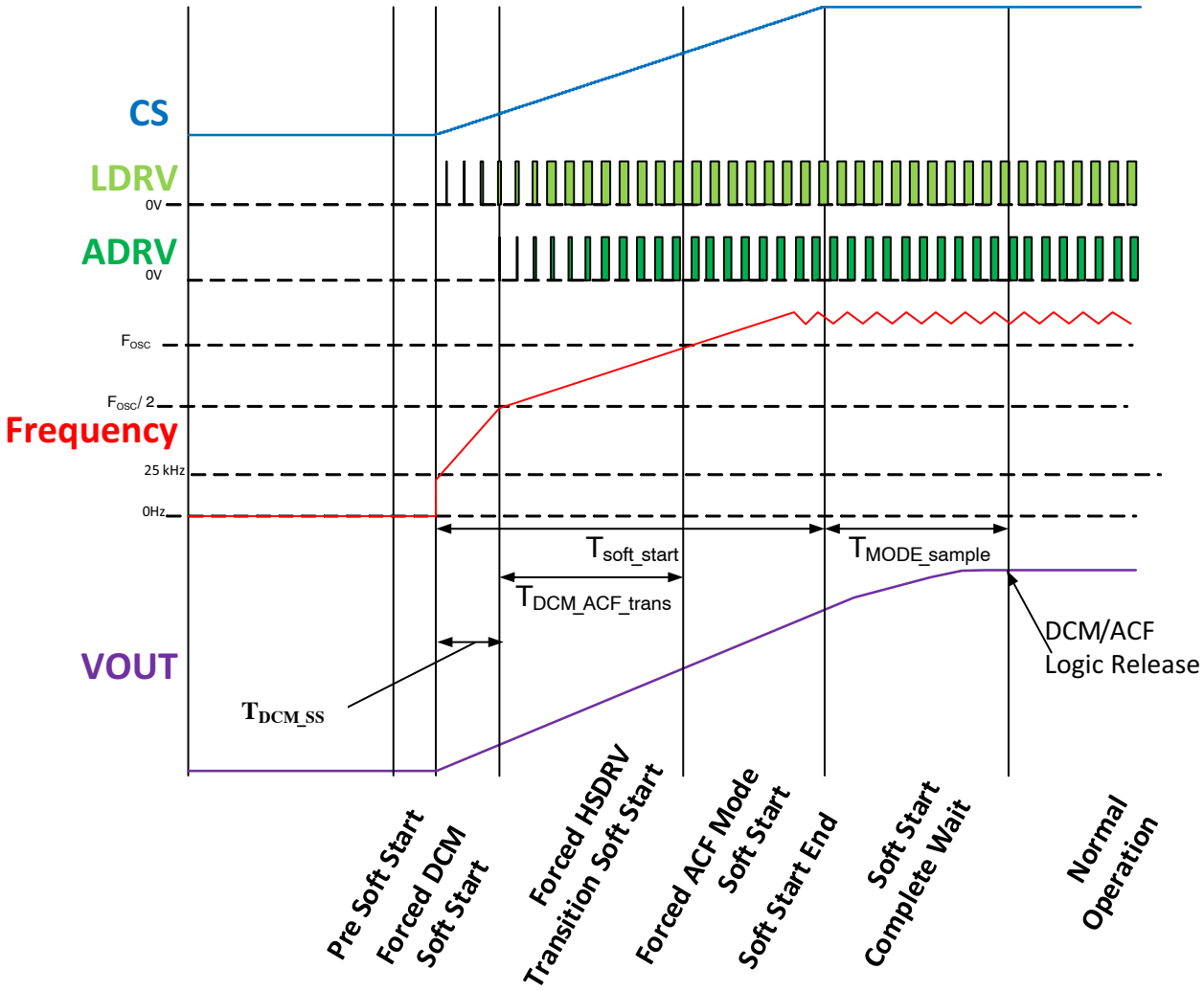


Figure 22. Duty Cycle and Frequency Modulation

Slope Compensation

Fixed frequency peak current mode control architecture is prone to sub−harmonic oscillation for D > 0.5. Sub−harmonic oscillations are typically characterized by observing the SW node alternating wide and narrow pulse−widths. An additional compensating ramp, if either added to the sensed inductor current or subtracted from the loop error voltage (FB), will prevent the sub−harmonic oscillations. In a flyback topology employing current mode control, the slope of this stabilizing ramp also known as slope compensation, is proportional to the down slope of the power converter (Vout/L). The minimum amount of slope compensation to negate the oscillation is equal to 1/2 the down slope. However, for dead−band compensation, the ramp is equal to one times the down slope. Note that with higher slope compensation, the power converter's AC characteristics will start resembling that of voltage mode control. Slope compensation is set to 136 mv/ µs. Slope compensation is completely disabled in DCM operation.

Feedback Pin

The FB pin is equipped with many pullup current sources and resistors. The pullup current sources and resistors work in conjunction with the opto−coupler to regulate the system. Many options are available to assist in stabilizing the system and to provide low standby current. Feedback resistor pullups and current sources once programmed by the OTP are not changed dynamically in operation but are fixed to the selected value.

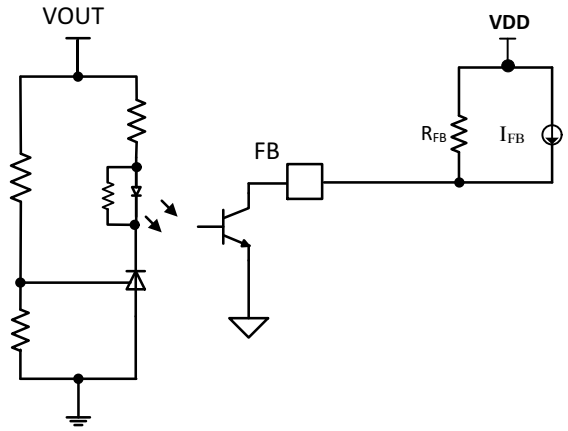


Figure 23. FB Resistor and Current Pullup Diagram

Low Side Driver

The low side driver is a ground based driver and is suitable for direct driving high capacitance switches due to the sourcing current I_{LS_src} (typically 1.3 A) resulting in a rise time of T_{LS_rise} (typically 9.9 ns) with a 1 nF load. No additional pull down circuitry is needed as the sinking current I_{LS_snk} (typically 2.5 A) results in a fall time of T_{LS_fall} (typically 3 ns) with a 1 nF load. The low side driver is also equipped with an internal clamp $V_{LDRV(low)}$ (typically 12 V) to_prevent the voltage on the gate from exceeding the maximum rating if the V_{CC} voltage of the controller increases beyond 20 V and to minimize losses in the system. The IC draws I_{CC3} (typically 4.7 mA) when the IC is switching both LDRV and ADRV drivers at 500 kHz with 100 pF load, but increases to I_{CC4} and I_{CC5} when fully loaded at 100 kHz and 500 kHz to 3.6 mA and 8.2 mA, respectively.

Active Clamp Driver

The Active Clamp Driver ADRV ground based driver is suitable for sending 5 V logic square wave signals to a high side driver with a built in level shifter to modulate the on time of the active clamp MOSFET. The drive with 150 mA of sourcing current and 200 mA of sinking current is also sufficient to drive a pulse transformer. Note that when the IC is in DCM Mode, the ADRV and the 5 V rail are disabled.

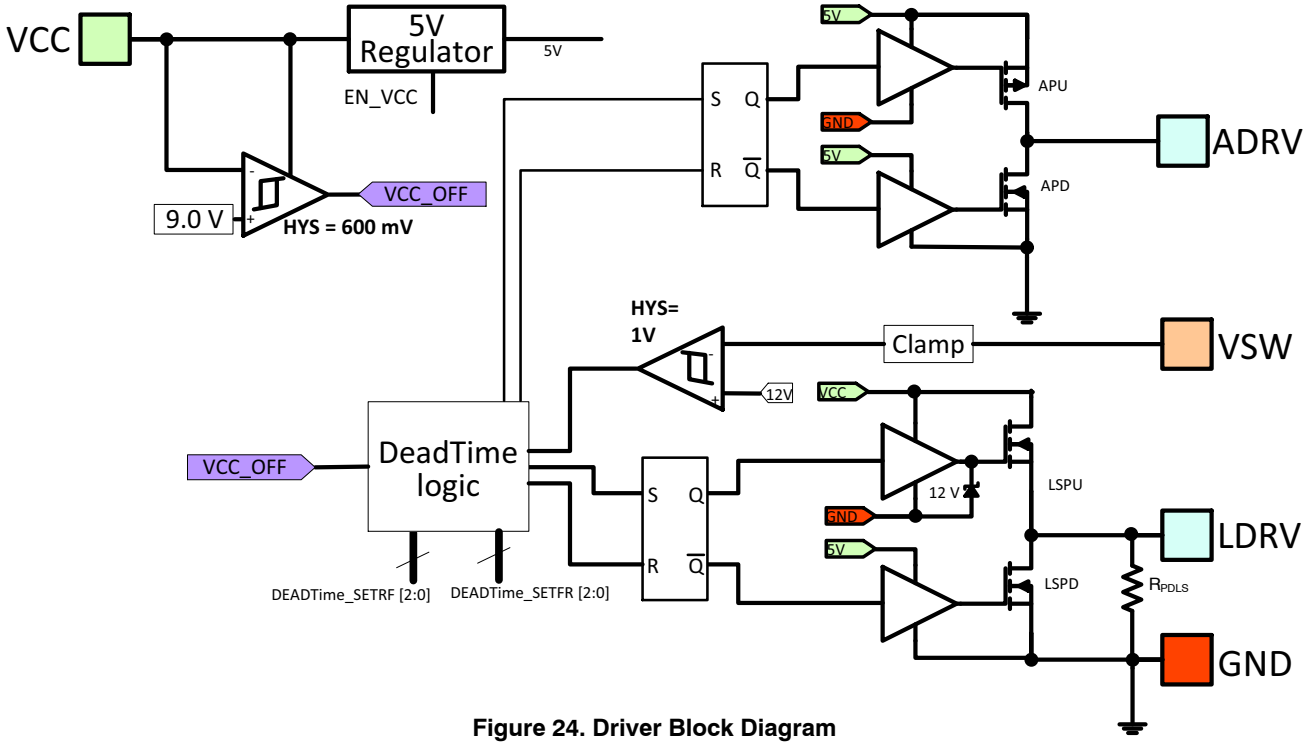


Figure 24. Driver Block Diagram

Adaptive Dead−Time

The NCP1568 implements an inbuilt adaptive dead−time that maximizes the efficiency of an active clamp flyback converter. The dead−time for the active clamp topology can be described by first identifying the two modes of operation of the switch node (SW) or bridge node. When the topology is actively clamping and the SW is high, current will be flowing into and out of the clamp capacitor. The time that the energy is stored and recycled in the clamp capacitor is referred to as the resonant mode and is identified with a high voltage on the switch node. During the resonant mode, the high side MOSFET or body diode is conducting. When the low side MOSFET is conducting, the SW is near ground potential, coincides with the positive slope of the primary inductor current, and is referred to as energy storage mode. The current is ramped up in the magnetizing inductance during the energy storage mode until the low side drive transitions from high to low. The switch node is then pulled high by the circulating currents. The rate at which the SW changes voltage is dependent on the voltage controlled

parasitic capacitance of the selected MOSFETs at the bridge node, the primary current, the magnetizing inductance, the leakage inductance, and other factors. Since many of the governing factors determining the rise and fall time of the switch node are design specific, an active dead−time control circuitry must be employed to optimize efficiency for a wide range of applications. During the energy storage to resonant mode transition, the majority of the transition time is spent charging the relatively large C_{OSS} capacitance of the low side MOSFET. The resulting slope of the voltage change at low voltages is in the order of 100 MV/s. Once the switch node has started to charge the C_{OSS}, the capacitance decreases rapidly and the slope can increase on the switch node to as much as 10 GV/s. The active dead−time control starts a timer once the LDRV internal logic has transitioned from TTL logic level high to low referred to as D_{T_Max}. The D_{T_Max} is a fail−safe dead timer that ensures normal operation. After the low side driver logic transition is tripped, the part will monitor the voltage at SW to determine when it has exceeded 12 V. Once the 12 V threshold is exceeded, a second timer is started called DT_E_R. Once the timer DT_E_R has expired, the ADRV will generate a 5 V logic level high and the high side driver will start signaling to turn on the high side MOSFET so that the high side MOSFET will start conducting. If the DT_MAX timer expires before the 12 V threshold is met and the additional DT_E_R timer has not expired, this failure will be counted, but the ADRV will not be forced on. Once the SW is high and the high side MOSFET is conducting, the high side drive will remain high until the end of the cycle. At the end of the cycle, the ADRV will be driven to the off state. When the internal pre−level shifted ADRV TTL logic transitions from high to low, a DT_MAX timer is started. The switch node then discharges until it reaches DT_R_E_TH, at which time the DT_R_E timer is started. Once either the DT_R_E or the DT_MAX timer has expired, the LDRV will transition from low to high and the process will continue. The dead time D_{T_Max} only applies to the full ACF Mode of operation and as such is blanked from ACF to DCM and DCM to ACF transitions when the ADRV pulses are phased in with LEM. Further, DT_MAX is not observed during soft start of ACF hold.

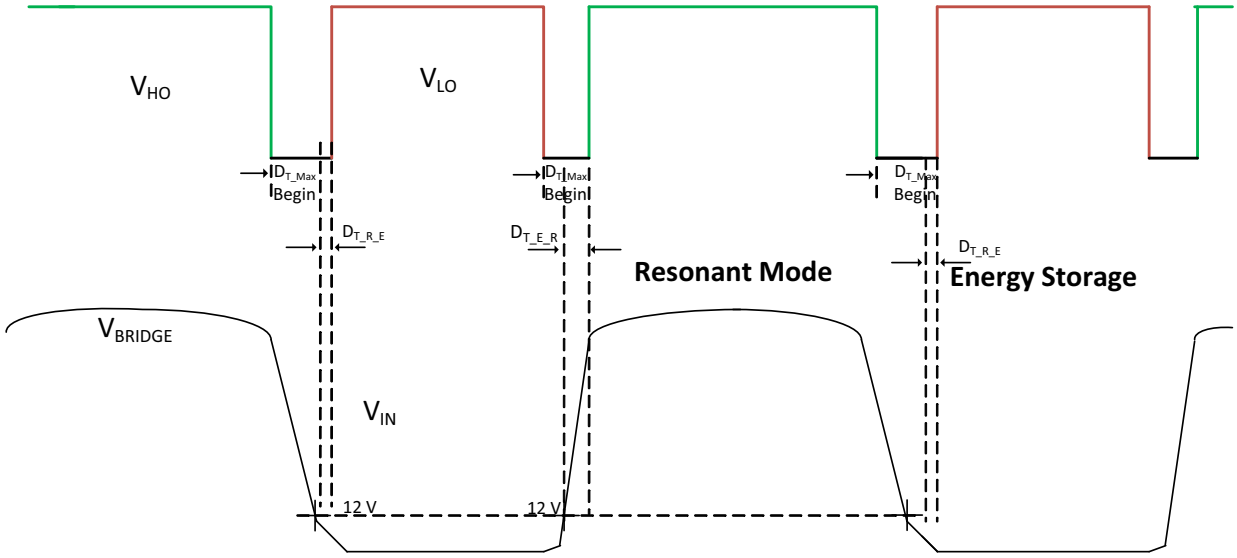


Figure 25. Dead−Time and Mode Identification

OTHER PROTECTION FEATURES

FLT Input

The NCP1568 includes a dedicated fault input accessible via the FLT pin. The controller can be latched off or restarted by pulling the pin up above the upper fault threshold (typically 3.0 V). Likewise, the controller can be latched off or or restarted if the FLT pin voltage, V_{FLT}, is pulled below the lower fault threshold (typically 0.4 V). The controller operates normally while the FLT pin voltage is maintained within the upper and lower fault thresholds. Figure 26 shows the architecture of the FLT input.

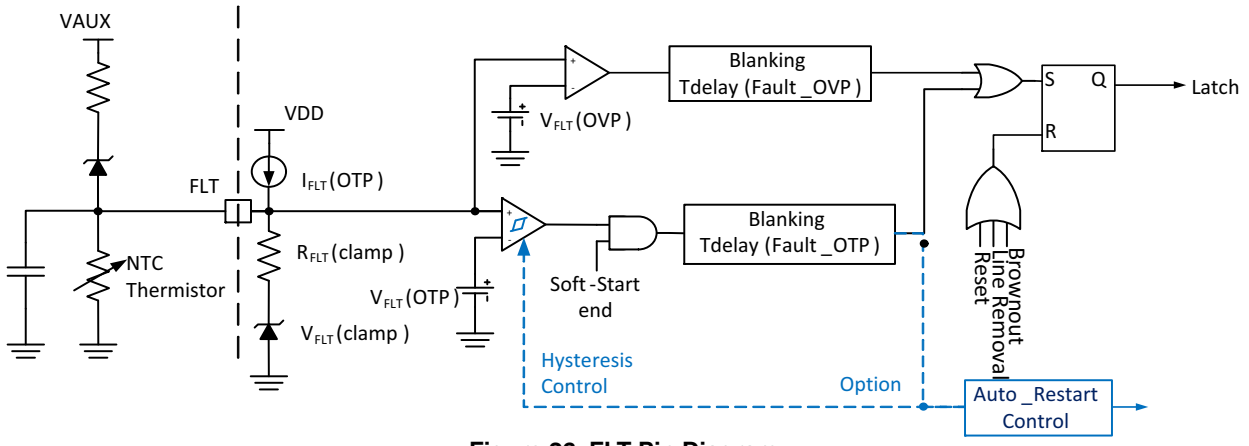


Figure 26. FLT Pin Diagram

OTP FLT Threshold and Fault Handling

The primary purpose of the lower FLT threshold is to detect an over−temperature fault using an NTC thermistor. A pull up current source, (typically 45.5 μA) generates a voltage drop across an external thermistor. The resistance of the NTC thermistor decreases as the temperature rises, resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below the $V_{FLT(OTP\_in)}$ threshold. The FLT voltage must drop below the threshold for longer than $t_{delay(OTP)}$ (typically 30 μs), then the IC will take the appropriate action. If the IC is programmed to latch, the V_{CC} voltage must go below Vcc(reset) before normal operation can continue. If the IC is programmed to restart, the part will initiate a soft start once the temperature decreases and the corresponding NTC voltage has increased enough to exceed the $V_{FLT(OTP\_out)}$ threshold (typically 900 mV).

OTP FLT Threshold Startup

A bypass capacitor is usually connected between the FLT and GND pins and it will take some time for VFLT to reach its steady state value once IFLT(OTP) is enabled. The IC is prevented from switching as long as the FLT voltage is below the VFLT(OTP_in) threshold. When adapters are produced they must go through a burn in process. The process calls for the adapter to be heated up to higher ambient temperatures (typically 65°C), then powered on and allowed to operate for an extended period of time to catch any assembly or part defects early before they are shipped to end customers. With the above burn in process, the FLT pin can cause the NTC to trip and keep the part off during the burn in process. To prevent the adapter from failing the burn in test, the adapter must start up when the FLT voltage exceeds VFLT(OTP_out) (typically 400 mV), rather than VFLT(OTP_in) (typically 920 mV). Further, the IC must successfully complete a soft start by reaching the end of forced ACF without triggering a VCC off. The state flow diagram pertaining to the FLT pin lower threshold voltage resets is shown in Figure 27.

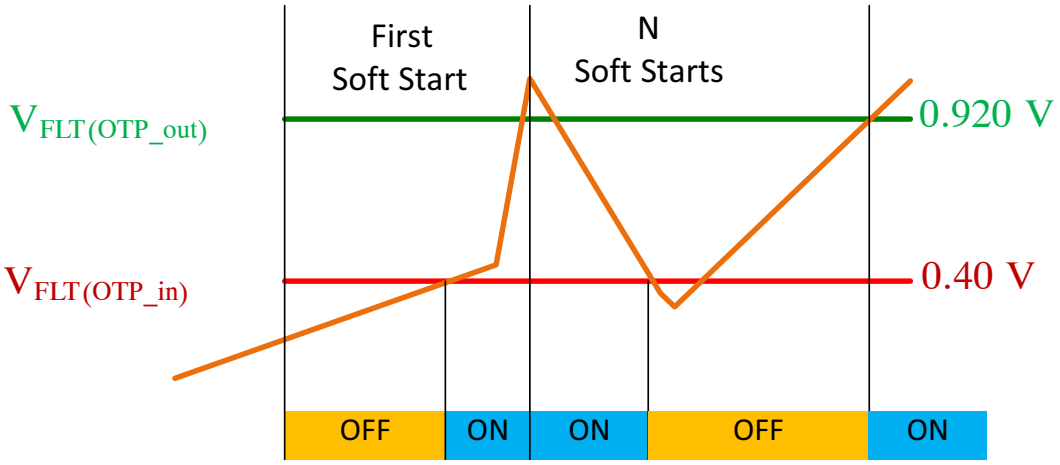


Figure 27. FLT Pin Diagram

The IC enables above $V_{FLT(OTP\_in)}$ in soft start only, rather than $V_{FLT(OTP\_out)}$. The rest of the functionality of the FLT pin after a successful soft start is unchanged. Therefore, a lower fault (i.e. over−temperature) is acknowledged under the $V_{FLT(OTP\_in)}$ threshold in soft start, holding the part in reset until the threshold is clear. When the FLT pin is below the $V_{FLT(OTP\_in)}$ threshold the current draw of the IC is I_{CC1A} (typically 190 μA).

OVP FLT Threshold

The upper fault threshold is intended to be used to prevent an overvoltage using a zener diode and a resistor in series from the auxiliary winding voltage (V_{AUX}) to ground with the FLT pin connected at the anode as shown in Figure 26. To reach the upper threshold, the external pull−up current has to be greater than the pull−down capability of the clamp $V_{FLT\ (clamp)}$ (typically 1.7 V) and $R_{FLT\ (clamp)}$ (typically 1.7 kΩ) the resistor in series. The FLT voltage must increase above the threshold for longer than $t_{delay(OTP)}$ (typically 30 μs), then IC will take the appropriate action of latching or restarting. If the IC is programmed to latch, the V_{CC} voltage must go below $V_{CC(reset)}$ before normal operation can continue. If the IC is programmed to restart, the part will initiate a soft start once the V_{AUX} voltage decreases below the hysteresis of OVP comparator. The clamp prevents the FLT pin voltage from reaching the upper latch threshold if the pin is open (typically 1.7 V). When the FLT pin is above the $V_{FLT(OVP)}$ threshold, the current draw of the IC is I_{CC1B} (typically 190 μA).

When the auto recovery option is selected for the fault pin, $I_{FLT(OTP)}$ remains enabled while the lower fault is present independent of V_{CC} in order to provide temperature hysteresis. The controller can detect an upper OVP fault once V_{CC} exceeds $V_{CC(reset)}$. Once the controller is latched, it is reset if a brown−out condition is detected or if V_{CC} is cycled down to its reset level, $V_{CC(reset)}$. In the typical application these conditions occur only if the ac voltage is removed from the system.

Over Power Protection

The maximum power delivered by an isolated power converter is controlled by limiting the peak inductor on a pulse by pulse basin on the primary side. Power converters typically do not deliver the same maximum output power across all line conditions. Energy delivery is influenced by duty ratio, line voltage, and switching frequency. The duty ratio changes with line voltage and hence with a fixed peak current the average inductor current varies over line voltage. The slope of the current increases as the line voltage increases, delivering more energy with a fixed propagation delay in high line operation. An internal line OPP compensation is provided where line sensed discrete steps provide a transconductance (g_m)of 174 nA/V sourced out of the CS pin such that users and compensate for selected inductance. The propagation delays of all comparators connected to the CS pin such as SCP, OCP, Peak Current Freeze, and the PWM comparator all benefit from the line compensation.

Current Limit

The current passing through the primary main FET is sensed via a resistor at the CS pin. The ramping current sensed by the CS pin is used to modulate the loop error voltage (FB) to generate PWM signals; it is also used for cycle by cycle peak current limit control and detection of a short circuit condition. Figure 28 below shows the block diagram of the current limit circuitry.

Internal leading edge blanking (LEB) circuitry masks the current sense information before applying it to the current monitoring comparators. LEB prevents unwanted noise from terminating the drive pulses prematurely. It is recommended to place a small RC filter close to the CS pin to suppress additional noise. The LEB period begins once LDRV reaches approximately 2 V. An internal switch $R_{CS(switch)}$ discharges and holds the CS pin low at the conclusion of every cycle for 100 ns In DCM operation, LEB is implemented by pulling the CS pin low for the LEB period at the beginning of LDRV pulse.

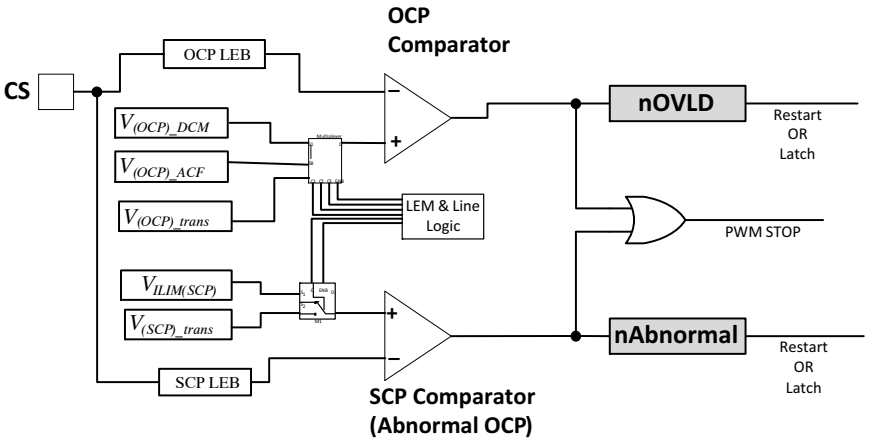


Figure 28. Current Limit Comparators

Cycle−by−Cycle Current Limiting

Cycle−by−cycle (CBC) current limiting is implemented using the OCP comparator and terminates the drive pulse if the CS voltage exceeds the $V_{ILIM\ (OCP)}$ threshold in ACF, DCM, and skip mode of operation. In transition mode of operation this threshold is raised to $V_{ILIM\ (OCP)\ Trans}$ to facilitate the increased ΔIm while transitioning into or out of ACF operation. When the CS voltage crosses the $V_{ILIM\ (OCP)}$, an error flag is asserted and the counter counts up 2 counts. If a single cycle occurs in which the $V_{ILIM\ (OCP)}$ is not triggered, the counter counts down 1 count. The counter update is done at switching frequency. Hence depending upon the mode of operation (ACF vs DCM), line & load conditions, the time it takes to reach full count varies. If the counter has reached full count, a latch or auto−recover is enabled dependent on options selected referred to at OCP reaction.

The OCP threshold depends on mode of operation i.e. DCM vs ACF & line voltage. In the DCM operation the OCP threshold is 800 mV. However, in ACF mode of operation depending on the line voltage the threshold varies. This feature is implemented to compensate for higher frequency of operation at higher line voltage. Please refer to the electrical table for line voltage vs OCP level numbers.

Table 7. CURRENT LIMIT COUNTS AND TIMING

Switching Frequency (kHz)	Counts (k)	Limiting Time (ms)	Switching Frequency (kHz)	Counts (k)	Limiting Time (ms)
100	5	25	100	20	100
250	5	10	250	20	40
500	5	5	500	20	20
1000	5	2.5	1000	20	10

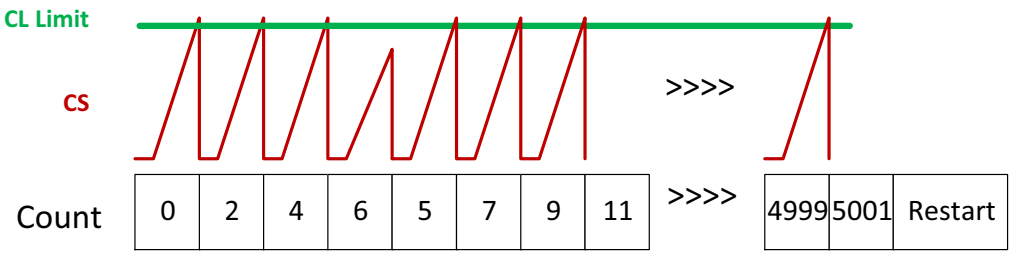


Figure 29. Current Limit Counting Scheme

Short Circuit Protection

Short circuit protection is implemented using the SCP comparator; it terminates the drive pulse if the CS voltage exceeds the VILIM (SCP) threshold in ACF, DCM, and skip mode of operation after $T_{LEB(SCP)}$. The time $T_{LEB(SCP)}$ is shorter than the $T_{LEB(OCP)}$ by approximately 50 ns. A sharp rise in current can occur in the primary if a winding is shorted or a component is faulty. When the SCP comparator trips, a count is incremented and a counter tracks the number of SCP events. Once the number of consecutive SCP events crosses N_{SCP} as defined in the electrical table, then the part latches off or restarts according to the OTP bits programmed referred to a SCP reaction.

OCP and SCP Level During Transition

The OCP and SCP have two discrete levels at a given input AC voltage. The first level for the current limit is based on the peak AC input line voltage. The NCP1568 ZVS frequency modulation scheme increases the frequency as the line voltage increases, the current limit must be decreased to compensate for the increased available output power when the voltage and frequency increase. The SCP and OCP levels described in the above section are steady state normal protections. When the system is transitioning from ACF operation to DCM operation or DCM operation to ACF operation via the LEM process described in the corresponding sections, the current limits are changed. When the system is undergoing the transition, the OCP and SCP levels are increased from the $V_{(OCP)\_ACF\_90}$ (800 mV at low line) to the $V_{ILIM(OCP)\_Trans}$ 1.2 V and the $V_{ILIM(SCP)}$ 1.2 V to $V_{ILIM(SCP)\_Trans}$ 1.4 V. The current limit levels are increased on the rising edge of the first low side drive pulse of the LEM transition and remain at that level for 1 ms after the LEM process has completed as shown in Figure 30.

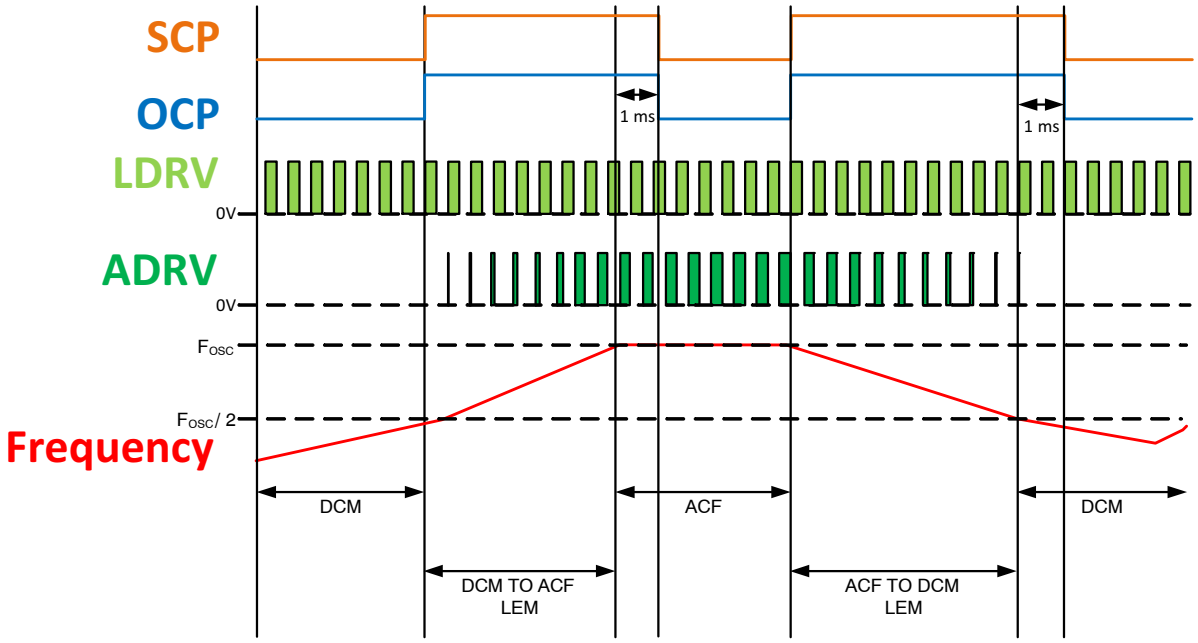


Figure 30. OCP and SCP Timing

Dynamic Self Supply (DSS)

When the IC is not switching and either waiting for restart or latched, power is maintained to the part by sourcing I_{start2} until the V_{CC} pin is charged to the $V_{CC(on)}$ threshold. The part will continue to use power, discharging the V_{CC} pin voltage until the $V_{CC(off)}$ threshold is tripped, at which time the part will source I_{start2}. The charging and discharging of the V_{CC} voltage, also referred to as dynamic self−supply (DSS) will continue until input voltage is removed and reapplied to the power supply or until restart is initiated.

Auto Recovery and Latch

The auto recovery fault behavior is used to protect the end user from any abnormal conditions, to reduce power consumption during a fault condition, and to allow the adapter to recover quickly as soon as the issue has been resolved. If a fault occurs when the IC is configured to auto−recovery, ADRV and LDRV are driven low and the part remains off for T_{auto_off} time. At the end of T_{auto_off}, the IC is restarted once $V_{CC(on)}$ is reached and allowed to soft start.

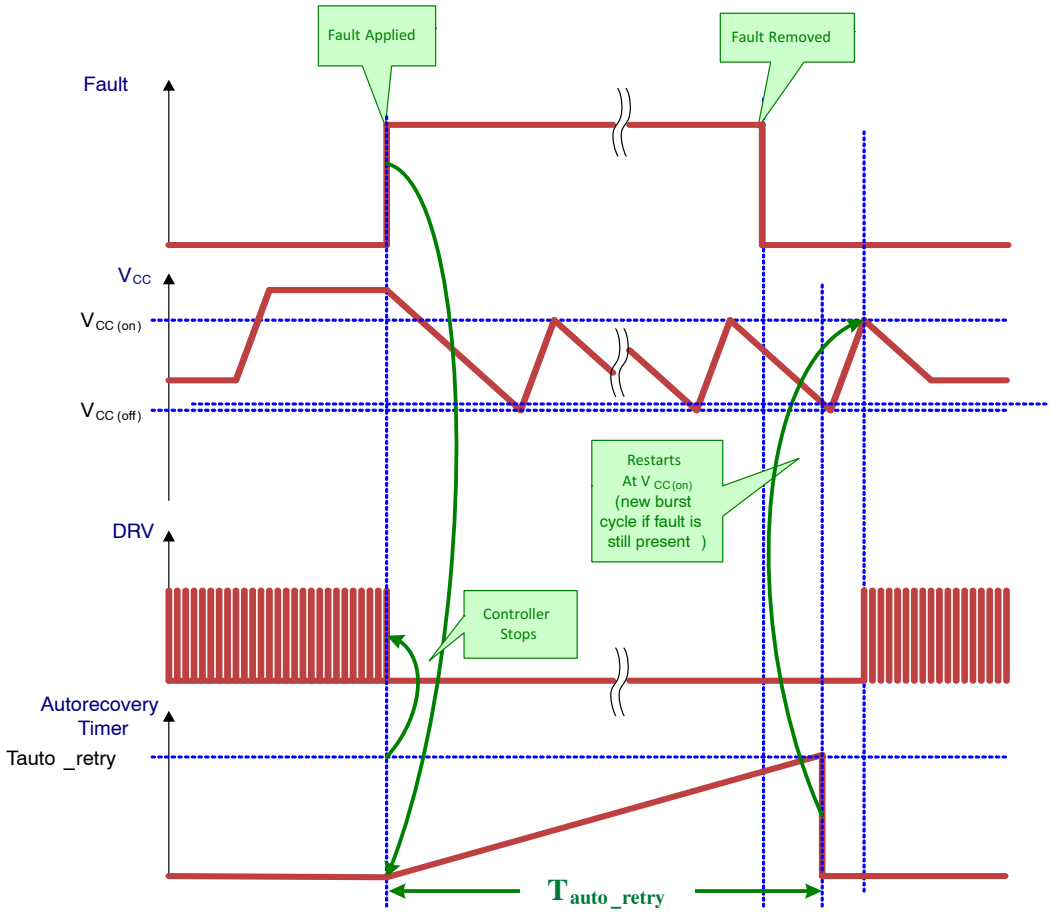


Figure 31. Fault Recovery Behavior

Latching Fault Behavior

The purpose of a latch fault is to require user intervention to restore proper operation of the adapter or power supply. The user is expected to unplug and replug the adapter to enable the power supply to attempt regulation. If a fault occurs and the NCP1568 is configured to have a latch fault in ACF operation, DCM operation, or skip operation once the current clock cycle expires, both LDRV and ADRV are terminated. In skip operation since there are no pulses, no pulses will be produced as a result of a latch fault. The part then monitors the line to determine when power has been removed and maintains V_{CC} voltage by DSS. When line voltage has been removed, the part will start X2 discharge (see the line removal section). When the FLT pin initiates a latch fault, the current draw of the IC is I_{CC1C} (typically 153 μA).

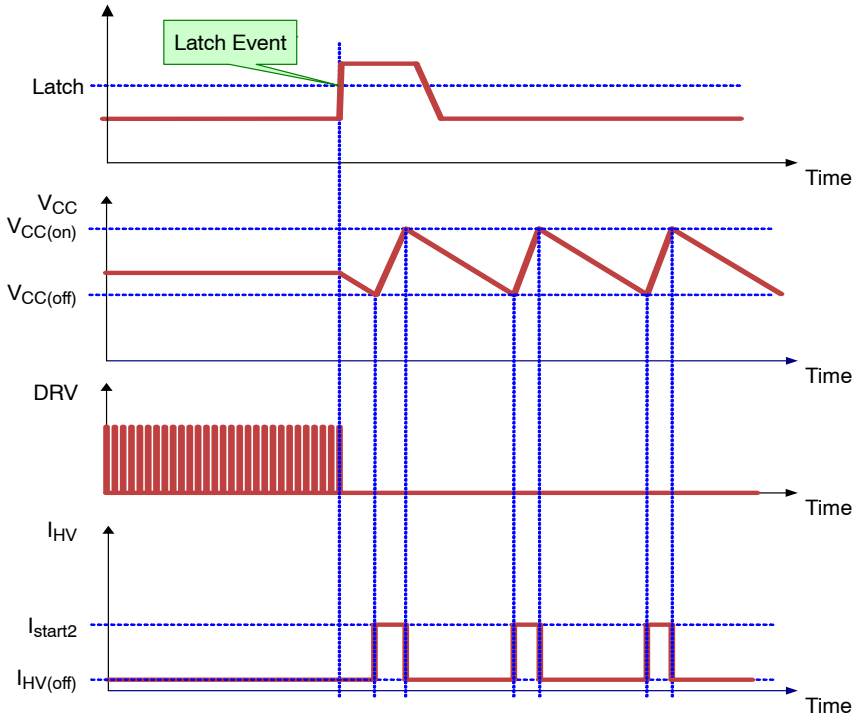
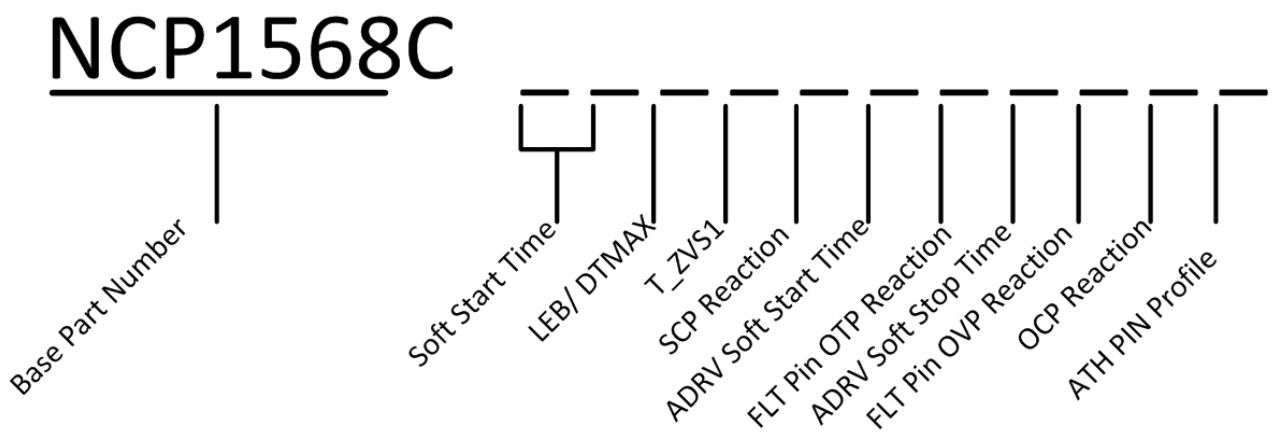


Figure 32. Fault Latched Behavior

Thermal Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the controller. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN} (typically 150°C). When a thermal shutdown fault is detected, the controller enters a non−latching fault mode and remains there until the junction temperature drops below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, (typically 40°C). The thermal shutdown is also cleared if V_{CC} drops below $V_{CC(reset)}$, or a line removal fault is detected. A new power up sequence commences at the next $V_{CC(on)}$.

Part Number Ordering Information



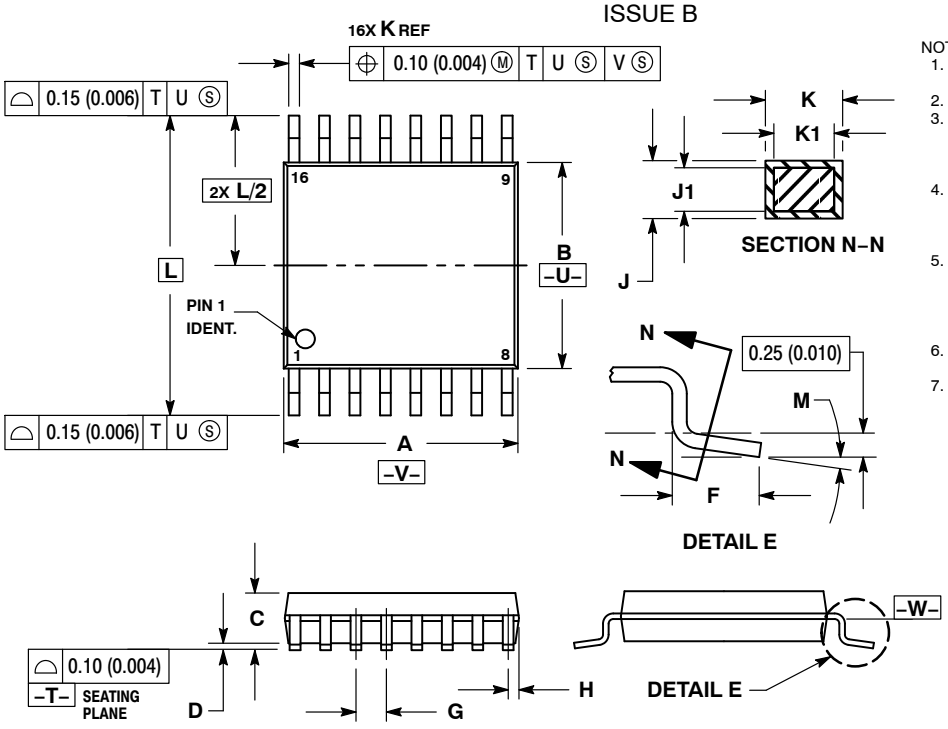
Base Part Number	Soft Start Time	LEB/ DTMAX T_ZVS1	T_ZVS2	SCP Reaction	ADRV Soft−Start	FLT Pin OTP Reaction	ADRV Soft−Stop	FLT Pin OVP Reaction	OCP Reaction	ATH PIN Profile
NCP1568C	4	0	0	L	0	L	0	L	L	0
	8	1	1	A	1	A	1	A	A	1
	16	2	2		2		2			2
	32	3	3		3		3			
		4	4							
		5	5							
		6	6							
		7	7							

EXAMPLE

Part Number	Description	Comment
NCP1568C806AAAAC0	Auto Frequency adjustment Soft Start Time 8 ms LEB= 178 ns T_ZVS1+ TZVS2 = 360 ns SCP, FLT OTP, FLT OVP, OCP reaction = auto Recovery Ath pin Profile optimized for low range 1.12 V to 2.2 V	Good to For USB PD
NCP1568C806AAAAC2	Auto Frequency adjustment Soft Start Time 8 ms LEB= 178 ns T_ZVS1+ TZVS2 = 360 ns SCP, FLT OTP, FLT OVP, OCP reaction = auto Recovery IDTH current profile optimized for Oscillator Option C Ath pin Profile optimized for low range 1.8 V to 2.9 V	Good to For High output voltage fixed voltage

PACKAGE DIMENSIONS

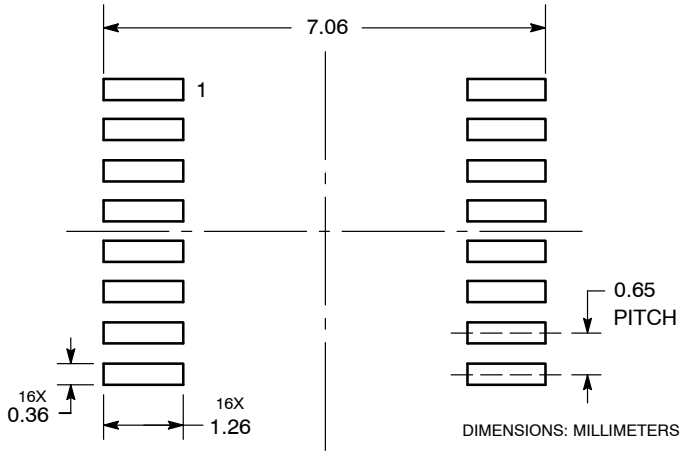
TSSOP−16
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative