LS2088A

QorIQ LS2088A/LS2048A Data Sheet

Features

- 64-bit Arm® Cortex®-A72 CPUs
  - LS2088A has eight A72 cores arranged as four clusters. Each cluster has two cores sharing a 1 MB L2 cache
  - LS2048A has four A72 cores arranged as two clusters. Each cluster has two cores sharing a 1 MB L2 cache
  - Up to 2.1 GHz
- 1 MB platform cache with ECC protection
- Hierarchical interconnect fabric
- Two 64-bit DDR4 SDRAM memory controllers with ECC and interleaving support
  - Up to 2.1 GT/s
- One secondary 32-bit DDR4 SDRAM memory controller, intended for use by the AIOP
  - Up to 1.6 GT/s
- DPAA2 (Datapath acceleration architecture, second generation) incorporating acceleration for the following functions:
  - Wire-rate IO Processor(WRIOP) for packet parsing, classification, and distribution
  - Queue management for scheduling, packet sequencing, and congestion management; Hardware buffer management for buffer allocation and de-allocation (QBMan)
  - Cryptography acceleration (SEC 5.2) at up to 20 Gbps
  - RegEx pattern matching acceleration (PME 2.0) at up to 10 Gbps
  - Decompression/compression acceleration (DCE 1.0) at up to 20 Gbps
  - Accelerated I/O processing (AIOP) at up to 20 Gbps
- qDMA engine
- 16 SerDes lanes at up to 10.3125 GHz
- Ethernet interfaces
  - Up to eight 10 Gbps Ethernet MACs
  - Up to sixteen 1 / 2.5 Gbps Ethernet MACs
- High-speed peripheral interfaces
  - Four PCIe 3.0 controllers. PCIe3 is capable of x8/x4/x2/x1 and SR-IOV and the other three (PCIe1, PCIe2 and PCIe4) are capable of x4/x2/x1 and do not support SR-IOV.
  - At platform speeds of 533 MHz or higher, there is no limitation to PCIe speed/width
  - At platform speed less than 533 MHz, all four PCIe controllers can run GEN1 and GEN2 speed at full width. For GEN3 speed, PCIe1/PCIe2/PCIe4 can only run x2 width, PCIe3 can only run x4 width.
- Additional peripheral interfaces
  - Two serial ATA (SATA 3.0) controllers
  - Two high-speed USB 3.0 controllers with integrated PHY
  - Enhanced secure digital host controller
  - Serial peripheral interface (SPI) controller
  - Quad Serial peripheral interface (QSPI) controller
  - Four I2C controllers
  - Two DUARTs
  - Integrated flash controller (IFC 2.0) supporting NAND and NOR flash
- Support for hardware virtualization and partitioning enforcement
- Implements trust architecture combined with TrustZone®
  - Service processor (SP) provides pre-boot initialization and secure-boot capabilities

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

Table of Contents

1 Overview 3
2 Pin assignments 3
2.1 1292 ball layout diagrams 3
2.2 Pinout list 10
3 Electrical characteristics 57
3.1 Overall DC electrical characteristics 57
3.2 Power sequencing 62
3.3 Power-down requirements 64
3.4 Power characteristics 64
3.5 Power-on ramp rate 67
3.6 Input clocks 67
3.7 RESET initialization 73
3.8 DDR4 SDRAM controller 73
3.9 SPI interface 79
3.10 QuadSPI interface 84
3.11 DUART interface 88
3.12 Ethernet management interface 1 and 2, IEEE Std 1588 89
3.13 USB 2.0 interface 92
3.14 USB 3.0 interface 93
3.15 Integrated flash controller 95
3.16 Enhanced secure digital host controller (eSDHC) 112
3.17 Generic interrupt controller (GIC) 116
3.18 JTAG controller 117
3.19 I2C interface 120
3.20 GPIO interface 122
3.21 Battery-backed security monitor interface 123
3.22 High-speed serial interfaces (HSSI) 124
4 Hardware design considerations 167
4.1 Clock ranges 167
4.2 Power supply design 168
5 Thermal 169
5.1 Temperature diode 170
6 Package information 170
6.1 Package parameters for the FC-PBGA 170
6.2 Mechanical dimensions of the FC-PBGA 171
7 Security fuse processor 173
8 Ordering information 173
8.1 Part numbering nomenclature 173
8.2 Part marking 174
9 Revision history 175

1 Overview

The LS2088A and LS2048A have eight and four, respectively, Arm® Cortex®-A72 cores built on Armv8-A architecture with high-performance data path acceleration and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and military/aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, gateways, and general-purpose embedded computing systems. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also simplifying the board design.

This figure shows the block diagram of the chip.

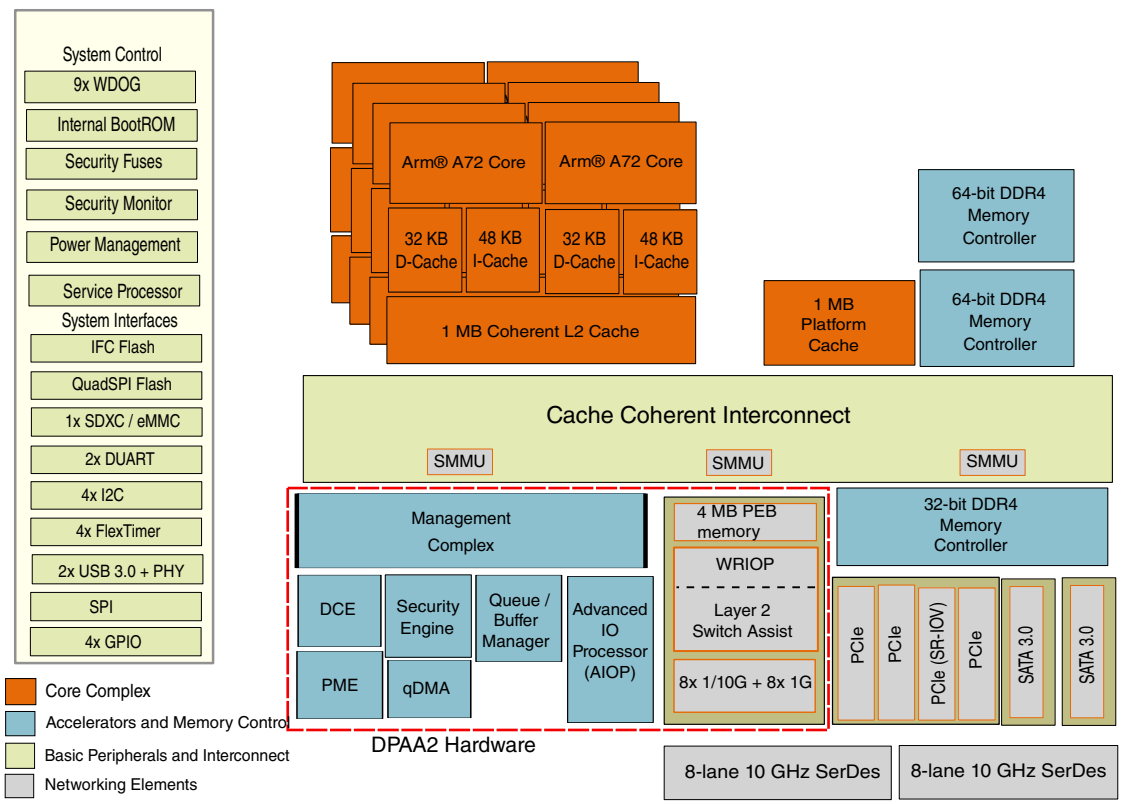

Figure 1. LS2088A block diagram

2 Pin assignments

2.1 1292 ball layout diagrams

The figure below shows the complete view of the ball map diagram. Figure 3, Figure 4, Figure 5, and Figure 6 show quadrant views.

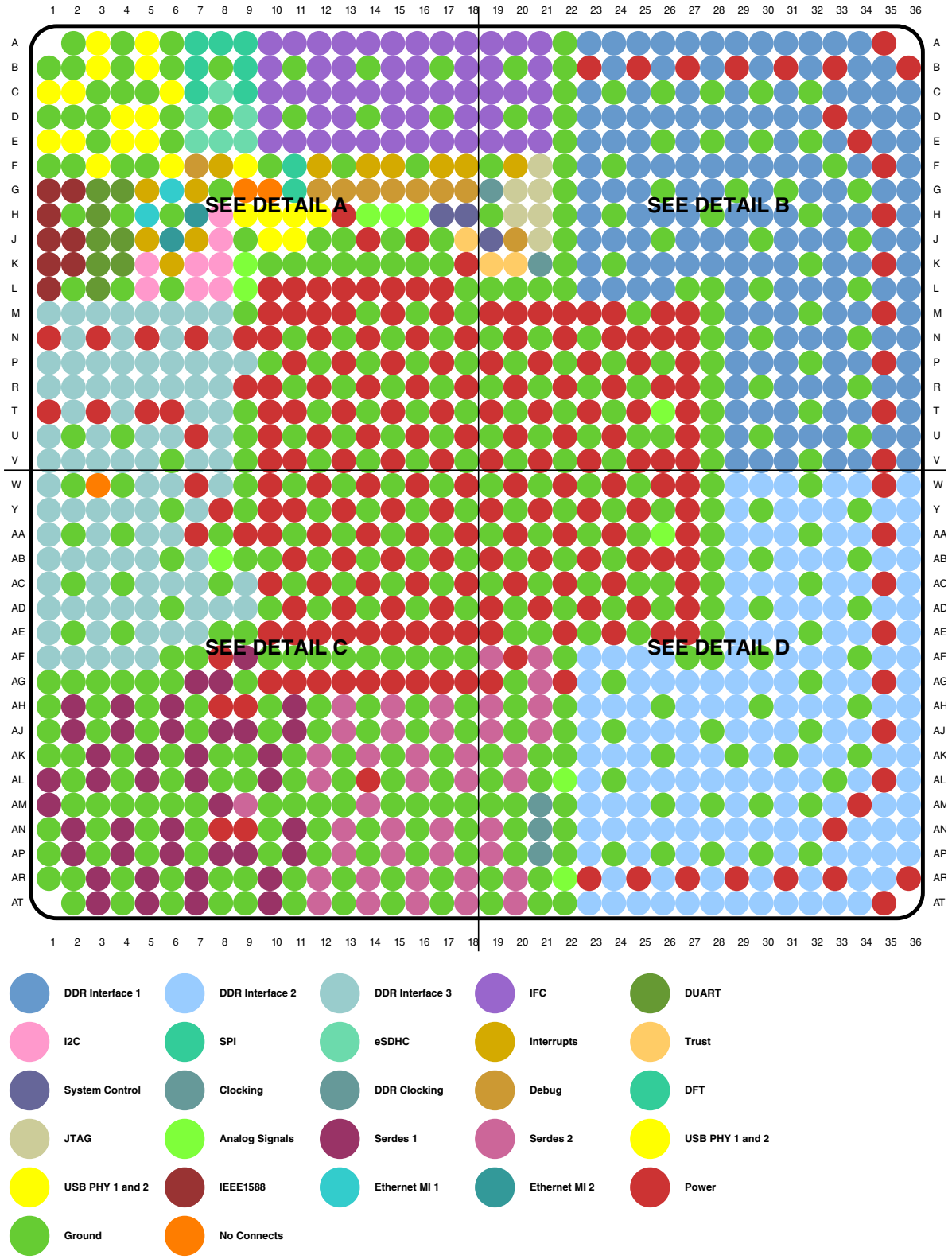

Figure 2. Complete BGA Map for the

QorIQ LS2088A/LS2048A Data Sheet, Rev. 3, 09/2020

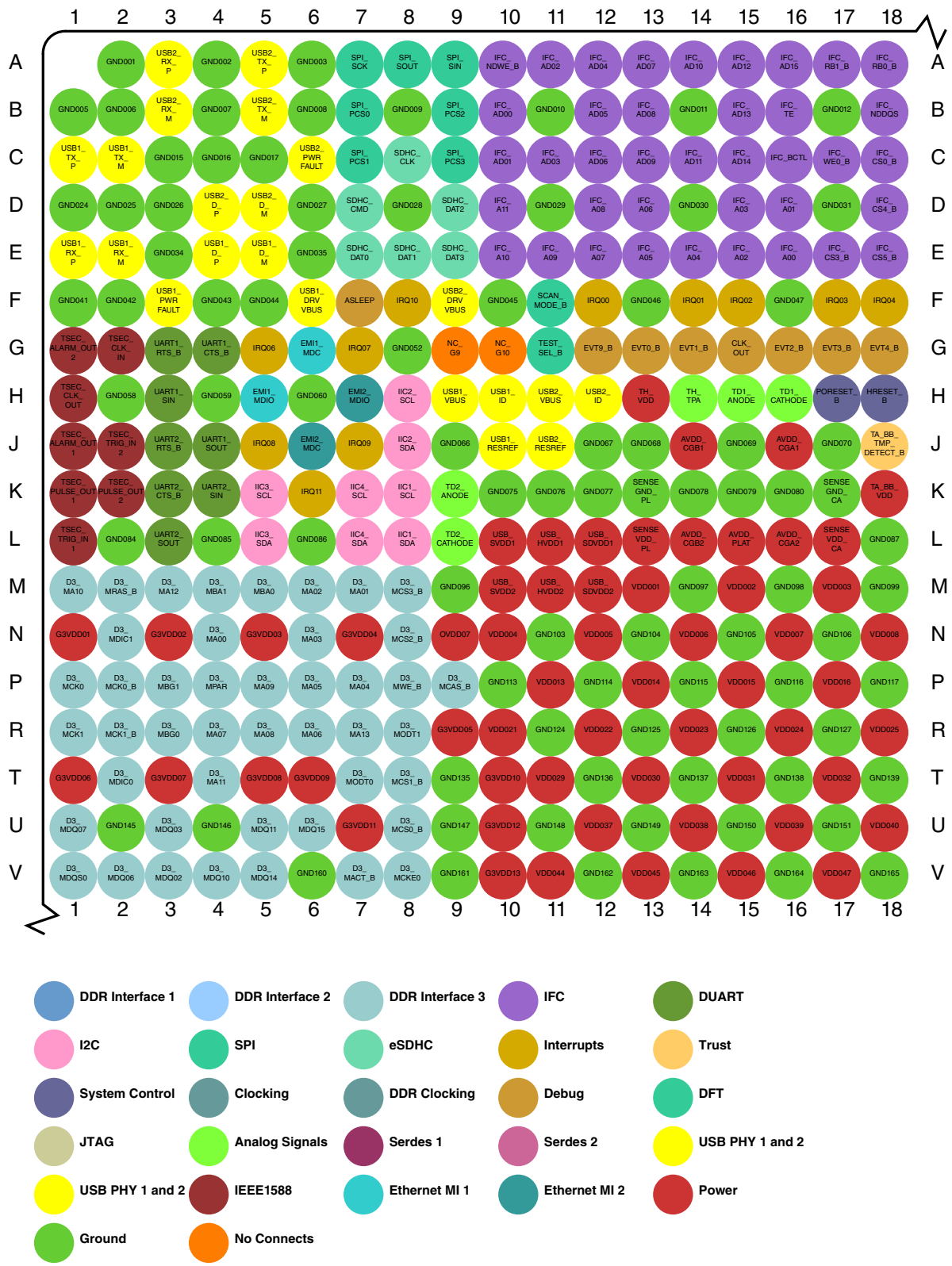

Figure 3. Detail A

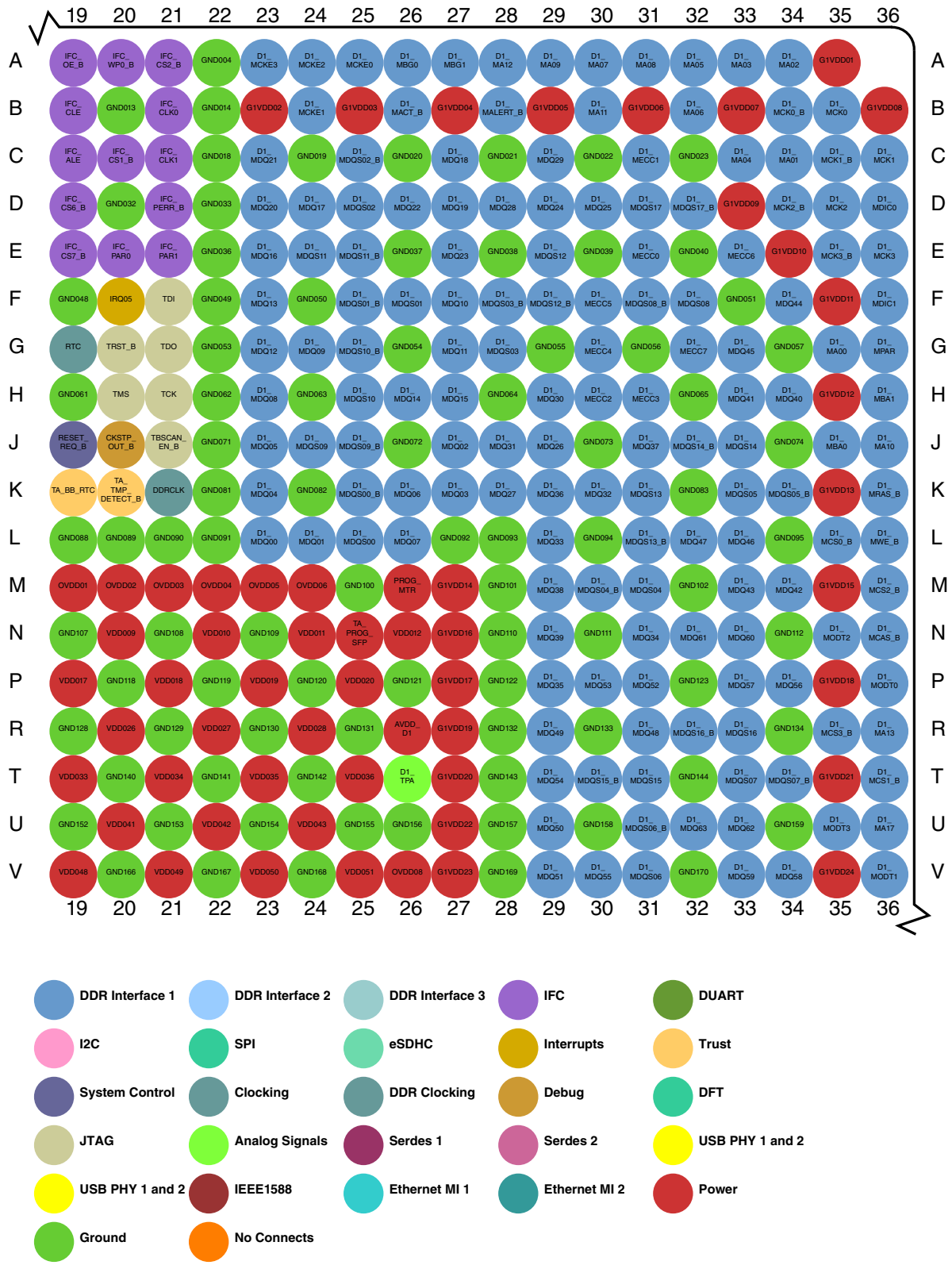

Figure 4. Detail B

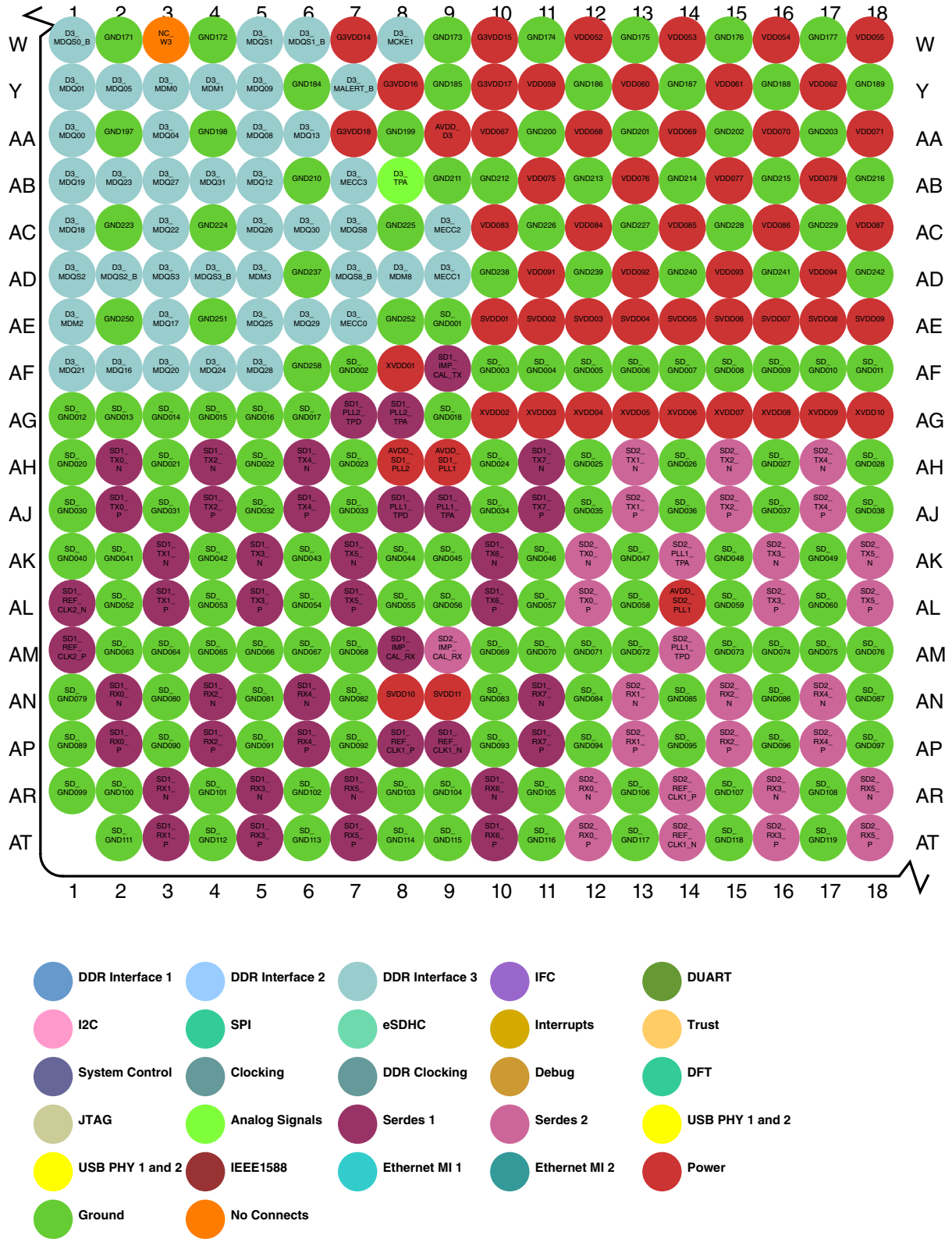

Figure 5. Detail C

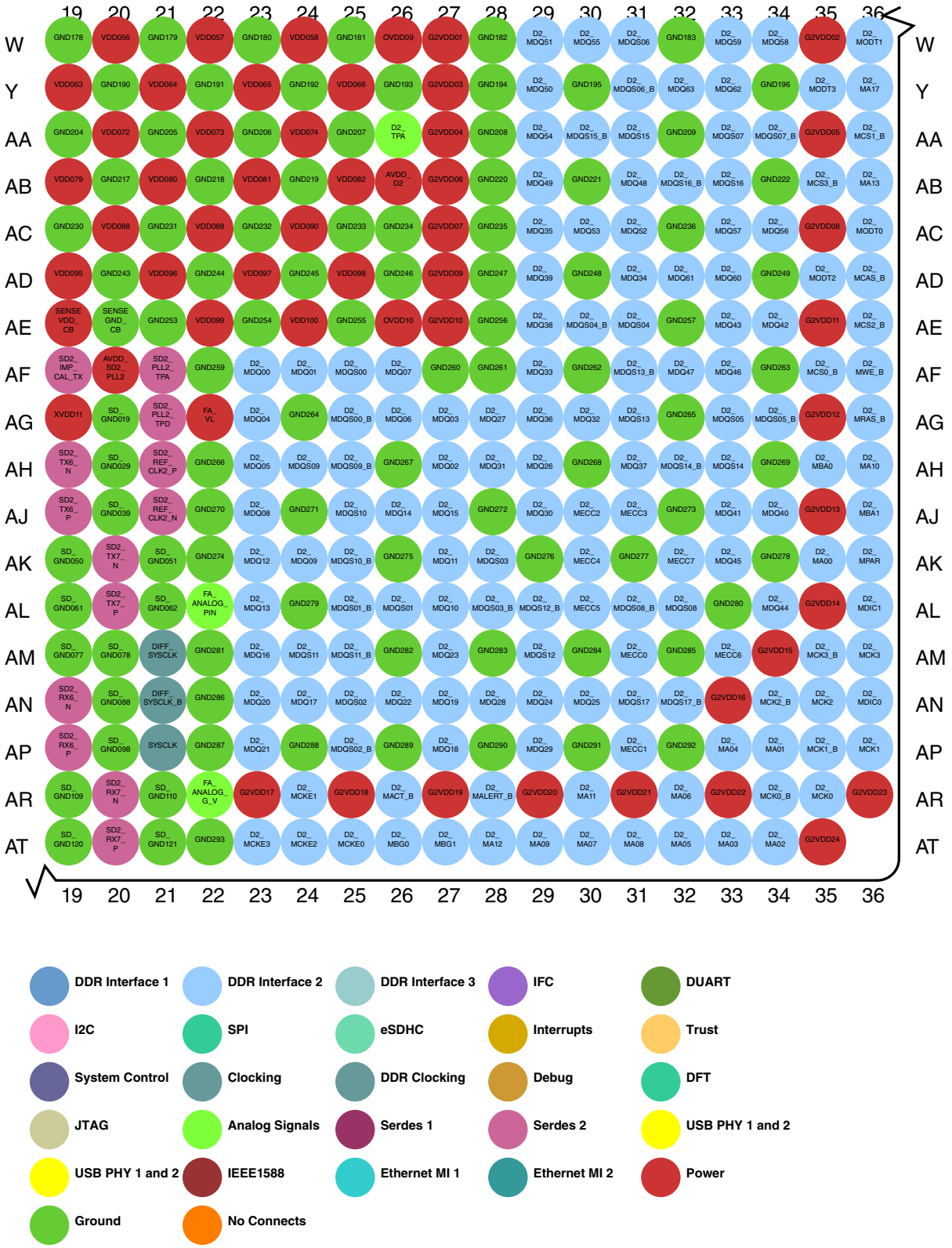

Figure 6. Detail D

2.2 Pinout list

This table provides the pinout listing for the LS2088A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	G35	O	$G1V_{DD}$	---
D1_MA01	Address	C34	O	$G1V_{DD}$	---
D1_MA02	Address	A34	O	$G1V_{DD}$	---
D1_MA03	Address	A33	O	$G1V_{DD}$	---
D1_MA04	Address	C33	O	$G1V_{DD}$	---
D1_MA05	Address	A32	O	$G1V_{DD}$	---
D1_MA06	Address	B32	O	$G1V_{DD}$	---
D1_MA07	Address	A30	O	$G1V_{DD}$	---
D1_MA08	Address	A31	O	$G1V_{DD}$	---
D1_MA09	Address	A29	O	$G1V_{DD}$	---
D1_MA10	Address	J36	O	$G1V_{DD}$	---
D1_MA11	Address	B30	O	$G1V_{DD}$	---
D1_MA12	Address	A28	O	$G1V_{DD}$	---
D1_MA13	Address	R36	O	$G1V_{DD}$	---
D1_MA17	Address	U36	O	$G1V_{DD}$	---
D1_MACT_B	Activate	B26	O	$G1V_{DD}$	---
D1_MALERT_B	Alert	B28	I	$G1V_{DD}$	1, 29
D1_MBA0	Bank Select	J35	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	H36	O	$G1V_{DD}$	---
D1_MBG0	Bank Group	A26	O	$G1V_{DD}$	---
D1_MBG1	Bank Group	A27	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe / MA[15]	N36	O	$G1V_{DD}$	---
D1_MCK0	Clock	B35	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	B34	O	$G1V_{DD}$	---
D1_MCK1	Clock	C36	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	C35	O	$G1V_{DD}$	---
D1_MCK2	Clock	D35	O	$G1V_{DD}$	---
D1_MCK2_B	Clock Complement	D34	O	$G1V_{DD}$	---
D1_MCK3	Clock	E36	O	$G1V_{DD}$	---
D1_MCK3_B	Clock Complement	E35	O	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCKE0	Clock Enable	A25	O	$G1V_{DD}$	2
D1_MCKE1	Clock Enable	B24	O	$G1V_{DD}$	2
D1_MCKE2	Clock Enable	A24	O	$G1V_{DD}$	2
D1_MCKE3	Clock Enable	A23	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	L35	O	$G1V_{DD}$	---
D1_MCS1_B	Chip Select	T36	O	$G1V_{DD}$	---
D1_MCS2_B	Chip Select / MCID[0]	M36	O	$G1V_{DD}$	---
D1_MCS3_B	Chip Select / MCID[1]	R35	O	$G1V_{DD}$	---
D1_MDIC0	Driver Impedance Calibration	D36	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedance Calibration	F36	IO	$G1V_{DD}$	3
D1_MDM0/**D1_MDQS09**	Data Mask	J24	O	$G1V_{DD}$	1
D1_MDM1/**D1_MDQS10**	Data Mask	H25	O	$G1V_{DD}$	1
D1_MDM2/**D1_MDQS11**	Data Mask	E24	O	$G1V_{DD}$	1
D1_MDM3/**D1_MDQS12**	Data Mask	E29	O	$G1V_{DD}$	1
D1_MDM4/**D1_MDQS13**	Data Mask	K31	O	$G1V_{DD}$	1
D1_MDM5/**D1_MDQS14**	Data Mask	J33	O	$G1V_{DD}$	1
D1_MDM6/**D1_MDQS15**	Data Mask	T31	O	$G1V_{DD}$	1
D1_MDM7/**D1_MDQS16**	Data Mask	R33	O	$G1V_{DD}$	1
D1_MDM8/**D1_MDQS17**	Data Mask	D31	O	$G1V_{DD}$	1
D1_MDQ00	Data	L23	IO	$G1V_{DD}$	---
D1_MDQ01	Data	L24	IO	$G1V_{DD}$	---
D1_MDQ02	Data	J27	IO	$G1V_{DD}$	---
D1_MDQ03	Data	K27	IO	$G1V_{DD}$	---
D1_MDQ04	Data	K23	IO	$G1V_{DD}$	---
D1_MDQ05	Data	J23	IO	$G1V_{DD}$	---
D1_MDQ06	Data	K26	IO	$G1V_{DD}$	---
D1_MDQ07	Data	L26	IO	$G1V_{DD}$	---
D1_MDQ08	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ09	Data	G24	IO	$G1V_{DD}$	---
D1_MDQ10	Data	F27	IO	$G1V_{DD}$	---
D1_MDQ11	Data	G27	IO	$G1V_{DD}$	---
D1_MDQ12	Data	G23	IO	$G1V_{DD}$	---
D1_MDQ13	Data	F23	IO	$G1V_{DD}$	---
D1_MDQ14	Data	H26	IO	$G1V_{DD}$	---
D1_MDQ15	Data	H27	IO	$G1V_{DD}$	---
D1_MDQ16	Data	E23	IO	$G1V_{DD}$	---
D1_MDQ17	Data	D24	IO	$G1V_{DD}$	---
D1_MDQ18	Data	C27	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ19	Data	D27	IO	$G1V_{DD}$	---
D1_MDQ20	Data	D23	IO	$G1V_{DD}$	---
D1_MDQ21	Data	C23	IO	$G1V_{DD}$	---
D1_MDQ22	Data	D26	IO	$G1V_{DD}$	---
D1_MDQ23	Data	E27	IO	$G1V_{DD}$	---
D1_MDQ24	Data	D29	IO	$G1V_{DD}$	---
D1_MDQ25	Data	D30	IO	$G1V_{DD}$	---
D1_MDQ26	Data	J29	IO	$G1V_{DD}$	---
D1_MDQ27	Data	K28	IO	$G1V_{DD}$	---
D1_MDQ28	Data	D28	IO	$G1V_{DD}$	---
D1_MDQ29	Data	C29	IO	$G1V_{DD}$	---
D1_MDQ30	Data	H29	IO	$G1V_{DD}$	---
D1_MDQ31	Data	J28	IO	$G1V_{DD}$	---
D1_MDQ32	Data	K30	IO	$G1V_{DD}$	---
D1_MDQ33	Data	L29	IO	$G1V_{DD}$	---
D1_MDQ34	Data	N31	IO	$G1V_{DD}$	---
D1_MDQ35	Data	P29	IO	$G1V_{DD}$	---
D1_MDQ36	Data	K29	IO	$G1V_{DD}$	---
D1_MDQ37	Data	J31	IO	$G1V_{DD}$	---
D1_MDQ38	Data	M29	IO	$G1V_{DD}$	---
D1_MDQ39	Data	N29	IO	$G1V_{DD}$	---
D1_MDQ40	Data	H34	IO	$G1V_{DD}$	---
D1_MDQ41	Data	H33	IO	$G1V_{DD}$	---
D1_MDQ42	Data	M34	IO	$G1V_{DD}$	---
D1_MDQ43	Data	M33	IO	$G1V_{DD}$	---
D1_MDQ44	Data	F34	IO	$G1V_{DD}$	---
D1_MDQ45	Data	G33	IO	$G1V_{DD}$	---
D1_MDQ46	Data	L33	IO	$G1V_{DD}$	---
D1_MDQ47	Data	L32	IO	$G1V_{DD}$	---
D1_MDQ48	Data	R31	IO	$G1V_{DD}$	---
D1_MDQ49	Data	R29	IO	$G1V_{DD}$	---
D1_MDQ50	Data	U29	IO	$G1V_{DD}$	---
D1_MDQ51	Data	V29	IO	$G1V_{DD}$	---
D1_MDQ52	Data	P31	IO	$G1V_{DD}$	---
D1_MDQ53	Data	P30	IO	$G1V_{DD}$	---
D1_MDQ54	Data	T29	IO	$G1V_{DD}$	---
D1_MDQ55	Data	V30	IO	$G1V_{DD}$	---
D1_MDQ56	Data	P34	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ57	Data	P33	IO	$G1V_{DD}$	---
D1_MDQ58	Data	V34	IO	$G1V_{DD}$	---
D1_MDQ59	Data	V33	IO	$G1V_{DD}$	---
D1_MDQ60	Data	N33	IO	$G1V_{DD}$	---
D1_MDQ61	Data	N32	IO	$G1V_{DD}$	---
D1_MDQ62	Data	U33	IO	$G1V_{DD}$	---
D1_MDQ63	Data	U32	IO	$G1V_{DD}$	---
D1_MDQS00	Data Strobe	L25	IO	$G1V_{DD}$	---
D1_MDQS00_B	Data Strobe	K25	IO	$G1V_{DD}$	---
D1_MDQS01	Data Strobe	F26	IO	$G1V_{DD}$	---
D1_MDQS01_B	Data Strobe	F25	IO	$G1V_{DD}$	---
D1_MDQS02	Data Strobe	D25	IO	$G1V_{DD}$	---
D1_MDQS02_B	Data Strobe	C25	IO	$G1V_{DD}$	---
D1_MDQS03	Data Strobe	G28	IO	$G1V_{DD}$	---
D1_MDQS03_B	Data Strobe	F28	IO	$G1V_{DD}$	---
D1_MDQS04	Data Strobe	M31	IO	$G1V_{DD}$	---
D1_MDQS04_B	Data Strobe	M30	IO	$G1V_{DD}$	---
D1_MDQS05	Data Strobe	K33	IO	$G1V_{DD}$	---
D1_MDQS05_B	Data Strobe	K34	IO	$G1V_{DD}$	---
D1_MDQS06	Data Strobe	V31	IO	$G1V_{DD}$	---
D1_MDQS06_B	Data Strobe	U31	IO	$G1V_{DD}$	---
D1_MDQS07	Data Strobe	T33	IO	$G1V_{DD}$	---
D1_MDQS07_B	Data Strobe	T34	IO	$G1V_{DD}$	---
D1_MDQS08	Data Strobe	F32	IO	$G1V_{DD}$	---
D1_MDQS08_B	Data Strobe	F31	IO	$G1V_{DD}$	---
D1_MDQS09/D1_MDM0	Data Strobe (x4 support)	J24	IO	$G1V_{DD}$	---
D1_MDQS09_B	Data Strobe (x4 support)	J25	IO	$G1V_{DD}$	18
D1_MDQS10/D1_MDM1	Data Strobe (x4 support)	H25	IO	$G1V_{DD}$	---
D1_MDQS10_B	Data Strobe (x4 support)	G25	IO	$G1V_{DD}$	18
D1_MDQS11/D1_MDM2	Data Strobe (x4 support)	E24	IO	$G1V_{DD}$	---
D1_MDQS11_B	Data Strobe (x4 support)	E25	IO	$G1V_{DD}$	18
D1_MDQS12/D1_MDM3	Data Strobe (x4 support)	E29	IO	$G1V_{DD}$	---
D1_MDQS12_B	Data Strobe (x4 support)	F29	IO	$G1V_{DD}$	18
D1_MDQS13/D1_MDM4	Data Strobe (x4 support)	K31	IO	$G1V_{DD}$	---
D1_MDQS13_B	Data Strobe (x4 support)	L31	IO	$G1V_{DD}$	---
D1_MDQS14/D1_MDM5	Data Strobe (x4 support)	J33	IO	$G1V_{DD}$	---
D1_MDQS14_B	Data Strobe (x4 support)	J32	IO	$G1V_{DD}$	---
D1_MDQS15/D1_MDM6	Data Strobe (x4 support)	T31	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS15_B	Data Strobe (x4 support)	T30	IO	$G1V_{DD}$	---
D1_MDQS16/D1_MDM7	Data Strobe (x4 support)	R33	IO	$G1V_{DD}$	---
D1_MDQS16_B	Data Strobe (x4 support)	R32	IO	$G1V_{DD}$	---
D1_MDQS17/D1_MDM8	Data Strobe (x4 support)	D31	IO	$G1V_{DD}$	---
D1_MDQS17_B	Data Strobe (x4 support)	D32	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	E31	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	C31	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	H30	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	H31	IO	$G1V_{DD}$	---
D1_MECC4	Error Correcting Code	G30	IO	$G1V_{DD}$	---
D1_MECC5	Error Correcting Code	F30	IO	$G1V_{DD}$	---
D1_MECC6	Error Correcting Code	E33	IO	$G1V_{DD}$	---
D1_MECC7	Error Correcting Code	G32	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	P36	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination / MCID[2]	V36	O	$G1V_{DD}$	2
D1_MODT2	On Die Termination	N35	O	$G1V_{DD}$	2
D1_MODT3	On Die Termination	U35	O	$G1V_{DD}$	2
D1_MPAR	Address Parity Out	G36	O	$G1V_{DD}$	---
D1_MRAS_B	Row Address Strobe / MA[16]	K36	O	$G1V_{DD}$	---
D1_MWE_B	Write Enable / MA[14]	L36	O	$G1V_{DD}$	---
DDR SDRAM Memory Interface 2					
D2_MA00	Address	AK35	O	$G2V_{DD}$	---
D2_MA01	Address	AP34	O	$G2V_{DD}$	---
D2_MA02	Address	AT34	O	$G2V_{DD}$	---
D2_MA03	Address	AT33	O	$G2V_{DD}$	---
D2_MA04	Address	AP33	O	$G2V_{DD}$	---
D2_MA05	Address	AT32	O	$G2V_{DD}$	---
D2_MA06	Address	AR32	O	$G2V_{DD}$	---
D2_MA07	Address	AT30	O	$G2V_{DD}$	---
D2_MA08	Address	AT31	O	$G2V_{DD}$	---
D2_MA09	Address	AT29	O	$G2V_{DD}$	---
D2_MA10	Address	AH36	O	$G2V_{DD}$	---
D2_MA11	Address	AR30	O	$G2V_{DD}$	---
D2_MA12	Address	AT28	O	$G2V_{DD}$	---
D2_MA13	Address	AB36	O	$G2V_{DD}$	---
D2_MA17	Address	Y36	O	$G2V_{DD}$	---
D2_MACT_B	Activate	AR26	O	$G2V_{DD}$	---
D2_MALERT_B	Alert	AR28	I	$G2V_{DD}$	1, 29

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MBA0	Bank Select	AH35	O	$G2V_{DD}$	---
D2_MBA1	Bank Select	AJ36	O	$G2V_{DD}$	---
D2_MBG0	Bank Group	AT26	O	$G2V_{DD}$	---
D2_MBG1	Bank Group	AT27	O	$G2V_{DD}$	---
D2_MCAS_B	Column Address Strobe / MA[15]	AD36	O	$G2V_{DD}$	---
D2_MCK0	Clock	AR35	O	$G2V_{DD}$	---
D2_MCK0_B	Clock Complement	AR34	O	$G2V_{DD}$	---
D2_MCK1	Clock	AP36	O	$G2V_{DD}$	---
D2_MCK1_B	Clock Complement	AP35	O	$G2V_{DD}$	---
D2_MCK2	Clock	AN35	O	$G2V_{DD}$	---
D2_MCK2_B	Clock Complement	AN34	O	$G2V_{DD}$	---
D2_MCK3	Clock	AM36	O	$G2V_{DD}$	---
D2_MCK3_B	Clock Complement	AM35	O	$G2V_{DD}$	---
D2_MCKE0	Clock Enable	AT25	O	$G2V_{DD}$	2
D2_MCKE1	Clock Enable	AR24	O	$G2V_{DD}$	2
D2_MCKE2	Clock Enable	AT24	O	$G2V_{DD}$	2
D2_MCKE3	Clock Enable	AT23	O	$G2V_{DD}$	2
D2_MCS0_B	Chip Select	AF35	O	$G2V_{DD}$	---
D2_MCS1_B	Chip Select	AA36	O	$G2V_{DD}$	---
D2_MCS2_B	Chip Select / MCID[0]	AE36	O	$G2V_{DD}$	---
D2_MCS3_B	Chip Select / MCID[1]	AB35	O	$G2V_{DD}$	---
D2_MDIC0	Driver Impedance Calibration	AN36	IO	$G2V_{DD}$	3
D2_MDIC1	Driver Impedance Calibration	AL36	IO	$G2V_{DD}$	3
D2_MDM0/**D2_MDQS09**	Data Mask	AH24	O	$G2V_{DD}$	1
D2_MDM1/**D2_MDQS10**	Data Mask	AJ25	O	$G2V_{DD}$	1
D2_MDM2/**D2_MDQS11**	Data Mask	AM24	O	$G2V_{DD}$	1
D2_MDM3/**D2_MDQS12**	Data Mask	AM29	O	$G2V_{DD}$	1
D2_MDM4/**D2_MDQS13**	Data Mask	AG31	O	$G2V_{DD}$	1
D2_MDM5/**D2_MDQS14**	Data Mask	AH33	O	$G2V_{DD}$	1
D2_MDM6/**D2_MDQS15**	Data Mask	AA31	O	$G2V_{DD}$	1
D2_MDM7/**D2_MDQS16**	Data Mask	AB33	O	$G2V_{DD}$	1
D2_MDM8/**D2_MDQS17**	Data Mask	AN31	O	$G2V_{DD}$	1
D2_MDQ00	Data	AF23	IO	$G2V_{DD}$	---
D2_MDQ01	Data	AF24	IO	$G2V_{DD}$	---
D2_MDQ02	Data	AH27	IO	$G2V_{DD}$	---
D2_MDQ03	Data	AG27	IO	$G2V_{DD}$	---
D2_MDQ04	Data	AG23	IO	$G2V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ05	Data	AH23	IO	$G2V_{DD}$	---
D2_MDQ06	Data	AG26	IO	$G2V_{DD}$	---
D2_MDQ07	Data	AF26	IO	$G2V_{DD}$	---
D2_MDQ08	Data	AJ23	IO	$G2V_{DD}$	---
D2_MDQ09	Data	AK24	IO	$G2V_{DD}$	---
D2_MDQ10	Data	AL27	IO	$G2V_{DD}$	---
D2_MDQ11	Data	AK27	IO	$G2V_{DD}$	---
D2_MDQ12	Data	AK23	IO	$G2V_{DD}$	---
D2_MDQ13	Data	AL23	IO	$G2V_{DD}$	---
D2_MDQ14	Data	AJ26	IO	$G2V_{DD}$	---
D2_MDQ15	Data	AJ27	IO	$G2V_{DD}$	---
D2_MDQ16	Data	AM23	IO	$G2V_{DD}$	---
D2_MDQ17	Data	AN24	IO	$G2V_{DD}$	---
D2_MDQ18	Data	AP27	IO	$G2V_{DD}$	---
D2_MDQ19	Data	AN27	IO	$G2V_{DD}$	---
D2_MDQ20	Data	AN23	IO	$G2V_{DD}$	---
D2_MDQ21	Data	AP23	IO	$G2V_{DD}$	---
D2_MDQ22	Data	AN26	IO	$G2V_{DD}$	---
D2_MDQ23	Data	AM27	IO	$G2V_{DD}$	---
D2_MDQ24	Data	AN29	IO	$G2V_{DD}$	---
D2_MDQ25	Data	AN30	IO	$G2V_{DD}$	---
D2_MDQ26	Data	AH29	IO	$G2V_{DD}$	---
D2_MDQ27	Data	AG28	IO	$G2V_{DD}$	---
D2_MDQ28	Data	AN28	IO	$G2V_{DD}$	---
D2_MDQ29	Data	AP29	IO	$G2V_{DD}$	---
D2_MDQ30	Data	AJ29	IO	$G2V_{DD}$	---
D2_MDQ31	Data	AH28	IO	$G2V_{DD}$	---
D2_MDQ32	Data	AG30	IO	$G2V_{DD}$	---
D2_MDQ33	Data	AF29	IO	$G2V_{DD}$	---
D2_MDQ34	Data	AD31	IO	$G2V_{DD}$	---
D2_MDQ35	Data	AC29	IO	$G2V_{DD}$	---
D2_MDQ36	Data	AG29	IO	$G2V_{DD}$	---
D2_MDQ37	Data	AH31	IO	$G2V_{DD}$	---
D2_MDQ38	Data	AE29	IO	$G2V_{DD}$	---
D2_MDQ39	Data	AD29	IO	$G2V_{DD}$	---
D2_MDQ40	Data	AJ34	IO	$G2V_{DD}$	---
D2_MDQ41	Data	AJ33	IO	$G2V_{DD}$	---
D2_MDQ42	Data	AE34	IO	$G2V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ43	Data	AE33	IO	$G2V_{DD}$	---
D2_MDQ44	Data	AL34	IO	$G2V_{DD}$	---
D2_MDQ45	Data	AK33	IO	$G2V_{DD}$	---
D2_MDQ46	Data	AF33	IO	$G2V_{DD}$	---
D2_MDQ47	Data	AF32	IO	$G2V_{DD}$	---
D2_MDQ48	Data	AB31	IO	$G2V_{DD}$	---
D2_MDQ49	Data	AB29	IO	$G2V_{DD}$	---
D2_MDQ50	Data	Y29	IO	$G2V_{DD}$	---
D2_MDQ51	Data	W29	IO	$G2V_{DD}$	---
D2_MDQ52	Data	AC31	IO	$G2V_{DD}$	---
D2_MDQ53	Data	AC30	IO	$G2V_{DD}$	---
D2_MDQ54	Data	AA29	IO	$G2V_{DD}$	---
D2_MDQ55	Data	W30	IO	$G2V_{DD}$	---
D2_MDQ56	Data	AC34	IO	$G2V_{DD}$	---
D2_MDQ57	Data	AC33	IO	$G2V_{DD}$	---
D2_MDQ58	Data	W34	IO	$G2V_{DD}$	---
D2_MDQ59	Data	W33	IO	$G2V_{DD}$	---
D2_MDQ60	Data	AD33	IO	$G2V_{DD}$	---
D2_MDQ61	Data	AD32	IO	$G2V_{DD}$	---
D2_MDQ62	Data	Y33	IO	$G2V_{DD}$	---
D2_MDQ63	Data	Y32	IO	$G2V_{DD}$	---
D2_MDQS00	Data Strobe	AF25	IO	$G2V_{DD}$	---
D2_MDQS00_B	Data Strobe	AG25	IO	$G2V_{DD}$	---
D2_MDQS01	Data Strobe	AL26	IO	$G2V_{DD}$	---
D2_MDQS01_B	Data Strobe	AL25	IO	$G2V_{DD}$	---
D2_MDQS02	Data Strobe	AN25	IO	$G2V_{DD}$	---
D2_MDQS02_B	Data Strobe	AP25	IO	$G2V_{DD}$	---
D2_MDQS03	Data Strobe	AK28	IO	$G2V_{DD}$	---
D2_MDQS03_B	Data Strobe	AL28	IO	$G2V_{DD}$	---
D2_MDQS04	Data Strobe	AE31	IO	$G2V_{DD}$	---
D2_MDQS04_B	Data Strobe	AE30	IO	$G2V_{DD}$	---
D2_MDQS05	Data Strobe	AG33	IO	$G2V_{DD}$	---
D2_MDQS05_B	Data Strobe	AG34	IO	$G2V_{DD}$	---
D2_MDQS06	Data Strobe	W31	IO	$G2V_{DD}$	---
D2_MDQS06_B	Data Strobe	Y31	IO	$G2V_{DD}$	---
D2_MDQS07	Data Strobe	AA33	IO	$G2V_{DD}$	---
D2_MDQS07_B	Data Strobe	AA34	IO	$G2V_{DD}$	---
D2_MDQS08	Data Strobe	AL32	IO	$G2V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQS08_B	Data Strobe	AL31	IO	$G2V_{DD}$	---
D2_MDQS09/D2_MDM0	Data Strobe (x4 support)	AH24	IO	$G2V_{DD}$	---
D2_MDQS09_B	Data Strobe (x4 support)	AH25	IO	$G2V_{DD}$	18
D2_MDQS10/D2_MDM1	Data Strobe (x4 support)	AJ25	IO	$G2V_{DD}$	---
D2_MDQS10_B	Data Strobe (x4 support)	AK25	IO	$G2V_{DD}$	18
D2_MDQS11/D2_MDM2	Data Strobe (x4 support)	AM24	IO	$G2V_{DD}$	---
D2_MDQS11_B	Data Strobe (x4 support)	AM25	IO	$G2V_{DD}$	18
D2_MDQS12/D2_MDM3	Data Strobe (x4 support)	AM29	IO	$G2V_{DD}$	---
D2_MDQS12_B	Data Strobe (x4 support)	AL29	IO	$G2V_{DD}$	18
D2_MDQS13/D2_MDM4	Data Strobe (x4 support)	AG31	IO	$G2V_{DD}$	---
D2_MDQS13_B	Data Strobe (x4 support)	AF31	IO	$G2V_{DD}$	---
D2_MDQS14/D2_MDM5	Data Strobe (x4 support)	AH33	IO	$G2V_{DD}$	---
D2_MDQS14_B	Data Strobe (x4 support)	AH32	IO	$G2V_{DD}$	---
D2_MDQS15/D2_MDM6	Data Strobe (x4 support)	AA31	IO	$G2V_{DD}$	---
D2_MDQS15_B	Data Strobe (x4 support)	AA30	IO	$G2V_{DD}$	---
D2_MDQS16/D2_MDM7	Data Strobe (x4 support)	AB33	IO	$G2V_{DD}$	---
D2_MDQS16_B	Data Strobe (x4 support)	AB32	IO	$G2V_{DD}$	---
D2_MDQS17/D2_MDM8	Data Strobe (x4 support)	AN31	IO	$G2V_{DD}$	---
D2_MDQS17_B	Data Strobe (x4 support)	AN32	IO	$G2V_{DD}$	---
D2_MECC0	Error Correcting Code	AM31	IO	$G2V_{DD}$	---
D2_MECC1	Error Correcting Code	AP31	IO	$G2V_{DD}$	---
D2_MECC2	Error Correcting Code	AJ30	IO	$G2V_{DD}$	---
D2_MECC3	Error Correcting Code	AJ31	IO	$G2V_{DD}$	---
D2_MECC4	Error Correcting Code	AK30	IO	$G2V_{DD}$	---
D2_MECC5	Error Correcting Code	AL30	IO	$G2V_{DD}$	---
D2_MECC6	Error Correcting Code	AM33	IO	$G2V_{DD}$	---
D2_MECC7	Error Correcting Code	AK32	IO	$G2V_{DD}$	---
D2_MODT0	On Die Termination	AC36	O	$G2V_{DD}$	2
D2_MODT1	On Die Termination / MCID[2]	W36	O	$G2V_{DD}$	2
D2_MODT2	On Die Termination	AD35	O	$G2V_{DD}$	2
D2_MODT3	On Die Termination	Y35	O	$G2V_{DD}$	2
D2_MPAR	Address Parity Out	AK36	O	$G2V_{DD}$	---
D2_MRAS_B	Row Address Strobe / MA[16]	AG36	O	$G2V_{DD}$	---
D2_MWE_B	Write Enable / MA[14]	AF36	O	$G2V_{DD}$	---
DDR SDRAM Memory Interface 3					
D3_MA00	Address	N4	O	$G3V_{DD}$	---
D3_MA01	Address	M7	O	$G3V_{DD}$	---
D3_MA02	Address	M6	O	$G3V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D3_MA03	Address	N6	O	$G3V_{DD}$	---
D3_MA04	Address	P7	O	$G3V_{DD}$	---
D3_MA05	Address	P6	O	$G3V_{DD}$	---
D3_MA06	Address	R6	O	$G3V_{DD}$	---
D3_MA07	Address	R4	O	$G3V_{DD}$	---
D3_MA08	Address	R5	O	$G3V_{DD}$	---
D3_MA09	Address	P5	O	$G3V_{DD}$	---
D3_MA10	Address	M1	O	$G3V_{DD}$	---
D3_MA11	Address	T4	O	$G3V_{DD}$	---
D3_MA12	Address	M3	O	$G3V_{DD}$	---
D3_MA13	Address	R7	O	$G3V_{DD}$	---
D3_MACT_B	Activate	V7	O	$G3V_{DD}$	---
D3_MALERT_B	Alert	Y7	I	$G3V_{DD}$	1, 29
D3_MBA0	Bank Select	M5	O	$G3V_{DD}$	---
D3_MBA1	Bank Select	M4	O	$G3V_{DD}$	---
D3_MBG0	Bank Group	R3	O	$G3V_{DD}$	---
D3_MBG1	Bank Group	P3	O	$G3V_{DD}$	---
D3_MCAS_B	Column Address Strobe	P9	O	$G3V_{DD}$	---
D3_MCK0	Clock	P1	O	$G3V_{DD}$	---
D3_MCK0_B	Clock Complement	P2	O	$G3V_{DD}$	---
D3_MCK1	Clock	R1	O	$G3V_{DD}$	---
D3_MCK1_B	Clock Complement	R2	O	$G3V_{DD}$	---
D3_MCKE0	Clock Enable	V8	O	$G3V_{DD}$	2
D3_MCKE1	Clock Enable	W8	O	$G3V_{DD}$	2
D3_MCS0_B	Chip Select	U8	O	$G3V_{DD}$	---
D3_MCS1_B	Chip Select	T8	O	$G3V_{DD}$	---
D3_MCS2_B	Chip Select	N8	O	$G3V_{DD}$	---
D3_MCS3_B	Chip Select	M8	O	$G3V_{DD}$	---
D3_MDIC0	Driver Impedance Calibration	T2	IO	$G3V_{DD}$	3
D3_MDIC1	Driver Impedance Calibration	N2	IO	$G3V_{DD}$	3
D3_MDM0	Data Mask	Y3	O	$G3V_{DD}$	---
D3_MDM1	Data Mask	Y4	O	$G3V_{DD}$	---
D3_MDM2	Data Mask	AE1	O	$G3V_{DD}$	---
D3_MDM3	Data Mask	AD5	O	$G3V_{DD}$	---
D3_MDM8	Data Mask	AD8	O	$G3V_{DD}$	---
D3_MDQ00	Data	AA1	IO	$G3V_{DD}$	---
D3_MDQ01	Data	Y1	IO	$G3V_{DD}$	---
D3_MDQ02	Data	V3	IO	$G3V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D3_MDQ03	Data	U3	IO	$G3V_{DD}$	---
D3_MDQ04	Data	AA3	IO	$G3V_{DD}$	---
D3_MDQ05	Data	Y2	IO	$G3V_{DD}$	---
D3_MDQ06	Data	V2	IO	$G3V_{DD}$	---
D3_MDQ07	Data	U1	IO	$G3V_{DD}$	---
D3_MDQ08	Data	AA5	IO	$G3V_{DD}$	---
D3_MDQ09	Data	Y5	IO	$G3V_{DD}$	---
D3_MDQ10	Data	V4	IO	$G3V_{DD}$	---
D3_MDQ11	Data	U5	IO	$G3V_{DD}$	---
D3_MDQ12	Data	AB5	IO	$G3V_{DD}$	---
D3_MDQ13	Data	AA6	IO	$G3V_{DD}$	---
D3_MDQ14	Data	V5	IO	$G3V_{DD}$	---
D3_MDQ15	Data	U6	IO	$G3V_{DD}$	---
D3_MDQ16	Data	AF2	IO	$G3V_{DD}$	---
D3_MDQ17	Data	AE3	IO	$G3V_{DD}$	---
D3_MDQ18	Data	AC1	IO	$G3V_{DD}$	---
D3_MDQ19	Data	AB1	IO	$G3V_{DD}$	---
D3_MDQ20	Data	AF3	IO	$G3V_{DD}$	---
D3_MDQ21	Data	AF1	IO	$G3V_{DD}$	---
D3_MDQ22	Data	AC3	IO	$G3V_{DD}$	---
D3_MDQ23	Data	AB2	IO	$G3V_{DD}$	---
D3_MDQ24	Data	AF4	IO	$G3V_{DD}$	---
D3_MDQ25	Data	AE5	IO	$G3V_{DD}$	---
D3_MDQ26	Data	AC5	IO	$G3V_{DD}$	---
D3_MDQ27	Data	AB3	IO	$G3V_{DD}$	---
D3_MDQ28	Data	AF5	IO	$G3V_{DD}$	---
D3_MDQ29	Data	AE6	IO	$G3V_{DD}$	---
D3_MDQ30	Data	AC6	IO	$G3V_{DD}$	---
D3_MDQ31	Data	AB4	IO	$G3V_{DD}$	---
D3_MDQS0	Data Strobe	V1	IO	$G3V_{DD}$	---
D3_MDQS0_B	Data Strobe	W1	IO	$G3V_{DD}$	---
D3_MDQS1	Data Strobe	W5	IO	$G3V_{DD}$	---
D3_MDQS1_B	Data Strobe	W6	IO	$G3V_{DD}$	---
D3_MDQS2	Data Strobe	AD1	IO	$G3V_{DD}$	---
D3_MDQS2_B	Data Strobe	AD2	IO	$G3V_{DD}$	---
D3_MDQS3	Data Strobe	AD3	IO	$G3V_{DD}$	---
D3_MDQS3_B	Data Strobe	AD4	IO	$G3V_{DD}$	---
D3_MDQS8	Data Strobe	AC7	IO	$G3V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D3_MDQS8_B	Data Strobe	AD7	IO	$G3V_{DD}$	---
D3_MECC0	Error Correcting Code	AE7	IO	$G3V_{DD}$	---
D3_MECC1	Error Correcting Code	AD9	IO	$G3V_{DD}$	---
D3_MECC2	Error Correcting Code	AC9	IO	$G3V_{DD}$	---
D3_MECC3	Error Correcting Code	AB7	IO	$G3V_{DD}$	---
D3_MODT0	On Die Termination	T7	O	$G3V_{DD}$	2
D3_MODT1	On Die Termination	R8	O	$G3V_{DD}$	2
D3_MPAR	Address Parity Out	P4	O	$G3V_{DD}$	---
D3_MRAS_B	Row Address Strobe	M2	O	$G3V_{DD}$	---
D3_MWE_B	Write Enable	P8	O	$G3V_{DD}$	---
Integrated Flash Controller					
IFC_A00/GPIO1_16/ QSPI_A_CS0	IFC Address	E16	O	OV_{DD}	1, 5
IFC_A01/GPIO1_17/ QSPI_A_CS1	IFC Address	D16	O	OV_{DD}	1, 5
IFC_A02/GPIO1_18/ QSPI_A_SCK	IFC Address	E15	O	OV_{DD}	1, 5
IFC_A03/GPIO1_19/ QSPI_B_CS0	IFC Address	D15	O	OV_{DD}	1, 5
IFC_A04/GPIO1_20/ QSPI_B_CS1	IFC Address	E14	O	OV_{DD}	1, 5
IFC_A05/GPIO1_21/ QSPI_B_SCK	IFC Address	E13	O	OV_{DD}	1, 5
IFC_A06/GPIO2_00/ IFC_WP1_B/QSPI_A_DATA0	IFC Address	D13	O	OV_{DD}	1
IFC_A07/GPIO2_01/ IFC_WP2_B/QSPI_A_DATA1	IFC Address	E12	O	OV_{DD}	1
IFC_A08/GPIO2_02/ IFC_WP3_B/QSPI_A_DATA2	IFC Address	D12	O	OV_{DD}	1
IFC_A09/GPIO2_03/ IFC_RB2_B/QSPI_A_DATA3	IFC Address	E11	O	OV_{DD}	1
IFC_A10/GPIO2_04/ IFC_RB3_B/QSPI_A_DQS	IFC Address	E10	O	OV_{DD}	1
IFC_A11/GPIO2_05/ IFC_RB4_B/QSPI_B_DQS	IFC Address	D10	O	OV_{DD}	1
IFC_AD00/GPIO1_00/ cfg_gpinput00	IFC Address / Data	B10	IO	OV_{DD}	9
IFC_AD01/GPIO1_01/ cfg_gpinput01	IFC Address / Data	C10	IO	OV_{DD}	9
IFC_AD02/GPIO1_02/ cfg_gpinput02	IFC Address / Data	A11	IO	OV_{DD}	9
IFC_AD03/GPIO1_03/ cfg_gpinput03	IFC Address / Data	C11	IO	OV_{DD}	9

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_AD04/GPIO1_04/ cfg_gpinput04	IFC Address / Data	A12	IO	OV_{DD}	9
IFC_AD05/GPIO1_05/ cfg_gpinput05	IFC Address / Data	B12	IO	OV_{DD}	9
IFC_AD06/GPIO1_06/ cfg_gpinput06	IFC Address / Data	C12	IO	OV_{DD}	9
IFC_AD07/GPIO1_07/ cfg_gpinput07	IFC Address / Data	A13	IO	OV_{DD}	9
IFC_AD08/GPIO1_08/ cfg_rcw_src01	IFC Address / Data	B13	IO	OV_{DD}	9
IFC_AD09/GPIO1_09/ cfg_rcw_src02	IFC Address / Data	C13	IO	OV_{DD}	9
IFC_AD10/GPIO1_10/ cfg_rcw_src03	IFC Address / Data	A14	IO	OV_{DD}	9
IFC_AD11/GPIO1_11/ cfg_rcw_src04	IFC Address / Data	C14	IO	OV_{DD}	9
IFC_AD12/GPIO1_12/ cfg_rcw_src05	IFC Address / Data	A15	IO	OV_{DD}	9
IFC_AD13/GPIO1_13/ cfg_rcw_src06	IFC Address / Data	B15	IO	OV_{DD}	9
IFC_AD14/GPIO1_14/ cfg_rcw_src07	IFC Address / Data	C15	IO	OV_{DD}	9
IFC_AD15/GPIO1_15/ cfg_rcw_src08	IFC Address / Data	A16	IO	OV_{DD}	9
IFC_ALE/GPIO1_24	IFC Address Latch Enable	C19	O	OV_{DD}	1, 5
IFC_BCTL/GPIO2_12	IFC Buffer control	C16	O	OV_{DD}	1
IFC_CLE/GPIO1_25/ cfg_rcw_src0	IFC NAND Command Latch Enable / Write Enable 1 / NOR Address active-low Valid	B19	O	OV_{DD}	1, 4
IFC_CLK0/GPIO2_17	IFC Clock	B21	O	OV_{DD}	1
IFC_CLK1/GPIO2_18	IFC Clock	C21	O	OV_{DD}	1
IFC_CS0_B/GPIO2_08	IFC Chip Select	C18	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_09	IFC Chip Select	C20	O	OV_{DD}	1, 6
IFC_CS2_B/GPIO2_10	IFC Chip Select	A21	O	OV_{DD}	1, 6
IFC_CS3_B/GPIO2_11/ QSPI_B_DATA3/ QSPI_A_DATA7	IFC Chip Select	E17	O	OV_{DD}	1, 6
IFC_CS4_B/GPIO3_02	IFC Chip Select	D18	O	OV_{DD}	1, 6
IFC_CS5_B/GPIO3_03	IFC Chip Select	E18	O	OV_{DD}	1, 6
IFC_CS6_B/GPIO3_04	IFC Chip Select	D19	O	OV_{DD}	1, 6
IFC_CS7_B/GPIO3_05	IFC Chip Select	E19	O	OV_{DD}	1, 6
IFC_NDDQS/GPIO2_13	IFC DQS Strobe	B18	IO	OV_{DD}	9

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_NDWE_B/GPIO2_19	IFC NAND Write Enable / NAND DDR Clock	A10	O	OV_{DD}	1
IFC_OE_B/GPIO1_26	IFC Output Enable	A19	O	OV_{DD}	1, 5
IFC_PAR0/GPIO2_06/ QSPI_B_DATA0/ QSPI_A_DATA4	IFC Address & Data Parity	E20	IO	OV_{DD}	9
IFC_PAR1/GPIO2_07/ QSPI_B_DATA1/ QSPI_A_DATA5	IFC Address & Data Parity	E21	IO	OV_{DD}	9
IFC_PERR_B/GPIO2_16/ QSPI_B_DATA2/ QSPI_A_DATA6	IFC Parity Error	D21	I	OV_{DD}	1
IFC_RB0_B/GPIO2_14	IFC Ready/Busy CS0	A18	I	OV_{DD}	1, 6
IFC_RB1_B/GPIO2_15	IFC Ready/Busy CS1	A17	I	OV_{DD}	1, 6
IFC_RB2_B/**IFC_A09**/ GPIO2_03/QSPI_A_DATA3	IFC Ready/Busy CS 2	E11	I	OV_{DD}	1
IFC_RB3_B/**IFC_A10**/ GPIO2_04/QSPI_A_DQS	IFC Ready/Busy CS 3	E10	I	OV_{DD}	1
IFC_RB4_B/**IFC_A11**/ GPIO2_05/QSPI_B_DQS	IFC Ready/Busy CS 4	D10	I	OV_{DD}	1
IFC_TE/GPIO1_23/cfg_ifc_te	IFC External Transceiver Enable	B16	O	OV_{DD}	1, 4
IFC_WE0_B/GPIO1_22/ cfg_eng_use0	IFC Write Enable 0 / Start of Frame	C17	O	OV_{DD}	1, 28
IFC_WP0_B/GPIO1_27	IFC Write Protect	A20	O	OV_{DD}	1, 5
IFC_WP1_B/**IFC_A06**/ GPIO2_00/QSPI_A_DATA0	IFC Write Protect	D13	O	OV_{DD}	1
IFC_WP2_B/**IFC_A07**/ GPIO2_01/QSPI_A_DATA1	IFC Write Protect	E12	O	OV_{DD}	1
IFC_WP3_B/**IFC_A08**/ GPIO2_02/QSPI_A_DATA2	IFC Write Protect	D12	O	OV_{DD}	1
DUART					
UART1_CTS_B/GPIO3_10/ UART3_SIN	Clear To Send	G4	I	OV_{DD}	1
UART1_RTS_B/GPIO3_08/ UART3_SOUT	Ready to Send	G3	O	OV_{DD}	1
UART1_SIN	Receive Data	H3	I	OV_{DD}	1
UART1_SOUT	Transmit Data	J4	O	OV_{DD}	1
UART2_CTS_B/GPIO3_11/ UART4_SIN	Clear To Send	K3	I	OV_{DD}	1
UART2_RTS_B/GPIO3_09/ UART4_SOUT	Ready to Send	J3	O	OV_{DD}	1
UART2_SIN/GPIO3_07	Receive Data	K4	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART2_SOUT/GPIO3_06	Transmit Data	L3	O	OV_{DD}	1
UART3_SIN/**UART1_CTS_B**/ GPIO3_10	Receive Data	G4	I	OV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO3_08	Transmit Data	G3	O	OV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO3_11	Receive Data	K3	I	OV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO3_09	Transmit Data	J3	O	OV_{DD}	1
I2C					
IIC1_SCL	Serial Clock	K8	IO	OV_{DD}	7, 8
IIC1_SDA	Serial Data	L8	IO	OV_{DD}	7, 8
IIC2_SCL/GPIO3_12/ SDHC_CD_B	Serial Clock	H8	IO	OV_{DD}	7, 8
IIC2_SDA/GPIO3_13/ SDHC_WP	Serial Data	J8	IO	OV_{DD}	7, 8
IIC3_SCL/GPIO4_00/EVT5_B/ SPI_PCS4	Serial Clock	K5	IO	OV_{DD}	7, 8
IIC3_SDA/GPIO4_01/EVT6_B/ SPI_PCS5	Serial Data	L5	IO	OV_{DD}	7, 8
IIC4_SCL/GPIO4_02/EVT7_B	Serial Clock	K7	IO	OV_{DD}	7, 8
IIC4_SDA/GPIO4_03/EVT8_B	Serial Data	L7	IO	OV_{DD}	7, 8
SPI Interface					
SPI_PCS0/GPIO3_17/ SDHC_DAT4/SDHC_VS	SPI Chip Select	B7	IO	OV_{DD}	---
SPI_PCS1/GPIO3_18/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	C7	O	OV_{DD}	1
SPI_PCS2/GPIO3_19/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	B9	O	OV_{DD}	1
SPI_PCS3/GPIO3_20/ SDHC_DAT7/ SDHC_DAT123_DIR	SPI Chip Select	C9	O	OV_{DD}	1
SPI_PCS4/**IIC3_SCL**/ GPIO4_00/EVT5_B	Chip Select 4	K5	O	OV_{DD}	1
SPI_PCS5/**IIC3_SDA**/ GPIO4_01/EVT6_B	Chips Select 5	L5	O	OV_{DD}	1
SPI_SCK/GPIO3_16	SPI Clock	A7	IO	OV_{DD}	---
SPI_SIN/GPIO3_15	Master In Slave Out	A9	I	OV_{DD}	1
SPI_SOUT/GPIO3_14	Master Out Slave In	A8	O	OV_{DD}	1
eSDHC					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_CD_B/**IIC2_SCL**/ GPIO3_12	SDHC Card Detect	H8	I	OV_{DD}	1
SDHC_CLK/GPIO3_26	Host to Card Clock	C8	O	OV_{DD}	1
SDHC_CMD/GPIO3_21	Command/Response	D7	IO	OV_{DD}	24
SDHC_CMD_DIR/**SPI_PCS1**/ GPIO3_18/SDHC_DAT5	DIR	C7	O	OV_{DD}	1
SDHC_DAT0/GPIO3_22	Data	E7	IO	OV_{DD}	24
SDHC_DAT0_DIR/**SPI_PCS2**/ GPIO3_19/SDHC_DAT6	DIR	B9	O	OV_{DD}	1
SDHC_DAT1/GPIO3_23	Data	E8	IO	OV_{DD}	24
SDHC_DAT123_DIR/ **SPI_PCS3**/GPIO3_20/ SDHC_DAT7	DIR	C9	O	OV_{DD}	1
SDHC_DAT2/GPIO3_24	Data	D9	IO	OV_{DD}	24
SDHC_DAT3/GPIO3_25	Data	E9	IO	OV_{DD}	24
SDHC_DAT4/**SPI_PCS0**/ GPIO3_17/SDHC_VS	Data	B7	IO	OV_{DD}	---
SDHC_DAT5/**SPI_PCS1**/ GPIO3_18/SDHC_CMD_DIR	Data	C7	IO	OV_{DD}	---
SDHC_DAT6/**SPI_PCS2**/ GPIO3_19/SDHC_DAT0_DIR	Data	B9	IO	OV_{DD}	---
SDHC_DAT7/**SPI_PCS3**/ GPIO3_20/ SDHC_DAT123_DIR	Data	C9	IO	OV_{DD}	---
SDHC_VS/**SPI_PCS0**/ GPIO3_17/SDHC_DAT4	VS	B7	O	OV_{DD}	1
SDHC_WP/**IIC2_SDA**/ GPIO3_13	Write Protect	J8	I	OV_{DD}	1
Interrupt Controller					
IRQ00	External Interrupt	F12	I	OV_{DD}	1
IRQ01	External Interrupt	F14	I	OV_{DD}	1
IRQ02	External Interrupt	F15	I	OV_{DD}	1
IRQ03/GPIO3_27	External Interrupt	F17	I	OV_{DD}	1
IRQ04/GPIO3_28	External Interrupt	F18	I	OV_{DD}	1
IRQ05/GPIO3_29	External Interrupt	F20	I	OV_{DD}	1
IRQ06/GPIO4_04	External Interrupt	G5	I	OV_{DD}	1
IRQ07/GPIO4_05	External Interrupt	G7	I	OV_{DD}	1
IRQ08/GPIO4_06	External Interrupt	J5	I	OV_{DD}	1
IRQ09/GPIO4_07	External Interrupt	J7	I	OV_{DD}	1
IRQ10/GPIO4_08	External Interrupt	F8	I	OV_{DD}	1
IRQ11/GPIO4_09	External Interrupt	K6	I	OV_{DD}	1

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
Trust					
TA_BB_RTC	Reserved	K19	I	$TA_BB_V_{DD}$	15
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	J18	I	$TA_BB_V_{DD}$	---
TA_TMP_DETECT_B	Tamper Detect	K20	I	OV_{DD}	---
System Control					
HRESET_B	Hard Reset	H18	IO	OV_{DD}	7, 8
PORESET_B	Power On Reset	H17	I	OV_{DD}	---
RESET_REQ_B	Reset Request (POR or Hard)	J19	O	OV_{DD}	1, 5
Clocking					
DIFF_SYSCLK	System Clock Differential (positive)	AM21	I	OV_{DD}	---
DIFF_SYSCLK_B	System Clock Differential (negative)	AN21	I	OV_{DD}	---
RTC/GPIO3_30	Real Time Clock	G19	I	OV_{DD}	1
SYSCLK	System Clock	AP21	I	OV_{DD}	---
DDR Clocking					
DDRCLK	DDR Controller Reference Clock	K21	I	OV_{DD}	---
Debug					
ASLEEP/GPIO1_28	Asleep	F7	O	OV_{DD}	1, 5
CKSTP_OUT_B	Reserved	J20	O	OV_{DD}	1, 6, 7
CLK_OUT	Clock Out	G15	O	OV_{DD}	---
EVT0_B	Event 0	G13	IO	OV_{DD}	9
EVT1_B	Event 1	G14	IO	OV_{DD}	9
EVT2_B	Event 2	G16	IO	OV_{DD}	9
EVT3_B	Event 3	G17	IO	OV_{DD}	9
EVT4_B	Event 4	G18	IO	OV_{DD}	9
EVT5_B/**IIC3_SCL**/GPIO4_00/ SPI_PCS4	Event 5	K5	IO	OV_{DD}	---
EVT6_B/**IIC3_SDA**/GPIO4_01/ SPI_PCS5	Event 6	L5	IO	OV_{DD}	---
EVT7_B/**IIC4_SCL**/GPIO4_02	Event 7	K7	IO	OV_{DD}	---
EVT8_B/**IIC4_SDA**/GPIO4_03	Event 8	L7	IO	OV_{DD}	---
EVT9_B/GPIO4_10	Event 9	G12	IO	OV_{DD}	6, 7
DFT					
SCAN_MODE_B	Reserved	F11	I	OV_{DD}	10
TEST_SEL_B	Reserved	G11	I	OV_{DD}	14
JTAG					
TBSCAN_EN_B	Test Boundary Scan Enable	J21	I	OV_{DD}	13

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TCK	Test Clock	H21	I	OV_{DD}	---
TDI	Test Data In	F21	I	OV_{DD}	9
TDO	Test Data Out	G21	O	OV_{DD}	2
TMS	Test Mode Select	H20	I	OV_{DD}	9
TRST_B	Test Reset	G20	I	OV_{DD}	9
Analog Signals					
D1_TPA	DDR Controller 1 Test Point Analog	T26	IO	$G1V_{DD}$	12
D2_TPA	DDR Controller 2 Test Point Analog	AA26	IO	$G2V_{DD}$	12
D3_TPA	DDR Controller 3 Test Point Analog	AB8	IO	$G3V_{DD}$	12
FA_ANALOG_G_V	Reserved	AR22	IO	OV_{DD}	15
FA_ANALOG_PIN	Reserved	AL22	IO	OV_{DD}	15
TD1_ANODE	Thermal diode anode	H15	IO	OV_{DD}	17
TD1_CATHODE	Thermal diode cathode	H16	IO	OV_{DD}	17
TD2_ANODE	Thermal diode anode	K9	IO	OV_{DD}	17
TD2_CATHODE	Thermal diode cathode	L9	IO	OV_{DD}	17
TH_TPA	Thermal Test Point Analog	H14	-	OV_{DD}	12
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedance Calibration	AM8	I	SV_{DD}	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AF9	I	XV_{DD}	16
SD1_PLL1_TPA	SerDes PLL 1 Test Point Analog	AJ9	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	SerDes Test Point Digital	AJ8	O	XV_{DD}	12
SD1_PLL2_TPA	SerDes PLL 2 Test Point Analog	AG8	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	SerDes Test Point Digital	AG7	O	XV_{DD}	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AP9	I	SV_{DD}	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AP8	I	SV_{DD}	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AL1	I	SV_{DD}	---
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AM1	I	SV_{DD}	---
SD1_RX0_N	SerDes Receive Data (negative)	AN2	I	SV_{DD}	---
SD1_RX0_P	SerDes Receive Data (positive)	AP2	I	SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_RX1_N	SerDes Receive Data (negative)	AR3	I	SV_{DD}	---
SD1_RX1_P	SerDes Receive Data (positive)	AT3	I	SV_{DD}	---
SD1_RX2_N	SerDes Receive Data (negative)	AN4	I	SV_{DD}	---
SD1_RX2_P	SerDes Receive Data (positive)	AP4	I	SV_{DD}	---
SD1_RX3_N	SerDes Receive Data (negative)	AR5	I	SV_{DD}	---
SD1_RX3_P	SerDes Receive Data (positive)	AT5	I	SV_{DD}	---
SD1_RX4_N	SerDes Receive Data (negative)	AN6	I	SV_{DD}	---
SD1_RX4_P	SerDes Receive Data (positive)	AP6	I	SV_{DD}	---
SD1_RX5_N	SerDes Receive Data (negative)	AR7	I	SV_{DD}	---
SD1_RX5_P	SerDes Receive Data (positive)	AT7	I	SV_{DD}	---
SD1_RX6_N	SerDes Receive Data (negative)	AR10	I	SV_{DD}	---
SD1_RX6_P	SerDes Receive Data (positive)	AT10	I	SV_{DD}	---
SD1_RX7_N	SerDes Receive Data (negative)	AN11	I	SV_{DD}	---
SD1_RX7_P	SerDes Receive Data (positive)	AP11	I	SV_{DD}	---
SD1_TX0_N	SerDes Transmit Data (negative)	AH2	O	XV_{DD}	---
SD1_TX0_P	SerDes Transmit Data (positive)	AJ2	O	XV_{DD}	---
SD1_TX1_N	SerDes Transmit Data (negative)	AK3	O	XV_{DD}	---
SD1_TX1_P	SerDes Transmit Data (positive)	AL3	O	XV_{DD}	---
SD1_TX2_N	SerDes Transmit Data (negative)	AH4	O	XV_{DD}	---
SD1_TX2_P	SerDes Transmit Data (positive)	AJ4	O	XV_{DD}	---
SD1_TX3_N	SerDes Transmit Data (negative)	AK5	O	XV_{DD}	---
SD1_TX3_P	SerDes Transmit Data (positive)	AL5	O	XV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_TX4_N	SerDes Transmit Data (negative)	AH6	O	XV_{DD}	---
SD1_TX4_P	SerDes Transmit Data (positive)	AJ6	O	XV_{DD}	---
SD1_TX5_N	SerDes Transmit Data (negative)	AK7	O	XV_{DD}	---
SD1_TX5_P	SerDes Transmit Data (positive)	AL7	O	XV_{DD}	---
SD1_TX6_N	SerDes Transmit Data (negative)	AK10	O	XV_{DD}	---
SD1_TX6_P	SerDes Transmit Data (positive)	AL10	O	XV_{DD}	---
SD1_TX7_N	SerDes Transmit Data (negative)	AH11	O	XV_{DD}	---
SD1_TX7_P	SerDes Transmit Data (positive)	AJ11	O	XV_{DD}	---
SerDes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedance Calibration	AM9	I	SV_{DD}	11
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AF19	I	XV_{DD}	16
SD2_PLL1_TPA	SerDes PLL 1 Test Point Analog	AK14	O	AVDD_SD2_PLL1	12
SD2_PLL1_TPD	SerDes Test Point Digital	AM14	O	XV_{DD}	12
SD2_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF21	O	AVDD_SD2_PLL2	12
SD2_PLL2_TPD	SerDes Test Point Digital	AG21	O	XV_{DD}	12
SD2_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AT14	I	SV_{DD}	---
SD2_REF_CLK1_P	SerDes PLL 1 Reference Clock	AR14	I	SV_{DD}	---
SD2_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AJ21	I	SV_{DD}	---
SD2_REF_CLK2_P	SerDes PLL 2 Reference Clock	AH21	I	SV_{DD}	---
SD2_RX0_N	SerDes Receive Data (negative)	AR12	I	SV_{DD}	---
SD2_RX0_P	SerDes Receive Data (positive)	AT12	I	SV_{DD}	---
SD2_RX1_N	SerDes Receive Data (negative)	AN13	I	SV_{DD}	---
SD2_RX1_P	SerDes Receive Data (positive)	AP13	I	SV_{DD}	---
SD2_RX2_N	SerDes Receive Data (negative)	AN15	I	SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_RX2_P	SerDes Receive Data (positive)	AP15	I	SV_{DD}	---
SD2_RX3_N	SerDes Receive Data (negative)	AR16	I	SV_{DD}	---
SD2_RX3_P	SerDes Receive Data (positive)	AT16	I	SV_{DD}	---
SD2_RX4_N	SerDes Receive Data (negative)	AN17	I	SV_{DD}	---
SD2_RX4_P	SerDes Receive Data (positive)	AP17	I	SV_{DD}	---
SD2_RX5_N	SerDes Receive Data (negative)	AR18	I	SV_{DD}	---
SD2_RX5_P	SerDes Receive Data (positive)	AT18	I	SV_{DD}	---
SD2_RX6_N	SerDes Receive Data (negative)	AN19	I	SV_{DD}	---
SD2_RX6_P	SerDes Receive Data (positive)	AP19	I	SV_{DD}	---
SD2_RX7_N	SerDes Receive Data (negative)	AR20	I	SV_{DD}	---
SD2_RX7_P	SerDes Receive Data (positive)	AT20	I	SV_{DD}	---
SD2_TX0_N	SerDes Transmit Data (negative)	AK12	O	XV_{DD}	---
SD2_TX0_P	SerDes Transmit Data (positive)	AL12	O	XV_{DD}	---
SD2_TX1_N	SerDes Transmit Data (negative)	AH13	O	XV_{DD}	---
SD2_TX1_P	SerDes Transmit Data (positive)	AJ13	O	XV_{DD}	---
SD2_TX2_N	SerDes Transmit Data (negative)	AH15	O	XV_{DD}	---
SD2_TX2_P	SerDes Transmit Data (positive)	AJ15	O	XV_{DD}	---
SD2_TX3_N	SerDes Transmit Data (negative)	AK16	O	XV_{DD}	---
SD2_TX3_P	SerDes Transmit Data (positive)	AL16	O	XV_{DD}	---
SD2_TX4_N	SerDes Transmit Data (negative)	AH17	O	XV_{DD}	---
SD2_TX4_P	SerDes Transmit Data (positive)	AJ17	O	XV_{DD}	---
SD2_TX5_N	SerDes Transmit Data (negative)	AK18	O	XV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_TX5_P	SerDes Transmit Data (positive)	AL18	O	XV_{DD}	---
SD2_TX6_N	SerDes Transmit Data (negative)	AH19	O	XV_{DD}	---
SD2_TX6_P	SerDes Transmit Data (positive)	AJ19	O	XV_{DD}	---
SD2_TX7_N	SerDes Transmit Data (negative)	AK20	O	XV_{DD}	---
SD2_TX7_P	SerDes Transmit Data (positive)	AL20	O	XV_{DD}	---
USB PHY 1 & 2					
USB1_D_M	USB PHY Data Minus	E5	IO	-	---
USB1_D_P	USB PHY Data Plus	E4	IO	-	---
USB1_ID	USB PHY ID Detect	H10	I	-	---
USB1_RESREF	USB PHY Impedance Calibration	J10	IO	-	25
USB1_RX_M	USB PHY 3.0 Receive Data (negative)	E2	I	-	---
USB1_RX_P	USB PHY 3.0 Receive Data (positive)	E1	I	-	---
USB1_TX_M	USB PHY 3.0 Transmit Data (negative)	C2	O	-	---
USB1_TX_P	USB PHY 3.0 Transmit Data (positive)	C1	O	-	---
USB1_VBUS	USB PHY VBUS	H9	I	-	27
USB2_D_M	USB PHY Data Minus	D5	IO	-	---
USB2_D_P	USB PHY Data Plus	D4	IO	-	---
USB2_ID	USB PHY ID Detect	H12	I	-	---
USB2_RESREF	USB PHY Impedance Calibration	J11	IO	-	25
USB2_RX_M	USB PHY 3.0 Receive Data (negative)	B3	I	-	---
USB2_RX_P	USB PHY 3.0 Receive Data (positive)	A3	I	-	---
USB2_TX_M	USB PHY 3.0 Transmit Data (negative)	B5	O	-	---
USB2_TX_P	USB PHY 3.0 Transmit Data (positive)	A5	O	-	---
USB2_VBUS	USB PHY VBUS	H11	I	-	27
USB PHY 1 & 2					
USB1_DRVVBUS/GPIO4_24	USB PHY Digital signal - Drive VBUS	F6	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_PWRFAULT/GPIO4_25	USB PHY Digital signal - Power Fault	F3	I	OV_{DD}	1
USB2_DRVVBUS/GPIO4_26	USB PHY Digital signal - Drive VBUS	F9	O	OV_{DD}	1
USB2_PWRFAULT/GPIO4_27	USB PHY Digital signal - Power Fault	C6	I	OV_{DD}	1
IEEE1588					
TSEC_1588_ALARM_OUT1/ GPIO4_19	Alarm Out 1	J1	O	OV_{DD}	1
TSEC_1588_ALARM_OUT2/ GPIO4_20	Alarm Out 2	G1	O	OV_{DD}	1
TSEC_1588_CLK_IN/ GPIO4_16	Clock In	G2	I	OV_{DD}	1
TSEC_1588_CLK_OUT/ GPIO4_21	Clock Out	H1	O	OV_{DD}	1
TSEC_1588_PULSE_OUT1/ GPIO4_22	Pulse Out 1	K1	O	OV_{DD}	1
TSEC_1588_PULSE_OUT2/ GPIO4_23	Pulse Out 2	K2	O	OV_{DD}	1
TSEC_1588_TRIG_IN1/ GPIO4_17	Trigger In 1	L1	I	OV_{DD}	1
TSEC_1588_TRIG_IN2/ GPIO4_18	Trigger In 2	J2	I	OV_{DD}	1
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	G6	O	OV_{DD}	---
EMI1_MDIO	Management Data In/Out	H5	IO	OV_{DD}	---
Ethernet Management Interface 2					
EMI2_MDC	Management Data Clock	J6	O	OV_{DD}	---
EMI2_MDIO	Management Data In/Out	H7	IO	OV_{DD}	---
General Purpose Input/Output					
GPIO1_00/**IFC_AD00**/ cfg_gpinput00	General Purpose Input/Output	B10	IO	OV_{DD}	---
GPIO1_01/**IFC_AD01**/ cfg_gpinput01	General Purpose Input/Output	C10	IO	OV_{DD}	---
GPIO1_02/**IFC_AD02**/ cfg_gpinput02	General Purpose Input/Output	A11	IO	OV_{DD}	---
GPIO1_03/**IFC_AD03**/ cfg_gpinput03	General Purpose Input/Output	C11	IO	OV_{DD}	---
GPIO1_04/**IFC_AD04**/ cfg_gpinput04	General Purpose Input/Output	A12	IO	OV_{DD}	---
GPIO1_05/**IFC_AD05**/ cfg_gpinput05	General Purpose Input/Output	B12	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO1_06/**IFC_AD06**/ cfg_gpinput06	General Purpose Input/Output	C12	IO	OV_{DD}	---
GPIO1_07/**IFC_AD07**/ cfg_gpinput07	General Purpose Input/Output	A13	IO	OV_{DD}	---
GPIO1_08/**IFC_AD08**/ cfg_rcw_src01	General Purpose Input/Output	B13	IO	OV_{DD}	---
GPIO1_09/**IFC_AD09**/ cfg_rcw_src02	General Purpose Input/Output	C13	IO	OV_{DD}	---
GPIO1_10/**IFC_AD10**/ cfg_rcw_src03	General Purpose Input/Output	A14	IO	OV_{DD}	---
GPIO1_11/**IFC_AD11**/ cfg_rcw_src04	General Purpose Input/Output	C14	IO	OV_{DD}	---
GPIO1_12/**IFC_AD12**/ cfg_rcw_src05	General Purpose Input/Output	A15	IO	OV_{DD}	---
GPIO1_13/**IFC_AD13**/ cfg_rcw_src06	General Purpose Input/Output	B15	IO	OV_{DD}	---
GPIO1_14/**IFC_AD14**/ cfg_rcw_src07	General Purpose Input/Output	C15	IO	OV_{DD}	---
GPIO1_15/**IFC_AD15**/ cfg_rcw_src08	General Purpose Input/Output	A16	IO	OV_{DD}	---
GPIO1_16/**IFC_A00**/ QSPI_A_CS0	General Purpose Input/Output	E16	IO	OV_{DD}	5
GPIO1_17/**IFC_A01**/ QSPI_A_CS1	General Purpose Input/Output	D16	IO	OV_{DD}	5
GPIO1_18/**IFC_A02**/ QSPI_A_SCK	General Purpose Input/Output	E15	IO	OV_{DD}	5
GPIO1_19/**IFC_A03**/ QSPI_B_CS0	General Purpose Input/Output	D15	IO	OV_{DD}	5
GPIO1_20/**IFC_A04**/ QSPI_B_CS1	General Purpose Input/Output	E14	IO	OV_{DD}	5
GPIO1_21/**IFC_A05**/ QSPI_B_SCK	General Purpose Input/Output	E13	IO	OV_{DD}	5, 5
GPIO1_22/**IFC_WE0_B**/ cfg_eng_use0	General Purpose Input/Output	C17	IO	OV_{DD}	28
GPIO1_23/**IFC_TE**/cfg_ifc_te	General Purpose Input/Output	B16	IO	OV_{DD}	4
GPIO1_24/**IFC_ALE**	General Purpose Input/Output	C19	IO	OV_{DD}	5
GPIO1_25/**IFC_CLE**/ cfg_rcw_src0	General Purpose Input/Output	B19	IO	OV_{DD}	4
GPIO1_26/**IFC_OE_B**	General Purpose Input/Output	A19	IO	OV_{DD}	5
GPIO1_27/**IFC_WP0_B**	General Purpose Input/Output	A20	IO	OV_{DD}	5
GPIO1_28/**ASLEEP**	General Purpose Input/Output	F7	IO	OV_{DD}	5, 5
GPIO2_00/**IFC_A06**/ IFC_WP1_B/QSPI_A_DATA0	General Purpose Input/Output	D13	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_01/**IFC_A07**/ IFC_WP2_B/QSPI_A_DATA1	General Purpose Input/Output	E12	IO	OV_{DD}	---
GPIO2_02/**IFC_A08**/ IFC_WP3_B/QSPI_A_DATA2	General Purpose Input/Output	D12	IO	OV_{DD}	---
GPIO2_03/**IFC_A09**/ IFC_RB2_B/QSPI_A_DATA3	General Purpose Input/Output	E11	IO	OV_{DD}	---
GPIO2_04/**IFC_A10**/ IFC_RB3_B/QSPI_A_DQS	General Purpose Input/Output	E10	IO	OV_{DD}	---
GPIO2_05/**IFC_A11**/ IFC_RB4_B/QSPI_B_DQS	General Purpose Input/Output	D10	IO	OV_{DD}	---
GPIO2_06/**IFC_PAR0**/ QSPI_B_DATA0/ QSPI_A_DATA4	General Purpose Input/Output	E20	IO	OV_{DD}	---
GPIO2_07/**IFC_PAR1**/ QSPI_B_DATA1/ QSPI_A_DATA5	General Purpose Input/Output	E21	IO	OV_{DD}	---
GPIO2_08/**IFC_CS0_B**	General Purpose Input/Output	C18	IO	OV_{DD}	---
GPIO2_09/**IFC_CS1_B**	General Purpose Input/Output	C20	IO	OV_{DD}	---
GPIO2_10/**IFC_CS2_B**	General Purpose Input/Output	A21	IO	OV_{DD}	---
GPIO2_11/**IFC_CS3_B**/ QSPI_B_DATA3/ QSPI_A_DATA7	General Purpose Input/Output	E17	IO	OV_{DD}	---
GPIO2_12/**IFC_BCTL**	General Purpose Input/Output	C16	IO	OV_{DD}	---
GPIO2_13/**IFC_NDDQS**	General Purpose Input/Output	B18	IO	OV_{DD}	---
GPIO2_14/**IFC_RB0_B**	General Purpose Input/Output	A18	IO	OV_{DD}	---
GPIO2_15/**IFC_RB1_B**	General Purpose Input/Output	A17	IO	OV_{DD}	---
GPIO2_16/**IFC_PERR_B**/ QSPI_B_DATA2/ QSPI_A_DATA6	General Purpose Input/Output	D21	IO	OV_{DD}	---
GPIO2_17/**IFC_CLK0**	General Purpose Input/Output	B21	IO	OV_{DD}	---
GPIO2_18/**IFC_CLK1**	General Purpose Input/Output	C21	IO	OV_{DD}	---
GPIO2_19/**IFC_NDWE_B**	General Purpose Input/Output	A10	IO	OV_{DD}	---
GPIO3_02/**IFC_CS4_B**	General Purpose Input/Output	D18	IO	OV_{DD}	---
GPIO3_03/**IFC_CS5_B**	General Purpose Input/Output	E18	IO	OV_{DD}	---
GPIO3_04/**IFC_CS6_B**	General Purpose Input/Output	D19	IO	OV_{DD}	---
GPIO3_05/**IFC_CS7_B**	General Purpose Input/Output	E19	IO	OV_{DD}	---
GPIO3_06/**UART2_SOUT**	General Purpose Input/Output	L3	IO	OV_{DD}	---
GPIO3_07/**UART2_SIN**	General Purpose Input/Output	K4	IO	OV_{DD}	---
GPIO3_08/**UART1_RTS_B**/ UART3_SOUT	General Purpose Input/Output	G3	IO	OV_{DD}	---
GPIO3_09/**UART2_RTS_B**/ UART4_SOUT	General Purpose Input/Output	J3	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_10/**UART1_CTS_B**/ UART3_SIN	General Purpose Input/Output	G4	IO	OV_{DD}	---
GPIO3_11/**UART2_CTS_B**/ UART4_SIN	General Purpose Input/Output	K3	IO	OV_{DD}	---
GPIO3_12/**IIC2_SCL**/ SDHC_CD_B	General Purpose Input/Output	H8	IO	OV_{DD}	---
GPIO3_13/**IIC2_SDA**/ SDHC_WP	General Purpose Input/Output	J8	IO	OV_{DD}	---
GPIO3_14/**SPI_SOUT**	General Purpose Input/Output	A8	IO	OV_{DD}	---
GPIO3_15/**SPI_SIN**	General Purpose Input/Output	A9	IO	OV_{DD}	---
GPIO3_16/**SPI_SCK**	General Purpose Input/Output	A7	IO	OV_{DD}	---
GPIO3_17/**SPI_PCS0**/ SDHC_DAT4/SDHC_VS	General Purpose Input/Output	B7	IO	OV_{DD}	---
GPIO3_18/**SPI_PCS1**/ SDHC_DAT5/ SDHC_CMD_DIR	General Purpose Input/Output	C7	IO	OV_{DD}	---
GPIO3_19/**SPI_PCS2**/ SDHC_DAT6/ SDHC_DAT0_DIR	General Purpose Input/Output	B9	IO	OV_{DD}	---
GPIO3_20/**SPI_PCS3**/ SDHC_DAT7/ SDHC_DAT123_DIR	General Purpose Input/Output	C9	IO	OV_{DD}	---
GPIO3_21/**SDHC_CMD**	General Purpose Input/Output	D7	IO	OV_{DD}	---
GPIO3_22/**SDHC_DAT0**	General Purpose Input/Output	E7	IO	OV_{DD}	---
GPIO3_23/**SDHC_DAT1**	General Purpose Input/Output	E8	IO	OV_{DD}	---
GPIO3_24/**SDHC_DAT2**	General Purpose Input/Output	D9	IO	OV_{DD}	---
GPIO3_25/**SDHC_DAT3**	General Purpose Input/Output	E9	IO	OV_{DD}	---
GPIO3_26/**SDHC_CLK**	General Purpose Input/Output	C8	IO	OV_{DD}	---
GPIO3_27/**IRQ03**	General Purpose Input/Output	F17	IO	OV_{DD}	---
GPIO3_28/**IRQ04**	General Purpose Input/Output	F18	IO	OV_{DD}	---
GPIO3_29/**IRQ05**	General Purpose Input/Output	F20	IO	OV_{DD}	---
GPIO3_30/**RTC**	General Purpose Input/Output	G19	IO	OV_{DD}	---
GPIO4_00/**IIC3_SCL**/EVT5_B/ SPI_PCS4	General Purpose Input/Output	K5	IO	OV_{DD}	---
GPIO4_01/**IIC3_SDA**/EVT6_B/ SPI_PCS5	General Purpose Input/Output	L5	IO	OV_{DD}	---
GPIO4_02/**IIC4_SCL**/EVT7_B	General Purpose Input/Output	K7	IO	OV_{DD}	---
GPIO4_03/**IIC4_SDA**/EVT8_B	General Purpose Input/Output	L7	IO	OV_{DD}	---
GPIO4_04/**IRQ06**	General Purpose Input/Output	G5	IO	OV_{DD}	---
GPIO4_05/**IRQ07**	General Purpose Input/Output	G7	IO	OV_{DD}	---
GPIO4_06/**IRQ08**	General Purpose Input/Output	J5	IO	OV_{DD}	---
GPIO4_07/**IRQ09**	General Purpose Input/Output	J7	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO4_08/**IRQ10**	General Purpose Input/Output	F8	IO	OV_{DD}	---
GPIO4_09/**IRQ11**	General Purpose Input/Output	K6	IO	OV_{DD}	---
GPIO4_10/**EVT9_B**	General Purpose Input/Output	G12	IO	OV_{DD}	---
GPIO4_16/ **TSEC_1588_CLK_IN**	General Purpose Input/Output	G2	IO	OV_{DD}	---
GPIO4_17/ **TSEC_1588_TRIG_IN1**	General Purpose Input/Output	L1	IO	OV_{DD}	---
GPIO4_18/ **TSEC_1588_TRIG_IN2**	General Purpose Input/Output	J2	IO	OV_{DD}	---
GPIO4_19/ **TSEC_1588_ALARM_OUT1**	General Purpose Input/Output	J1	IO	OV_{DD}	---
GPIO4_20/ **TSEC_1588_ALARM_OUT2**	General Purpose Input/Output	G1	IO	OV_{DD}	---
GPIO4_21/ **TSEC_1588_CLK_OUT**	General Purpose Input/Output	H1	IO	OV_{DD}	---
GPIO4_22/ **TSEC_1588_PULSE_OUT1**	General Purpose Input/Output	K1	IO	OV_{DD}	---
GPIO4_23/ **TSEC_1588_PULSE_OUT2**	General Purpose Input/Output	K2	IO	OV_{DD}	---
GPIO4_24/**USB1_DRVVBUS**	General Purpose Input/Output	F6	IO	OV_{DD}	---
GPIO4_25/**USB1_PWRFAULT**	General Purpose Input/Output	F3	IO	OV_{DD}	---
GPIO4_26/**USB2_DRVVBUS**	General Purpose Input/Output	F9	IO	OV_{DD}	---
GPIO4_27/**USB2_PWRFAULT**	General Purpose Input/Output	C6	IO	OV_{DD}	---
Quad SPI					
QSPI_A_CS0/**IFC_A00**/ GPIO1_16	Channel A Chip Select 0	E16	O	OV_{DD}	1, 5
QSPI_A_CS1/**IFC_A01**/ GPIO1_17	Channel A Chip Select 1	D16	O	OV_{DD}	1, 5
QSPI_A_DATA0/**IFC_A06**/ GPIO2_00/IFC_WP1_B	Channel A Data I/O 0	D13	IO	OV_{DD}	---
QSPI_A_DATA1/**IFC_A07**/ GPIO2_01/IFC_WP2_B	Channel A Data I/O 1	E12	IO	OV_{DD}	---
QSPI_A_DATA2/**IFC_A08**/ GPIO2_02/IFC_WP3_B	Channel A Data I/O 2	D12	IO	OV_{DD}	---
QSPI_A_DATA3/**IFC_A09**/ GPIO2_03/IFC_RB2_B	Channel A Data I/O 3	E11	IO	OV_{DD}	---
QSPI_A_DATA4/**IFC_PAR0**/ GPIO2_06/QSPI_B_DATA0	Channel A Data I/O 4	E20	IO	OV_{DD}	---
QSPI_A_DATA5/**IFC_PAR1**/ GPIO2_07/QSPI_B_DATA1	Channel A Data I/O 5	E21	IO	OV_{DD}	---
QSPI_A_DATA6/ **IFC_PERR_B**/GPIO2_16/ QSPI_B_DATA2	Channel A Data I/O 6	D21	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
QSPI_A_DATA7/**IFC_CS3_B**/ GPIO2_11/QSPI_B_DATA3	Channel A Data I/O 7	E17	IO	OV_{DD}	---
QSPI_A_DQS/**IFC_A10**/ GPIO2_04/IFC_RB3_B	Channel A Data Strobe	E10	I	OV_{DD}	1
QSPI_A_SCK/**IFC_A02**/ GPIO1_18	Channel A Clock	E15	O	OV_{DD}	1, 5
QSPI_B_CS0/**IFC_A03**/ GPIO1_19	Channel B Chip Select 0	D15	O	OV_{DD}	1, 5
QSPI_B_CS1/**IFC_A04**/ GPIO1_20	Channel B Chip Select 1	E14	O	OV_{DD}	1, 5
QSPI_B_DATA0/**IFC_PAR0**/ GPIO2_06/QSPI_A_DATA4	Channel B DATA I/O 0	E20	IO	OV_{DD}	---
QSPI_B_DATA1/**IFC_PAR1**/ GPIO2_07/QSPI_A_DATA5	Channel B DATA I/O 1	E21	IO	OV_{DD}	---
QSPI_B_DATA2/ **IFC_PERR_B**/GPIO2_16/ QSPI_A_DATA6	Channel B DATA I/O 2	D21	IO	OV_{DD}	---
QSPI_B_DATA3/**IFC_CS3_B**/ GPIO2_11/QSPI_A_DATA7	Channel B DATA I/O 3	E17	IO	OV_{DD}	---
QSPI_B_DQS/**IFC_A11**/ GPIO2_05/IFC_RB4_B	Channel B Data Strobe	D10	I	OV_{DD}	1
QSPI_B_SCK/**IFC_A05**/ GPIO1_21	Channel B Clock	E13	O	OV_{DD}	1, 5, 5
Power-On Reset Configuration					
cfg_eng_use0/**IFC_WE0_B**/ GPIO1_22	Power-on reset configuration	C17	I	OV_{DD}	1, 28
cfg_gpinput00/**IFC_AD00**/ GPIO1_00	Power-on reset configuration	B10	I	OV_{DD}	1
cfg_gpinput01/**IFC_AD01**/ GPIO1_01	Power-on reset configuration	C10	I	OV_{DD}	1
cfg_gpinput02/**IFC_AD02**/ GPIO1_02	Power-on reset configuration	A11	I	OV_{DD}	1
cfg_gpinput03/**IFC_AD03**/ GPIO1_03	Power-on reset configuration	C11	I	OV_{DD}	1
cfg_gpinput04/**IFC_AD04**/ GPIO1_04	Power-on reset configuration	A12	I	OV_{DD}	1
cfg_gpinput05/**IFC_AD05**/ GPIO1_05	Power-on reset configuration	B12	I	OV_{DD}	1
cfg_gpinput06/**IFC_AD06**/ GPIO1_06	Power-on reset configuration	C12	I	OV_{DD}	1
cfg_gpinput07/**IFC_AD07**/ GPIO1_07	Power-on reset configuration	A13	I	OV_{DD}	1
cfg_ifc_te/**IFC_TE**/GPIO1_23	Power-on reset configuration	B16	I	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
cfg_rcw_src01/**IFC_AD08**/ GPIO1_08	Power-on reset configuration	B13	I	OV_{DD}	1
cfg_rcw_src02/**IFC_AD09**/ GPIO1_09	Power-on reset configuration	C13	I	OV_{DD}	1
cfg_rcw_src03/**IFC_AD10**/ GPIO1_10	Power-on reset configuration	A14	I	OV_{DD}	1
cfg_rcw_src04/**IFC_AD11**/ GPIO1_11	Power-on reset configuration	C14	I	OV_{DD}	1
cfg_rcw_src05/**IFC_AD12**/ GPIO1_12	Power-on reset configuration	A15	I	OV_{DD}	1
cfg_rcw_src06/**IFC_AD13**/ GPIO1_13	Power-on reset configuration	B15	I	OV_{DD}	1
cfg_rcw_src07/**IFC_AD14**/ GPIO1_14	Power-on reset configuration	C15	I	OV_{DD}	1
cfg_rcw_src08/**IFC_AD15**/ GPIO1_15	Power-on reset configuration	A16	I	OV_{DD}	1
Power and Ground Signals					
GND001	GND	A2	---	---	---
GND002	GND	A4	---	---	---
GND003	GND	A6	---	---	---
GND004	GND	A22	---	---	---
GND005	GND	B1	---	---	---
GND006	GND	B2	---	---	---
GND007	GND	B4	---	---	---
GND008	GND	B6	---	---	---
GND009	GND	B8	---	---	---
GND010	GND	B11	---	---	---
GND011	GND	B14	---	---	---
GND012	GND	B17	---	---	---
GND013	GND	B20	---	---	---
GND014	GND	B22	---	---	---
GND015	GND	C3	---	---	---
GND016	GND	C4	---	---	---
GND017	GND	C5	---	---	---
GND018	GND	C22	---	---	---
GND019	GND	C24	---	---	---
GND020	GND	C26	---	---	---
GND021	GND	C28	---	---	---
GND022	GND	C30	---	---	---
GND023	GND	C32	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND024	GND	D1	---	---	---
GND025	GND	D2	---	---	---
GND026	GND	D3	---	---	---
GND027	GND	D6	---	---	---
GND028	GND	D8	---	---	---
GND029	GND	D11	---	---	---
GND030	GND	D14	---	---	---
GND031	GND	D17	---	---	---
GND032	GND	D20	---	---	---
GND033	GND	D22	---	---	---
GND034	GND	E3	---	---	---
GND035	GND	E6	---	---	---
GND036	GND	E22	---	---	---
GND037	GND	E26	---	---	---
GND038	GND	E28	---	---	---
GND039	GND	E30	---	---	---
GND040	GND	E32	---	---	---
GND041	GND	F1	---	---	---
GND042	GND	F2	---	---	---
GND043	GND	F4	---	---	---
GND044	GND	F5	---	---	---
GND045	GND	F10	---	---	---
GND046	GND	F13	---	---	---
GND047	GND	F16	---	---	---
GND048	GND	F19	---	---	---
GND049	GND	F22	---	---	---
GND050	GND	F24	---	---	---
GND051	GND	F33	---	---	---
GND052	GND	G8	---	---	---
GND053	GND	G22	---	---	---
GND054	GND	G26	---	---	---
GND055	GND	G29	---	---	---
GND056	GND	G31	---	---	---
GND057	GND	G34	---	---	---
GND058	GND	H2	---	---	---
GND059	GND	H4	---	---	---
GND060	GND	H6	---	---	---
GND061	GND	H19	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND062	GND	H22	---	---	---
GND063	GND	H24	---	---	---
GND064	GND	H28	---	---	---
GND065	GND	H32	---	---	---
GND066	GND	J9	---	---	---
GND067	GND	J12	---	---	---
GND068	GND	J13	---	---	---
GND069	GND	J15	---	---	---
GND070	GND	J17	---	---	---
GND071	GND	J22	---	---	---
GND072	GND	J26	---	---	---
GND073	GND	J30	---	---	---
GND074	GND	J34	---	---	---
GND075	GND	K10	---	---	---
GND076	GND	K11	---	---	---
GND077	GND	K12	---	---	---
GND078	GND	K14	---	---	---
GND079	GND	K15	---	---	---
GND080	GND	K16	---	---	---
GND081	GND	K22	---	---	---
GND082	GND	K24	---	---	---
GND083	GND	K32	---	---	---
GND084	GND	L2	---	---	---
GND085	GND	L4	---	---	---
GND086	GND	L6	---	---	---
GND087	GND	L18	---	---	---
GND088	GND	L19	---	---	---
GND089	GND	L20	---	---	---
GND090	GND	L21	---	---	---
GND091	GND	L22	---	---	---
GND092	GND	L27	---	---	---
GND093	GND	L28	---	---	---
GND094	GND	L30	---	---	---
GND095	GND	L34	---	---	---
GND096	GND	M9	---	---	---
GND097	GND	M14	---	---	---
GND098	GND	M16	---	---	---
GND099	GND	M18	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND100	GND	M25	---	---	---
GND101	GND	M28	---	---	---
GND102	GND	M32	---	---	---
GND103	GND	N11	---	---	---
GND104	GND	N13	---	---	---
GND105	GND	N15	---	---	---
GND106	GND	N17	---	---	---
GND107	GND	N19	---	---	---
GND108	GND	N21	---	---	---
GND109	GND	N23	---	---	---
GND110	GND	N28	---	---	---
GND111	GND	N30	---	---	---
GND112	GND	N34	---	---	---
GND113	GND	P10	---	---	---
GND114	GND	P12	---	---	---
GND115	GND	P14	---	---	---
GND116	GND	P16	---	---	---
GND117	GND	P18	---	---	---
GND118	GND	P20	---	---	---
GND119	GND	P22	---	---	---
GND120	GND	P24	---	---	---
GND121	GND	P26	---	---	---
GND122	GND	P28	---	---	---
GND123	GND	P32	---	---	---
GND124	GND	R11	---	---	---
GND125	GND	R13	---	---	---
GND126	GND	R15	---	---	---
GND127	GND	R17	---	---	---
GND128	GND	R19	---	---	---
GND129	GND	R21	---	---	---
GND130	GND	R23	---	---	---
GND131	GND	R25	---	---	---
GND132	GND	R28	---	---	---
GND133	GND	R30	---	---	---
GND134	GND	R34	---	---	---
GND135	GND	T9	---	---	---
GND136	GND	T12	---	---	---
GND137	GND	T14	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND138	GND	T16	---	---	---
GND139	GND	T18	---	---	---
GND140	GND	T20	---	---	---
GND141	GND	T22	---	---	---
GND142	GND	T24	---	---	---
GND143	GND	T28	---	---	---
GND144	GND	T32	---	---	---
GND145	GND	U2	---	---	---
GND146	GND	U4	---	---	---
GND147	GND	U9	---	---	---
GND148	GND	U11	---	---	---
GND149	GND	U13	---	---	---
GND150	GND	U15	---	---	---
GND151	GND	U17	---	---	---
GND152	GND	U19	---	---	---
GND153	GND	U21	---	---	---
GND154	GND	U23	---	---	---
GND155	GND	U25	---	---	---
GND156	GND	U26	---	---	---
GND157	GND	U28	---	---	---
GND158	GND	U30	---	---	---
GND159	GND	U34	---	---	---
GND160	GND	V6	---	---	---
GND161	GND	V9	---	---	---
GND162	GND	V12	---	---	---
GND163	GND	V14	---	---	---
GND164	GND	V16	---	---	---
GND165	GND	V18	---	---	---
GND166	GND	V20	---	---	---
GND167	GND	V22	---	---	---
GND168	GND	V24	---	---	---
GND169	GND	V28	---	---	---
GND170	GND	V32	---	---	---
GND171	GND	W2	---	---	---
GND172	GND	W4	---	---	---
GND173	GND	W9	---	---	---
GND174	GND	W11	---	---	---
GND175	GND	W13	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND176	GND	W15	---	---	---
GND177	GND	W17	---	---	---
GND178	GND	W19	---	---	---
GND179	GND	W21	---	---	---
GND180	GND	W23	---	---	---
GND181	GND	W25	---	---	---
GND182	GND	W28	---	---	---
GND183	GND	W32	---	---	---
GND184	GND	Y6	---	---	---
GND185	GND	Y9	---	---	---
GND186	GND	Y12	---	---	---
GND187	GND	Y14	---	---	---
GND188	GND	Y16	---	---	---
GND189	GND	Y18	---	---	---
GND190	GND	Y20	---	---	---
GND191	GND	Y22	---	---	---
GND192	GND	Y24	---	---	---
GND193	GND	Y26	---	---	---
GND194	GND	Y28	---	---	---
GND195	GND	Y30	---	---	---
GND196	GND	Y34	---	---	---
GND197	GND	AA2	---	---	---
GND198	GND	AA4	---	---	---
GND199	GND	AA8	---	---	---
GND200	GND	AA11	---	---	---
GND201	GND	AA13	---	---	---
GND202	GND	AA15	---	---	---
GND203	GND	AA17	---	---	---
GND204	GND	AA19	---	---	---
GND205	GND	AA21	---	---	---
GND206	GND	AA23	---	---	---
GND207	GND	AA25	---	---	---
GND208	GND	AA28	---	---	---
GND209	GND	AA32	---	---	---
GND210	GND	AB6	---	---	---
GND211	GND	AB9	---	---	---
GND212	GND	AB10	---	---	---
GND213	GND	AB12	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND214	GND	AB14	---	---	---
GND215	GND	AB16	---	---	---
GND216	GND	AB18	---	---	---
GND217	GND	AB20	---	---	---
GND218	GND	AB22	---	---	---
GND219	GND	AB24	---	---	---
GND220	GND	AB28	---	---	---
GND221	GND	AB30	---	---	---
GND222	GND	AB34	---	---	---
GND223	GND	AC2	---	---	---
GND224	GND	AC4	---	---	---
GND225	GND	AC8	---	---	---
GND226	GND	AC11	---	---	---
GND227	GND	AC13	---	---	---
GND228	GND	AC15	---	---	---
GND229	GND	AC17	---	---	---
GND230	GND	AC19	---	---	---
GND231	GND	AC21	---	---	---
GND232	GND	AC23	---	---	---
GND233	GND	AC25	---	---	---
GND234	GND	AC26	---	---	---
GND235	GND	AC28	---	---	---
GND236	GND	AC32	---	---	---
GND237	GND	AD6	---	---	---
GND238	GND	AD10	---	---	---
GND239	GND	AD12	---	---	---
GND240	GND	AD14	---	---	---
GND241	GND	AD16	---	---	---
GND242	GND	AD18	---	---	---
GND243	GND	AD20	---	---	---
GND244	GND	AD22	---	---	---
GND245	GND	AD24	---	---	---
GND246	GND	AD26	---	---	---
GND247	GND	AD28	---	---	---
GND248	GND	AD30	---	---	---
GND249	GND	AD34	---	---	---
GND250	GND	AE2	---	---	---
GND251	GND	AE4	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND252	GND	AE8	---	---	---
GND253	GND	AE21	---	---	---
GND254	GND	AE23	---	---	---
GND255	GND	AE25	---	---	---
GND256	GND	AE28	---	---	---
GND257	GND	AE32	---	---	---
GND258	GND	AF6	---	---	---
GND259	GND	AF22	---	---	---
GND260	GND	AF27	---	---	---
GND261	GND	AF28	---	---	---
GND262	GND	AF30	---	---	---
GND263	GND	AF34	---	---	---
GND264	GND	AG24	---	---	---
GND265	GND	AG32	---	---	---
GND266	GND	AH22	---	---	---
GND267	GND	AH26	---	---	---
GND268	GND	AH30	---	---	---
GND269	GND	AH34	---	---	---
GND270	GND	AJ22	---	---	---
GND271	GND	AJ24	---	---	---
GND272	GND	AJ28	---	---	---
GND273	GND	AJ32	---	---	---
GND274	GND	AK22	---	---	---
GND275	GND	AK26	---	---	---
GND276	GND	AK29	---	---	---
GND277	GND	AK31	---	---	---
GND278	GND	AK34	---	---	---
GND279	GND	AL24	---	---	---
GND280	GND	AL33	---	---	---
GND281	GND	AM22	---	---	---
GND282	GND	AM26	---	---	---
GND283	GND	AM28	---	---	---
GND284	GND	AM30	---	---	---
GND285	GND	AM32	---	---	---
GND286	GND	AN22	---	---	---
GND287	GND	AP22	---	---	---
GND288	GND	AP24	---	---	---
GND289	GND	AP26	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND290	GND	AP28	---	---	---
GND291	GND	AP30	---	---	---
GND292	GND	AP32	---	---	---
GND293	GND	AT22	---	---	---
SD_GND001	Serdes GND	AE9	---	---	---
SD_GND002	Serdes GND	AF7	---	---	---
SD_GND003	Serdes GND	AF10	---	---	---
SD_GND004	Serdes GND	AF11	---	---	---
SD_GND005	Serdes GND	AF12	---	---	---
SD_GND006	Serdes GND	AF13	---	---	---
SD_GND007	Serdes GND	AF14	---	---	---
SD_GND008	Serdes GND	AF15	---	---	---
SD_GND009	Serdes GND	AF16	---	---	---
SD_GND010	Serdes GND	AF17	---	---	---
SD_GND011	Serdes GND	AF18	---	---	---
SD_GND012	Serdes GND	AG1	---	---	---
SD_GND013	Serdes GND	AG2	---	---	---
SD_GND014	Serdes GND	AG3	---	---	---
SD_GND015	Serdes GND	AG4	---	---	---
SD_GND016	Serdes GND	AG5	---	---	---
SD_GND017	Serdes GND	AG6	---	---	---
SD_GND018	Serdes GND	AG9	---	---	---
SD_GND019	Serdes GND	AG20	---	---	---
SD_GND020	Serdes GND	AH1	---	---	---
SD_GND021	Serdes GND	AH3	---	---	---
SD_GND022	Serdes GND	AH5	---	---	---
SD_GND023	Serdes GND	AH7	---	---	---
SD_GND024	Serdes GND	AH10	---	---	---
SD_GND025	Serdes GND	AH12	---	---	---
SD_GND026	Serdes GND	AH14	---	---	---
SD_GND027	Serdes GND	AH16	---	---	---
SD_GND028	Serdes GND	AH18	---	---	---
SD_GND029	Serdes GND	AH20	---	---	---
SD_GND030	Serdes GND	AJ1	---	---	---
SD_GND031	Serdes GND	AJ3	---	---	---
SD_GND032	Serdes GND	AJ5	---	---	---
SD_GND033	Serdes GND	AJ7	---	---	---
SD_GND034	Serdes GND	AJ10	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND035	Serdes GND	AJ12	---	---	---
SD_GND036	Serdes GND	AJ14	---	---	---
SD_GND037	Serdes GND	AJ16	---	---	---
SD_GND038	Serdes GND	AJ18	---	---	---
SD_GND039	Serdes GND	AJ20	---	---	---
SD_GND040	Serdes GND	AK1	---	---	---
SD_GND041	Serdes GND	AK2	---	---	---
SD_GND042	Serdes GND	AK4	---	---	---
SD_GND043	Serdes GND	AK6	---	---	---
SD_GND044	Serdes GND	AK8	---	---	---
SD_GND045	Serdes GND	AK9	---	---	---
SD_GND046	Serdes GND	AK11	---	---	---
SD_GND047	Serdes GND	AK13	---	---	---
SD_GND048	Serdes GND	AK15	---	---	---
SD_GND049	Serdes GND	AK17	---	---	---
SD_GND050	Serdes GND	AK19	---	---	---
SD_GND051	Serdes GND	AK21	---	---	---
SD_GND052	Serdes GND	AL2	---	---	---
SD_GND053	Serdes GND	AL4	---	---	---
SD_GND054	Serdes GND	AL6	---	---	---
SD_GND055	Serdes GND	AL8	---	---	---
SD_GND056	Serdes GND	AL9	---	---	---
SD_GND057	Serdes GND	AL11	---	---	---
SD_GND058	Serdes GND	AL13	---	---	---
SD_GND059	Serdes GND	AL15	---	---	---
SD_GND060	Serdes GND	AL17	---	---	---
SD_GND061	Serdes GND	AL19	---	---	---
SD_GND062	Serdes GND	AL21	---	---	---
SD_GND063	Serdes GND	AM2	---	---	---
SD_GND064	Serdes GND	AM3	---	---	---
SD_GND065	Serdes GND	AM4	---	---	---
SD_GND066	Serdes GND	AM5	---	---	---
SD_GND067	Serdes GND	AM6	---	---	---
SD_GND068	Serdes GND	AM7	---	---	---
SD_GND069	Serdes GND	AM10	---	---	---
SD_GND070	Serdes GND	AM11	---	---	---
SD_GND071	Serdes GND	AM12	---	---	---
SD_GND072	Serdes GND	AM13	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND073	Serdes GND	AM15	---	---	---
SD_GND074	Serdes GND	AM16	---	---	---
SD_GND075	Serdes GND	AM17	---	---	---
SD_GND076	Serdes GND	AM18	---	---	---
SD_GND077	Serdes GND	AM19	---	---	---
SD_GND078	Serdes GND	AM20	---	---	---
SD_GND079	Serdes GND	AN1	---	---	---
SD_GND080	Serdes GND	AN3	---	---	---
SD_GND081	Serdes GND	AN5	---	---	---
SD_GND082	Serdes GND	AN7	---	---	---
SD_GND083	Serdes GND	AN10	---	---	---
SD_GND084	Serdes GND	AN12	---	---	---
SD_GND085	Serdes GND	AN14	---	---	---
SD_GND086	Serdes GND	AN16	---	---	---
SD_GND087	Serdes GND	AN18	---	---	---
SD_GND088	Serdes GND	AN20	---	---	---
SD_GND089	Serdes GND	AP1	---	---	---
SD_GND090	Serdes GND	AP3	---	---	---
SD_GND091	Serdes GND	AP5	---	---	---
SD_GND092	Serdes GND	AP7	---	---	---
SD_GND093	Serdes GND	AP10	---	---	---
SD_GND094	Serdes GND	AP12	---	---	---
SD_GND095	Serdes GND	AP14	---	---	---
SD_GND096	Serdes GND	AP16	---	---	---
SD_GND097	Serdes GND	AP18	---	---	---
SD_GND098	Serdes GND	AP20	---	---	---
SD_GND099	Serdes GND	AR1	---	---	---
SD_GND100	Serdes GND	AR2	---	---	---
SD_GND101	Serdes GND	AR4	---	---	---
SD_GND102	Serdes GND	AR6	---	---	---
SD_GND103	Serdes GND	AR8	---	---	---
SD_GND104	Serdes GND	AR9	---	---	---
SD_GND105	Serdes GND	AR11	---	---	---
SD_GND106	Serdes GND	AR13	---	---	---
SD_GND107	Serdes GND	AR15	---	---	---
SD_GND108	Serdes GND	AR17	---	---	---
SD_GND109	Serdes GND	AR19	---	---	---
SD_GND110	Serdes GND	AR21	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND111	Serdes GND	AT2	---	---	---
SD_GND112	Serdes GND	AT4	---	---	---
SD_GND113	Serdes GND	AT6	---	---	---
SD_GND114	Serdes GND	AT8	---	---	---
SD_GND115	Serdes GND	AT9	---	---	---
SD_GND116	Serdes GND	AT11	---	---	---
SD_GND117	Serdes GND	AT13	---	---	---
SD_GND118	Serdes GND	AT15	---	---	---
SD_GND119	Serdes GND	AT17	---	---	---
SD_GND120	Serdes GND	AT19	---	---	---
SD_GND121	Serdes GND	AT21	---	---	---
SENSEGND_CA	GND Sense pin	K17	---	---	---
SENSEGND_CB	GND Sense pin	AE20	---	---	---
SENSEGND_PL	GND Sense pin	K13	---	---	---
OVDD01	General I/O supply	M19	---	OV_{DD}	---
OVDD02	General I/O supply	M20	---	OV_{DD}	---
OVDD03	General I/O supply	M21	---	OV_{DD}	---
OVDD04	General I/O supply	M22	---	OV_{DD}	---
OVDD05	General I/O supply	M23	---	OV_{DD}	---
OVDD06	General I/O supply	M24	---	OV_{DD}	---
OVDD07	General I/O supply	N9	---	OV_{DD}	---
OVDD08	General I/O supply	V26	---	OV_{DD}	---
OVDD09	General I/O supply	W26	---	OV_{DD}	---
OVDD10	General I/O supply	AE26	---	OV_{DD}	---
G1VDD01	DDR supply for port 1	A35	---	$G1V_{DD}$	---
G1VDD02	DDR supply for port 1	B23	---	$G1V_{DD}$	---
G1VDD03	DDR supply for port 1	B25	---	$G1V_{DD}$	---
G1VDD04	DDR supply for port 1	B27	---	$G1V_{DD}$	---
G1VDD05	DDR supply for port 1	B29	---	$G1V_{DD}$	---
G1VDD06	DDR supply for port 1	B31	---	$G1V_{DD}$	---
G1VDD07	DDR supply for port 1	B33	---	$G1V_{DD}$	---
G1VDD08	DDR supply for port 1	B36	---	$G1V_{DD}$	---
G1VDD09	DDR supply for port 1	D33	---	$G1V_{DD}$	---
G1VDD10	DDR supply for port 1	E34	---	$G1V_{DD}$	---
G1VDD11	DDR supply for port 1	F35	---	$G1V_{DD}$	---
G1VDD12	DDR supply for port 1	H35	---	$G1V_{DD}$	---
G1VDD13	DDR supply for port 1	K35	---	$G1V_{DD}$	---
G1VDD14	DDR supply for port 1	M27	---	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD15	DDR supply for port 1	M35	---	$G1V_{DD}$	---
G1VDD16	DDR supply for port 1	N27	---	$G1V_{DD}$	---
G1VDD17	DDR supply for port 1	P27	---	$G1V_{DD}$	---
G1VDD18	DDR supply for port 1	P35	---	$G1V_{DD}$	---
G1VDD19	DDR supply for port 1	R27	---	$G1V_{DD}$	---
G1VDD20	DDR supply for port 1	T27	---	$G1V_{DD}$	---
G1VDD21	DDR supply for port 1	T35	---	$G1V_{DD}$	---
G1VDD22	DDR supply for port 1	U27	---	$G1V_{DD}$	---
G1VDD23	DDR supply for port 1	V27	---	$G1V_{DD}$	---
G1VDD24	DDR supply for port 1	V35	---	$G1V_{DD}$	---
G2VDD01	DDR supply for port 2	W27	---	$G2V_{DD}$	---
G2VDD02	DDR supply for port 2	W35	---	$G2V_{DD}$	---
G2VDD03	DDR supply for port 2	Y27	---	$G2V_{DD}$	---
G2VDD04	DDR supply for port 2	AA27	---	$G2V_{DD}$	---
G2VDD05	DDR supply for port 2	AA35	---	$G2V_{DD}$	---
G2VDD06	DDR supply for port 2	AB27	---	$G2V_{DD}$	---
G2VDD07	DDR supply for port 2	AC27	---	$G2V_{DD}$	---
G2VDD08	DDR supply for port 2	AC35	---	$G2V_{DD}$	---
G2VDD09	DDR supply for port 2	AD27	---	$G2V_{DD}$	---
G2VDD10	DDR supply for port 2	AE27	---	$G2V_{DD}$	---
G2VDD11	DDR supply for port 2	AE35	---	$G2V_{DD}$	---
G2VDD12	DDR supply for port 2	AG35	---	$G2V_{DD}$	---
G2VDD13	DDR supply for port 2	AJ35	---	$G2V_{DD}$	---
G2VDD14	DDR supply for port 2	AL35	---	$G2V_{DD}$	---
G2VDD15	DDR supply for port 2	AM34	---	$G2V_{DD}$	---
G2VDD16	DDR supply for port 2	AN33	---	$G2V_{DD}$	---
G2VDD17	DDR supply for port 2	AR23	---	$G2V_{DD}$	---
G2VDD18	DDR supply for port 2	AR25	---	$G2V_{DD}$	---
G2VDD19	DDR supply for port 2	AR27	---	$G2V_{DD}$	---
G2VDD20	DDR supply for port 2	AR29	---	$G2V_{DD}$	---
G2VDD21	DDR supply for port 2	AR31	---	$G2V_{DD}$	---
G2VDD22	DDR supply for port 2	AR33	---	$G2V_{DD}$	---
G2VDD23	DDR supply for port 2	AR36	---	$G2V_{DD}$	---
G2VDD24	DDR supply for port 2	AT35	---	$G2V_{DD}$	---
G3VDD01	DDR supply for port 3	N1	---	$G3V_{DD}$	---
G3VDD02	DDR supply for port 3	N3	---	$G3V_{DD}$	---
G3VDD03	DDR supply for port 3	N5	---	$G3V_{DD}$	---
G3VDD04	DDR supply for port 3	N7	---	$G3V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G3VDD05	DDR supply for port 3	R9	---	$G3V_{DD}$	---
G3VDD06	DDR supply for port 3	T1	---	$G3V_{DD}$	---
G3VDD07	DDR supply for port 3	T3	---	$G3V_{DD}$	---
G3VDD08	DDR supply for port 3	T5	---	$G3V_{DD}$	---
G3VDD09	DDR supply for port 3	T6	---	$G3V_{DD}$	---
G3VDD10	DDR supply for port 3	T10	---	$G3V_{DD}$	---
G3VDD11	DDR supply for port 3	U7	---	$G3V_{DD}$	---
G3VDD12	DDR supply for port 3	U10	---	$G3V_{DD}$	---
G3VDD13	DDR supply for port 3	V10	---	$G3V_{DD}$	---
G3VDD14	DDR supply for port 3	W7	---	$G3V_{DD}$	---
G3VDD15	DDR supply for port 3	W10	---	$G3V_{DD}$	---
G3VDD16	DDR supply for port 3	Y8	---	$G3V_{DD}$	---
G3VDD17	DDR supply for port 3	Y10	---	$G3V_{DD}$	---
G3VDD18	DDR supply for port 3	AA7	---	$G3V_{DD}$	---
SVDD01	SerDes core logic supply	AE10	---	SV_{DD}	---
SVDD02	SerDes core logic supply	AE11	---	SV_{DD}	---
SVDD03	SerDes core logic supply	AE12	---	SV_{DD}	---
SVDD04	SerDes core logic supply	AE13	---	SV_{DD}	---
SVDD05	SerDes core logic supply	AE14	---	SV_{DD}	---
SVDD06	SerDes core logic supply	AE15	---	SV_{DD}	---
SVDD07	SerDes core logic supply	AE16	---	SV_{DD}	---
SVDD08	SerDes core logic supply	AE17	---	SV_{DD}	---
SVDD09	SerDes core logic supply	AE18	---	SV_{DD}	---
SVDD10	SerDes core logic supply	AN8	---	SV_{DD}	---
SVDD11	SerDes core logic supply	AN9	---	SV_{DD}	---
XVDD01	SerDes transceiver supply	AF8	---	XV_{DD}	---
XVDD02	SerDes transceiver supply	AG10	---	XV_{DD}	---
XVDD03	SerDes transceiver supply	AG11	---	XV_{DD}	---
XVDD04	SerDes transceiver supply	AG12	---	XV_{DD}	---
XVDD05	SerDes transceiver supply	AG13	---	XV_{DD}	---
XVDD06	SerDes transceiver supply	AG14	---	XV_{DD}	---
XVDD07	SerDes transceiver supply	AG15	---	XV_{DD}	---
XVDD08	SerDes transceiver supply	AG16	---	XV_{DD}	---
XVDD09	SerDes transceiver supply	AG17	---	XV_{DD}	---
XVDD10	SerDes transceiver supply	AG18	---	XV_{DD}	---
XVDD11	SerDes transceiver supply	AG19	---	XV_{DD}	---
FA_VL	Reserved	AG22	---	FA_VL	15
PROG_MTR	Reserved	M26	---	PROG_MTR	15

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TA_PROG_SFP	SFP Fuse Programming Override supply	N25	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	H13	---	TH_V_{DD}	---
VDD001	Supply for cores and platform	M13	---	V_{DD}	---
VDD002	Supply for cores and platform	M15	---	V_{DD}	---
VDD003	Supply for cores and platform	M17	---	V_{DD}	---
VDD004	Supply for cores and platform	N10	---	V_{DD}	---
VDD005	Supply for cores and platform	N12	---	V_{DD}	---
VDD006	Supply for cores and platform	N14	---	V_{DD}	---
VDD007	Supply for cores and platform	N16	---	V_{DD}	---
VDD008	Supply for cores and platform	N18	---	V_{DD}	---
VDD009	Supply for cores and platform	N20	---	V_{DD}	---
VDD010	Supply for cores and platform	N22	---	V_{DD}	---
VDD011	Supply for cores and platform	N24	---	V_{DD}	---
VDD012	Supply for cores and platform	N26	---	V_{DD}	---
VDD013	Supply for cores and platform	P11	---	V_{DD}	---
VDD014	Supply for cores and platform	P13	---	V_{DD}	---
VDD015	Supply for cores and platform	P15	---	V_{DD}	---
VDD016	Supply for cores and platform	P17	---	V_{DD}	---
VDD017	Supply for cores and platform	P19	---	V_{DD}	---
VDD018	Supply for cores and platform	P21	---	V_{DD}	---
VDD019	Supply for cores and platform	P23	---	V_{DD}	---
VDD020	Supply for cores and platform	P25	---	V_{DD}	---
VDD021	Supply for cores and platform	R10	---	V_{DD}	---
VDD022	Supply for cores and platform	R12	---	V_{DD}	---
VDD023	Supply for cores and platform	R14	---	V_{DD}	---
VDD024	Supply for cores and platform	R16	---	V_{DD}	---
VDD025	Supply for cores and platform	R18	---	V_{DD}	---
VDD026	Supply for cores and platform	R20	---	V_{DD}	---
VDD027	Supply for cores and platform	R22	---	V_{DD}	---
VDD028	Supply for cores and platform	R24	---	V_{DD}	---
VDD029	Supply for cores and platform	T11	---	V_{DD}	---
VDD030	Supply for cores and platform	T13	---	V_{DD}	---
VDD031	Supply for cores and platform	T15	---	V_{DD}	---
VDD032	Supply for cores and platform	T17	---	V_{DD}	---
VDD033	Supply for cores and platform	T19	---	V_{DD}	---
VDD034	Supply for cores and platform	T21	---	V_{DD}	---
VDD035	Supply for cores and platform	T23	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD036	Supply for cores and platform	T25	---	V_{DD}	---
VDD037	Supply for cores and platform	U12	---	V_{DD}	---
VDD038	Supply for cores and platform	U14	---	V_{DD}	---
VDD039	Supply for cores and platform	U16	---	V_{DD}	---
VDD040	Supply for cores and platform	U18	---	V_{DD}	---
VDD041	Supply for cores and platform	U20	---	V_{DD}	---
VDD042	Supply for cores and platform	U22	---	V_{DD}	---
VDD043	Supply for cores and platform	U24	---	V_{DD}	---
VDD044	Supply for cores and platform	V11	---	V_{DD}	---
VDD045	Supply for cores and platform	V13	---	V_{DD}	---
VDD046	Supply for cores and platform	V15	---	V_{DD}	---
VDD047	Supply for cores and platform	V17	---	V_{DD}	---
VDD048	Supply for cores and platform	V19	---	V_{DD}	---
VDD049	Supply for cores and platform	V21	---	V_{DD}	---
VDD050	Supply for cores and platform	V23	---	V_{DD}	---
VDD051	Supply for cores and platform	V25	---	V_{DD}	---
VDD052	Supply for cores and platform	W12	---	V_{DD}	---
VDD053	Supply for cores and platform	W14	---	V_{DD}	---
VDD054	Supply for cores and platform	W16	---	V_{DD}	---
VDD055	Supply for cores and platform	W18	---	V_{DD}	---
VDD056	Supply for cores and platform	W20	---	V_{DD}	---
VDD057	Supply for cores and platform	W22	---	V_{DD}	---
VDD058	Supply for cores and platform	W24	---	V_{DD}	---
VDD059	Supply for cores and platform	Y11	---	V_{DD}	---
VDD060	Supply for cores and platform	Y13	---	V_{DD}	---
VDD061	Supply for cores and platform	Y15	---	V_{DD}	---
VDD062	Supply for cores and platform	Y17	---	V_{DD}	---
VDD063	Supply for cores and platform	Y19	---	V_{DD}	---
VDD064	Supply for cores and platform	Y21	---	V_{DD}	---
VDD065	Supply for cores and platform	Y23	---	V_{DD}	---
VDD066	Supply for cores and platform	Y25	---	V_{DD}	---
VDD067	Supply for cores and platform	AA10	---	V_{DD}	---
VDD068	Supply for cores and platform	AA12	---	V_{DD}	---
VDD069	Supply for cores and platform	AA14	---	V_{DD}	---
VDD070	Supply for cores and platform	AA16	---	V_{DD}	---
VDD071	Supply for cores and platform	AA18	---	V_{DD}	---
VDD072	Supply for cores and platform	AA20	---	V_{DD}	---
VDD073	Supply for cores and platform	AA22	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD074	Supply for cores and platform	AA24	---	V_{DD}	---
VDD075	Supply for cores and platform	AB11	---	V_{DD}	---
VDD076	Supply for cores and platform	AB13	---	V_{DD}	---
VDD077	Supply for cores and platform	AB15	---	V_{DD}	---
VDD078	Supply for cores and platform	AB17	---	V_{DD}	---
VDD079	Supply for cores and platform	AB19	---	V_{DD}	---
VDD080	Supply for cores and platform	AB21	---	V_{DD}	---
VDD081	Supply for cores and platform	AB23	---	V_{DD}	---
VDD082	Supply for cores and platform	AB25	---	V_{DD}	---
VDD083	Supply for cores and platform	AC10	---	V_{DD}	---
VDD084	Supply for cores and platform	AC12	---	V_{DD}	---
VDD085	Supply for cores and platform	AC14	---	V_{DD}	---
VDD086	Supply for cores and platform	AC16	---	V_{DD}	---
VDD087	Supply for cores and platform	AC18	---	V_{DD}	---
VDD088	Supply for cores and platform	AC20	---	V_{DD}	---
VDD089	Supply for cores and platform	AC22	---	V_{DD}	---
VDD090	Supply for cores and platform	AC24	---	V_{DD}	---
VDD091	Supply for cores and platform	AD11	---	V_{DD}	---
VDD092	Supply for cores and platform	AD13	---	V_{DD}	---
VDD093	Supply for cores and platform	AD15	---	V_{DD}	---
VDD094	Supply for cores and platform	AD17	---	V_{DD}	---
VDD095	Supply for cores and platform	AD19	---	V_{DD}	---
VDD096	Supply for cores and platform	AD21	---	V_{DD}	---
VDD097	Supply for cores and platform	AD23	---	V_{DD}	---
VDD098	Supply for cores and platform	AD25	---	V_{DD}	---
VDD099	Supply for cores and platform	AE22	---	V_{DD}	---
VDD100	Supply for cores and platform	AE24	---	V_{DD}	---
TA_BB_VDD	Battery Backed Security Monitor supply	K18	---	TA_BB_V_{DD}	19
AVDD_PLAT	Platform PLL supply	L15	---	AVDD_PLAT	---
AVDD_D1	DDR1 PLL supply	R26	---	AVDD_D1	---
AVDD_D2	DDR2 PLL supply	AB26	---	AVDD_D2	---
AVDD_D3	DDR3 PLL supply	AA9	---	AVDD_D3	---
AVDD_SD1_PLL1	SerDes1 PLL 1 supply	AH9	---	AVDD_SD1_PLL1	---
AVDD_SD1_PLL2	SerDes1 PLL 2 supply	AH8	---	AVDD_SD1_PLL2	---
AVDD_SD2_PLL1	SerDes2 PLL 1 supply	AL14	---	AVDD_SD2_PLL1	---
AVDD_SD2_PLL2	SerDes2 PLL 2 supply	AF20	---	AVDD_SD2_PLL2	---
USB_HVDD1	USB PHY3.3V HS and SS Supply	L11	---	USB_HV_{DD}	20

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB_HVDD2	USB PHY3.3V HS and SS Supply	M11	---	USB_HV_{DD}	20
USB_SDVDD1	USB PHY Analog and Digital HS Supply	L12	---	USB_SDV_{DD}	20
USB_SDVDD2	USB PHY Analog and Digital HS Supply	M12	---	USB_SDV_{DD}	20
USB_SVDD1	USB PHY Analog and Digital SS Supply	L10	---	USB_SV_{DD}	20
USB_SVDD2	USB PHY Analog and Digital SS Supply	M10	---	USB_SV_{DD}	20
SENSEVDD_CA	VDD Sense pin	L17	---	SENSEVDD_CA	---
SENSEVDD_CB	VDD Sense pin	AE19	---	SENSEVDD_CB	---
SENSEVDD_PL	VDD Sense pin	L13	---	SENSEVDD_PL	---
AVDD_CGA1	A72 Core Cluster Group A PLL1 supply	J16	---	AVDD_CGA1	---
AVDD_CGA2	A72 Core Cluster Group A PLL2 supply	L16	---	AVDD_CGA2	---
AVDD_CGB1	A72 Core Cluster Group B PLL1 supply	J14	---	AVDD_CGB1	---
AVDD_CGB2	A72 Core Cluster Group B PLL2 supply	L14	---	AVDD_CGB2	---
No Connection Pins					
NC_G10	No Connection	G10	---	---	---
NC_G9	No Connection	G9	---	---	---
NC_W3	No Connection	W3	---	---	---

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

3. MDIC[0] is grounded through an 162 Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 162 Ω precision 1% resistor. For either full or half driver strength calibration of DDR I/Os, use the same MDIC resistor value of 162 Ω. Memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR4 I/Os. The MDIC[0:1] pins must be connected to 162 Ω precision 1% resistors.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (1 kΩ) to the respective power supply for normal operation.

11. This pin requires a 200 Ω pull-up to respective power-supply.

12. Do not connect. These pins should be left floating.

13. TBSCAN_EN_B is an IEEE 1149.1 JTAG Compliance Enable pin. 0: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL. 1: JTAG connects to DAP controller for the ARM core debug. In normal operation, this pin must be pulled high to OVDD with 4.7 Kohm.

14. For LS2088A, this pin must be pulled high through 1 to 10 kΩ resistor to OVDD. For LS2048A, this pin must be pulled low through 1 to 10 kΩ resistor to GND.

15. These pins must be tied to ground (GND).

16. This pin requires a 698 Ω pull-up to respective power supply.

17. These pins should be tied to ground if the diode is not used for temperature monitoring. For details, see the Connection Recommendations section.

18. When the Dn_MDQS_B[9:17] pins are not used, terminate the pin with 50 Ω to VTT or 100 Ω to GND. When using a discrete x8 or x16 DRAM, place the termination close to the device pin. When the signals are connected to a DIMM connector that is used only by DIMMs with an x8 or x16 DRAM, terminate the pin close to the DIMM connector.

19. This pin must be powered up all the time, even when the secure boot is not used, or the secure boot is used without the low power feature.

20. This pin supplies power to both the USB1 and USB2 controllers. If any of USB1 or USB2 is used, this pin must be powered.

24. Recommend that a weak pull-up resistor (10-100 kΩ) be placed on this pin to the respective power supply.

25. This pin must be tied to GND through a 200 Ω 1% precision resistor.

27. The permissible voltage range is 0-5.5 V.

28. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reach its operating condition.

29. When using discrete DRAM or RDIMM, the MALERT_B pin needs a 50 Ω to 100 Ω pull-up resistor to GVDD.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1]

Characteristic		Symbol	Min Value	Max Value	Unit	Notes
Core and platform supply voltage		V_{DD}	-0.3	1.1	V	2
PLL supply voltage (core, platform, DDR)		AV_{DD}_CGA1 AV_{DD}_CGA2 AV_{DD}_CGB1 AV_{DD}_CGB2 AV_{DD}_PLAT AV_{DD}_D1 AV_{DD}_D2 AV_{DD}_D3	-0.3	1.98	V	—
PLL supply voltage (SerDes, filtered from XV_{DD})		AV_{DD}_SD1_PLL1 AV_{DD}_SD1_PLL2 AV_{DD}_SD2_PLL1 AV_{DD}_SD2_PLL2	-0.3	1.48	V	—
Fuse programming override supply		TA_PROG_SFP	-0.3	1.98	V	—
Thermal monitor unit supply		TH_V_{DD}	-0.3	1.98	V	—
General I/O supply		OV_{DD}	-0.3	1.98	V	—
DDR4 DRAM I/O voltage		$G1V_{DD}$, $G2V_{DD}$, $G3V_{DD}$	-0.3	1.32	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		SV_{DD}	-0.3	1.1	V	—
Pad power supply for SerDes transmitters		XV_{DD}	-0.3	1.45	V	—
USB PHY 3.3 V HS(High Speed) and SS(Super Speed) supply voltage		USB_HV_{DD}	-0.3	3.63	V	—
USB PHY Analog and Digital HS supply voltage		USB_SDV_{DD}	-0.3	1.1	V	—
USB PHY Analog and Digital SS supply voltage		USB_SV_{DD}	-0.3	1.1	V	—
Battery Backed Security Monitor supply		TA_BB_V_{DD}	-0.3	1.1	V	—
Input voltage	DDR4 DRAM signal	MV_{IN}	-0.3	GV_{DD} + 0.3	V	3
	General I/O signals	OV_{IN}	-0.3	OV_{DD} + 0.3	V	4, 5
	SerDes signals	SV_{IN}	-0.4	SV_{DD} + 0.3	V	4
	USB PHY 3.3 HS signals	USB_HV_{IN}	-0.3	USB_HV_{DD} + 0.3	V	4
	USB PHY SS signals	USB_SV_{IN}	-0.3	USB_SV_{DD} + 0.3	V	4
Storage temperature range		T_{STG}	-55	150	°C	—

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

Table 2. Absolute maximum ratings[1]

Characteristic	Symbol	Min Value	Max Value	Unit	Notes
3. **Caution:** MV_{IN} must not exceed GnV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.					
4. SV_{IN}, USB_HV_{IN}, USB_SV_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.					
5. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.					

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Characteristic		Symbol	Recommended value	Unit	Notes
VID Core and platform supply voltage	At initial start-up	V_{DD}	1.05 ± 30 mV or VID ± 30 mV	V	1, 2, 3, 5, 6
	During normal operation		VID ± 30 mV	V	1, 2, 3, 5, 6
PLL supply voltage (core, platform, DDR)		AV_{DD}_CGA1 AV_{DD}_CGA2 AV_{DD}_CGB1 AV_{DD}_CGB2 AV_{DD}_PLAT AV_{DD}_D1 AV_{DD}_D2 AV_{DD}_D3	1.8 V ± 90 mV	V	—
PLL supply voltage (SerDes, filtered from XV_{DD})		$AV_{DD}_SD1_PLL1$ $AV_{DD}_SD1_PLL2$ $AV_{DD}_SD2_PLL1$ $AV_{DD}_SD2_PLL2$	1.35 V ± 67 mV	V	—
Fuse programming override supply		TA_PROG_SFP	1.80 V ± 90 mV	V	4
Thermal monitor unit supply		TH_V_{DD}	1.8 V ± 90 mV	V	—
General I/O supply voltage		OV_{DD}	1.8 V ± 90 mV	V	—

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended value	Unit	Notes
DDR4 I/O voltage		$G1V_{DD}$, $G2V_{DD}$, $G3V_{DD}$	1.2 V ± 60 mV	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		SV_{DD}	1.0 V ± 30mV	V	6
Pad power supply for SerDes transmitters		XV_{DD}	1.35 V ± 67 mV	V	—
USB PHY 3.3 V HS(High Speed) and SS(Super Speed) supply voltage		USB_HV_{DD}	3.3 V ± 165 mV	V	—
USB PHY Analog and Digital HS supply voltage		USB_SDV_{DD}	1.0 V +50 mV/-30mV	V	6
USB PHY Analog and Digital SS supply voltage		USB_SV_{DD}	1.0 V +50 mV/-30mV	V	6
Battery Backed Security Monitor supply		$TA_BB_V_{DD}$	1.0 V +50 mV/-30mV		6
Input voltage	DDR4 DRAM signal	MV_{IN}	GND to GnV_{DD}	V	—
	General I/O signals	OV_{IN}	GND to OV_{DD}	V	—
	SerDes signals	SV_{IN}	GND to SV_{DD}	V	—
	USB PHY 3.3 HS signals	USB_HV_{IN}	GND to USB_HV_{DD}	V	—
	USB PHY SS signals	USB_SV_{IN}	GND to USB_SV_{DD}	V	—
Operating temperature range	Normal operation	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—
	Extended temperature	T_A, T_J	T_A = -40 (min) to T_J = 105 (max)	°C	—
	AEC-Q100 Grade 3 temperature	T_A	T_A = -40 (min) to 85 (max)	°C	7, 8
	Secure boot fuse programming	T_A, T_J	T_A = 0 (min) to T_J = 70 (max)	°C	4

Notes:

1. See Voltage ID (VID) controllable supply in this document and "Core and platform supply voltage filtering" in the design checklist for additional information.

2. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

3. Operation at 1.1 V is allowable for up to 25 ms at initial power on.

4. TA_PROG_SFP must be supplied 1.80 V and the chip must operate in the specified fuse programming temperature range (0 - 70°C) only during secure boot fuse programming. For all other operating conditions, TA_PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power sequencing.

5. Voltage ID (VID) operating range is between 0.90 to 1.05 V. Regulator selection should be based on Vout range of at least 0.875 to 1.1 V, with resolution of 12.5 mV or better.

6. For supported voltage requirement for a given part number, contact your NXP sales representative.

7. Only available on automotive grade parts

8. The Tj must not exceed 105°C. Proper thermal solution should be applied to meet this requirement.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.

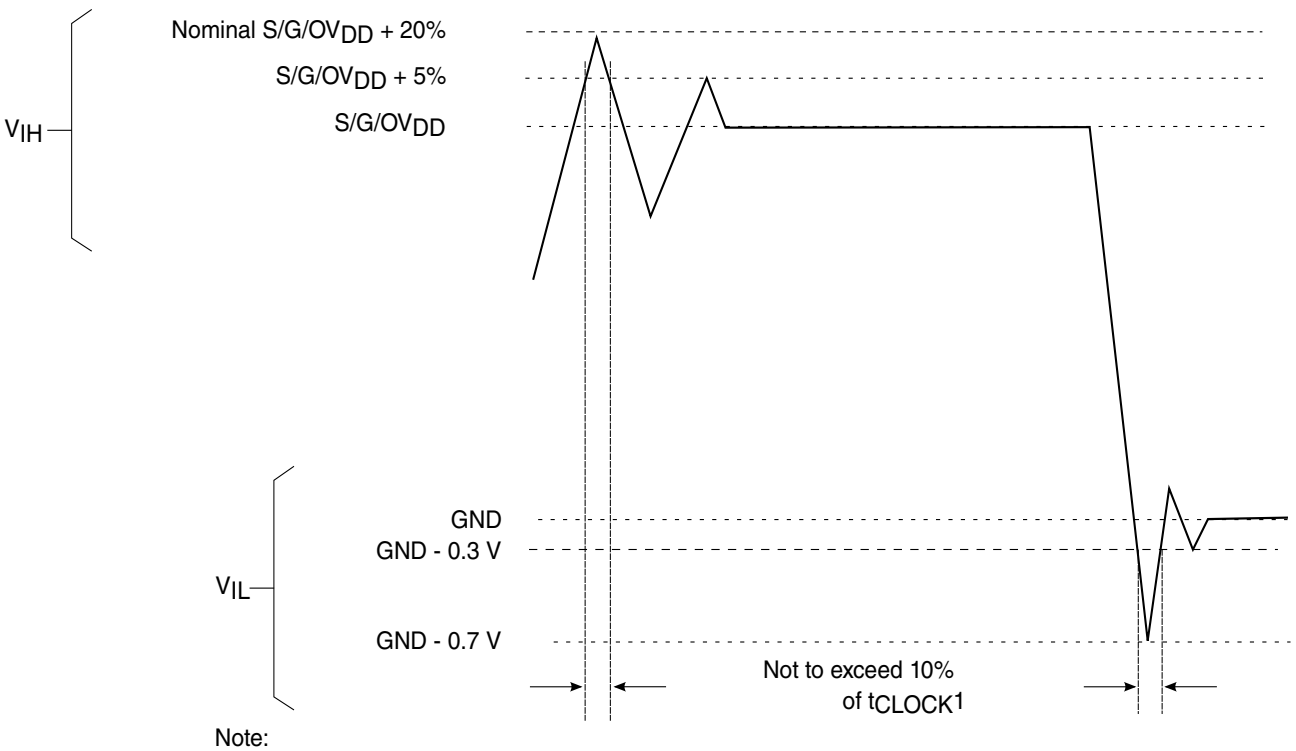


Figure 7. Overshoot/Undershoot voltage for $GV_{DD}/OV_{DD}/SV_{DD}$

The core and platform voltages must always be provided at nominal VID. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the internally generated MV_{REF} signal. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE

These values are preliminary estimates.

Table 4. Output drive capability

Driver type	Output impedance (Ω)	Supply voltage	Notes
DDR4 signal	18 (full-strength mode) 27 (half-strength mode)	GV_{DD} = 1.2 V	1
General I/O signals	45	OV_{DD} = 1.8 V	—
Notes: 1. The drive strength of the DDR4 interface in half-strength mode is at T_j = 105 °C and at GV_{DD} (min).			

3.2 Power sequencing

For power up, the following sequence should be followed:

1. VDD must reach 90% of its value before G*n*V_{DD} reaches 10% of its value. During V_{DD} ramping, PORESET_B must be held low and TA_PROG_SFP must be grounded. All other power supplies(OV_{DD}, USB_HV_{DD}, USB_SV_{DD}, USB_SDV_{DD}, SV_{DD}, XV_{DD}, TA_BB_V_{DD}, TH_V_{DD}, AV_{DD} (cores, platform, DDR), and AV_{DD}_SD*m*_PLL*n*) have no ordering requirement with respect to one another and with respect to V_{DD} and G*n*V_{DD}. All supplies must be at their stable values within 400 ms.
2. Negate PORESET_B input as long as the required assertion/hold time has been met per Table 19.
3. For secure boot fuse programming, use the following steps:
   a. After negation of PORESET_B, drive TA_PROG_SFP = 1.80 V after a required minimum delay per Table 5.
   b. After fuse programming is completed, it is required to return TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 5. See Security fuse processor, for additional details.

NOTE

If using Trust Architecture Security Monitor battery backed features, prior to V_{DD} ramping up to 0.5 V level, ensure that OV_{DD} is properly ramped and SYSCLK or DIFF_SYSCLK / DIFF_SYSCLK_B is running. The clock should have a minimum frequency of 800 MHz and a maximum frequency no greater than the supported system clock frequency for the device.

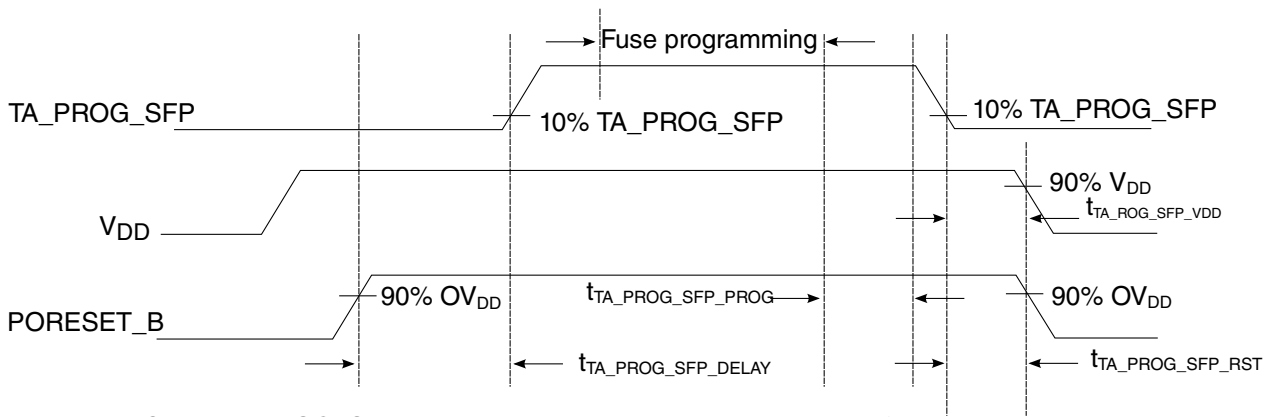
Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} supplies, there will be a brief period as the V_{DD} powers up that the I/Os associated with that I/O supply may go from being tristated to an indeterminate state (either driven to a logic one or zero) and extra current may be drawn by the device.

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

This figure provides the TA_PROG_SFP timing diagram.



NOTE: TA_PROG_SFP must be stable at 1.80 V prior to initiating fuse programming.

Figure 8. TA_PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 5. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{TA_PROG_SFP_DELAY}$	100	—	SYSCLKs	1
$t_{TA_PROG_SFP_PROG}$	0	—	µs	2
$t_{TA_PROG_SFP_VDD}$	0	—	µs	3
$t_{TA_PROG_SFP_RST}$	0	—	µs	4

Table continues on the next page...

Table 5. TA_PROG_SFP timing [5] (continued)

Driver type	Min	Max	Unit	Notes
1. Delay required from the de-assertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% TA_PROG_SFP ramp up.				
2. Delay required from fuse programming finished to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.80 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is completed, it is required to return TA_PROG_SFP = GND.				
3. Delay required from TA_PROG_SFP ramp down complete to V_{DD} ramp down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before V_{DD} is at 90% V_{DD}.				
4. Delay required from TA_PROG_SFP ramp down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.				
5. Only two secure boot fuse programming events are permitted per lifetime of a device.				

Warning

TA_PROG_SFP ramp up slew rate must not exceed 18,000V/s. Ramp down does not have a slew rate constraint.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 5.

NOTE

All input signals, including I/Os that are configured as inputs, driven into the chip need to monotonically increase/decrease through entire rise/fall durations.

3.4 Power characteristics

These tables show the thermal power dissipation of the V_{DD} power supply for four A72 core/platform/DDR frequency combinations.

Table 6. LS2088A VDD power dissipation for the thermal design at 85C

A72 frequency (MHz)	Coherency domain frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	AIOP DDR data rate(MT/s)	V_{DD} (V)	Power (W)	Notes
2100	1600	800	2133	1600	VID	36.3	1, 2, 3, 4
2000	1600	800	2133	1600	VID	35.7	1, 2, 3, 4
2000	1400	700	2133	1600	VID	35.4	1, 2, 3, 4, 5
1800	1400	700	1867	1600	VID	27.3	1, 2, 3, 4
1600	1200	600	1600	1600	VID	24.1	1, 2, 3, 4

Notes:

1. VDD must run at VID voltage level, which is defined in FUSESR register

2. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform at 100% activity factor. AIOP is powered but idle.

3. Thermal power are based on worst-case processed device. The above powers are measured at the junction temperature of 85C.

4. Refer to AN4977 "QorIQ LS2088A Family Design Checklist":

Section 4.2 "Maximum VDD Power and IO Power" shows the maximum power dissipation across junction temperature range. This should be used as guide for power supply design and regulator sizing.

Section 7.23.1 "Thermal Power" shows the thermal power across junction temperature range. This data should be used thermal solution design.

5. Valid for part numbers with "7" in option code

Table 7. LS2048A VDD power dissipation for the thermal design at 85C

A72 frequency (MHz)	Coherency domain frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	AIOP DDR data rate(MT/s)	V_{DD} (V)	Power (W)	Notes
2100	1600	800	2133	1600	VID	27.2	1, 2, 3, 4
2000	1600	800	2133	1600	VID	26.8	1, 2, 3, 4
2000	1400	700	2133	1600	VID	26.5	1, 2, 3, 4, 5
1800	1400	700	1867	1600	VID	20.4	1, 2, 3, 4
1600	1200	600	1600	1600	VID	18.2	1, 2, 3, 4

Notes:

1. VDD must run at VID voltage level, which is defined in FUSESR register

2. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor. AIOP is powered but idle.

3. Thermal power are based on worst-case processed device. The above powers are measured at the junction temperature of 85C.

4. Refer to AN4977 "QorIQ LS2088A Family Design Checklist":

Section 4.2 "Maximum VDD Power and IO Power" shows the maximum power dissipation across junction temperature range. This should be used as guide for power supply design and regulator sizing.

Section 7.23.1 "Thermal Power" shows the thermal power across junction temperature range. This data should be used thermal solution design.

Table 7. LS2048A VDD power dissipation for the thermal design at 85C

A72 frequency (MHz)	Coherency domain frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	AIOP DDR data rate(MT/s)	V_{DD} (V)	Power (W)	Notes
5. Valid for part numbers with "7" in option code							

The following table shows the estimated power saving for the low power modes.

Table 8. LS2088A/LS2048A low power mode power saving, 65ºC[1,2,3]

Low Power Mode		Core/Platform/DDR				Units	Comments	Notes
NXP	Arm®	2100/800/2133 MHz, VDD=1.0 V	2000/800/2133 MHz, VDD=1.0V	1800/700/1867 MHz, VDD=1.0 V	1600/600/1600 MHz, VDD=0.9 V			
PW15	STANDBYWFI/WFE	1.26	1.19	1.06	0.74	Watts	Saving realized moving from run to PW15 per core	4
PW20	STANDBYWFI/ WFE-retain	1.31	1.25	1.12	0.77	Watts	Saving realized moving from run to PW20 per core	4
PCL10	STANDBYWFIL2	0.20	0.19	0.19	0.14	Watts	Saving realized moving from PW15 or PW20 to PCL10 per cluster	
LPM20	—	0.75	0.74	0.71	0.47	Watts	Saving realized moving from PCL10 to LPM20 per device	

Notes:

1. Power for V_{DD} only.
2. Typical power assumes Dhrystone running with activity factor of 70%. AIOP is powered but idle.
3. Typical power based on nominal process device.
4. PW15, PW20 power savings with one core. Maximum savings would be N times, where N is the number of used cores.

The following table shows the estimated power dissipation on the TA_BB_V_{DD} supply for the LS2088A/LS2048A at allowable voltage levels.

Table 9. TA_BB_V_{DD} power dissipation

Supply	Maximum	Unit	Notes
TA_BB_V_{DD} (LS2088A/LS2048A off, 70°C)	55	uW	1
TA_BB_V_{DD} (LS2088A/LS2048A off, 40°C)	40	uW	1

Notes:

1. When LS2088A/LS2048A is off, TA_BB_V_{DD} may be supplied by battery power to retain the Zeroizable Master Key and other trust architecture state. Board should implement a PMIC, which switches TA_BB_V_{DD} to battery when SoC powered down. See the LS2088A reference manual trust architecture chapter for more information.

3.5 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 10. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/GnV_{DD}/SV_{DD}/XV_{DD}/ V_{DD}, all AV_{DD} supplies.)	—	25	V/ms	1, 2
Required ramp rate for TA_PROG_SFP	—	18	V/ms	1, 2

Notes:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

3.6 Input clocks

3.6.1 System clock (SYSCLK) timing specifications

This section provides the system clock DC and AC timing specifications.

3.6.1.1 System clock DC timing specifications

This table provides the system clock (SYSCLK) DC characteristics.

Table 11. SYSCLK DC electrical characteristics[3]

Characteristic	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	—	V	1
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2, 3

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3.

3.6.1.2 System clock AC timing specifications

This table provides the system clock (SYSCLK) AC timing specifications.

Table 12. SYSCLK AC timing specifications[5]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	83.3	—	133.3	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	12	ns	1, 2
SYSCLK duty cycle	t_{KHK} / t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at -56 dBc	—	—	—	500	KHz	4
AC input swing limits	ΔV_{AC}	0.60 x OV_{DD}	—	OV_{DD}	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V, see Table 3.

3.6.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content.

The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 13. Spread-spectrum clock source recommendations[1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—

Table continues on the next page...

Table 13. Spread-spectrum clock source recommendations[1] (continued)

Parameter	Min	Max	Unit	Notes
Frequency spread	—	1.0	%	2, 3

Notes:

1. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3.
2. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 12.
3. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

3.6.3 Differential System clock (DIFF_SYSCLK/DIFF_SYSCLK_B) timing specifications

Differential system clocking mode requires an onboard oscillator to provide reference clock input to Differential System clock pair (DIFF_SYSCLK/DIFF_SYSCLK_B).

This Differential clock pair can be configured to provide clock to Core, Platform and USB PLLs.

This figure shows a receiver reference diagram of the Differential System clock.

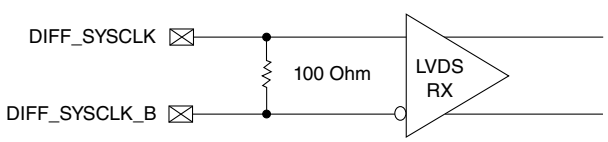


Figure 9. LVDS receiver

This section provides the differential system clock DC and AC timing specifications.

3.6.3.1 Differential System clock DC timing specifications

The differential system clock receiver voltage requirements are as specified in the Recommended operating conditions table.

The differential system clock can also be single-ended. For this, DIFF_SYSCLK_B should be connected to $OV_{DD}/2$.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) DC specifications.

Table 14. Differential system clock DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage swing	V_{id}	100	-	600	mV	2
Input common mode voltage	V_{icm}	50	-	1570	mV	-
Power supply current	I_{cc}	-	-	5	mA	-
Input capacitance	C_{in}	1.45	1.5	1.55	pF	-

Note:

1. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3 for details.
2. Input differential voltage swing (Vid) specified is equal to |VDIFF_SYSCLK_P - VDIFF_SYSCLK_N|

3.6.3.2 Differential System clock AC timing specifications

Differential System clock(DIFF_SYSCLK/DIFF_SYSCLK_B) input pair supports input clock frequency of 83.3-133.3MHz

Spread spectrum clocking is not supported on differential system clock pair input.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) AC specifications.

Table 15. Differential system clock AC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
DIFF_SYSCLK/DIFF_SYSCLK_B frequency range	t_{DIFF_SYSCLK}	83.3		133.3	MHz	-
DIFF_SYSCLK/DIFF_SYSCLK_B frequency tolerance	t_{DIFF_TOL}	-300	-	+300	ppm	-
Duty cycle	t_{DIFF_DUTY}	40	50	60	%	-
Clock period jitter (peak to peak)	t_{DIFF_TJ}	-	-	100	ps	1

Note:

1. This is evaluated with supply noise profile at +/- 5% sine wave
2. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3

3.6.4 USB reference clock specification

USB PHY needs a reference clock. There are two options for the reference clock: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B.

This table provides the additional requirements when SYSCLK or DIFF_SYSCLK/ DIFF_SYSCLK_B is used as USB REFCLK.

Table 16. REFCLK requirements for USB PHY

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
REFCLK duty cycle	t_{KHK} / t_{SYSCLK}	45	—	55	—	—
REFCLK frequency	f_{SYSCLK}	—	100	—	MHz	—
REFCLK frequency offset	FREF_OFFSET	-300	—	300	ppm	—
REFCLK random jitter	RMSJREF_CLK	—	—	3	ps	1, 2
REFCLK cycle-to-cycle jitter	DJREF_CLK	-150		150	ps	3
Notes: 1. 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz. 2. The peak-to-peak Rj specification is calculated as 14.069 times the RMS Rj for 10-12 BER. 3. DJ across all frequencies.						

3.6.5 Real-time clock timing

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed.

3.6.6 DDR clock timing

This section provides the DDR clock DC and AC timing specifications.

3.6.6.1 DDR clock DC electrical characteristics

This table provides the DDR clock (DDRCLK) DC electrical characteristics.

Table 17. DDRCLK DC electrical characteristics[3]

Characteristic	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	—	V	1

Table continues on the next page...

Table 17. DDRCLK DC electrical characteristics[3] (continued)

Characteristic	Symbol	Min	Typical	Max	Unit	Notes
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3.

3.6.6.2 DDR clock AC timing specifications

This table provides the DDR clock (DDRCLK) AC timing specifications.

Table 18. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	100	—	133.3	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	7.5	—	10	ns	1, 2
DDRCLK duty cycle	t_{KHK} / t_{DDRCLK}	40	—	60	%	2
DDRCLK slew rate	—	1	—	4	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	—
DDRCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits	ΔV_{AC}	0.60 x OV_{DD}	—	OV_{DD}	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3.

3.6.7 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, such as SerDes, see the specific interface section.

3.7 RESET initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table describes the AC electrical specifications for the RESET initialization timing.

Table 19. RESET initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B	1	—	ms	1
Required input assertion time of HRESET_B	32	—	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	—	10	SYSCLK	4
Maximum rise/fall time of PORESET_B	—	1	SYSCLK	4
Input setup time for POR configs (other than cfg_eng_use0) with respect to negation of PORESET_B	4	—	SYSCLKs	2,5
Input hold time for all POR configs with respect to negation of PORESET_B	2	—	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	—	5	SYSCLKs	2

Notes:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. SYSCLK is the primary clock input for the chip.
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in section "Power-On Reset Sequence" in the chip reference manual.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
5. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reach its operating condition.

3.8 DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

NOTE

When operating at a DDR data rate of 1866 MT/s or higher, only one dual-ranked module per memory controller is supported.

3.8.1 DDR4 SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 20. DDR4 SDRAM interface DC electrical characteristics (GV_{DD} = 1.2 V)[7]

Parameter	Symbol	Min	Max	Unit	Notes
Input low	V_{IL}	—	0.7 x GV_{DD} - 0.175	V	3, 5
Input high	V_{IH}	0.7 x GV_{DD} + 0.175	—	V	3, 5
I/O leakage current	I_{OZ}	-165	165	µA	4

Notes:

1. GV_{DD} is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. V_{TT} and VREFCA are applied directly to the DRAM device. Both V_{TT} and VREFCA voltages must track $GV_{DD}/2$.
3. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
4. Output leakage is measured with all outputs disabled, 0V ≤ VOUT ≤ GV_{DD}.
5. Internal Vref for data bus must be set to 0.7 x GV_{DD}.
6. See the IBIS model for the complete output IV curve characteristics.
7. For recommended operating conditions, see Table 3.

3.8.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.8.2.1 DDR4 SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 21. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5%)$_1$

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage ≤ 2133 MT/s data rate	V_{ILAC}	—	0.7 x GV_{DD} - 0.175	V	—
AC input high voltage ≤ 2133 MT/s data rate	V_{IHAC}	0.7 x GV_{DD} + 0.175	—	V	—

Note:

1. For recommended operating conditions, see Table 3.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 22. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5% for DDR4)$_3$

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS-MDQ/MECC	t_{CISKEW}	—	—	ps	1
2133 MT/s data rate		-80	80		
1866 MT/s data rate		-93	93		
1600 MT/s data rate		-112	112		
1333 MT/s data rate		-125	125		
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	—	—	ps	2
2133 MT/s data rate		-154	154		
1866 MT/s data rate		-175	175		
1600 MT/s data rate		-200	200		
1333 MT/s data rate		-250	250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

3. For recommended operating conditions, see Table 3.

This figure shows the DDR4 SDRAM interface input timing diagram.

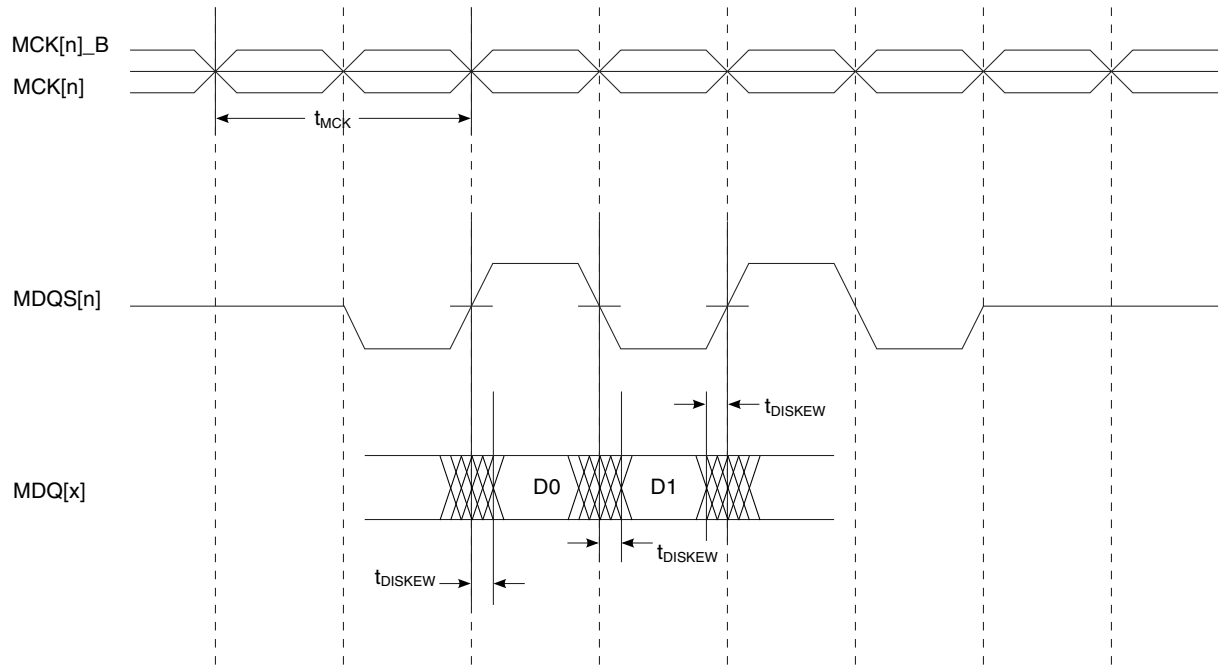


Figure 10. DDR4 SDRAM interface input timing diagram

3.8.2.2 DDR4 SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR4 SDRAM interface.

Table 23. DDR4 SDRAM interface output AC timing specifications (GV_{DD} = 1.2 V)[7]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	938	1500	ps	2
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	—	—	ps	3
2133 MT/s data rate		350	—		
1866 MT/s data rate		410	—		
1600 MT/s data rate		495	—		
1333 MT/s data rate		606	—		
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	—	—	ps	3
2133 MT/s data rate		350	—		
1866 MT/s data rate		390	—		
1600 MT/s data rate		495	—		
1333 MT/s data rate		606	—		
MCK to MDQS Skew	t_{DDKHMH}	-150	150	ps	4,7
MDQ/MECC/MDM output data eye	$t_{DDKXDEYE}$	—	—	ps	5
2133 MT/s data rate		320	—		
1866 MT/s data rate		350	—		

Table continues on the next page...

Table 23. DDR4 SDRAM interface output AC timing specifications (GV_{DD} = 1.2 V)[7] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
1600 MT/s data rate		400	—		
1333 MT/s data rate		500	—		
MDQS preamble	t_{DDKHMP}	0.9 x t_{MCK}	—	ps	—
MDQS postamble	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ps	—

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

3. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.

4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. Note that this is required to program the start value of the DQS adjust for write leveling.

7. For recommended operating conditions, see Table 3.

NOTE

For the ADDR/CMD/CNTL setup and hold specifications in Table 23, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR4 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

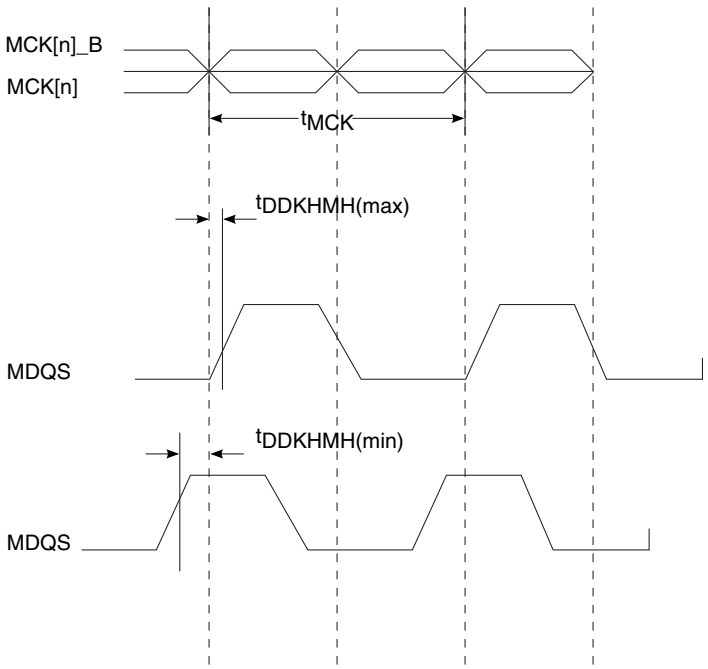


Figure 11. t_{DDKHMH} timing diagram

This figure shows the DDR4 SDRAM output timing diagram.

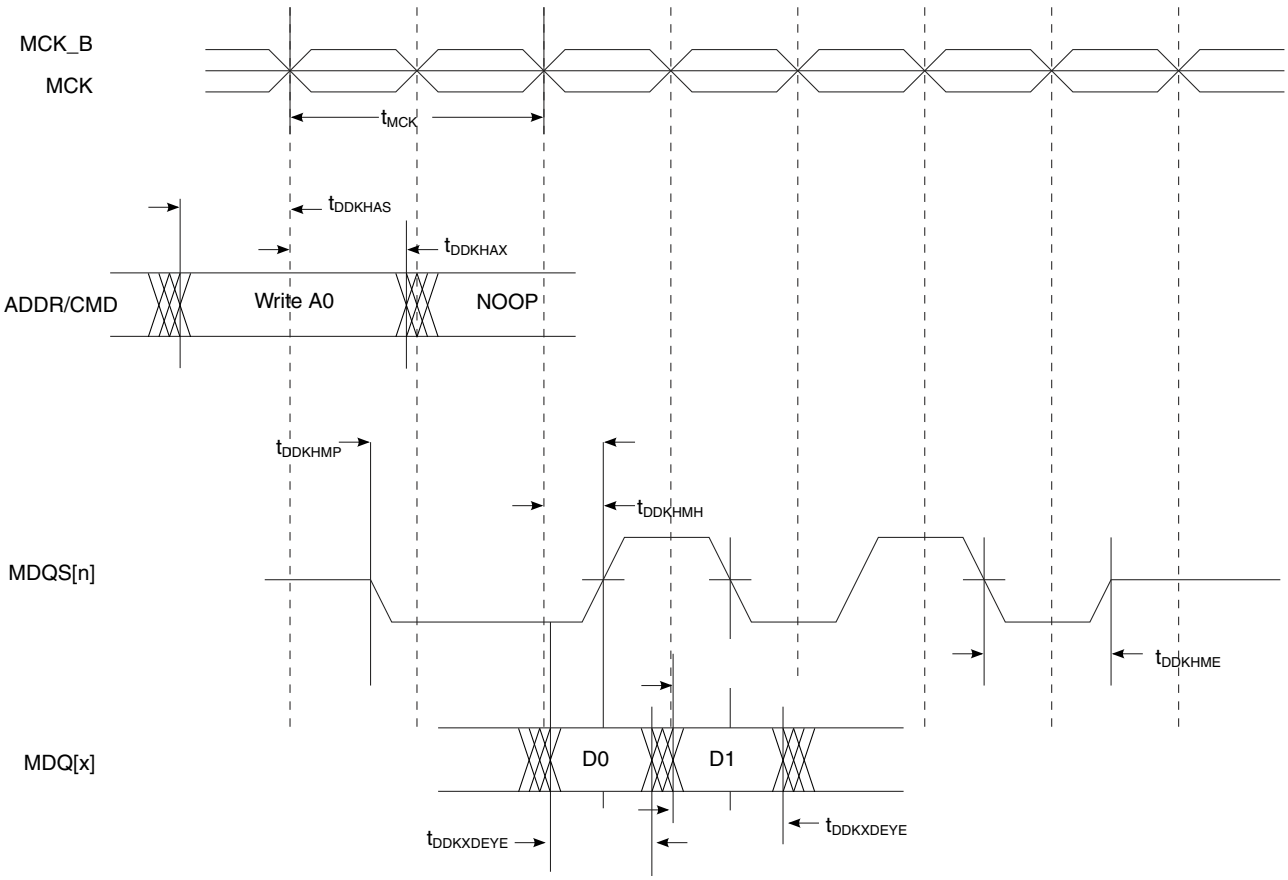


Figure 12. DDR4 output timing diagram

3.9 SPI interface

This section describes the DC and AC electrical characteristics for the SPI interface.

3.9.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface operating at OV_{DD} = 1.8 V.

Table 24. SPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage	V_{OH}	1.35	—	V	—

Table continues on the next page...

Table 24. SPI DC electrical characteristics (1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
(OV_{DD} = min, I_{OH} = -0.5 mA)					
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.9.2 SPI AC timing specifications

This table provides the SPI timing specifications.

Table 25. SPI AC timing specifications

Parameter	Symbol	Condition	Min	Max	Unit	Notes
SCK Cycle Time	t_{SCK}	—	t_{SYS} * 2	—	ns	
SCK Clock Pulse Width	t_{SDC}	—	40%	60%	t_{SCK}	
CS to SCK Delay	t_{CSC}	Master	tp*2-6	—	ns	1,2
After SCK Delay	t_{ASC}	Master	tp*2-1	—	ns	1,2
Slave Access Time (SS active to SOUT driven)	t_A	Slave	—	15	ns	
Slave Disable Time (SS inactive to SOUT High-Z or invalid)	t_{DI}	Slave	—	10	ns	
Data Setup Time for Inputs	t_{NIIVKH}	Master	9	—	ns	
	t_{NEIVKH}	Slave	4	—		
Data Hold Time for Inputs	t_{NIIXKH}	Master	0	—	ns	
	t_{NEIXKH}	Slave	2	—		
Data Valid (after SCK edge) for Outputs	t_{NIKHOV}	Master	—	5	ns	
	t_{NEKHOV}	Slave	—	10		
Data Hold Time for Outputs	t_{NIKHOX}	Master	0	—	ns	
	t_{NEKHOX}	Slave	0	—		

Notes:

1. tp is the input clock period for the SPI controller. 1/tp is the platform clock/2.
2. The delay is programmable. Refer to CTARx register in LS2088A RM for more details.

This figure shows the SPI timing master when CPHA = 0.

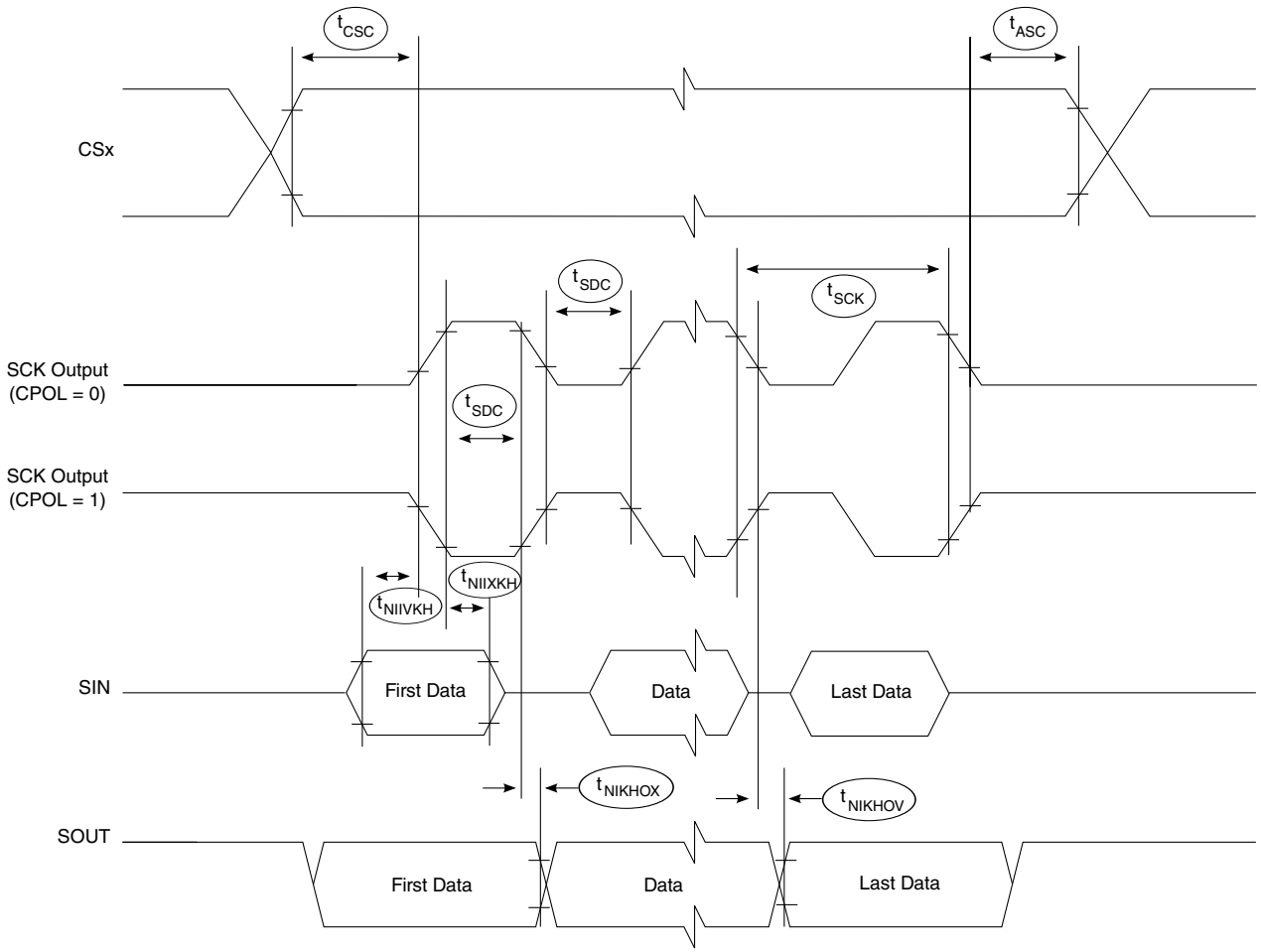


Figure 13. SPI classic SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

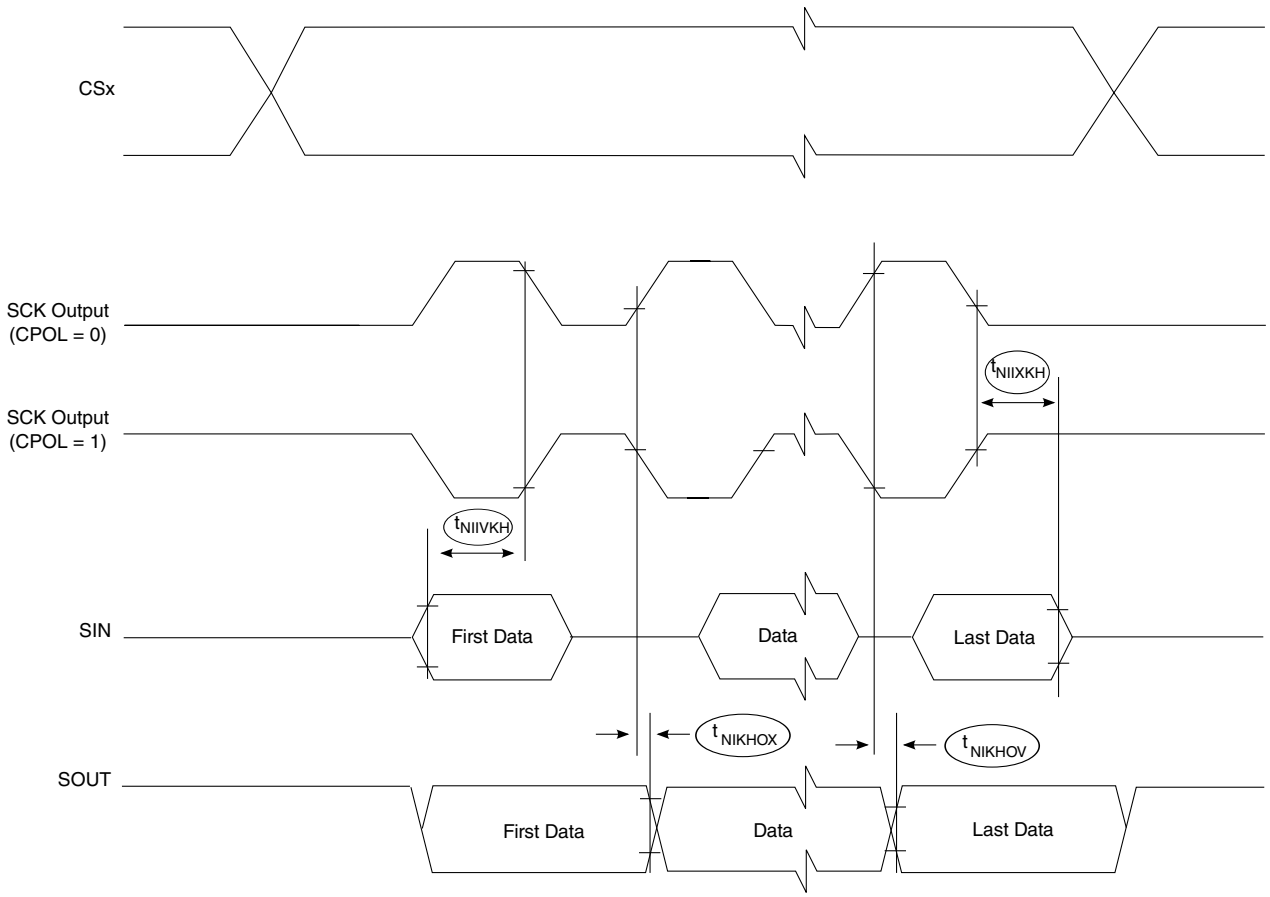


Figure 14. SPI classic SPI timing master, CPHA = 1

This figure shows the SPI timing slave when CPHA = 0.

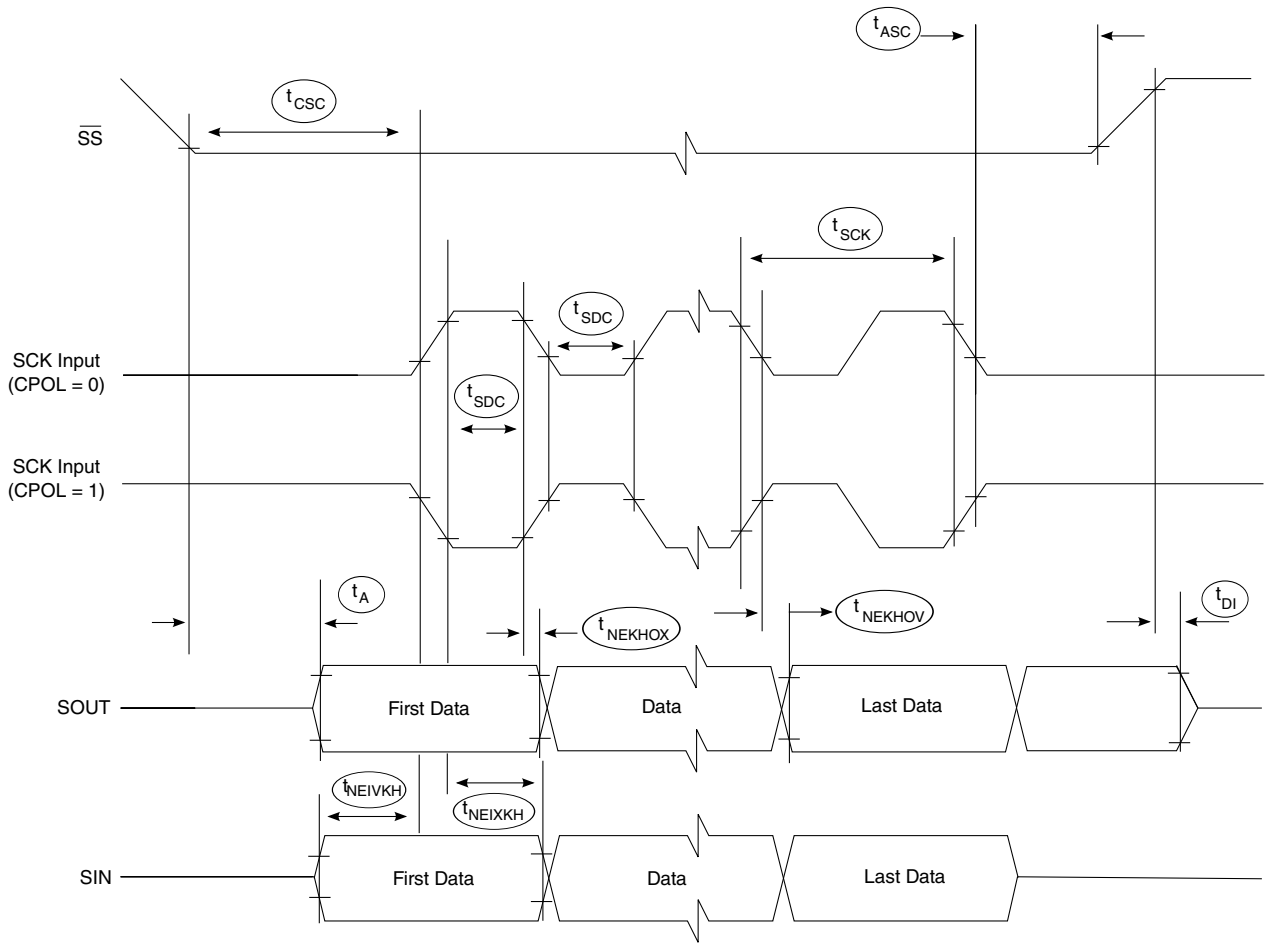


Figure 15. SPI classic SPI timing slave, CPHA = 0

This figure shows the SPI timing slave when CPHA = 1.

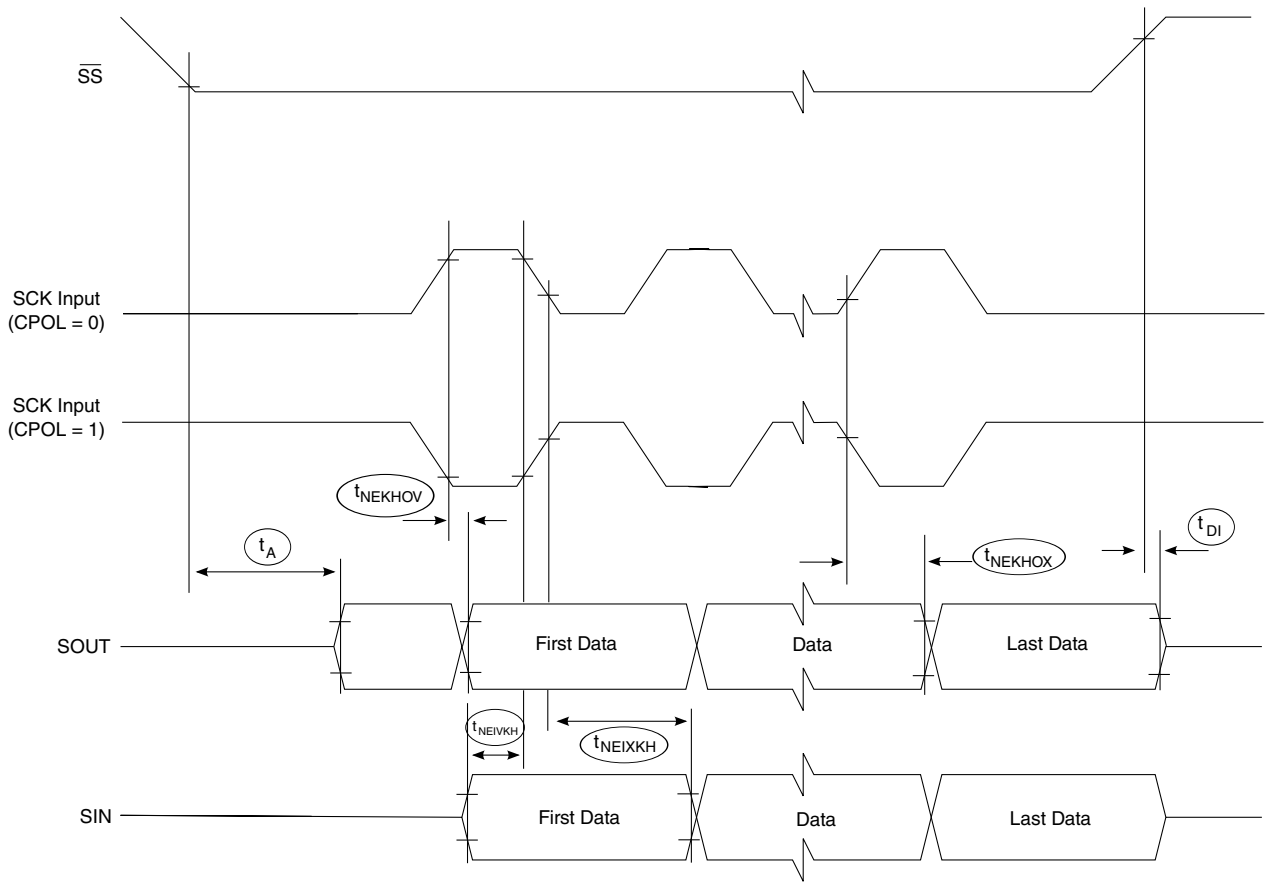


Figure 16. SPI classic SPI timing slave, CPHA = 1

3.10 QuadSPI interface

This section describes the DC and AC electrical characteristics for the QuadSPI interface.

3.10.1 QuadSPI DC electrical characteristics

This table provides the DC electrical characteristics for the QuadSPI interface operating at OV_{DD} = 1.8 V.

Table 26. QuadSPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7*OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2*OV_{DD}	V	1
Input current (0 V ≤ V_{IN} ≤)	I_{IN}	—	±50	μA	2
Output high voltage (I_{OH} = -100 μA)	V_{OH}	OV_{DD} - 0.2	—	V	—

Table continues on the next page...

Table 26. QuadSPI DC electrical characteristics (1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (I_{OL} = 100 µA)	V_{OL}	—	0.2	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. At recommended operating conditions with OV_{DD} = 1.8 V.

3.10.2 QuadSPI AC timing specifications

This section describes the QuadSPI timing specifications in both SDR and DDR modes. All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing figures in this section.

3.10.2.1 QuadSPI timing SDR mode

This table provides the QuadSPI input and output timing in SDR mode (MCR[DQS_EN] = 0, regarding to the 1st sample point. See qSPI_SMPR[xSDLY, xSPHS] in the corresponding reference manual for different sampling points).

Table 27. SDR mode QuadSPI input and output timing

Parameter	Symbol	Min	Max	Unit
Clock rise/fall time	T_{RISE}/T_{FALL}	1	—	ns
CS output hold time	$t_{NIKHOX2}$-	-3.3+j*T	—	ns
CS valid to clock	$t_{NIKHOV2}$	-3.0+k*T	—	ns
Setup time for incoming data	t_{NIIVKH}	5.59	—	ns
Hold time requirement for incoming data	t_{NIIXKH}	1.0	—	ns
Output data delay	t_{NIKHOV}	—	1.45	ns
Output data hold	t_{NIKHOX}	-1.45	—	ns

Note: T: Clock period. j: qSPI_FLSHCR[TCSH]; k:depends qSPI_FLSHCR[TCSS].

This table provides the QuadSPI input and output timing in SDR mode with internal DQS (MCR[DQS_EN] = 1, regarding to the 1st sample point).

Table 28. SDR mode QuadSPI input and output timing

Parameter	Symbol	Min	Max	Unit
Clock rise/fall time	T_{RISE}/T_{FALL}	1	—	ns
CS output hold time	$t_{NIKHOX2}$-	-0.45+j*T	—	ns

Table continues on the next page...

Table 28. SDR mode QuadSPI input and output timing (continued)

Parameter	Symbol	Min	Max	Unit
CS valid to clock	$t_{NIKHOV2}$	-3.0+k*T	—	ns
Setup time for incoming data	t_{NIIVKH}	2.59-Tcoars-Ttap	—	ns
Hold time requirement for incoming data	t_{NIIXKH}	0.01+Tcoars +Ttap	—	ns
Output data delay	t_{NIKHOV}	—	1.45	ns
Output data hold	t_{NIKHOX}	-1.45	—	ns

Note: T: Clock period. i: depending qSPI_SMPR[xSDLY, xSPHS]; j: qSPI_FLSHCR[TCSH]; k:depends qSPI_FLSHCR[TCSS]; Ttapx: SOCCFG[7:0]/ SOCCFG[23:16].

This figure shows the QuadSPI AC timing in SDR mode.

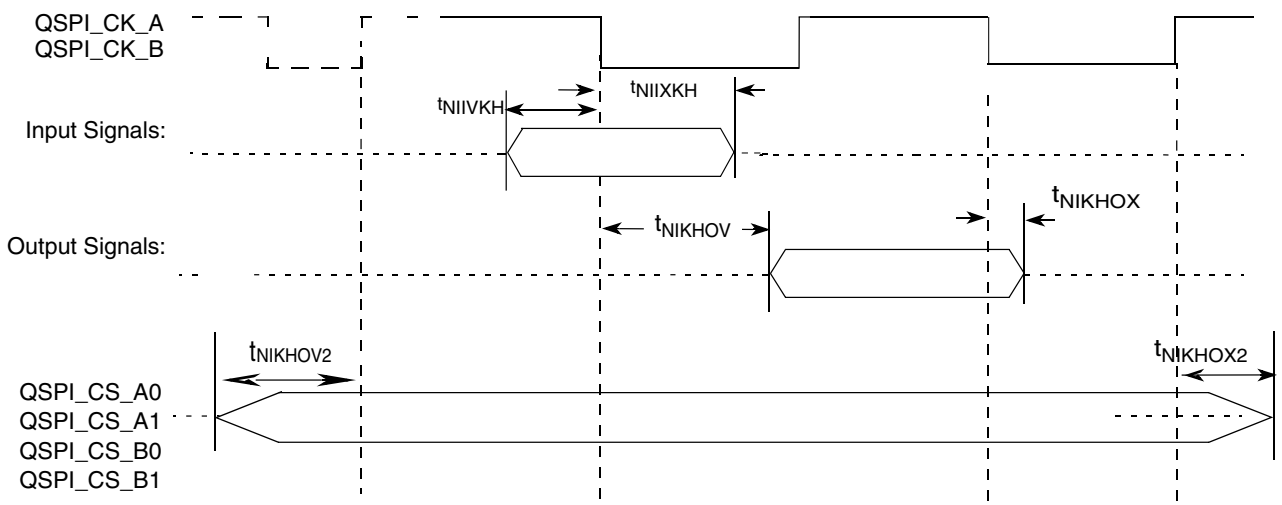


Figure 17. QuadSPI AC timing — SDR mode

3.10.2.2 QuadSPI timing DDR mode

This table provides the QuadSPI input and output timing in DDR mode with external DQS/delay chain (MCR[DQS_EN] = 1, regarding to the 1st sample point.)

Table 29. DDR mode QuadSPI input and output timing

Parameter	Symbol	Min	Max	Unit
Clock rise/fall time	T_{RISE} T_{FALL}	1	—	ns
CS output hold time	$t_{NIKHOX2}$	-3.3+j*T	—	ns

Table continues on the next page...

Table 29. DDR mode QuadSPI input and output timing (continued)

Parameter	Symbol	Min	Max	Unit
CS valid to clock	$t_{NIKHOV2}$	-3.0+k*T	—	ns
DQS to data skew (ns)	t_{NIIVKH} t_{NIIVKL}	-0.91	0.9	ns
Output Data Valid	t_{NIKHOV}	—	*0.9+m*T/8*	ns
Output Data Hold	t_{NIKHOX}	*-0.9+m*T/8*	—	ns

Note: T: Clock period. j: qSPI_FLSHCR[TCSH]; k:depends qSPI_FLSHCR[TCSS]; m: QSPI_FLSHCR[TDH].

This figure shows the QuadSPI AC timing in DDR mode.

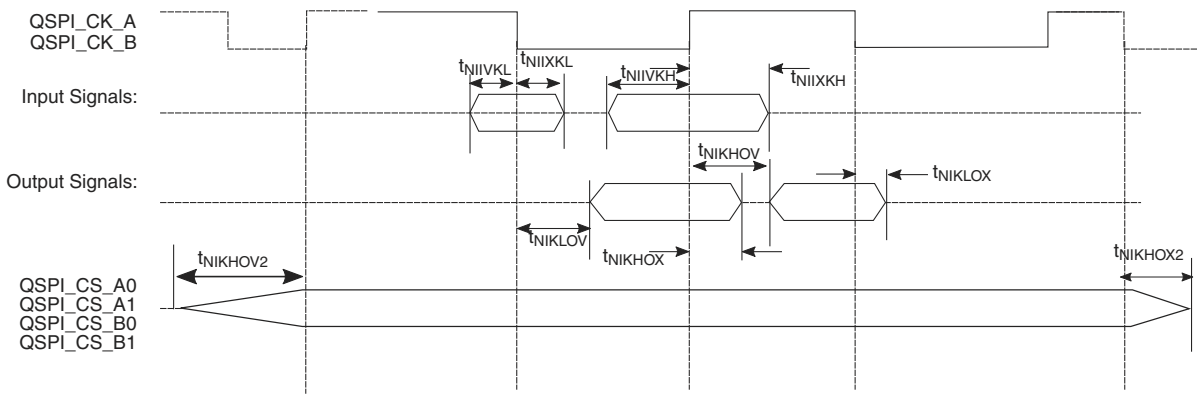


Figure 18. QuadSPI AC timing — DDR mode

This figure shows the QuadSPI data input timing in DDR mode with an external DQS.

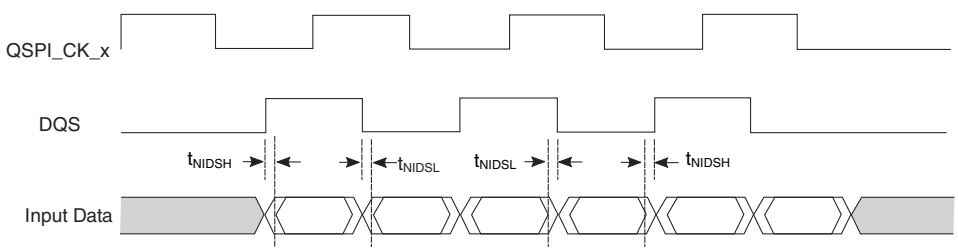


Figure 19. QuadSPI input AC timing — DDR mode with an external DQS

This figure shows the QuadSPI clock input timing diagram.

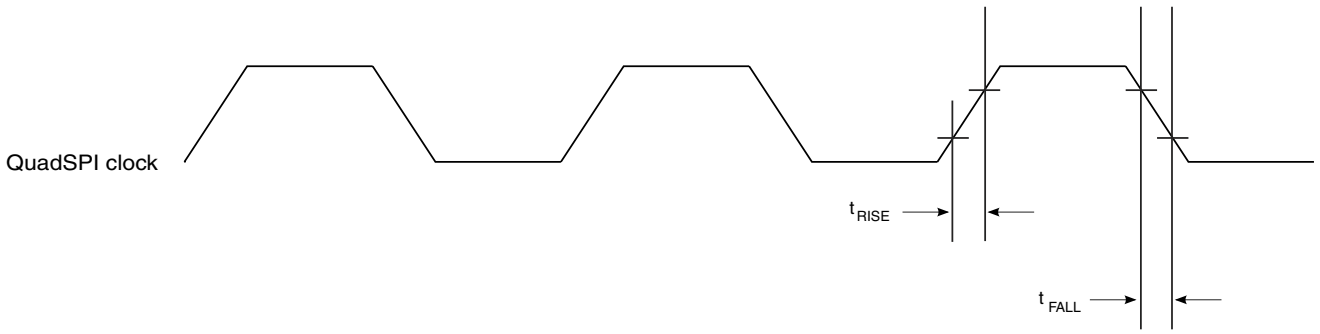


Figure 20. QuadSPI clock input timing diagram

This figure shows the AC test load for QuadSPI.

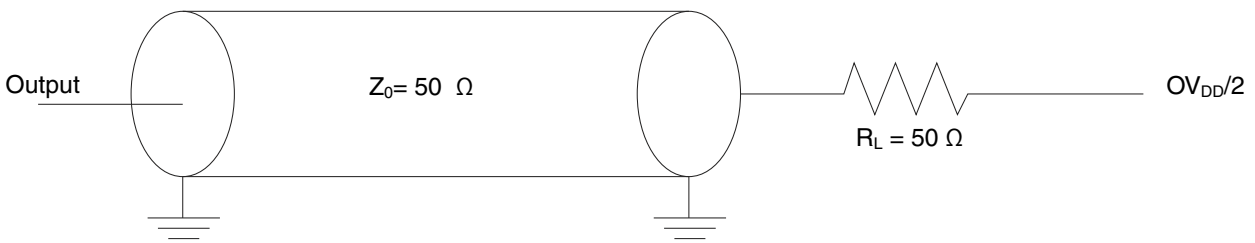


Figure 21. AC test load for QuadSPI

3.11 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

3.11.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at OV_{DD} = 1.8 V.

Table 30. DUART DC electrical characteristics(1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—
Notes:					

Table 30. DUART DC electrical characteristics(1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.					
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.					
3. For recommended operating conditions, see Table 3.					

3.11.2 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

Table 31. DUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 x 16)	baud	1, 2
Notes:			
1. f_{PLAT} refers to the internal platform clock.			
2. The actual attainable baud rate is limited by the latency of interrupt processing.			
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.			

3.12 Ethernet management interface 1 and 2, IEEE Std 1588™

This section provides the AC and DC electrical characteristics for the Ethernet controller and the Ethernet management interfaces.

3.12.1 Ethernet management interface (EMI)

This section discusses the electrical characteristics for the EMI1 and EMI2 interfaces.

Both EMI1 and EMI2 interfaces support IEEE Std 802.3™ Clause 22 and Clause 45.

Note that both EMI1 and EMI2 are powered by 1.8V OV_{DD}, so external voltage level translators are needed to connect to PHY devices.

3.12.1.1 Ethernet management interface DC electrical characteristics

The DC electrical characteristics for EMI1_MDIO, EMI1_MDC, EMI2_MDIO and EMI2_MDC are provided in this section.

Table 32. Ethernet management interface DC electrical characteristics (OV_{DD} = 1.8 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input high current (V_{IN} = OV_{DD})	I_{IH}	—	50	μA	2
Input low current (V_{IN} = GND)	I_{IL}	-50	—	μA	—
Output high voltage (OV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	1.35	OV_{DD} + 0.3	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND - 0.3	0.40	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.12.1.2 Ethernet management interface AC electrical specifications

This table provides the Ethernet management interface AC timing specifications.

Table 33. Ethernet management interface AC timing specifications[4]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	5	MHz	2
MDC clock pulse width high	t_{MDCH}	80	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	V - 3ns	—	V + 3ns	ns	3
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the Ethernet clock frequency (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. MDIO timing is configurable by programming MDIO_CFG. V value is determined by MDIO_CFG[NEG], MDIO_CFG[MDIO_HOLD] and MDIO[EHOL]. The easiest way is to program NEG=1, then MDIO is driven at negative edge of MDC, satisfying both setup and hold time reqirement of Ethernet PHY. If using MDIO_HOLD/EHOL to control the timing, enet_clk in the manual is equal to platform clock speed. See *Data Path Acceleration Architecture, Second Generation (DPAA2) Hardware Reference Manual*.
4. For recommended operating conditions, see Table 3.

3.12.2 IEEE 1588 electrical specifications

3.12.2.1 IEEE 1588 DC Electrical Characteristics

This table shows IEEE 1588 DC electrical characteristics when operating at OV_{DD} = 1.8 V supply.

Table 34. IEEE 1588 DC electrical characteristics (OV_{DD} = 1.8 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (OV_{IN}= 0 V or OV_{IN}= OV_{DD})	I_{IH}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	OV_{DD} + 0.3	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	GND - 0.3	0.40	V	—

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

3. For recommended operating conditions, see Table 3.

3.12.2.2 IEEE 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

Table 35. IEEE 1588 AC timing specifications[2]

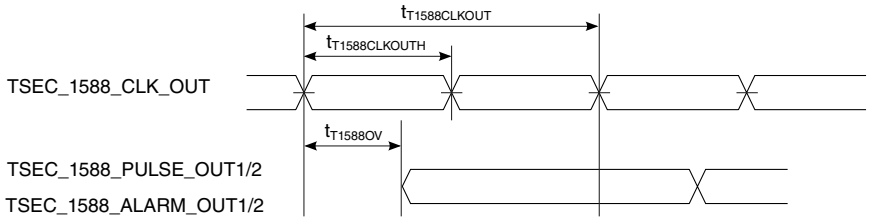
Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	6.0	—	—	ns	—
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time TSEC_1588_CLK_IN (20% -80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time TSEC_1588_CLK_IN (80% -20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0.5	—	4.0	ns	—
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{T1588CLK}$	—	—	ns	1

Notes:

1. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

2. For recommended operating conditions, see Table 3.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 22. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

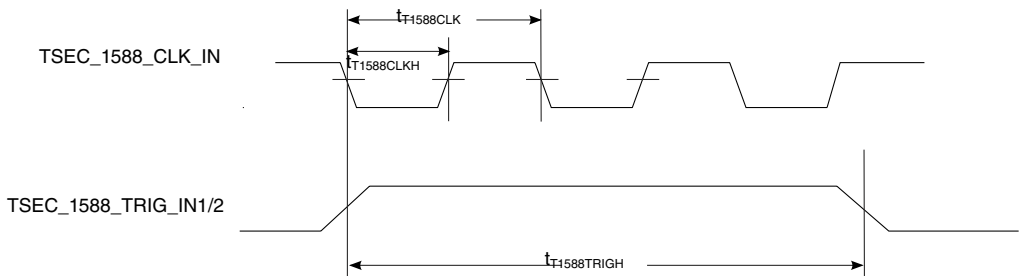


Figure 23. IEEE 1588 input AC timing

3.13 USB 2.0 interface

This section provides the AC and DC electrical specifications for the USB 2.0 interface.

3.13.1 USB 2.0 DC electrical characteristics

This table provides the DC electrical characteristics for the USB 2.0 interface at USB_HV_{DD} = 3.3 V.

Table 36. USB 2.0 DC electrical characteristics (USB_HV_{DD} = 3.3 V) [3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	-	V	1
Input low voltage	V_{IL}	-	0.8	V	1
Input current (USB_HV_{IN} = 0 V or USB_HV_{IN}= USB_HV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	-	V	-
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.3	V	-
Notes:					

Table 36. USB 2.0 DC electrical characteristics (USB_HV_{DD} = 3.3 V) [3]

Parameter	Symbol	Min	Max	Unit	Notes
1. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 3.					
2. The symbol USB_HV_{IN}, in this case, represents the USB_HV_{IN} symbol referenced in Table 3					
3. For recommended operating conditions, see Table 3					

3.13.2 USB 2.0 AC timing specifications

This section describes the AC timing specifications for the on-chip USB PHY. See Chapter 7 in the *Universal Serial Bus Revision 2.0 Specification* for more information.

3.14 USB 3.0 interface

This section describes the DC and AC electrical specifications for the USB 3.0 interface.

3.14.1 USB 3.0 DC electrical characteristics

This table provides the USB 3.0 transmitter (Tx) DC electrical characteristics at package pins.

Table 37. USB 3.0 transmitter DC electrical characteristics[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800	1000	1200	$mV_{p\text{-}p}$
Low power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400	—	1200	$mV_{p\text{-}p}$
Transmitter de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3	—	4	dB
Differential impedance	Z_{diffTX}	72	100	120	Ω
Transmitter common mode impedance	$R_{TX\text{-}DC}$	18	—	30	Ω
Absolute DC common mode voltage between U1 and U0	$T_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$	—	—	200	mV
DC electrical idle differential output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0	—	10	mV
Note:					
1. For recommended operating conditions, see Table 3.					

This table provides the USB 3.0 receiver DC electrical characteristics at the recieve package pins.

Table 38. USB 3.0 receiver DC electrical characteristics

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Differential receiver input impedance	$R_{RX-DIFF-DC}$	72	100	120	Ω	—
Receiver DC common mode impedance	R_{RX-DC}	18	—	30	Ω	—
DC input CM input impedance for V > 0 during reset or power down	$Z_{RX-HIGH-IMP-DC}$	25 K	—	—	Ω	—
LFPS detect threshold	$V_{RX-IDLE-DET-DC-DIFFpp}$	100	—	300	mV	1
Note: 1. Below the minimum is noise. Must wake up above the maximum.						

3.14.2 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 39. USB 3.0 transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Speed	—	—	5.0	—	Gb/s	—
Transmitter eye	t_{TX-Eye}	0.625	—	—	UI	—
Unit interval	UI	199.94	—	200.06	ps	2
AC coupling capacitor	AC coupling capacitor	75	—	200	nF	—
Note: 1. For recommended operating conditions, see Table 3. 2. UI does not account for SSC-caused variations.						

This table provides the USB 3.0 receiver AC timing specifications at recieve package pins.

Table 40. USB 3.0 receiver AC timing specifications[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit interval	UI	199.94	—	200.06	ps	2
Notes: 1. For recommended operating conditions, see Table 3. 2. UI does not account for SSC-caused variations.						

3.14.3 USB 3.0 LFPS specifications

This table provides the key LFPS electrical specifications at the transmitter.

Table 41. LFPS electrical specifications at the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Period	tPeriod	20	—	100	ns	—
Peak-to-peak differential amplitude	$V_{TX-DIFF-PP-LFPS}$	800	—	1200	mV	—
Low-power peak-to-peak differential amplitude	$V_{TX-DIFF-PP-LFPS-LP}$	400	—	600	mV	—
Rise/fall time	$t_{RiseFall2080}$	—	—	4	ns	1
Duty cycle	Duty cycle	40	—	60	%	1
Note: 1. Measured at compliance TP1. See Figure 24 for details.						

This figure shows the transmitter normative setup with reference channel as per USB 3.0 specifications.

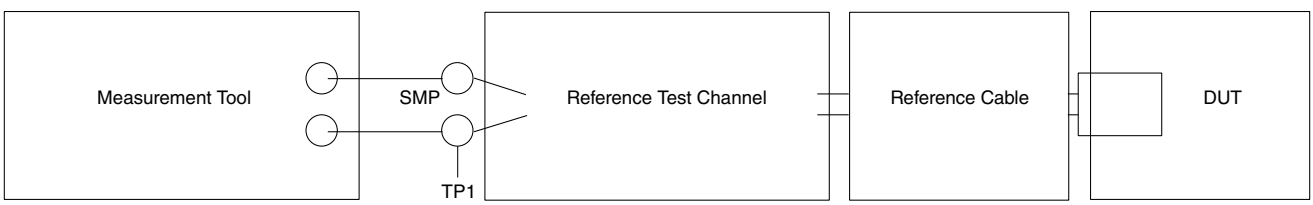


Figure 24. Transmitter normative setup

3.15 Integrated flash controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.15.1 Integrated flash controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at OV_{DD} = 1.8 V.

Table 42. Integrated flash controller DC electrical characteristics (OV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.2	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1

Table continues on the next page...

Table 42. Integrated flash controller DC electrical characteristics (OV_{DD} = 1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Note
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.32	V	-

NOTE:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.15.2 Integrated flash controller AC timing specifications

This section describes the AC timing specifications for the integrated flash controller.

3.15.2.1 Test Condition

This figure provides the AC test load for the integrated flash controller.

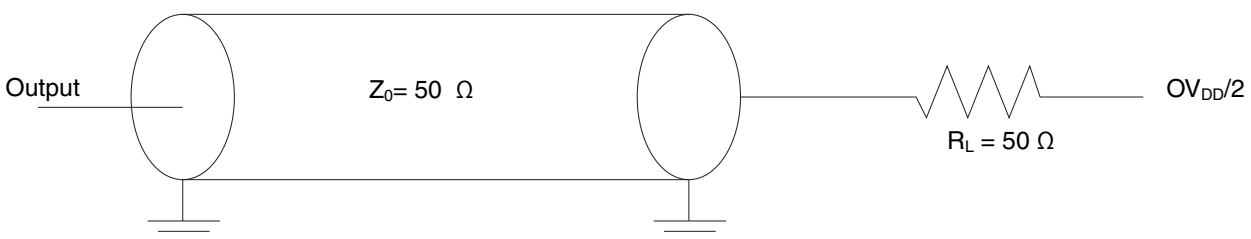


Figure 25. Integrated Flash Controller AC Test Load

3.15.2.2 IFC AC timing specifications (GPCM/GASIC)

This table describes the input AC timing specifications of the IFC-GPCM and IFC-GASIC interface.

Table 43. Integrated flash controller input timing specifications for GPCM and GASIC mode (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	-	ns	-
Input hold	$t_{IBIXKH1}$	1	-	ns	-

NOTE:

1. For recommended operating conditions, see Table 3.

This figure shows the input AC timing diagram for IFC-GPCM, IFC-GASIC interface.

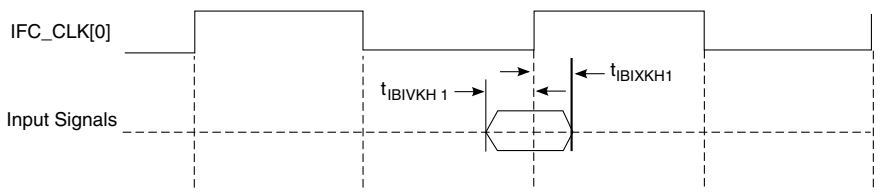


Figure 26. IFC-GPCM, IFC-GASIC input AC timings

This table describes the output AC timing specifications of IFC-GPCM and IFC-GASIC interface.

Table 44. Integrated flash controller IFC-GPCM and IFC-GASIC interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	-
Output delay	$t_{IBKLOV1}$	-	1.59	ns	-
Output hold	t_{IBKLOX}	-	-2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	-

NOTE:

1. Output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 3.

This figure shows the output AC timing diagram for IFC-GPCM, IFC-GASIC interface.

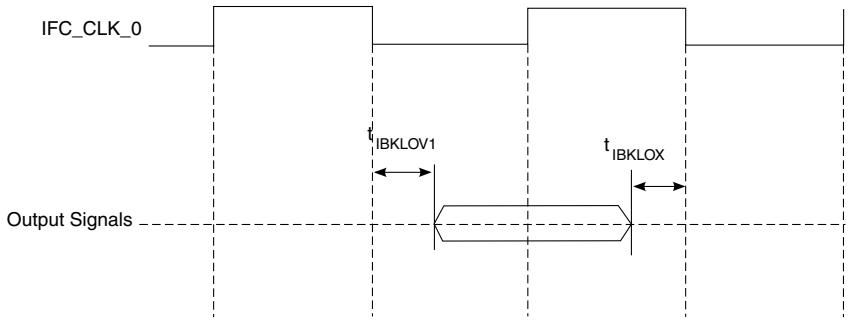


Figure 27. IFC-GPCM, IFC-GASIC signals

3.15.2.3 IFC AC timing specifications (NOR)

This table describes the input timing specifications of the IFC-NOR interface.

Table 45. Integrated Flash Controller input timing specifications for NOR mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	(2 x t_{IP_CLK}) + 2	—	ns	1
Input hold	$t_{IBIXKH2}$	(1 x t_{IP_CLK}) + 1	—	ns	1

Notes:

1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.
2. For recommended operating conditions, see Table 3.
3. The NOR flash state machine will de-assert OE_B once the flash controller samples data. Hold time given in the datasheet tIBIXKH2 is not a requirement for customer but rather an information used internally for test purpose.

This figure shows the AC input timing diagram for input signals of IFC-NOR interface. Here TRAD is a programmable delay parameter. See the IFC section of the reference manual for more information.

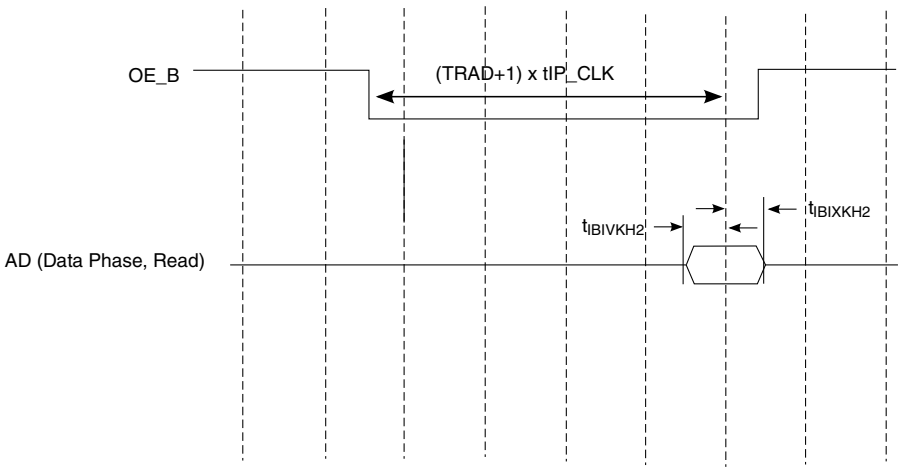


Figure 28. IFC-NOR Interface input AC timings

This table describes the output AC timing specifications of IFC-NOR interface.

Table 46. Integrated Flash Controller IFC-NOR interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	—	±1.5	ns	1

Notes:

1. This effectively means that a signal change may appear anywhere within $\pm t_{IBKLOV2}$ (max) duration, from the point where it's expected to change.
2. For recommended operating conditions, see Table 3.

This figure shows the AC timing diagram for output signals of IFC-NOR interface. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. In a read operation, OE_B is supposed to change TACO (a programmable delay, see the IFC section of the reference manual for more information) time after CS_B. Because of skew between the signals, OE_B may change anywhere within the time window defined by $t_{IBKLOV2}$. This concept applies to other output signals of IFC-NOR interface, as well. The figure is an example to show the skew between any two chronological toggling signals as per the protocol. Here is the list of IFC-NOR output signals: NRALE, NRAVD_B, NRWE_B, NROE_B, CS_B, AD(Address phase).

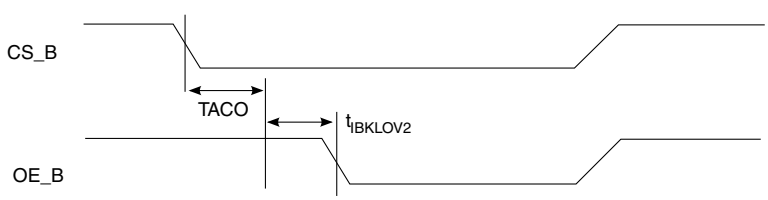


Figure 29. IFC-NOR interface output AC timings

3.15.2.4 IFC AC timing specifications (NAND)

This table describes the input timing specifications of the IFC-NAND interface.

Table 47. Integrated flash controller input timing specifications for NAND mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH3}$	1	-	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	-	t_{IP_CLK}	1
NOTE: 1. t_{IP_CLK} is the period of IP clock on which the IFC is running. 2. For recommended operating conditions, see Table 3.					

This figure shows the AC input timing diagram for IFC-NAND interface input signals. Note that TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

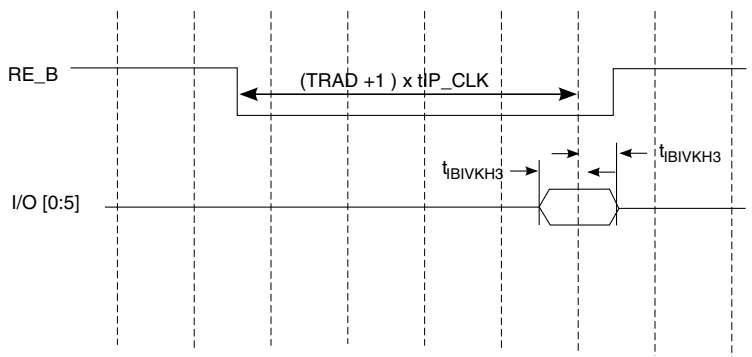


Figure 30. IFC-NAND interface input AC timing diagram

NOTE

t_{IP_CLK} is the period of the IP clock (not the IFC_CLK) on which the IFC is running.

This table describes the output AC timing specifications for the IFC-NAND interface.

Table 48. Integrated flash controller IFC-NAND interface output timing specifications (V_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	-	±1.55	ns	1
NOTE:					

Table 48. Integrated flash controller IFC-NAND interface output timing specifications (V_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
1. This effectively means that a signal change may appear anywhere within $t_{IBKLOV3}$ (min) to $t_{IBKLOV3}$ (max) duration, from the point where it is expected to change. 2. For recommended operating conditions, see Table 3.					

This figure shows the AC timing diagram for output signals of the IFC-NAND interface. The timing specifications illustrated here are derived by taking timings between two signals, for example, CS_B and CLE. CLE is expected to change TCCST (a programmable delay) time after CS_B. For more information, see the IFC section of the chip reference manual. Because of skew between the signals, CLE may change anywhere within the time window defined by $t_{IBKLOV3}$. This concept applies to other output signals of the IFC-NAND interface as well. The diagram is an example that shows the skew between any two chronological toggling signals, as per the protocol. The list of output signals is as follows: NDWE_B, NDRE_B, NDALE, WP_B, NDCLE, CS_B, and AD.

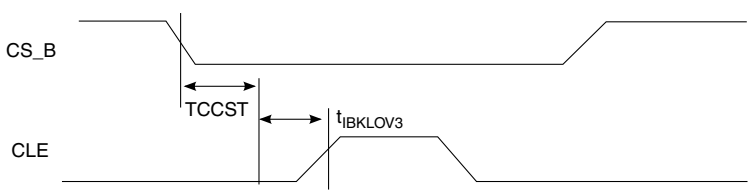


Figure 31. IFC-NAND interface output AC timing diagram

3.15.2.5 IFC-NAND SDR AC timing specifications

This table describes the AC timing specifications for the IFC-NAND SDR interface. These specifications are compliant with the SDR mode for ONFI specification revision 3.0.

Table 49. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OV_{DD} = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Fig
Address cycle to data loading time	tADL	O	TADLE - 1.5(ns)	TADLE + 1.5(ns)	t_{IP_CLK}	Figure 32
ALE hold time	tALH	O	TWCHT - 1.5(ns)	TWCHT + 1.5(ns)	t_{IP_CLK}	Figure 34
ALE setup time	tALS	O	TWP - 1.5(ns)	TWP + 1.5(ns)	t_{IP_CLK}	Figure 34

Table continues on the next page...

Table 49. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OV_{DD} = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Fig
ALE to RE_n delay	tAR	O	TWHRE - 1.5(ns)	TWHRE + 1.5(ns)	t_{IP_CLK}	Figure 35
CE_n hold time	tCH	O	5 + 1.5(ns)	-	ns	Figure 33
CE_n high to input hi-Z	tCHZ	I	TRHZ - 1.5(ns)	TRHZ + 1.5(ns)	t_{IP_CLK}	Figure 36
CLE hold time	tCLH	O	TWCHT - 1.5(ns)	TWCHT + 1.5(ns)	t_{IP_CLK}	Figure 34
CLE to RE_n delay	tCLR	O	TWHRE - 1.5(ns)	TWHRE - 1.5(ns)	t_{IP_CLK}	Figure 37
CLE setup time	tCLS	O	TWP - 1.5(ns)	TWP + 1.5(ns)	t_{IP_CLK}	Figure 34
CE_n high to input hold	tCOH	I	150 - 1.5(ns)	-	ns	Figure 36
CE_n setup time	tCS	O	TCS - 1.5(ns)	TCS + 1.5(ns)	t_{IP_CLK}	Figure 34
Data hold time	tDH	O	TWCHT - 1.5(ns)	TWCHT + 1.5(ns)	t_{IP_CLK}	Figure 34
Data setup time	tDS	O	TWP - 1.5(ns)	TWP + 1.5(ns)	t_{IP_CLK}	Figure 34
Busy time for Set Features and Get Features	tFEAT	O	-	FTOCNT	t_{IP_CLK}	Figure 38
Output hi-Z to RE_n low	tIR	O	TWHRE - 1.5(ns)	TWHRE + 1.5(ns)	t_{IP_CLK}	Figure 39
Interface and Timing Mode Change time	tITC	O	-	FTOCNT	t_{IP_CLK}	Figure 38
RE_n cycle time	tRC	O	TRP + TREH - 1.5(ns)	TRP + TREH + 1.5(ns)	t_{IP_CLK}	Figure 36
RE_n access time	tREA	I	-	(TRAD - 1) + 2(ns)	t_{IP_CLK}	Figure 36
RE_n high hold time	tREH	I	TREH	TREH	t_{IP_CLK}	Figure 36
RE_n high to input hold	tRHOH	I	0	-	ns	Figure 36
RE_n high to WE_n low	tRHW	O	100 + 1.5(ns)	-	ns	Figure 40
RE_n high to input hi-Z	tRHZ	I	TRHZ - 1.5(ns)	TRHZ + 1.5(ns)	t_{IP_CLK}	Figure 36
RE_n low to input data hold	tRLOH	I	0	-	ns	Figure 41
RE_n pulse width	tRP	O	TRP	TRP	t_{IP_CLK}	Figure 36
Ready to data input cycle (data only)	tRR	O	TRR - 1.5(ns)	TRR + 1.5(ns)	t_{IP_CLK}	Figure 36
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	tRST (raw NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 42
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	tRST2 (EZ NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 42
(WE_n high or CLK rising edge) to SR[6] low	tWB	O	TWBE + TWH - 1.5(ns)	TWBE + TWH + 1.5(ns)	t_{IP_CLK}	Figure 34
WE_n cycle time	tWC	O	TWP + TWH	TWP + TWH	t_{IP_CLK}	Figure 43
WE_n high hold time	tWH	O	TWH	TWH	t_{IP_CLK}	Figure 43

Table continues on the next page...

Table 49. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OV_{DD} = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Fig
Command, address, or data input cycle to data output cycle	tWHR	O	TWHRE + TWH - 1.5(ns)	TWHRE + TWH + 1.5(ns)	t_{IP_CLK}	Figure 44
WE_n pulse width	tWP	O	TWP	TWP	t_{IP_CLK}	Figure 34
WP_n transition to command cycle	tWW	O	TWW - 1.5(ns)	TWW + 1.5(ns)	t_{IP_CLK}	Figure 45
Data Input hold	tIBIXKH4	I	1	-	t_{IP_CLK}	Figure 46

NOTE:

1. t_{IP_CLK} is the clock period of IP clock (on which IFC IP is running). Note that that the IFC IP clcok doesn't come out of device.

2. For the definition of parameters (like TADL) mentioned in min/max columns check the IFC section of the device's reference manual.

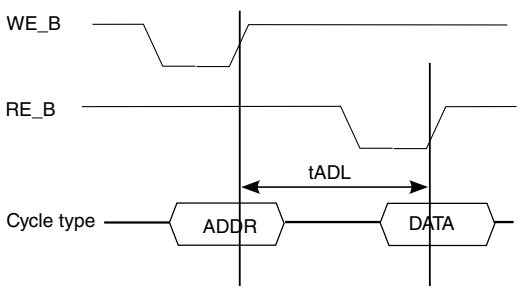


Figure 32. tADL timing

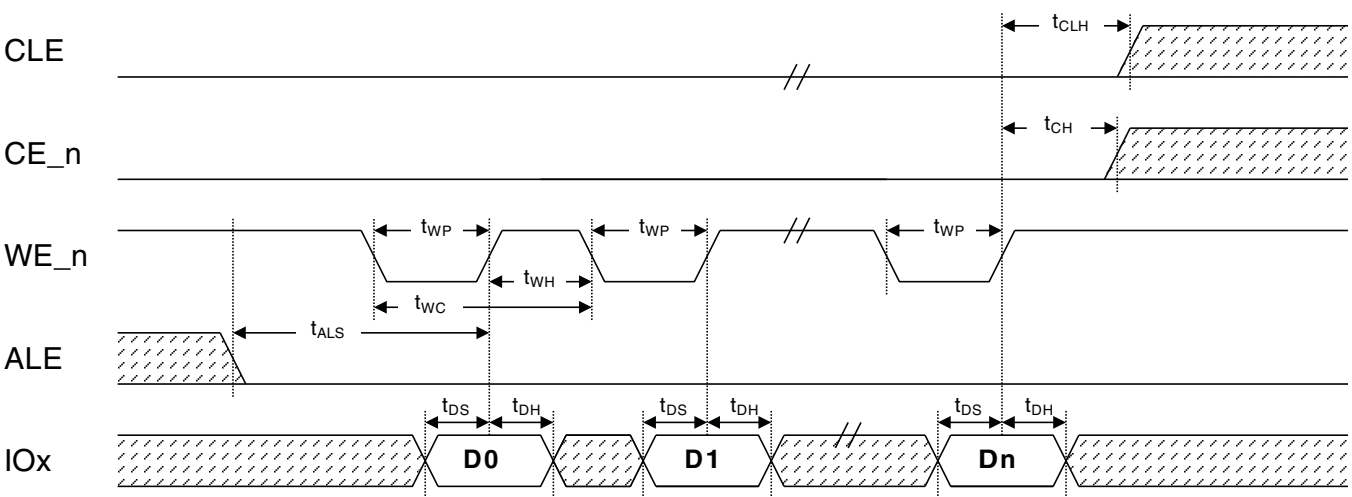


Figure 33. Data output cycle timings

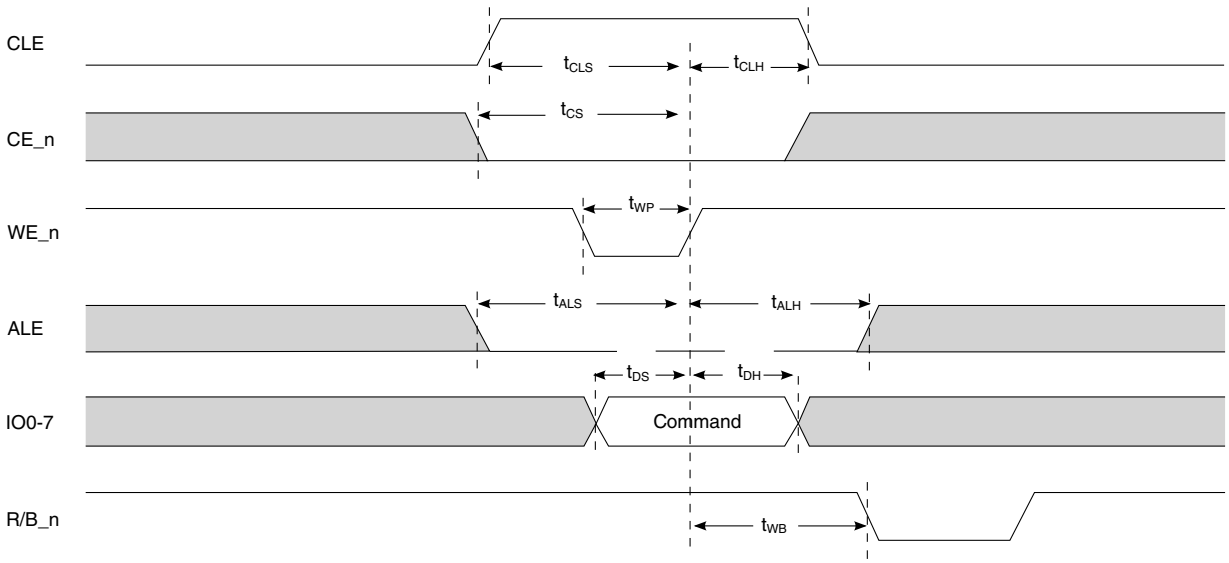


Figure 34. Command cycle

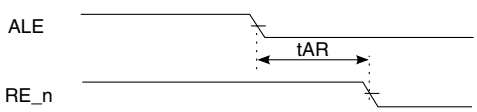


Figure 35. tAR timings

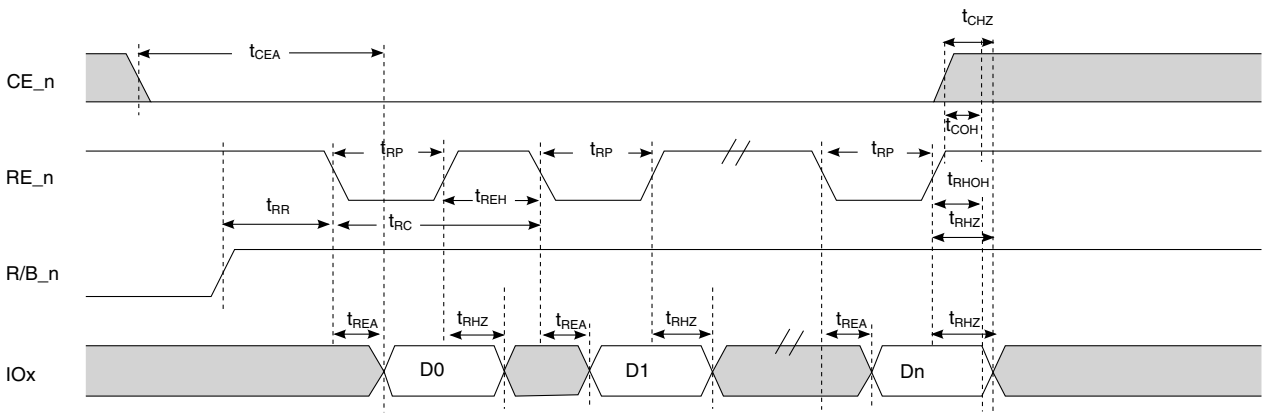


Figure 36. Data input cycle timings

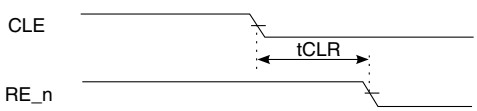


Figure 37. tCLR timings

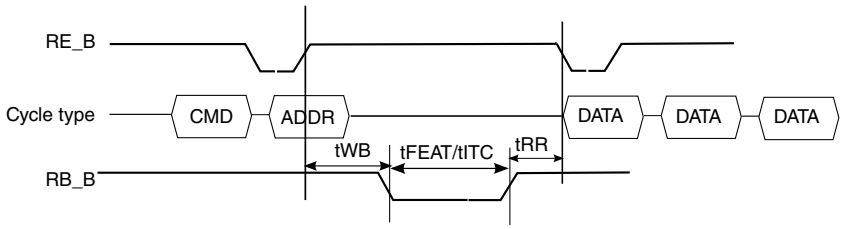


Figure 38. tWB, tFEAT, tITC, tRR timings

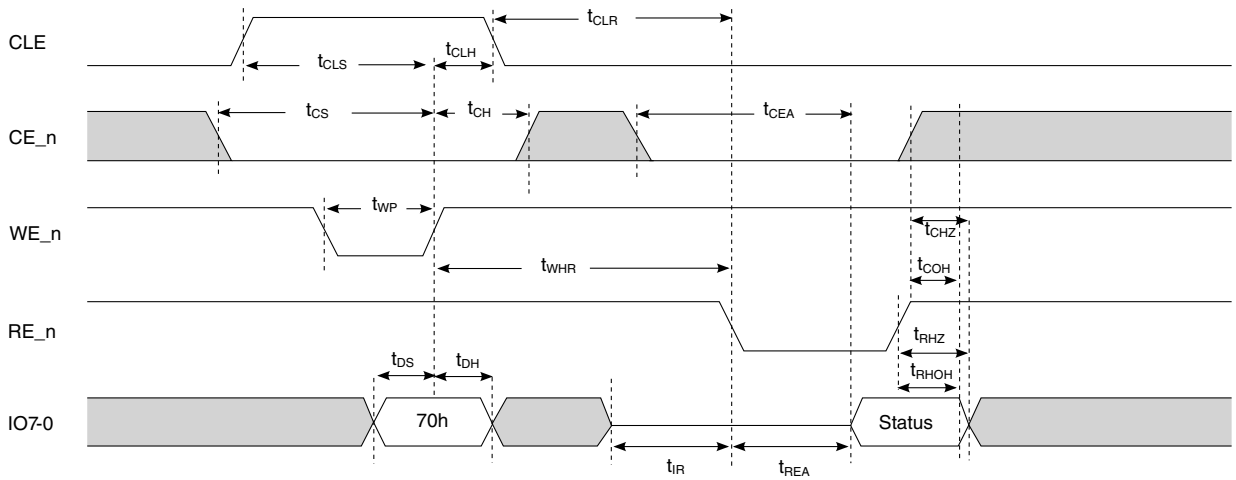


Figure 39. Read status timings

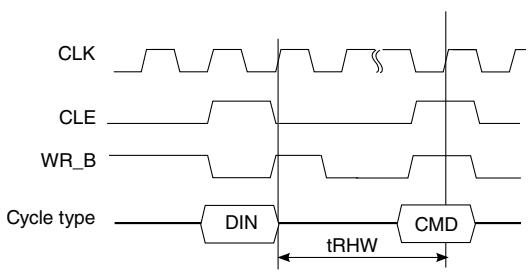


Figure 40. tRHW timings

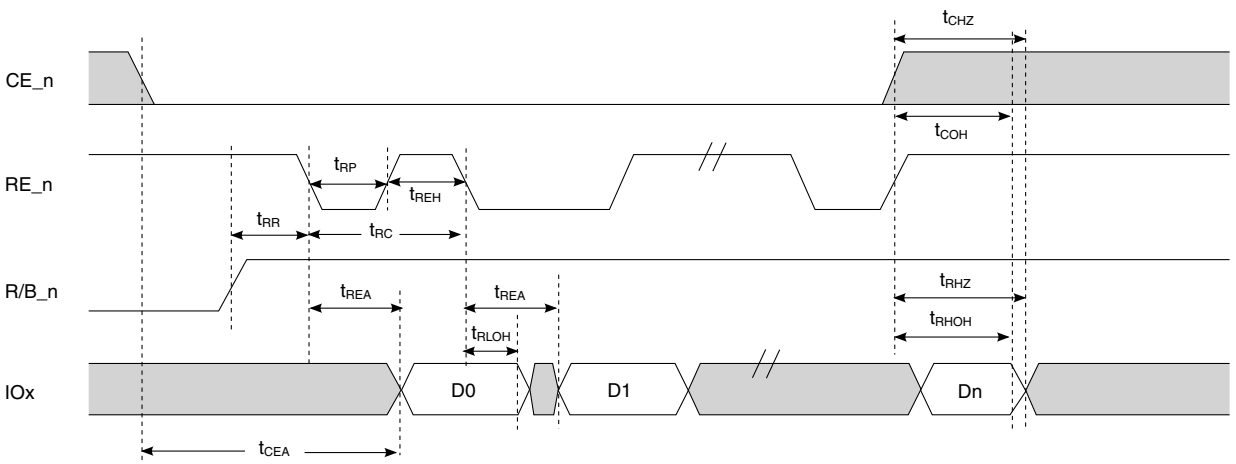


Figure 41. EDO mode data input cycle timings

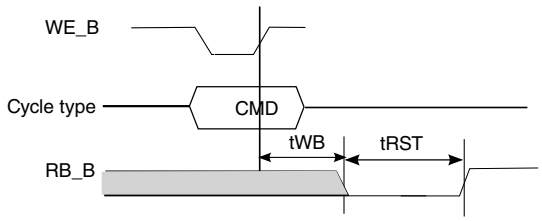


Figure 42. tWB, tRST timings

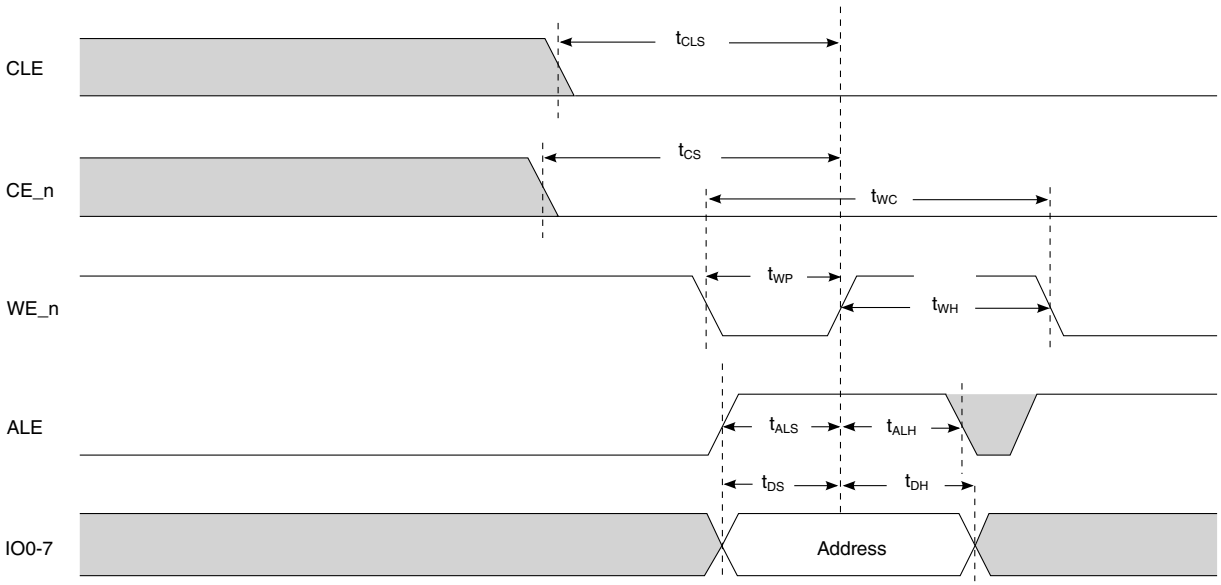


Figure 43. Address latch timings

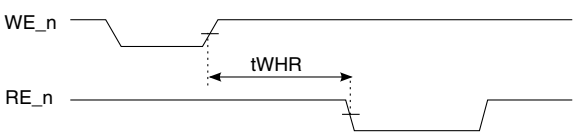


Figure 44. tWHR timings

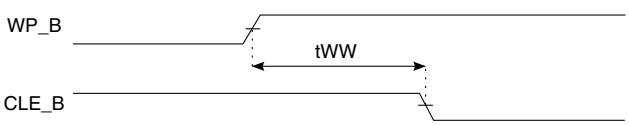


Figure 45. tWW timings

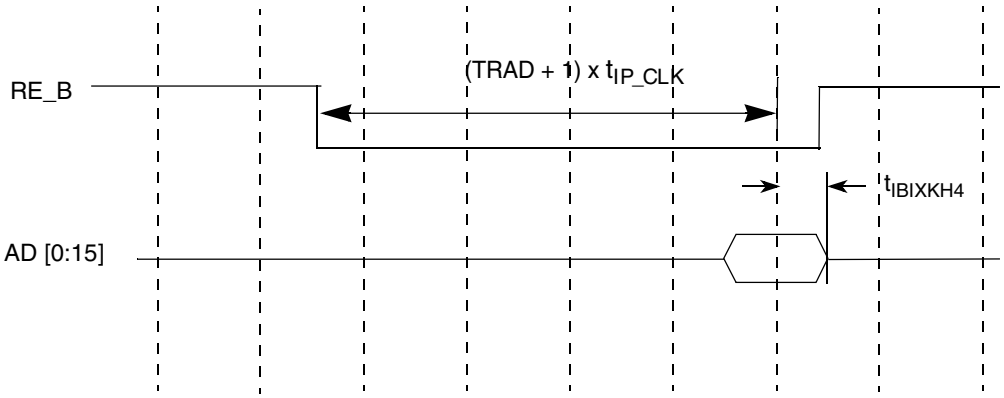


Figure 46. tIBIXKH4 timings

3.15.2.6 IFC-NAND NVDDR AC timing specification

Table below describes the AC timing specifications of IFC-NAND NVDDR interface. These specifications are compliant to NVDDR mode of ONFI specification revision 3.0.

Table 50. Integrated Flash Controller IFC-NAND NVDDR interface AC timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	I/O	Min	Max	Unit	Fig
Access window of DQ[7:0] from CLK	tAC	I	3 - 150 (ps)	20 + 150 (ps)	ns	Figure 50
Address cycle to data loading time	tADL	I	TADL	—	t_{IP_CLK}	Figure 51
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) Fast	tCADf	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}	Figure 47
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) slow	tCADs	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}	Figure 47
Command/address DQ hold time	tCAH	O	2 + 150 (ps)	—	ns	Figure 47
CLE and ALE hold time	tCALH	O	2 + 150 (ps)	—	ns	Figure 47
CLE and ALE setup time	tCALS	O	2 + 150 (ps)	—	ns	Figure 47
Command/address DQ setup time	tCAS	O	2 + 150 (ps)	—	ns	Figure 47
CE# hold time	tCH	O	2 + 150 (ps)	—	ns	Figure 47
Average clock cycle time, also known as tCK	tCK(avg) or tCK	O	10	—	ns	Figure 47
Absolute clock period, measured from rising edge to the next consecutive rising edge	tCK(abs)	O	tCK(avg) + tJIT(per) min	tCK(avg) + tJIT(per) max	ns	Figure 47
Clock cycle high	tCKH(abs)	O	0.45	0.55	tCK	Figure 47

Table continues on the next page...

Table 50. Integrated Flash Controller IFC-NAND NVDDR interface AC timing specifications (OV_{DD} = 1.8 V)[2] (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Fig
Clock cycle low	tCKL(abs)	O	0.45	0.55	tCK	Figure 47
Data input end to W/R# high B16	tCKWR	O	TCKWR - 150 (ps)	TCKWR + 150 (ps)	t_{IP_CLK}	Figure 50
CE# setup time	tCS	O	TCS - 150 (ps)	TCS + 150 (ps)	t_{IP_CLK}	Figure 49
Data DQ hold time	tDH	O	1050	—	ps	Figure 49
Access window of DQS from CLK	tDQSCK	I	—	20 + 150 (ps)	ns	Figure 50
W/R# low to DQS/DQ driven by device	tDQSD	I	-150 (ps)	18 + 150 (ps)	ns	Figure 50
DQS output high pulse width	tDQSH	O	0.45	0.55	tCK	Figure 49
W/R# high to DQS/DQ tri-state by device	tDQSHZ	O	RHZ - 150 (ps)	RHZ + 150 (ps)	t_{IP_CLK}	Figure 47
DQS output low pulse width	tDQSL	O	0.45	0.55	tCK	Figure 49
DQS-DQ skew, DQS to last DQ valid, per access	tDQSQ	I	—	1000	ps	Figure 50
Data output to first DQS latching transition	tDQSS	O	0.75 + 150 (ps)	1.25 - 150 (ps)	tCK	Figure 49
Data DQ setup time	tDS	O	1050	—	ps	Figure 49
DQS falling edge to CLK rising - hold time	tDSH	O	0.2 + 150 (ps)	—	tCK	Figure 49
DQS falling edge to CLK rising - setup time	tDSS	O	0.2 + 150 (ps)	—	tCK	Figure 49
Input data valid window	tDVW	I	tDVW = tQH - tDQSQ	—	ns	Figure 50
Busy time for Set Features and Get Features	tFEAT	I	—	FTOCNT	t_{IP_CLK}	Figure 52
Half-clock period	tHP	O	tHP = min(tCKL, tCKH)	—	ns	Figure 50
Interface and Timing Mode Change time	tITC	I	—	FTOCNT	t_{IP_CLK}	Figure 52
The deviation of a given tCK(abs) from tCK(avg)	tJIT(per)	O	-0.5	0.5	ns	NA
DQ-DQS hold, DQS to first DQ to go non-valid, per access	tQH	I	tQH = tHP - tQHS	—	t_{IP_CLK}	Figure 50
Data hold skew factor	tQHS	I	-	1 + 150(ps)	ns	NA
Data input cycle to command, address, or data output cycle	tRHW	O	TRHW	—	t_{IP_CLK}	Figure 53
Ready to data input cycle (data only)	tRR	I	TRR	—	t_{IP_CLK}	Figure 52
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	tRST (raw NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 54
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	tRST2 (EZ NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 54

Table continues on the next page...

Table 50. Integrated Flash Controller IFC-NAND NVDDR interface AC timing specifications (OV_{DD} = 1.8 V)[2] (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Fig
CLK rising edge to SR[6] low	tWB	O	TWB - 150 (ps)	TWB + 150 (ps)	t_{IP_CLK}	Figure 54
Command, address or data output cycle to data input cycle	tWHR	O	TWHR	—	t_{IP_CLK}	Figure 55
DQS write preamble	tWPRE	O	1.5	—	tCK	Figure 49
DQS write postamble	tWPST	O	1.5	—	tCK	Figure 49
W/R# low to data input cycle	tWRCK	I	TWRCK - 150 (ps)	TWRCK + 150 (ps)	t_{IP_CLK}	Figure 50
WP# transition to command cycle	tWW	O	TWW - 150 (ps)	TWW + 150 (ps)	t_{IP_CLK}	Figure 56

NOTE:

1. t_{IP_CLK} is the clock period of IP clock (on which IFC IP is running). Note that that the IFC IP clcok doesn't come out of device.

2. For the definition of parameters (like TADL) mentioned in min/max columns check the IFC section of the device's reference manual.

Following diagrams show the AC timing diagram for IFC-NAND NVDDR interface.

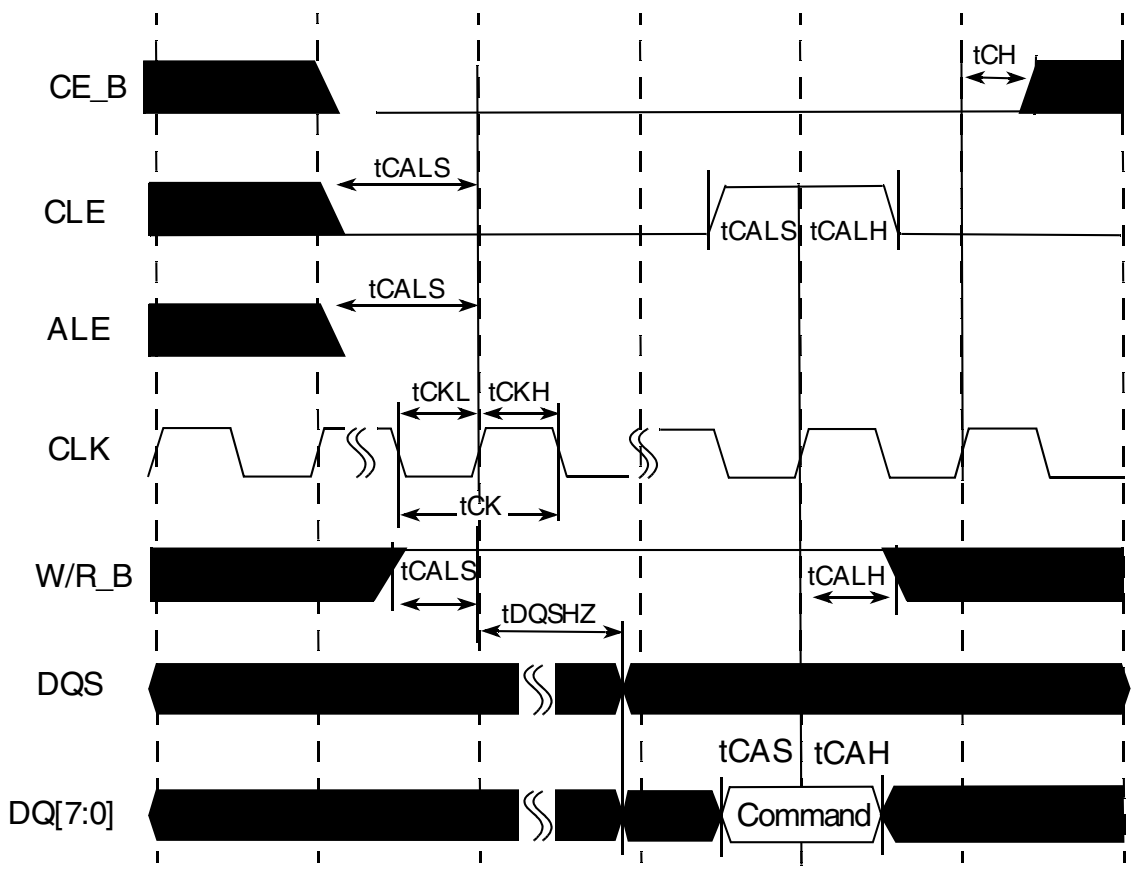


Figure 47. Command cycle

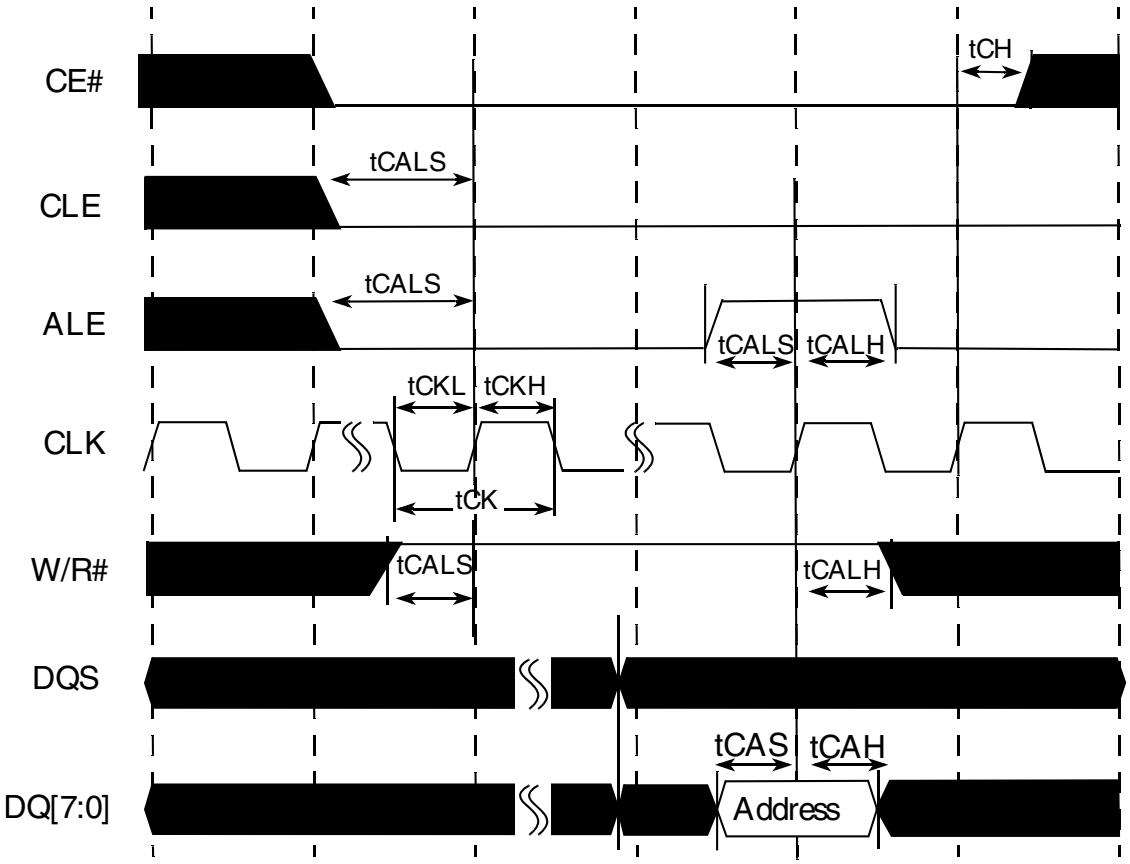


Figure 48. Address cycle

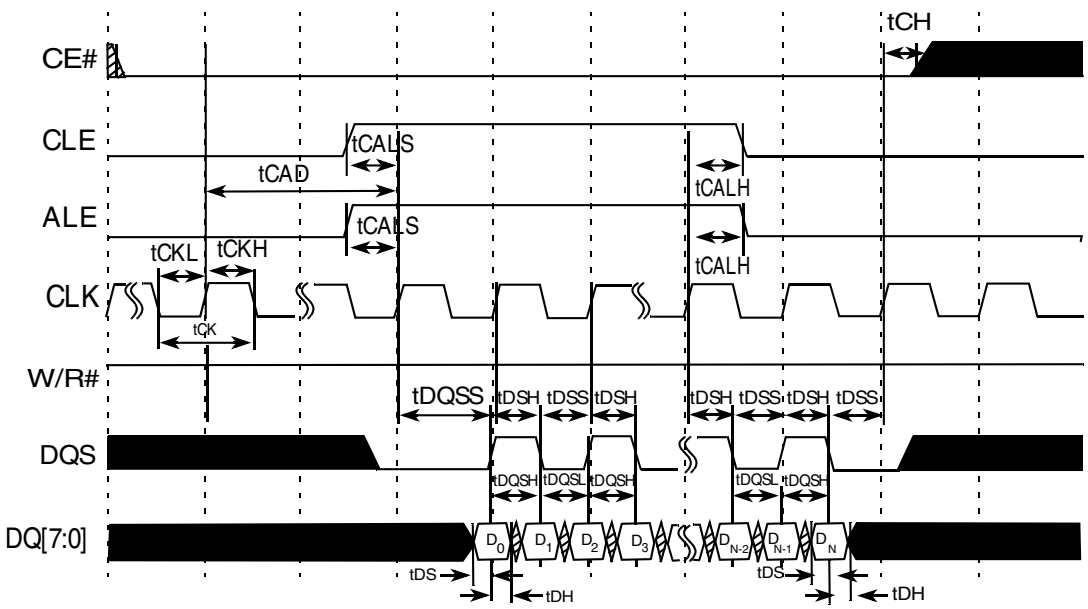


Figure 49. Write cycle

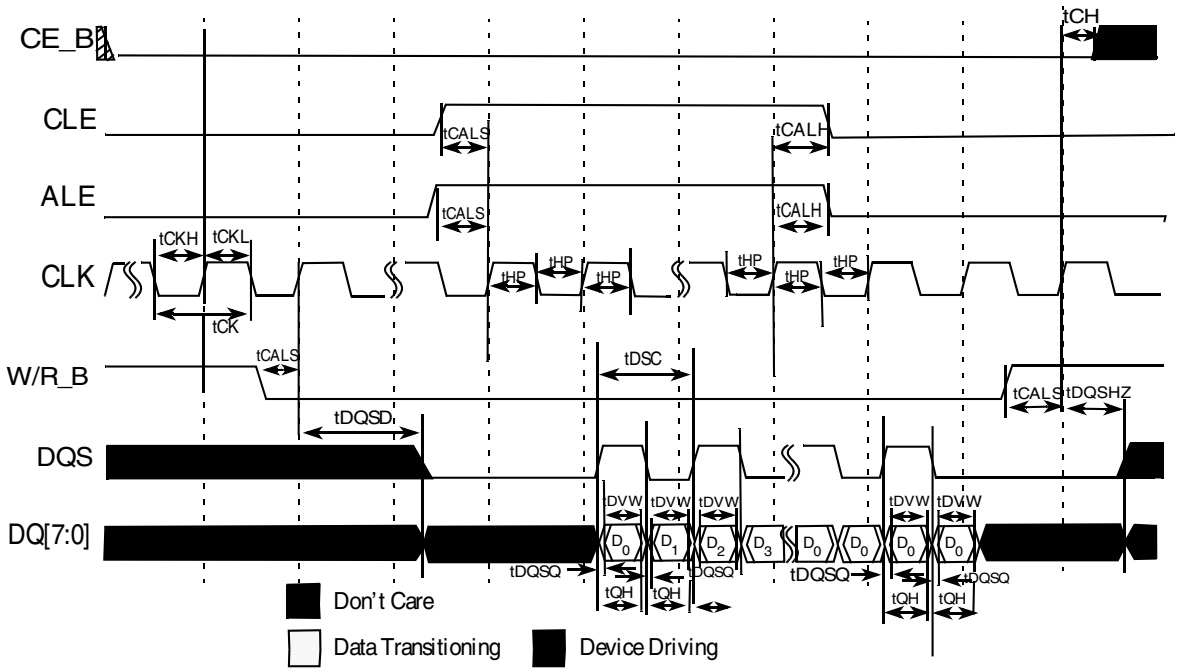


Figure 50. Read cycle

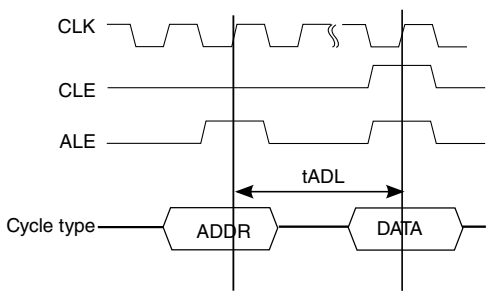


Figure 51. tADL timings

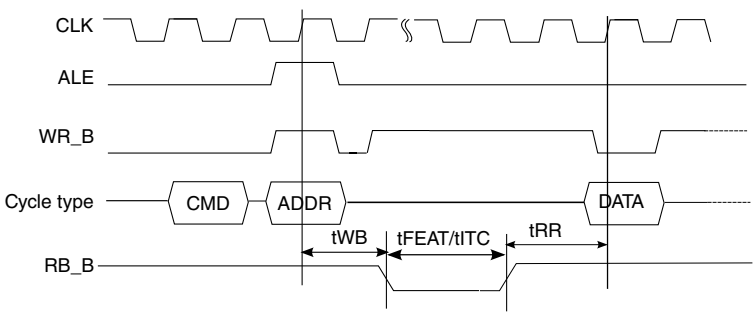


Figure 52. tWB, tFEAT, tITC, tRR timings

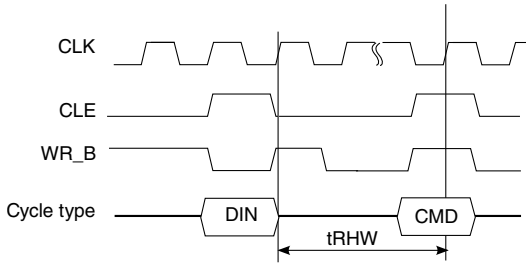


Figure 53. tRHW timings

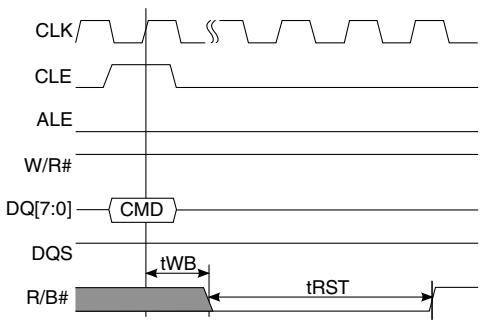


Figure 54. tWB, tRST timings

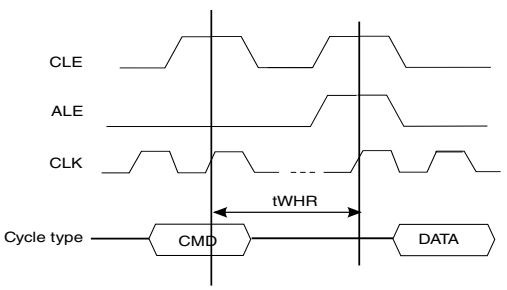


Figure 55. tWHR timings

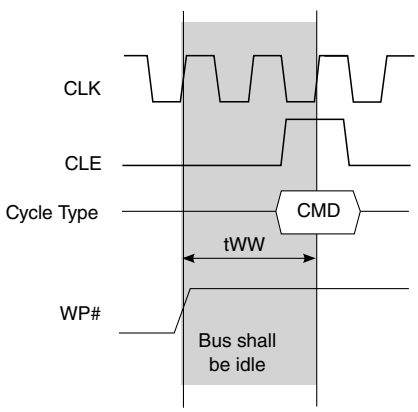


Figure 56. tWW timings

3.16 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.16.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 51. eSDHC interface DC electrical characteristics (dual-voltage cards)[3]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.7 x OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	1
Input/Output leakage current	I_{IN}/I_{OZ}	—	-50	50	µA	—
Output high voltage	V_{OH}	I_{OH} = -100 µA at OV_{DD} min	OV_{DD} - 0.2 V	—	V	—
Output low voltage	V_{OL}	I_{OL}= 100 µA at OV_{DD} min	—	0.2	V	—
Output high voltage	V_{OH}	I_{OH} = -100 mA	OV_{DD} - 0.2	-	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	-	0.3	V	2

1. The min V_{IL} and V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. Open-drain mode is for MMC cards only.

3. For recommended operating conditions, see Table 3.

3.16.2 eSDHC AC timing specifications

Table 52. eSDHC AC timing specifications[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/high-speed mode MMC Full-speed/high-speed mode	f_{SHSCK}	0	25/50 20/52	MHz	2, 4
SD_CLK clock low time-Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time-Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	2.5	—	ns	3, 4, 5
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	4, 5
Output hold time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOX}$	-3	—	ns	4, 5
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	—	3	ns	4, 5
Notes:					

Table 52. eSDHC AC timing specifications[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). 2. In full-speed mode, the clock frequency value can be 0-25 MHz for an SD/SDIO card and 0-20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50 MHz for an SD/SDIO card and 0-52 MHz for an MMC card. 3. To satisfy setup timing, one-way board-routing delay between Host and Card, on SD_CLK, SD_CMD, and SD_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SD_CLK, SD_CMD, and SD_DATx should not exceed 1.5ns. 4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF. 5. The parameter values apply to both full-speed and high-speed modes. 6. For recommended operating conditions, see Table 3.					

This figure provides the eSDHC clock input timing diagram.

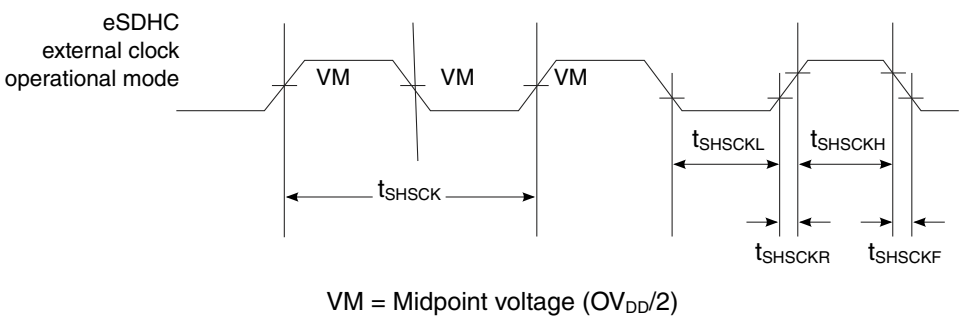
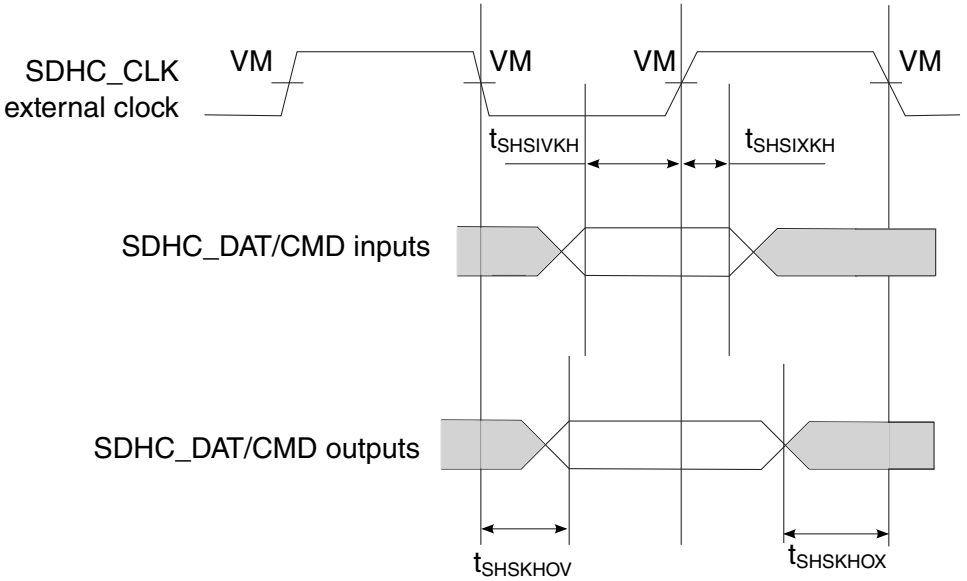


Figure 57. eSDHC clock input timing diagram

This figure provides the data and command input/output timing diagram.



VM = Midpoint voltage ($OV_{DD}/2$)

Figure 58. eSDHC data and command input/output timing diagram referenced to clock

This table provides the eSDHC AC timing specifications for eMMC HS200 mode.

Table 53. eSDHC AC timing specifications (eMMC HS200)

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHCK}	-	200	MHz	-
SDHC_CLK clock rise and fall times	t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	T_{SHKHOX}	1.6	-	ns	1
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	T_{SHKHOV}	-	2.9	ns	1
Input data window (UI)	t_{SHIDV}	0.475	-	Unit Interval	1
Notes: 1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$. 2. At recommended operating conditions with =1.8 V.					

This figure provides the eSDHC HS200 mode timing diagram.

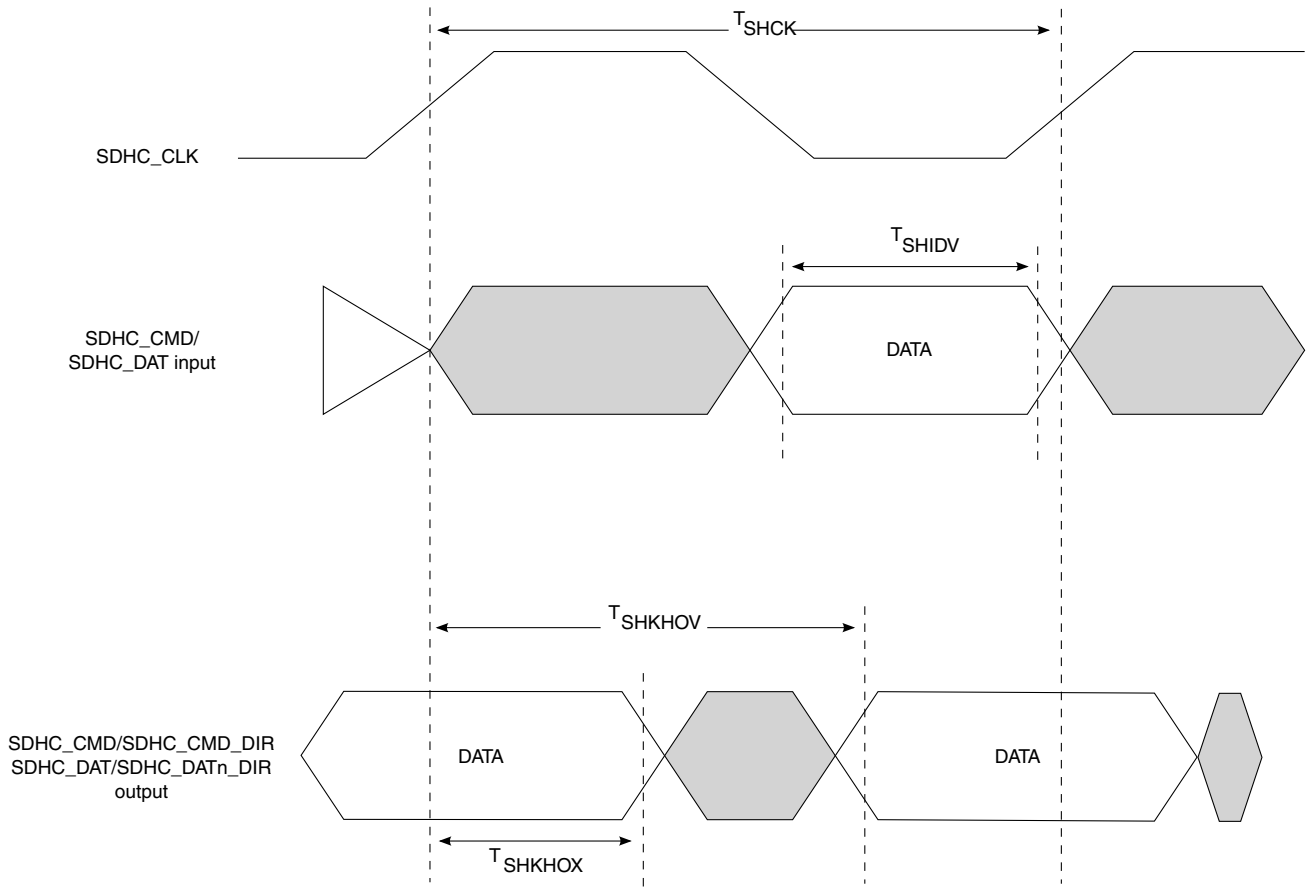


Figure 59. eSDHC HS200 mode timing diagram

3.17 Generic interrupt controller (GIC)

This section describes the DC and AC electrical specifications for the generic interrupt controller.

3.17.1 GIC DC characteristics

This figure provides the DC electrical characteristics for IRQ[0:11] and EVT[0:9]_B.

Table 54. GIC DC electrical characteristics (OV_{DD} = 1.8 V)[3]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—

Table continues on the next page...

Table 54. GIC DC electrical characteristics (OV_{DD} = 1.8 V)[3] (continued)

Characteristic	Symbol	Min	Max	Unit	Notes
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.17.2 GIC AC timing specifications

This table provides the GIC input and output AC timing specifications for IRQ[0:11] and EVT[0:9]_B.

Table 55. GIC Input AC timing specifications[2]

Characteristic	Symbol	Min	Max	Unit	Notes
GIC inputs-minimum pulse width	t_{PIWID}	3	—	SYSCLKs	1

1. GIC inputs and outputs are asynchronous to any visible clock. GIC outputs must be synchronized before use by any external synchronous logic. GIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.
2. For recommended operating conditions, see Table 3.

3.18 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.18.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 56. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	-100/+50	µA	2,4
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—

Table continues on the next page...

Table 56. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Table 3.
3. For recommended operating conditions, see Table 3.
4. TDI, TMS, TRST_B have internal pull-ups per IEEE Std 1149.1 specification.

3.18.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 60 through Figure 63.

Table 57. JTAG AC timing specifications[4]

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	—
TRST_B assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times	t_{JTKLDV}			ns	3
Boundary-scan data		—	15		
TDO		—	10		
Output hold times	t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. For recommended operating conditions, see Table 3.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

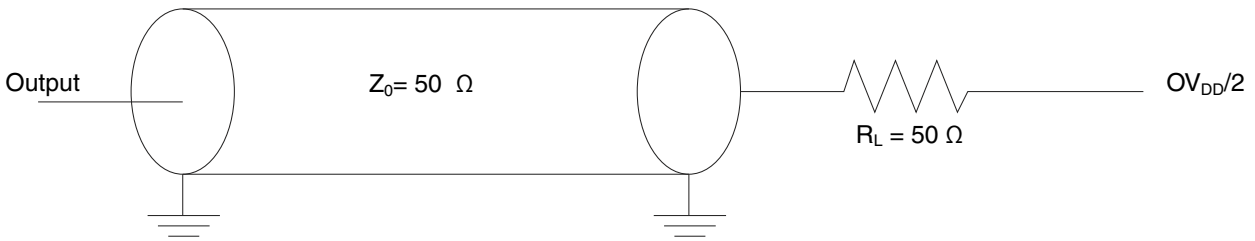


Figure 60. AC test load for the JTAG interface

This figure provides the JTAG clock input timing diagram.

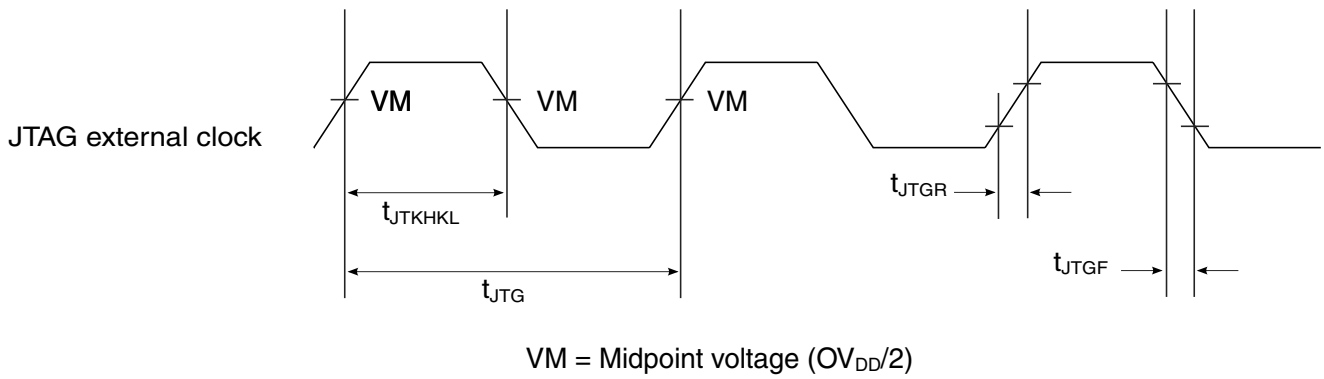


Figure 61. JTAG clock input timing diagram

This figure provides the TRST_B timing diagram.

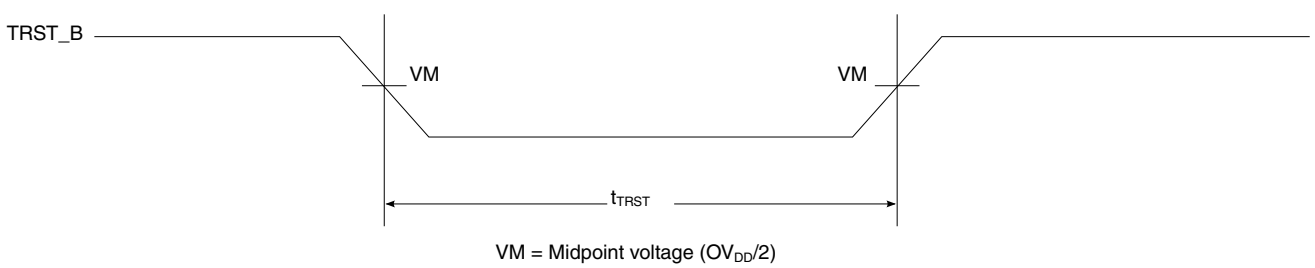


Figure 62. TRST_B timing diagram

This figure provides the boundary-scan timing diagram.

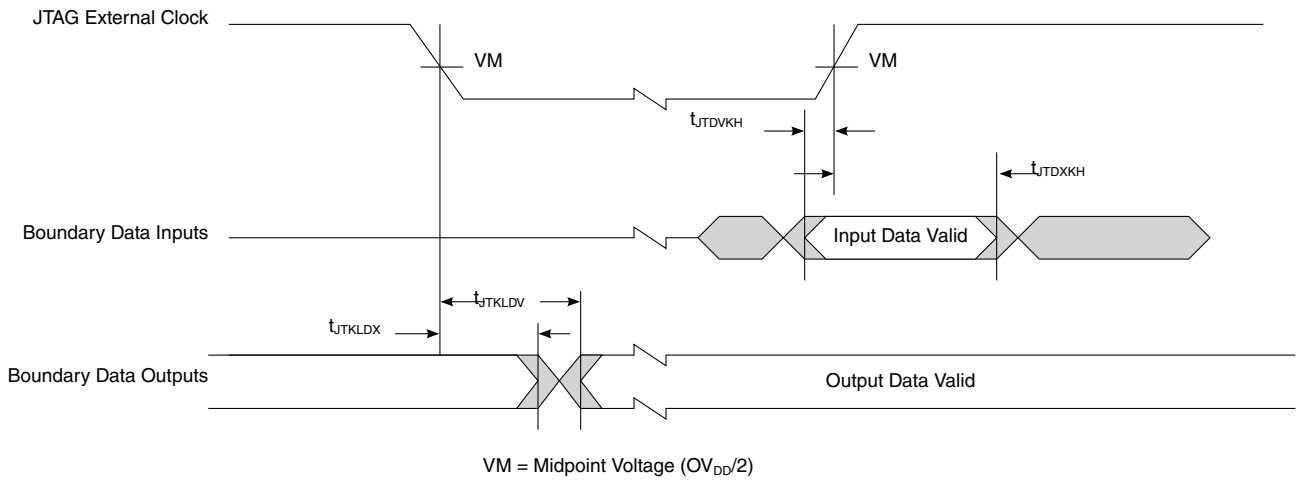


Figure 63. Boundary-scan timing diagram

3.19 I^2C interface

This section describes the DC and AC electrical characteristics for the I^2C interface.

3.19.1 I^2C DC electrical characteristics

This table provides the DC electrical characteristics for the I^2C interfaces operating at 1.8 V.

Table 58. I^2C DC electrical characteristics (OV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.36	V	
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 x OV_{DD} and 0.9 x OV_{DD}(max)	I_I	-50	50	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. See the chip reference manual for information about the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.
4. For recommended operating conditions, see Table 3.

3.19.2 I²C AC timing specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 59. I²C AC timing specifications[5]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	µs	—
High period of the SCL clock	t_{I2CH}	0.6	—	µs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time:	t_{I2DXKL}			µs	3
CBUS compatible masters		—	—		
I²C bus devices		0	—		
Data output delay time	t_{I2OVKL}	—	0.9	µs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 x OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 x OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

2. The requirements for I²C frequency calculation must be followed. See *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).

3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).

4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

5. For recommended operating conditions, see Table 3.

This figure provides the AC test load for the I²C.

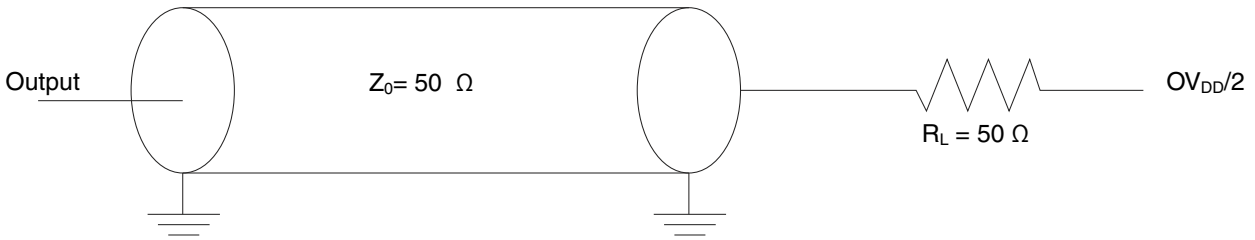


Figure 64. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

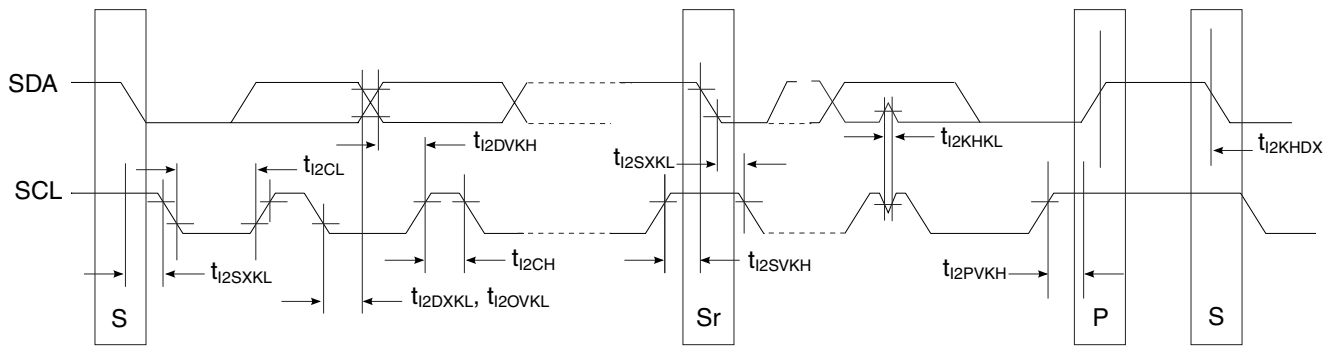


Figure 65. I²C Bus AC timing diagram

3.20 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface.

3.20.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at OV_{DD} or OV_{DD}= 1.8 V.

Table 60. GPIO DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—

Table continues on the next page...

Table 60. GPIO DC electrical characteristics (1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.20.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 61. GPIO input AC timing specifications[2]

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. For recommended operating conditions, see Table 3.

This figure provides the AC test load for the GPIO.

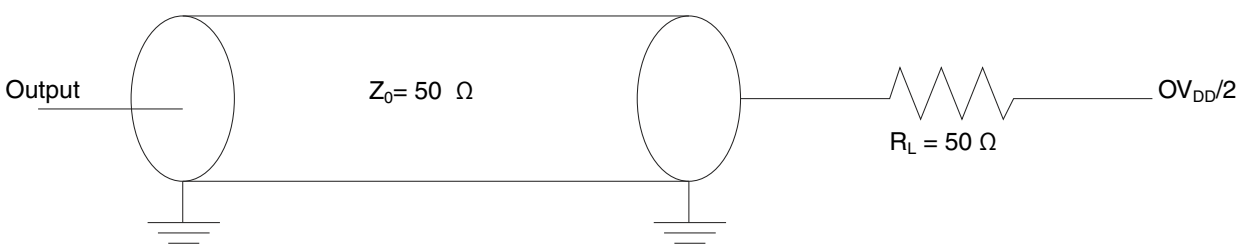


Figure 66. GPIO AC test load

3.21 Battery-backed security monitor interface

This section describes the DC and AC electrical characteristics for the battery-backed security monitor interface, which includes the TA_BB_TMP_DETECT_B pin.

3.21.1 Battery-backed security monitor interface DC electrical characteristics

This table provides the DC electrical characteristics for the battery-backed security monitor interface operating at 1.0 V ($TA_BB_V_{DD}$).

Table 62. Battery-backed security monitor interface DC electrical characteristics (1.0 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.8	—	V	1
Input low voltage	V_{IL}	—	0.3	V	1
Input current (V_{IN} = 0 V or V_{IN} = $TA_BB_V_{DD}$)	I_{IN}	—	±50	μA	2
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max $TA_BB_V_{DD}$ values found in Table 3.					
2. The symbol V_{IN}, in this case, represents the $TA_BB_V_{DD}$ symbol referenced in Table 3.					
3. For recommended operating conditions, see Table 3.					

3.21.2 Battery-backed security monitor interface AC timing specifications

This table provides the AC timing specifications for the battery-backed security monitor interface.

Table 63. Battery-backed security monitor interface AC timing specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
TA_BB_TMP_DETECT_B	t_{TMP}	100	—	—	ns	1
Notes:						
1. TA_BB_TMP_DETECT_B is asynchronous to any clock.						
2. For recommended operating conditions, see Table 3.						

3.22 High-speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SATA, XAUI, XFI, SGMII, and QSGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

3.22.1 Signal terms definition

The SerDes uses differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

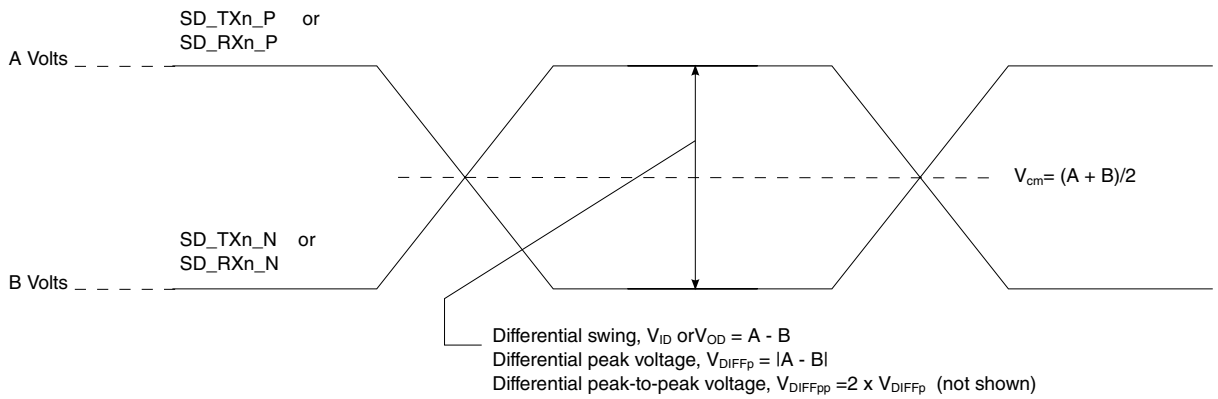


Figure 67. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD_TXn_P}$ - $V_{SD_TXn_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD_RXn_P}$ - $V_{SD_RXn_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 72 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SD_TXn_P} + V_{SD_TXn_N}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.22.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N for SerDes 1, SD2_REF_CLK[1:2]_P and SD2_REF_CLK[1:2]_N for SerDes 2.

SerDes 1-2 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SerDes 1: XFI, XAUI, SGMII, QSGMII, PCIe
- SerDes 2: PCIe, SGMII, SATA

The following sections describe the SerDes reference clock requirements and provide application information.

3.22.2.1 SerDes spread-spectrum clock source recommendations

SDn_REF_CLKn_P/SDn_REF_CLKn_N are designed to work with spread-spectrum clock for PCI Express protocol only with the spreading specification defined in Table 64. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

For SATA protocol, the SerDes transmitter does not support spread-spectrum clocking. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking

The spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum supported protocols. For example, if the spread-spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SATA/SGMII/QSGMII/XAUI/XFI due to the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

Table 64. SerDes spread-spectrum clock source recommendations[1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	-0.5	%	2

Notes:

1. At recommended operating conditions. See Table 3.
2. Only down-spreading is allowed.

3.22.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

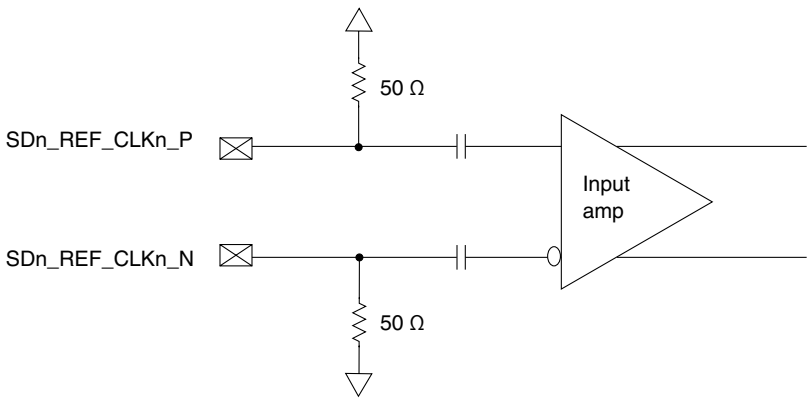


Figure 68. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements ($SV_{DD}n$) are as specified in Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The are internally AC-coupled differential inputs as shown in Figure 68. Each differential clock input (SD*n*_REF_CLK*n*_P or SD*n*_REF_CLK*n*_N) has on-chip 50-Ω termination to SD_GND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SD_GND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to

16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N inputs cannot drive 50 Ω to SD_GND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.22.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below.

Differential mode:

- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
- For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 69 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

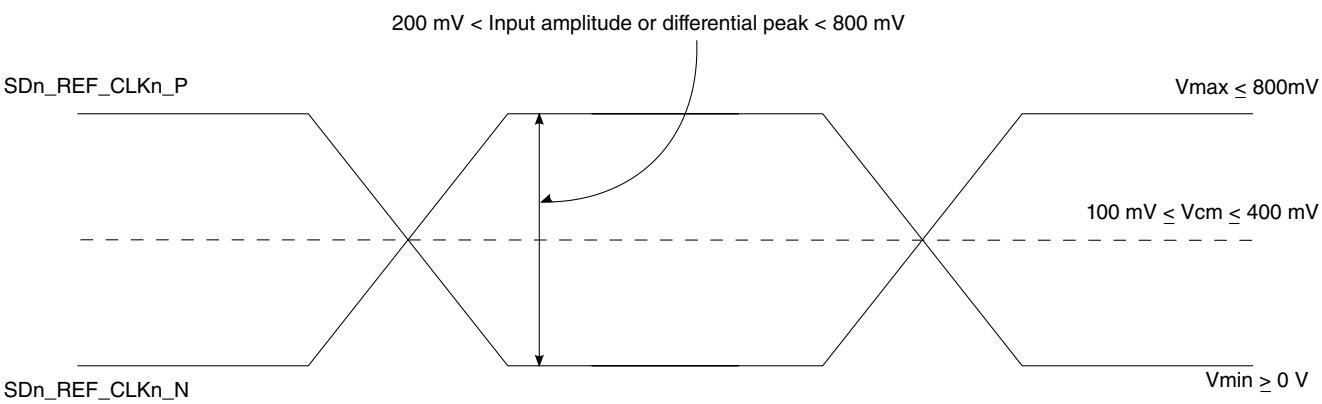


Figure 69. Differential reference clock input DC requirements (external DC-coupled)

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SD_GND. Each signal wire

of the differential inputs is allowed to swing below and above the common mode voltage (SD_GND). Figure 70 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

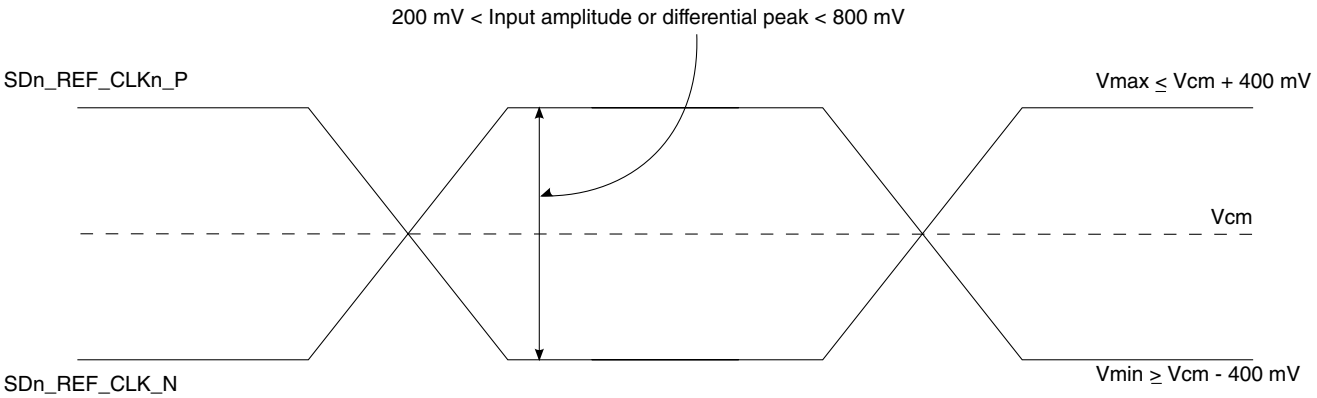


Figure 70. Differential reference clock input DC requirements (external AC-coupled)

Single-ended mode:

- The reference clock can also be single-ended. The SDn_REF_CLKn_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SDn_REF_CLKn_N either left unconnected or tied to ground.
- The SDn_REF_CLKn_P input average voltage must be between 200 and 400 mV. Figure 71 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SDn_REF_CLKn_N) through the same source impedance as the clock input (SDn_REF_CLKn_P) in use.

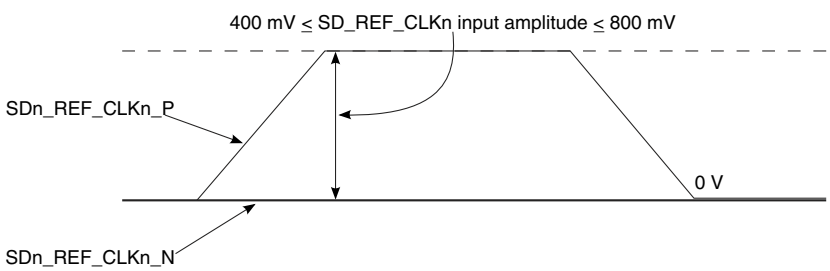


Figure 71. Single-ended reference clock input DC requirements

3.22.2.4 AC requirements for SerDes reference clocks

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates up to 8 Gb/s.

This includes PCI Express (2.5, 5, 8 GT/s), SGMII (1.25Gbps), 2.5x SGMII (3.125Gbps), QSGMII (5Gbps), XAUI (3.125 Gbps), and SerDes reference clocks to be guaranteed by the customer's application design.

Table 65. SDn_REF_CLKn_P/ SDn_REF_CLKn_N input clock requirements ($SV_{DD}n$ = 1.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
frequency range	t_{CLK_REF}	—	100/125/156.25	—	MHz	2
clock frequency tolerance	t_{CLK_TOL}	-300	—	300	ppm	3
clock frequency tolerance	t_{CLK_TOL}	-100	—	100	ppm	4
reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	6
10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	—	—	3	ps RMS	7
> 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	—	—	3.1	ps RMS	7
RMS reference clock jitter	$t_{REFCLK\text{-}RMS\text{-}DC}$	—	—	1	ps RMS	8
rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	9
Differential input high voltage	V_{IH}	200	—	—	mV	5
Differential input low voltage	V_{IL}	—	—	-200	mV	5
Rising edge rate to falling edge rate matching	Rise-Fall Matching	—	—	20	%	10, 11

Notes:

1. For recommended operating conditions, see Table 3.
2. **Caution:** Only 100, 125 and 156.25 have been tested. Inbetween values do not work correctly with the rest of the system.
3. For PCI Express (2.5, 5, 8 GT/s)
4. For SGMII, 2.5x SGMII, QSGMII, XAUI
5. Measurement taken from differential waveform
6. Limits from PCI Express CEM Rev 2.0
7. For PCI Express-5 GT/s, per PCI Express base specification rev 3.0
8. For PCI-Express-8 GT/s, per PCI-Express base specification rev 3.0
9. Measured from -200 mV to +200 mV on the differential waveform (derived from minus). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 72.
10. Measurement taken from single-ended waveform
11. Matching applies to rising edge for and falling edge rate for . It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLKn_P rising meets SDn_REF_CLKn_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SDn_REF_CLKn_P must be compared to the fall edge rate of SDn_REF_CLKn_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 73.

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 Gb/s.

This includes XFI (10.3125 Gbps) SerDes reference clocks to be guaranteed by the customer's application design.

Table 66. input clock requirements for XFI (10.3125)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
frequency range	t_{CLK_REF}	—	156.25	—	MHz	2
clock frequency tolerance	t_{CLK_TOL}	-100	—	100	ppm	—
reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	3
single side band noise	@1 kHz	—	—	-85	dBC/Hz	4
single side band noise	@10 kHz	—	—	-108	dBC/Hz	4
single side band noise	@100 kHz	—	—	-128	dBC/Hz	4
single side band noise	@1 MHz	—	—	-138	dBC/Hz	4
single side band noise	@10MHz	—	—	-138	dBC/Hz	4
random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	—	—	0.8	ps	—
total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	—	—	11	ps	—
spurious noise (1.2 MHz to 15 MHz)	—	—	—	-75	dBC	—

Notes:

1. For recommended operating conditions, see Table 3.
2. **Caution:** Only 156.25 have been tested. Inbetween values do not work correctly with the rest of the system.
3. Measurement taken from differential waveform.
4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.

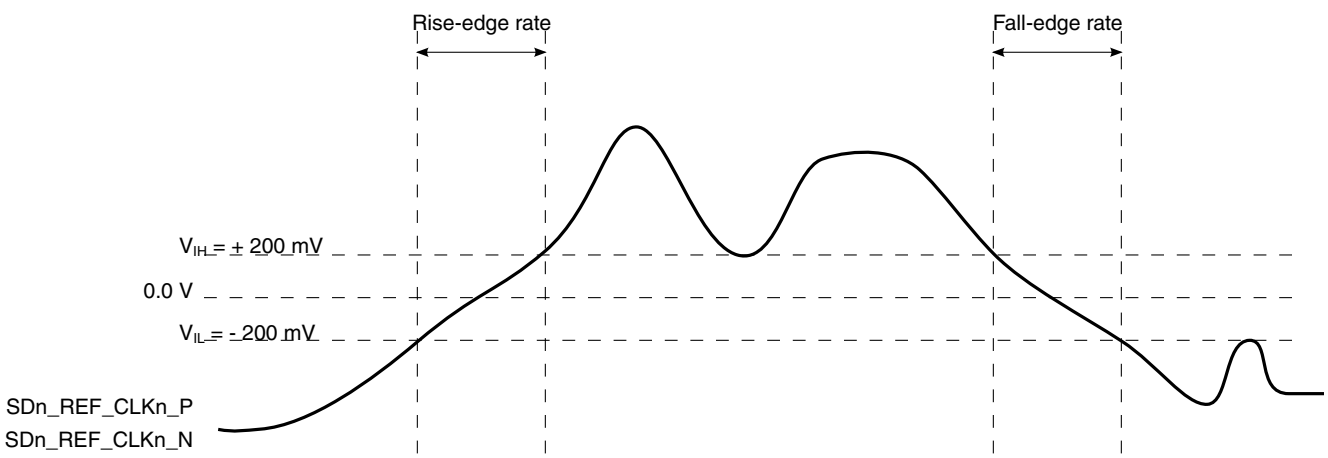


Figure 72. Differential measurement points for rise and fall time

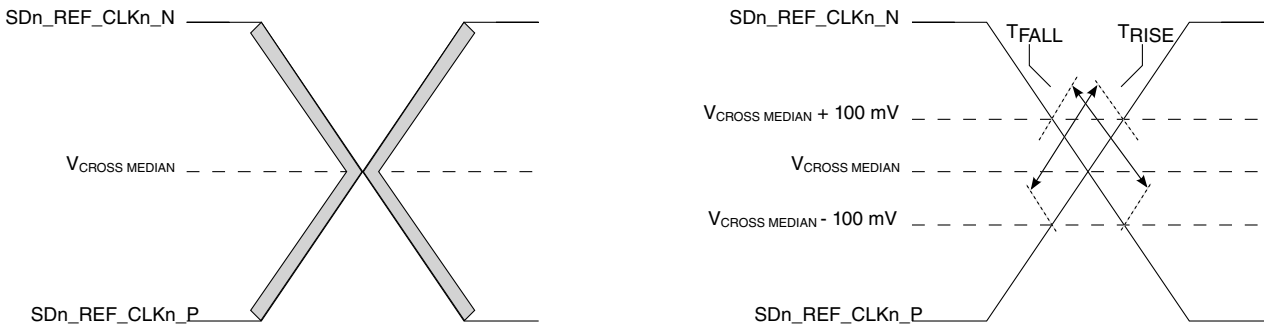


Figure 73. Single-ended measurement points for rise and fall time matching

3.22.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

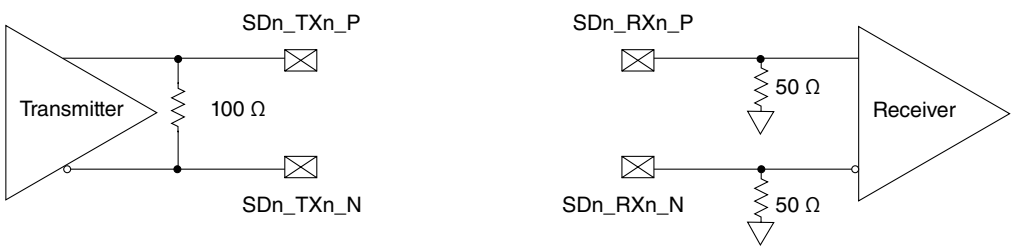


Figure 74. SerDes transmitter and receiver reference circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- XAUI interface
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface
- XFI interface

Note that external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.22.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

If the platform speed runs at 533 MHz, there is no limitation to PCIe speed/width. If the platform speed runs at 500 MHz, all four PCIe controllers can run GEN1 and GEN2 speed at full width. For GEN3 speed, PEX1/PEX2/PEX4 can only run x2 width, PEX3 can only run x4 width.

3.22.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.22.4.2 PCI Express clocking requirements for SDn_REF_CLKn_P and SDn_REF_CLKn_N

SerDes 1-2 (SD[1:2]_REF_CLK[1:2]_P and SD[1:2]_REF_CLK[1:2]_N) may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is supported on SerDes 1 and 2.

For more information on these specifications, see SerDes reference clocks.

3.22.4.3 PCI Express DC physical layer characteristics

This section contains the DC characteristics for the physical layer of PCI Express on this chip.

3.22.4.3.1 PCI Express DC physical layer transmitter characteristics

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 67. PCI Express 2.5 GT/s differential transmitter output DC characteristics (XV_{DD} = 1.35 V)[1]

Characteristic	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p}$ = 2 x | $V_{TX\text{-}D+}$ - $V_{TX\text{-}D-}$ |
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance

Table continues on the next page...

Table 67. PCI Express 2.5 GT/s differential transmitter output DC characteristics (XV_{DD} = 1.35 V)[1] (continued)

Characteristic	Symbol	Min	Typical	Max	Units	Notes
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 2.0 (5 GT/s) DC characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 68. PCI Express 5 GT/s differential transmitter output DC characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 3.0 (8 GT/s) DC characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 69. PCI Express 8 GT/s differential transmitter output DC characteristics (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800	—	1300	mVp-p	See Note 1.
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400	—	1300	mV	See Note 1.

Table continues on the next page...

Table 69. PCI Express 8 GT/s differential transmitter output DC characteristics (XV_{DD} = 1.35 V)[3] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	—
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	—
Minimum swing during EIEOS for full swing	$V_{TX-EIEOS-FS}$	250	—	—	mVp-p	See Note 2
Minimum swing during EIEOS for reduced swing	$V_{TX-EIEOS-RS}$	232	—	—	mVp-p	See Note 2
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

3. For recommended operating conditions, see Table 3.

3.22.4.4 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the DC characteristics for the PCI Express 1.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 70. PCI Express 2.5 GT/s differential receiver input DC characteristics (SV_{DD} = 1.0 V)[4]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.

Table continues on the next page...

Table 70. PCI Express 2.5 GT/s differential receiver input DC characteristics (SV_{DD} = 1.0 V)[4] (continued)

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 x $\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 3.

This table defines the DC characteristics for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 71. PCI Express 5 GT/s differential receiver input DC characteristics (SV_{DD} = 1.0 V)[4]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p}$ = 2 x $\|V_{RX-D+} - V_{RX-D-}\|$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 x $\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

Table 71. PCI Express 5 GT/s differential receiver input DC characteristics (SV_{DD} = 1.0 V)[4]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground. 4. For recommended operating conditions, see Table 3.						

This table defines the DC characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 72. PCI Express 8 GT/s differential receiver input DC characteristics (SV_{DD} = 1.0 V)[6]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Generator launch voltage	$V_{RX-LAUNCH-8G}$	—	800	—	mV	Measured at TP1 per PCI Express base spec. rev 3.0
Eye height (-20dB Channel)	$V_{RX-SV-8G}$	25	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-12dB Channel)	$V_{RX-SV-8G}$	50	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-3dB Channel)	$V_{RX-SV-8G}$	200	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver
Notes: 1. Measured at the package pins with a test load of 50 Ω to GND on each pin. 2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port. 3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground. 4. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage. 5. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post processing data captured at TP2. 6. For recommended operating conditions, see Table 3.						

3.22.4.5 PCI Express AC physical layer specifications

This section contains the AC specifications for the physical layer of PCI Express on this device.

3.22.4.5.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the PCI Express 1.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 73. PCI Express 2.5 GT/s differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 76 and measured over any 250 consecutive transmitter UIs.

2. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

4. For recommended operating conditions, see Table 3.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 74. PCI Express 5 GT/s differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 76 and measured over any 250 consecutive transmitter UIs.
2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
3. For recommended operating conditions, see Table 3.

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 75. PCI Express 8 GT/s differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Transmitter uncorrelated total jitter	T_{TX-UTJ}	—	—	31.25	ps p-p	—
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	—	—	12	ps p-p	—
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	—	—	24	ps p-p	See Note 1, 2
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	—	—	10	ps p-p	See Note 1, 2

Table continues on the next page...

Table 75. PCI Express 8 GT/s differential transmitter output AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data dependent jitter	T_{TX-DDJ}	—	—	18	ps p-p	See Note 2
AC coupling capacitor	C_{TX}	176	—	265	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. PWJ parameters shall be measured after data dependent jitter (DDJ) separation.
2. Measured with optimized preset value after de-embedding to transmitter pin.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 3.

3.22.4.5.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 76. PCI Express 2.5 GT/s differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

Table 76. PCI Express 2.5 GT/s differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 76 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram. 2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram. 3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data. 4. For recommended operating conditions, see Table 3.						

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 77. PCI Express 5 GT/s differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture
Note: 1. For recommended operating conditions, see Table 3.						

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 78. PCI Express 8 GT/s differential receiver input AC specifications[5]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note 1.
Eye Width at TP2P	$T_{RX-SV-8G}$	0.3	—	0.35	UI	See Note 1

Table continues on the next page...

Table 78. PCI Express 8 GT/s differential receiver input AC specifications[5] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14	—	—	mV	Frequency = 2.1GHz. See Note 2.
Sinusoidal Jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	—	—	0.1	UI p-p	Fixed at 100 MHz. See Note 3.
Random Jitter	$T_{RX-SV-RJ-8G}$	—	—	2.0	ps RMS	Random jitter spectrally flat before filtering. See Note 4.

Note:

1. $T_{RX-SV-8G}$ is referenced to TP2P and obtained after post processing data captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.
2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.
3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in Figure 75.
4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 75 for details. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.
5. For recommended operating conditions, see Table 3.

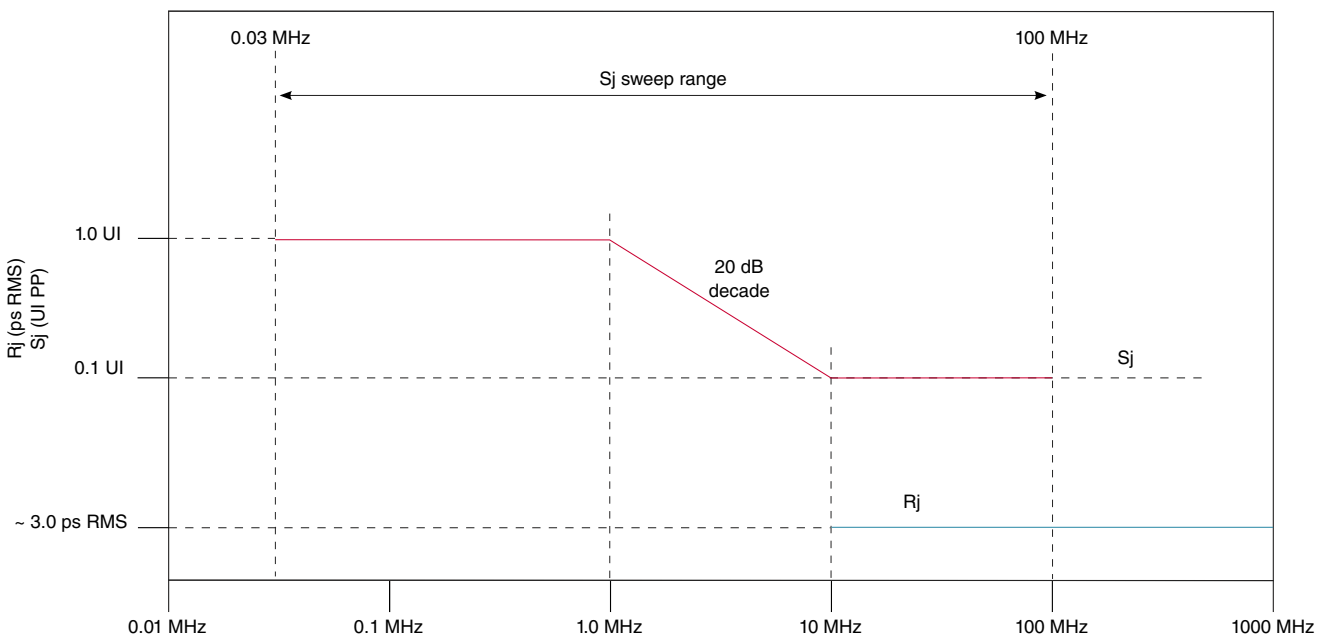


Figure 75. Swept sinusoidal jitter mask

3.22.4.6 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/

board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

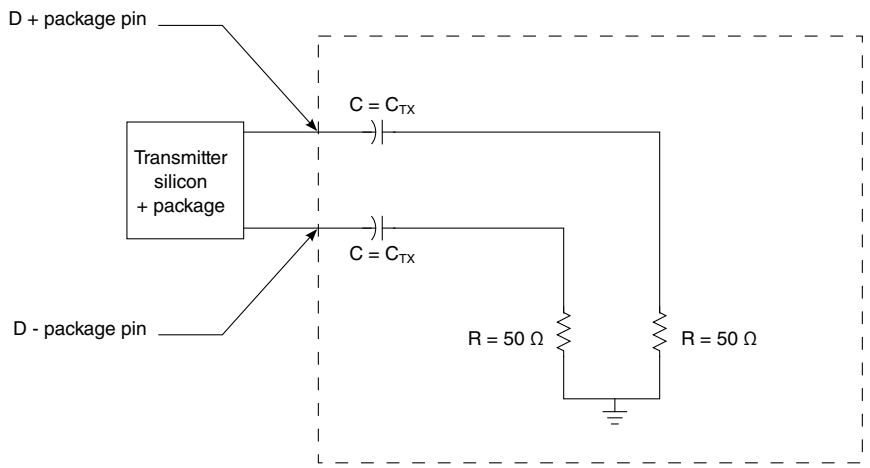


Figure 76. Test/measurement load

3.22.5 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

3.22.5.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.22.5.1.1 SATA DC transmitter output characteristics

The table below provides the DC differential transmitter output DC characteristics for the SATA interface at Gen1i/1m 1.5 Gbits/s transmission.

Table 79. Gen1i/1m 1.5G transmitter (Tx) DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	2
Notes:						

Table 79. Gen1i/1m 1.5G transmitter (Tx) DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
1. Terminated by 50 Ω load. 2. DC impedance. 3. For recommended operating conditions, see Table 3.						

The table below provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m 3.0 Gbits/s transmission.

Table 80. Gen 2i/2m 3.0G transmitter (Tx) DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter diff output voltage	V_{SATA_TXDIFF}	400	-	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	2
1. Terminated by 50 Ω load. 2. DC impedance. 3. For recommended operating conditions, see Table 3.						

The table below provides the differential transmitter output DC characteristics for the SATA interface at Gen3i 6.0 Gbits/s transmission.

Table 81. Gen 3i 6.0G transmitter (Tx) DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter diff output voltage	V_{SATA_TXDIFF}	240	-	900	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	2
1. Terminated by 50 Ω load. 2. DC impedance. 3. For recommended operating conditions, see Table 3.						

3.22.5.1.2 SATA DC receiver (Rx) input characteristics

The table below provides the Gen1i/1m 1.5Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 82. Gen1i/1m 1.5G receiver input DC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	-	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2

Table continues on the next page...

Table 82. Gen1i/1m 1.5G receiver input DC specifications (SV_{DD} = 1.0 V)[3] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
OOB signal detection threshold	V_{SATA_OOB}	50	100	200	mV p-p	-
1. Voltage relative to common of either signal comprising a differential pair 2. DC impedance. 3. For recommended operating conditions, see Table 3.						

The table below provides the Gen2i/2m 3Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 83. Gen2i/2m 3G receiver input DC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	-	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	125	200	mV p-p	-
Notes: 1. Voltage relative to common of either signal comprising a differential pair 2. DC impedance 3. For recommended operating conditions, see Table 3.						

The table below provides the Gen3i 6Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 84. Gen3i 6G receiver input DC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	-	1000	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	125	200	mV p-p	-
Notes: 1. Voltage relative to common of either signal comprising a differential pair 2. DC impedance 3. For recommended operating conditions, see Table 3.						

3.22.5.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

3.22.5.2.1 AC requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in the Table 85 to be guaranteed by the customer's application design.

Table 85. SATA reference clock input requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/SD_REF_CLK frequency range	t_{CLK_REF}	-	100/125	-	MHz	1
SD_REF_CLK/SD_REF_CLK clock frequency tolerance	t_{CLK_TOL}	-350	-	+350	ppm	-
SD_REF_CLK/SD_REF_CLK reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	-
SD_REF_CLK/SD_REF_CLK cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	-	-	100	ps	2
SD_REF_CLK/SD_REF_CLK total reference clock jitter, phase jitter (peak-peak)	t_{CLK_PJ}	-50	-	+50	ps	2, 3, 4

Notes:

1. **Caution:** Only 100, 125MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
4. Total peak-to-peak deterministic jitter should be less than or equal to 50 ps.

The figure below shows the reference clock timing waveform.

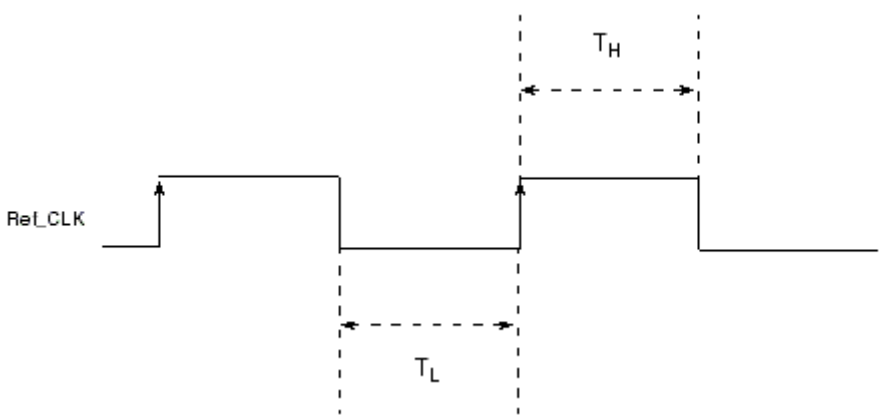


Figure 77. Reference clock timing waveform

3.22.5.2.2 AC transmitter output characteristics

The table below provides the differential transmitter output AC characteristics for the SATA interface at Gen1i/1m 1.5Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen1i/1m 1.5G transmitter (Tx) AC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	-	1.5	-	Gbps	-
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	-
Total jitter data-data 5 UI	$U_{SATA_TXTJ5UI}$	-	-	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	-	-	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	-	-	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	-	-	0.22	UI p-p	1
1. Measured at transmitter output pins peak to peak phase variation, random data pattern 2. For recommended operating conditions, see Table 3.						

The table below provides the differential transmitter output AC characteristics for the SATA interface at Gen2i/2m 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 2i/2m 3G transmitter (Tx) AC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	-	3.0	-	Gbps	-
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	-
Total jitter fC3dB = fBAUD ÷ 10	$U_{SATA_TXTJfB/10}$	-	-	0.3	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXTJfB/500}$	-	-	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXTJfB/1667}$	-	-	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA_TXDJfB/10}$	-	-	0.17	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXDJfB/500}$	-	-	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXDJfB/1667}$	-	-	0.35	UI p-p	1
1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern 2. For recommended operating conditions, see Table 3.						

The table below provides the differential transmitter output AC characteristics for the SATA interface at Gen3i 6.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 88. Gen 3i 6G transmitter (Tx) AC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	T_{UI}	166.6083	166.6667	167.5583	ps	-
Total jitter before and after compliance interconnect channel	JT	-	-	0.52	UI p-p	1

Table continues on the next page...

Table 88. Gen 3i 6G transmitter (Tx) AC specifications (XV_{DD} = 1.35 V)[2] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Random jitter before compliance interconnect channel	JR	-	-	0.18	UI p-p	1

1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern
2. For recommended operating conditions, see Table 3.

3.22.5.2.3 AC differential receiver input characteristics

The table below provides the Gen1i/1m or 1.5Gbits/s differential receiver input AC characteristics for the SATA interface.

Table 89. Gen 1i/1m 1.5G receiver (Rx) AC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	-
Total jitter data-data 5 UI	$U_{SATA_TXTJ5UI}$	-	-	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	-	-	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	-	-	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	-	-	0.35	UI p-p	1

1. Measured at receiver.
2. The AC timing specifications do not include RefClk jitter.
3. For recommended operating conditions, see Table 3.

The table below provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m 3.0 Gbits/s transmission.

Table 90. Gen 2i/2m 3G receiver (Rx) AC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	-
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA_TXTJfB/10}$	-	-	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXTJfB/500}$	-	-	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXTJfB/1667}$	-	-	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA_TXDJfB/10}$	-	-	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXDJfB/500}$	-	-	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXDJfB/1667}$	-	-	0.35	UI p-p	1

1. Measured at receiver.
2. The AC timing specifications do not include RefClk jitter.
3. For recommended operating conditions, see Table 3.

The table below provides the Gen3i 6.0Gbits/s differential receiver input AC characteristics for the SATA interface.

Table 91. Gen 3i 6.0G receiver (Rx) AC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	166.6083	166.6667	167.5583	ps	-
Total jitter after compliance interconnect channel	$_{JT}$	-	-	0.60	UI p-p	1
Random jitter before compliance interconnect channel	$_{JR}$	-	-	0.18	UI p-p	1
1. Measured at receiver. 2. The AC timing specifications do not include RefClk jitter. 3. For recommended operating conditions, see Table 3.						

3.22.6 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 78, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SD_GND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 74.

3.22.6.1 SGMII clocking requirements for

When operating in SGMII mode, a SerDes reference clock is required on SDn_REF_CLK[1:2]_P and SDn_REF_CLK[1:2]_Npins. Both SerDes 1 and SerDes 2 may be used for SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.22.6.2 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.22.6.2.1 SGMII and SGMII 2.5x transmit DC characteristics

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) as shown in Figure 79.

Table 92. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	—	—	mV	1
Output differential voltage[2, 3] (XV_{DD-Typ} at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	—
		293.8	459.0	665.6		—
		266.9	417.0	604.7		—
		240.6	376.0	545.2		—
		213.1	333.0	482.9		—
		186.9	292.0	423.4		—
		160.0	250.0	362.5		—
Output impedance (differential)	R_O	80	100	120	Ω	—

Notes:

1. This does not align to DC-coupled SGMII.
2. $\lvert V_{OD} \rvert = \lvert V_{SD_TXn_P} - V_{SD_TXn_N} \rvert$. $\lvert V_{OD} \rvert$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times \lvert V_{OD} \rvert$.
3. The $\lvert V_{OD} \rvert$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD*n*_TXn_P and SD*n*_TXn_N.
4. For recommended operating conditions, see Table 3.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

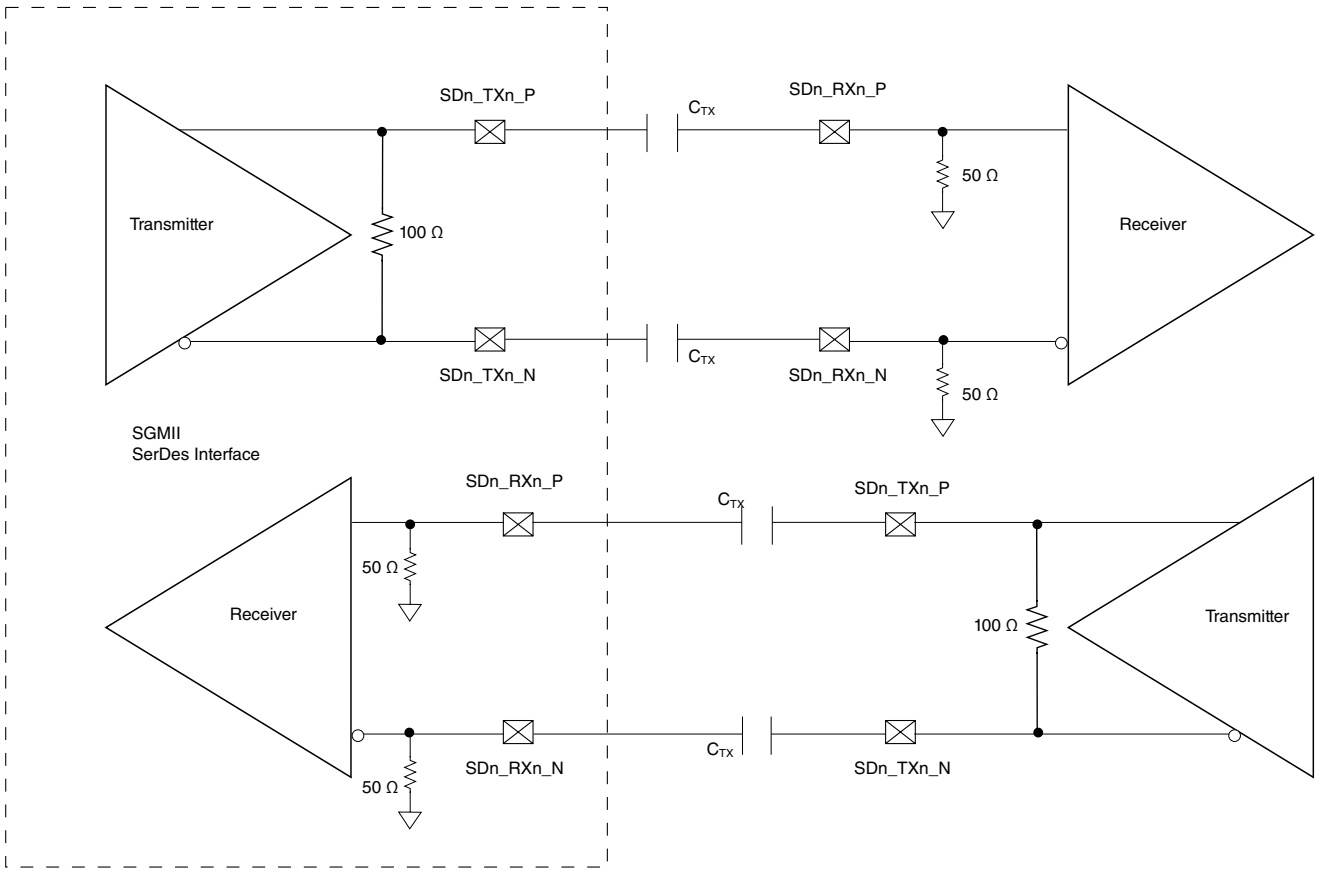


Figure 78. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

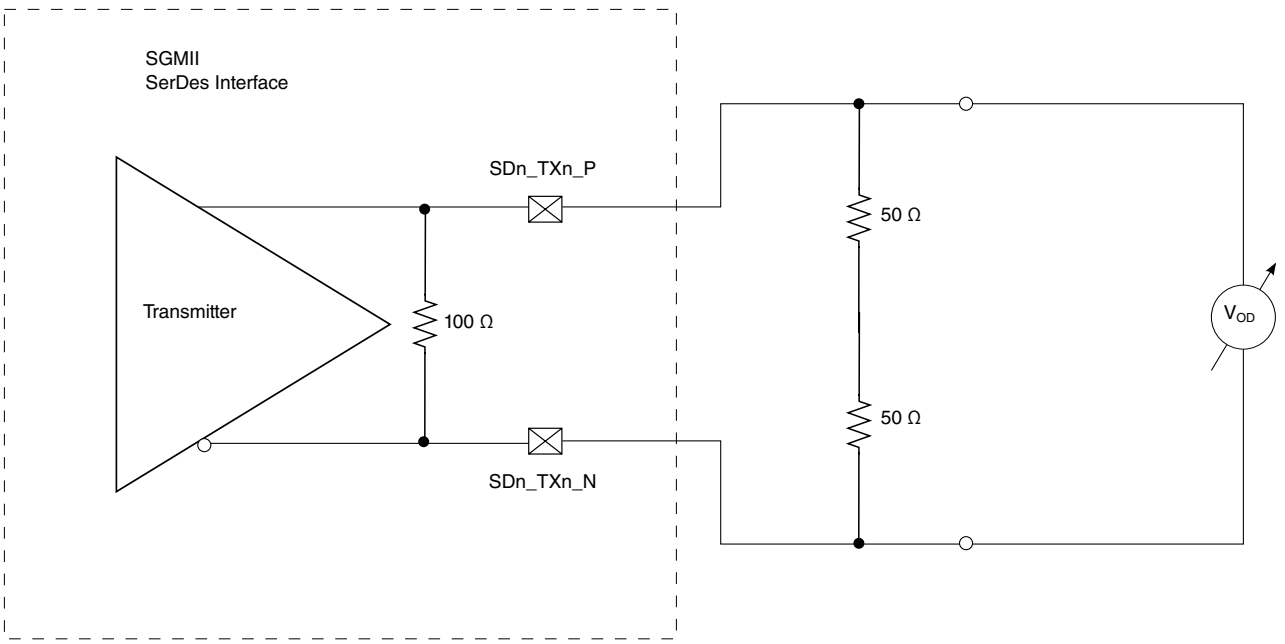


Figure 79. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 93. SGMII 2.5x transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	—	600	mV	—
Output impedance (differential)	R_O	80	100	120	Ω	—
Notes: 1. For recommended operating conditions, see Table 3.						

3.22.6.2.2 SGMII and SGMII 2.5x DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 94. SGMII DC receiver electrical characteristics (SV_{DD} = 1.0V)[4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		—	N/A			—	1
Input differential voltage	—	$V_{RX_DIFFp\text{-}p}$	100	—	1200	mV	2
	—		175	—			
Loss of signal threshold	—	V_{LOS}	30	—	100	mV	3
	—		65	—	175		

Table continues on the next page...

Table 94. SGMII DC receiver electrical characteristics (SV_{DD} = 1.0V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver differential input impedance	Z_{RX_DIFF}	80	—	120	Ω	—

Notes:

1. Input must be externally AC coupled.
2. $V_{RX_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express AC physical layer receiver specifications, for further explanation.
4. For recommended operating conditions, see Table 3.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 95. SGMII 2.5x receiver DC timing specifications (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX_DIFFp\text{-}p}$	200	—	1200	mV	—
Loss of signal threshold	V_{LOS}	75	—	200	mV	—
Receiver differential input impedance	Z_{RX_DIFF}	80	—	120	Ω	—

Note:

1. For recommended operating conditions, see Table 3.

3.22.6.3 SGMII AC timing specifications

This section discusses the AC timing specifications for the SGMII interface.

3.22.6.3.1 SGMII and SGMII 2.5x transmit AC timing specifications

This table provides the SGMII and SGMII 2.5x transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 96. SGMII transmit AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	—
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5x SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	2

Notes:

1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.

Table 96. SGMII transmit AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.						
3. For recommended operating conditions, see Table 3.						

3.22.6.3.2 SGMII AC measurement details

Transmitter and receiver AC specifications are measured at the transmitter outputs (_TX*n*_P and _TX*n*_N) or at the receiver inputs (_RX*n*_P and _RX*n*_N) respectively, as depicted in this figure.

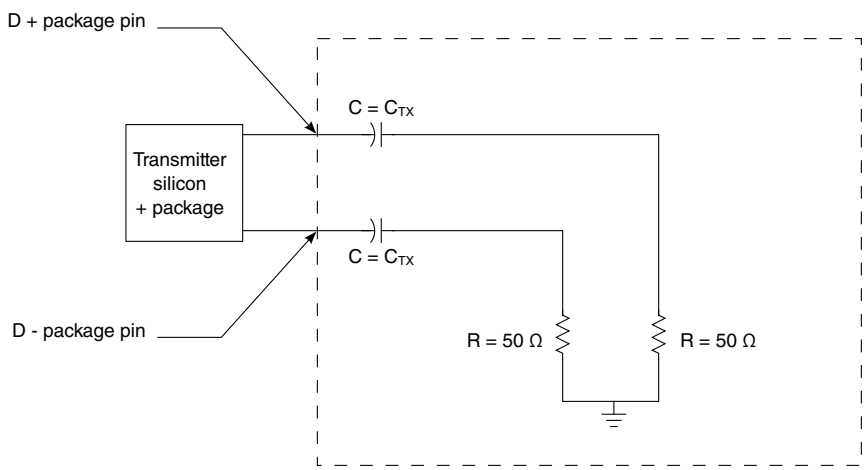


Figure 80. SGMII AC test/measurement load

3.22.6.3.3 SGMII and SGMII 2.5x receiver AC timing specification

This table provides the SGMII and SGMII 2.5x receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. The clock is recovered from the data.

Table 97. SGMII receiver AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	—	—	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total jitter tolerance	J_T	—	—	0.65	UI p-p	1, 2
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5x SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1
Notes:						

Table 97. SGMII receiver AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Measured at receiver 2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects. 3. For recommended operating conditions, see Table 3.						

3.22.7 QSGMII interface

This section describes the QSGMII clocking and its DC and AC electrical characteristics.

3.22.7.1 QSGMII clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

For more information on these specifications, see SerDes reference clocks.

3.22.7.2 QSGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.22.7.2.1 QSGMII transmitter DC characteristics

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N).

Table 98. QSGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[1]

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	V_{DIFF}	400	—	900	mV	—
Differential resistance	T_{RD}	80	100	120	Ω	—
Note: 1. For recommended operating conditions, see Table 3.						

3.22.7.2.2 QSGMII DC receiver electrical characteristics

This table defines the QSGMII receiver DC electrical characteristics.

Table 99. QSGMII receiver DC timing specifications (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{DIFF}	100	—	900	mV	—
Differential resistance	R_{RDIN}	80	100	120	Ω	—

Notes:

1. For recommended operating conditions, see Table 3.

3.22.7.3 QSGMII AC timing specifications

This section discusses the AC timing specifications for the QSGMII interface.

3.22.7.3.1 QSGMII transmitter AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 100. QSGMII transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter baud rate	T_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	—
Uncorrelated high probability jitter	T_{UHPJ}	—	—	0.15	UI p-p	—
Total jitter tolerance	J_T	—	—	0.30	UI p-p	—

Notes:

1. For recommended operating conditions, see Table 3.

3.22.7.3.2 QSGMII receiver AC timing Specification

This table provides the QSGMII receiver AC timing specifications.

Table 101. QSGMII receiver AC timing specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	—
Uncorrelated bounded high probability jitter	R_{DJ}	—	—	0.15	UI p-p	—
Correlated bounded high probability jitter	R_{CBHPJ}	—	—	0.30	UI p-p	1
Bounded high probability jitter	R_{BHPJ}	—	—	0.45	UI p-p	—
Sinusoidal jitter, maximum	R_{SJ-max}	—	—	5.00	UI p-p	—
Sinusoidal jitter, high frequency	R_{SJ-hf}	—	—	0.05	UI p-p	—
Total jitter (does not include sinusoidal jitter)	R_{Tj}	—	—	0.60	UI p-p	—

Notes:

1. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
2. For recommended operating conditions, see Table 3.

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

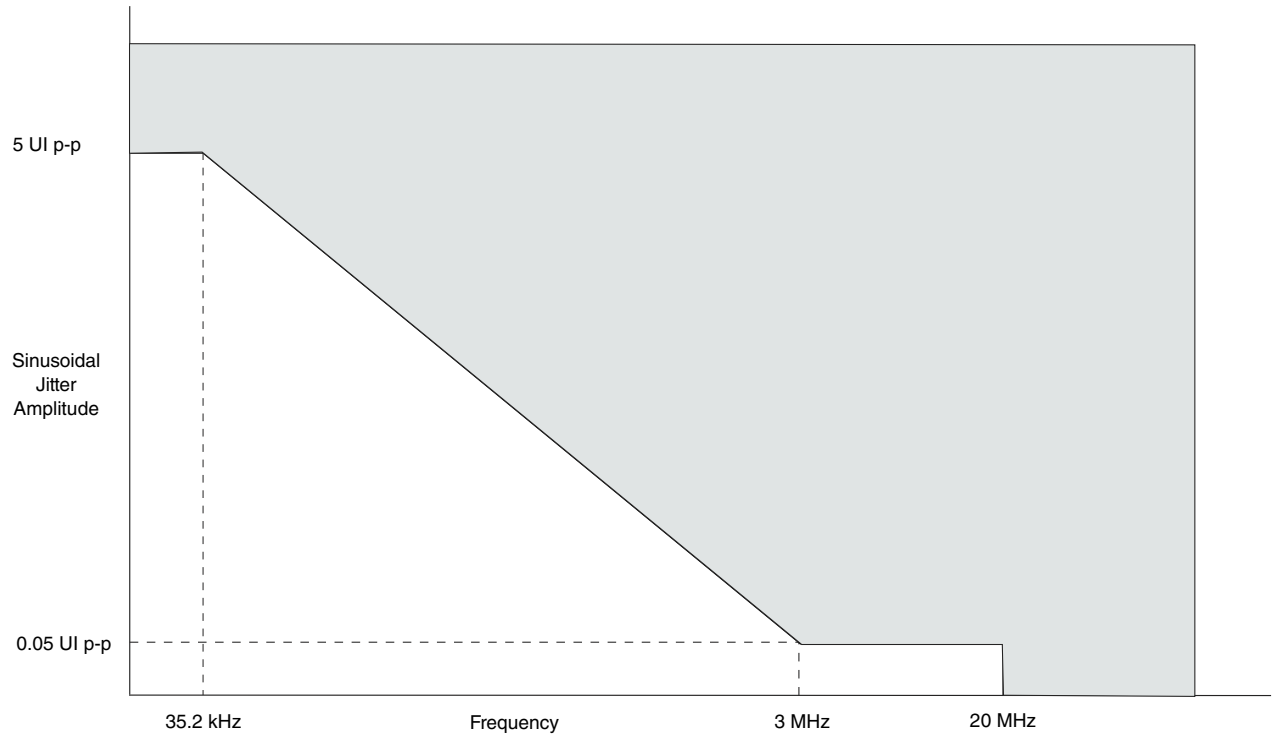


Figure 81. QSGMII single-frequency sinusoidal jitter limits

3.22.8 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

3.22.8.1 XFI clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N

Only SerDes 1 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N) may be used for SerDes XFI configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.22.8.2 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

3.22.8.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 102. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	360	—	770	mV	2
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14\ dB}$	0.6	1.1	1.6	dB	3
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5\ dB}$	3	3.5	4	dB	4
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66\ dB}$	4.1	4.6	5.1	dB	5
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0\ dB}$	5.5	6.0	6.5	dB	6
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5\ dB}$	9	9.5	10	dB	7
Differential resistance	T_{RD}	80	100	120	Ω	—

Notes:

1. For recommended operating conditions, see Table 3.
2. LNmTECR0[EQ_AMP_RED] = 000111
3. LNmTECR0[EQ_POST1Q] = 00011
4. LNmTECR0[EQ_POST1Q] = 01000
5. LNmTECR0[EQ_POST1Q] = 01010
6. LNmTECR0[EQ_POST1Q] = 01100
7. LNmTECR0[EQ_POST1Q] = 10000

3.22.8.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

Table 103. XFI receiver DC electrical characteristics (SV_{DD} = 1.0V)[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	110	—	1050	mV	1
Differential resistance	R_{RD}	80	100	120	Ω	—

1. Measured at receiver
2. For recommended operating conditions, see Table 3.

3.22.8.3 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

3.22.8.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 104. XFI transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s
Unit Interval	UI	—	96.96	—	ps
Deterministic jitter	D_J	—	—	0.15	UI p-p
Total jitter	T_J	—	—	0.30	UI p-p

Notes:

1. For recommended operating conditions, see Table 3.

3.22.8.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 105. XFI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s	—
Unit Interval	UI	—	96.96	—	ps	—
Total non-EQJ jitter	$T_{NON-EQJ}$	—	—	0.45	UI p-p	1
Total jitter tolerance	T_J	—	—	0.65	UI p-p	1, 2

1. The total jitter (T_J) consists of Random Jitter (R_J), Duty Cycle Distortion (DCD), Periodic Jitter (P_J), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (R_J), and periodic jitter (P_J). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = T_J - ISI = R_J + DCD + P_J

2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of transmitter equalization and amplitude is required for performance optimization.

3. For recommended operating conditions, see Table 3.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

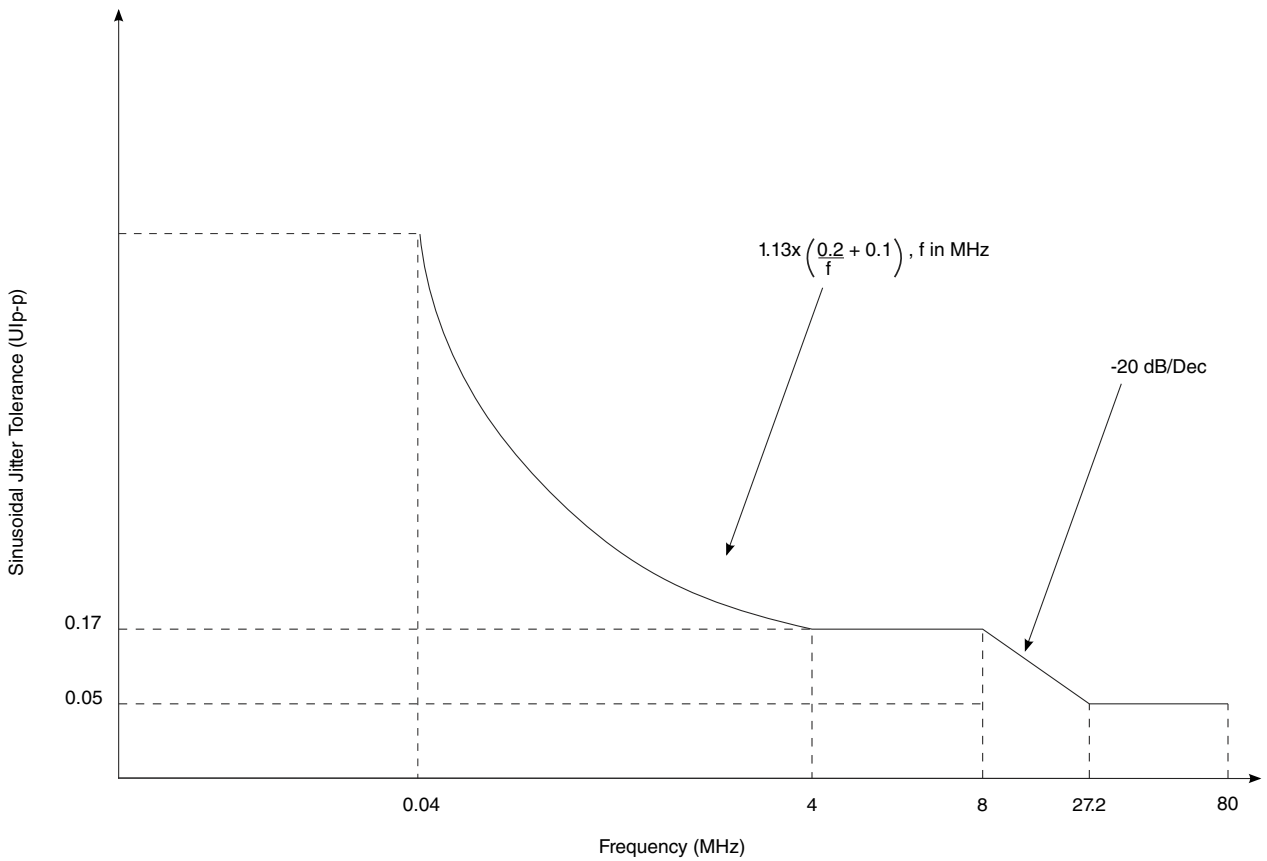


Figure 82. XFI host receiver input sinusoidal jitter tolerance

3.22.9 XAUI interface

This section describes the DC and AC electrical specifications for the XAUI bus.

3.22.9.1 XAUI DC electrical characteristics

This section discusses the XAUI DC electrical characteristics for the clocking signals, transmitter, and receiver.

3.22.9.1.1 DC requirements for XAUI SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

Only SerDes 1 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N) may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.22.9.1.2 XAUI transmitter DC electrical characteristics

This table defines the XAUI transmitter DC electrical characteristics.

Table 106. XAUI transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output voltage	V_O	-0.40	—	2.30	V	2
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p	—
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	3
Notes: 1. For recommended operating conditions, see Table 3. 2. Absolute output voltage limit 3. Transmitter DC differential impedance						

3.22.9.1.3 XAUI receiver DC electrical characteristics

This table defines the XAUI receiver DC electrical characteristics.

Table 107. XAUI receiver DC timing specifications (SV_{DD} = 1.0 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	—	1600	mV p-p	2
DC Differential receiver input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	3
Notes: 1. For recommended operating conditions, see Table 3. 2. Measured at the receiver 3. Receiver DC differential impedance						

3.22.9.2 XAUI AC timing specifications

This section explains the AC requirements for the XAUI interface.

3.22.9.2.1 XAUI transmitter AC timing specifications

This table defines the XAUI transmitter AC timing specifications. RefClk jitter is not included.

Table 108. XAUI transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 3.125 GBaud	UI	320 - 100 ppm	320	320 + 100 ppm	ps

Notes:

1. For recommended operating conditions, see Table 3.

3.22.9.2.2 XAUI receiver AC timing specifications

This table defines the receiver AC specifications for XAUI. RefClk jitter is not included.

Table 109. XAUI receiver AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	—	—	0.37	UI p-p	2
Combined deterministic and random jitter tolerance	J_{DR}	—	—	0.55	UI p-p	2
Total jitter tolerance	J_T	—	—	0.65	UI p-p	2, 3
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 3.125 GBaud	UI	320 - 100 ppm	320	320 + 100 ppm	ps	—

Notes:

1. For recommended operating conditions, see Table 3.
2. Measured at receiver
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

3.22.10 10GBase-KR interface

This section describes the 10GBase-KR clocking requirements and its DC and AC electrical characteristics.

3.22.10.1 10GBase-KR clocking requirements for SD1_REF_CLK*n* and SD1_REF_CLK*n*_B

Only SerDes 1 (SD1_REF_CLK[1:2] and SD1_REF_CLK[1:2]_B) may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks .

3.22.10.2 10GBase-KR DC electrical characteristics

This section describes the DC electrical characteristics for 10GBase-KR.

3.22.10.2.1 10GBase-KR transmitter DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 110. 10GBaseKR transmitter DC electrical characteristics (XV_{DD} = 1.35V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800	-	1200	mV	2
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	3
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	4
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	5
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	6
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	7
Differential resistance	T_{RD}	80	100	120	Ω	-

1. For recommended operating conditions, see Table 3.
2. LNmTECR0[EQ_AMP_RED] = 000000
3. LNmTECR0[EQ_POST1Q] = 00011
4. LNmTECR0[EQ_POST1Q] = 01000
5. LNmTECR0[EQ_POST1Q] = 01010
6. LNmTECR0[EQ_POST1Q] = 01100
7. LNmTECR0[EQ_POST1Q] = 10000

3.22.10.2.2 10GBase-KR receiver DC electrical characteristics

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 111. 10GBase-KR receiver DC electrical characteristics (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	-	-	1200	mV	-
Differential resistance	R_{RD}	80	-	120	Ω	-

1. For recommended operating conditions, see Table 3.

3.22.10.3 10GBase-KR AC timing specifications

This section describes the AC timing specifications for 10GBase-KR.

3.22.10.3.1 10GBase-KR transmitter AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

Table 112. 10GBase-KR transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s
Uncorrelated high probability jitter/Random jitter	U_{HPJ}/R_J	-	-	0.15	UI p-p
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p
1. For recommended operating conditions, see Table 3.					

3.22.10.3.2 10GBase-KR receiver AC timing specifications

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 113. 10GBase-KR receiver AC timing specifications[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s	-
Random jitter	R_J	-	-	0.130	UI p-p	-
Sinusodial jitter, maximum	$S_{J\text{-}max}$	-	-	0.115	UI p-p	-
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	-
Total jitter	T_J	-	-	See Note 1	UI p-p	1
1. The total jitter (TJ) is per Interference tolerance test IEEE Standard 802.3ap-2007 specified in Annex 69A. 2. For recommended operating conditions, see Table 3.						

3.22.11 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC-coupled operation is supported.

3.22.11.1 1000Base-KX DC electrical characteristics

3.22.11.1.1 1000Base-KX transmitter DC specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (_TXn_P and _TXn_N).

Table 114. 1000Base-KX transmitter DC specifications

Parameter	Symbols	Min	Typ	Max	Units	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800	—	1600	mV	1
Differential resistance	T_{RD}	80	100	120	Ω	—
Notes: 1. SRDSxLNmTECR0[AMP_RED]=00_0000. 2. For recommended operating conditions, see Table 3.						

3.22.11.1.2 1000Base-KX receiver DC specifications

Table below provides the 1000Base-KX receiver DC timing specifications.

Table 115. 1000Base-KX receiver DC specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Input differential voltage	$V_{RX-DIFFp-p}$	—	—	1600	mV	1
Differential resistance	T_{RDIN}	80	—	120	Ω	—
Notes: 1. For recommended operating conditions, see Table 3.						

3.22.11.2 1000Base-KX AC electrical characteristics

3.22.11.2.1 1000Base-KX transmitter AC specifications

Table below provides the 1000Base-KX transmitter AC specification.

Table 116. 1000Base-KX transmitter AC specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Baud rate	T_{BAUD}	1.25 - 100ppm	1.25	1.25 + 100ppm	Gb/s	—

Table continues on the next page...

Table 116. 1000Base-KX transmitter AC specifications (continued)

Parameter	Symbols	Min	Typical	Max	Units	Notes
Uncorrelated high probability jitter/ random jitter	$T_{UHPJ}T_{RJ}$	—	—	0.15	UI p-p	—
Deterministic jitter	T_{DJ}	—	—	0.10	UI p-p	—
Total jitter	T_{TJ}	—	—	0.25	UI p-p	1
Notes: 1. Total jitter is specified at a BER of 10^{-12}. 2. For recommended operating conditions, see Table 3.						

3.22.11.2.2 1000Base-KX receiver AC specifications

Table below provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

Table 117. 1000Base-KX receiver AC specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Receiver baud rate	R_{BAUD}	1.25 - 100ppm	1.25	1.25 + 100ppm	Gb/s	—
Random jitter	R_{RJ}	—	—	0.15	UI p-p	1
Sinusoidal jitter, maximum	R_{SJ-max}	—	—	0.10	UI p-p	2
Total jitter	R_{TJ}	—	—	See Note 3	UI p-p	2
Notes: 1. Random jitter is specified at a BER of 10^{-12}. 2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007. 3. Per IEEE 802.3ap-clause 70. 4. The AC specifications do not include Refclk jitter. 5. For recommended operating conditions, see Table 3.						

4 Hardware design considerations

4.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 118. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency										Unit	Notes
	1600 MHz		1800 MHz		2000 MHz/800 MHz		2000 MHz/700 MHz		2100 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Core frequency	800	1600	800	1800	800	2000	800	2000	800	2100	MHz	1
Coherency Domain frequency	1000	1200	1000	1400	1000	1600	1000	1400	1000	1600	MHz	
Platform clock frequency	500	600	500	700	500	800	500	700	500	800	MHz	1
Memory bus clock frequency (DDRC1, DDRC2)	625	800	625	933	625	1066	625	1066	625	1066	MHz	1, 2
Memory bus clock frequency (DDRC3)	625	800	625	800	625	800	625	800	625	800	MHz	1, 2
IFC clock frequency	-	100	-	100	-	100	-	100	-	100	MHz	3
AIOP/WRIOP	500	600	500	700	500	800	500	700	500	800	MHz	

Notes:

1. **Caution:** The coherency domain clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, coherency domain and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR4 data rate.

3. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by half of the platform clock frequency divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

4.2 Power supply design

For additional details on the power supply design, see AN4977, *QorIQ LS2088A Family Design Checklist*.

4.2.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip. V_{DD} supply should be separated from the SerDes 1.0 V supply SV_{DD}. It is required in order to control the V_{DD} supply only.

NOTE

During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating V_{DD} at initial start-up of 1.05 V. It is highly recommended to select a regulator with a Vout range of at least 0.875 V to 1.1 V, with a resolution of 12.5 mV or better, when implementing a VID solution.

The table below lists the valid VID efuse values that will be programmed at the factory for this chip.

Table 119. Fuse Status Register (DCFG_CCSR_FUSESR)

Binary value of DA_V / DA_ALT_V	V_{DD} voltage
00000	default (1.05 V)
00010	0.9750 V
01000	0.9000 V
10000	1.0000 V
10010	1.0250 V
All other values	Reserved

For additional information on VID, see the chip reference manual.

5 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 120. Package thermal characteristics[1]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	13	°C/W	
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	10	°C/W	
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	8	°C/W	
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	6	°C/W	
Junction to board	—	$R_{\Theta JB}$	3	°C/W	
Junction to case top	—	$R_{\Theta JCtop}$	0.3	°C/W	
Junction to Lid top	—	$R_{\Theta JLtop}$	0.1	°C/W	

Table continues on the next page...

Table 120. Package thermal characteristics[1] (continued)

Rating	Board	Symbol	Value	Unit	Notes

Notes:

1. See "Thermal management information" in the design checklist for additional details.

2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

4. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

5. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

6. Junction-to-Lid-Top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

5.1 Temperature diode

The chip has a temperature diode that can be used to monitor its temperature by using some external temperature monitoring devices (such as Analog Devices, ADT7481A). For more information, see AN4787.

The followings are the specifications of the chip temperature diode:

- Operating range: 10 - 230 μA
- Ideality factor over temperature range 85°C - 105°C, n = 1.006 ± 0.003, with approximate error ± 1 °C and error under ± 3 °C for temperature range 0 °C to 85 °C.

6 Package information

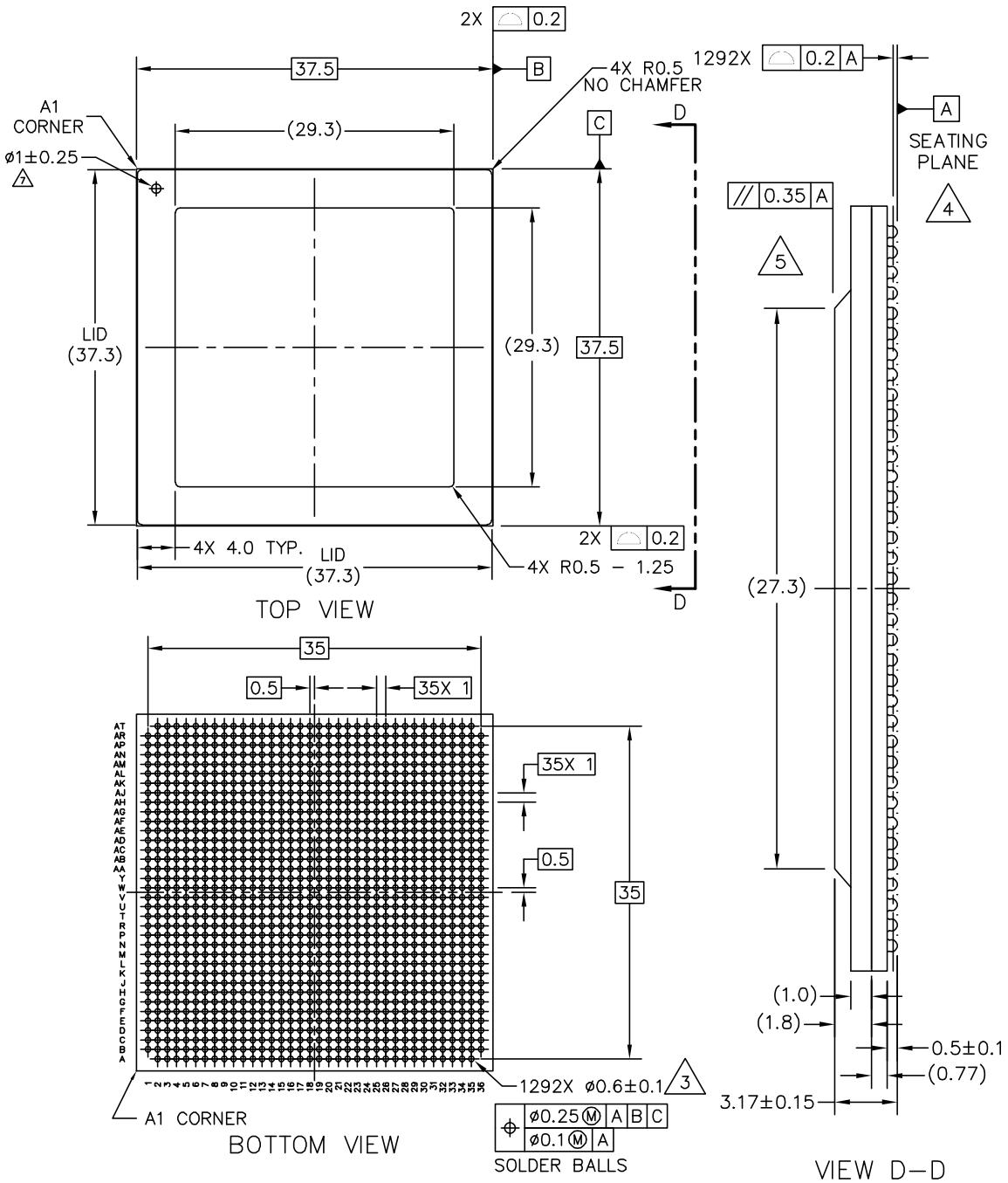
6.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 37.5 mm x 37.5 mm, 1292 flip-chip plastic lidded ball grid array (FC-PBGA).

- Package outline—37.5 mm x 37.5 mm
- Interconnects—1292
- Ball Pitch—1 mm
- Ball Diameter (typical)—0.6 mm
- Solder Balls—96.5% Sn, 3% Ag, 0.5% Cu
- Module height—3.02 mm (minimum), 3.17 mm (typical), 3.32 mm (maximum)

6.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.



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TITLE: FC PBGA, WITH LID, 37.5 X 37.5 X 3.17 PKG, 1 MM PITCH, 1292 I/O	DOCUMENT NO: 98ASA00618D	REV: O
	STANDARD: NON–JEDEC	
	19 MAY 2014	

Figure 83. Mechanical dimensions of the FC-PBGA with full lid

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 thru hole shall be centered within foot area.
8. 37.7 mm maximum package assembly (lid + laminate) X and Y.

7 Security fuse processor

This chip implements the QorIQ platform's trust architecture, supporting capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.80 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

8.1 Part numbering nomenclature

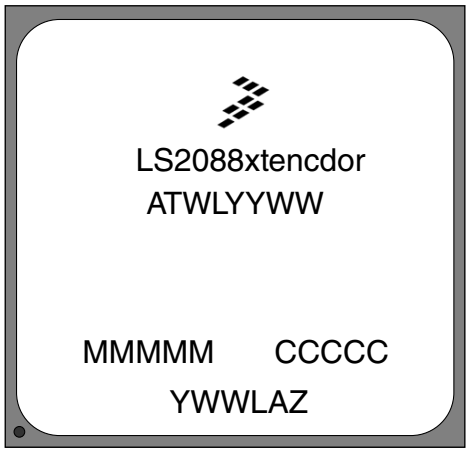
This table provides the NXP Layerscape platform part numbering nomenclature.

Table 121. Part numbering nomenclature

q	*p*	*g*	*c*	*u*	*c*	*t*	*e*	*n*	*c*	*d*	*o*	r
Qual Status	**Product Generation**	**Performance Level**	**Number of Cores**	**Unique ID**	**Core Type**	**Temperature Range**	**Encryption**	**Package**	**Top Core Freq**	**DDR Freq**	**Option Code**	**Revision**
(blank) = Qualified P = Pre-qual S = Special	LS = Layerscape	2	08 04	8 = AIOP on, L2 switch on	A = Arm	S = 0–105°C X = -40–105°C	E = Export controlled crypto hardware enabled N = Export controlled crypto hardware disabled	7 = FC-PBGA	Q = 1.6 GHz T = 1.8 GHz V = 2.0 GHz 1 = 2.1 GHz	Q = 1.6 GHz T = 1.867 GHz 1 = 2.133 GHz	Blank = Standard device 7 = Platform speed limited to 700 MHz. Only available for 2GHz core.	B = Rev 1.1

8.2 Part marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Legend:
LS2088xtencdor is the part marking on the die. See the corresponding orderable part number in the table above.
ATWLYYWW is the test traceability code.
MMMMM is the mask number.
WLSQXXXXXX is the lot number.
CCCCC is the country code.
YWWLAZ is the assembly traceability code.

Figure 84. Part marking for FC-PBGA chip

9 Revision history

This table summarizes revisions to this document.

Table 122. Revision history

Revision	Date	Description
3	09/2020	• Changed the value of Cryptography acceleration from 10 Gbps to 20 Gbps in Features • Updated Power characteristics, added a new row for 2000/700 MHz core speed • Added 2000/700 MHz core speed to Clock ranges • Added the option code in Part numbering nomenclature
2	05/2020	• In the pinout list, added a new note 29 to D1_MALERT_B/D2_MALERT_B/D3_MALERT_B • Updated Table 23 • Corrected table reference in DDR4 SDRAM interface output AC timing specifications
1	11/2018	• Updated Figure 12 • Added note 3 in Table 45 • Added Temperature diode
0	04/2018	Initial release

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