

74AC377 • 74ACT377

Octal D-Type Flip-Flop with Clock Enable

General Description

The AC/ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

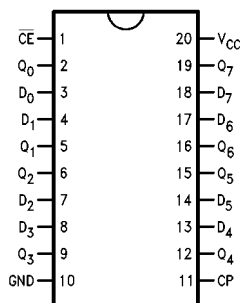
- I_{CC} reduced by 50%
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See 273 for master reset version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- ACT377 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC377PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT377PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

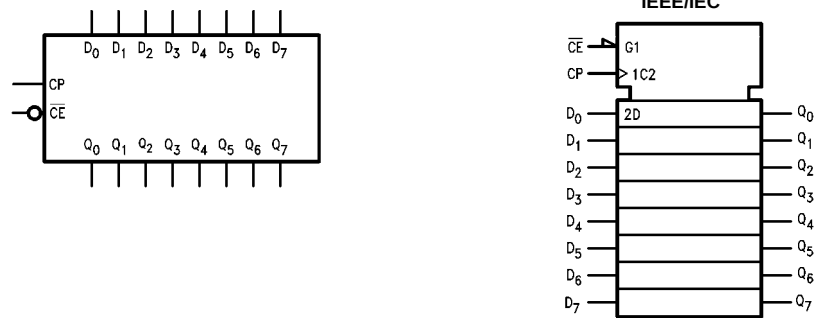


Pin Descriptions

Pin Names	Description
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0-Q_7	Data Outputs
CP	Clock Pulse Input

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Logic Symbols

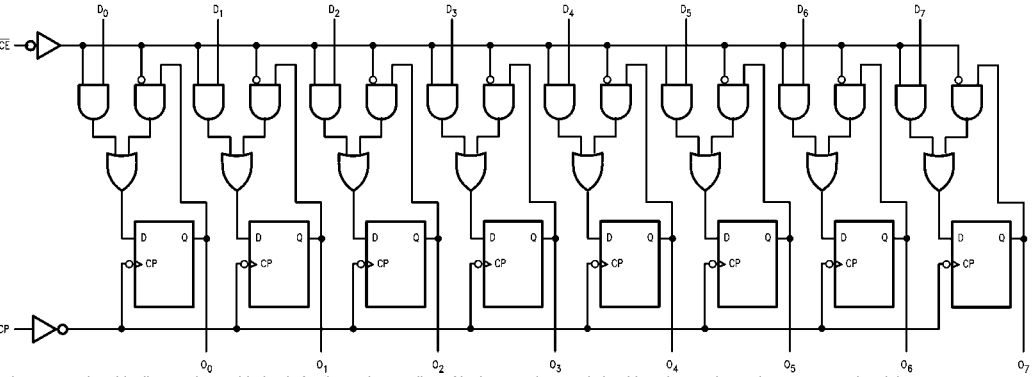


Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load '1'		L	H	H
Load '0'		L	L	L
Hold (Do Nothing)		H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = −12 mA I _{OH} = −24 mA I _{OH} = −24 mA (Note 2)
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA I _{OL} = 24 mA I _{OL} = 24 mA (Note 2)
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 3)	5.5			−75	mA	V _{OHD} = 3.85V Min
I _{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V _{IN} = V _{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1V or V _{CC} -0.1V
		5.5	1.5	2.0				
V _{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1V or V _{CC} -0.1V
		5.5	1.5	0.8				
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76		V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 5)
		5.5		4.86	4.76			
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44		V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 5)
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5		mA	V _I = V _{CC} - 2.1V
I _{OLD}	Minimum Dynamic	5.5			75		mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 6)	5.5			-75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0		μA	V _{IN} = V _{CC} or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = +25°C			T _A = -40°C to +85°C		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	3.3	90	125		75		MHz
		5.0	140	175		125		
t _{PLH}	Propagation Delay CP to Q _n	3.3	3.0	8.0	13.0	1.5	14.0	ns
		5.0	2.0	6.0	9.0	1.5	10.0	
t _{PHL}	Propagation Delay CP to Q _n	3.3	3.5	8.5	13.0	2.0	14.5	ns
		5.0	2.5	6.5	10.0	1.5	11.0	

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC

Symbol	Parameter	V _{CC} (V) (Note 8)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW D _n to CP	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
t _H	Hold Time, HIGH or LOW D _n to CP	3.3	-2.0	0	0	ns
		5.0	-1.0	1.0	1.0	
t _S	Setup Time, HIGH or LOW $\overline{\text{CE}}$ to CP	3.3	4.0	6.0	7.5	ns
		5.0	2.5	4.0	4.5	
t _H	Hold Time, HIGH or LOW $\overline{\text{CE}}$ to CP	3.3	-3.5	0	0	ns
		5.0	-2.0	1.0	1.0	
t _W	CP Pulse Width HIGH or LOW	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	

Note 8: Voltage Range 3.3 is 3.0V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) (Note 9)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	5.0	140	175		125		MHz
t _{PLH}	Propagation Delay CP to Q _n	5.0	3.0	6.5	9.0	2.5	10.0	ns
t _{PHL}	Propagation Delay CP to Q _n	5.0	3.5	7.0	10.0	2.5	11.0	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

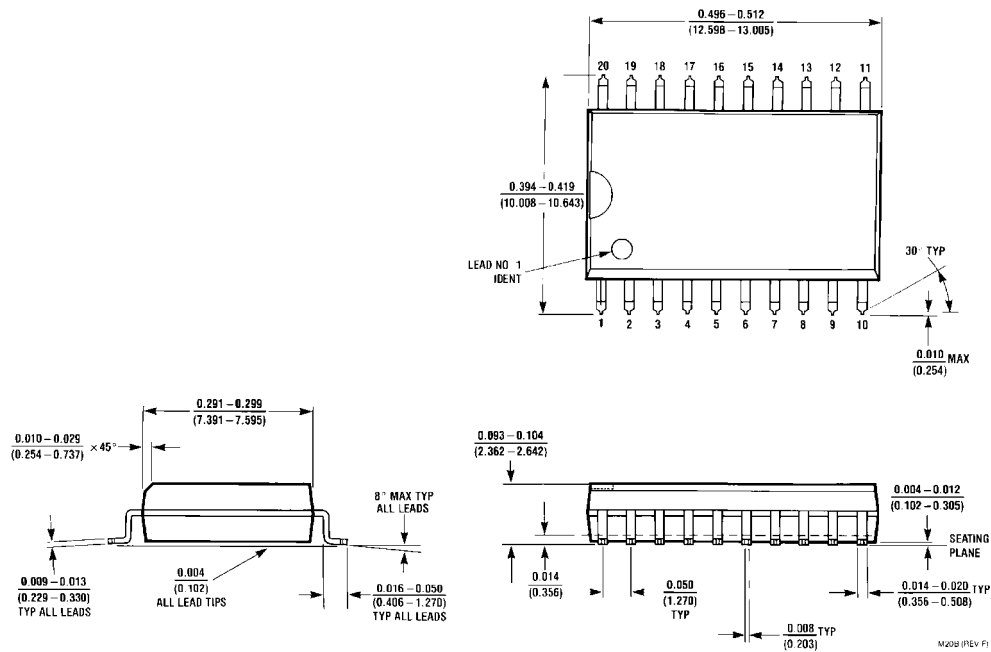
Symbol	Parameter	V _{CC} (V) (Note 10)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW D _n to CP	5.0	2.5	4.5	5.5	ns
t _H	Hold Time, HIGH or LOW D _n to CP	5.0	-1.0	1.0	1.0	ns
t _S	Setup Time, HIGH or LOW $\overline{\text{CE}}$ to CP	5.0	2.5	4.5	5.5	ns
t _H	Hold Time, HIGH or LOW $\overline{\text{CE}}$ to CP	5.0	-1.0	1.0	1.0	ns
t _W	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	90.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

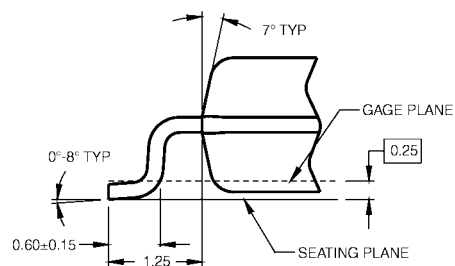


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

LAND PATTERN RECOMMENDATION


DIMENSIONS ARE IN MILLIMETERS

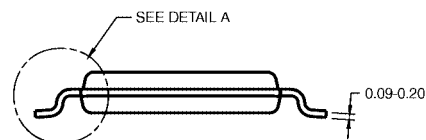
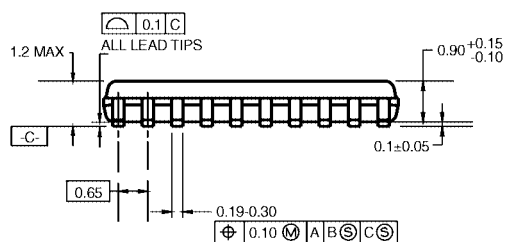
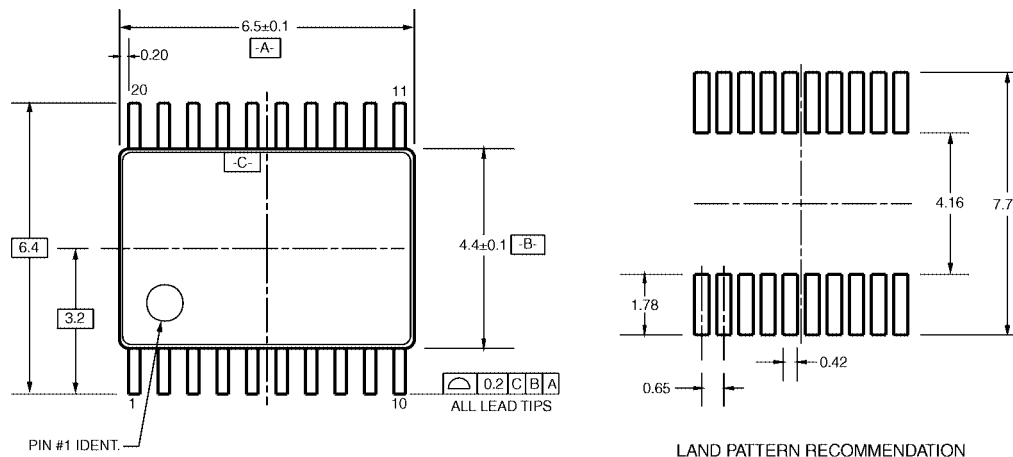

DETAIL A
NOTES:

- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

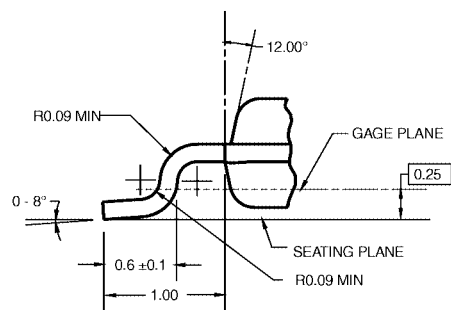


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

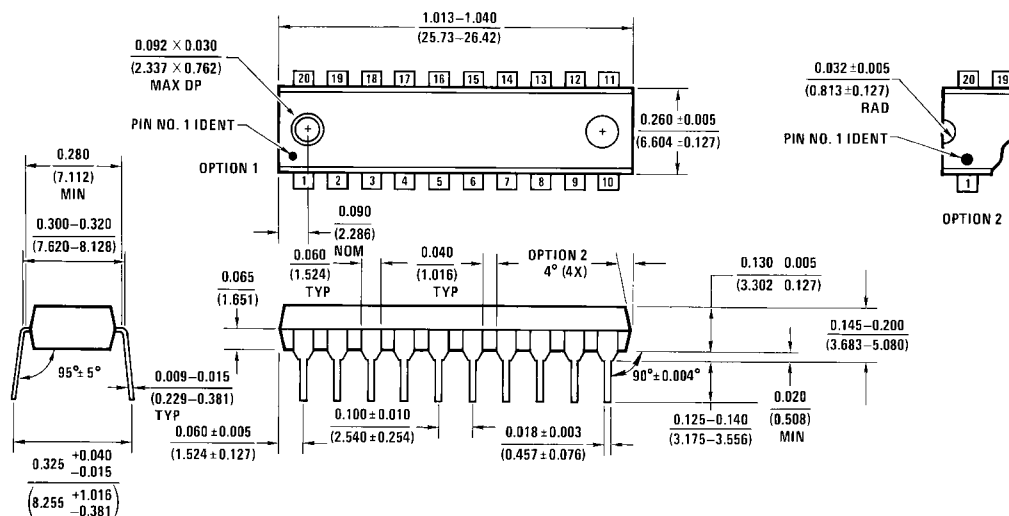
MTC20RevD1



DETAIL A

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com