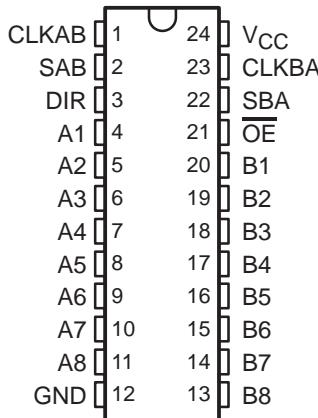


SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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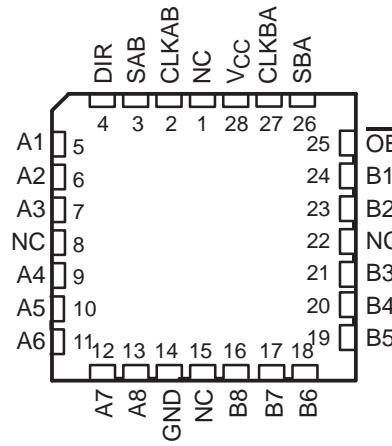
- Typical V_{OLP} (Output Ground Bounce)
 <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (-32 -mA I_{OH} , 64 -mA I_{OL})
- I_{off} Supports Partial-Power-Down Mode Operation

SN54ABT646A . . . JT OR W PACKAGE
SN74ABT646A . . . DB, DGV, DW, NS, NT, OR PW PACKAGE
(TOP VIEW)



- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54ABT646A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT646A devices.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – NT	Tube	SN74ABT646ANT	SN74ABT646ANT
	SOIC – DW	Tube	SN74ABT646ADW	ABT646A
		Tape and reel	SN74ABT646ADWR	
	SOP – NS	Tape and reel	SN74ABT646ANSR	ABT646A
	SSOP – DB	Tape and reel	SN74ABT646ADBR	AB646A
	TSSOP – PW	Tube	SN74ABT646APW	AB646A
		Tape and reel	SN74ABT646APWR	
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74ABT646ADGVR	AB646A
	CDIP – JT	Tube	SNJ54ABT646AJT	SNJ54ABT646AJT
	CFP – W	Tube	SNJ54ABT646AW	SNJ54ABT646AW
	LCCC – FK	Tube	SNJ54ABT646AFK	SNJ54ABT646AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54ABT646A, SN74ABT646A
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description/ordering information(continued)

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

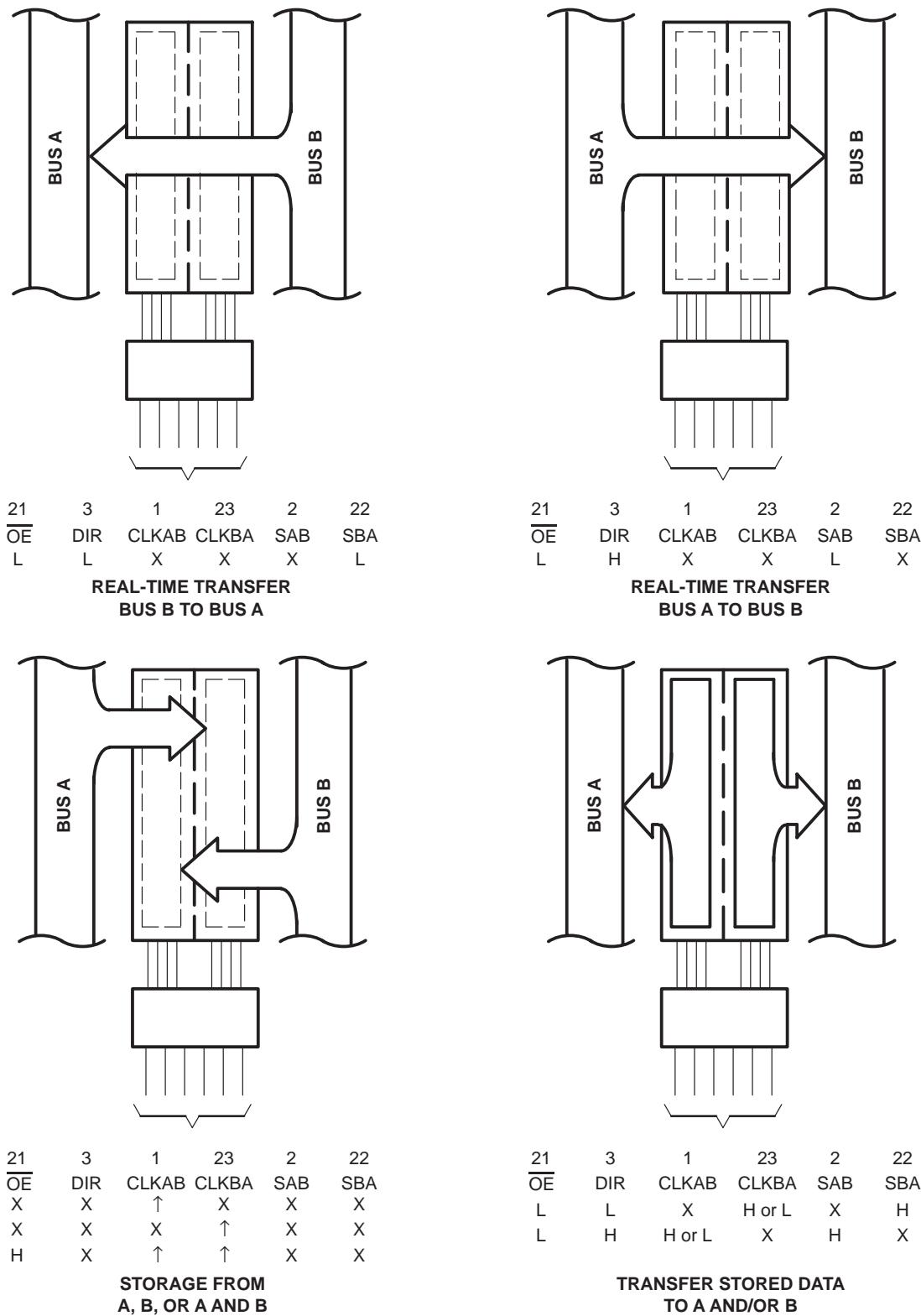
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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Pin numbers shown are for the DB, DGV, DW, JT, NS, NT, PW, and W packages.

Figure 1. Bus-Management Functions

SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

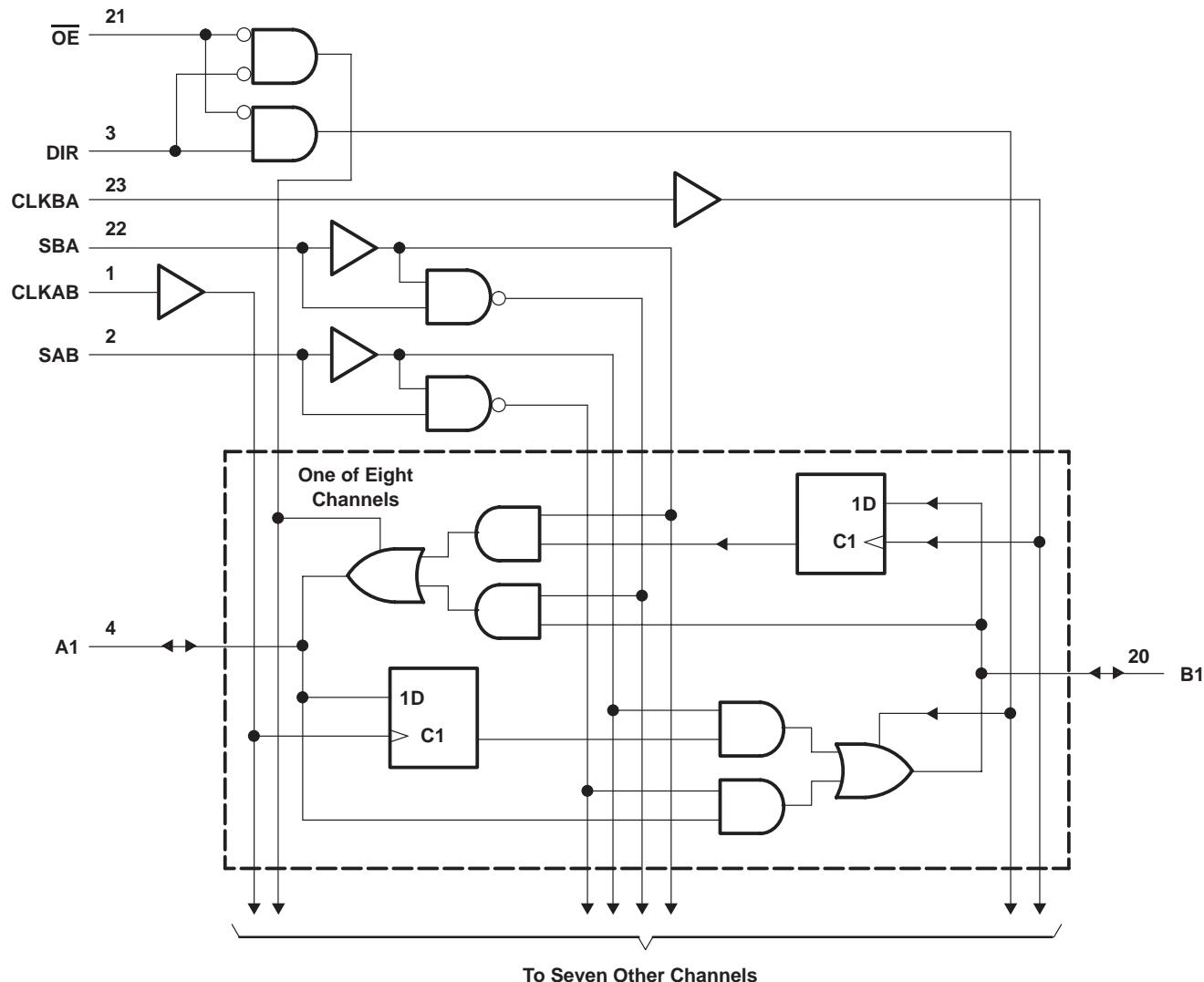
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FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data-output functions can be enabled or disabled by various signals at \overline{OE} and DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, NS, NT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-3.

recommended operating conditions (see Note 4)

		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		5		5	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA = 25°C			SN54ABT646A		SN74ABT646A		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
VIK	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
VOH	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2		2				
		I _{OH} = -32 mA	2*				2		
VOL	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V
		I _{OL} = 64 mA		0.55*				0.55	
V _{hys}		100							mV
I _I	Control inputs A or B ports	V _{CC} = 5.5 V, V _I = V _{CC} or GND	±1		±1		±1		μA
				±100		±100		±100	
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V			10§		10§		10§	μA
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V			-10§		-10§		-10§	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high		50		50		50	μA
I _{O¶}	V _{CC} = 5.5 V, V _O = 2.5 V	-50 -100 -180		-50 -180		-50 -180		-50 -180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	250		250		250		μA
		Outputs low	30		30		30		mA
		Outputs disabled	250		250		250		μA
ΔI _{CC} ‡	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V		7					pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		12					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ This data-sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		SN54ABT646A				UNIT	
		V _{CC} = 5 V, TA = 25°C		MIN	MAX		
		MIN	MAX				
f _{clock}	Clock frequency			125	125	MHz	
t _w	Pulse duration, CLK high or low			4	4	ns	
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑			3	3.5	ns	
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑			1.5	1.5	ns	

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OCTAL BUS TRANSCEIVERS AND REGISTERS
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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

			SN74ABT646A			UNIT	
			V _{CC} = 5 V, T _A = 25°C		MIN		
			MIN	MAX			
f _{clock}	Clock frequency			125	125	MHz	
t _w	Pulse duration, CLK high or low			4	4	ns	
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑			3	3	ns	
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑			0	0	ns	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT646A			UNIT	
			V _{CC} = 5 V, T _A = 25°C		MIN		
			MIN	TYP			
f _{max}			125	125	125	MHz	
t _{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	
t _{PHL}			1.7	4	5.1	6.7	
t _{PLH}	A or B	B or A	1.5	3	4.3	1.5	
t _{PHL}			1.5	3.3	4.6	5.6	
t _{PLH}	SAB or SBA†	B or A	1.5	4	5.7	1.5	
t _{PHL}			1.5	3.6	4.9	7.8	
t _{PZH}	OE	A or B	1.5	4.3	5.3	1.5	
t _{PZL}			3	5.8	8	10.5	
t _{PHZ}	OE	A or B	1.5	3.5	5.8	1	
t _{PLZ}			1.5	3	4	7.3	
t _{PZH}	DIR	A or B	1.5	4.5	5.7	1.5	
t _{PZL}			2.5	6.5	9	11	
t _{PHZ}	DIR	A or B	1.5	3.8	6.5	1	
t _{PLZ}			1.5	3.8	4.7	9	
						6.7	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**SN54ABT646A, SN74ABT646A
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS**

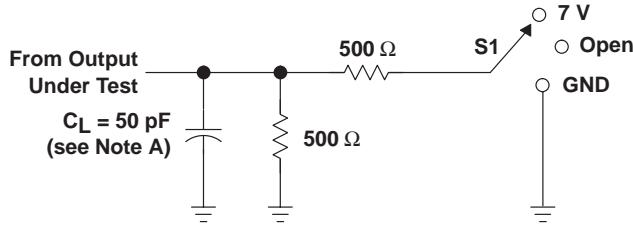
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 2)

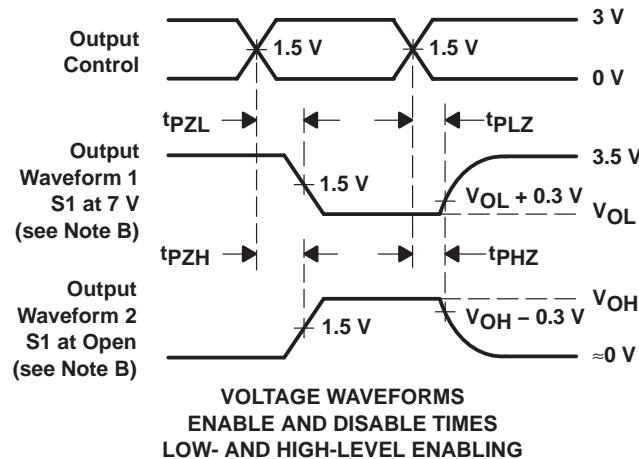
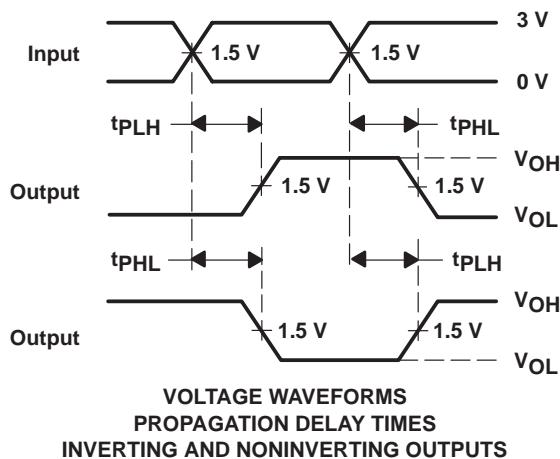
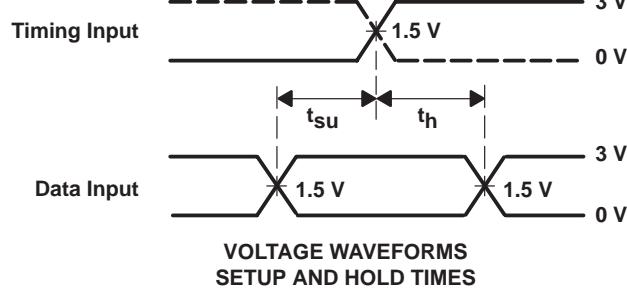
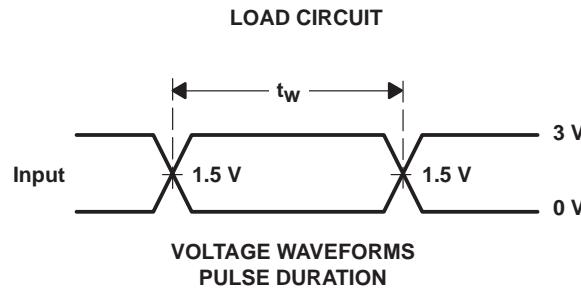
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT646A			UNIT		
			$V_{CC} = 5 \text{ V},$ $T_A = 25^\circ\text{C}$		MIN	TYP	MAX	
			MIN	TYP				
f_{max}			125		125		MHz	
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	3	4.3	1.5	4.8	ns
t_{PHL}			1.5	3.3	4.6	1.5	5.4	
t_{PLH}	SAB or SBA [†]	B or A	1.5	4	5.1	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	5.9	
t_{PZH}	\overline{OE}	A or B	1.5	4.3	5.3	1.5	6.3	ns
t_{PZL}			3	5.8	7.4	3	8.8	
t_{PHZ}	\overline{OE}	A or B	1.5	3.5	4.5	1.5	5	ns
t_{PLZ}			1.5	3	4	1.5	4.5	
t_{PZH}	DIR	A or B	1.5	4.5	5.7	1.5	6.7	ns
t_{PZL}			2.5	6.5	9	2.5	9.5	
t_{PHZ}	DIR	A or B	1.5	3.8	5	1.5	5.7	ns
t_{PLZ}			1.5	3.8	4.7	1.5	6	

[†] These parameters are measured with the internal output state of the storage register opposite that of the bus input.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9457702Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9457702Q3A SNJ54ABT 646AFK	Samples
5962-9457702QKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9457702QK A SNJ54ABT646AW	Samples
5962-9457702QLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9457702QL A SNJ54ABT646AJT	Samples
SN74ABT646ADBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		
SN74ABT646ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB646A	Samples
SN74ABT646ADGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB646A	Samples
SN74ABT646ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT646A	Samples
SN74ABT646ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT646A	Samples
SN74ABT646ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT646A	Samples
SN74ABT646ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT646A	Samples
SN74ABT646ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT646ANT	Samples
SN74ABT646APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB646A	Samples
SN74ABT646APWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
SNJ54ABT646AFK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9457702Q3A SNJ54ABT 646AFK	Samples
SNJ54ABT646AJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9457702QL A SNJ54ABT646AJT	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54ABT646AW	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9457702QK A SNJ54ABT646AW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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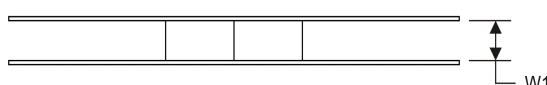
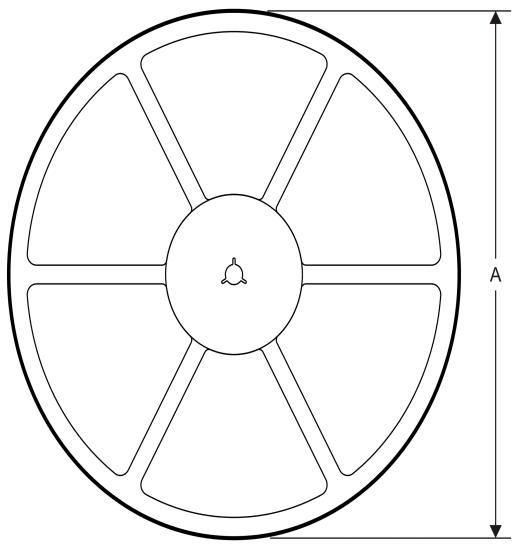
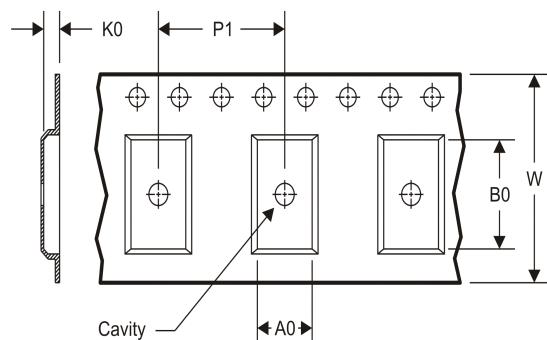
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OTHER QUALIFIED VERSIONS OF SN54ABT646A, SN74ABT646A :

- Catalog: [SN74ABT646A](#)
- Military: [SN54ABT646A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT646ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT646ADGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ABT646ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT646ANSR	SO	NS	24	2000	330.0	24.4	8.2	15.4	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

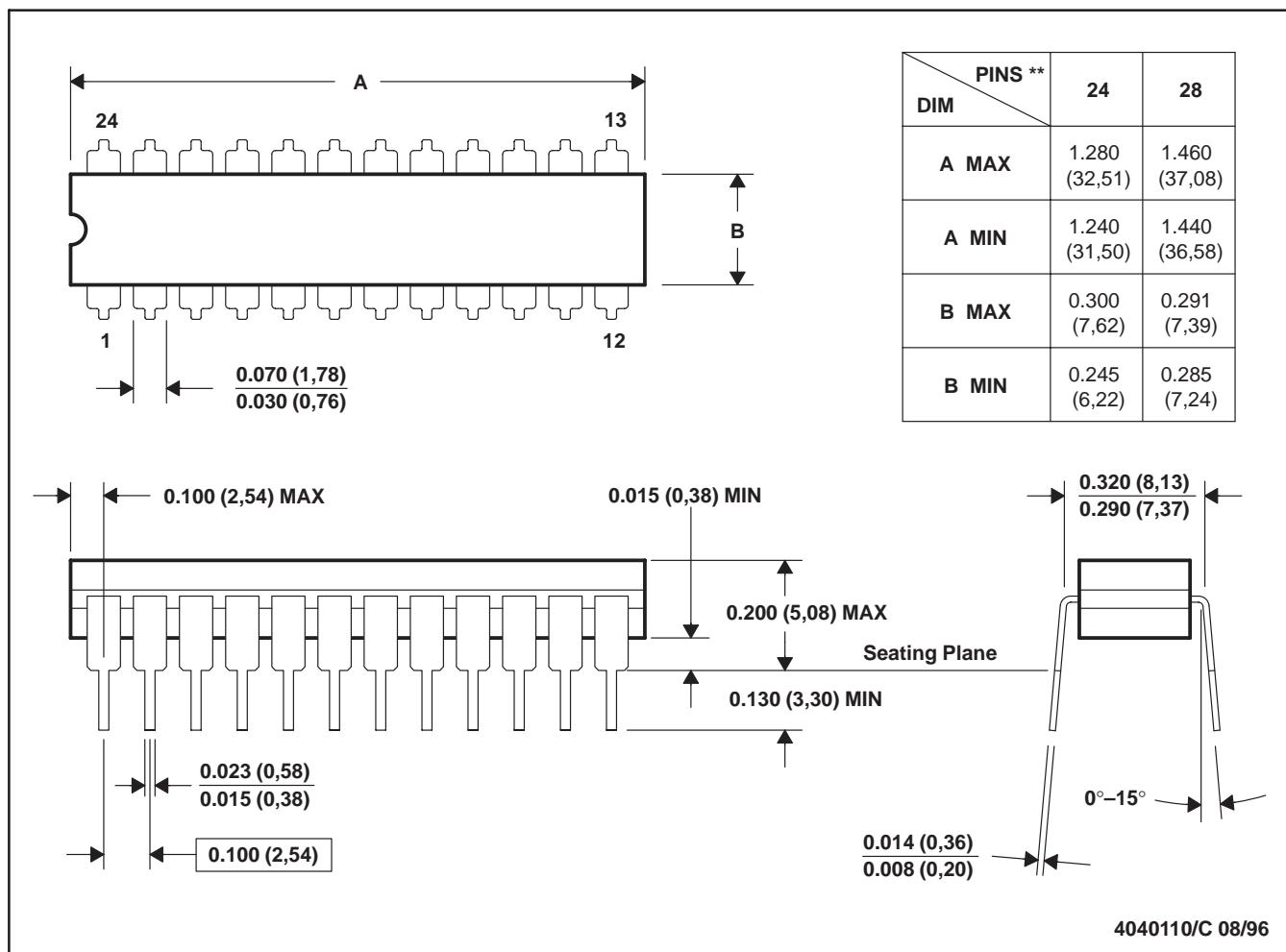

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT646ADBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74ABT646ADGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74ABT646ADWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74ABT646ANSR	SO	NS	24	2000	367.0	367.0	45.0

JT (R-GDIP-T**)

24 LEADS SHOWN

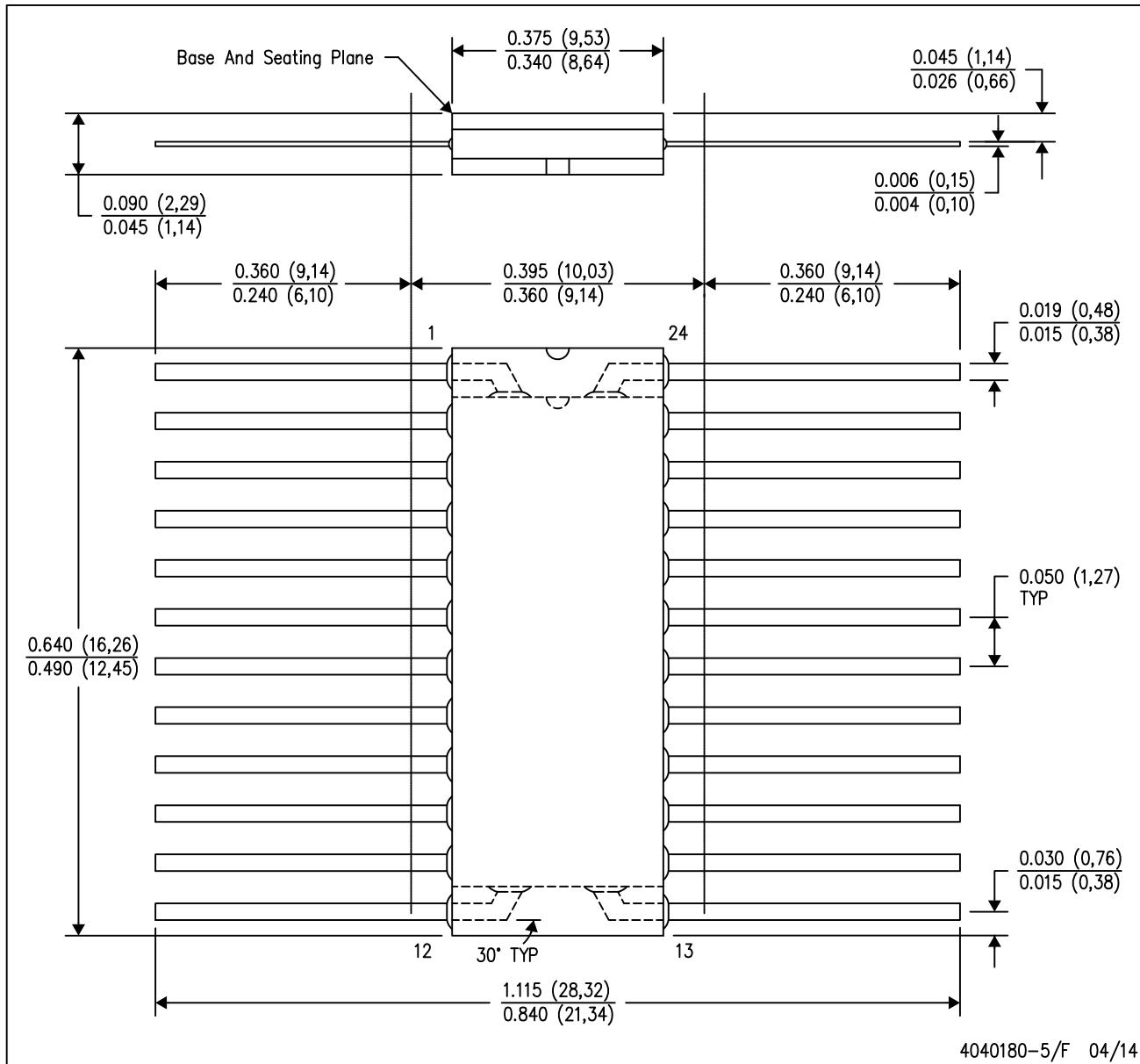
CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



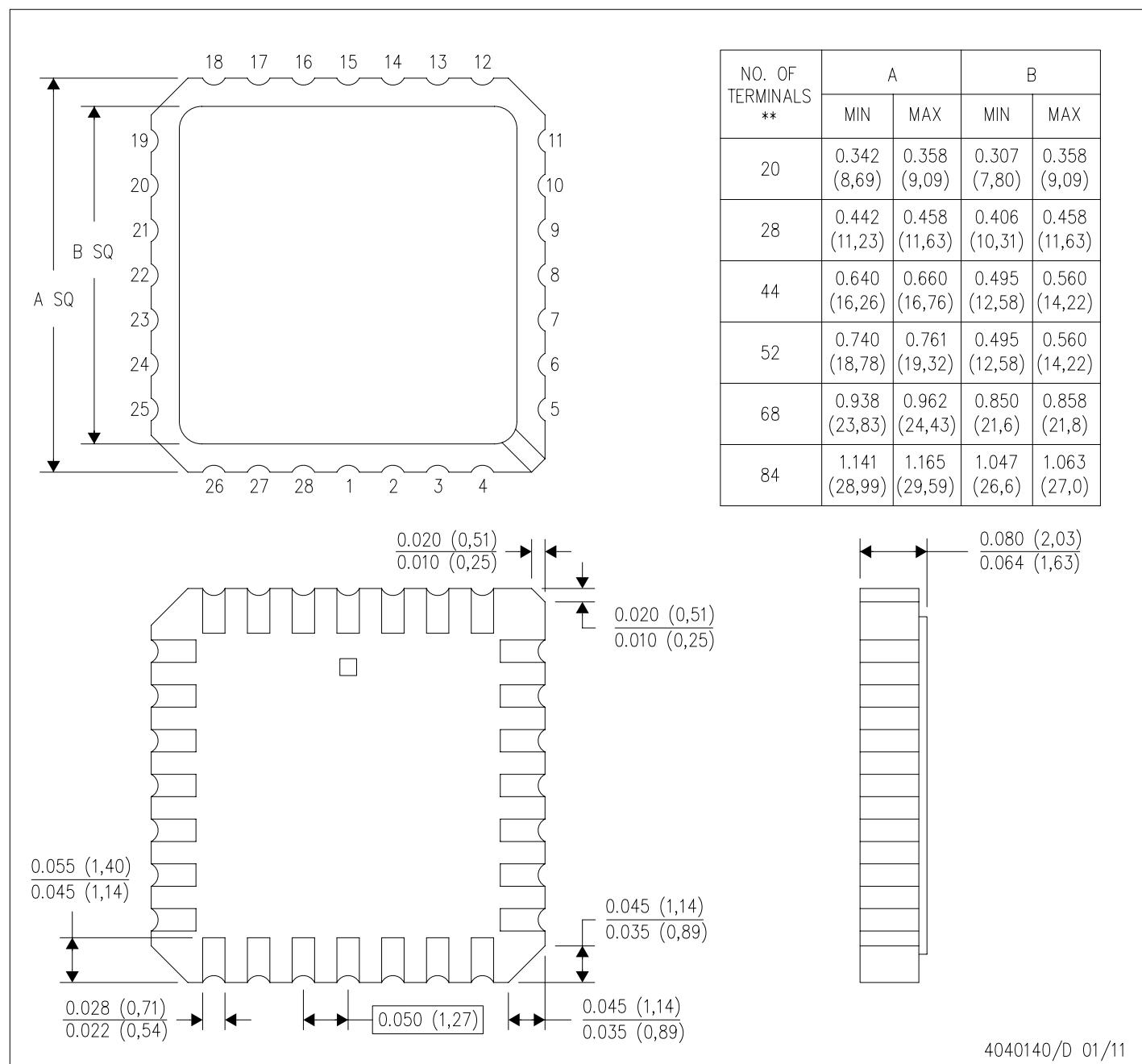
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

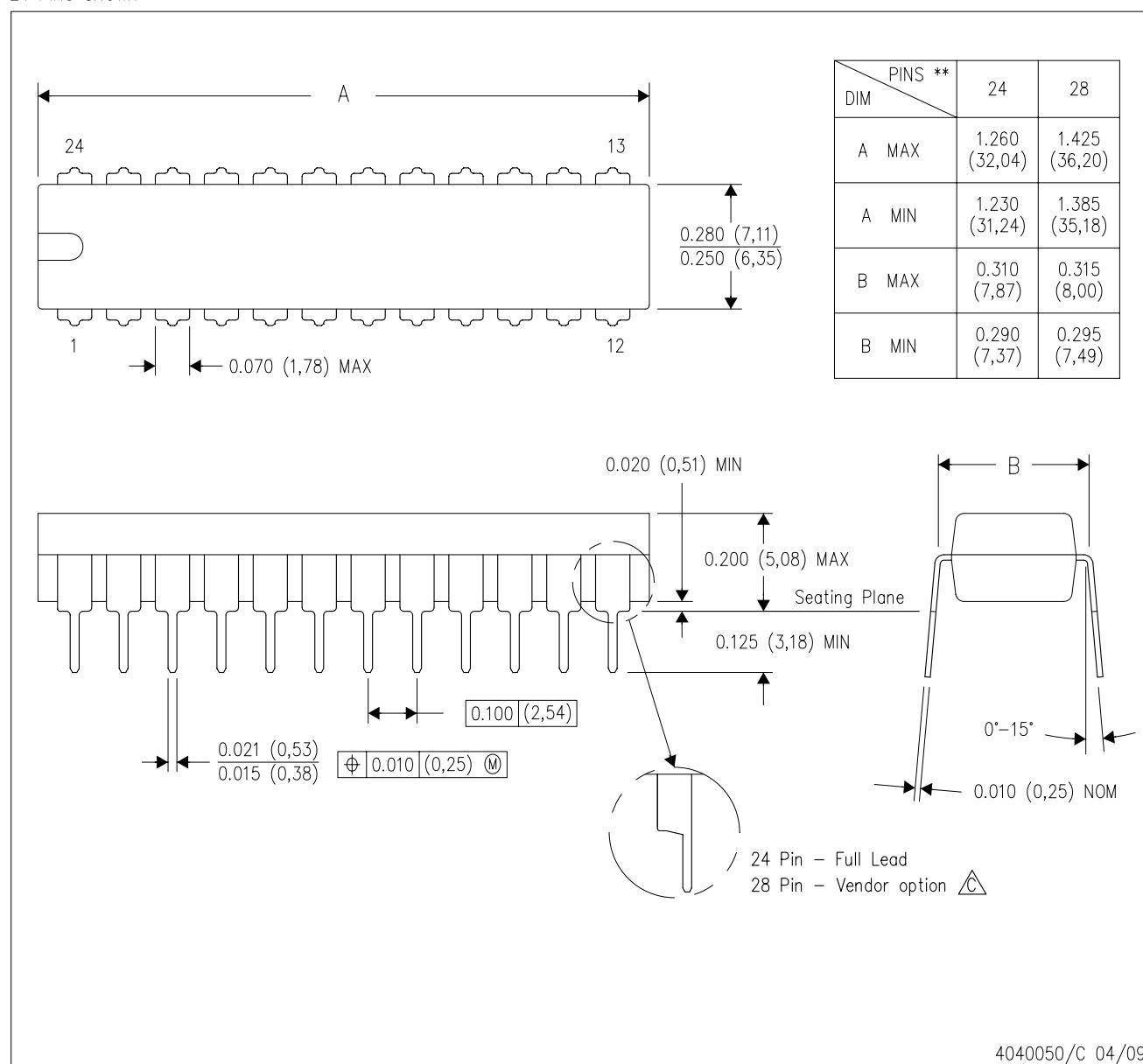
4040140/D 01/11

MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

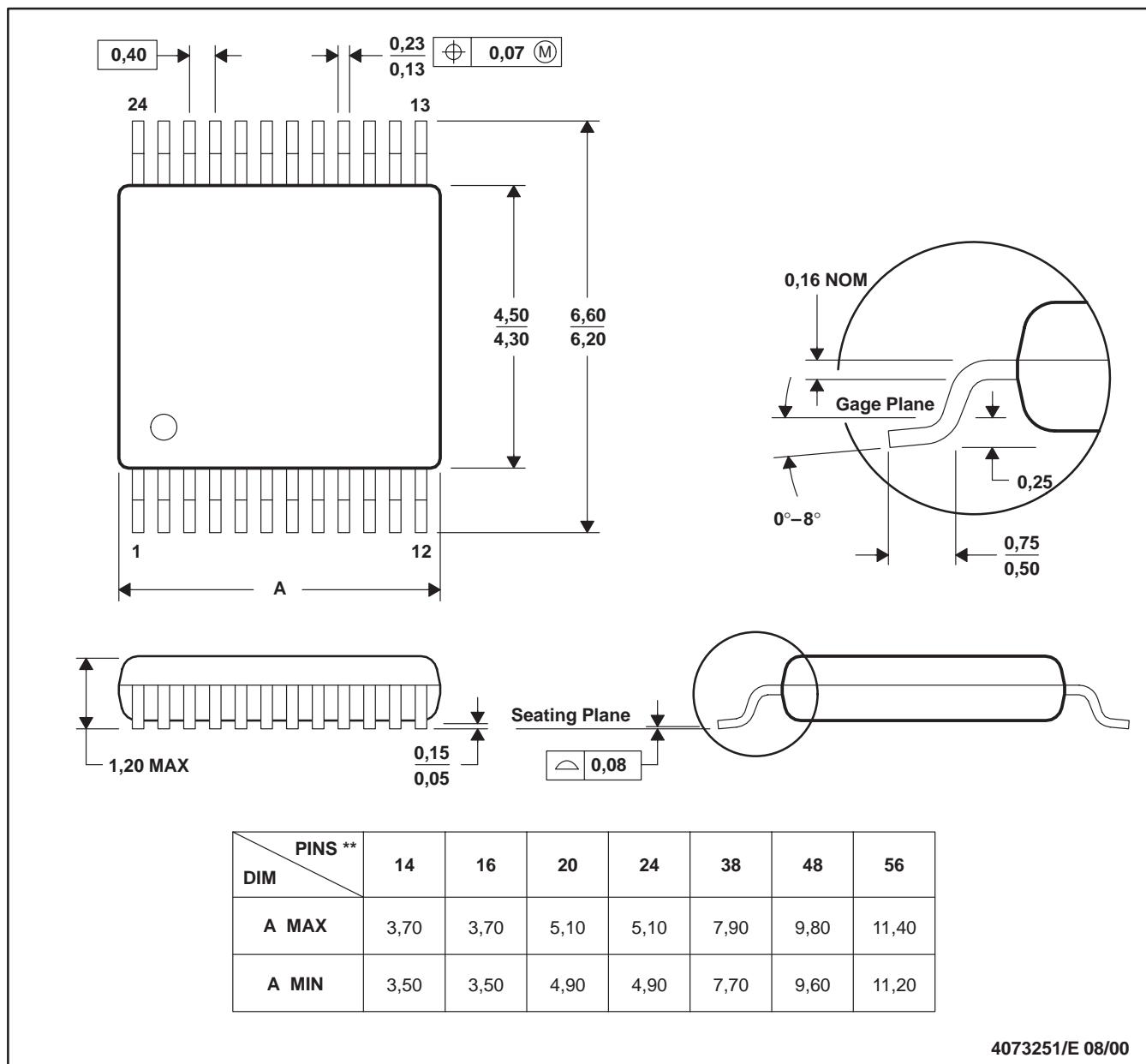
B. This drawing is subject to change without notice.

\triangle The 28 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

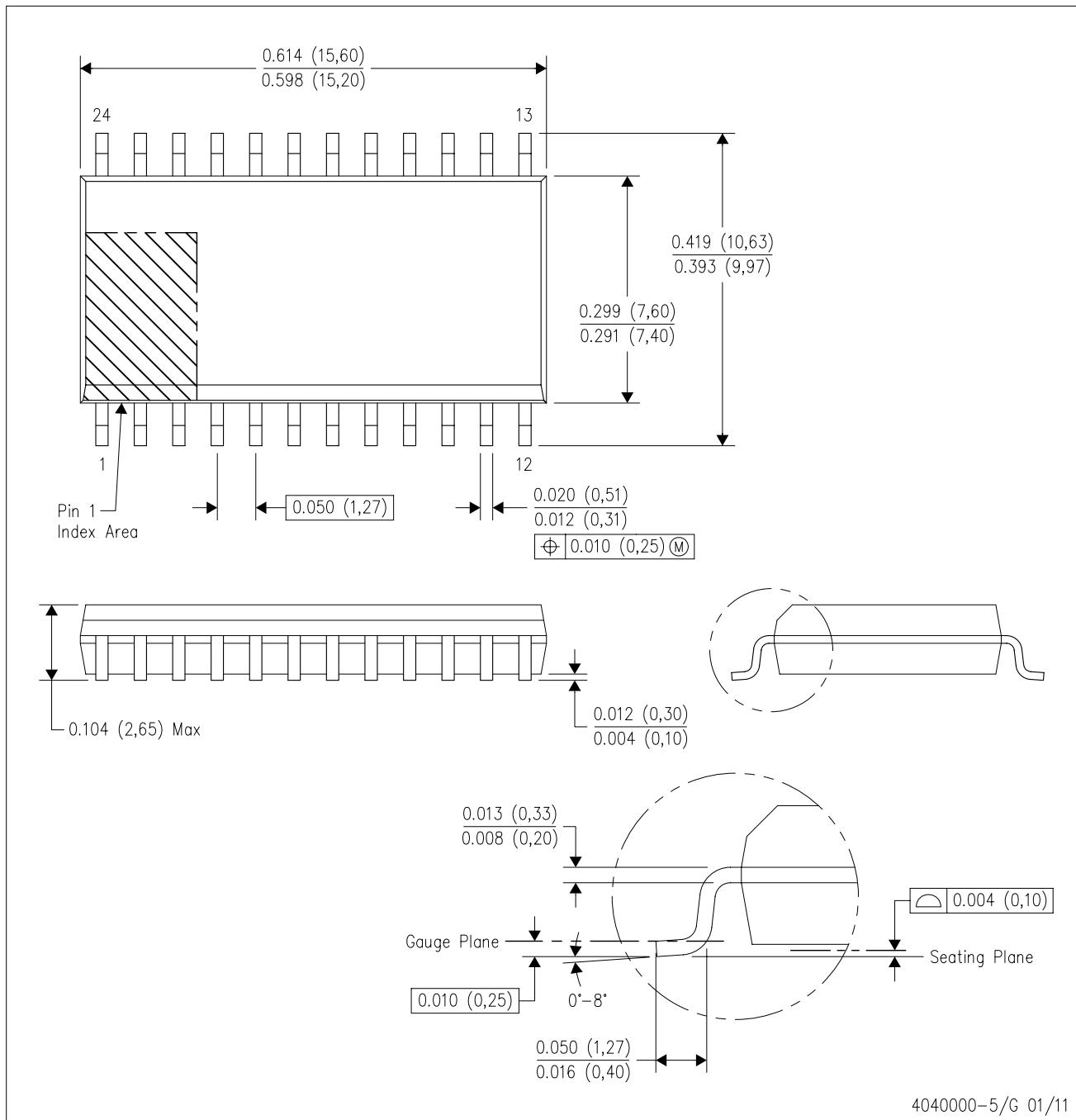
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

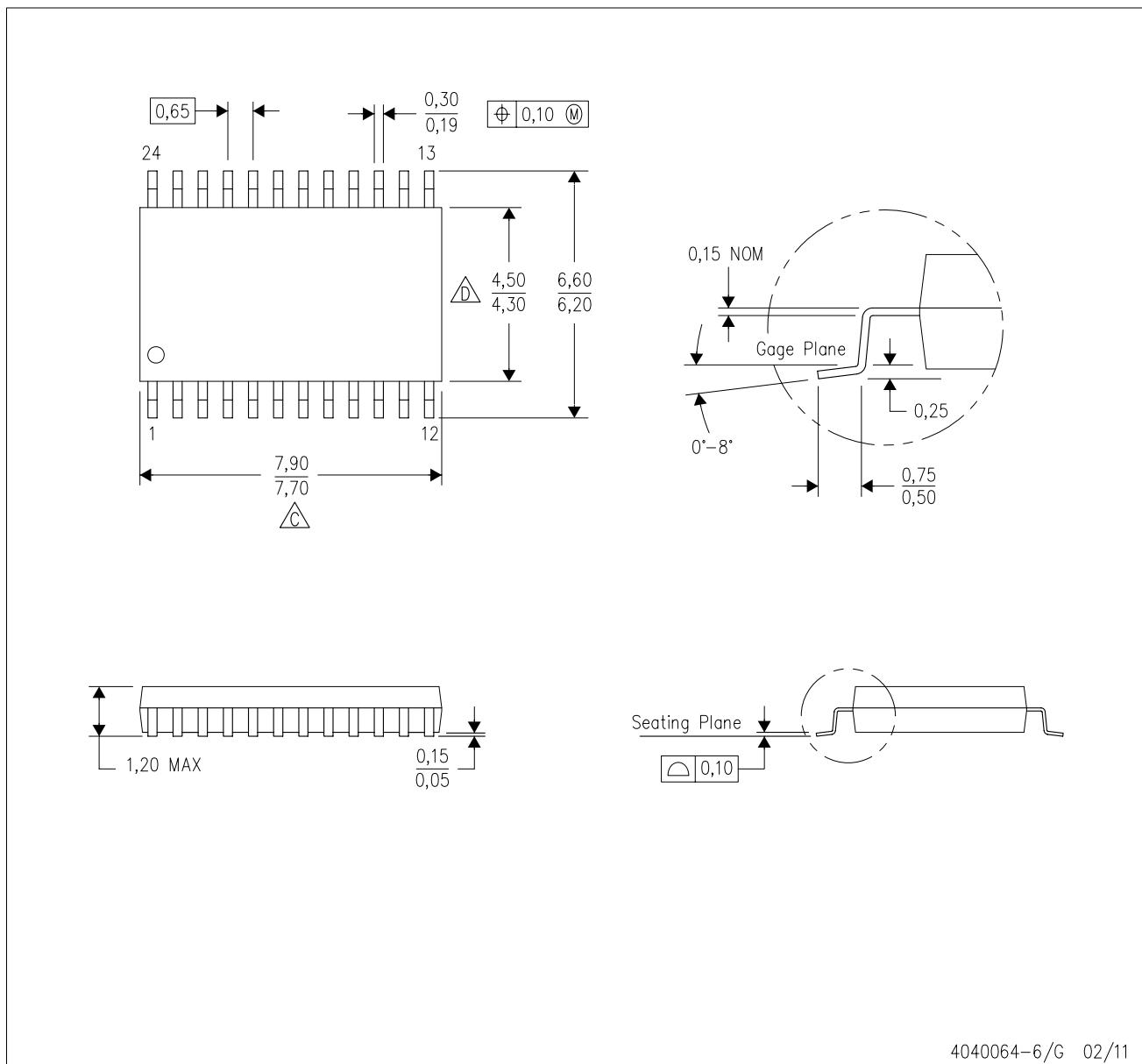


NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4040064-6/G 02/11

NOTES:

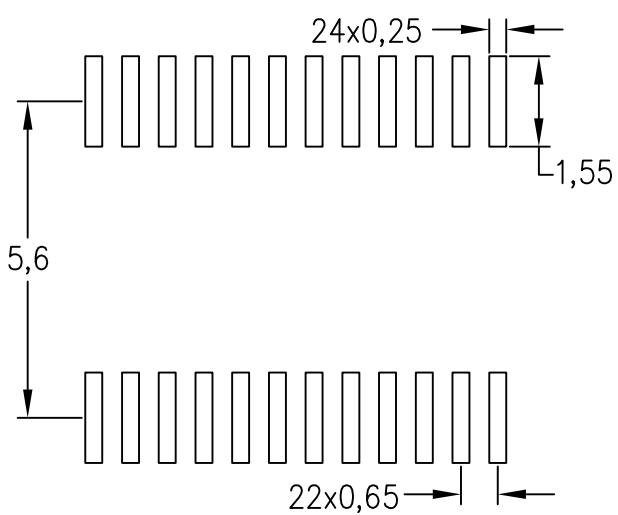
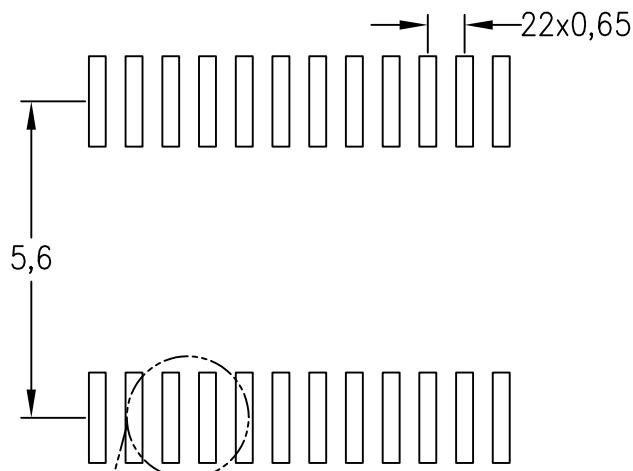
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
-  C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
-  D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

Pad Geometry

0,3
1,6
0,07
All Around

4211284-4/F 12/12

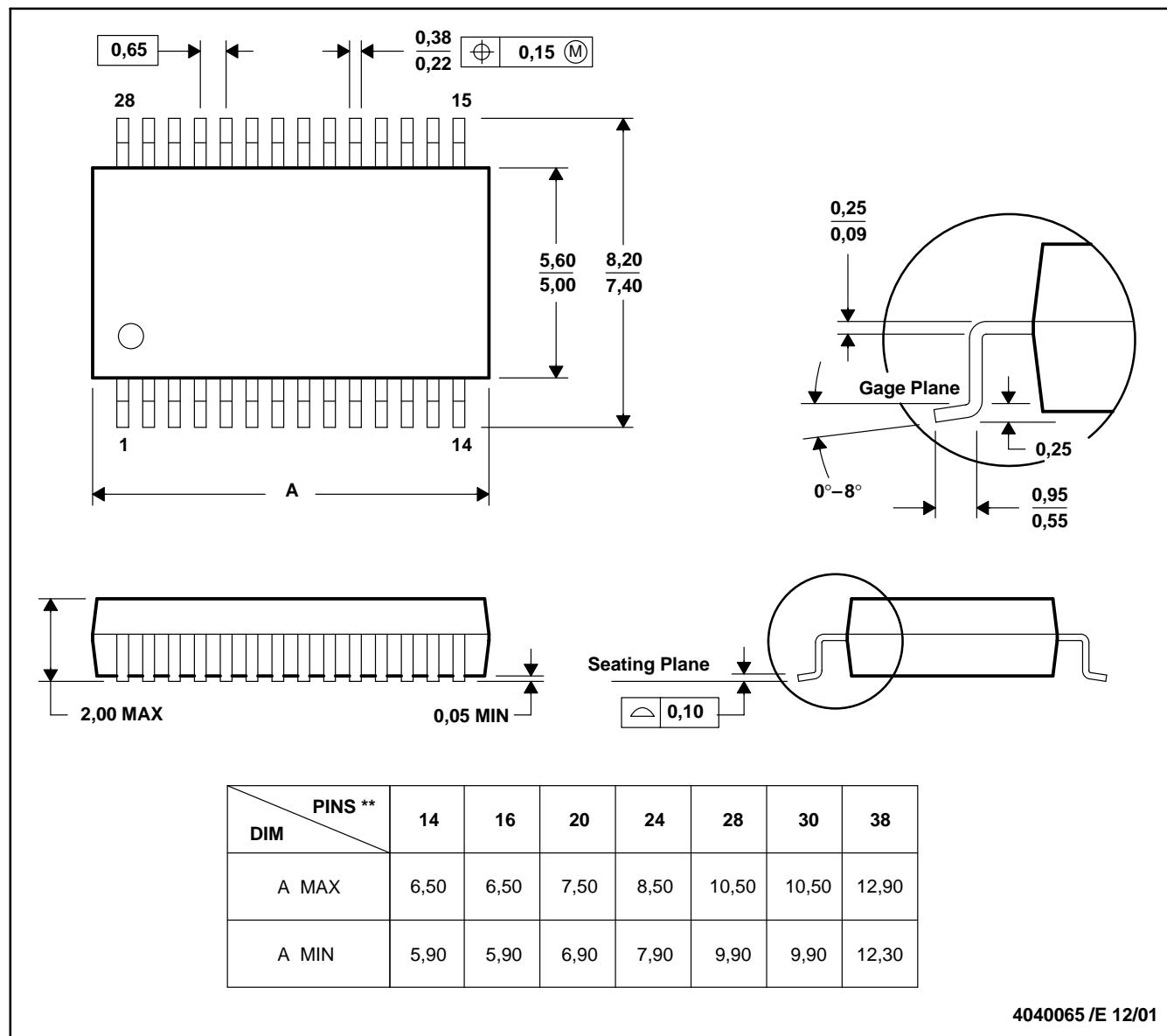
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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