

- State-of-the-Art **EPIC-IITM** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (-32-mA I_{OH} , 64-mA I_{OL})
- High-Impedance State During Power Up and Power Down
- Parity-Error Flag With Parity Generator/Checker
- Latch for Storage of Parity-Error Flag
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

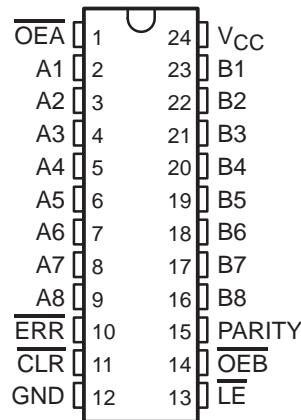
description

The 'ABT853 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error (ERR) output indicates whether or not an error in the B data has occurred. The output-enable (\overline{OEA} and \overline{OEB}) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT853 transceivers provide true data at their outputs.

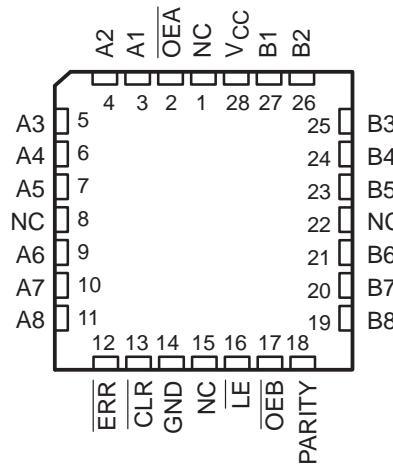
A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the \overline{ERR} flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable (\overline{LE}) and clear (\overline{CLR}) control inputs. When both \overline{OEA} and \overline{OEB} are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT853 . . . JT OR W PACKAGE
SN74ABT853 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT853 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN54ABT853, SN74ABT853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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description (continued)

The SN54ABT853 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT853 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						OUTPUTS AND I/Os				FUNCTION
<u>OEB</u>	<u>OEA</u>	<u>CLR</u>	<u>LE</u>	Σ OF H	Σ OF H	<u>A</u>	<u>B</u>	PARITY	<u>ERR</u> [‡]	
L	H	X	X	Odd		NA	A	L	NA	A data to B bus and generate parity
				Even				H		
H	L	X	L	NA	Odd		B	NA	H	B data to A bus and check parity
					Even				L	
H	L	H	H	NA	X		X	NA	NA	Store error flag
X	X	L	H	X	X		X	NA	NA	Clear error flag register
H	H	L	H	X			Z	Z	Z	Isolation [§] (parity check)
		X	L	L Odd						
		X	L	H Even						
L	L	X	X	Odd		NA	A	H	NA	A data to B bus and generate inverted parity
				Even				L		

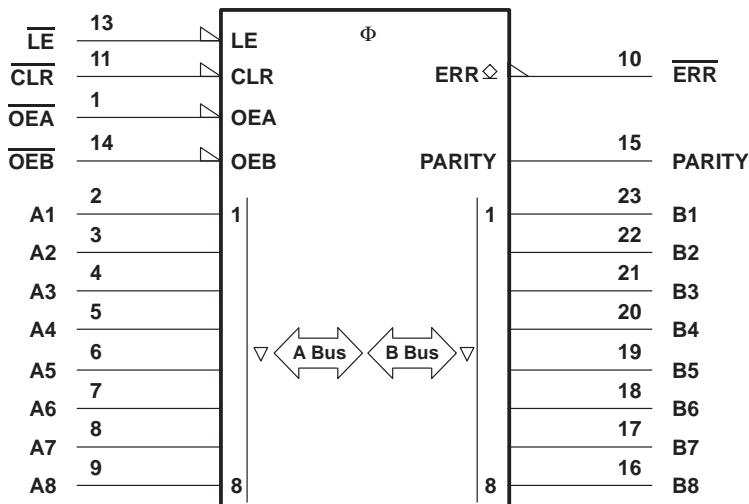
NA = not applicable, NC = no change, X = don't care

[†] Summation of high-level inputs includes PARITY along with Bi inputs.

[‡] Output states shown assume ERR was previously high.

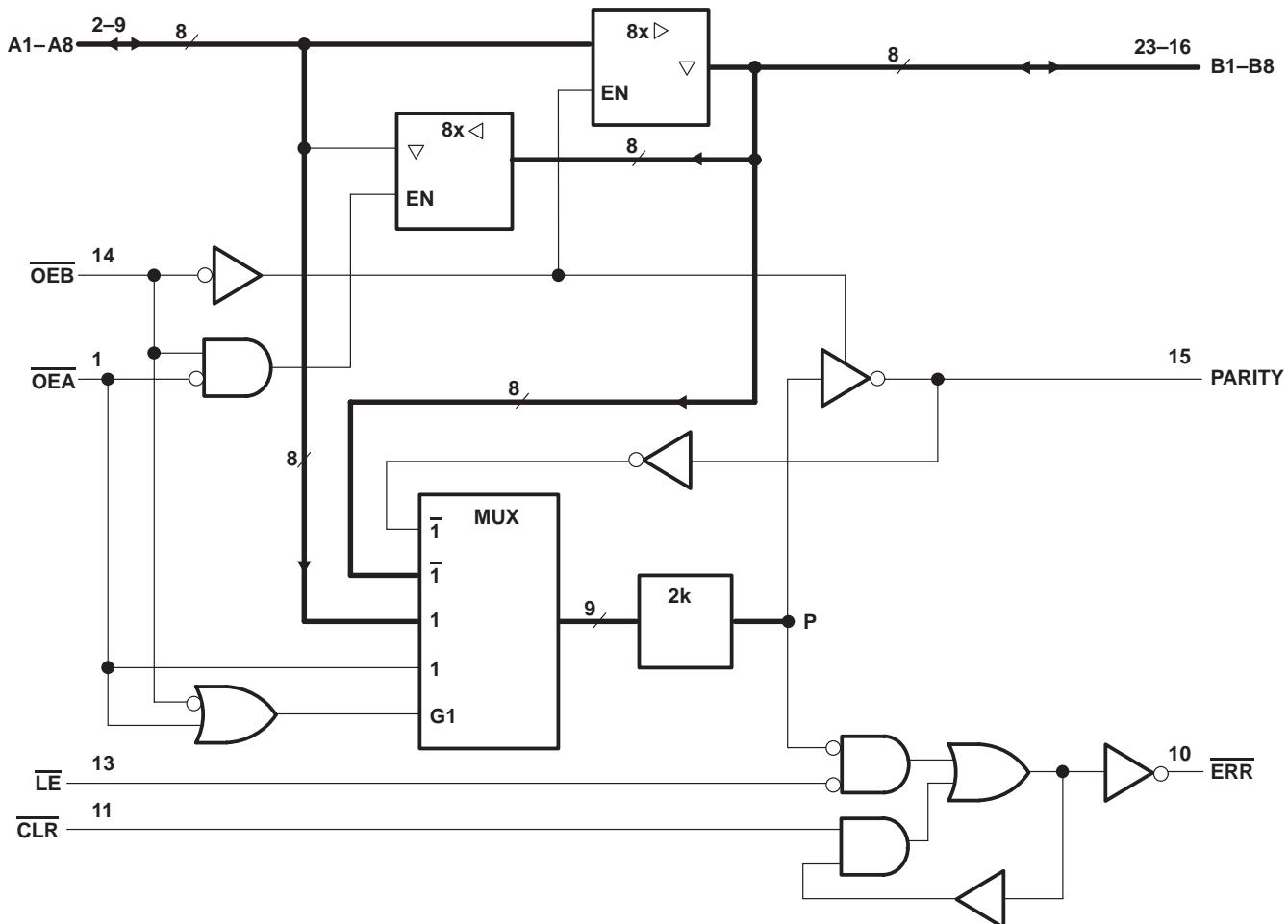
[§] In this mode, ERR (when clocked) shows inverted parity of the A bus.

logic symbol



[¶] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

ERROR-FLAG FUNCTION TABLE

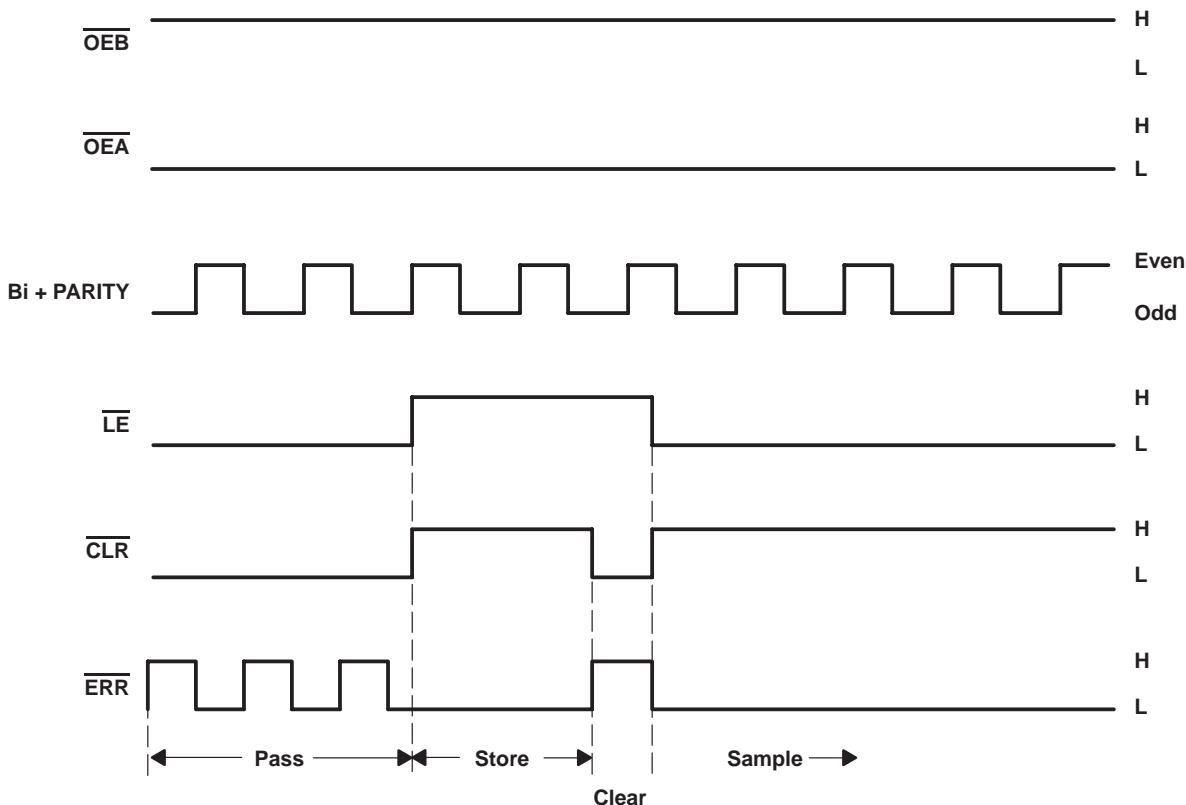
INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT ERR	FUNCTION
CLR	LE	POINT P	$\overline{ERR}_{N-1} \dagger$		
L	L	L H	X	L H	Pass
H	L	L X H	X L H	L L H	Sample
L	H	X	X	H	Clear
H	H	X	L H	L H	Store

[†] The state of \overline{ERR} before changes at CLR, LE, or point P

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error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



recommended operating conditions (see Note 3)

		SN54ABT853		SN74ABT853		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage			0.8	0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _{OH}	High-level output voltage	ERR		5.5	5.5	V
I _{OH}	High-level output current	Except ERR		-24	-32	mA
I _{OL}	Low-level output current			48	64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate			200	200	μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

SN54ABT853, SN74ABT853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA = 25°C			SN54ABT853	SN74ABT853	UNIT
		MIN	TPY†	MAX	MIN	MAX	
VIK	VCC = 4.5 V, I _I = -18 mA			-1.2	-1.2	-1.2	V
V _{OH}	VCC = 4.5 V, I _{OH} = -3 mA	2.5			2.5	2.5	V
	VCC = 5 V, I _{OH} = -3 mA	3			3	3	
	VCC = 4.5 V	I _{OH} = -24 mA	2		2		
		I _{OH} = -32 mA	2*			2	
V _{OL}	VCC = 4.5 V	I _{OL} = 24 mA	0.55		0.55		V
		I _{OL} = 64 mA	0.55*			0.55	
V _{hys}			100				mV
I _{OH}	ERR	VCC = 4.5 V, V _{OH} = 5.5 V		50	50	50	µA
I _I	Control inputs	VCC = 5.5 V, V _I = VCC or GND		±1	±1	±1	µA
	A or B ports			±100	±100	±100	
I _{OZPU} ‡	VCC = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, OE = X			±50	±50	±50	µA
I _{OZPD} ‡	VCC = 2.1 V to 0, V _O = 0.5 V to 2.7 V, OE = X			±50	±50	±50	µA
I _{OZH} §	VCC = 5.5 V, V _O = 2.7 V		10		10	10	µA
I _{OZL} §	VCC = 5.5 V, V _O = 0.5 V		-10		-10	-10	µA
I _{off}	VCC = 0, V _I or V _O ≤ 4.5 V		±100			±100	µA
I _{CEX}	VCC = 5.5 V, V _O = 5.5 V	Outputs high		50	50	50	µA
I _O ¶	VCC = 5.5 V, V _O = 2.5 V	-50 -100 -200#		-50 -200#	-50 -200#	-50 -200#	mA
I _{CC}	A or B ports	VCC = 5.5 V, I _O = 0, V _I = VCC or GND	Outputs high	1 250	450	250	µA
		Outputs low	24 38	38	38	mA	
		Outputs disabled	0.5 250	450	250	µA	
ΔI _{CC}	Data inputs	VCC = 5.5 V, One input at 3.4 V, Other inputs at VCC or GND	Outputs enabled		1.5	1.5	mA
			Outputs disabled		50	50	µA
	Control inputs	VCC = 5.5 V, One input at 3.4 V, Other inputs at VCC or GND		1.5	1.5	1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V		4.5			pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		10.5			pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at VCC = 5 V.

‡ This parameter is characterized, but not production tested.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This data sheet limit can vary among suppliers.

|| This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$	SN54ABT853		SN74ABT853		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	\overline{LE} high or low	3.5	3.5	3.5	3.5	ns
		CLR low	4	4	4	4	
t_{SU}	Setup time	B or PARITY before $\overline{LE} \downarrow$	9.4†	10.2	9.4†	9.4†	ns
		CLR before $\overline{LE} \downarrow$	2	2	2	2	
t_H	Hold time	B or PARITY after $\overline{LE} \downarrow$	0	0	0	0	ns
		CLR after $\overline{LE} \downarrow$	3	3	3	3	

† This data sheet limit can vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

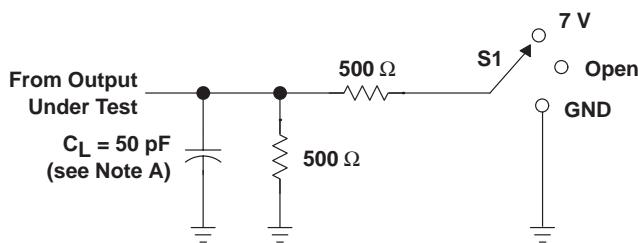
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$			SN54ABT853	SN74ABT853	UNIT	
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	A or B	B or A	1.2	4.8	1.2	6.4	1.2	5.3	ns
			1	4.8†	1	5.4	1	5.3†	
t_{PLH}	A	PARITY	2.1	9.5	2.1	13.3	2.1	11.2	ns
			2.5	9.7	2.5	11	2.5	11	
t_{PLH}	\overline{OE}	PARITY	1.8	8.5	1.8	13.6	1.8	10.5	ns
			2.3	8.6	2.3	11.7	2.3	10	
t_{PLH}	\overline{CLR}	\overline{ERR}	1	5.5	1	6.3	1	6.2	ns
t_{PLH}	\overline{LE}	ERR	1.8	5.1	1.8	6.1	1.8	6	ns
			1†	5.8	1†	6.7	1	6.6	
t_{PLH}	B or PARITY	ERR	2	10.1	2	11.8	2	11.7	ns
			2.2†	11.5	2.2†	12.9	2.2†	12.8	
t_{PZH}	\overline{OE}	A or B or PARITY	1	5.8†	1	8.8	1	6.7†	ns
			1.5†	5.8	1.5†	9.8	1.5†	6.7	
t_{PHZ}	\overline{OE}	A or B or PARITY	1.8†	7.3	1.8†	9.5	1.8†	7.9	ns
			2.1†	7.2	2.1†	8.2	2.1†	8.1	

† This data sheet limit can vary among suppliers.

SN54ABT853, SN74ABT853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

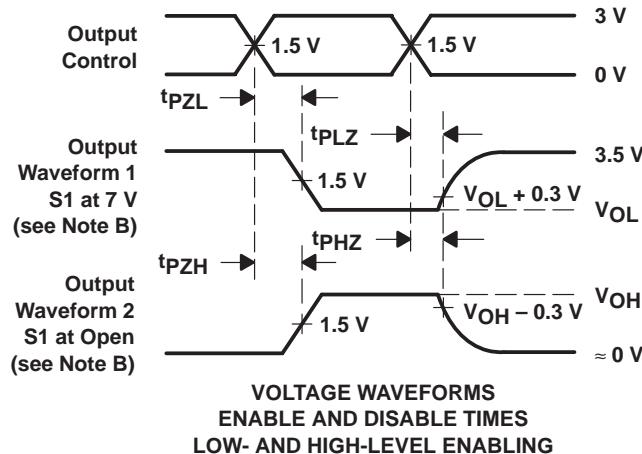
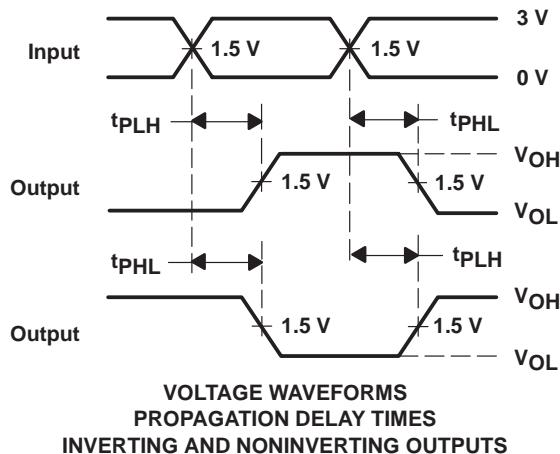
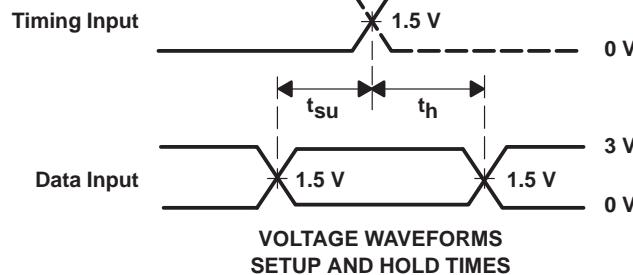
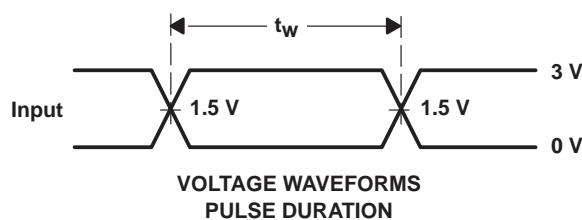
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	7 V
tPHZ/tPZH	Open

LOAD CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9674601Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9674601QKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-9674601QLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SN74ABT853DBLE	OBsolete	SSOP	DB	24		TBD	Call TI	Call TI
SN74ABT853DBRE4	ACTIVE	SSOP	DB	24		TBD	Call TI	Call TI
SN74ABT853DBRG4	ACTIVE	SSOP	DB	24		TBD	Call TI	Call TI
SN74ABT853DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT853DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT853DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT853DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT853DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT853DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT853NSRE4	ACTIVE	SO	NS	24		TBD	Call TI	Call TI
SN74ABT853NSRG4	ACTIVE	SO	NS	24		TBD	Call TI	Call TI
SN74ABT853NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT853NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT853PWE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74ABT853PWG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74ABT853PWLE	OBsolete	TSSOP	PW	24		TBD	Call TI	Call TI
SN74ABT853PWRE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74ABT853PWRG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI
SNJ54ABT853FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ABT853JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SNJ54ABT853W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS

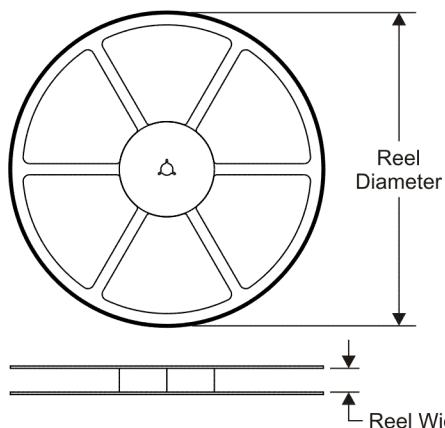
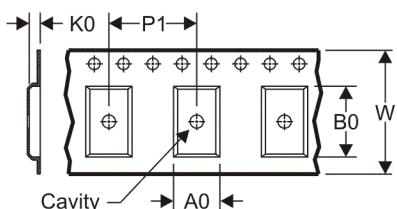
compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

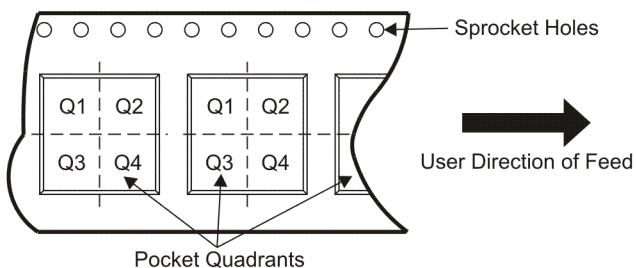
(³) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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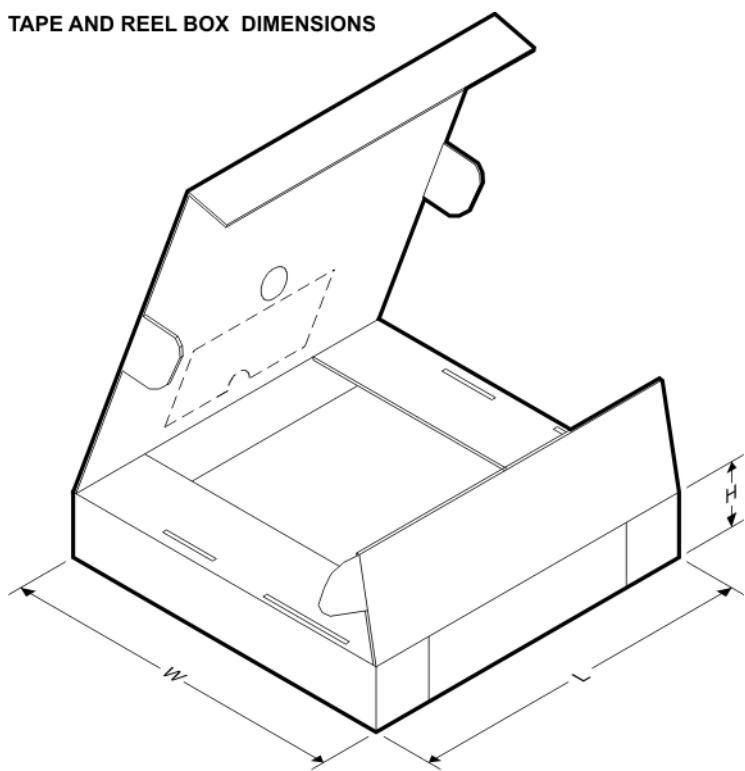
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT853DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

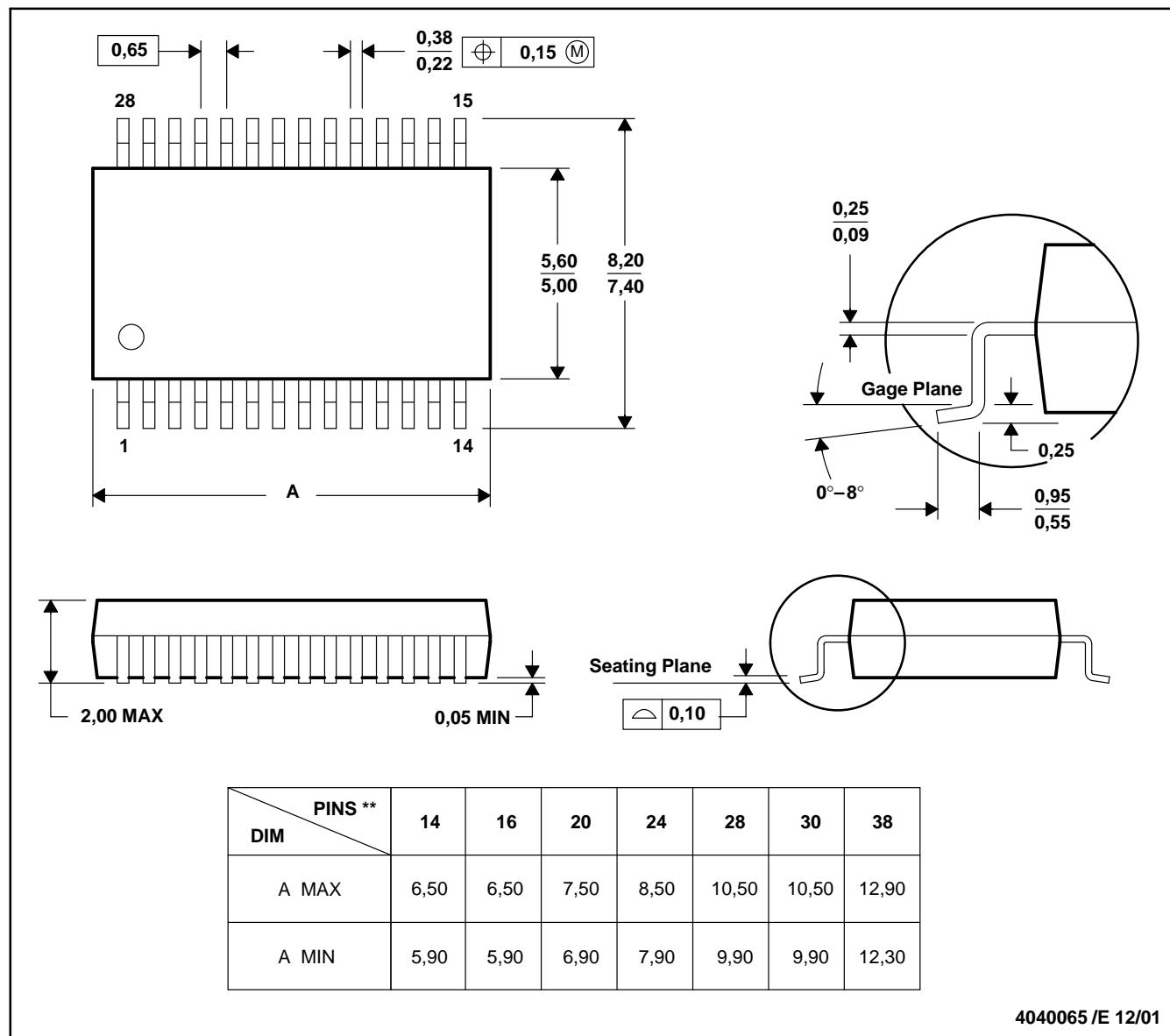
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT853DWR	SOIC	DW	24	2000	346.0	346.0	41.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

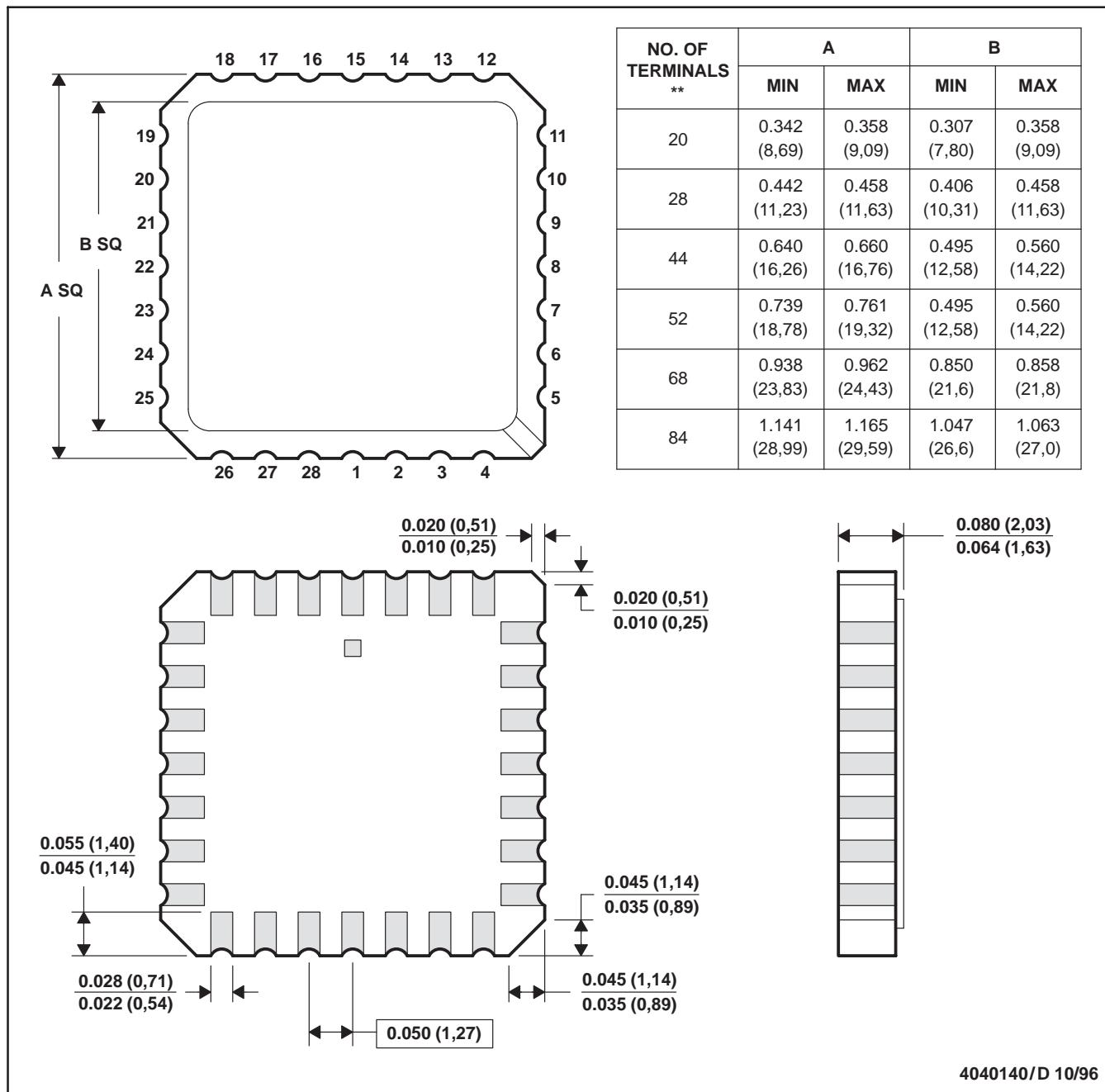


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



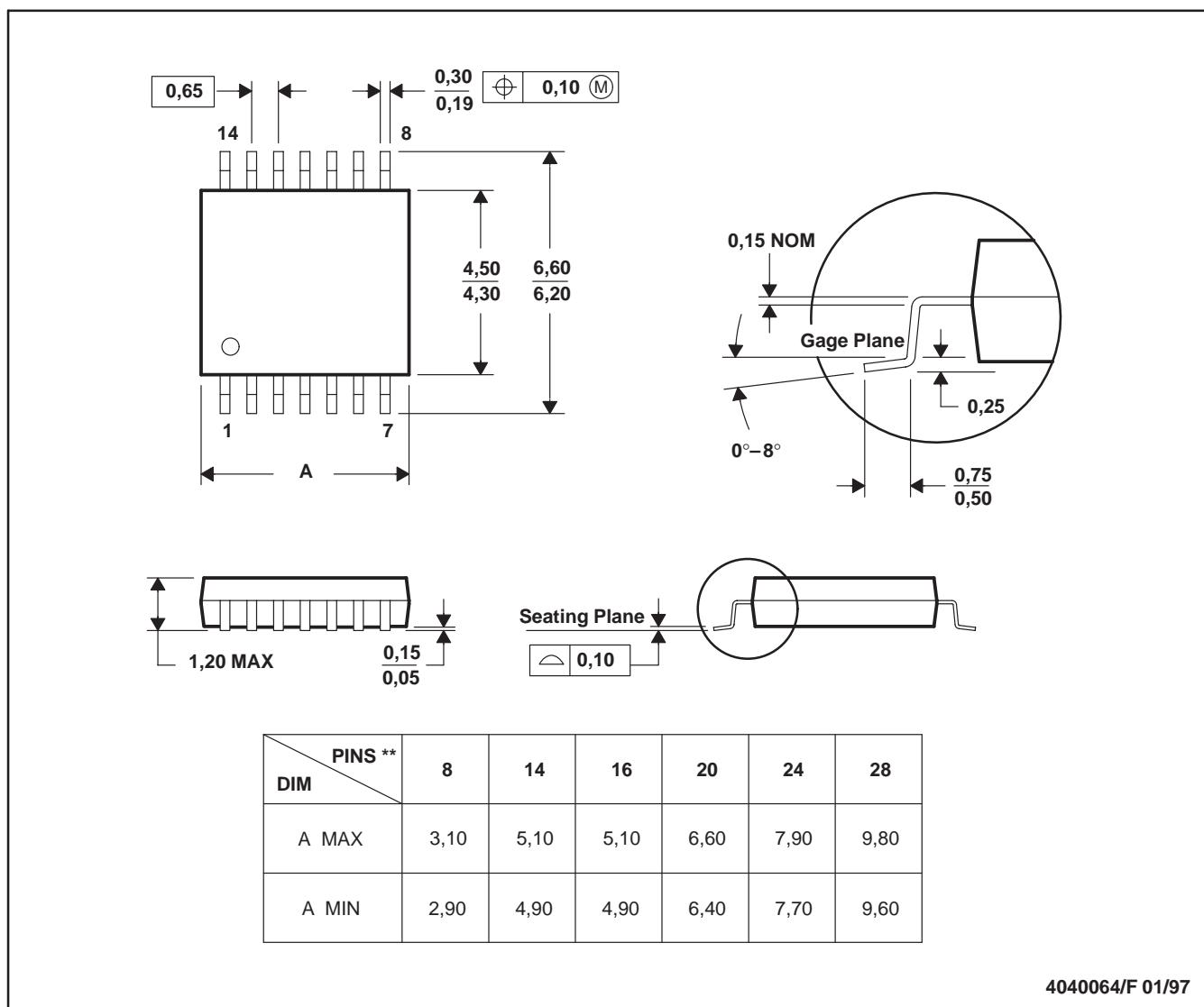
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES:

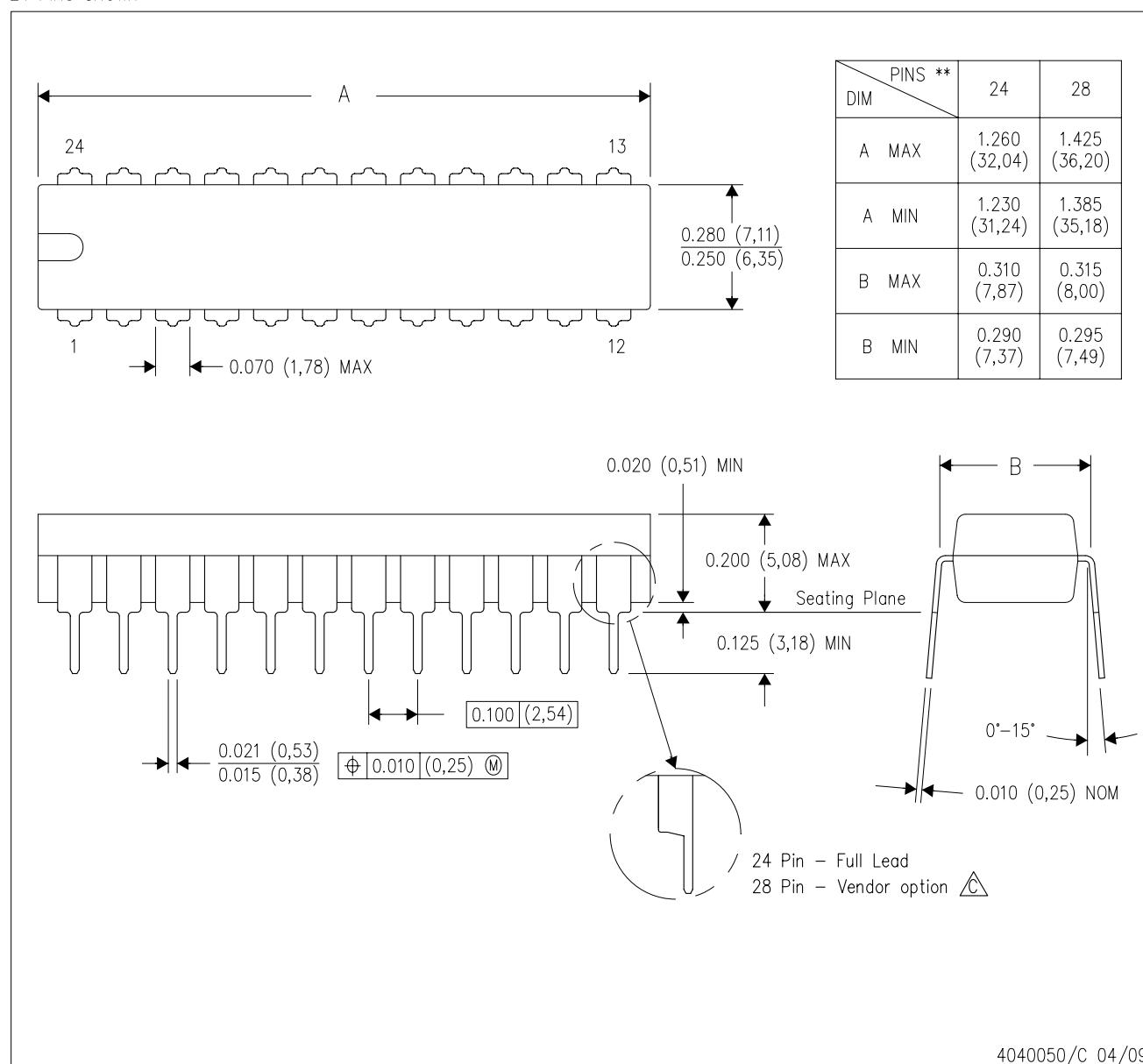
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



4040050/C 04/09

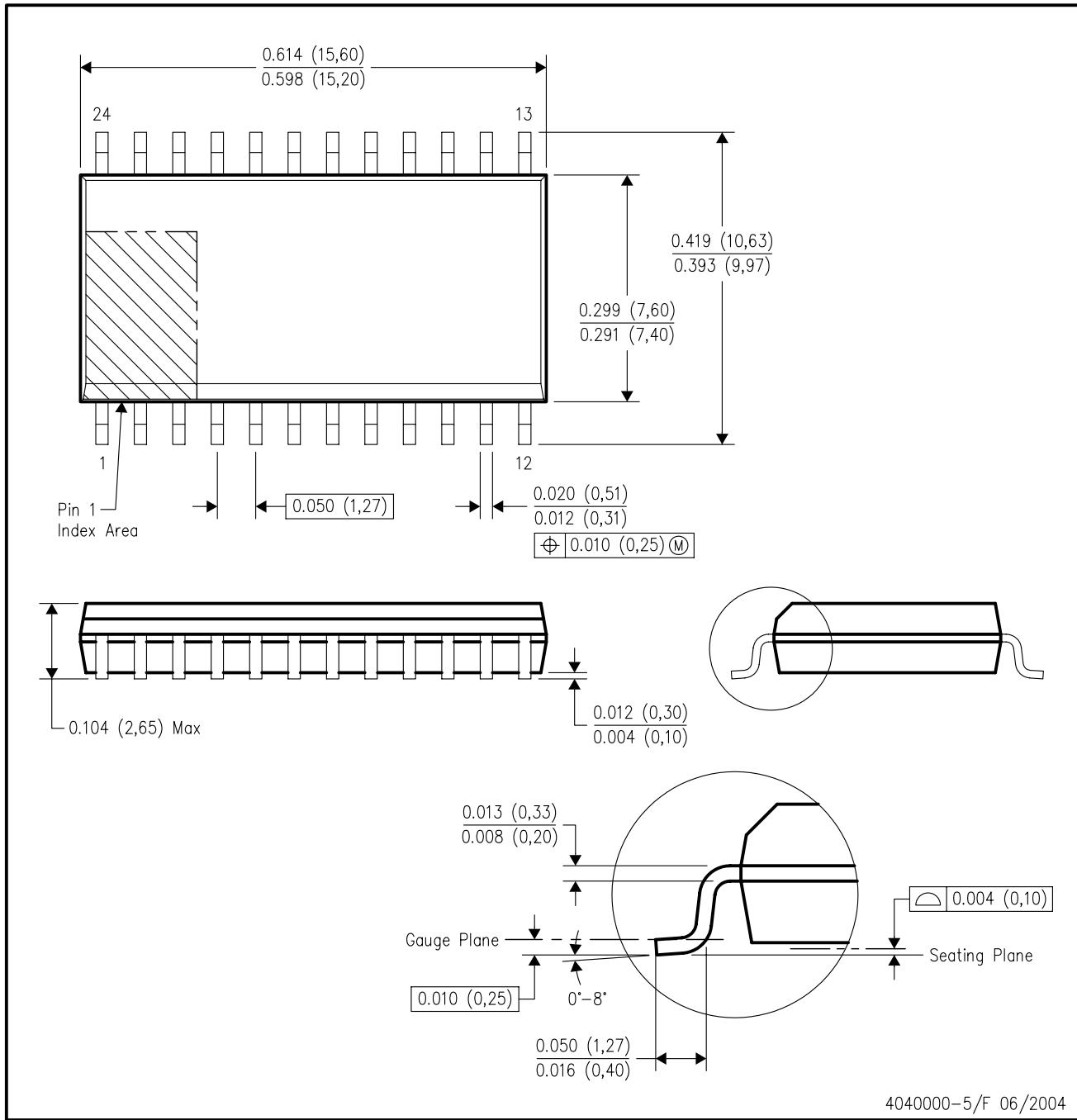
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

\triangle The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE

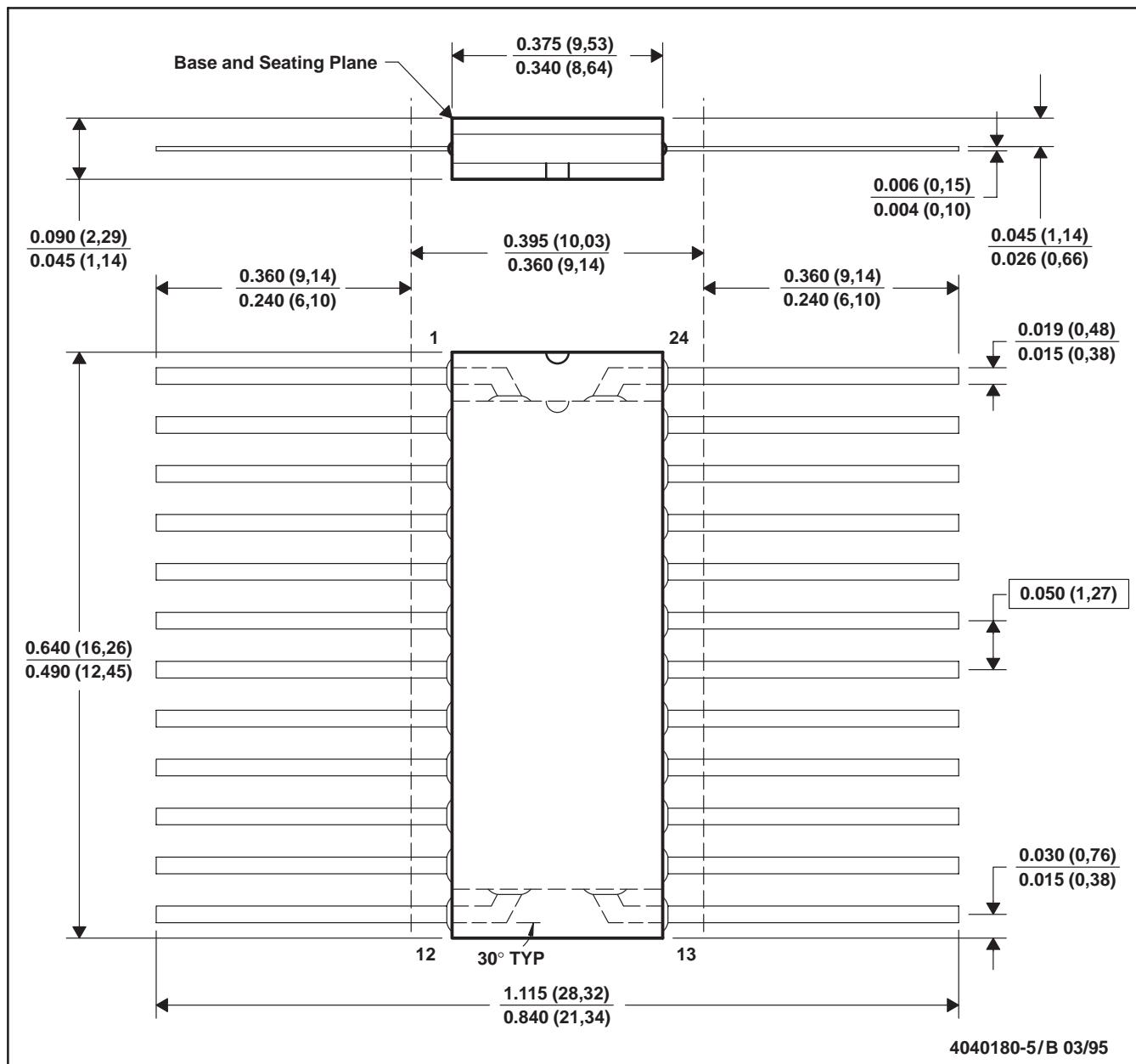


NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

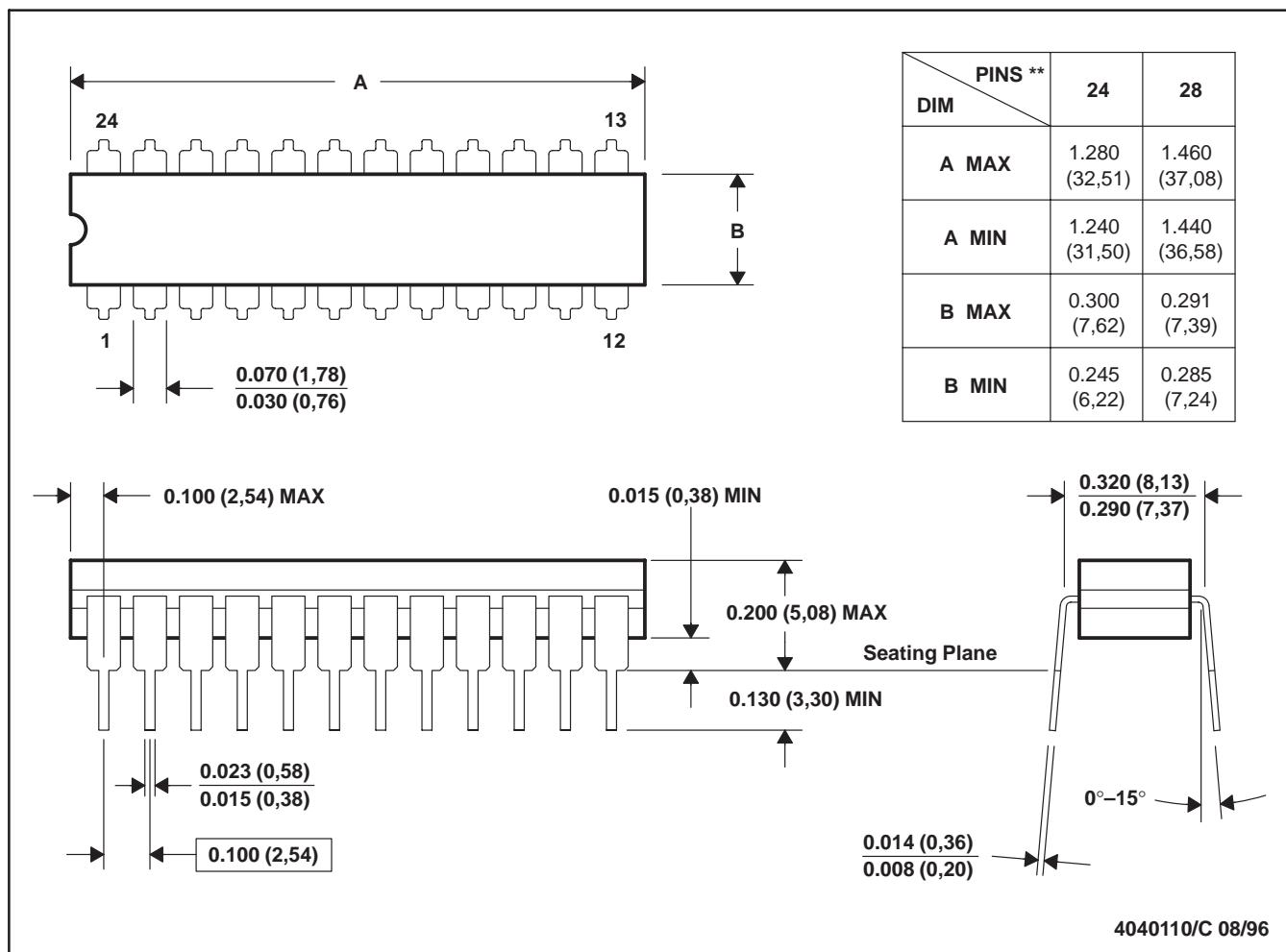


NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 E. Index point is provided on cap for terminal identification only.

JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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