



SANYO Semiconductors

## DATA SHEET

An ON Semiconductor Company

# LV8736V — Bi-CMOS LSI

## PWM Constant-Current Control Stepping Motor Driver

### Overview

The LV8736V is a 2-channel H-bridge driver IC that can switch a stepping motor driver, which is capable of micro-step drive and supports 2W 1-2 phase excitation, and two channels of a brushed motor driver, which supports forward, reverse, brake, and standby of a motor. It is ideally suited for driving brushed DC motors and stepping motors used in office equipment and amusement applications.

### Features

- Single-channel PWM current control stepping motor driver (selectable with DC motor driver channel 2) incorporated.
- BiCDMOS process IC
- Low on resistance (upper side :  $0.75\Omega$  ; lower side :  $0.5\Omega$  ; total of upper and lower :  $1.25\Omega$  ;  $T_a = 25^\circ\text{C}$ ,  $I_O = 1\text{A}$ )
- Excitation mode can be set to 2-phase, 1-2 phase, W1-2 phase , or 2W1-2 phase
- Excitation step proceeds only by step signal input
- Motor current selectable in four steps
- Output short-circuit protection circuit (selectable from latch-type or auto-reset-type) incorporated
- Unusual condition warning output pins
- Built-in thermal shutdown circuit
- No control power supply required

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter              | Symbol           | Conditions                        | Ratings    | Unit |
|------------------------|------------------|-----------------------------------|------------|------|
| Supply voltage         | $V_M$ max        |                                   | 36         | V    |
| Output peak current    | $I_O$ peak       | $t_w \leq 10\text{ms}$ , duty 20% | 1.5        | A    |
| Output current         | $I_O$ max        |                                   | 1          | A    |
| Logic input voltage    | $V_{IN}$ max     |                                   | -0.3 to +6 | V    |
| MONI/EMO input voltage | $V_{mo}/V_{emo}$ |                                   | -0.3 to +6 | V    |

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| Parameter                   | Symbol | Conditions | Ratings     | Unit |
|-----------------------------|--------|------------|-------------|------|
| Allowable power dissipation | Pd max | *          | 3.05        | W    |
| Operating temperature       | Topr   |            | -20 to +85  | °C   |
| Storage temperature         | Tstg   |            | -55 to +150 | °C   |

\* Specified circuit board : 90.0mm×90.0mm×1.6mm, glass epoxy 2-layer board, with backside mounting.

## Allowable Operating Ratings at Ta = 25°C

| Parameter                | Symbol          | Conditions | Ratings  | Unit |
|--------------------------|-----------------|------------|----------|------|
| Supply voltage range     | VM              |            | 9 to 32  | V    |
| Logic input voltage      | V <sub>IN</sub> |            | 0 to 5.5 | V    |
| VREF input voltage range | VREF            |            | 0 to 3   | V    |

## Electrical Characteristics at Ta = 25°C, VM = 24V, VREF = 1.5V

| Parameter                                                                |                   | Symbol              | Conditions                                              | Ratings |       |       | Unit |
|--------------------------------------------------------------------------|-------------------|---------------------|---------------------------------------------------------|---------|-------|-------|------|
|                                                                          |                   |                     |                                                         | min     | typ   | max   |      |
| Standby mode current drain                                               |                   | IMst                | ST = "L"                                                |         | 100   | 400   | μA   |
| Current drain                                                            |                   | IM                  | ST = "H", OE = "L", with no load                        |         | 3.2   | 5     | mA   |
| VREG5 output voltage                                                     |                   | Vreg5               | I <sub>O</sub> = -1mA                                   | 4.5     | 5     | 5.5   | V    |
| Thermal shutdown temperature                                             |                   | TSD                 | Design guarantee                                        | 150     | 180   | 200   | °C   |
| Thermal hysteresis width                                                 |                   | ΔTSD                | Design guarantee                                        |         | 40    |       | °C   |
| Motor driver                                                             |                   |                     |                                                         |         |       |       |      |
| Output on resistance                                                     |                   | Ronu                | I <sub>O</sub> = 1A, Upper-side on resistance           |         | 0.75  | 0.97  | Ω    |
|                                                                          |                   | Rond                | I <sub>O</sub> = 1A, Lower-side on resistance           |         | 0.5   | 0.65  | Ω    |
| Output leakage current                                                   |                   | I <sub>O</sub> leak |                                                         |         |       | 50    | μA   |
| Diode forward voltage                                                    |                   | VD                  | ID = -1A                                                |         | 1.2   | 1.4   | V    |
| Logic high-level input voltage                                           |                   | V <sub>INH</sub>    |                                                         | 2.0     |       |       | V    |
| Logic low-level input voltage                                            |                   | V <sub>INL</sub>    |                                                         |         |       | 0.8   | V    |
| Logic pin input current<br>other OE/CMK pin                              |                   | I <sub>INL</sub>    | V <sub>IN</sub> = 0.8V                                  | 4       | 8     | 12    | μA   |
|                                                                          |                   | I <sub>INH</sub>    | V <sub>IN</sub> = 5V                                    | 30      | 50    | 70    | μA   |
| OE / CMK pin input current                                               |                   | I <sub>CMKL</sub>   | DM = "L", OE/CMK = 0.8V                                 | 4       | 8     | 12    | μA   |
|                                                                          |                   | I <sub>CMKH</sub>   | DM = "L", OE/CMK = 5V                                   | 30      | 50    | 70    | μA   |
|                                                                          |                   | I <sub>CMK</sub>    | DM = "H", OE/CMK = 0V                                   | -32     | -25   | -18   | μA   |
| OE/CMK pin current LIMIT mask threshold voltage.                         |                   | V <sub>t</sub> CMK  | DM = "H"                                                | 1.2     | 1.5   | 1.8   | V    |
| Current setting comparator threshold voltage<br>(current step switching) | 2W1-2 phase drive | Vtdac0_2W           | Step 0 (When initialized : channel 1 comparator level)  | 0.291   | 0.3   | 0.309 | V    |
|                                                                          |                   | Vtdac1_2W           | Step 1 (Initial state+1)                                | 0.285   | 0.294 | 0.303 | V    |
|                                                                          |                   | Vtdac2_2W           | Step 2 (Initial state+2)                                | 0.267   | 0.276 | 0.285 | V    |
|                                                                          |                   | Vtdac3_2W           | Step 3 (Initial state+3)                                | 0.240   | 0.249 | 0.258 | V    |
|                                                                          |                   | Vtdac4_2W           | Step 4 (Initial state+4)                                | 0.201   | 0.21  | 0.219 | V    |
|                                                                          |                   | Vtdac5_2W           | Step 5 (Initial state+5)                                | 0.157   | 0.165 | 0.173 | V    |
|                                                                          |                   | Vtdac6_2W           | Step 6 (Initial state+6)                                | 0.107   | 0.114 | 0.121 | V    |
|                                                                          |                   | Vtdac7_2W           | Step 7 (Initial state+7)                                | 0.053   | 0.06  | 0.067 | V    |
|                                                                          | W1-2 phase drive  | Vtdac0_W            | Step 0 (When initialized : channel 1 comparator level)  | 0.291   | 0.3   | 0.309 | V    |
|                                                                          |                   | Vtdac2_W            | Step 2 (Initial state+1)                                | 0.267   | 0.276 | 0.285 | V    |
|                                                                          |                   | Vtdac4_W            | Step 4 (Initial state+2)                                | 0.201   | 0.21  | 0.219 | V    |
|                                                                          |                   | Vtdac6_W            | Step 6 (Initial state+3)                                | 0.107   | 0.114 | 0.121 | V    |
|                                                                          | 1-2 phase drive   | Vtdac0_H            | Step 0 (When initialized : channel 1 comparator level)  | 0.291   | 0.3   | 0.309 | V    |
|                                                                          |                   | Vtdac4_H            | Step 4 (Initial state+1)                                | 0.201   | 0.21  | 0.219 | V    |
|                                                                          | 2 phase drive     | Vtdac4_F            | Step 4' (When initialized : channel 1 comparator level) | 0.291   | 0.3   | 0.309 | V    |

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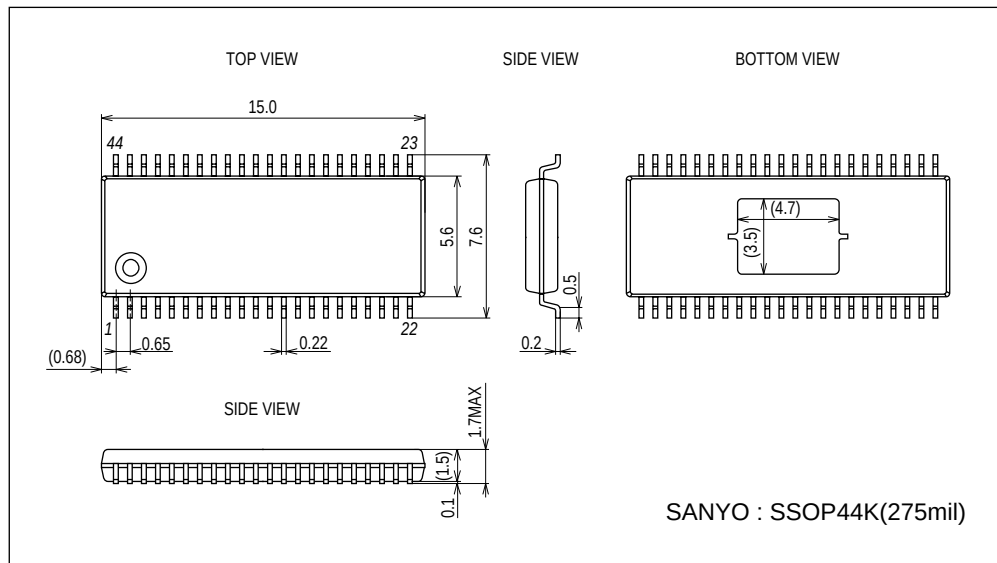
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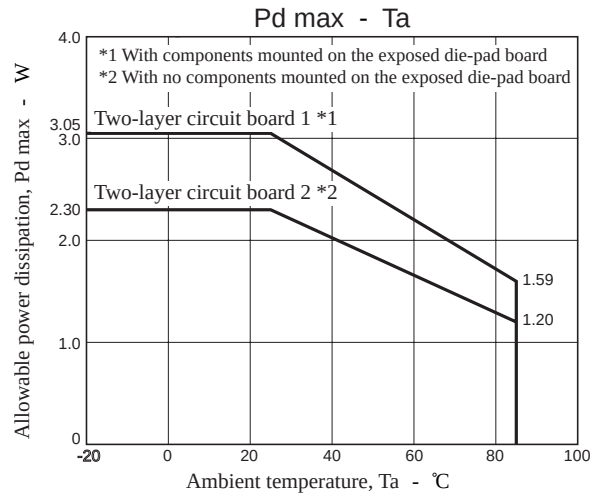
| Parameter                                                                            | Symbol  | Conditions         | Ratings |      |       | Unit |
|--------------------------------------------------------------------------------------|---------|--------------------|---------|------|-------|------|
|                                                                                      |         |                    | min     | typ  | max   |      |
| Current setting comparator threshold voltage<br>(current attenuation rate switching) | Vtatt00 | ATT1 = L, ATT2 = L | 0.291   | 0.3  | 0.309 | V    |
|                                                                                      | Vtatt01 | ATT1 = H, ATT2 = L | 0.232   | 0.24 | 0.248 | V    |
|                                                                                      | Vtatt10 | ATT1 = L, ATT2 = H | 0.143   | 0.15 | 0.157 | V    |
|                                                                                      | Vtatt11 | ATT1 = H, ATT2 = H | 0.053   | 0.06 | 0.067 | V    |
| Chopping frequency                                                                   | Fchop   | Cchop = 200pF      | 40      | 50   | 60    | kHz  |
| CHOP pin charge/discharge current                                                    | Ichop   |                    | 7       | 10   | 13    | μA   |
| Chopping oscillation circuit threshold voltage                                       | Vtup    |                    | 0.8     | 1    | 1.2   | V    |
| VREF pin input current                                                               | Iref    | VREF = 1.5V        | -0.5    |      |       | μA   |
| MONI pin saturation voltage                                                          | Vsatmon | Imoni = 1mA        |         |      | 400   | mV   |
| <b>Charge pump</b>                                                                   |         |                    |         |      |       |      |
| VG output voltage                                                                    | VG      |                    | 28      | 28.7 | 29.8  | V    |
| Rise time                                                                            | tONG    | VG = 0.1μF         |         | 200  | 500   | μS   |
| Oscillator frequency                                                                 | Fosc    |                    | 90      | 125  | 150   | kHz  |
| <b>Output short-circuit protection</b>                                               |         |                    |         |      |       |      |
| EMO pin saturation voltage                                                           | Vsatemo | Iemo = 1mA         |         |      | 400   | mV   |
| CEM pin charge current                                                               | Icem    | Vcem = 0V          | 7       | 10   | 13    | μA   |
| CEM pin threshold voltage                                                            | Vtcem   |                    | 0.8     | 1    | 1.2   | V    |

## Package Dimensions

unit : mm (typ)

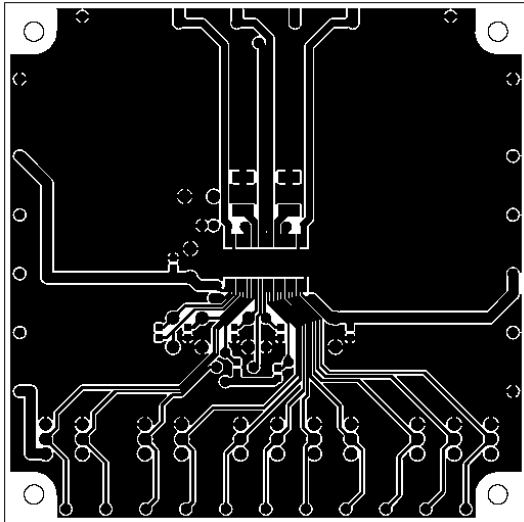
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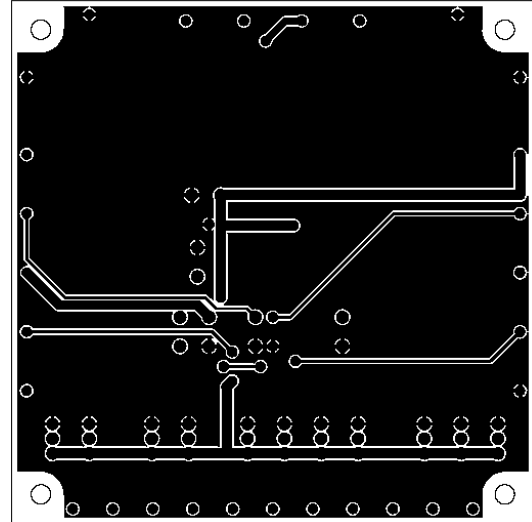


### Substrate Specifications (Substrate recommended for operation of LV8736V)

Size : 90mm × 90mm × 1.6mm (two-layer substrate [2S0P])  
 Material : Glass epoxy  
 Copper wiring density : L1 = 85% / L2 = 90%



L1 : Copper wiring pattern diagram



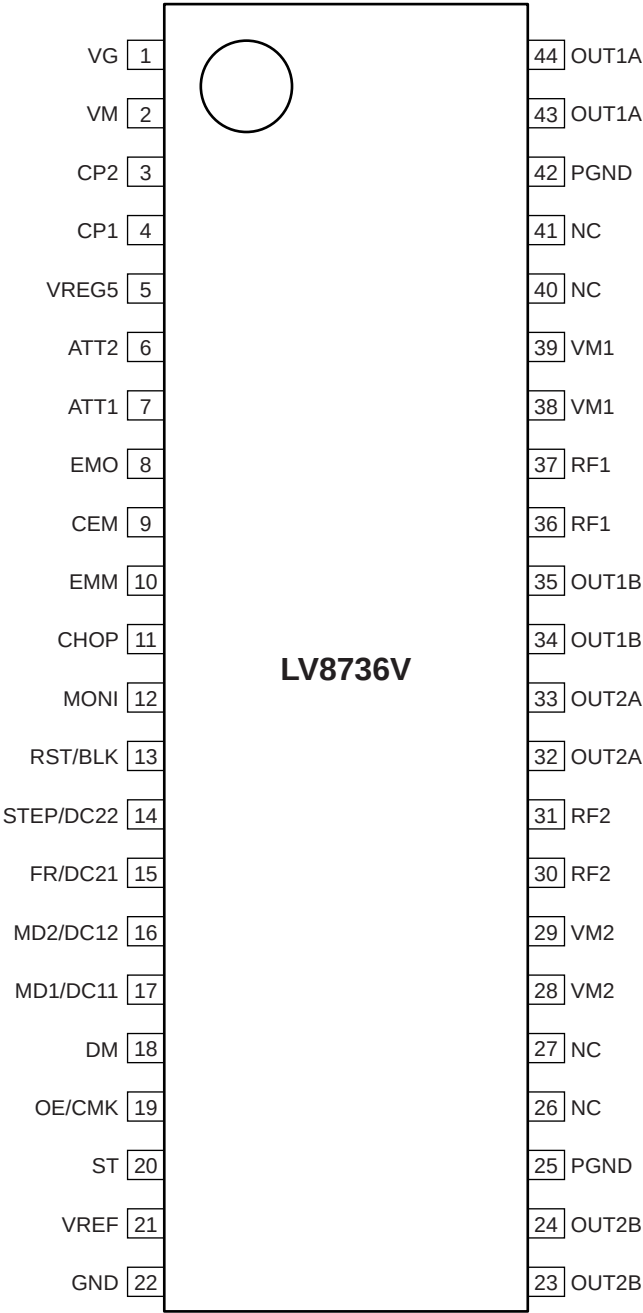
L2 : Copper wiring pattern diagram

### Cautions

- 1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.
- 2) For the set design, employ the derating design with sufficient margin.  
 Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.  
 Accordingly, the design must ensure these stresses to be as low or small as possible.  
 The guideline for ordinary derating is shown below :  
 (1)Maximum value 80% or less for the voltage rating  
 (2)Maximum value 80% or less for the current rating  
 (3)Maximum value 80% or less for the temperature rating
- 3) After the set design, be sure to verify the design with the actual product.  
 Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.  
 Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

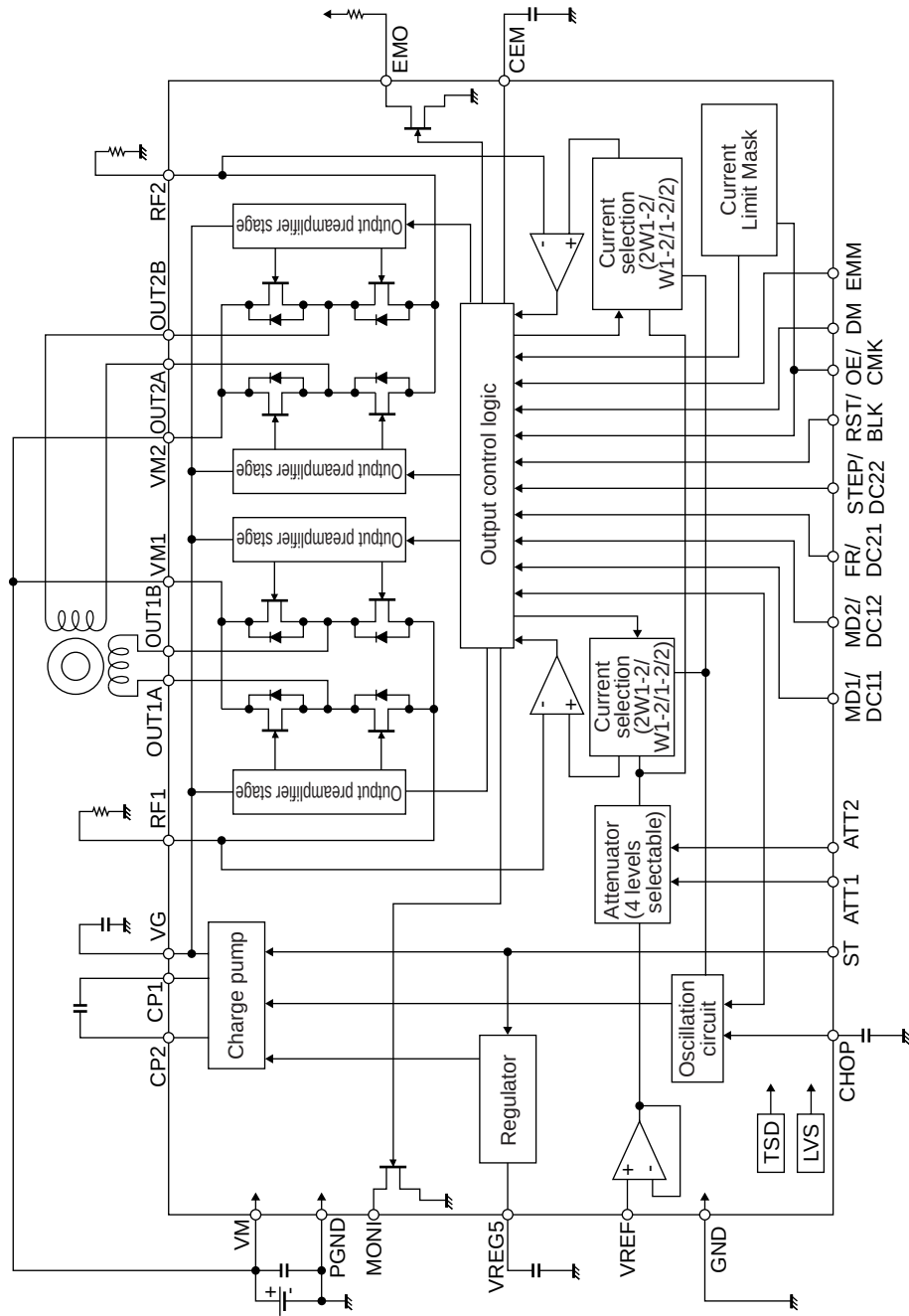
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Pin Assignment



Top view

# Block Diagram



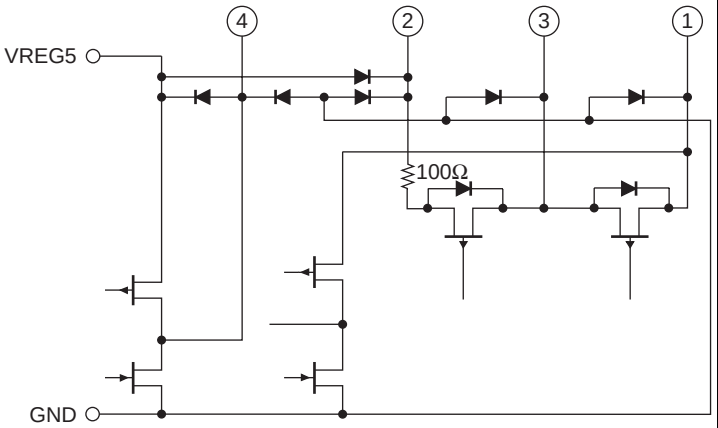
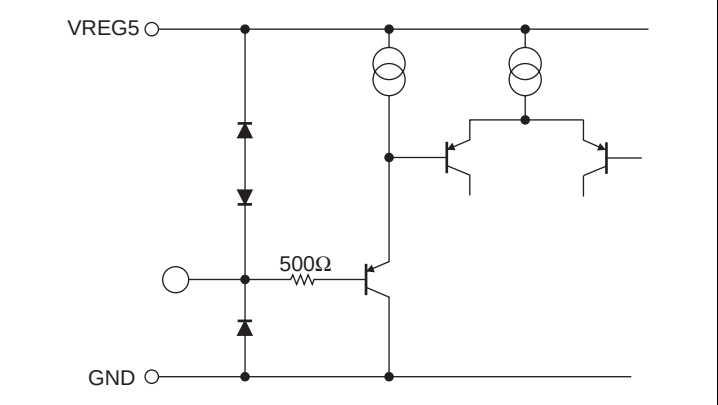
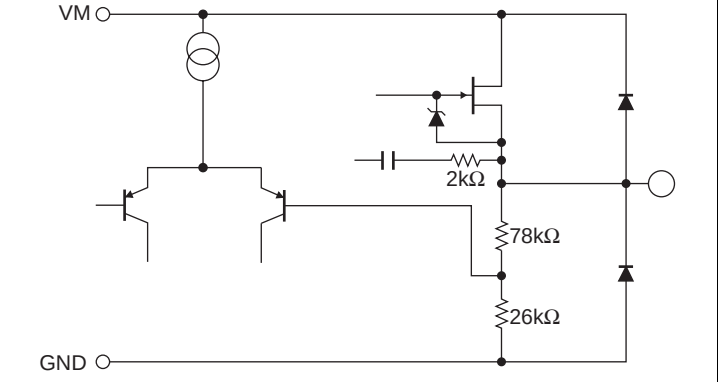
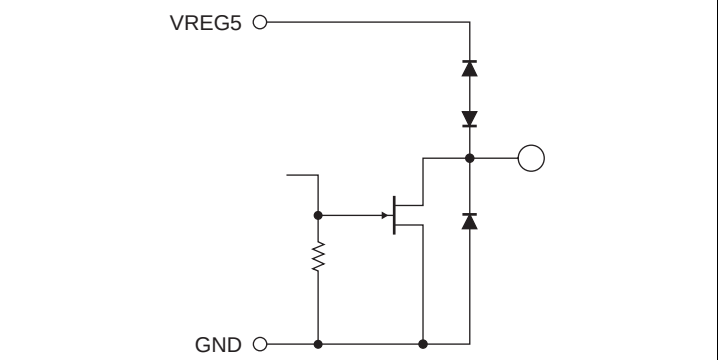
Pin Functions

| Pin No.                                                                                | Pin Name                                                                             | Pin Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Equivalent Circuit |
|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| 6<br>7<br>10<br>13<br>14<br>15<br>16<br>17<br>18                                       | ATT2<br>ATT1<br>EMM<br>RST/BLK<br>STEP/DC22<br>FR/DC21<br>MD2/DC12<br>MD1/DC11<br>DM | Motor holding current switching pin.<br>Motor holding current switching pin.<br>Output short-circuit protection mode switching pin.<br>RESET input pin (STM) / Blanking time switching pin (DCM).<br>STEP signal input pin (STM) / Channel 2 output control input pin 2 (DCM).<br>CW / CCW signal input pin (STM) / Channel 2 output control input pin 1 (DCM).<br>Excitation mode switching pin 2 (STM) / Channel 1 output control input pin 2 (DCM).<br>Excitation mode switching pin 1 (STM) / Channel 1 output control input pin 1 (DCM).<br>Drive mode (STM/DCM) switching pin. |                    |
| 20                                                                                     | ST                                                                                   | Chip enable pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                    |
| 23, 24<br>25, 42<br>28, 29<br>30, 31<br>32, 33<br>34, 35<br>36, 37<br>38, 39<br>43, 44 | OUT2B<br>PGND<br>VM2<br>RF2<br>OUT2A<br>OUT1B<br>RF1<br>VM1<br>OUT1A                 | Channel 2 OUTB output pin.<br>Power system ground.<br>Channel 2 motor power supply connection pin.<br>Channel 2 current-sense resistor connection pin.<br>Channel 2 OUTA output pin.<br>Channel 1 OUTB output pin.<br>Channel 1 current-sense resistor connection pin.<br>Channel 1 motor power supply pin.<br>Channel 1 OUTA output pin.                                                                                                                                                                                                                                            |                    |

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| Pin No.          | Pin Name               | Pin Function                                                                                                                                                  | Equivalent Circuit                                                                   |
|------------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| 1<br>2<br>3<br>4 | VG<br>VM<br>CP2<br>CP1 | Charge pump capacitor connection pin.<br>Motor power supply connection pin.<br>Charge pump capacitor connection pin.<br>Charge pump capacitor connection pin. |    |
| 21               | VREF                   | Constant current control reference voltage input pin.                                                                                                         |   |
| 5                | VREG5                  | Internal power supply capacitor connection pin.                                                                                                               |  |
| 8<br>12          | EMO<br>MONI            | Output short-circuit state warning output pin.<br>Position detection monitor pin.                                                                             |  |

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| Pin No.          | Pin Name | Pin Function                                                                    | Equivalent Circuit |
|------------------|----------|---------------------------------------------------------------------------------|--------------------|
| 9                | CEM      | Pin to connect the output short-circuit state detection time setting capacitor. |                    |
| 11               | CHOP     | Chopping frequency setting capacitor connection pin.                            |                    |
| 19               | OE       | Output enable signal input pin.                                                 |                    |
| 22               | GND      | Ground.                                                                         |                    |
| 26, 27<br>40, 41 | NC       | No Connection<br>(No internal connection to the IC)                             |                    |

## Description of operation

### Input Pin Function

The function to prevent including the turn from the input to the power supply is built into each input pin. Therefore, the current turns to the power supply even if power supply (VM) is turned off with the voltage impressed to the input pin and there is not crowding.

#### (1) Chip enable function

This IC is switched between standby and operating mode by setting the ST pin. In standby mode, the IC is set to power-save mode and all logic is reset. In addition, the internal regulator circuit and charge pump circuit do not operate in standby mode.

| ST          | Mode           | Internal regulator | Charge pump |
|-------------|----------------|--------------------|-------------|
| Low or Open | Standby mode   | Standby            | Standby     |
| High        | Operating mode | Operating          | Operating   |

#### (2) Drive mode switching pin function

The IC drive mode is switched by setting the DM pin. In STM mode, stepping motor channel 1 can be controlled by the CLK-IN input. In DCM mode, DC motor channel 2 or stepping motor channel 1 can be controlled by parallel input. Stepping motor control using parallel input is 2-phase or 1-2 phase full torque.

| DM          | Drive mode | Application                                               |
|-------------|------------|-----------------------------------------------------------|
| Low or Open | STM mode   | Stepping motor channel 1 (CLK-IN)                         |
| High        | DCM mode   | DC motor channel 2 or stepping motor channel 1 (parallel) |

STM mode (DM = Low or Open)

#### (1) STEP pin function

| Input |                                                                                     | Operating mode           |
|-------|-------------------------------------------------------------------------------------|--------------------------|
| ST    | STP                                                                                 |                          |
| Low   | *                                                                                   | Standby mode             |
| High  |  | Excitation step proceeds |
| High  |  | Excitation step is kept  |

#### (2) Excitation mode setting function

| MD1  | MD2  | Excitation mode        | Initial position |           |
|------|------|------------------------|------------------|-----------|
|      |      |                        | Channel 1        | Channel 2 |
| Low  | Low  | 2 phase excitation     | 100%             | -100%     |
| High | Low  | 1-2 phase excitation   | 100%             | 0%        |
| Low  | High | W1-2 phase excitation  | 100%             | 0%        |
| High | High | 2W1-2 phase excitation | 100%             | 0%        |

This is the initial position of each excitation mode in the initial state after power-on and when the counter is reset.

#### (3) Position detection monitoring function

The MONI position detection monitoring pin is of an open drian type.

When the excitation position is in the initial position, the MONI output is placed in the ON state.

(Refer to "Examples of current waveforms in each of the excitation modes.")

#### (4) Setting constant-current control reference current

This IC is designed to automatically exercise PWM constant-current chopping control for the motor current by setting the output current. Based on the voltage input to the VREF pin and the resistance connected between RF and GND, the output current that is subject to the constant-current control is set using the calculation formula below :

$$I_{OUT} = (VREF/5)/RF \text{ resistance}$$

\* The above setting is the output current at 100% of each excitation mode.

The voltage input to the VREF pin can be switched to four-step settings depending on the statuses of the two inputs, ATT1 and ATT2. This is effective for reducing power consumption when motor holding current is supplied.

Attenuation function for VREF input voltage

| ATT1 | ATT2 | Current setting reference voltage attenuation ratio |
|------|------|-----------------------------------------------------|
| Low  | Low  | 100%                                                |
| High | Low  | 80%                                                 |
| Low  | High | 50%                                                 |
| High | High | 20%                                                 |

The formula used to calculate the output current when using the function for attenuating the VREF input voltage is given below.

$$I_{OUT} = (VREF/5) \times (\text{attenuation ratio})/RF \text{ resistance}$$

Example : At VREF of 1.5V, a reference voltage setting of 100% [(ATT1, ATT2) = (L, L)] and an RF resistance of 0.5Ω, the output current is set as shown below.

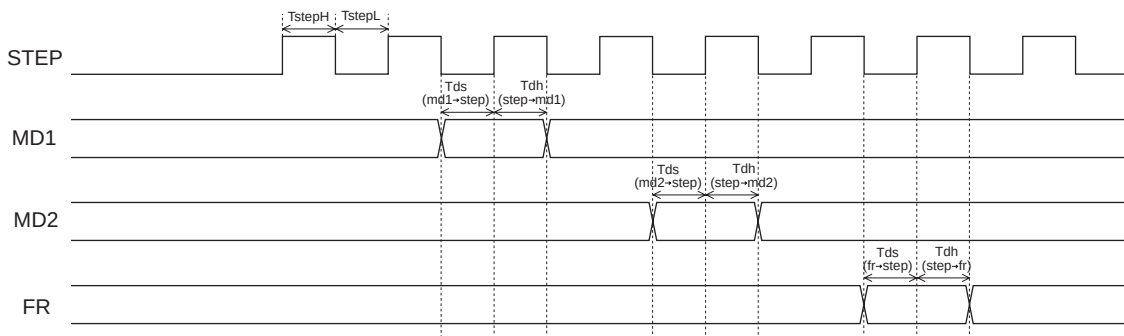
$$I_{OUT} = 1.5V/5 \times 100\%/0.5\Omega = 0.6A$$

If, in this state, (ATT1, ATT2) is set to (H, H), IOUT will be as follows :

$$I_{OUT} = 0.6A \times 20\% = 120mA$$

In this way, the output current is attenuated when the motor holding current is supplied so that power can be conserved.

#### (5) Input timing



TstepH/TstepL : Clock H/L pulse width (min 500ns)

Tds : Data set-up time (min 500ns)

Tdh : Data hold time (min 500ns)

#### (6) Blanking period

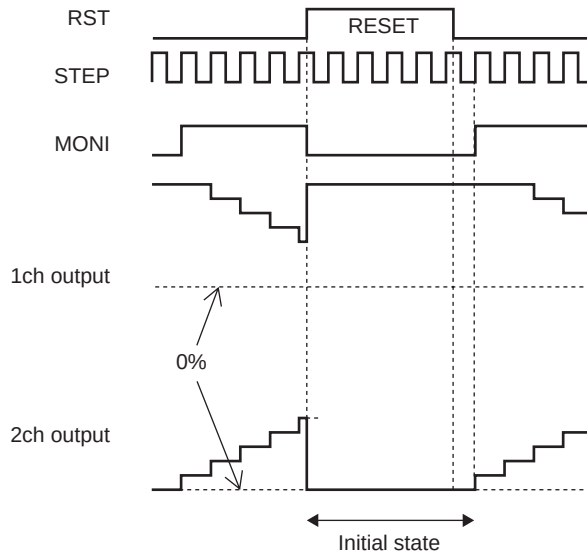
If, when exercising PWM constant-current chopping control over the motor current, the mode is switched from decay to charge, the recovery current of the parasitic diode may flow to the current sensing resistance, causing noise to be carried on the current sensing resistance pin, and this may result in erroneous detection. To prevent this erroneous detection, a blanking period is provided to prevent the noise occurring during mode switching from being received. During this period, the mode is not switched from charge to decay even if noise is carried on the current sensing resistance pin.

In the stepping motor driver mode (DM = Low or Open) of this IC, the blanking time is fixed at approximately 1μs. In the DC motor driver mode (DM = High), the blanking time can be switched to one of two levels using the RST/BLK pin. (Refer to "Blanking time switching function.")

### (7) Reset function

Only STM mode is pin at the DCM mode BLK: It operates as a switch function of the time of the branching.

| RST  | Operating mode   |
|------|------------------|
| Low  | Normal operation |
| High | Reset state      |

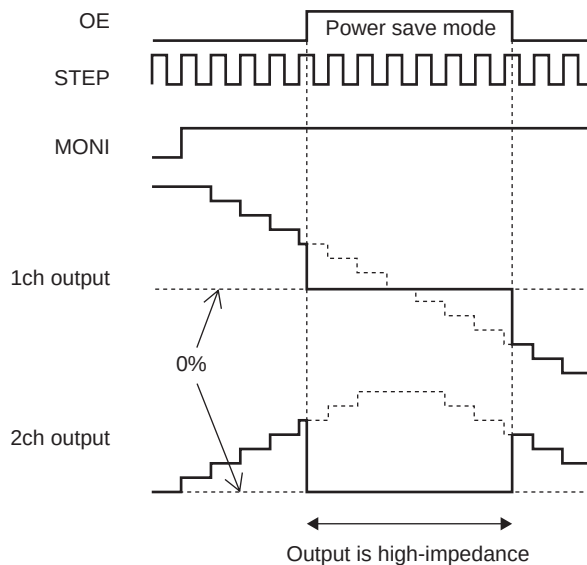


When the RST pin is set to High, the excitation position of the output is forcibly set to the initial state, and the MONI output is placed in the ON state. When RST is then set to Low, the excitation position is advanced by the next STEP input.

### (8) Output enable function

Only STM mode is pin at the DCM mode CMK: It operates as current LIMIT mask function.

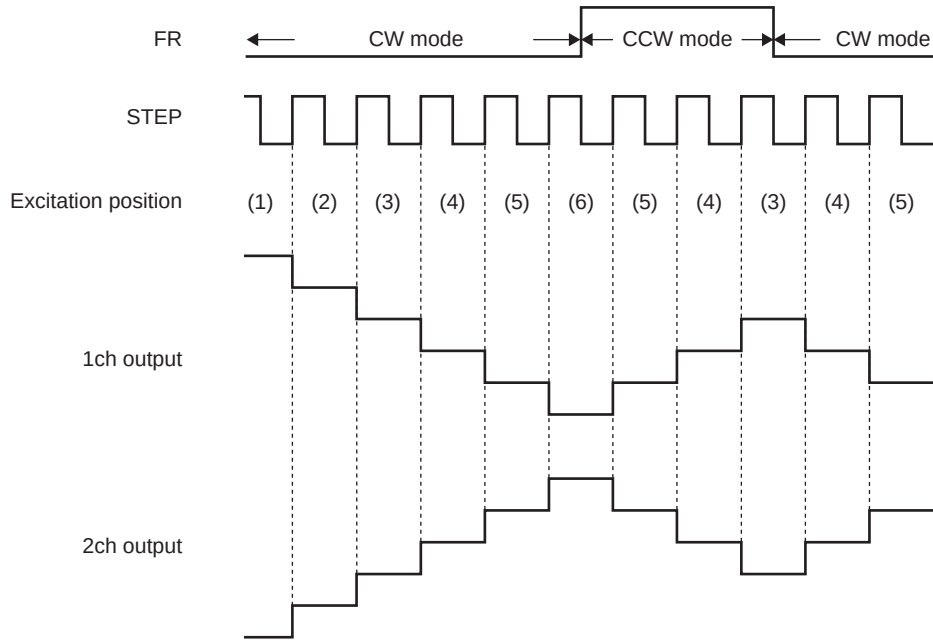
| OE   | Operating mode |
|------|----------------|
| Low  | Output ON      |
| High | Output OFF     |



When the OE pin is set High, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the STEP signal is input. Therefore, when OE is returned to Low, the output level conforms to the excitation position proceeded by the STEP input.

(9) Forward/reverse switching function

|      |                         |
|------|-------------------------|
| FR   | Operating mode          |
| Low  | Clockwise (CW)          |
| High | Counter-clockwise (CCW) |



The internal D/A converter proceeds by one bit at the rising edge of the input STEP pulse.

In addition, CW and CCW mode are switched by setting the FR pin.

In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.

In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(10) Chopping frequency setting

For constant-current control, this IC performs chopping operations at the frequency determined by the capacitor (Cchop) connected between the CHOP pin and GND.

The chopping frequency is set as shown below by the capacitor (Cchop) connected between the CHOP pin and GND.

$$F_{\text{chop}} = I_{\text{chop}} / (C_{\text{chop}} \times V_{\text{tchop}} \times 2) \text{ (Hz)}$$

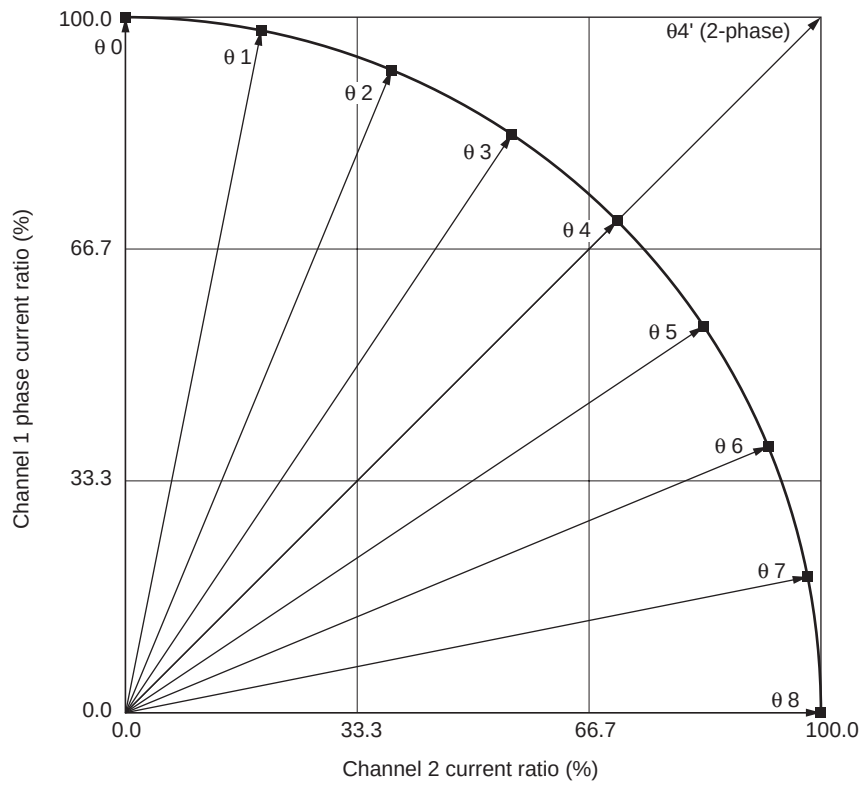
$I_{\text{chop}}$  : Capacitor charge/discharge current, typ 10μA

$V_{\text{tchop}}$  : Charge/discharge hysteresis voltage ( $V_{\text{tup}} - V_{\text{tdown}}$ ), typ 0.5V

For instance, when Cchop is 200pF, the chopping frequency will be as follows :

$$F_{\text{chop}} = 10\mu\text{A} / (200\text{pF} \times 0.5\text{V} \times 2) = 50\text{kHz}$$

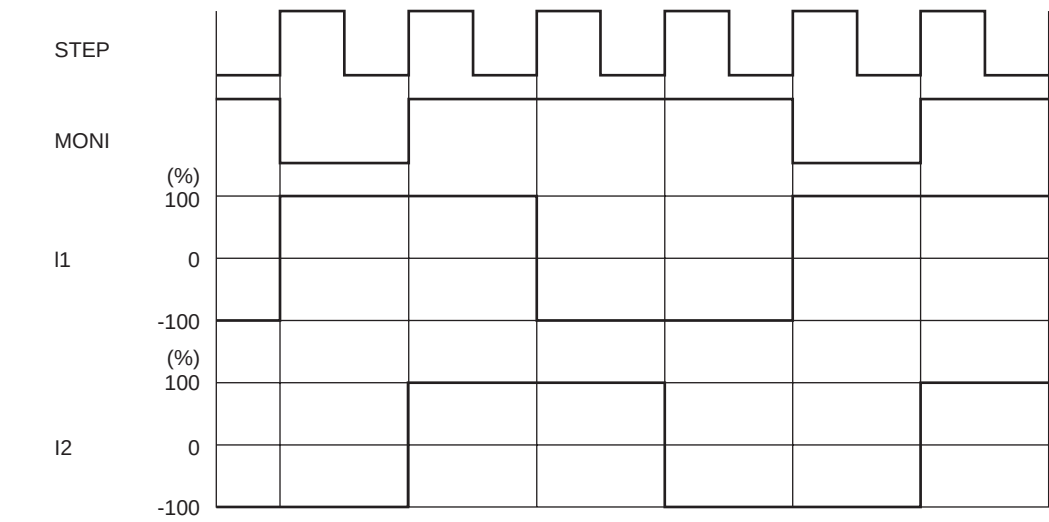
(11) Output current vector locus (one step is normalized to 90 degrees)



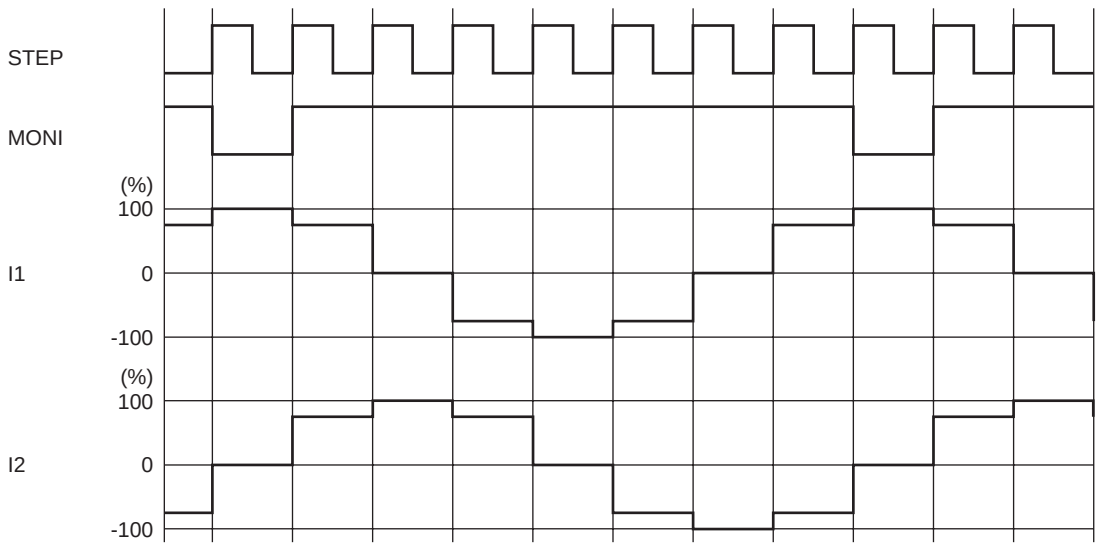
Setting current ration in each excitation mode

| STEP | 2W1-2 phase (%) |           | W1-2 phase (%) |           | 1-2 phase (%) |           | 2-phase (%) |           |
|------|-----------------|-----------|----------------|-----------|---------------|-----------|-------------|-----------|
|      | Channel 1       | Channel 2 | Channel 1      | Channel 2 | Channel 1     | Channel 2 | Channel 1   | Channel 2 |
| 00   | 100             | 0         | 100            | 0         | 100           | 0         |             |           |
| 01   | 98              | 20        |                |           |               |           |             |           |
| 02   | 92              | 38        | 92             | 38        |               |           |             |           |
| 03   | 83              | 55        |                |           |               |           |             |           |
| 04   | 70              | 70        | 70             | 70        | 70            | 70        | 100         | 100       |
| 05   | 55              | 83        |                |           |               |           |             |           |
| 06   | 38              | 92        | 38             | 92        |               |           |             |           |
| 07   | 20              | 98        |                |           |               |           |             |           |
| 08   | 0               | 100       | 0              | 100       | 0             | 100       |             |           |

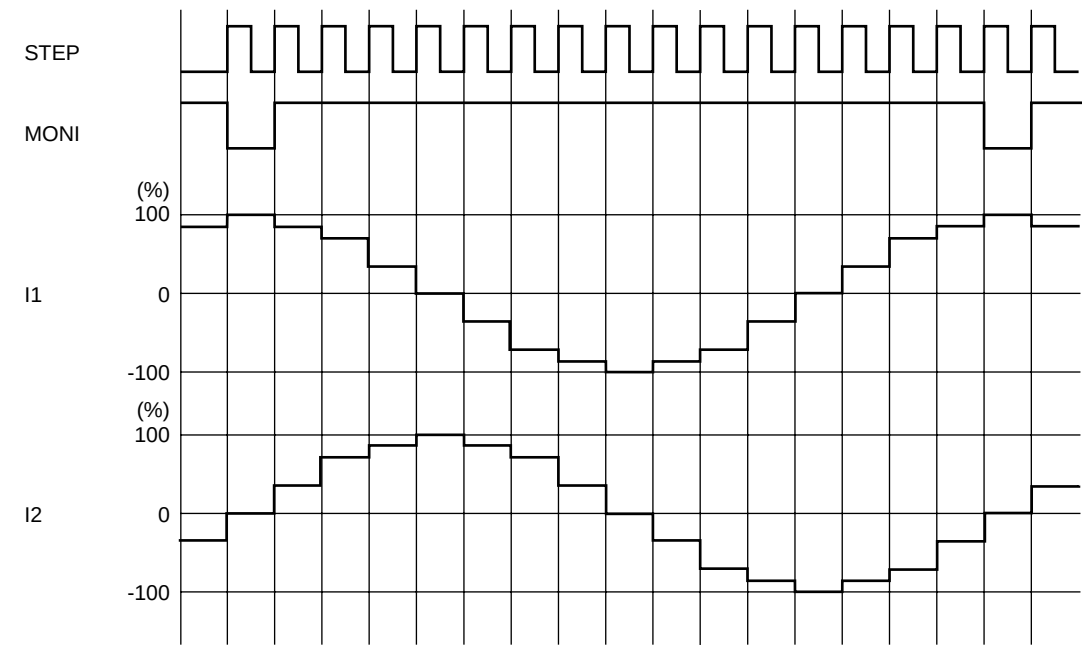
(12) Typical current waveform in each excitation mode  
2-phase excitation (CW mode)



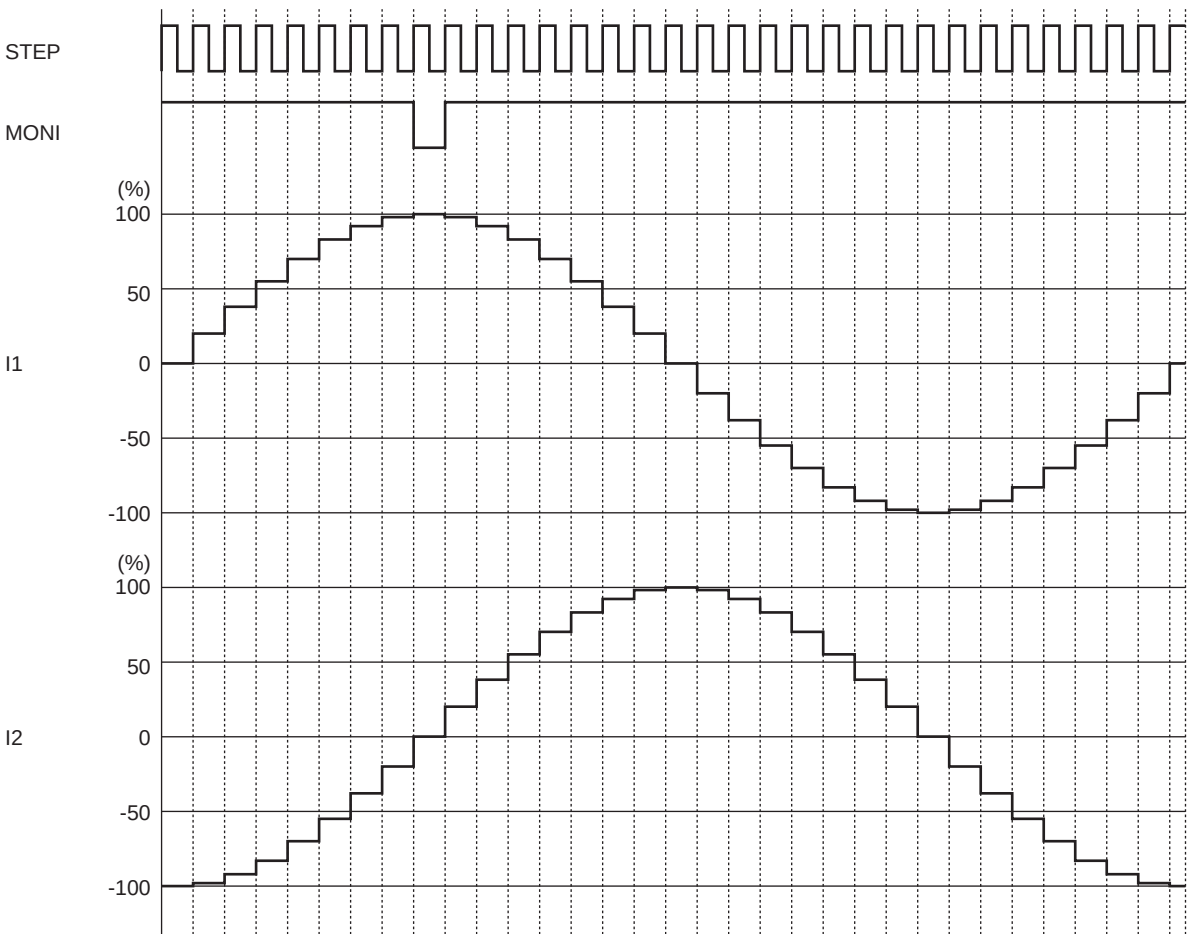
1-2 phase excitation (CW mode)



W1-2 phase excitation (CW mode)



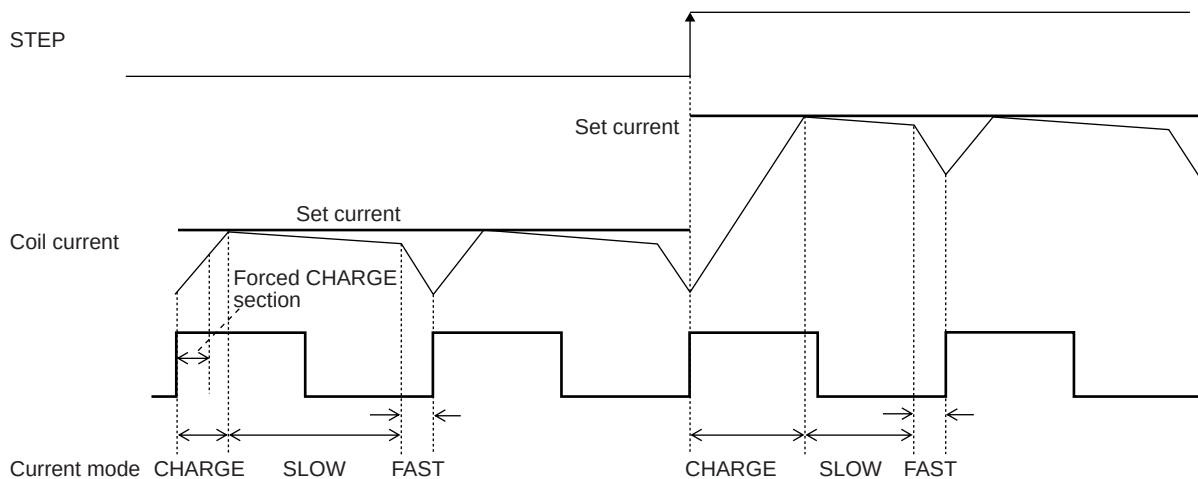
2W1-2 phase excitation (CW mode)



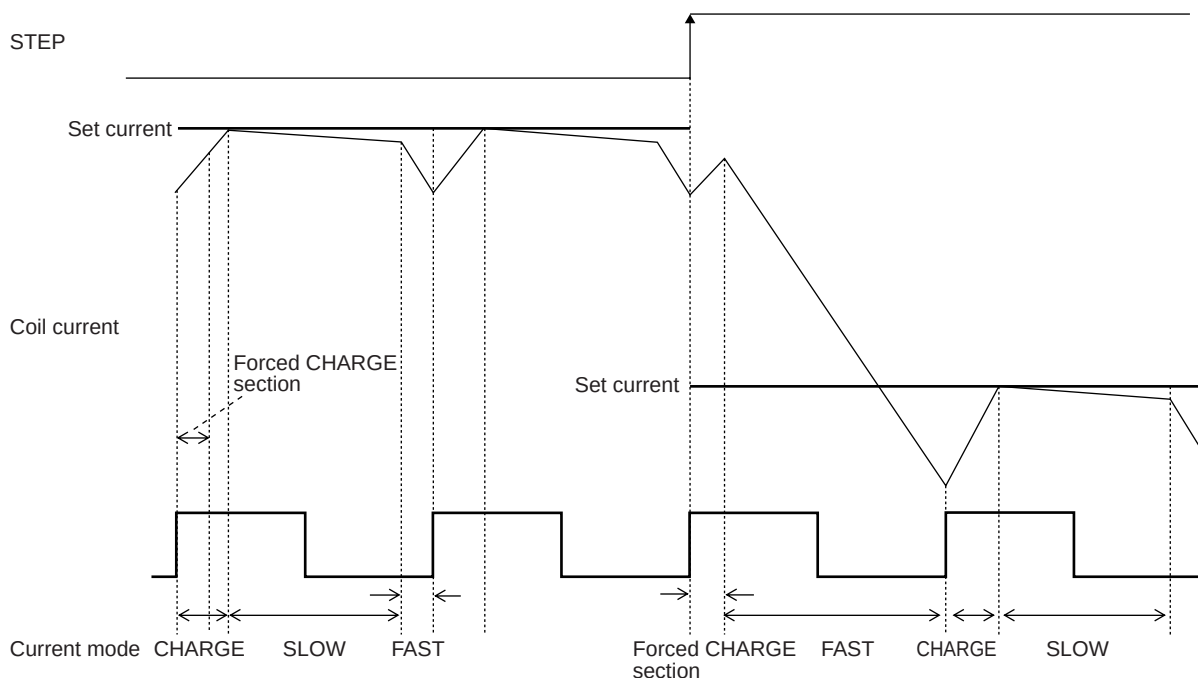


### (13) Current control operation specification

(Sine wave increasing direction)



(Sine wave decreasing direction)



In each current mode, the operation sequence is as described below :

- At rise of chopping frequency, the CHARGE mode begins. (In the time defined as the “blanking time,” the CHARGE mode is forced regardless of the magnitude of the coil current (ICOIL) and set current (IREF).)
- The coil current (ICOIL) and set current (IREF) are compared in this blanking time.

When  $(ICOIL < IREF)$  state exists ;

The CHARGE mode up to  $ICOIL \geq IREF$ , then followed by changeover to the SLOW DECAY mode, and finally by the FAST DECAY mode for approximately  $1\mu s$ .

When  $(ICOIL < IREF)$  state does not exist ;

The FAST DECAY mode begins. The coil current is attenuated in the FAST DECAY mode till one cycle of chopping is over.

Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the sine wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.

## DCM Mode (DM-High)

### (1) DCM mode output control logic

| Parallel input |           | Output     |            | Mode          |
|----------------|-----------|------------|------------|---------------|
| DC11 (21)      | DC12 (22) | OUT1 (2) A | OUT1 (2) B |               |
| Low            | Low       | OFF        | OFF        | Standby       |
| High           | Low       | High       | Low        | CW (Forward)  |
| Low            | High      | Low        | High       | CCW (Reverse) |
| High           | High      | Low        | Low        | Brake         |

### (2) Blanking time switching function

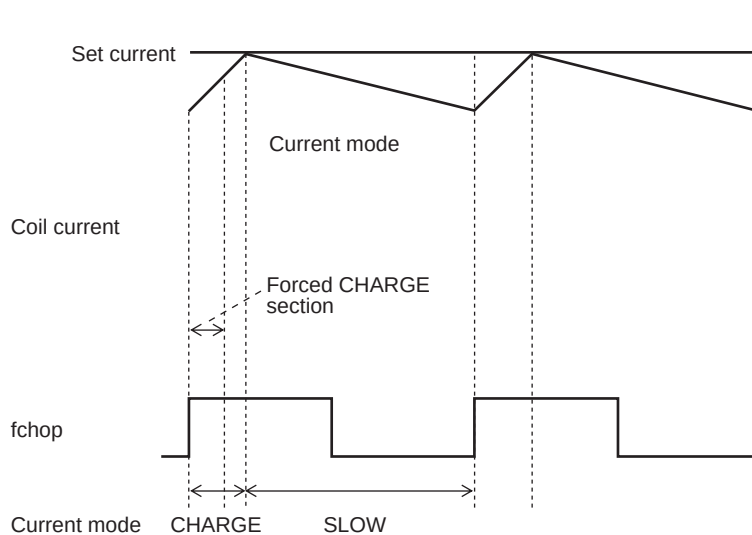
Only the DCM mode. At STM mode RST pin : It operates as RESET function.

| BLK  | Blanking time |
|------|---------------|
| Low  | 2μs           |
| High | 3μs           |

### (3) Current limit reference voltage setting function

By setting a current limit, this IC automatically exercises short braking control to ensure that when the motor current has reached this limit, the current will not exceed it.

(Current limit control time chart)



The limit current is set as calculated on the basis of the voltage input to the VREF pin and the resistance between the RF pin and GND using the formula given below.

$$I_{\text{limit}} = (V_{\text{REF}}/5) / R_{\text{F}} \text{ resistance}$$

The voltage applied to the VREF pin can be switched to any of the four setting levels depending on the statuses of the two inputs, ATT1 and ATT2.

Function for attenuating VREF input voltage

| ATT1 | ATT2 | Current setting reference voltage attenuation ratio |
|------|------|-----------------------------------------------------|
| Low  | Low  | 100%                                                |
| High | Low  | 80%                                                 |
| Low  | High | 50%                                                 |
| High | High | 20%                                                 |

The formula used to calculate the output current when using the function for attenuating the VREF input voltage is given below.

$$I_{\text{limit}} = (V_{\text{REF}}/5) \times (\text{attenuation ratio}) / R_{\text{F}} \text{ resistance}$$

Example : At VREF of 1.5V, a reference voltage setting of 100% [(ATT1, ATT2) = (L, L)] and an RF resistance of 0.5Ω, the output current is set as shown below.

$$I_{\text{limit}} = 1.5\text{V}/5 \times 100\%/0.5\Omega = 0.6\text{A}$$

If, in this state, (ATT1, ATT2) has been set to (H, H), I<sub>limit</sub> will be as follows :

$$I_{\text{limit}} = 0.6\text{A} \times 20\% = 120\text{mA}$$

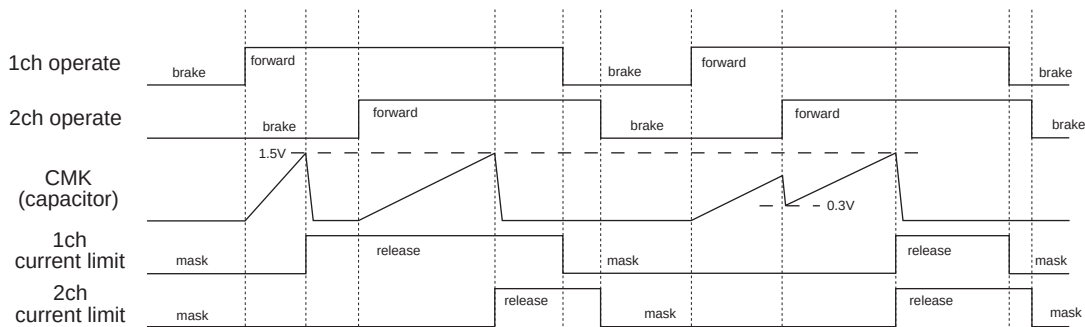
#### (4) Current LIMIT mask function

Only the DCM mode. At STM mode OE pin : It operates as output enable function.

The mask can do current LIMIT function during the fixed time set with the CMK pin at the DCM mode. It is effective to make it not hang to the limiter by the start current of the motor to set current LIMIT low.

The charge is begun, current LIMIT function is done to the CMK capacitor meanwhile when switching to forward/reverse mode, and the mask is done. Afterwards, the mask is released when the voltage of the CMK pin reaches set voltage (typ 1.5V), and the current limit function works.

When 2ch side begins forward (reverse) operation while the mask on 1ch side is operating, the CMK pin is discharged one degree up to a constant voltage, and begins charging again because the CMK pin becomes 2ch using combinedly. Meanwhile, 1ch side and 2ch side enter the state of the mask.



When the capacitor is not connected, the function of LIMIT in the current can be switched to operation/nonoperating state by the state of the input of the CMK pin.

| CMK         | Current LIMIT function |
|-------------|------------------------|
| "L"         | nonoperating           |
| "H" or OPEN | operation              |

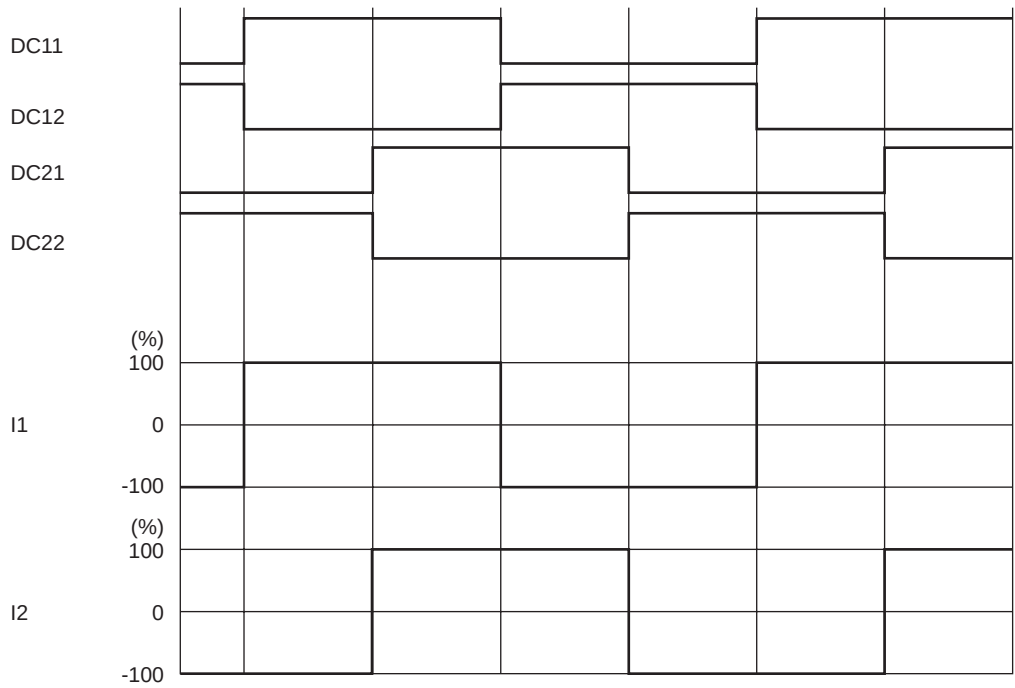
#### (5) Current LIMIT mask time (Tcmk)

The time of the mask of current LIMIT function can be set by connecting capacitor  $C_{CMK}$  between CMK pin - GND. Decide the value of capacitor  $C_{CMK}$  according to the following expressions.

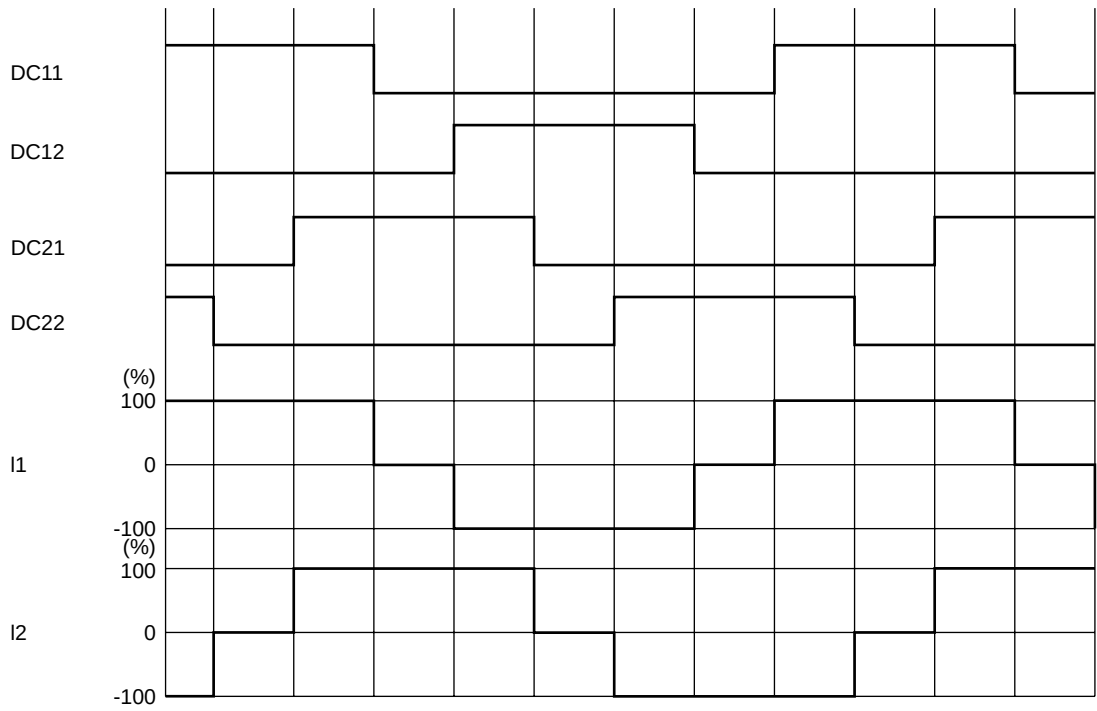
$$\text{Mask time : } T_{CMK} \quad T_{CMK} \approx -C_{CMK} \times R \times \ln \left( 1 - V_{tCMK} / (I_{CMK} \times R) \right) \quad (\text{sec})$$

$V_{tCMK}$  : LIMIT mask threshold voltage typ. 1.5V  
 $I_{CMK}$  : CMK pin charge current typ. 25 $\mu$ A  
 $R$  : Internal resistance typ. 100k $\Omega$

(6) Typical current waveform in each excitation mode when stepping motor parallel input control  
2-phase excitation (CW mode)



1-2 phase excitation full torque (CW mode)



## Output short-circuit protection function

This IC incorporates an output short-circuit protection circuit that, when the output has been shorted by an event such as shorting to power or shorting to ground, sets the output to the standby mode and turns on the warning output in order to prevent the IC from being damaged. In the stepping motor driver (STM) mode (DM = Low), this function sets the output to the standby mode for both channels by detecting the short-circuiting in one of the channels. In the DC motor driver mode (DM = High), channels 1 and 2 operate independently. (Even if the output of channel 1 has been short-circuited, channel 2 will operate normally.)

### (1) Output short-circuit protection operation changeover function

Changeover to the output short-circuit protection of IC is made by the setting of EMM pin.

| EMM         | State             |
|-------------|-------------------|
| Low or Open | Latch method      |
| High        | Auto reset method |

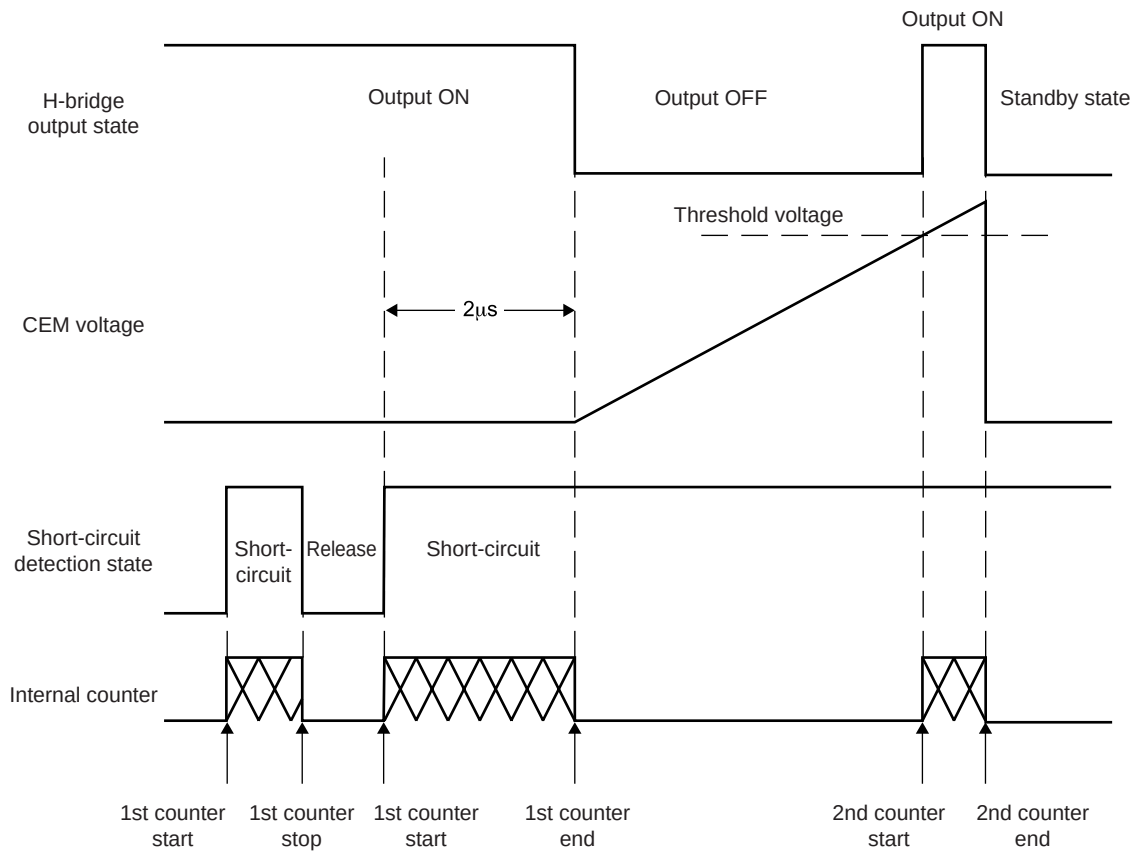
### (2) Latch type

In the latch mode, when the output current exceeds the detection current level, the output is turned OFF, and this state is held.

The detection of the output short-circuited state by the IC causes the output short-circuit protection circuit to be activated.

When the short-circuited state continues for the period of time set using the internal timer (approximately  $2\mu\text{s}$ ), the output in which the short-circuiting has been detected is first set to OFF. After this, the output is set to ON again as soon as the timer latch time (Tcem) described later has been exceeded, and if the short-circuited state is still detected, all the outputs of the channel concerned are switched to the standby mode, and this state is held.

This state is released by setting ST to low.



### (3) Auto reset type

In the automatic reset mode, when the output current exceeds the detection current level, the output waveform changes to the switching waveform.

As with the latch system, when the output short-circuited state is detected, the short-circuit protection circuit is activated. When the operation of the short-circuit detection circuit exceeds the timer latch time (Tcem) described later, the output is changed over to the standby mode and is reset to the ON mode again in 2ms (typ). In this event, if the overcurrent mode still continues, the switching mode described above is repeated until the overcurrent mode is canceled.

### (4) Unusual condition warning output pins (EMO, MONI)

The LV8731V is provided with the EMO pin which notifies the CPU of an unusual condition if the protection circuit operates by detecting an unusual condition of the IC. This pin is of the open-drain output type and when an unusual condition is detected, the EMO output is placed in the ON (EMO = Low) state.

In the DC motor driver mode (DM = High), the MONI pin also functions as a warning output pin.

The functions of the EMO pin and MONI pin change as shown below depending on the state of the DM pin.

When the DM is low (STM mode) :

EMO : Unusual condition warning output pin

MONI : Excitation initial position detection monitoring

When the DM is high (DCM) mode) :

EMO : Channel 1 warning output pin

MONI : Channel 2 warning output pin

Furthermore, the EMO (MONI) pin is placed in the ON state when one of the following conditions occurs.

1. Shorting-to-power, shorting-to-ground, or shorting-to-load occurs at the output pin and the output short-circuit protection circuit is activated.
2. The IC junction temperature rises and the thermal protection circuit is activated.

| Unusual condition                | DM = L (STM mode) |      | DM = H (DCM mode) |      |
|----------------------------------|-------------------|------|-------------------|------|
|                                  | EMO               | MONI | EMO               | MONI |
| Channel 1 short-circuit detected | ON                | -    | ON                | -    |
| Channel 2 short-circuit detected | ON                | -    | -                 | ON   |
| Overheating condition detected   | ON                | -    | ON                | ON   |

### (5) Timer latch time (Tcem)

The time taken for the output to be set to OFF when the output has been short-circuited can be set using capacitor Ccem, connected between the CEM pin and GND. The value of capacitor Ccem is determined by the formula given below.

Timer latch : Tcem

$$Tcem \approx Ccem \times Vtcm / Icem \text{ [sec]}$$

Vtcm : Comparator threshold voltage, typ 1V

Icem : CEM pin charge current, typ 10μA

## Overheating protection function

The overheating protection circuit is built into, and the output is turned off when junction temperature Tj exceeds 180°C, and the abnormal state warning output is turned on at the same time. The value of hysteresis and when it falls, the temperature drives the output again (automatic restoration).

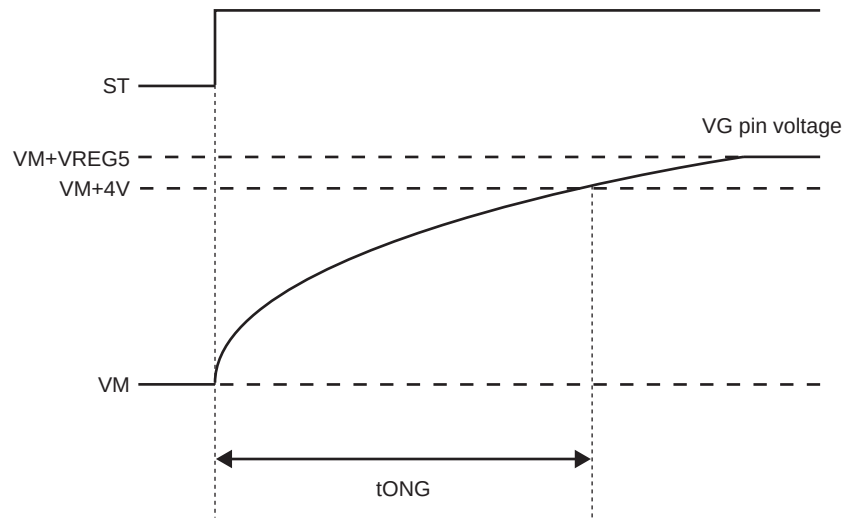
The overheating protection circuit doesn't secure protection and the destruction prevention of the set because it becomes operation by the area where ratings Tjmax=150°C of the junction temperature was exceeded.

TSD = 180°C (typ)

ΔTSD = 40°C (typ)

**Charge Pump Circuit**

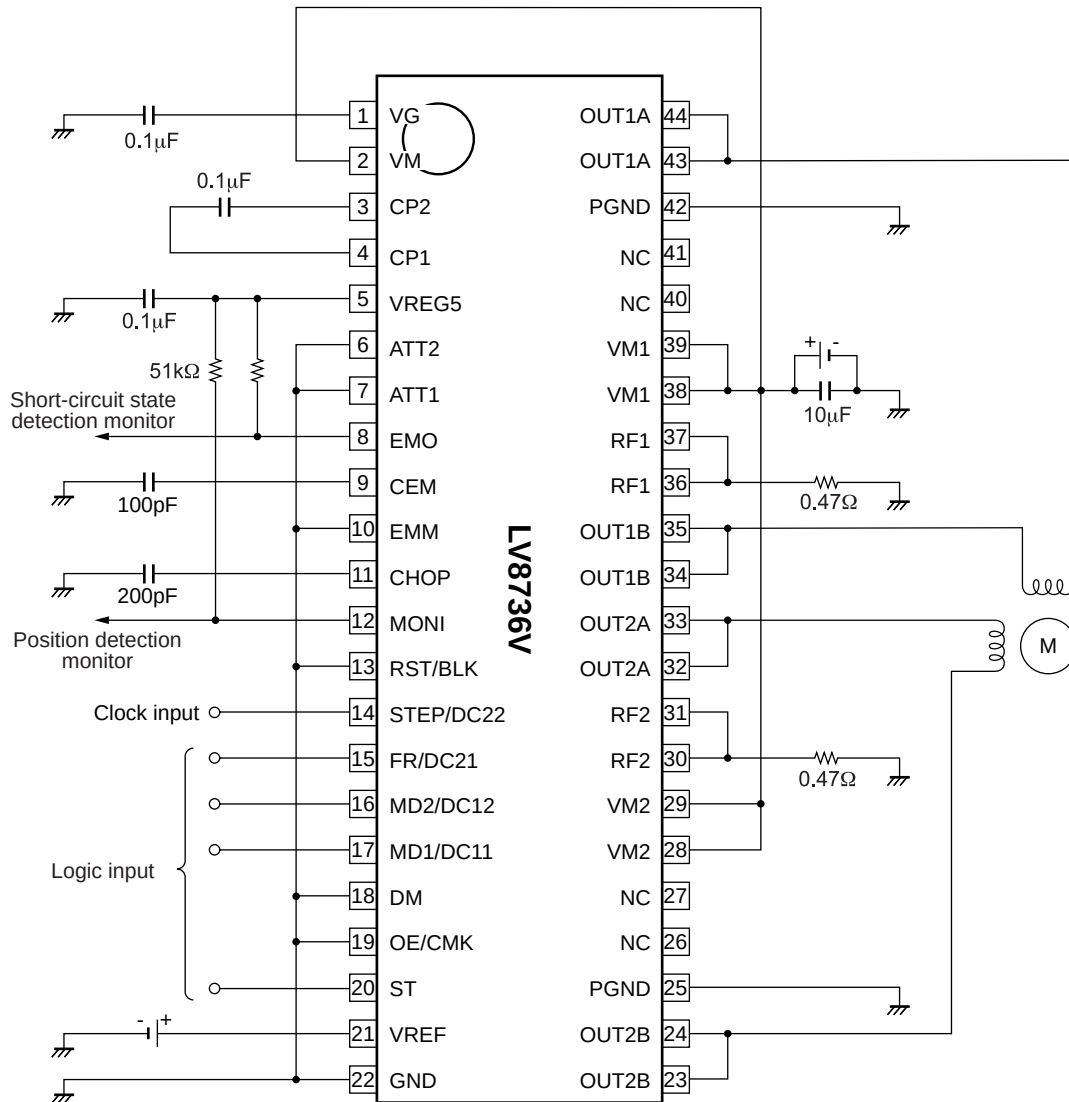
When the ST pin is set High, the charge pump circuit operates and the VG pin voltage is boosted from the VM voltage to the VM + VREG5 voltage. Because the output is not turned on if VM+4V or more is not pressured, the voltage of the VG pin recommends the drive of the motor to put the time of  $t_{ONG}$  or more, and to begin.



VG Pin Voltage Schematic View

## Application Circuit Example

- Stepping motor driver circuit (DM = Low)



The formulae for setting the constants in the examples of the application circuits above are as follows :

Constant current (100%) setting

When VREF = 1.5V

$$I_{OUT} = VREF / 5 / RF \text{ resistance} \\ = 1.5V / 5 / 0.47\Omega = 10.64A$$

Chopping frequency setting

$$F_{chop} = I_{chop} / (C_{chop} \times V_{tchop} \times 2) \\ = 10\mu A / (200pF \times 0.5V \times 2) = 50kHz$$

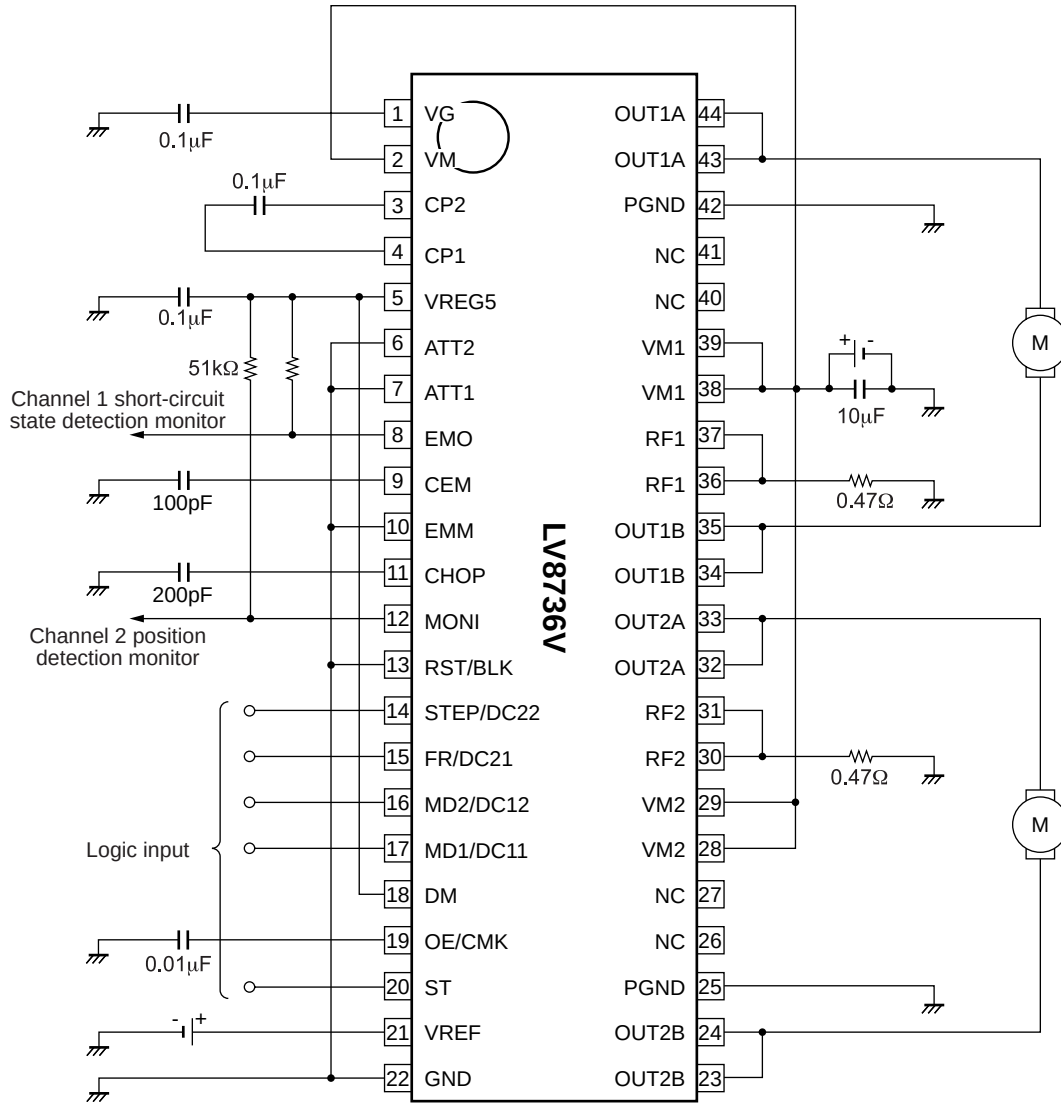
Timer latch time when the output is short-circuited

$$T_{cem} = C_{cem} \times V_{tcem} / I_{cem} \\ = 100pF \times 1V / 10\mu A = 10\mu s$$



## LV8736V

- DC motor driver circuit (DM = High, and the current limit function is in use.)



The formulae for setting the constants in the examples of the application circuits above are as follows :

Constant current limit (100%) setting

When VREF = 1.5V

$$I_{limit} = VREF / 5 / RF \text{ resistance}$$

$$= 1.5V / 5 / 0.47\Omega = 0.6A$$

Chopping frequency setting

$$F_{chop} = I_{chop} / (C_{chop} \times V_{tchop} \times 2)$$

$$= 10\mu A / (200pF \times 0.5V \times 2) = 50kHz$$

Timer latch time when the output is short-circuited

$$T_{cem} = C_{cem} \times V_{tcem} / I_{cem}$$

$$= 100pF \times 1V / 10\mu A = 10\mu s$$

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