

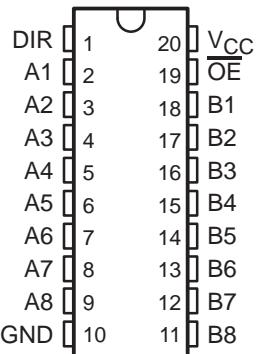
SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639 OCTAL BUS TRANSCEIVERS

SDAS123A – DECEMBER 1983 – REVISED JANUARY 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Choice of True or Inverting Logic
- A-Bus Outputs Are Open Collector; B-Bus Outputs Are 3 State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

DEVICE	A OUTPUT	B OUTPUT	LOGIC
SN74ALS638A, SN74AS638A	Open collector	3 state	Inverting
SN74ALS639A, SN74AS639	Open collector	3 state	True

DW OR N PACKAGE (TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3 state) or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are isolated.

The -1 version of SN74ALS638A is identical to the standard version, except that the recommended maximum I_{OL} is increased to 48 mA.

The SN74ALS638A, SN74ALS639A, SN74AS638A, and SN74AS639 are characterized for operation from 0°C to 70°C.

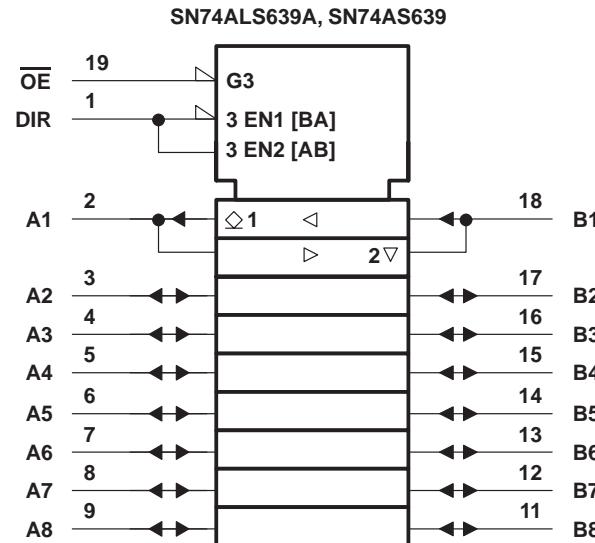
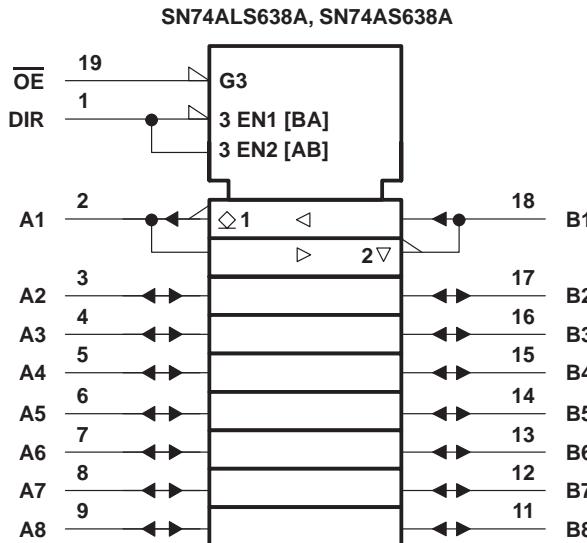
FUNCTION TABLE

INPUTS		OPERATION	
\overline{OE}	DIR	SN74ALS638A SN74AS638A	SN74ALS639A SN74AS639
L	L	B data to A bus	B data to A bus
L	H	\overline{A} data to B bus	A data to B bus
H	X	Isolation	Isolation

SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639 OCTAL BUS TRANSCEIVERS

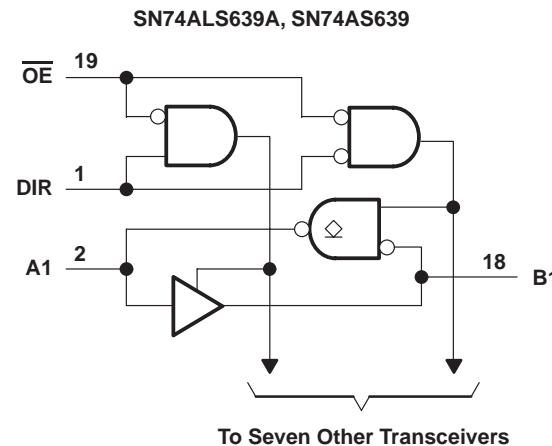
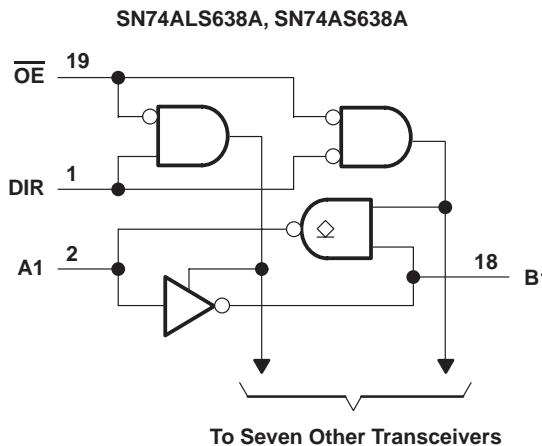
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logic symbols[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
A-bus I/O ports	7 V
B-bus I/O ports	5.5 V
Operating free-air temperature range, T_A : SN74ALS638A, SN74ALS639A	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639 OCTAL BUS TRANSCEIVERS

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recommended operating conditions

		SN74ALS638A SN74ALS639A			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage		0.8		V
V _{OH}	High-level output voltage	A ports		5.5	V
I _{OH}	High-level output current	B ports		-15	mA
I _{OL}	Low-level output current	A or B ports		24	mA
				48 [†]	
T _A	Operating free-air temperature	0	70		°C

[†] Applies only to the SN74ALS638A-1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN74ALS638A SN74ALS639A	UNIT
					MIN	
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA		-1.5	V
I _{OH}	A ports	V _{CC} = 4.5 V,	V _{OH} = 5.5 V		0.1	mA
V _{OH}	B ports	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = -0.4 mA	V _{CC} - 2		V
		V _{CC} = 4.5 V	I _{OH} = -3 mA	2.4	3.2	
			I _{OH} = -15 mA	2		
V _{OL}	A or B ports	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	V
			I _{OL} = 24 mA	0.35	0.5	
			I _{OL} = 48 mA [†]	0.35	0.5	
I _I	Control inputs	V _{CC} = 5.5 V	V _I = 7 V		0.1	mA
	A or B ports		V _I = 5.5 V		0.1	
I _{IH}	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V		20	μA
	A or B ports [§]				20	
I _{IL}	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V		-0.1	mA
	A or B ports [§]				-0.1	
I _{O[¶]}	B ports	V _{CC} = 5.5 V,	V _O = 2.25 V	-30	-112	mA
I _{CC}	SN74ALS638A	V _{CC} = 5.5 V	Outputs high	18	30	mA
			Outputs low	26	41	
			Outputs disabled	16	30	
	SN74ALS639A	V _{CC} = 5.5 V	Outputs high	25	40	
			Outputs low	30	50	
			Outputs disabled	33	54	

[†] Applies only to the SN74ALS638A-1 version and only if V_{CC} is between 4.75 V and 5.25 V

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[¶] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639 OCTAL BUS TRANSCEIVERS

SDAS123A – DECEMBER 1983 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 680\text{ }\Omega$ (A outputs), $R1 = R2 = 500\text{ }\Omega$ (B outputs), $T_A = \text{MIN to MAX}^{\dagger}$	UNIT			
			SN74ALS638A		SN74ALS639A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	12	2	12	ns
t_{PHL}			2	12	2	12	
t_{PLH}	B	A	8	25	10	30	ns
t_{PHL}			8	30	5	22	
t_{PLH}	\overline{OE}	A	5	25	10	30	ns
t_{PHL}			10	45	10	35	
t_{PZH}	\overline{OE}	B	5	20	6	21	ns
t_{PZL}			5	22	8	25	
t_{PHZ}	\overline{OE}	B	2	10	2	10	ns
t_{PLZ}			3	15	3	16	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
A-bus I/O ports	7 V
B-bus I/O ports	5.5 V
Operating free-air temperature range, T_A : SN74AS638A, SN74AS639	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74AS638A SN74AS639			UNIT
	MIN	NOM	MAX			
V_{CC} Supply voltage	4.5	5	5.5	V		
V_{IH} High-level input voltage		2		V		
V_{IL} Low-level input voltage			0.8	V		
V_{OH} High-level output voltage	A ports		5.5	V		
I_{OH} High-level output current	B ports		-15	mA		
I_{OL} Low-level output current	A or B ports		64	mA		
T_A Operating free-air temperature	0		70	°C		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS638A		UNIT
				MIN	TYP†	
V_{IK}		$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$		-1.2	V
I_{OH}	A ports	$V_{CC} = 4.5 \text{ V}$,	$V_{OH} = 5.5 \text{ V}$		0.1	mA
V_{OH}	B ports	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$,	$I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$		V
		$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	
			$I_{OH} = -15 \text{ mA}$	2.4		
V_{OL}	A or B ports	$V_{CC} = 4.5 \text{ V}$,	$I_{OL} = 64 \text{ mA}$	0.35	0.55	V
I_I	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 7 \text{ V}$	0.1		mA
	A or B ports		$V_I = 5.5 \text{ V}$	0.1		
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 2.7 \text{ V}$	20		μA
	A or B ports‡			70		
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 0.4 \text{ V}$	-0.5		mA
	A or B ports‡			-0.75		
$I_O\$$		$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.25 \text{ V}$	-50	-150	mA
I_{CC}	SN74AS638A	$V_{CC} = 5.5 \text{ V}$	Outputs high	24	54	mA
			Outputs low	75	122	
			Outputs disabled	37	61	
	SN74AS639	$V_{CC} = 5.5 \text{ V}$	Outputs high	56	92	
			Outputs low	95	154	
			Outputs disabled	62	100	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

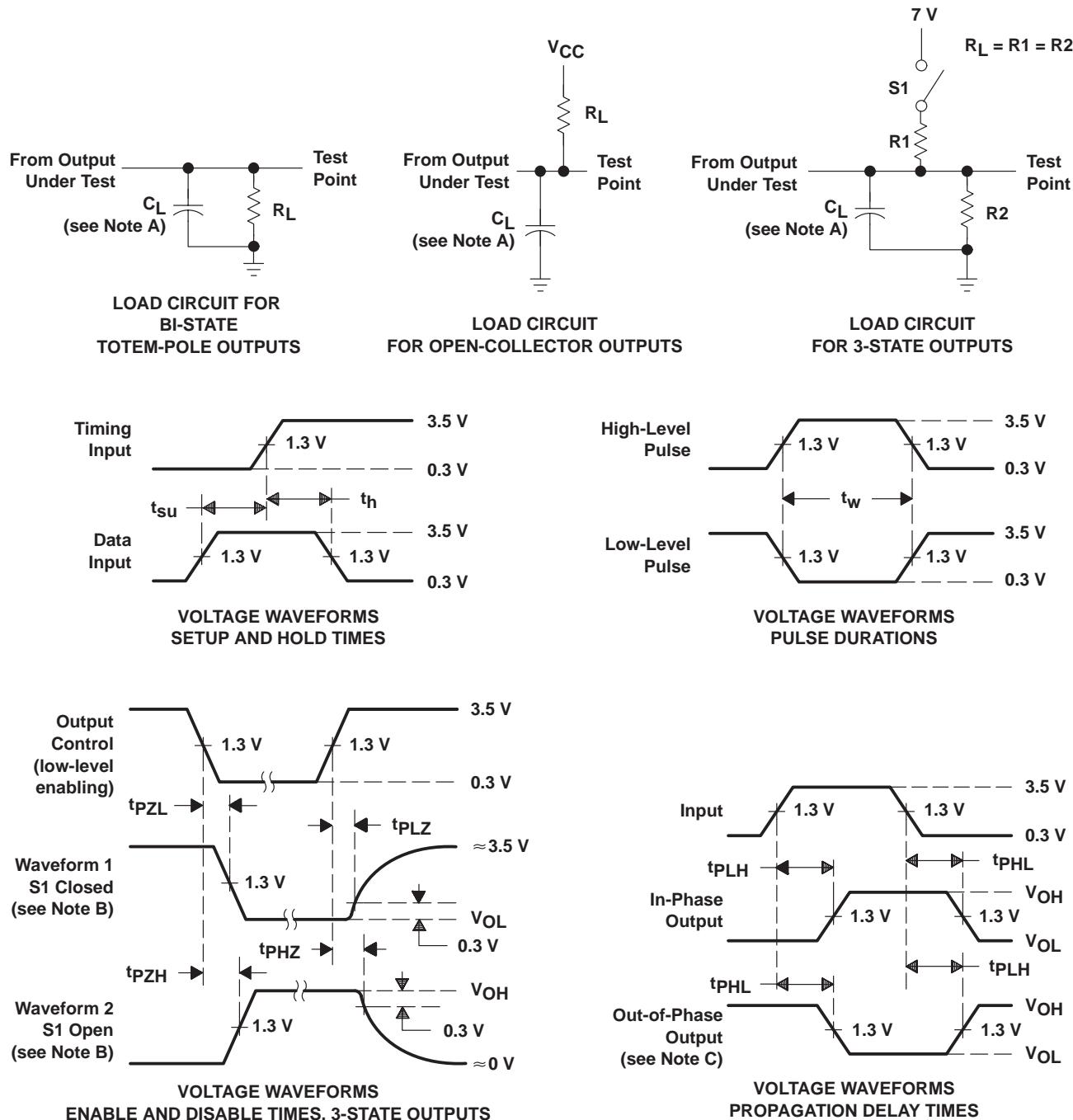
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$ (A outputs), $R_1 = R_2 = 500 \Omega$ (B outputs), $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN74AS638A		SN74AS639			
			MIN	MAX	MIN	MAX		
t_{PLH}	A	B	2	7	2	9.5	ns	
			2	6.5	2	9		
t_{PLH}	B	A	5	20	5	22	ns	
			2	7	2	9		
t_{PLH}	\overline{OE}	A	5	19	5	21.5	ns	
			2	9	2	11.5		
t_{PZH}	\overline{OE}	B	2	8	2	10.5	ns	
			2	10	2	10.5		
t_{PHZ}	\overline{OE}	B	2	7	2	7	ns	
			2	10	2	10.5		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639 OCTAL BUS TRANSCEIVERS

SDAS123A – DECEMBER 1983 – REVISED JANUARY 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALS638A-1DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638A-1DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638A-1DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638A-1DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638A-1DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638A-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS638A-1NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS638A-1NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638A-1NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638A-1NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS638ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS638ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS638ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALS639ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS639ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS639ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS638AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS638ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS638ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS638ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS638ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS639DW	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
SN74AS639DWR	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
SN74AS639N	OBsolete	PDIP	N	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

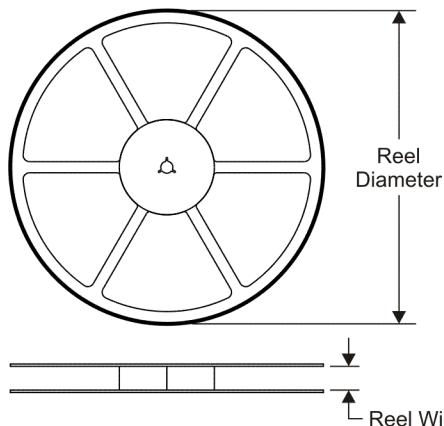
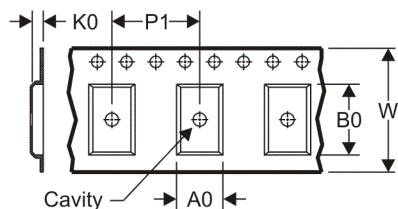
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

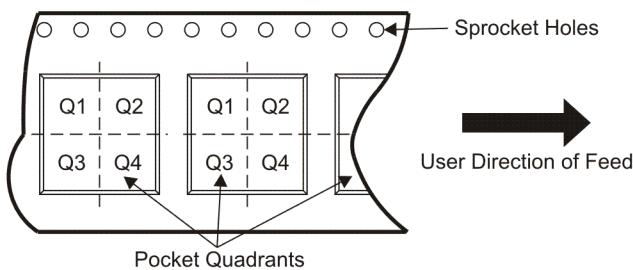
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


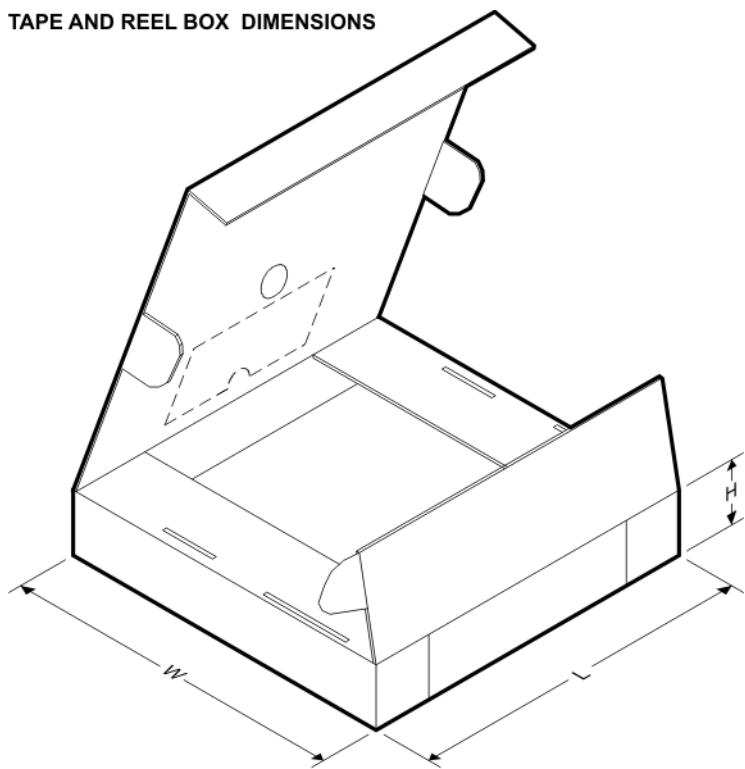
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS638A-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS639ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS638A-1DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS639ADWR	SOIC	DW	20	2000	346.0	346.0	41.0

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

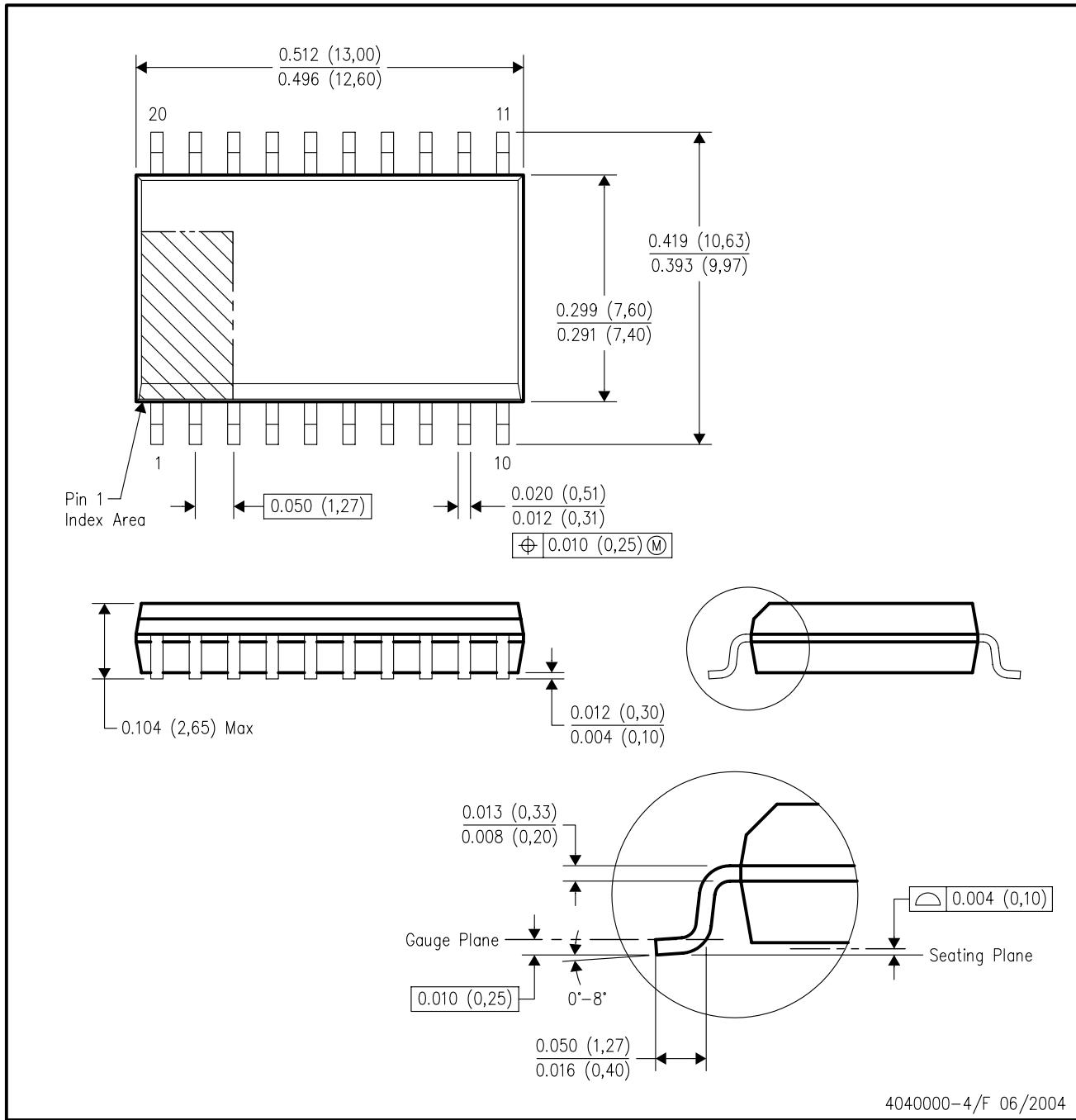


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DW (R-PDSO-G20)

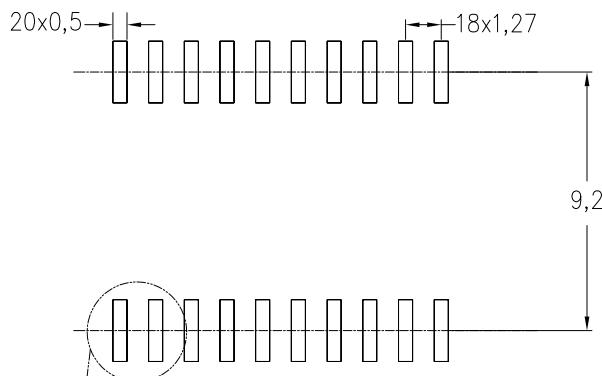
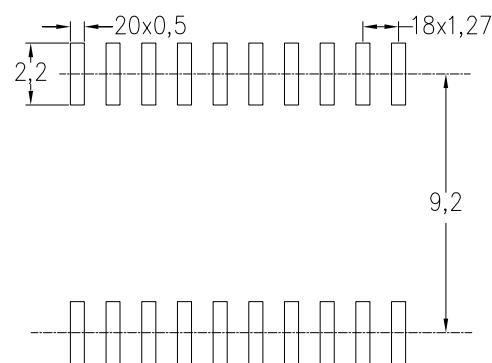
PLASTIC SMALL-OUTLINE PACKAGE



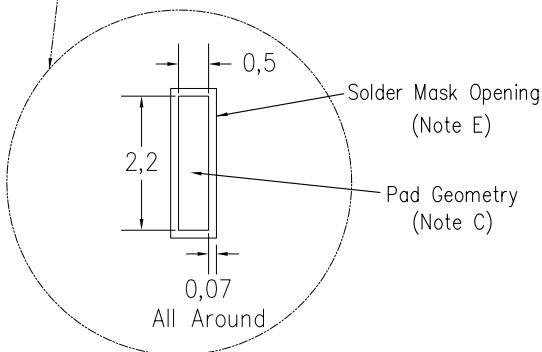
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

Example Board Layout
(Note C)Stencil Openings
(Note D)

Non Solder Mask Define Pad



4209202/A 01/08

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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