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# STK672-060-E

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**Thick-Film Hybrid IC**

**Unipolar Constant-current Chopper (external excitation  
PWM) Circuit with Built-in Microstepping Controller  
Stepping Motor Driver (sine wave drive)  
Output Current 1.2A (no heat sink\*)**

## Overview

The STK672-060-E is a stepping motor driver hybrid IC that uses power MOSFETs in the output stage. It includes a built-in microstepping controller and is based on a unipolar constant-current PWM system. The STK672-060-E supports application simplification and standardization by providing a built-in 4 phase distribution stepping motor controller. It supports five excitation methods: 2 phase, 1-2 phase, W1-2 phase, 2W1-2 phase, and 4W1-2 phase excitations, and can provide control of the basic stepping angle of the stepping motor divided into 1/16 step units. It also allows the motor speed to be controlled with only a clock signal.

The use of this hybrid IC allows designers to implement systems that provide high motor torques, low vibration levels, low noise, fast response, and high-efficiency drive.

## Applications

- Facsimile stepping motor drive (send and receive)
- Paper feed and optical system stepping motor drive in copiers
- Laser printer drum drive
- Printer carriage stepping motor drive
- X-Y plotter pen drive
- Other stepping motor applications

Note\*: Conditions:  $V_{CC1} = 24V$ ,  $I_{OH} = 1.2A$ , 2W1-2 excitation mode.

## Features

- Can implement stepping motor drive systems simply by providing a DC power supply and a clock pulse generator.

### <Control Block Features>

- One of five drive types can be selected with the drive mode settings (M1, M2, and M3)
  - 1) 2 phase excitation drive
  - 2) 1-2 phase excitation drive
  - 3) W1-2 phase excitation drive
  - 4) 2W1-2 phase excitation drive
  - 5) 4W1-2 phase excitation drive
- Provides four freely selectable modes for the vector locus during microstepping drive: circular mode, one inside mode, and two outside modes.
- Phase retention even if excitation is switched.
- The excitation phase state can be verified in real time using the MO1, MO2, and MOI signal output pins.
- The CLK input counter block can be selected to be one of the following by the high/low setting of the M3 input pin.
  - 1) Rising edge only
  - 2) Both rising and falling edges
- The CLK and RETURN input pins include built-in malfunction prevention circuits for external pulse noise.
- ENABLE and RESET pins provided. These are Schmitt trigger inputs with built-in 20k $\Omega$  (typical) pull-up resistors.
- No noise generation due to the difference between the A and B phase time constants during motor hold since external excitation is used.
- Microstepping operation supported even for small motor currents, since the reference voltage Vref can be set to any value between 0V and 1/2V<sub>CC2</sub>.

### <Driver Block>

- External excitation PWM drive allows a wide operating supply voltage range (V<sub>CC1</sub> = 10 to 45V) to be used.
- Current detection resistor (0.22 $\Omega$ ) built-in the hybrid IC itself.
- Power MOSFETs adopted for low drive loss.
- Provides a motor output drive current of I<sub>OH</sub> = 1.2A.

## Specifications

### Absolute Maximum Ratings at Ta = 25°C

| Parameter                       | Symbol               | Conditions                                   | Ratings      | Unit |
|---------------------------------|----------------------|----------------------------------------------|--------------|------|
| Maximum supply voltage 1        | V <sub>CC1</sub> max | No signal                                    | 52           | V    |
| Maximum supply voltage 2        | V <sub>CC2</sub> max | No signal                                    | -0.3 to +7.0 | V    |
| Input voltage                   | V <sub>IN</sub> max  | Logic input pins                             | -0.3 to +7.0 | V    |
| Output current                  | I <sub>OH</sub> max  | 0.5s, 1 pulse, when V <sub>CC1</sub> applied | 1.6          | A    |
| Repeated avalanche capacity     | E <sub>ar</sub> max  |                                              | 25           | mJ   |
| Allowable power dissipation     | P <sub>d</sub> max   | $\theta_{c-a} = 0$                           | 7            | W    |
| Operating substrate temperature | T <sub>c</sub> max   |                                              | 105          | °C   |
| Junction temperature            | T <sub>j</sub> max   |                                              | 150          | °C   |
| Storage temperature             | T <sub>stg</sub>     |                                              | -40 to +125  | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### Allowable Operating Ranges at Ta = 25°C

| Parameter                      | Symbol           | Conditions                                                     | Ratings               | Unit |
|--------------------------------|------------------|----------------------------------------------------------------|-----------------------|------|
| Supply voltage 1               | V <sub>CC1</sub> | With signals applied                                           | 10 to 45              | V    |
| Supply voltage 2               | V <sub>CC2</sub> | With signals applied                                           | 5 $\pm$ 5%            | V    |
| Input voltage                  | V <sub>IH</sub>  |                                                                | 0 to V <sub>CC2</sub> | V    |
| Phase driver withstand voltage | V <sub>DSS</sub> | Tr1, 2, 3, and 4 (the A, $\bar{A}$ , B, and $\bar{B}$ outputs) | 100 (min)             | V    |
| Output current                 | I <sub>OH</sub>  | Duty 50%                                                       | 1.2                   | A    |

## STK672-060-E

**Electrical Characteristics** at  $T_c = 25^\circ\text{C}$ ,  $V_{CC1} = 24\text{V}$ ,  $V_{CC2} = 5\text{V}$

| Parameters                         | Symbols    | Conditions                                                                                   | Rating |       |       | unit          |
|------------------------------------|------------|----------------------------------------------------------------------------------------------|--------|-------|-------|---------------|
|                                    |            |                                                                                              | min    | typ   | max   |               |
| Control supply current             | $I_{CC}$   | Pin 7, with ENABLE pin held low.                                                             |        | 2.5   | 14    | mA            |
| Output saturation voltage          | $V_{sat}$  | $R_L = 23\Omega$ ( $I \approx 1\text{A}$ )                                                   |        | 0.8   | 1.1   | V             |
| Average output current             | $I_{oave}$ | Load: $R = 3.5\Omega$ / $L = 3.8\text{mH}$<br>For each phase, $V_{ref} \approx 1.69\text{V}$ | 0.470  | 0.524 | 0.580 | A             |
| FET diode forward voltage          | $V_{df}$   | $I_f = 1\text{A}$                                                                            |        | 1.2   | 1.8   | V             |
| [Control Inputs]                   |            |                                                                                              |        |       |       |               |
| Input voltage                      | $V_{IH}$   | Except for the $V_{ref}$ pin                                                                 | 4      |       |       | V             |
|                                    | $V_{IL}$   | Except for the $V_{ref}$ pin                                                                 |        |       | 1     | V             |
| Input current                      | $I_{IH}$   | Except for the $V_{ref}$ pin                                                                 | 0      | 1     | 10    | $\mu\text{A}$ |
|                                    | $I_{IL}$   | Except for the $V_{ref}$ pin                                                                 | 125    | 250   | 510   | $\mu\text{A}$ |
| [Vref Input Pin]                   |            |                                                                                              |        |       |       |               |
| Input voltage                      | $V_I$      | Pin 8                                                                                        | 0      |       | 2.5   | V             |
| Input current                      | $I_I$      | Pin 8, $V_I = 2.5\text{V}$                                                                   | 330    | 415   | 545   | $\mu\text{A}$ |
| [Control Outputs]                  |            |                                                                                              |        |       |       |               |
| Output voltage                     | $V_{OH}$   | $I = -3\text{mA}$ , pins MOI, MO1, MO2                                                       | 2.4    |       |       | V             |
|                                    | $V_{OL}$   | $I = +3\text{mA}$ , pins MOI, MO1, MO2                                                       |        |       | 0.4   | V             |
| [Current Distribution Ratio (A-B)] |            |                                                                                              |        |       |       |               |
| 2W1-2, W1-2, 1-2                   | $V_{ref}$  | $\theta = 1/8$                                                                               |        | 100   |       | %             |
| 2W1-2, W1-2                        | $V_{ref}$  | $\theta = 2/8$                                                                               |        | 92    |       | %             |
| 2W1-2                              | $V_{ref}$  | $\theta = 3/8$                                                                               |        | 83    |       | %             |
| 2W1-2, W1-2, 1-2                   | $V_{ref}$  | $\theta = 4/8$                                                                               |        | 71    |       | %             |
| 2W1-2                              | $V_{ref}$  | $\theta = 5/8$                                                                               |        | 55    |       | %             |
| 2W1-2, W1-2                        | $V_{ref}$  | $\theta = 6/8$                                                                               |        | 40    |       | %             |
| 2W1-2                              | $V_{ref}$  | $\theta = 7/8$                                                                               |        | 21    |       | %             |
| 2                                  | $V_{ref}$  |                                                                                              |        | 100   |       | %             |
| PWM frequency                      | $f_c$      |                                                                                              | 37     | 47    | 57    | kHz           |

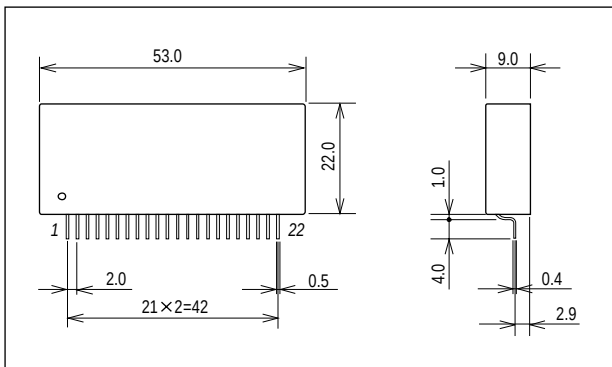
Note: A constant-voltage power supply must be used.

The design target value is shown for the current distribution ratio.

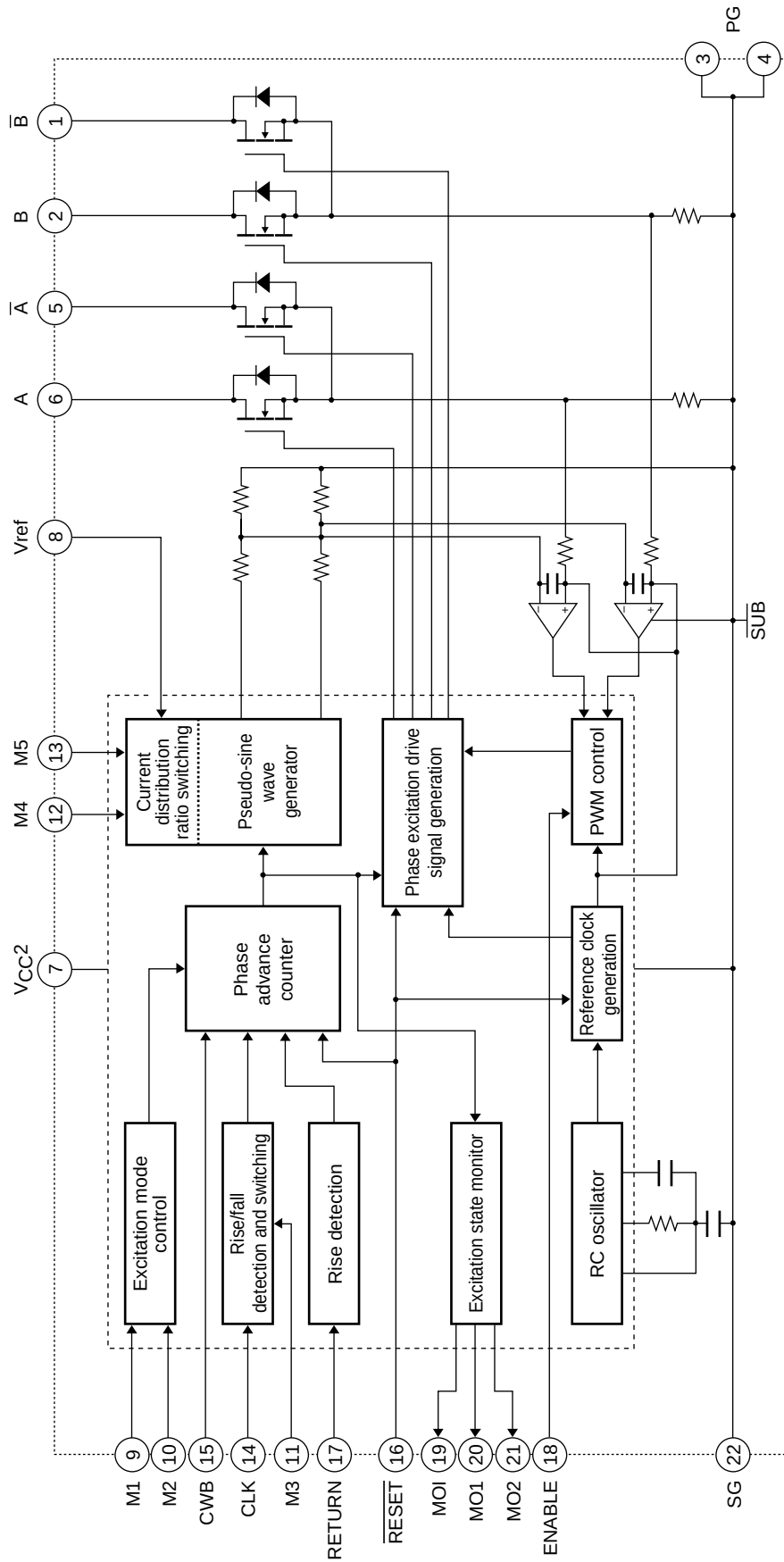
## Package Dimensions

unit:mm (typ)

4161



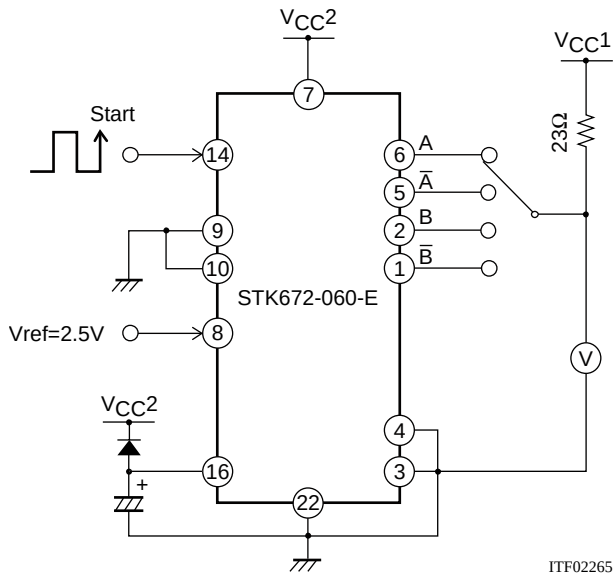
# Internal Block Diagram



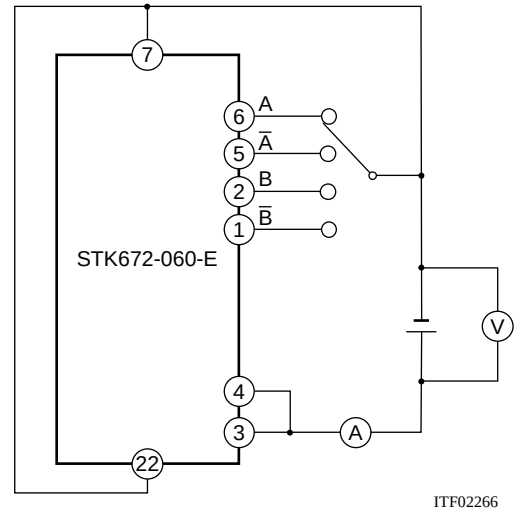
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## Test Circuit Diagrams

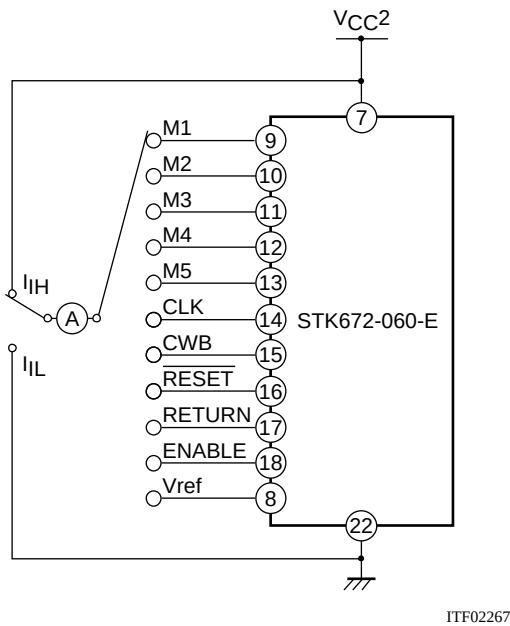
V<sub>sat</sub>



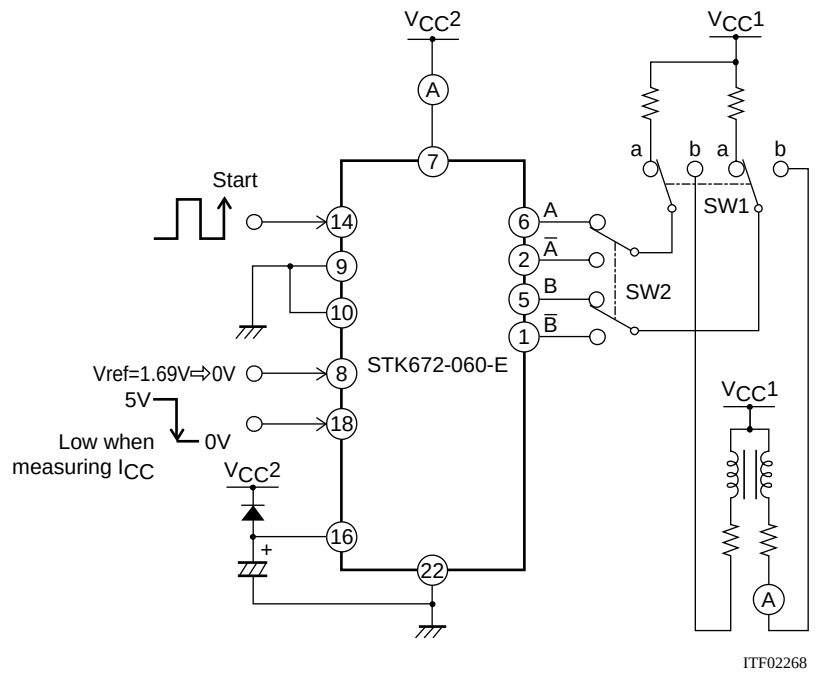
V<sub>df</sub>



I<sub>IH</sub>, I<sub>IL</sub>



I<sub>oave</sub>, I<sub>CC</sub>, f<sub>c</sub>



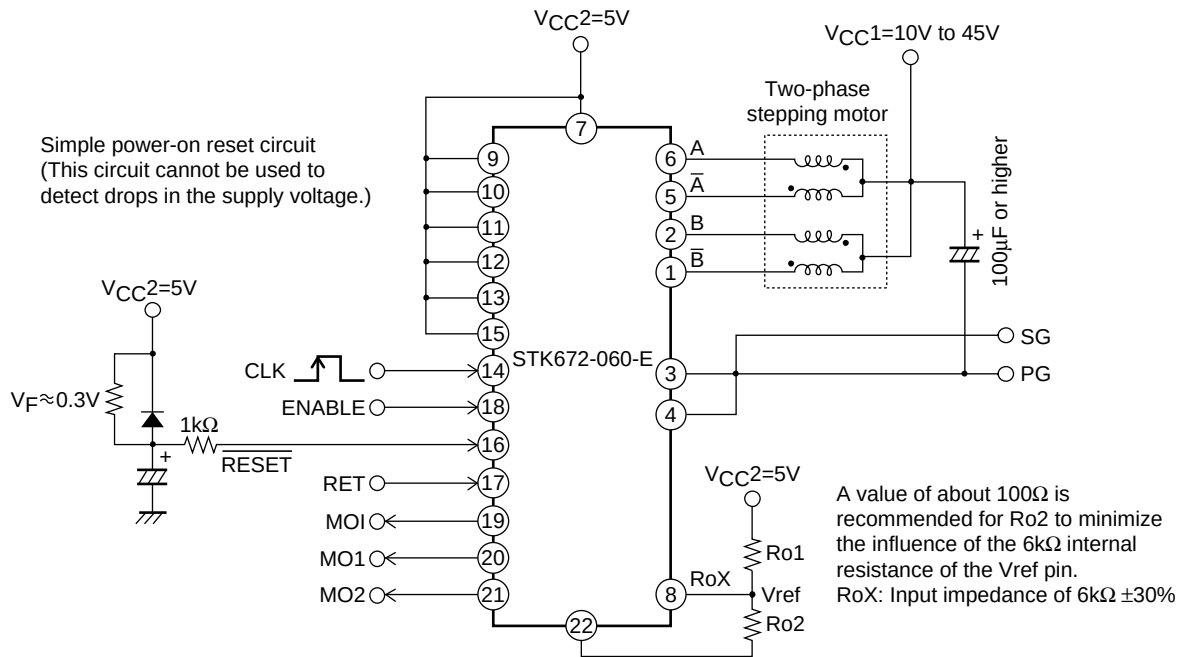
When measuring I<sub>oave</sub>: With SW1 set to 'b', V<sub>ref</sub> = 1.69V

When measuring f<sub>c</sub>: With SW1 set to 'a', V<sub>ref</sub> = 0V

When measuring I<sub>CC</sub>: Set ENABLE low

## Power-on Reset

The application must perform a power-on reset operation when  $V_{CC2}$  power is first applied to this hybrid IC. Application circuit that used 2W1-2 phase excitation (microstepping operation) mode.



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## Setting the Motor Current

The motor current  $I_{OH}$  is set by the Vref voltage on the hybrid IC pin 8. The following formula gives the relationship between  $I_{OH}$  and Vref.

$$R_{oX} = (R_{o2} \times 6k\Omega) \div (R_{o2} + 6k\Omega) \quad (1)$$

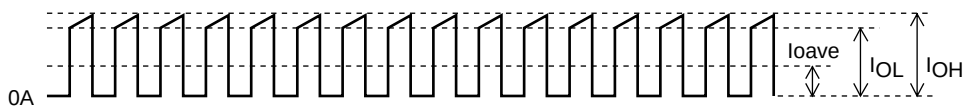
$$V_{ref} = V_{CC2} \times R_{oX} \div (R_{o1} + R_{oX}) \quad (2)$$

$$I_{OH} = \frac{1}{K} \times \frac{V_{ref}}{R_s} \quad (3)$$

K: 7.66 (voltage divider ratio),

$R_s$ : 0.22Ω (This is the hybrid IC's internal current detection resistor. It has a tolerance of  $\pm 3\%$ .)

Applications can use motor currents from the current (0.05 to 0.1A) set by the duty of the frequency set by the oscillator up to the limit of the allowable operating range,  $I_{OH} = 1.2A$



Motor current waveform

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## Function Table

|    |                      |                       |                        |                        |                                   |
|----|----------------------|-----------------------|------------------------|------------------------|-----------------------------------|
| M2 | 0                    | 0                     | 1                      | 1                      | Phase switching clock edge timing |
| M1 | 0                    | 1                     | 0                      | 1                      |                                   |
| M3 |                      |                       |                        |                        |                                   |
| 1  | 2 phase excitation   | 1-2 phase excitation  | W1-2 phase excitation  | 2W1-2 phase excitation | Rising edge only                  |
| 0  | 1-2 phase excitation | W1-2 phase excitation | 2W1-2 phase excitation | 4W1-2 phase excitation | Rising and falling edges          |

|     | Forward | Reverse |
|-----|---------|---------|
| CWB | 0       | 1       |

| ENABLE | Motor current is cut off when low |
|--------|-----------------------------------|
| RESET  | Active low                        |

|     | A | $\bar{A}$ | B | $\bar{B}$ |
|-----|---|-----------|---|-----------|
| MO1 | 1 | 0         | 0 | 1         |
| MO2 | 0 | 0         | 1 | 1         |

## Printed Circuit Board Design Recommendations

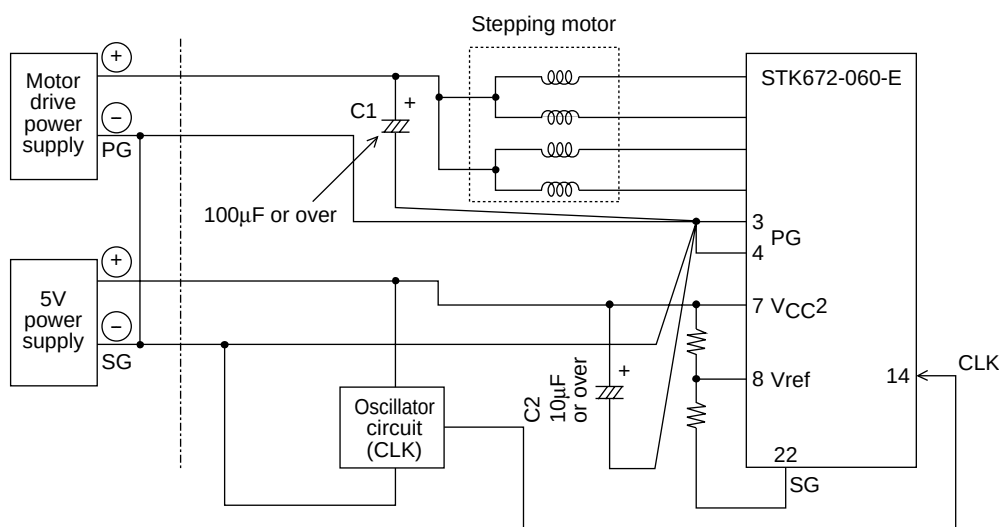
This hybrid IC has two grounds, the PG pins (pins 3 and 4) and the SG pin (pin 22). These are connected internally in the hybrid IC.

Two power supplies are required: a motor drive supply and a 5V supply for the hybrid IC itself. If the ground connections for these supplies are not good, the motor current waveforms may become unstable, motor noise may increase, and vibration levels may increase. Use appropriate wiring for these grounds. Here we present two methods for implementing these ground connections.

If the grounds for the motor drive supply and the hybrid IC 5V supply are connected in the immediate vicinity of the power supplies:

- If PG and SG are shorted at the power supply, connect only the PG line to pins 3 and 4 on the hybrid IC. Also, be sure that no problems occur due to voltage drops due to common impedances. In the specifications, this must be  $V_{CC2} \pm 5\%$ .
- The current waveforms will be more stable if the Vref ground is connected to pin 22.
- For initial values, use  $100\mu\text{F}$  or over for C1 and  $10\mu\text{F}$  or over for C2.

Locate C1 as close to the hybrid IC as possible, and the capacitor ground line must be as short as possible.

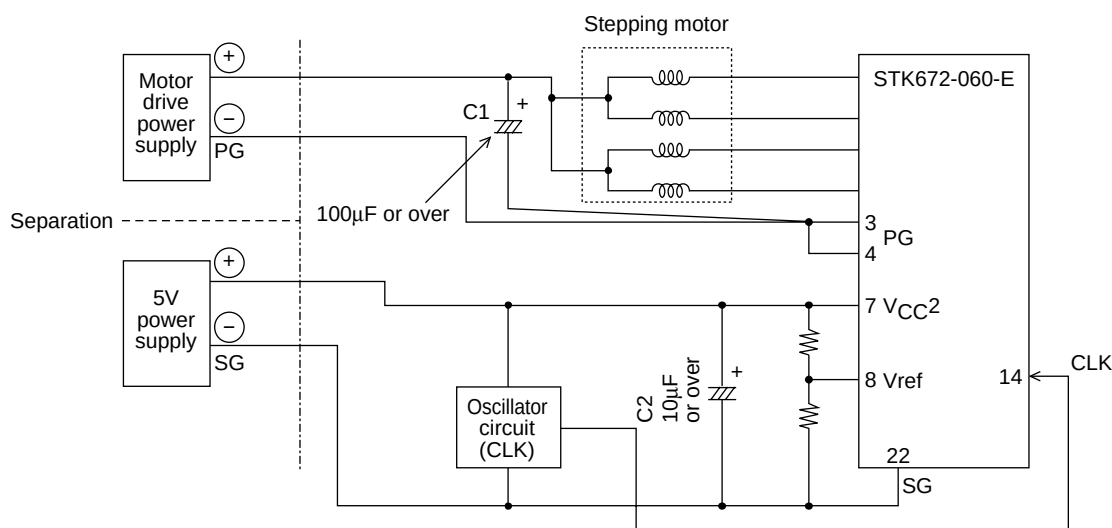


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If the grounds for the motor drive supply and the hybrid IC 5V supply are separated:

- Insert a capacitor (C1) of  $100\mu\text{F}$  or over as close as possible to the hybrid IC. The capacitor ground line must be as short as possible.

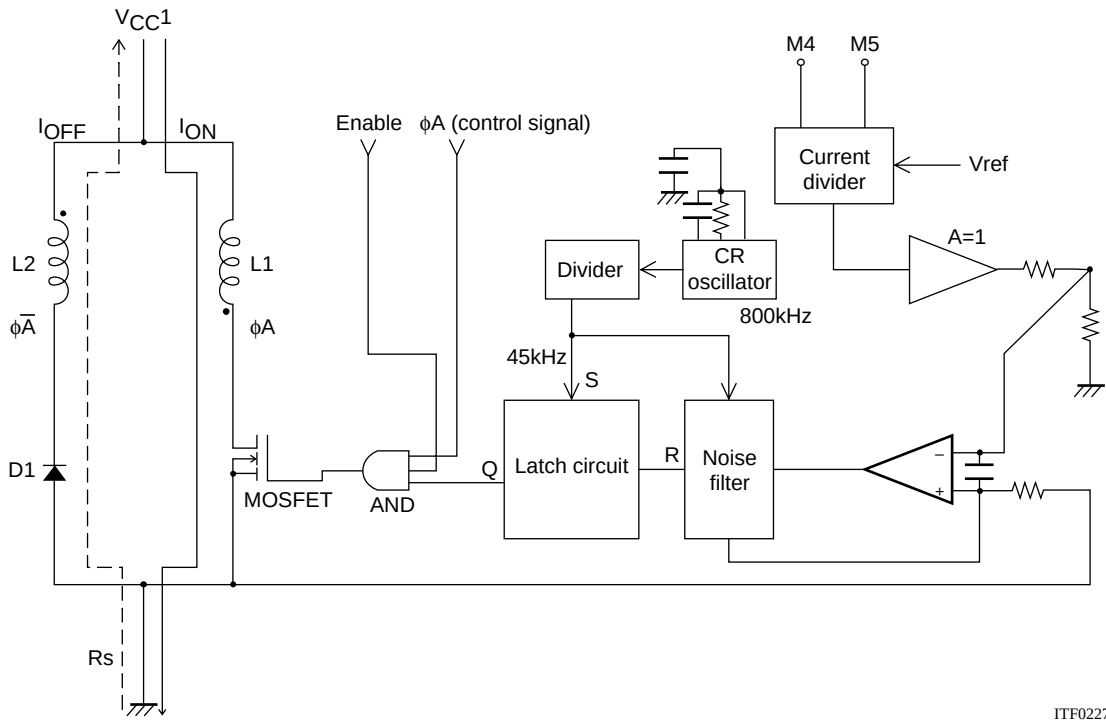
The capacitor C2 may be included if necessary. Its ground line should also be as short as possible.



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## Functional Description

### External Excitation Chopper Drive Block Description



Driver Block Basic Circuit Structure

Since this hybrid IC adopts an external excitation method, no external oscillator circuit is required.

When a high level is input to  $\phi A$  in the basic driver block circuit shown in the figure and the MOSFET is turned on, the comparator + input will go low and the comparator output will go low. Since a set signal with the PWM period will be input, the Q output will go high, and the MOSFET will be turned on as its initial value.

The current  $I_{ON}$  flowing in the MOSFET passes through L1 and generates a potential difference in  $R_s$ . Then, when the  $R_s$  potential and the  $V_{ref}$  potential become the same, the comparator output will invert, and the reset signal Q output will invert to the low level. Then, the MOSFET will be turned off and the energy stored in L1 will be induced in L2 and the current  $I_{OFF}$  will be regenerated to the power supply. This state will be maintained until the time when an input to the latch circuit set pin occurs.

In this manner, the Q output is turned off and on repeatedly by the reset and set signals, thus implementing constant current control. The resistor and capacitor on the comparator input are spike removal circuit elements and synchronize with the PWM frequency. Since this hybrid IC uses a fixed frequency due to the external excitation method and at the same time also adopts a synchronized PWM technique, it can suppress the noise associated with holding a position when the motor is locked.

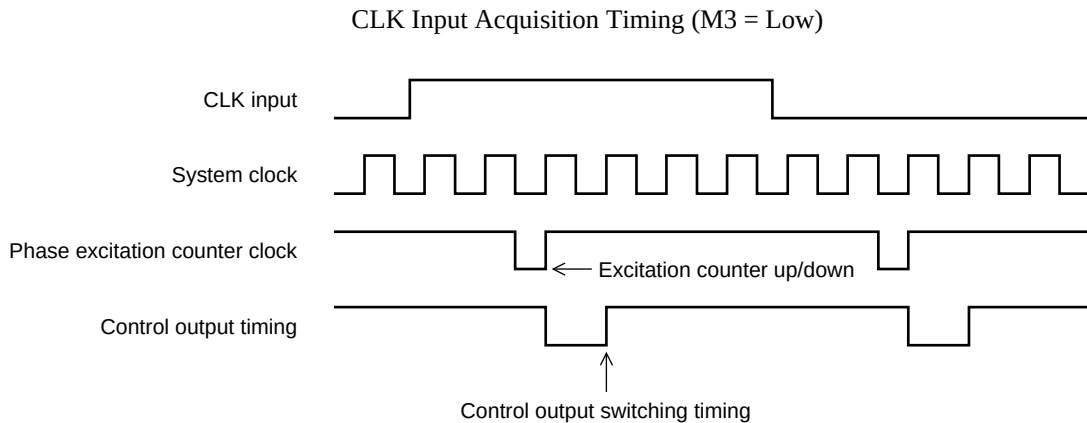
### Input Pin Functions

| Pin No.   | Symbol     | Function                            | Pin circuit type                                     |
|-----------|------------|-------------------------------------|------------------------------------------------------|
| 14        | CLK        | Phase switching clock               | Built-in pull-up resistor CMOS Schmitt trigger input |
| 15        | CWB        | Rotation direction setting (CW/CCW) | Built-in pull-up resistor CMOS Schmitt trigger input |
| 17        | RETURN     | Forced phase origin return          | Built-in pull-up resistor CMOS Schmitt trigger input |
| 18        | ENABLE     | Output cutoff                       | Built-in pull-up resistor CMOS Schmitt trigger input |
| 9, 10, 11 | M1, M2, M3 | Excitation mode setting             | Built-in pull-up resistor CMOS Schmitt trigger input |
| 12, 13    | M4, M5     | Vector locus setting                | Built-in pull-up resistor CMOS Schmitt trigger input |
| 16        | RESET      | System reset                        | Built-in pull-up resistor CMOS Schmitt trigger input |
| 8         | Vref       | Current setting                     | Operational amplifier input                          |



## Input Signal Functions and Timing

- CLK (phase switching clock)
  - 1) Input frequency range: DC to 50kHz
  - 2) Minimum pulse width: 10μs
  - 3) Duty: 40 to 60% (However, the minimum pulse width takes precedence when M3 is high.)
  - 4) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
  - 5) Built-in multi-stage noise rejection circuit
  - 6) Function:
    - When M3 is high or open: The phase excited (driven) is advanced one step on each CLK rising edge.
    - When M3 is low: The phase is advanced one step by both rising and falling edges, for a total of two steps per cycle.



- CWB (Method for setting the rotation direction)
  - 1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
  - 2) Function:
    - When CWB is low: The motor turns in the clockwise direction.
    - When CWB is high: The motor turns in the counterclockwise direction.
  - 3) Notes: When M3 is low, the CWB input must not be changed for about 6.25μs before or after a rising or falling edge on the CLK input.
- RETURN (Forcible return to the origin for the currently excited phase)
  - 1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
  - 2) Built-in noise rejection circuit
  - 3) Notes: The currently excited (driven) phase can be forcibly moved to the origin by switching this input from low to high. Normally, if this input is unused, it must be left open or connected to V<sub>CC2</sub>.
- ENABLE (Controls the on/off state of the A,  $\bar{A}$ , B, and  $\bar{B}$  excitation drive outputs and selects either operating or hold as the internal state of this hybrid IC.)
  - 1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
  - 2) Function:
    - When ENABLE is high or open: Normal operating state
    - When ENABLE is low: This hybrid IC goes to the hold state and excitation drive output (motor current) is forcibly turned off. In this mode, the hybrid IC system clock is stopped and no inputs other than the reset input have any effect on the hybrid IC state.

• M1, M2, and M3 (Excitation mode and CLK input edge timing selection)

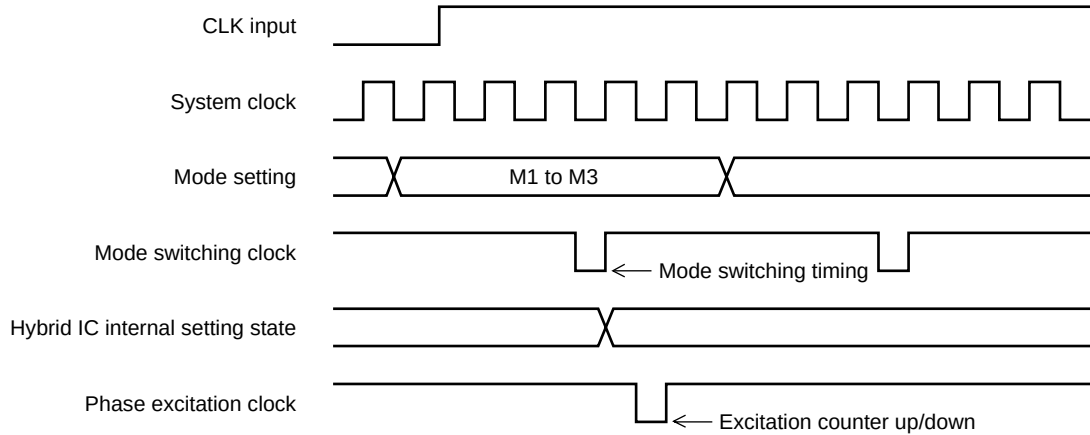
1) Pin circuit type: Built-in pull-up resistor (20k $\Omega$ , typical) CMOS Schmitt trigger structure

2) Function:

|    |                      |                       |                        |                        |                                   |
|----|----------------------|-----------------------|------------------------|------------------------|-----------------------------------|
| M2 | 0                    | 0                     | 1                      | 1                      | Phase switching clock edge timing |
| M1 | 0                    | 1                     | 0                      | 1                      |                                   |
| M3 |                      |                       |                        |                        |                                   |
| 1  | 2 phase excitation   | 1-2 phase excitation  | W1-2 phase excitation  | 2W1-2 phase excitation | Rising edge only                  |
| 0  | 1-2 phase excitation | W1-2 phase excitation | 2W1-2 phase excitation | 4W1-2 phase excitation | Rising and falling edges          |

3) Valid mode setting timing: Applications must not change the mode in the period 5 $\mu$ s before or after a CLK signal rising or falling edge.

Mode Setting Acquisition Timing

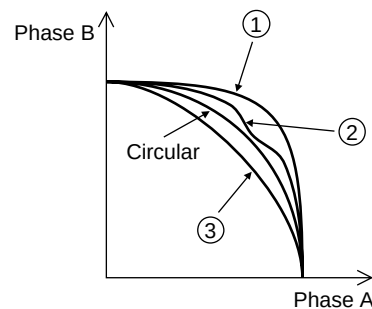


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• M4 and M5 (Microstepping mode rotation vector locus setting)

|      |          |   |   |   |
|------|----------|---|---|---|
| M4   | 1        | 0 | 1 | 0 |
| M5   | 1        | 0 | 0 | 1 |
| Mode | Circular | ① | ② | ③ |

See page 11 for details on the current division ratio.



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• RESET (Resets all parts of the system.)

1) Pin circuit type: Built-in pull-up resistor (20k $\Omega$ , typical) CMOS Schmitt trigger structure

2) Function:

- All circuit states are set to their initial values by setting the RESET pin low. (Note that the pulse width must be at least 10 $\mu$ s.)

At this time, the A and B phases are set to their origin, regardless of the excitation mode. The output current goes to about 71% after the reset is released.

3) Notes: When power is first applied to this hybrid IC, Vref must be established by applying a reset. Applications must apply a power on reset when the VCC2 power supply is first applied.

• Vref (Sets the current level used as the reference for constant-current detection.)

1) Pin circuit type: Analog input structure

2) Function:

- Constant-current control can be applied to the motor excitation current at 100% of the rated current by applying a voltage less than the control system power supply voltage VCC2 minus 2.5V.
- Applications can apply constant-current control proportional to the Vref voltage, with this value of 2.5V as the upper limit.

## Output Pin Functions

| Pin No. | Symbol   | Function                        | Pin circuit type        |
|---------|----------|---------------------------------|-------------------------|
| 19      | MOI      | Phase excitation origin monitor | Standard CMOS structure |
| 20, 21  | MO1, MO2 | Phase excitation state monitor  | Standard CMOS structure |

## Output Signal Functions and Timing

- A,  $\bar{A}$ , B, and  $\bar{B}$  (Motor phase excitation outputs)

1) Function:

- In the 4 phase and 2 phase excitation modes, a 3.75 $\mu$ s (typical) interval is set up between the A and  $\bar{A}$  and B and  $\bar{B}$  output signal transition times.

- MO1, MO2, and MOI (Phase excitation state monitors)

1) Pin circuit type: Standard CMOS structure

1) Function:

- Output of the current phase excitation output state.

| Phase coordinate | Phase A | Phase B | Phase $\bar{A}$ | Phase $\bar{B}$ |
|------------------|---------|---------|-----------------|-----------------|
| MO1              | 1       | 0       | 0               | 1               |
| MO2              | 0       | 1       | 0               | 1               |

MOI outputs a 0 when each phase is at the origin, and outputs a 1 otherwise.

- Current division ratios set by M3, M4, and M5 ..... Values provided for reference purposes.

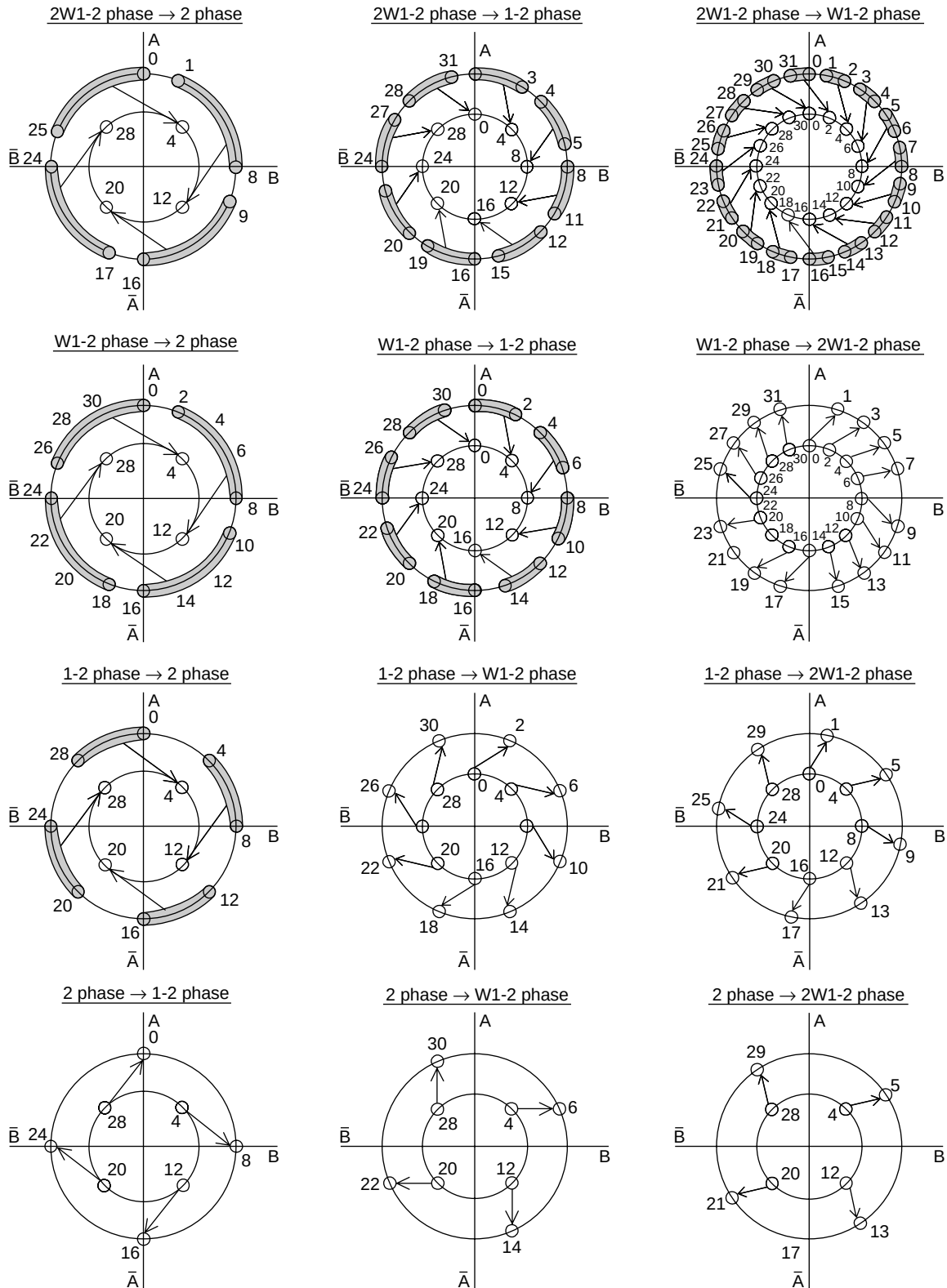
| Mode                   |        |        | Circular | ①      | ②      | ③      | Units | Number of steps |       |
|------------------------|--------|--------|----------|--------|--------|--------|-------|-----------------|-------|
| Setting                | M3 = 0 | M3 = 1 | M4 = 1   | M4 = 0 | M4 = 1 | M4 = 1 |       |                 |       |
|                        |        |        | M5 = 1   | M5 = 0 | M5 = 0 | M5 = 1 |       |                 |       |
| Current division ratio | 4W1-2  |        | 15       | 16     | 16     | 15     | %     |                 | 1/16  |
|                        |        | 2W1-2  | 21       | 25     | 24     | 20     |       | 1/8             | 2/16  |
|                        |        |        | 31       | 34     | 33     | 28     |       |                 | 3/16  |
|                        |        | 2W1-2  | 40       | 44     | 41     | 38     |       | 2/8             | 4/16  |
|                        |        |        | 47       | 50     | 49     | 44     |       |                 | 5/16  |
|                        |        | 2W1-2  | 55       | 59     | 56     | 53     |       | 3/8             | 6/16  |
|                        |        |        | 63       | 67     | 63     | 60     |       |                 | 7/16  |
|                        |        | 2W1-2  | 71       | 75     | 70     | 67     |       | 4/8             | 8/16  |
|                        |        |        | 76       | 81     | 76     | 73     |       |                 | 9/16  |
|                        |        | 2W1-2  | 83       | 87     | 84     | 81     |       | 5/8             | 10/16 |
|                        |        |        | 87       | 92     | 88     | 84     |       |                 | 11/16 |
|                        |        | 2W1-2  | 92       | 95     | 95     | 91     |       | 6/8             | 12/16 |
|                        |        |        | 96       | 98     | 98     | 93     |       |                 | 13/16 |
|                        |        | 2W1-2  | 100      | 100    | 100    | 100    |       | 7/8             | 14/16 |

[Load conditions]

$V_{CC1} = 24V$ ,  $V_{CC2} = 5V$ ,  $R/L = 3.5/3.8mH$

## Phase States During Excitation Switching

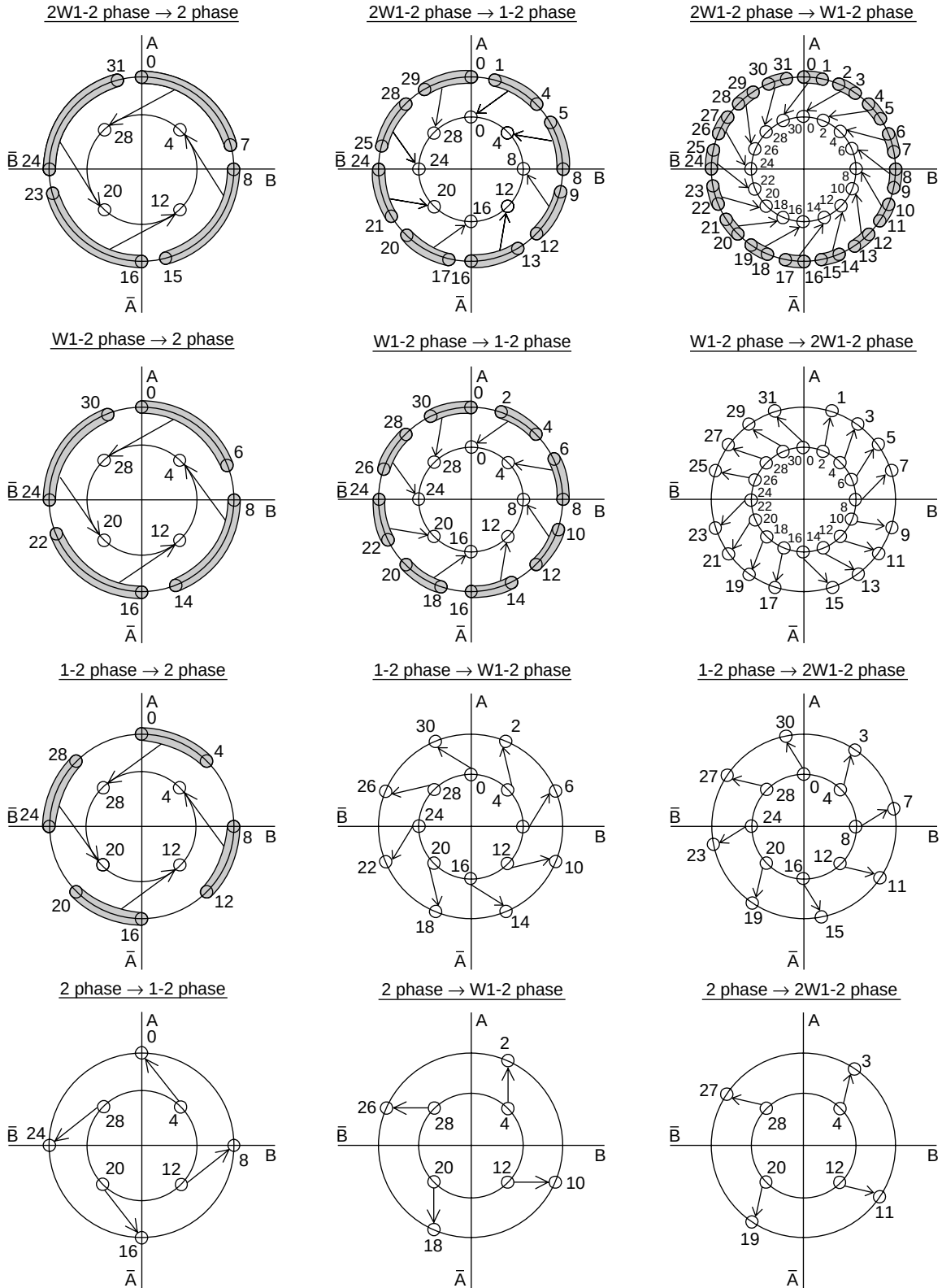
- Excitation phases before and after excitation mode switching <clockwise direction>



Excitation phase developed by the first CLK internal pulse after the change in the excitation mode setting with M1 and M  
 Excitation phase immediately prior to the excitation mode setting

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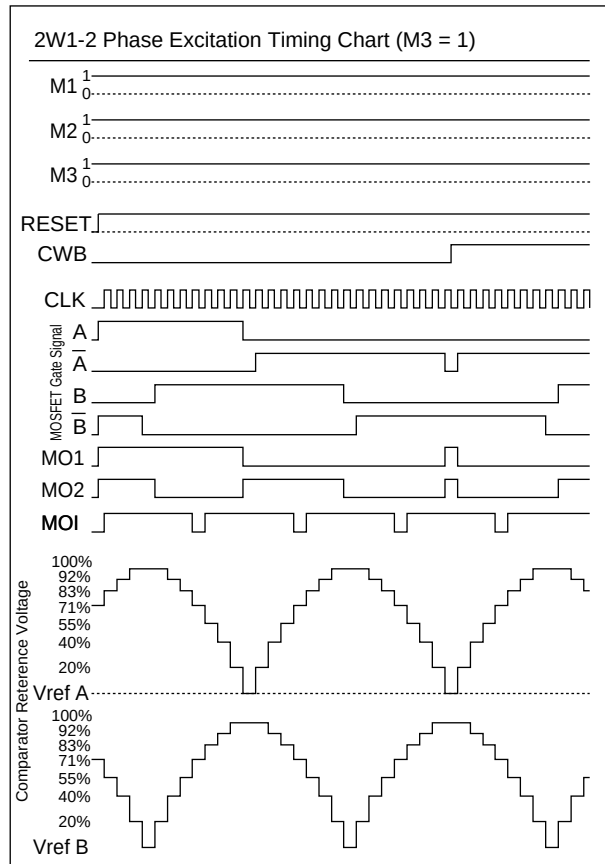
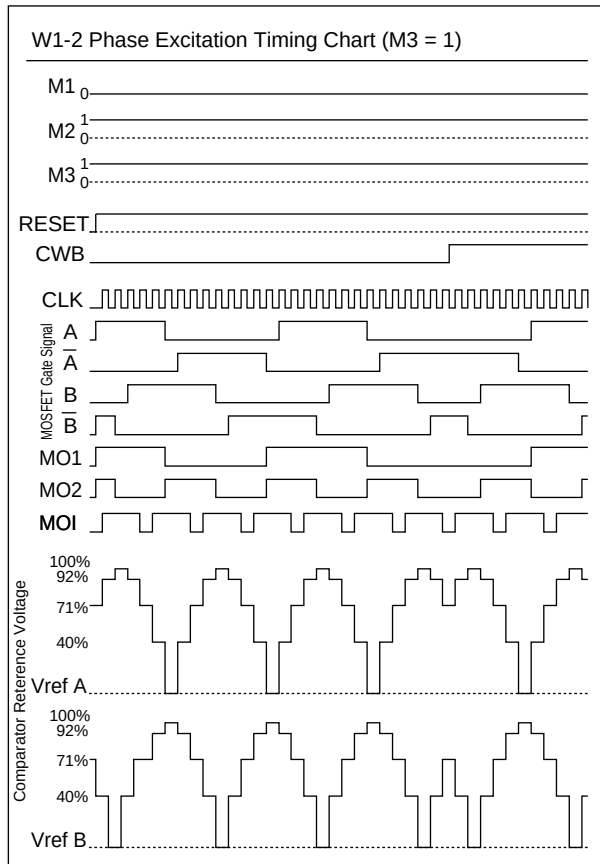
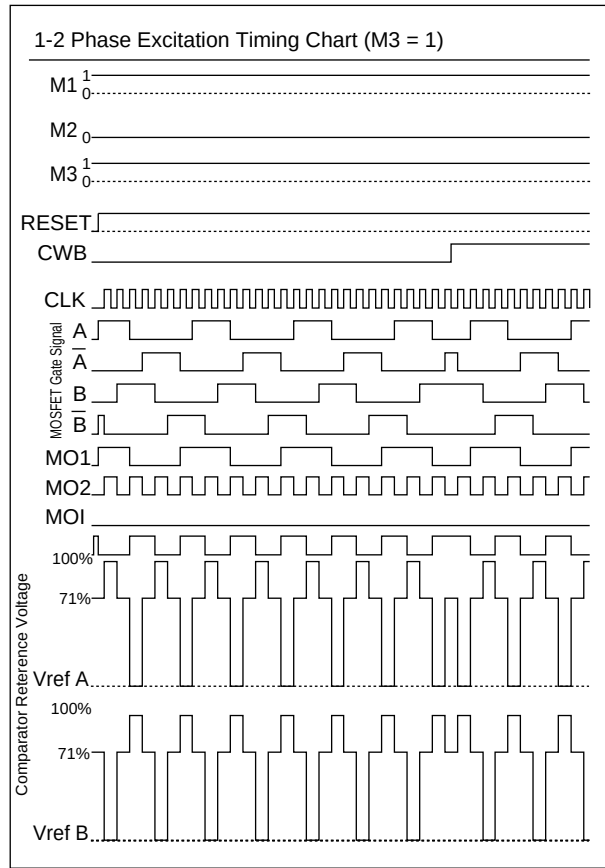
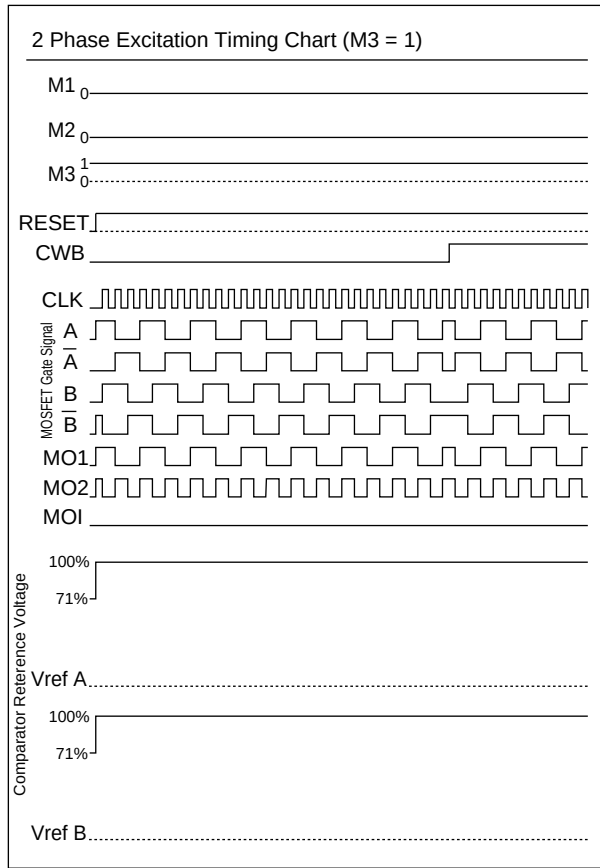
- Excitation phases before and after excitation mode switching <counterclockwise direction>



A13267

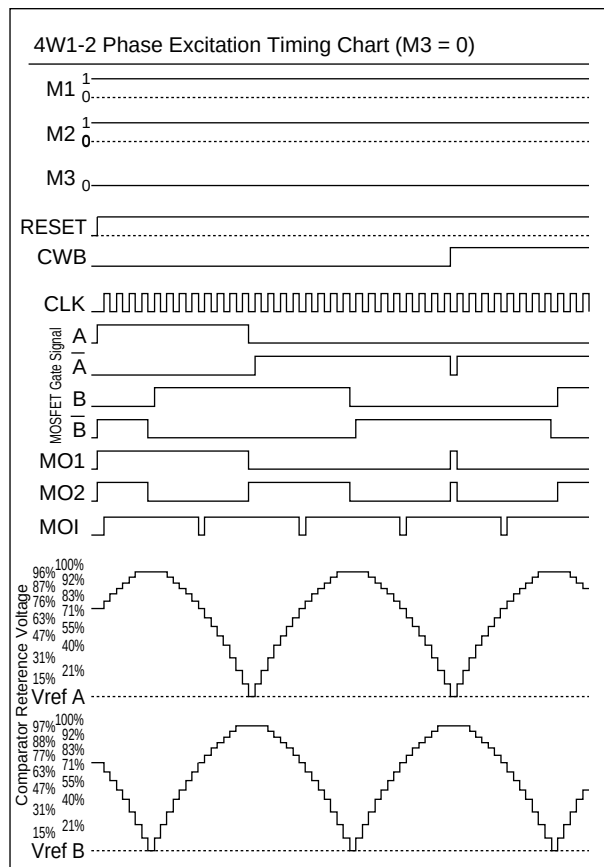
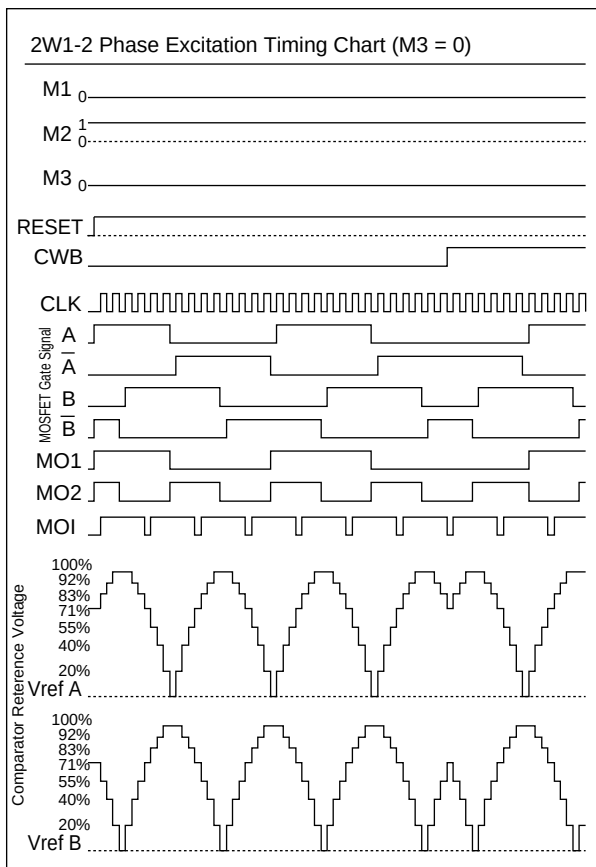
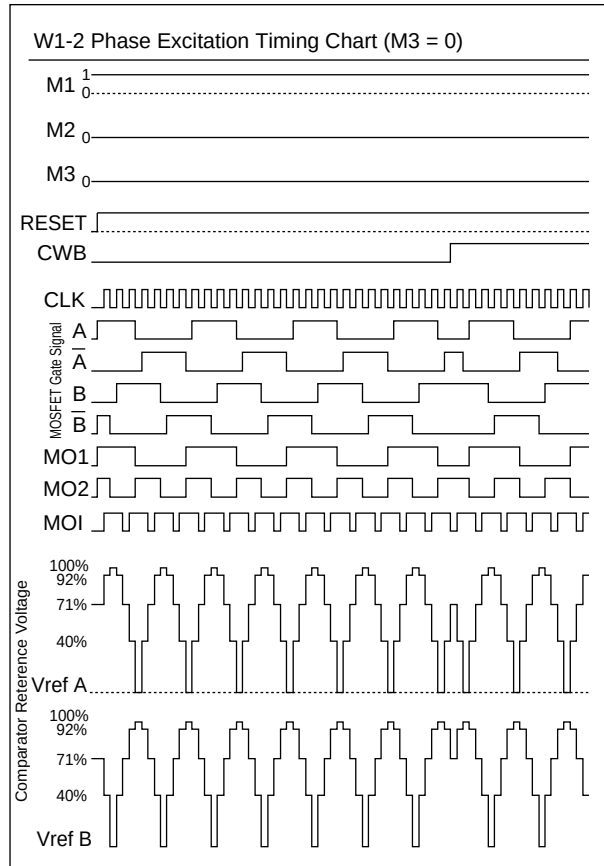
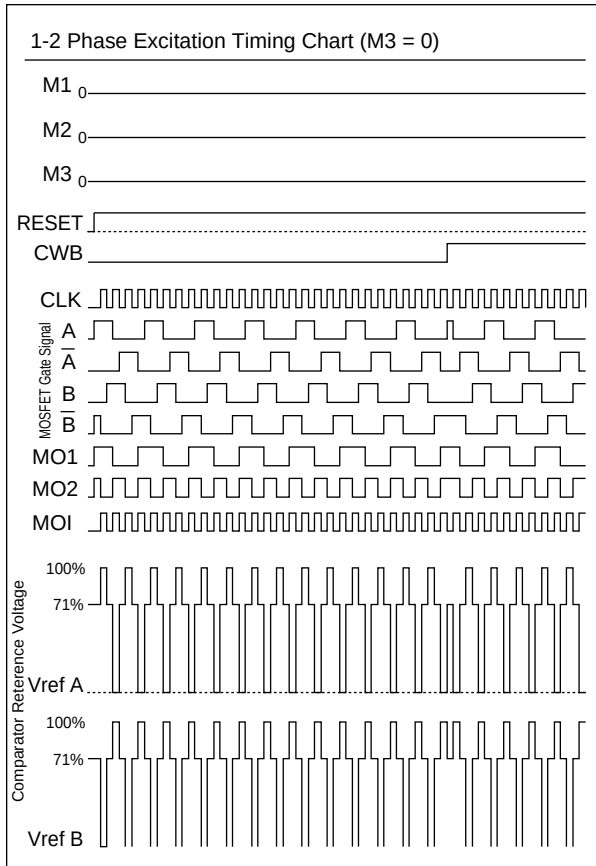
## Excitation Time and Timing Charts

- CLK rising edge operation



ITF02274

• CLK rising and falling edge operation



ITF02275

## Thermal Design

<Hybrid IC Average Internal Power Loss Pd>

The main elements internal to this hybrid IC with large average power losses are the current control devices, the regenerative current diodes, and the current detection resistor. Since sine wave drive is used, the average power loss during microstepping drive can be approximated by applying a waveform factor of 0.64 to the square wave loss during 2 phase excitation.

The losses in the various excitation modes are as follows.

$$\text{2 phase excitation} \quad Pd_{2EX} = (V_{sat} + V_{df}) \cdot \frac{f_{clock}}{2} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{2} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3)$$

$$\text{1-2 phase excitation} \quad Pd_{1-2EX} = 0.64 \cdot \left\{ (V_{sat} + V_{df}) \cdot \frac{f_{clock}}{4} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{4} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3) \right\}$$

$$\text{W1-2 phase excitation} \quad Pd_{W1-2EX} = 0.64 \cdot \left\{ (V_{sat} + V_{df}) \cdot \frac{f_{clock}}{8} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{8} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3) \right\}$$

$$\text{2W1-2 phase excitation} \quad Pd_{2W1-2EX} = 0.64 \cdot \left\{ (V_{sat} + V_{df}) \cdot \frac{f_{clock}}{16} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{16} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3) \right\}$$

$$\text{4W1-2 phase excitation} \quad Pd_{4W1-2EX} = 0.64 \cdot \left\{ (V_{sat} + V_{df}) \cdot \frac{f_{clock}}{16} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{16} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3) \right\}$$

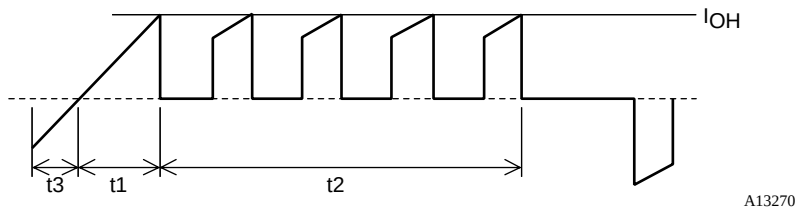
Here, t1 and t3 can be determined from the same formulas for all excitation methods.

$$t_1 = \frac{-L}{R + 0.7} \cdot \ln \left( 1 - \frac{R + 0.7}{V_{CC1}} \cdot I_{OH} \right) \quad t_3 = \frac{-L}{R} \cdot \ln \left( \frac{V_{CC1} + 0.7}{I_{OH} \cdot R + V_{CC1} + 0.7} \right)$$

However, the formula for t2 differs with the excitation method.

$$\text{2 phase excitation} \quad t_2 = \frac{2}{f_{clock}} - (t_1 + t_3) \quad \text{1-2 phase excitation} \quad t_2 = \frac{3}{f_{clock}} - t_1$$

$$\text{W1-2 phase excitation} \quad t_2 = \frac{7}{f_{clock}} - t_1 \quad \begin{matrix} \text{2W1-2 phase excitation} \\ \text{4W1-2 phase excitation} \end{matrix} \quad t_2 = \frac{15}{f_{clock}} - t_1$$



Motor Phase Current Model Figure (2 Phase Excitation)

f<sub>clock</sub> : CLK input frequency (Hz)

V<sub>sat</sub> : The voltage drop of the power MOSFET and the current detection resistor (V)

V<sub>df</sub> : The voltage drop of the body diode and the current detection resistor (V)

I<sub>OH</sub> : Phase current peak value (A)

t<sub>1</sub> : Phase current rise time (s)

t<sub>2</sub> : Constant-current operating time (s)

t<sub>3</sub> : Phase switching current regeneration time (s)

V<sub>CC1</sub> : Supply voltage applied to the motor (V)

L : Motor inductance (H)

R : Motor winding resistance (Ω)



<Determining the Size of the Hybrid IC Heat Sink>

Determine  $\theta_{c-a}$  for the heat sink from the average power loss determined in the previous item.

$$\theta_{c-a} = \frac{T_{c \max} - T_a}{P_{dEX}} \quad [^{\circ}\text{C/W}]$$

$T_{c \max}$ : Hybrid IC substrate temperature ( $^{\circ}\text{C}$ )

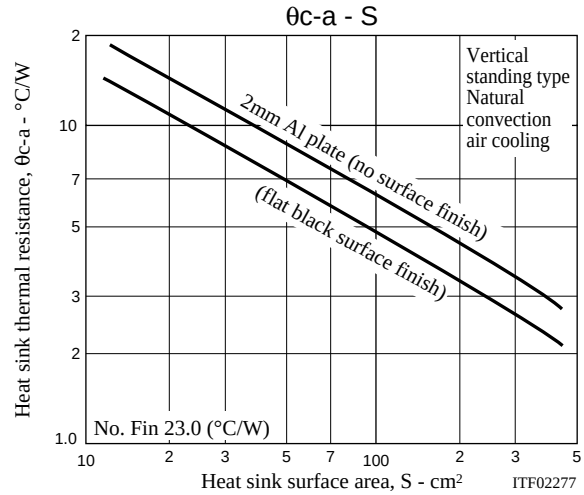
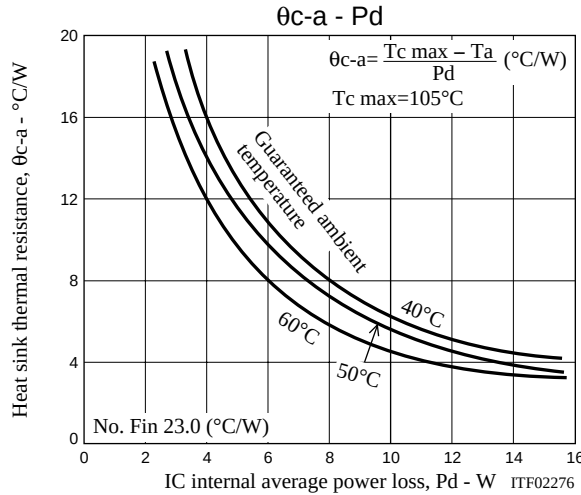
$T_a$ : Application internal temperature ( $^{\circ}\text{C}$ )

$P_{dEX}$ : Hybrid IC internal average loss (W)

Determine  $\theta_{c-a}$  from the above formula and then size S (in  $\text{cm}^2$ ) of the heat sink from the graphs shown below.

The ambient temperature of the device will vary greatly according to the air flow conditions within the application.

Therefore, always verify that the size of the heat sink is adequate to assure that the Hybrid IC back surface (the aluminum plate side) will never exceed a  $T_{c \max}$  of  $105^{\circ}\text{C}$ , whatever the operating conditions are.



Next we determine the usage conditions with no heat sink by determining the allowable hybrid IC internal average loss from the thermal resistance of the hybrid IC substrate, namely  $23^{\circ}\text{C/W}$ .

For a  $T_{c \max}$  of  $105^{\circ}\text{C}$  at an ambient temperature of  $50^{\circ}\text{C}$

$$P_{dEX} = \frac{105 - 50}{23} = 2.3\text{W}$$

For a  $T_{c \max}$  of  $105^{\circ}\text{C}$  at an ambient temperature of  $40^{\circ}\text{C}$

$$P_{dEX} = \frac{105 - 40}{23} = 2.8\text{W}$$

This hybrid IC can be used with no heat sink as long as it is used at operating conditions below the losses listed above. (See  $\Delta T_c - P_d$  curve in the graph on page 19.)

<Hybrid IC internal power element (MOSFET) junction temperature calculation>

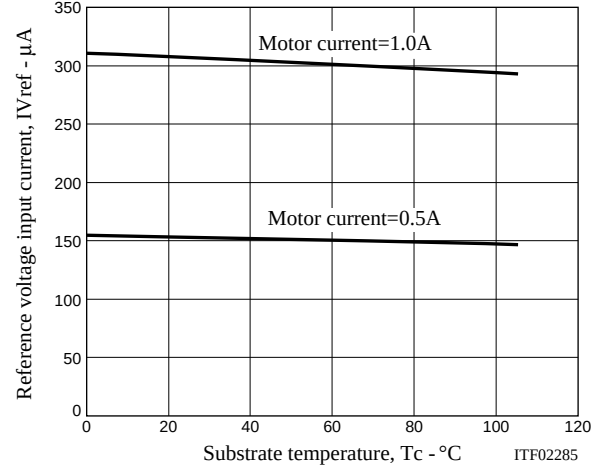
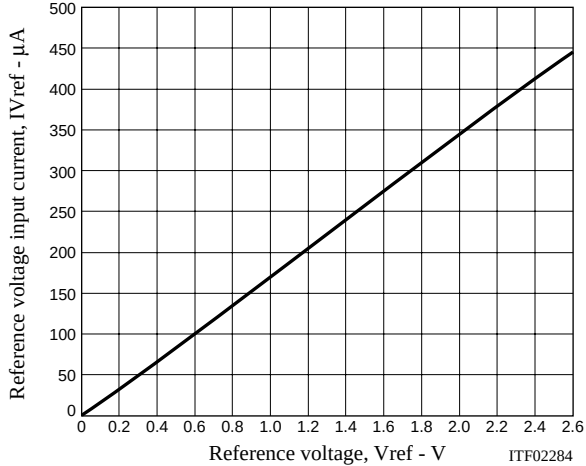
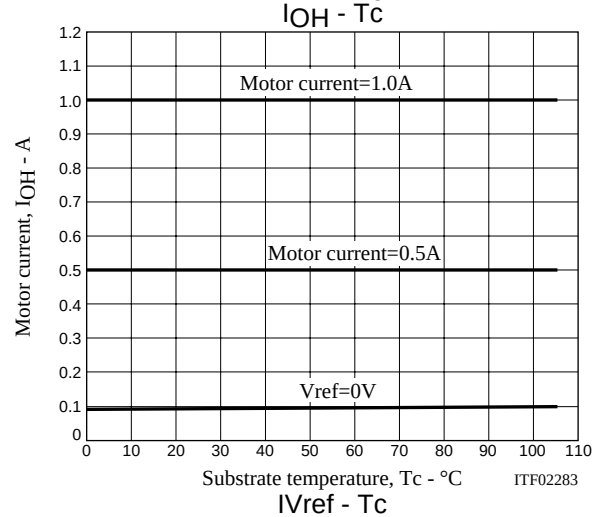
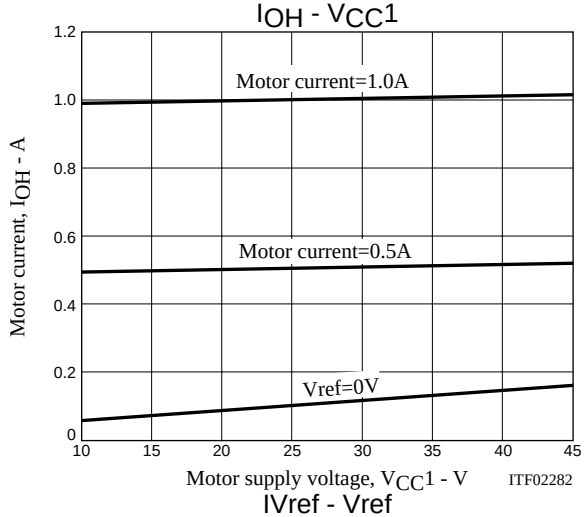
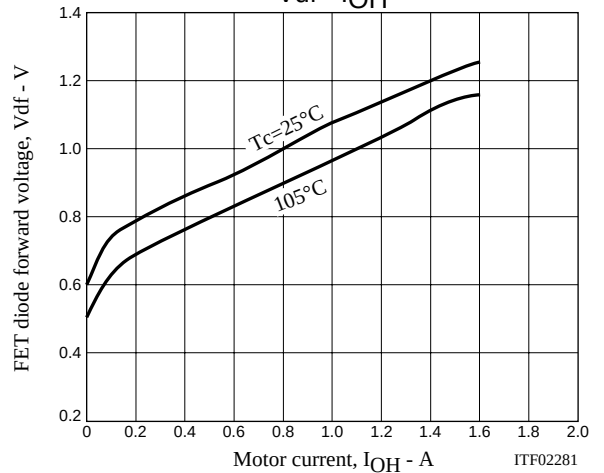
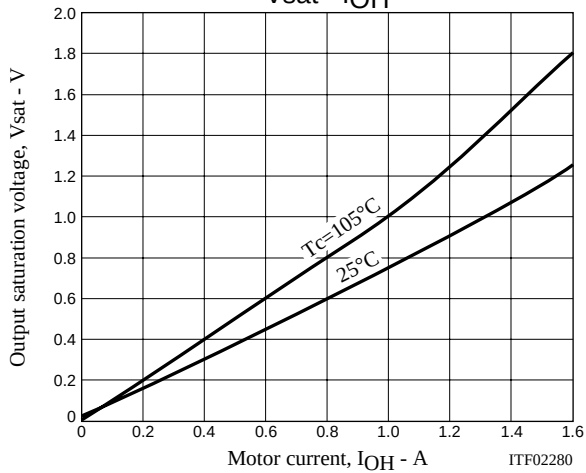
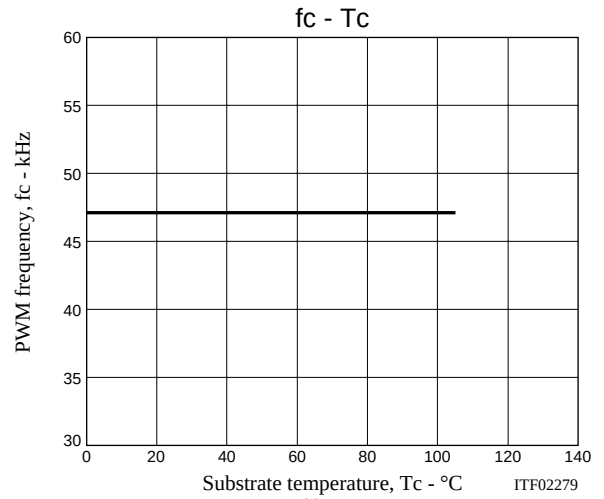
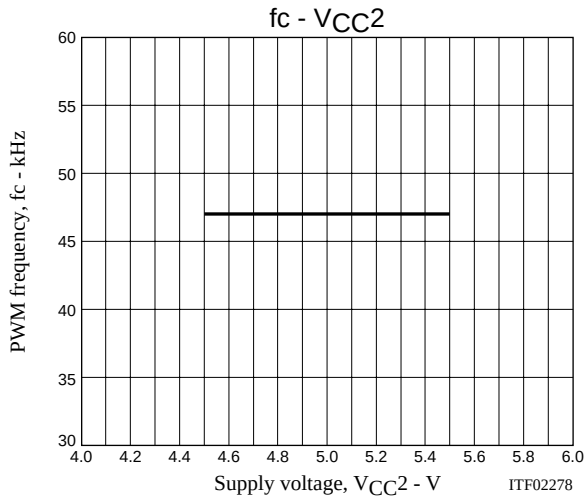
The junction temperature,  $T_j$ , of each device can be determined from the loss  $P_{ds}$  in each transistor and the thermal resistance  $\theta_{j-c}$ .

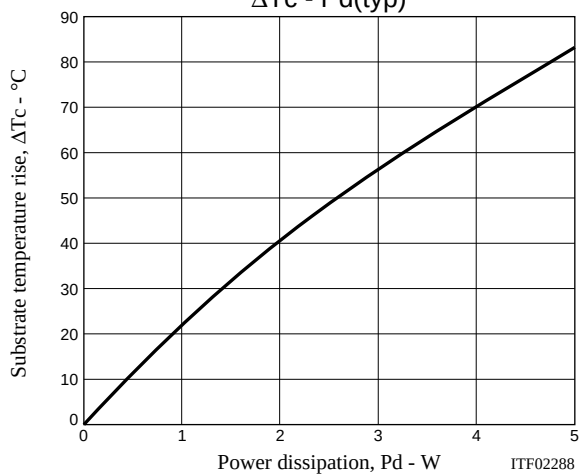
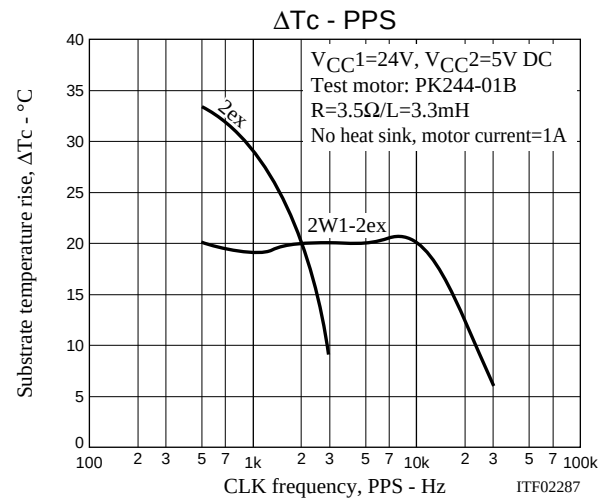
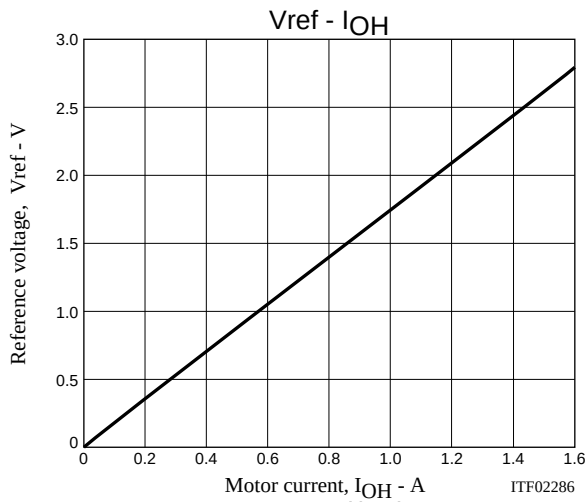
$$T_j = T_c + \theta_{j-c} \times P_{ds} \quad (^{\circ}\text{C})$$

Here, we determine  $P_{ds}$ , the loss for each transistor, by determining  $P_{dEX}$  in each excitation mode.

$$P_{ds} = P_{dEX}/4$$

The steady-state thermal resistance  $\theta_{j-c}$  of a power MOSFET is  $18^{\circ}\text{C/W}$ .





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