



16-Bit, Quad Voltage Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER: 200mW**
- **UNIPOLAR OR BIPOLAR OPERATION**
- **SINGLE SUPPLY OUTPUT RANGE: +10V**
- **DUAL SUPPLY OUTPUT RANGE: $\pm 10V$**
- **SETTLING TIME: $10\mu s$ to 0.003%**
- **16-BIT MONOTONICITY: $-40^{\circ}C$ to $+85^{\circ}C$**
- **PROGRAMMABLE RESET TO MID-SCALE
OR ZERO-SCALE**
- **DOUBLE-BUFFERED DATA INPUTS**
- **± 1 LSB DNL: $-40^{\circ}C$ to $+85^{\circ}C$**

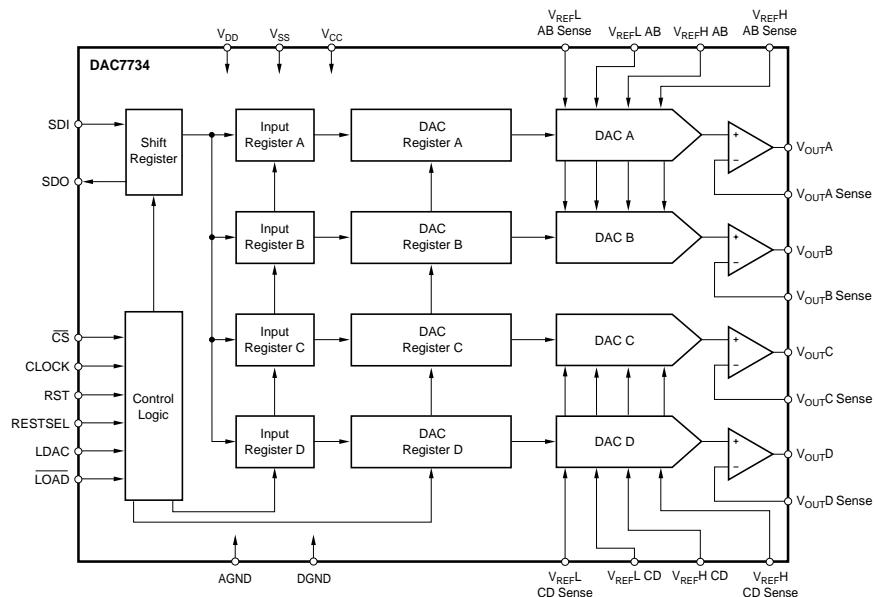
APPLICATIONS

- **PROCESS CONTROL**
- **ATE PIN ELECTRONICS**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

DESCRIPTION

The DAC7734 is a 16-bit, quad voltage output, digital-to-analog converter (DAC) with ensured 16-bit monotonic performance over the specified temperature range. It accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a serial data output for daisy-chaining multiple DACs. Programmable asynchronous reset clears all registers to a mid-scale code of 8000h or to a zero-scale of 0000h. The DAC7734 can operate from a single +15V supply or from +15V and $-15V$, and +5V supplies.

Low power and small size per DAC make the DAC7734 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7734 is available in a 48-lead SSOP package and offers ensured specifications over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

SPECIFICATIONS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7734E			DAC7734EB			DAC7734EC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY											
Linearity Error (INL) T_{MIN} to T_{MAX}	$T = 25^\circ C$			± 3 ± 4			*			± 2	LSB
Linearity Match T_{MIN} to T_{MAX}	$T = 25^\circ C$		± 4	± 3 ± 3		*	± 2 ± 2			± 3	LSB
Differential Linearity Error (DNL) T_{MIN} to T_{MAX}	$T = 25^\circ C$	14	± 0.01	± 0.025 ± 0.05 ± 0.025 ± 0.05 ± 0.024	15		*			± 1 ± 1	LSB
Monotonicity, T_{MIN} to T_{MAX}											Bits
Bipolar Zero Error	$T = 25^\circ C$						*			*	% of FSR
Bipolar Zero Error, T_{MIN} to T_{MAX}							*			*	% of FSR
Full-Scale Error	$T = 25^\circ C$						*			*	% of FSR
Full-Scale Error, T_{MIN} to T_{MAX}	Channel-to-Channel Matching			± 0.024			*			*	% of FSR
Bipolar Zero Matching	Channel-to-Channel Matching						*			*	% of FSR
Full-Scale Matching	At Full Scale			25			*			*	% of FSR
Power Supply Rejection Ratio (PSRR)							*			*	ppm/V
ANALOG OUTPUT											
Voltage Output										*	V
Output Current										*	mA
Maximum Load Capacitance										*	pF
Short-Circuit Current										*	mA
Short-Circuit Duration	To V_{SS} , V_{CC} or GND		V_{REFL} ± 5	500 ± 20 Indefinite	V_{REFH}	*	*	*	*	*	V
REFERENCE INPUT											
Ref High Input Voltage Range			$V_{REFL} + 1.25$		$+10$					*	V
Ref Low Input Voltage Range			-10		$V_{REFH} - 1.25$					*	V
Ref High Input Current			-0.3		2.6					*	mA
Ref Low Input Current			-3.2		-0.3					*	mA
DYNAMIC PERFORMANCE											
Settling Time	To $\pm 0.003\%$, 20V Output Step		9	11		*	*			*	μs
Channel-to-Channel Crosstalk	See Figure 5		0.5			*	*			*	LSB
Digital Feedthrough			2			*	*			*	$nV \cdot s$
Output Noise Voltage	$f = 10\text{kHz}$		60			*	*			*	nV/\sqrt{Hz}
DIGITAL INPUT											
V_{IH}			$0.7 \cdot V_{DD}$								V
V_{IL}			0								V
I_{IH}					V_{DD}						μA
I_{IL}					$0.3 \cdot V_{DD}$						μA
± 10					± 10						
± 10					± 10						
DIGITAL OUTPUT											
V_{OH}	$I_{OH} = -0.8\text{mA}$	3.6	4.5	0.4	*	*	*			*	V
V_{OL}	$I_{OL} = 1.6\text{mA}$	0.3			*	*	*			*	V
POWER SUPPLY											
V_{DD}			$+4.75$	$+5.0$	$+5.25$	*	*	*	*	*	V
V_{CC}			$+14.25$	$+15.0$	$+15.75$	*	*	*	*	*	V
V_{SS}			-14.25	-15.0	-15.75	*	*	*	*	*	V
I_{DD}				50						*	μA
I_{CC}				6						*	mA
I_{SS}				-5						*	mA
Power			170	200						*	mW
TEMPERATURE RANGE											
Specified Performance			-40		+85	*		*	*	*	$^\circ C$

* Specifications same as grade to the left.

SPECIFICATIONS (Single Supply)

At $T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = GND$, $V_{REFH} = +10V$, and $V_{REFL} = +50mV$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7734E			DAC7734EB			DAC7734EC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY											
Linearity Error ⁽¹⁾ (INL)	$T = 25^\circ C$				± 3	*	*			± 2	LSB
T_{MIN} to T_{MAX}			± 4		± 4					± 3	LSB
Linearity Match	$T = 25^\circ C$				± 3		± 2			± 1	LSB
Differential Linearity Error (DNL)	$T = 25^\circ C$				± 3		± 2			± 1	LSB
T_{MIN} to T_{MAX}		14			± 3		± 2			± 1	LSB
Monotonicity, T_{MIN} to T_{MAX}					± 3						Bits
Unipolar Zero	$T = 25^\circ C$				± 0.025		*			*	% of FSR
Unipolar Zero Error, T_{MIN} to T_{MAX}					± 0.05		*			*	% of FSR
Full-Scale Error	$T = 25^\circ C$				± 0.025		*			*	% of FSR
Full-Scale Error, T_{MIN} to T_{MAX}					± 0.05		*			*	% of FSR
Unipolar Zero Matching	Channel-to-Channel Matching				± 0.024		*			*	% of FSR
Full-Scale Matching	Channel-to-Channel Matching				± 0.024		*			*	% of FSR
Power Supply Rejection Ratio (PSRR)	At Full Scale			25			*			*	ppm/V
ANALOG OUTPUT											
Voltage Output	$V_{REFL} = 0V$, $V_{SS} = 0V$	0			V_{REFH}	*	*	*		*	V
Output Current	$R = 10k\Omega$	± 5				*	*	*			mA
Maximum Load Capacitance			500			*	*			*	pF
Short-Circuit Current			± 20		Indefinite		*			*	mA
Short-Circuit Duration	To V_{CC} or GND										
REFERENCE INPUT											
Ref High Input Voltage Range			$V_{REFL} + 1.25$			$+10$				*	V
Ref Low Input Voltage Range			0			$V_{REFH} - 1.25$				*	V
Ref High Input Current			-0.3			1.0				*	mA
Ref Low Input Current			-1.5			-0.3				*	mA
DYNAMIC PERFORMANCE											
Settling Time	To $\pm 0.003\%$, 10V Output Step		8	10		*	*			*	μs
Channel-to-Channel Crosstalk	See Figure 6		0.5			*				*	LSB
Digital Feedthrough			2			*				*	$nV \cdot s$
Output Noise Voltage	$f = 10kHz$		60			*				*	nV/\sqrt{Hz}
DIGITAL INPUT											
V_{IH}			$0.7 \cdot V_{DD}$			V_{DD}					V
V_{IL}			0			$0.3 \cdot V_{DD}$					V
I_{IH}						± 10					μA
I_{IL}						± 10					μA
DIGITAL OUTPUT											
V_{OH}	$I_{OH} = -0.8mA$	3.6	4.5	0.4	*	*	*	*	*	*	V
V_{OL}	$I_{OL} = 1.6mA$		0.3			*				*	V
POWER SUPPLY											
V_{DD}			+4.75	+5.0	+5.25	*	*	*	*	*	V
V_{CC}			+14.25	+15.0	+15.75	*	*	*	*	*	V
V_{SS}				0		*				*	V
I_{DD}				50		*				*	μA
I_{CC}				3.5		*				*	mA
Power			50	70		*				*	mW
TEMPERATURE RANGE											
Specified Performance		-40		+85	*			*	*	*	$^\circ C$

* Specifications same as grade to the left.

NOTE: (1) If $V_{SS} = 0V$, the specification applies at code 0021_H and above, due to possible negative zero scale error.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V_{CC} to V_{SS}	-0.3V to +32V
V_{CC} to AGND	-0.3V to +16V
V_{SS} to AGND	+0.3V to -16V
AGND to DGND	-0.3V to +0.3V
V_{REFH} to AGND	-9V to +11V
V_{REFL} to AGND	-11V to +9V
V_{DD} to GND	-0.3V to +6V
V_{REFH} to V_{REFL}	-1V to 22V
Digital Input Voltage to GND	-0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	-0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

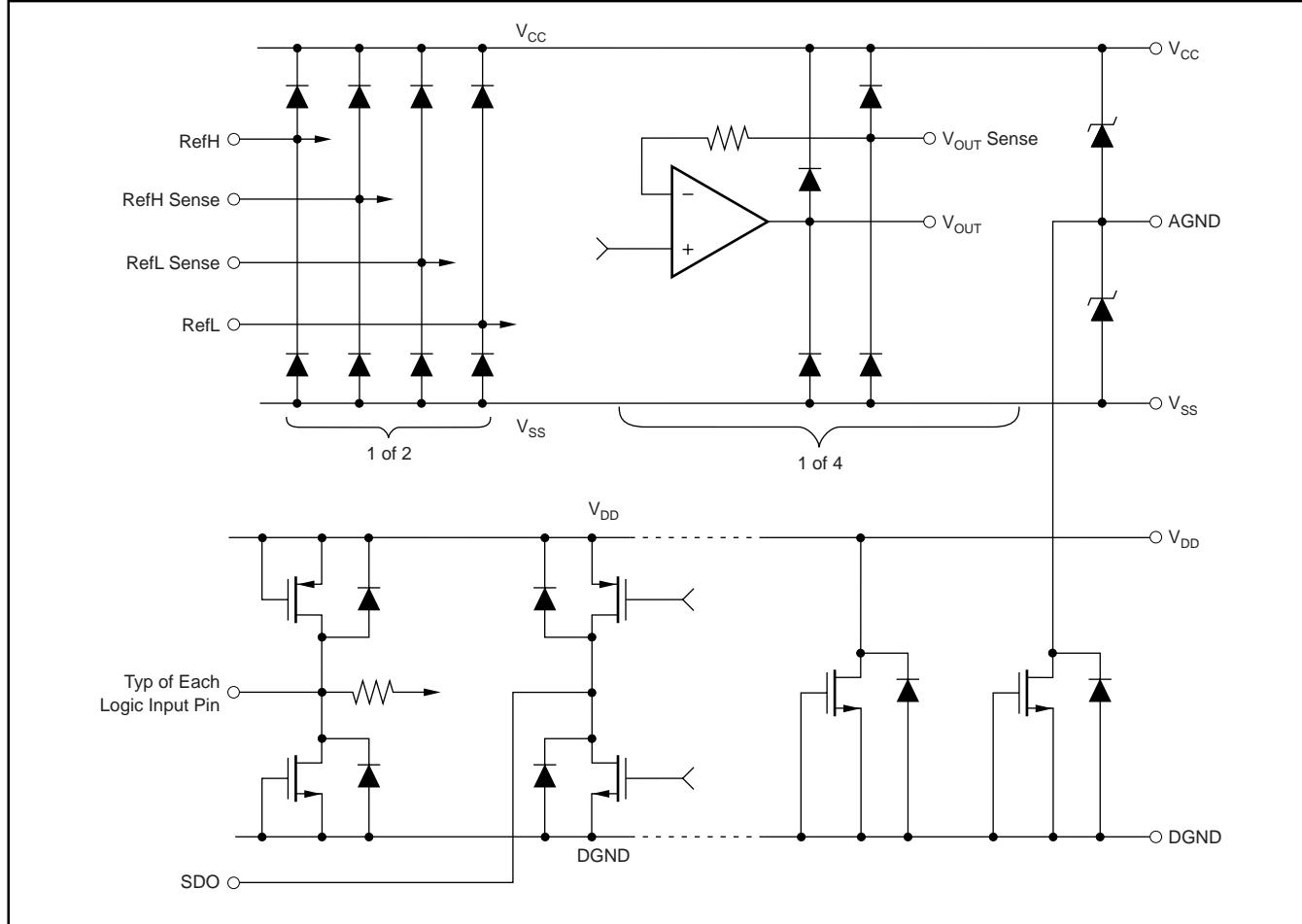
NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	LINEARITY ERROR (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC7734E "	± 4 "	± 3 "	SSOP-48	333 "	-40°C to +85°C "	DAC7734E DAC7734E/1K	Rails, 30 Tape and Reel, 1000
DAC7734EB "	± 4 "	± 2 "	SSOP-48	333 "	-40°C to +85°C "	DAC7734EB DAC7734EB/1K	Rails, 30 Tape and Reel, 1000
DAC7734EC "	± 3 "	± 1 "	SSOP-48	333 "	-40°C to +85°C "	DAC7734EC DAC7734EC/1K	Rails, 30 Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ESD PROTECTION CIRCUITS

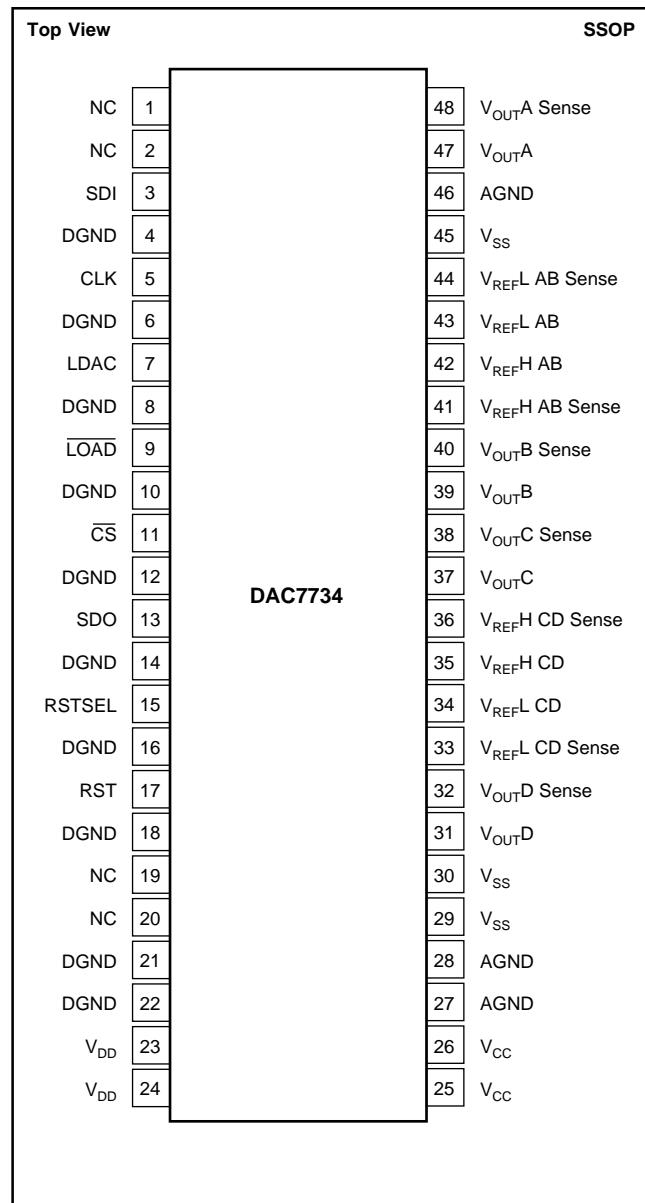


ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION



PIN DESCRIPTIONS

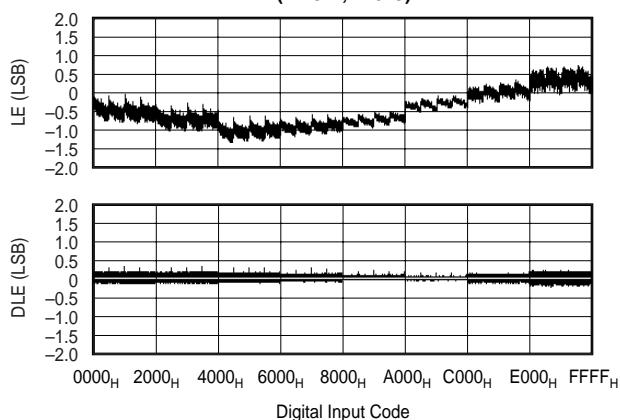
PIN	NAME	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	SDI	Serial Data Input
4	DGND	Digital Ground
5	CLK	Data Clock Input
6	DGND	Digital Ground
7	LDAC	DAC Register Load Control, Rising Edge Triggered
8	DGND	Digital Ground
9	LOAD	DAC Input Register Load Control, Active Low
10	DGND	Digital Ground
11	CS	Chip Select, Active Low
12	DGND	Digital Ground
13	SDO	Serial Data Output
14	DGND	Digital Ground
15	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST command will set the DAC registers to mid-scale (8000H). If LOW, a RST command will set the DAC registers to zero (0000H).
16	DGND	Digital Ground
17	RST	Reset, Rising Edge Triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.
18	DGND	Digital Ground
19	NC	No Connection
20	NC	No Connection
21	DGND	Digital Ground
22	DGND	Digital Ground
23	V _{DD}	Digital +5V Power Supply
24	V _{DD}	Digital +5V Power Supply
25	V _{CC}	Analog +15V Power Supply
26	V _{CC}	Analog +15V Power Supply
27	AGND	Analog Ground
28	AGND	Analog Ground
29	V _{SS}	Analog -15V Power Supply or 0V Single Supply
30	V _{SS}	Analog -15V Power Supply or 0V Single Supply
31	V _{OUTD}	DAC D Output Voltage
32	V _{OUTD} Sense	DAC D's Output Amplifier Inverting Input. Used to close feedback loop at load.
33	V _{REFL_CD} Sense	DAC C and D Reference Low Sense Input
34	V _{REFL_CD}	DAC C and D Reference Low Input
35	V _{REFH_CD}	DAC C and D Reference High Input
36	V _{REFH_CD} Sense	DAC C and D Reference High Sense Input
37	V _{OUTC}	DAC C Output Voltage
38	V _{OUTC} Sense	DAC C's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
39	V _{OUTB}	DAC B Output Voltage
40	V _{OUTB} Sense	DAC B's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
41	V _{REFH_AB} Sense	DAC A and B Reference High Sense Input
42	V _{REFH_AB}	DAC A and B Reference High Input
43	V _{OUTL_AB}	DAC A and B Reference Low Input
44	V _{REFL_AB} Sense	DAC A and B Reference Low Sense Input
45	V _{SS}	Analog -15V Power Supply or 0V Single Supply
46	AGND	Analog Ground
47	V _{OUTA}	DAC A Output Voltage
48	V _{OUTA} Sense	DAC A's Output Amplifier Inverting Input. Used to close the feedback loop at the load.

TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

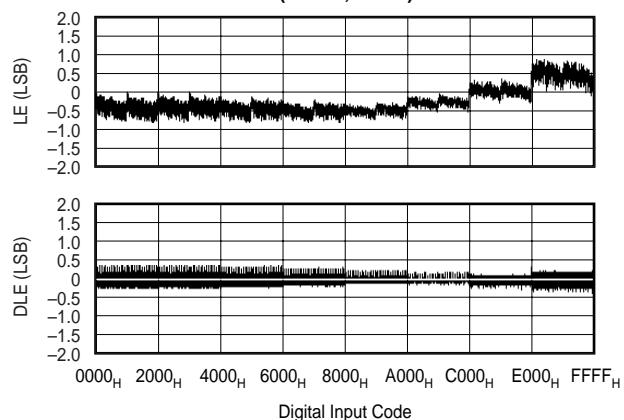
At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = 0$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.

+25°C

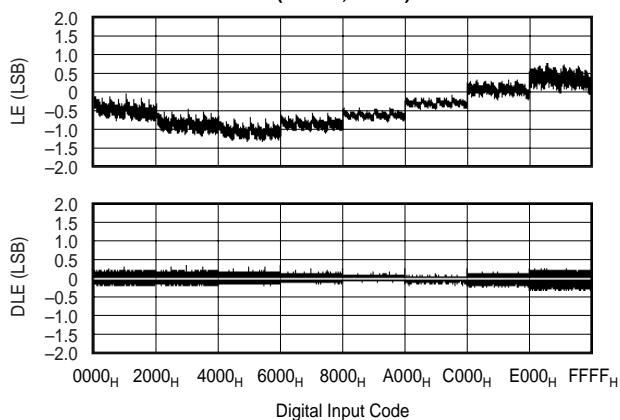
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)



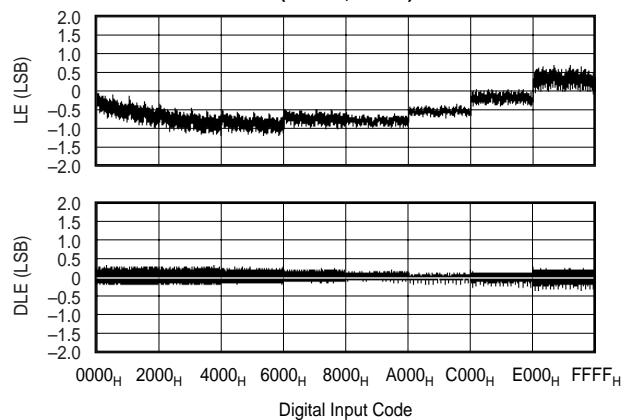
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

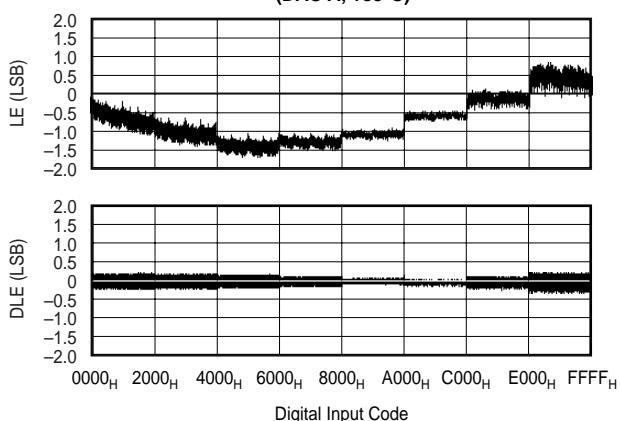


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

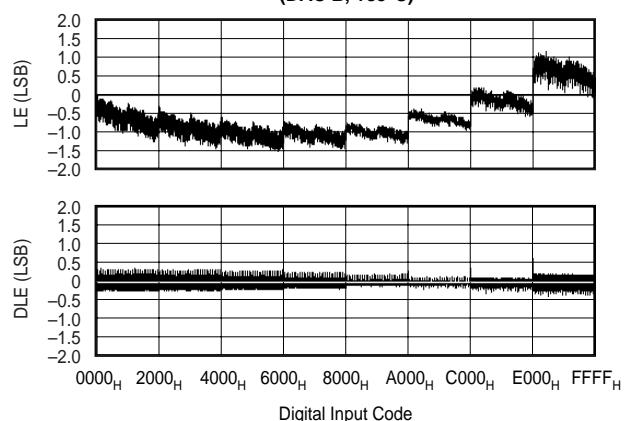


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

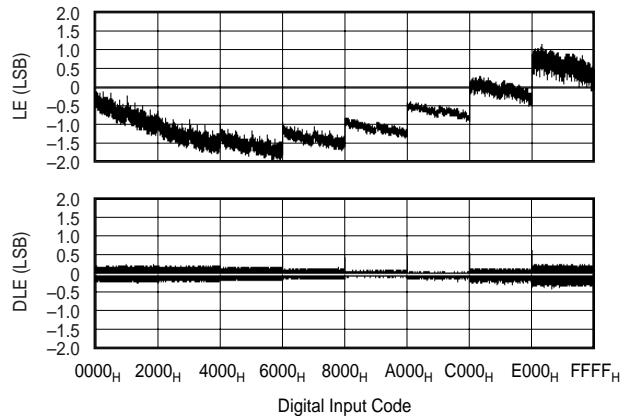


TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

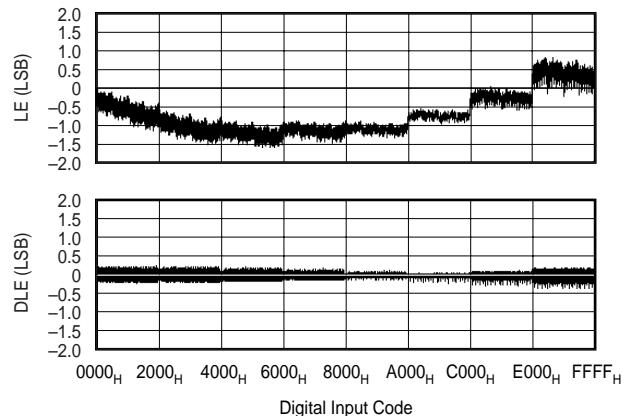
At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = 0$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.

+85°C (cont.)

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

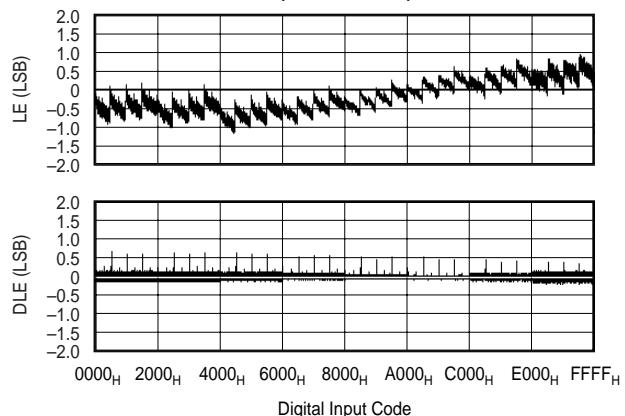


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

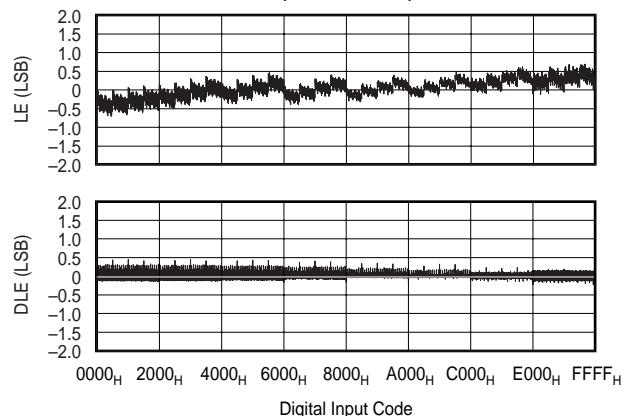


-40°C

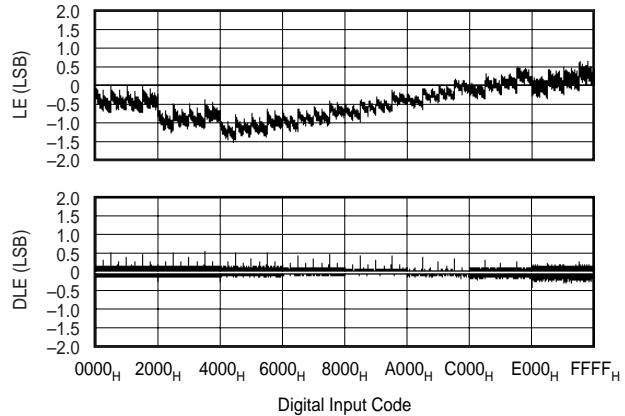
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, -40°C)



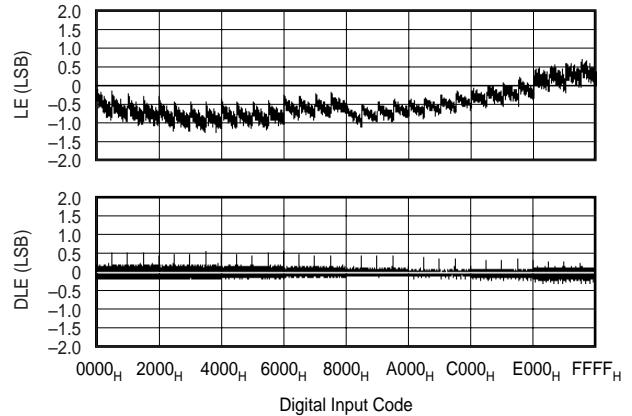
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, -40°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, -40°C)

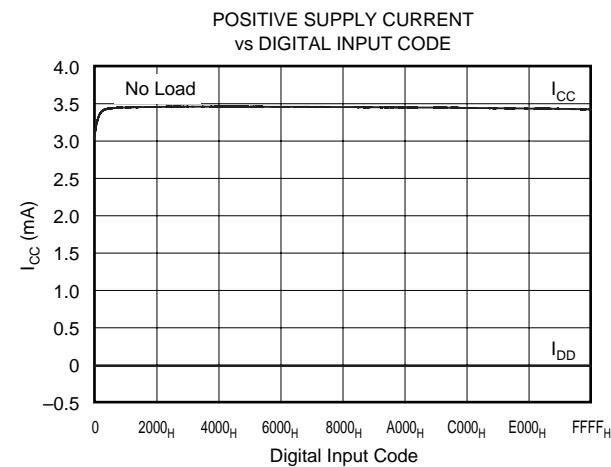
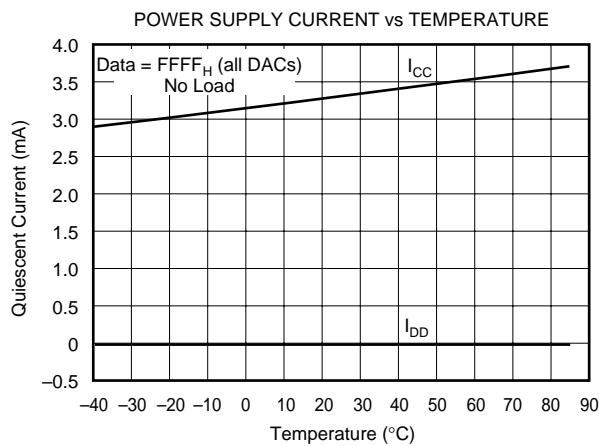
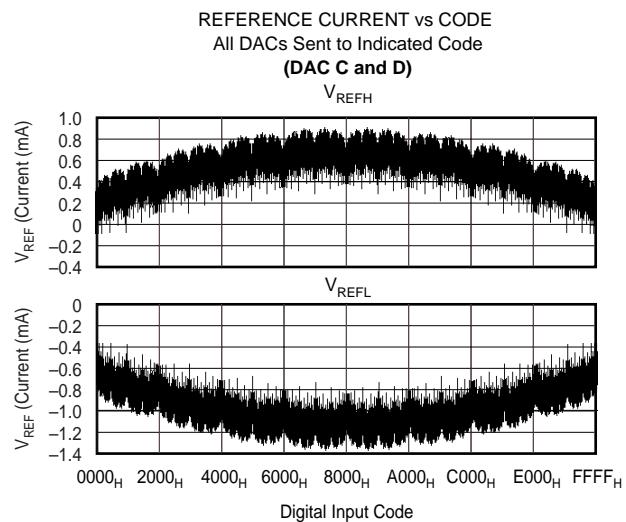
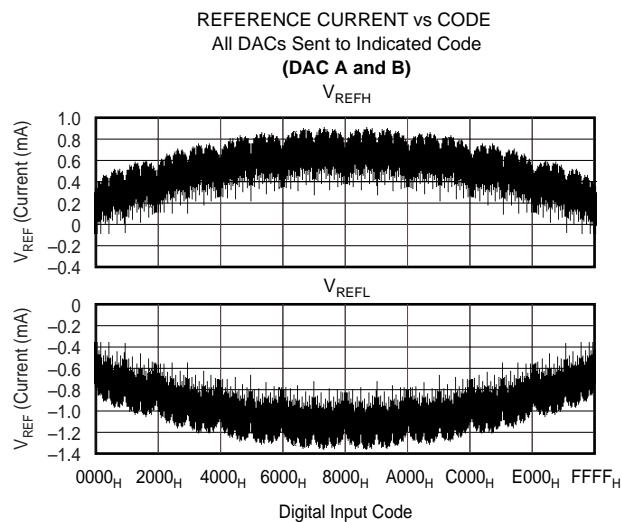
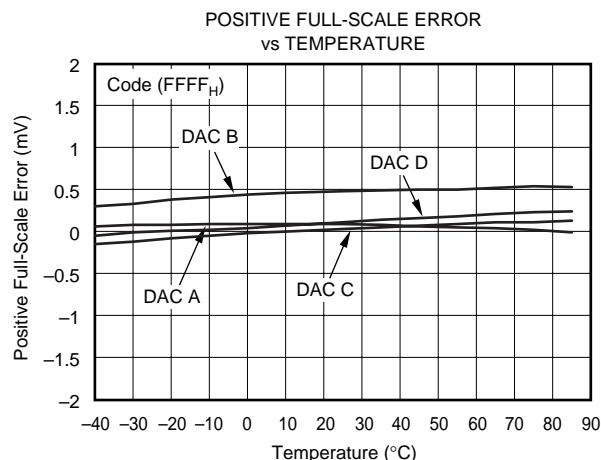
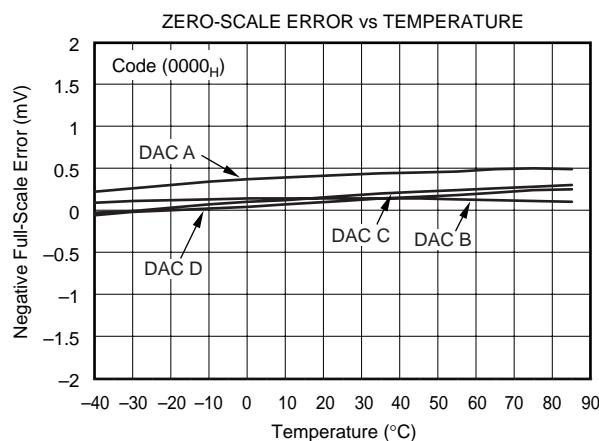


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, -40°C)



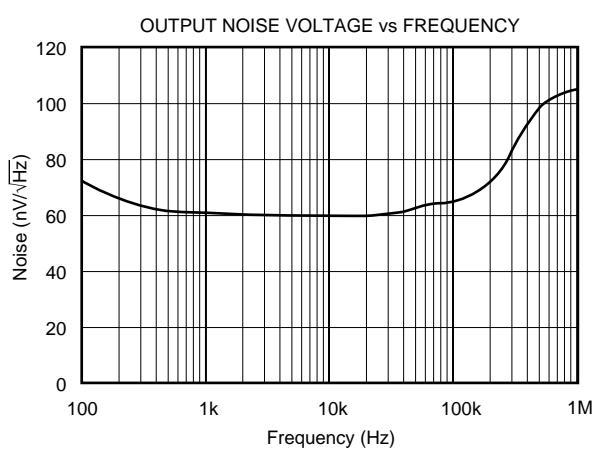
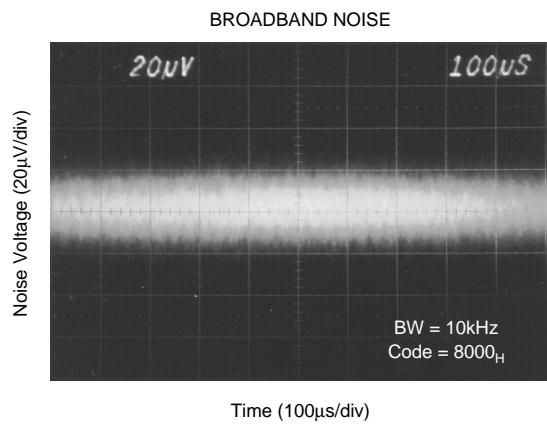
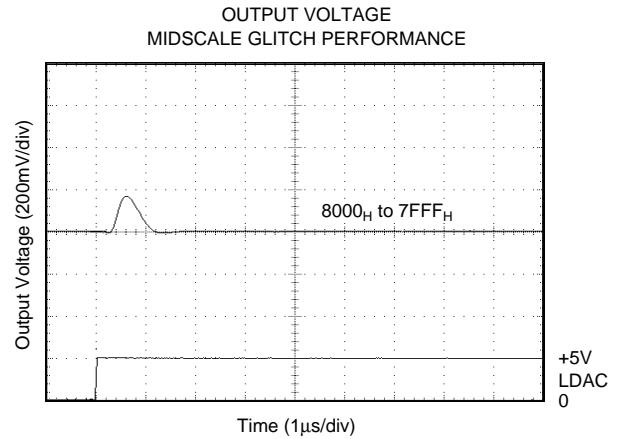
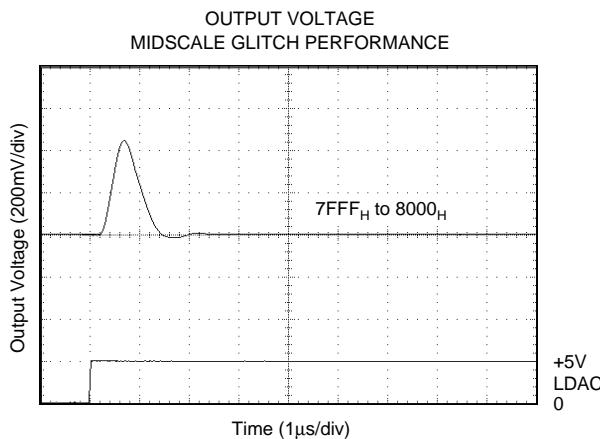
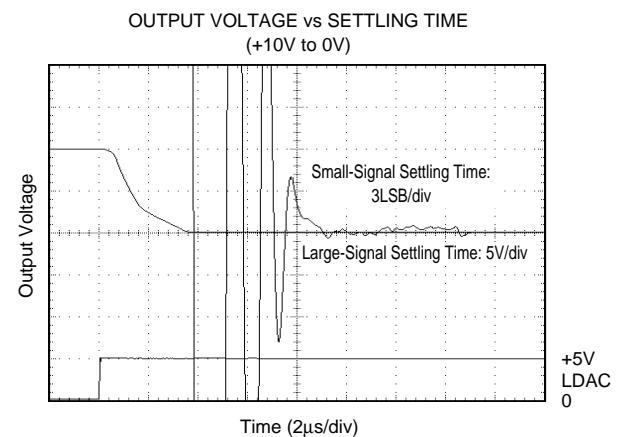
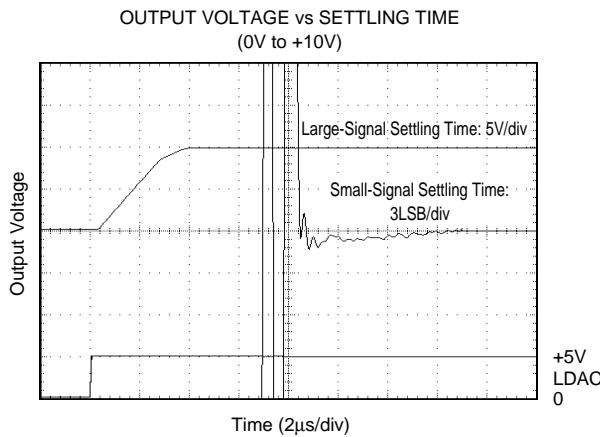
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = 0$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.



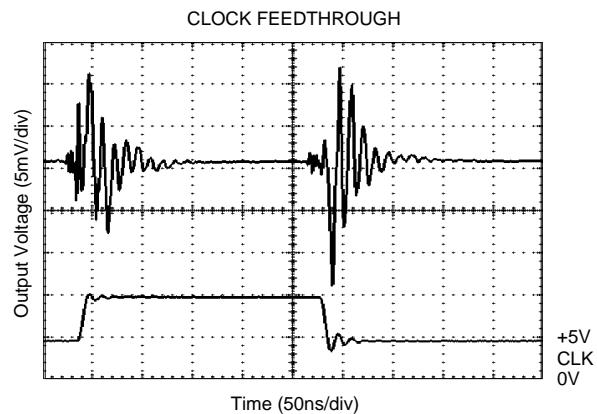
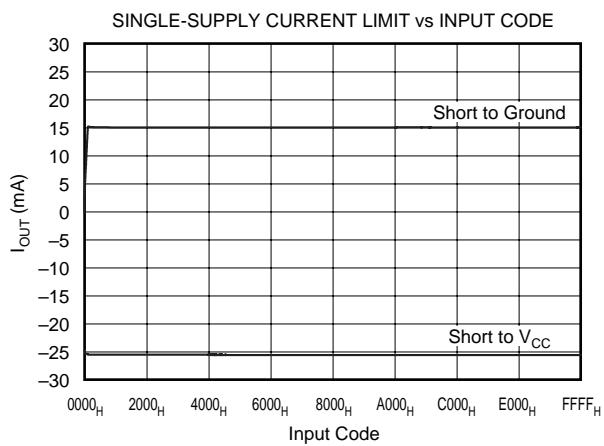
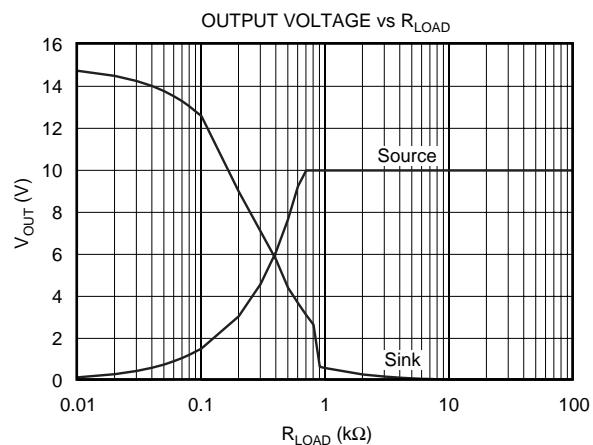
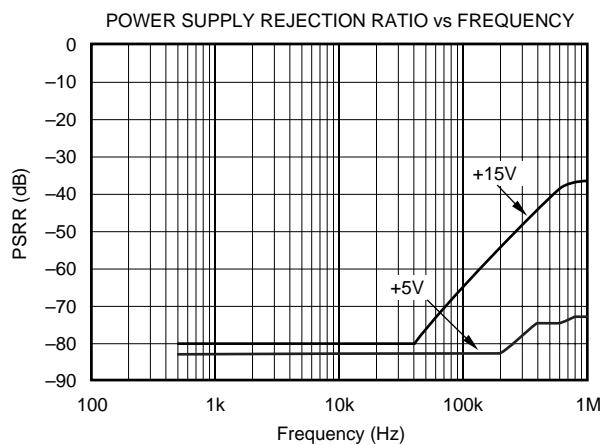
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = 0$, $V_{REFH} = +10V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = 0$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.

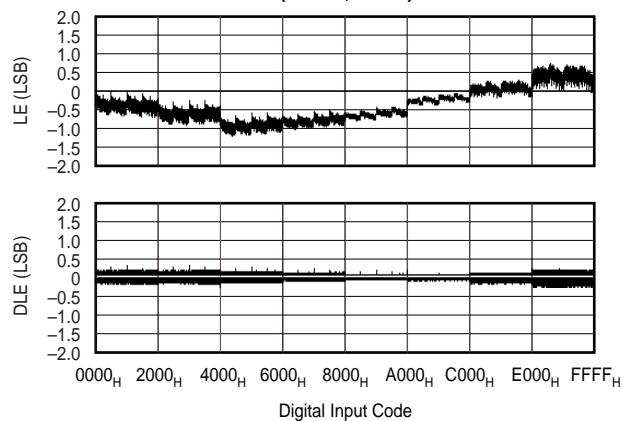


TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$

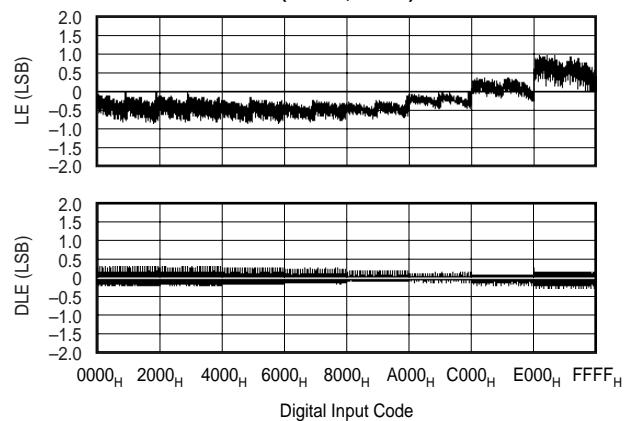
At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.

+25°C

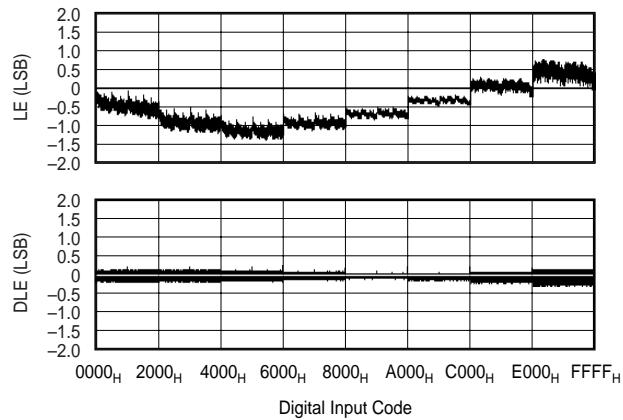
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)



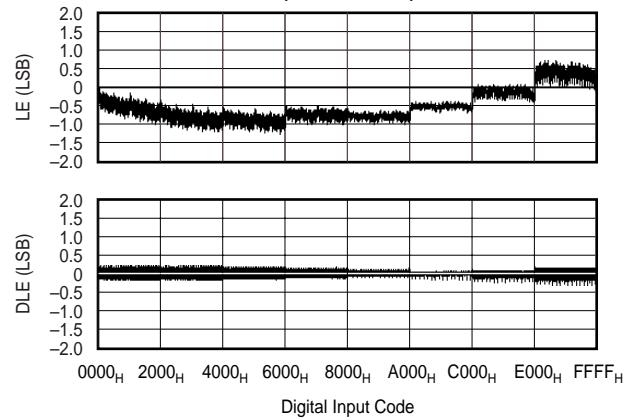
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

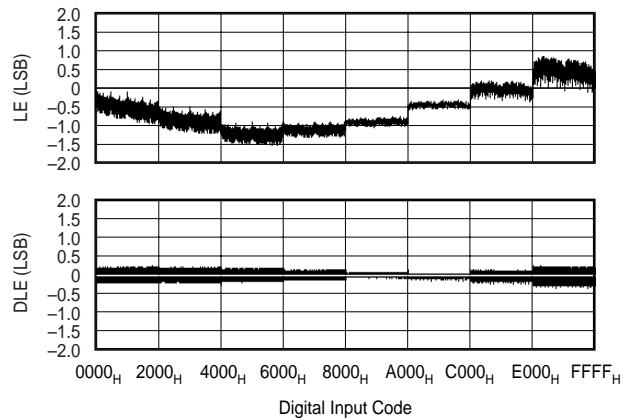


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

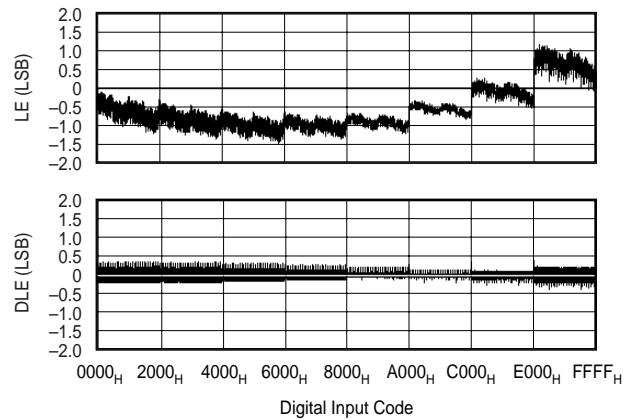


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)



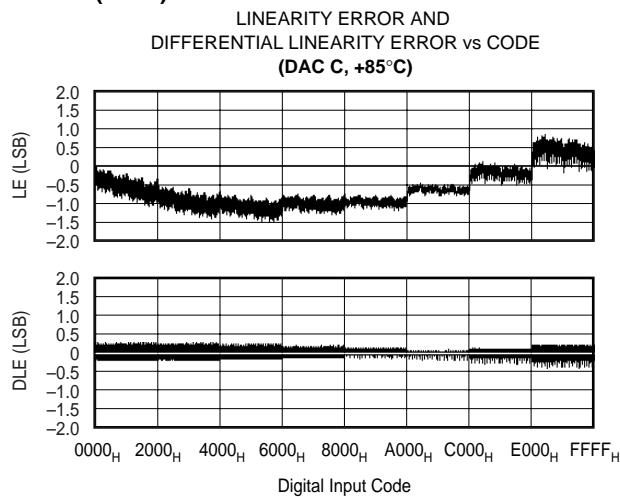
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)



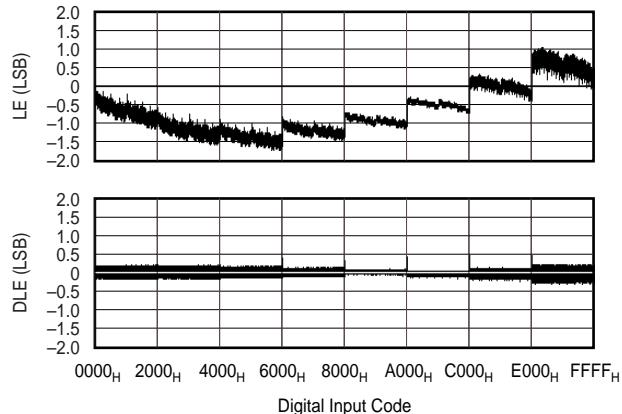
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.

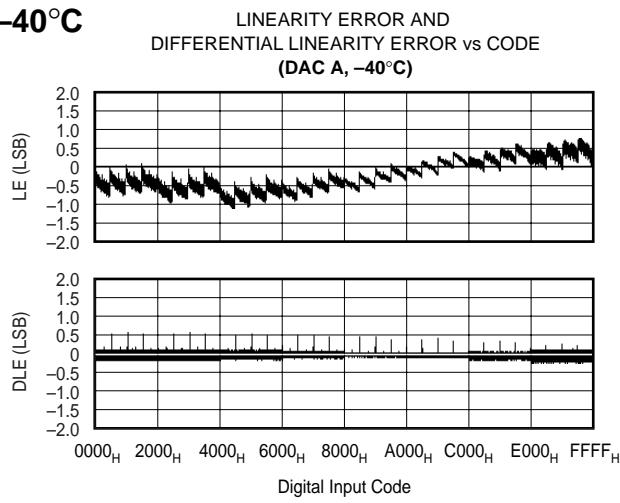
+85°C (cont.)



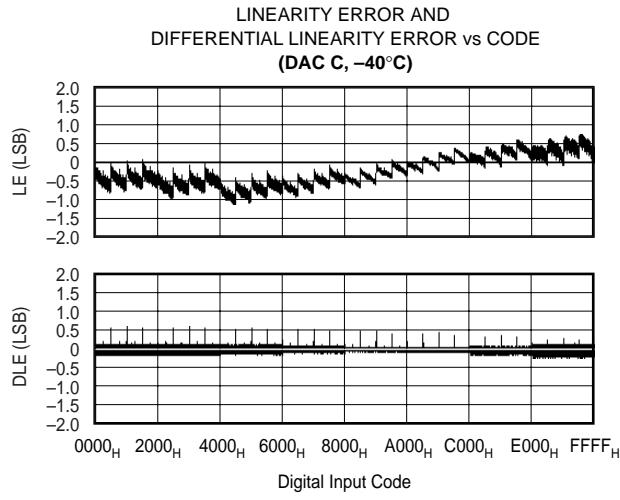
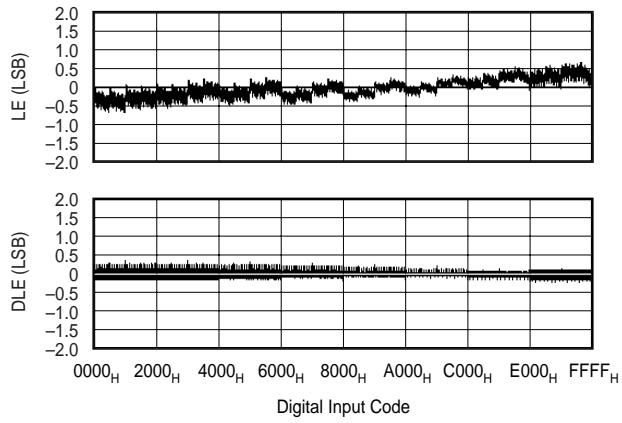
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, +85°C)



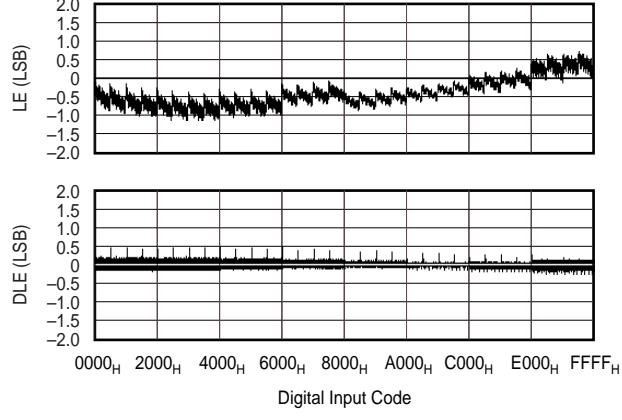
-40°C



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, -40°C)

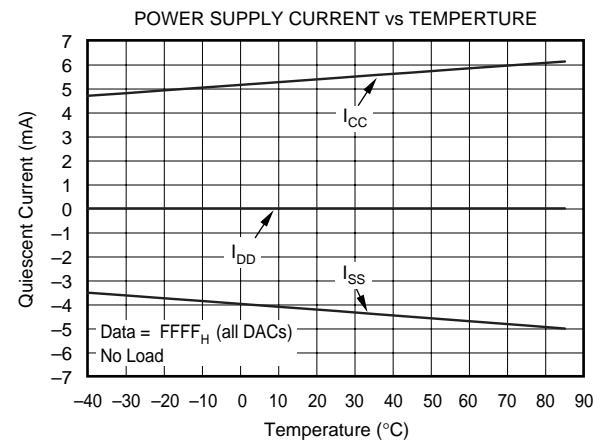
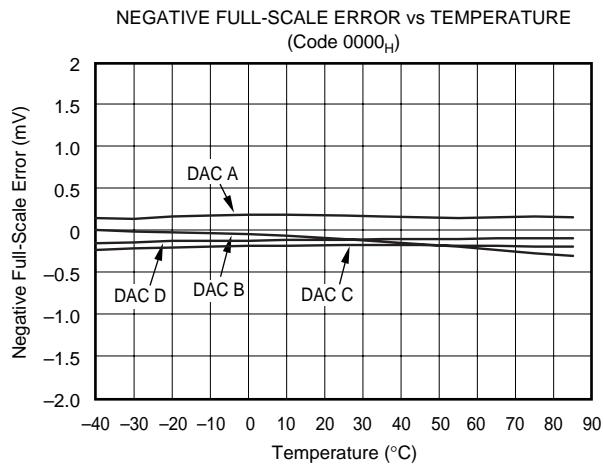
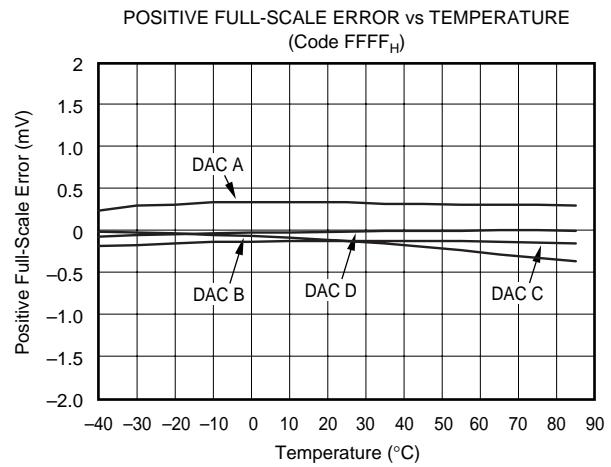
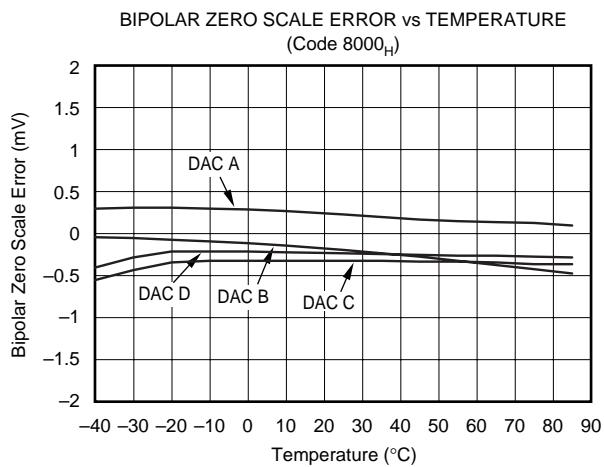
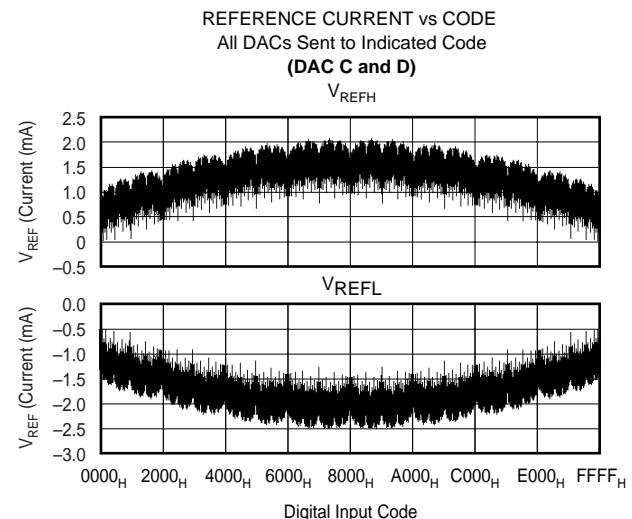
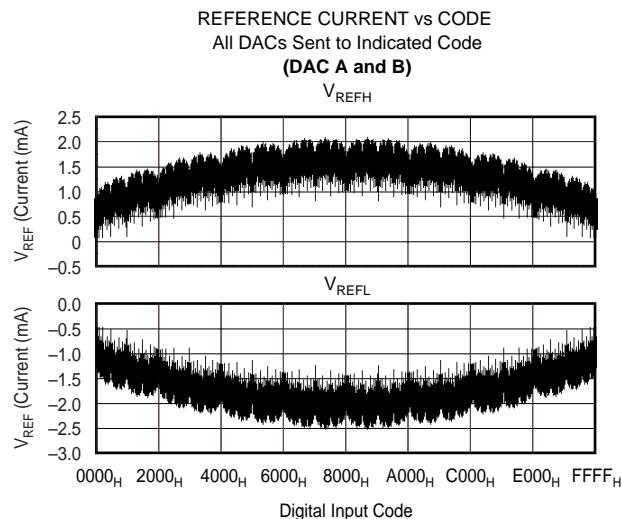


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, -40°C)



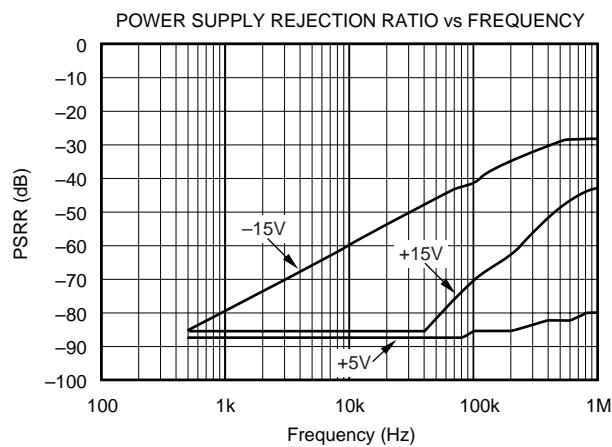
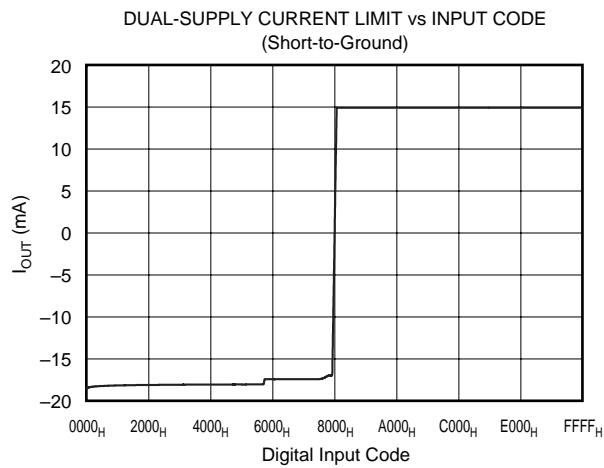
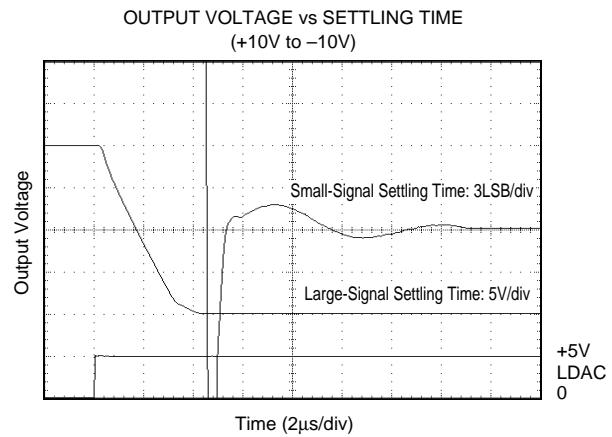
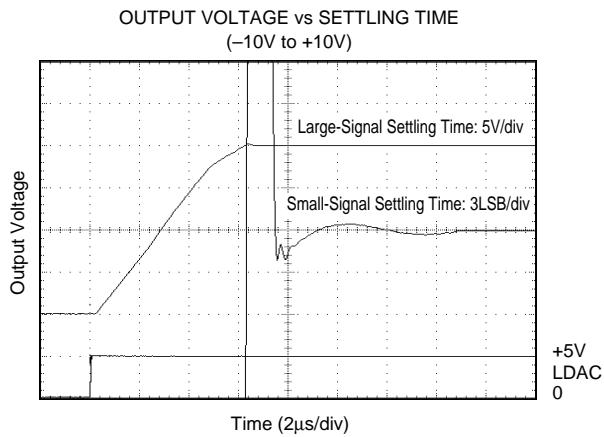
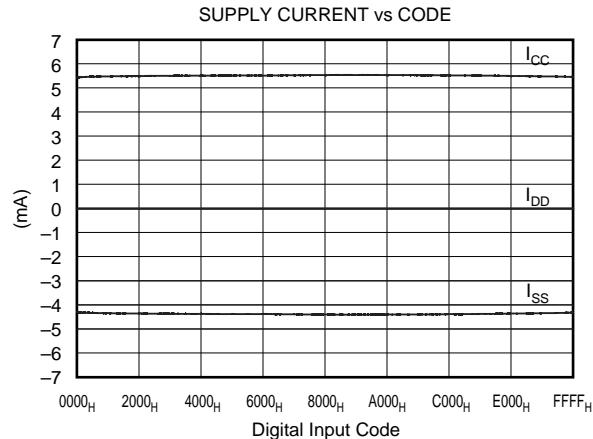
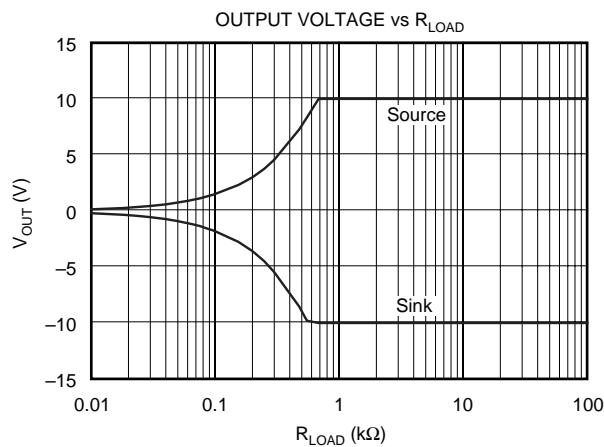
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.



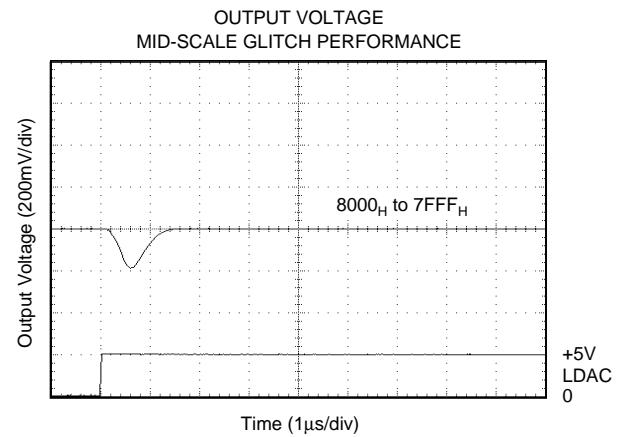
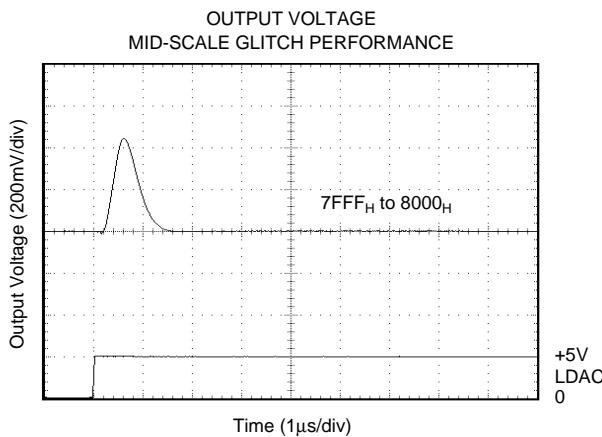
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.



THEORY OF OPERATION

The DAC7734 is a quad voltage output, 16-bit Digital-to-Analog Converter (DAC). The architecture is an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs, and output op amp, as shown in Figure 1. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references V_{REFL} and V_{REFH} .

The digital input is a 24-bit serial word that contains a 2-bit address code for selecting one of four DACs, a quick load bit, five unused bits, and the 16-bit DAC code (MSB first). The converters can be powered from either a single +15V supply or a dual $\pm 15V$ supply and a +5V logic supply. The device offers a reset function that immediately sets all DAC output voltages and DAC registers to mid-scale code 8000_H or to zero-scale, code 0000_H. See Figures 2 and 3 for the basic operation of the DAC7734.

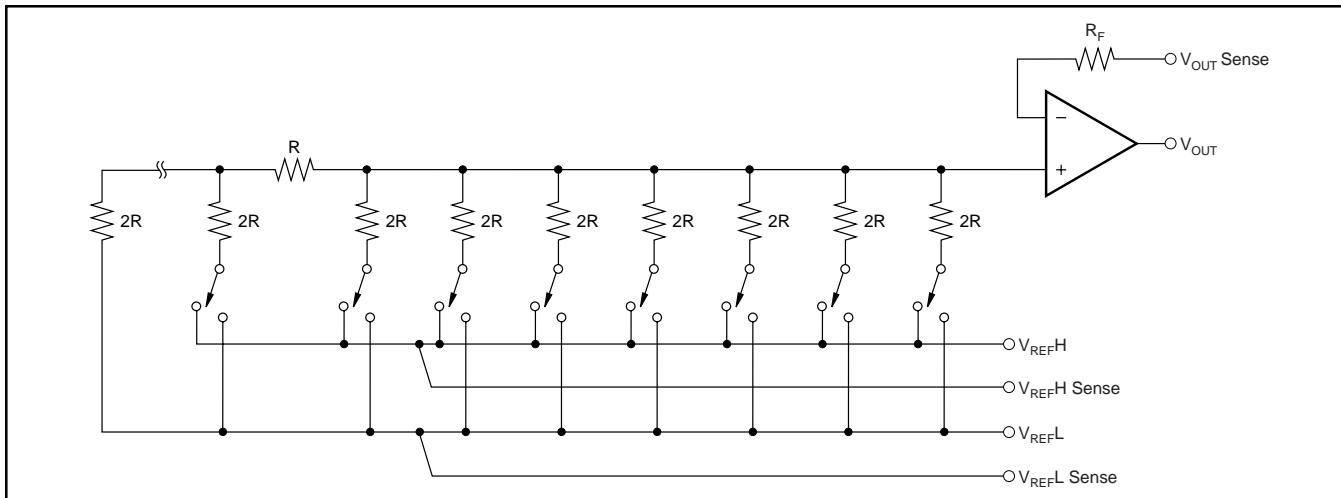


FIGURE 1. DAC7734 Architecture.

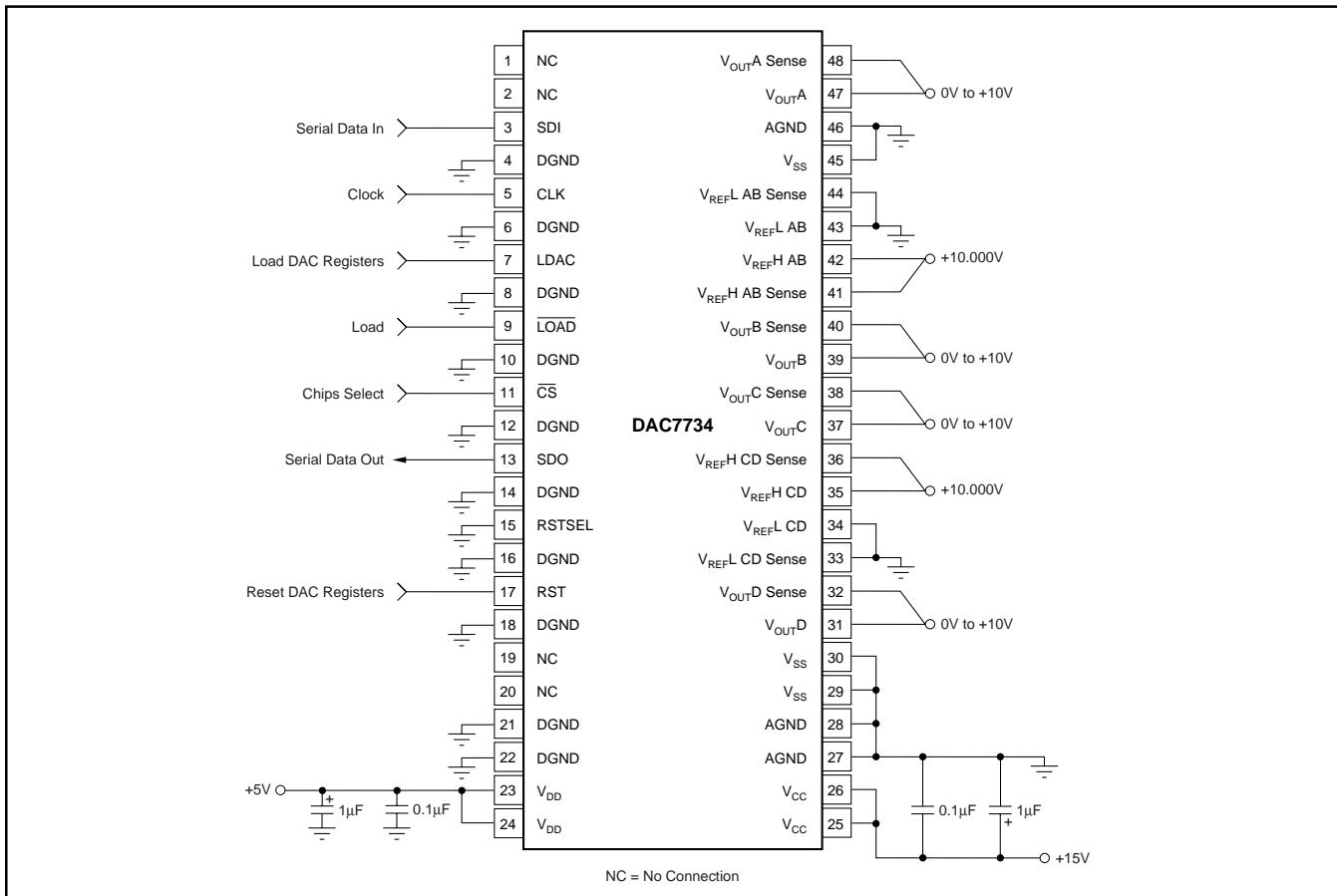


FIGURE 2. Basic Single-Supply Operation of the DAC7734.

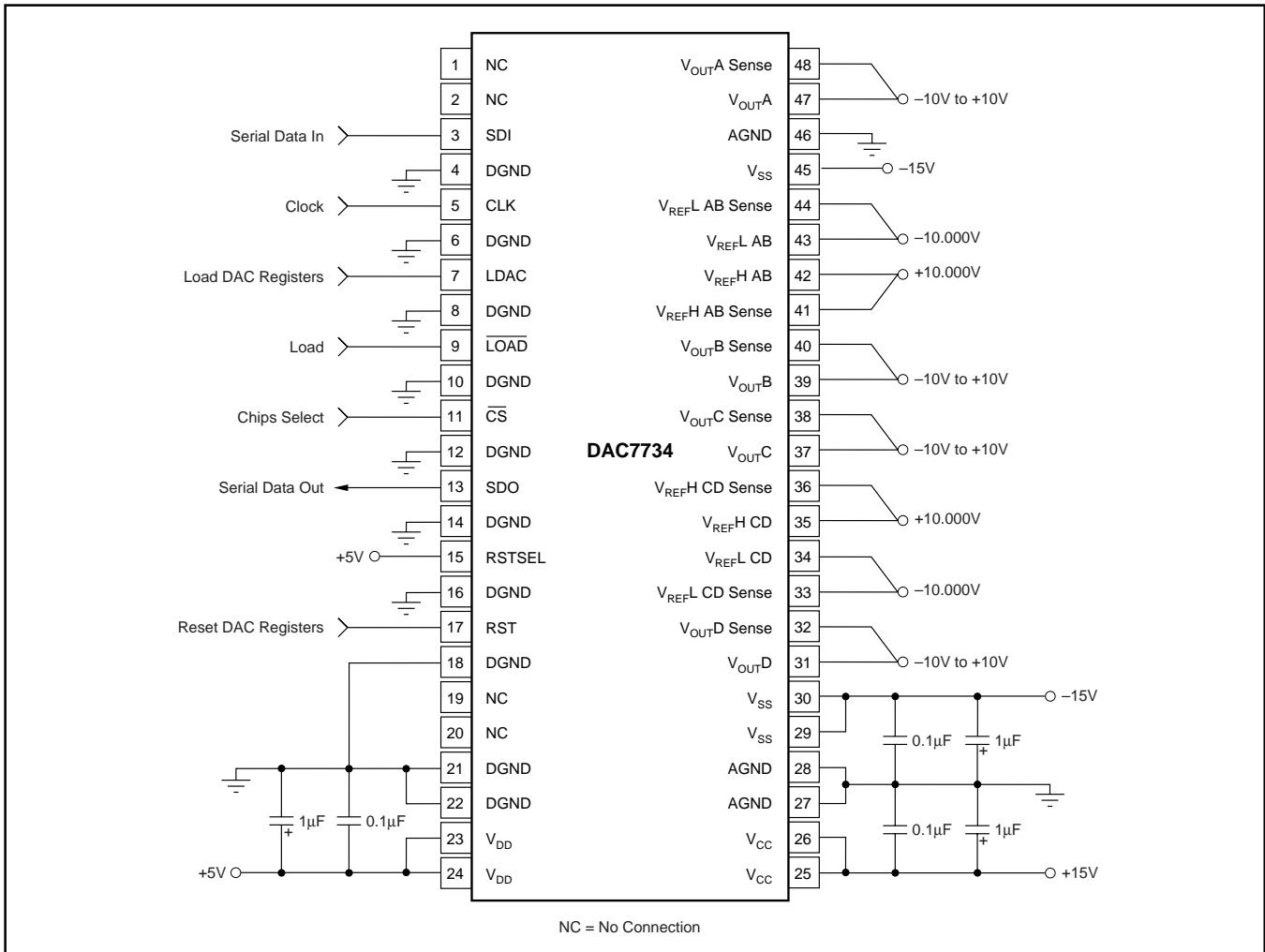


FIGURE 3. Basic Dual-Supply Operation of the DAC7734.

ANALOG OUTPUTS

When $V_{SS} = -15V$ (dual-supply operation), the output amplifier can swing to within 4V of the supply rails, ensured over the -40°C to $+85^{\circ}\text{C}$ temperature range. When $V_{SS} = 0V$ (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when $V_{SS} = 0V$. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of -5mV , the first specified output starts at code 0021_H.

Due to the high accuracy of these DACs, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 10V full-scale range has a 1LSB value of $152\mu\text{V}$. With a load current of 1mA, series wiring and connector resistance of only $150\text{m}\Omega$ (R_{W2}) will cause a voltage drop of $150\mu\text{V}$, as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board is $1/2\text{ m}\Omega$ per square. For a 1mA load, a 20 milli-inch wide printed circuit conductor 6 inches long will result in a voltage drop of $150\mu\text{V}$.

The DAC7734 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 4), thus ensuring an accurate output voltage.

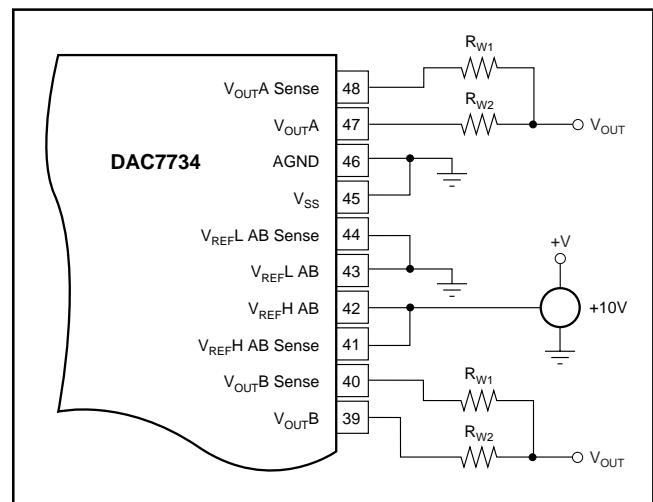


FIGURE 4. Analog Output Closed-Loop Configuration (1/2 DAC7734). R_W represents wiring resistances.

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH} , can be any voltage between $V_{SS} + 4V$ and $V_{CC} - 4V$, provided that V_{REFH} is at least 1.25V greater than V_{REFL} . The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of $-14.25V$ to $-15.75V$. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not ensured.

The current into the V_{REFH} input and out of V_{REFL} depends on the DAC output voltages, and can vary from a few microamps to approximately 2.0mA. The reference input appears as a varying load to the reference. The DAC7734 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 9 show different reference configurations, and the effect on the linearity and differential linearity.

The analog supplies must come up first. If V_{CC} and V_{SS} do not come up together, then V_{SS} should come up first. If the power supplies for the reference come up first, then the V_{CC} and V_{SS} supplies will be powered from the reference via the ESD protection diode; see the ESD protection circuits on page 4.

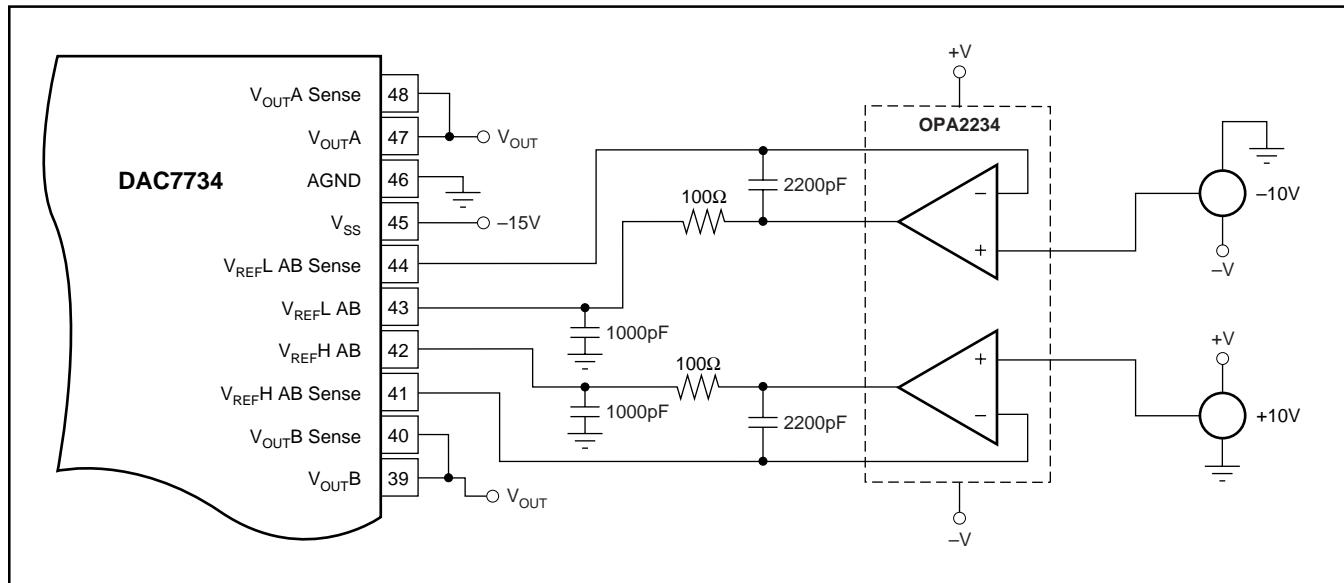


FIGURE 5. Dual-Supply Configuration-Buffered References, used for Dual-Supply Performance (1/2 DAC7734).

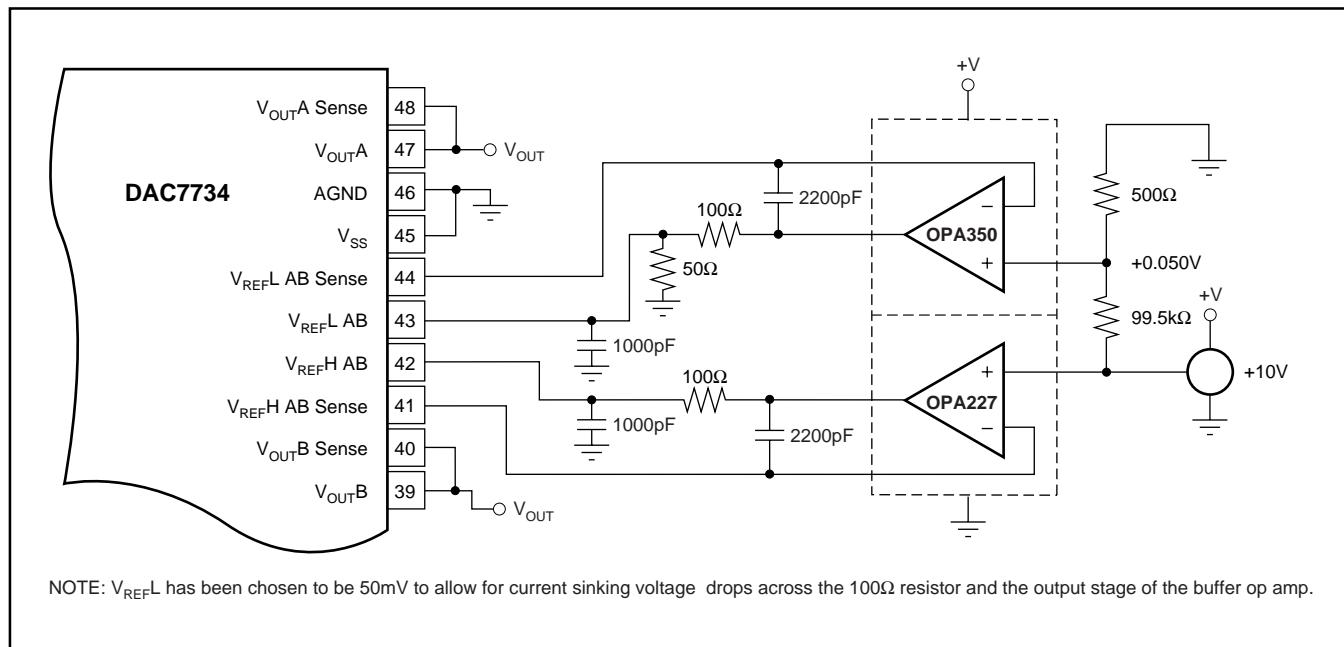


FIGURE 6. Single-Supply Buffered Reference with a Reference Low of 50mV used for Single-Supply Performance Curves (1/2 DAC7734).

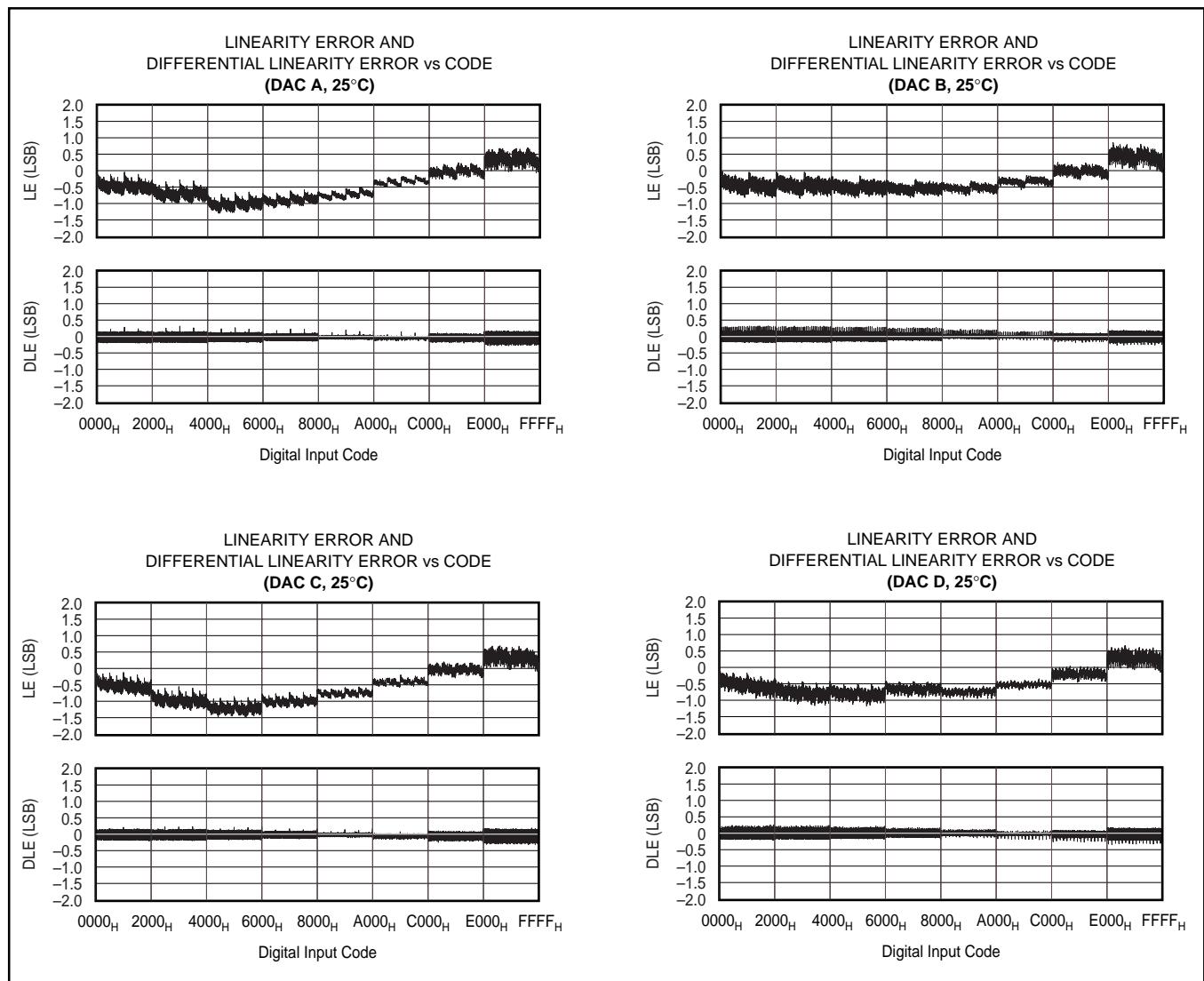


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 8.

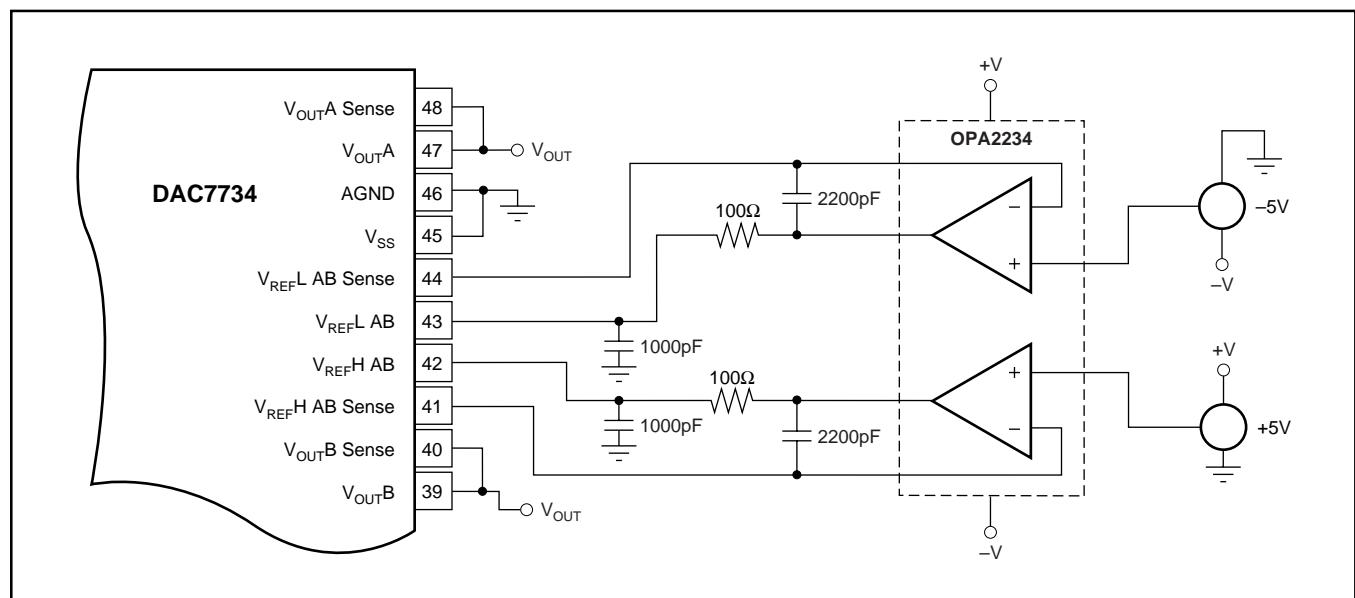


FIGURE 8. Dual-Supply Buffered Reference with $V_{REFL} = -5V$ and $V_{REFH} = +5V$ (1/2 DAC7734).

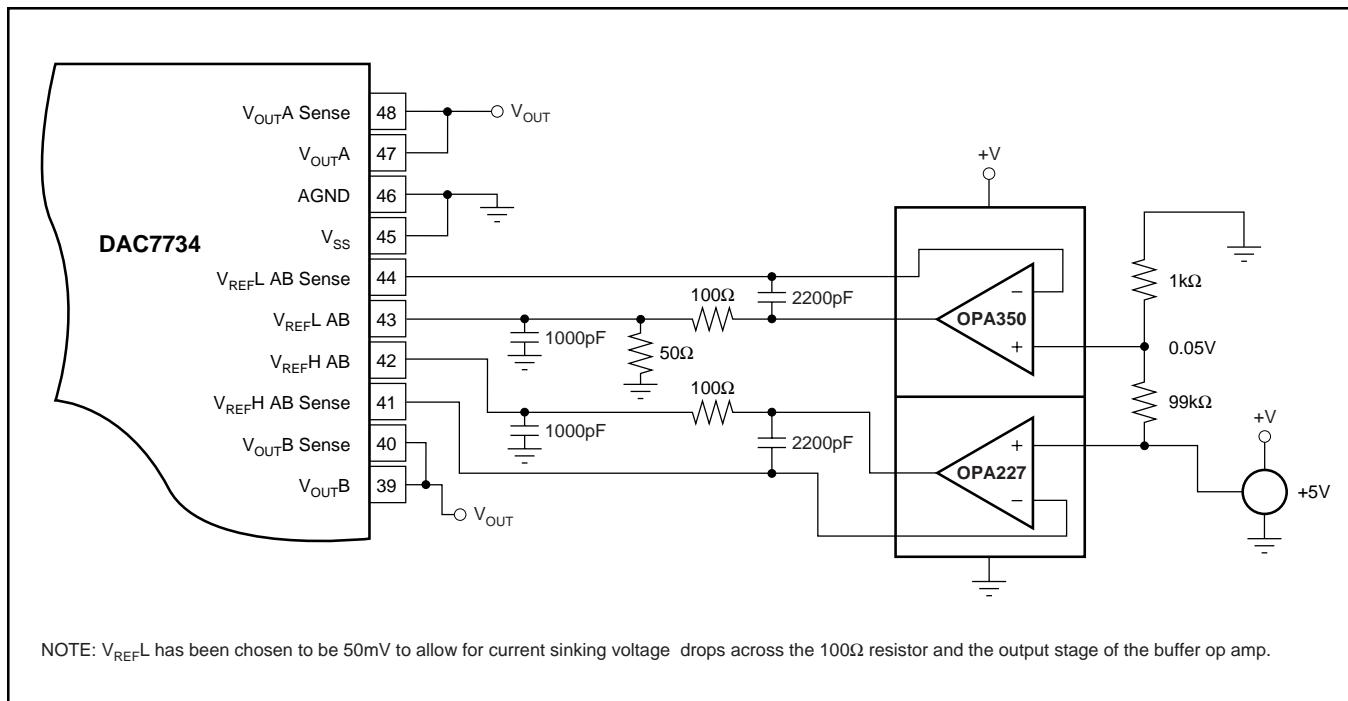


FIGURE 9. Single-Supply Buffered Reference with a Reference Low of 50mV and Reference High of +5V.

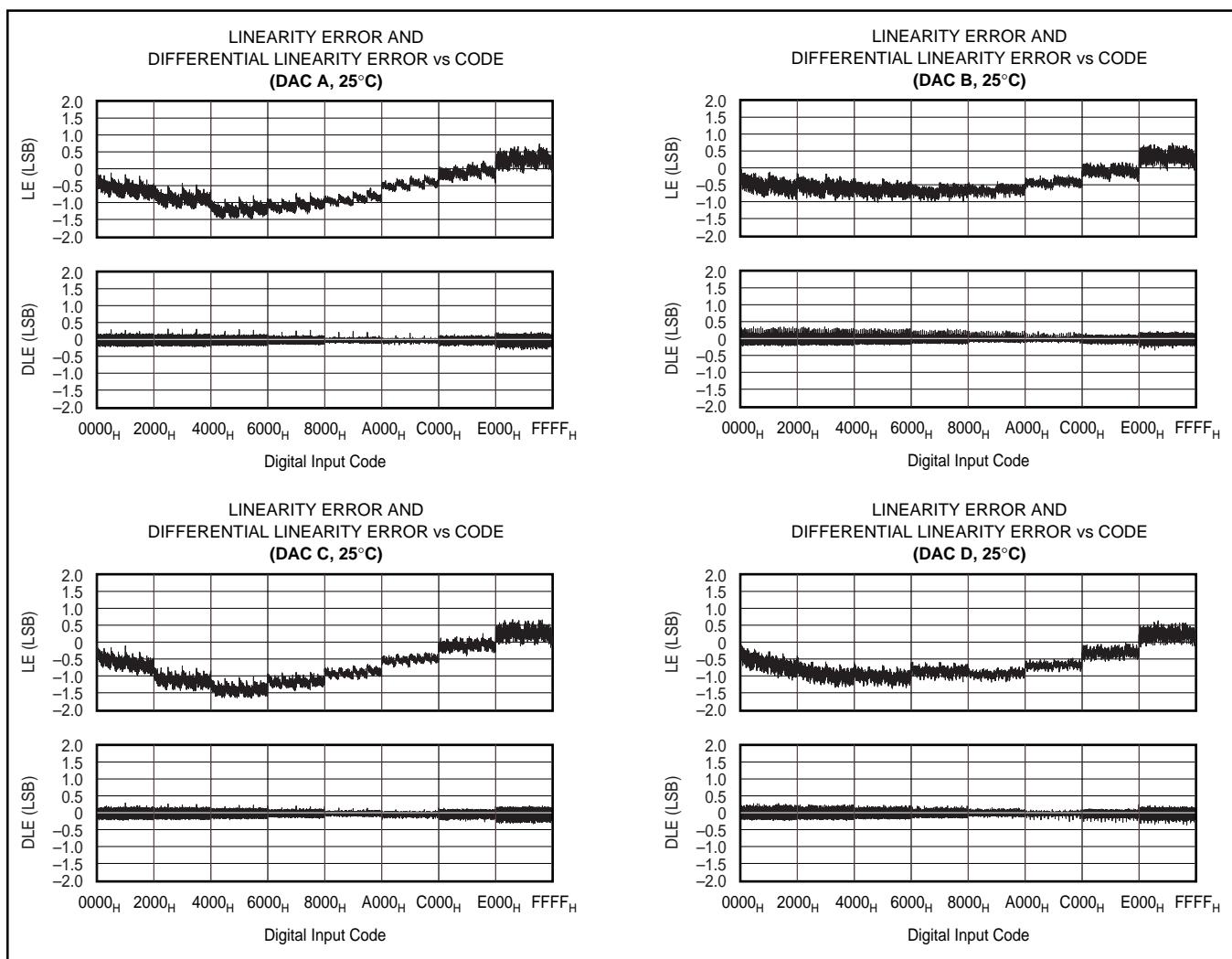


FIGURE 10. Integral Linearity and Differential Linearity Error Curves for Figure 9.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7734. The interface consists of a Signal Data Clock (CLK) input, Serial Data (SDI), DAC Input Register Load Control Signal (LOAD), and DAC Register Load Control Signal (LDAC). In addition, a Chip Select (CS) input is available to enable serial communication when there are multiple serial devices. An asynchronous Reset (RST) input, by the rising edge, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal.

The DAC code, quick load control, and address are provided via a 24-bit serial interface (see Table I). The first two bits shifted into the shift register, B23 and B22, are the DAC register address. These bits select the input register that will be updated when LOAD goes LOW. The third bit, B21, is a “Quick Load” bit such that if HIGH, the code in the shift register is loaded into ALL DAC input registers when the LOAD signal goes LOW, independent of the state of the address bits, B23 and B22. If the “Quick Load” bit is LOW, the contents of the shift register is loaded only to the DAC register that is addressed. Bits B20 through B16 are not used and can assume any logical value. The last sixteen bits, B15 through B0, make up the DAC code to be loaded into the selected input register.

The internal DAC register is edge-triggered and not level-triggered. When the LDAC signal is transitioned from LOW to HIGH, the digital word currently in the DAC input register is latched. The first set of registers (the DAC input registers) are level triggered via the LOAD signal. This double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. When the new data has been entered into the

device, all of the DAC outputs can be updated simultaneously by the rising edge of LDAC. Additionally, it allows the DAC input registers to be written to at any point, then the DAC output voltages can be synchronously changed via a trigger signal (LDAC).

Note that CS and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when CS rises at the end of a serial transfer. If CLK is LOW when CS rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both CS and CLK are used, CS should rise only when CLK is HIGH. If not, then either CS or CLK can be used to operate the shift register. See Table II for more information.

<u>CS</u> ⁽¹⁾	CLK ⁽¹⁾	<u>LOAD</u>	RST	SERIAL SHIFT REGISTER
H ⁽²⁾	X ⁽³⁾	H	H	No Change
L ⁽⁴⁾	L	H	H	No Change
L	↑ ⁽⁵⁾	H	H	Advanced One Bit
↑	L	H	H	Advanced One Bit
H ⁽⁶⁾	X	L ⁽⁷⁾	H	No Change
H ⁽⁶⁾	X	H	↑ ⁽⁸⁾	No Change

NOTES: (1) CS and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a “false clock” from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while LOAD is LOW, the selected DAC register will change as the shift register bits “flow” through A1 and A0. This will corrupt the data in each DAC register that has been erroneously selected. (8) Rising edge of RST causes no change in the contents of the serial shift register.

TABLE II. Serial Shift Register Truth Table.

SERIAL DATA INPUT

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	QUICK LOAD	X	X	X	X	X	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A1	A0	<u>CS</u>	RST	RSTSEL	LDAC	<u>LOAD</u>	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	H	X	X	L	Write	Hold	Write Input	A
L	H	L	H	X	X	L	Write	Hold	Write Input	B
H	L	L	H	X	X	L	Write	Hold	Write Input	C
H	H	L	H	X	X	L	Write	Hold	Write Input	D
X	X	H	H	X	↑	H	Hold	Write	Update	All
X	X	H	H	X	H	H	Hold	Hold	Hold	All
X	X	X	↑	L	X	X	Reset to Zero	Reset to Zero	Reset to Zero	All
X	X	X	↑	H	X	X	Reset to Midscale	Reset to Midscale	Reset to Midscale	All

TABLE I. DAC7734 Logic Truth Table.

SERIAL-DATA OUTPUT

The Serial-Data Output (SDO) is the internal shift register output. For DAC7734, the SDO is a driven output and does not require an external pull-up. Any number of DAC7734s can be daisy-chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 11.

DIGITAL TIMING

Figure 12 and Table III provide detailed timing for the digital interface of the DAC7734.

DIGITAL INPUT CODING

The DAC7734 input data is in Straight Binary format. The output voltage is given by Equation 1.

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \cdot N}{65,536} \quad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7734 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7734 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally-programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REFH} - V_{REFL}}{R_{SENSE}} \right) \cdot \left(\frac{N}{65,536} \right) \right) + \left(V_{REFL} / R_{SENSE} \right) \quad (2)$$

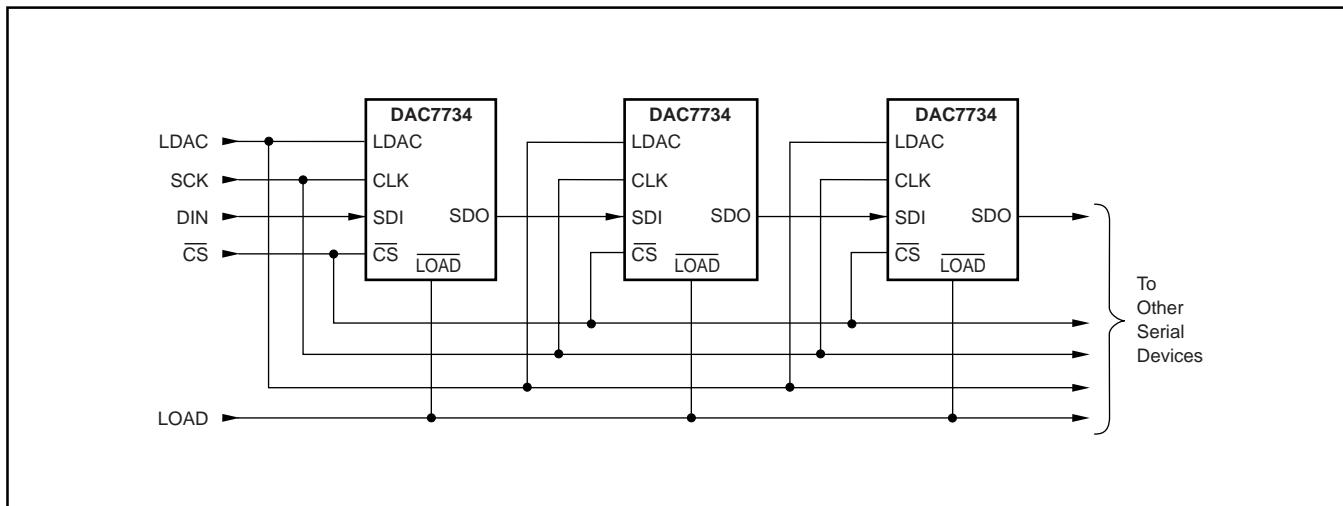


FIGURE 11. Daisy-Chaining DAC7734.

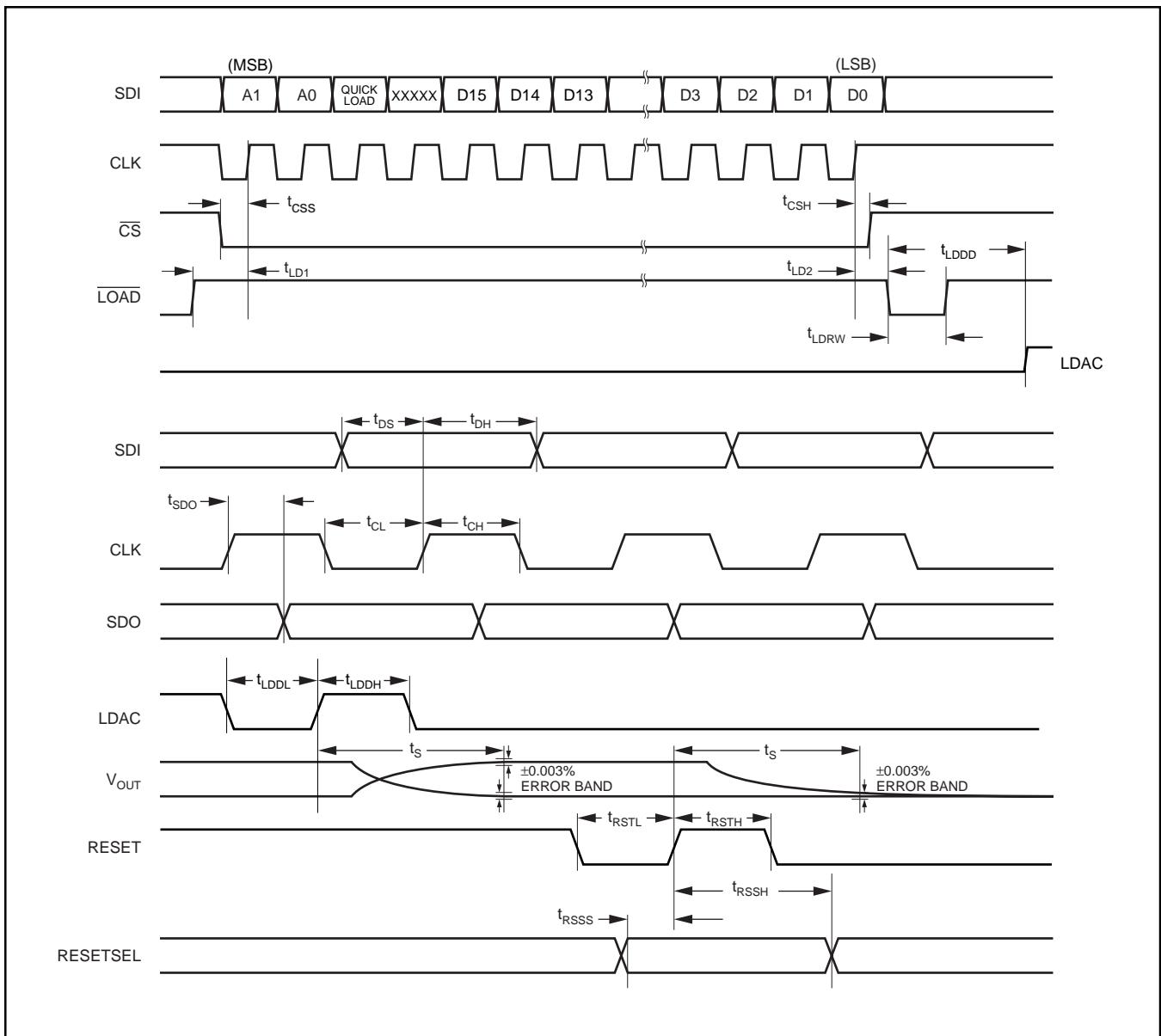


FIGURE 12. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{DS}	Data Valid to CLK Rising	10		ns
t_{DH}	Data Held Valid after CLK Rises	20		ns
t_{CH}	CLK HIGH	25		ns
t_{CL}	CLK LOW	25		ns
t_{CSS}	\overline{CS} LOW to CLK Rising	15		ns
t_{CSH}	CLK HIGH to \overline{CS} Rising	0		ns
t_{LD1}	LOAD HIGH to CLK Rising	10		ns
t_{LD2}	CLK Rising to LOAD LOW	30		ns
t_{LDRW}	LOAD LOW Time	30		ns
t_{LDDL}	LDAC LOW Time	40		ns
t_{LDDH}	LDAC HIGH Time	40		ns
t_{SDO}	SDO Propagation Delay	10		ns
t_{RSSS}	RESETSEL Valid to RESET HIGH	0	45	ns
t_{RSCH}	RESET HIGH to RESETSEL Not Valid	100		ns
t_{RSTL}	RESET LOW Time	10		ns
t_{RSTH}	RESET HIGH Time	10		ns
t_{LDDD}	LOAD LOW to LDAC Rising Time	40		ns
t_s	Settling Time		11 (dual)/10(single)	μs

TABLE III. Timing Specifications ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$).

Figure 13 shows a DAC7734 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{5V - 1V}{250\Omega} \right) \cdot \left(\frac{N}{65,536} \right) \right) + \left(\frac{1V}{250\Omega} \right) \quad (3)$$

At full-scale, the output current is 16mA, plus the 4mA, for the zero current. At zero scale, the output current is the offset current of 4mA (1V/250Ω).

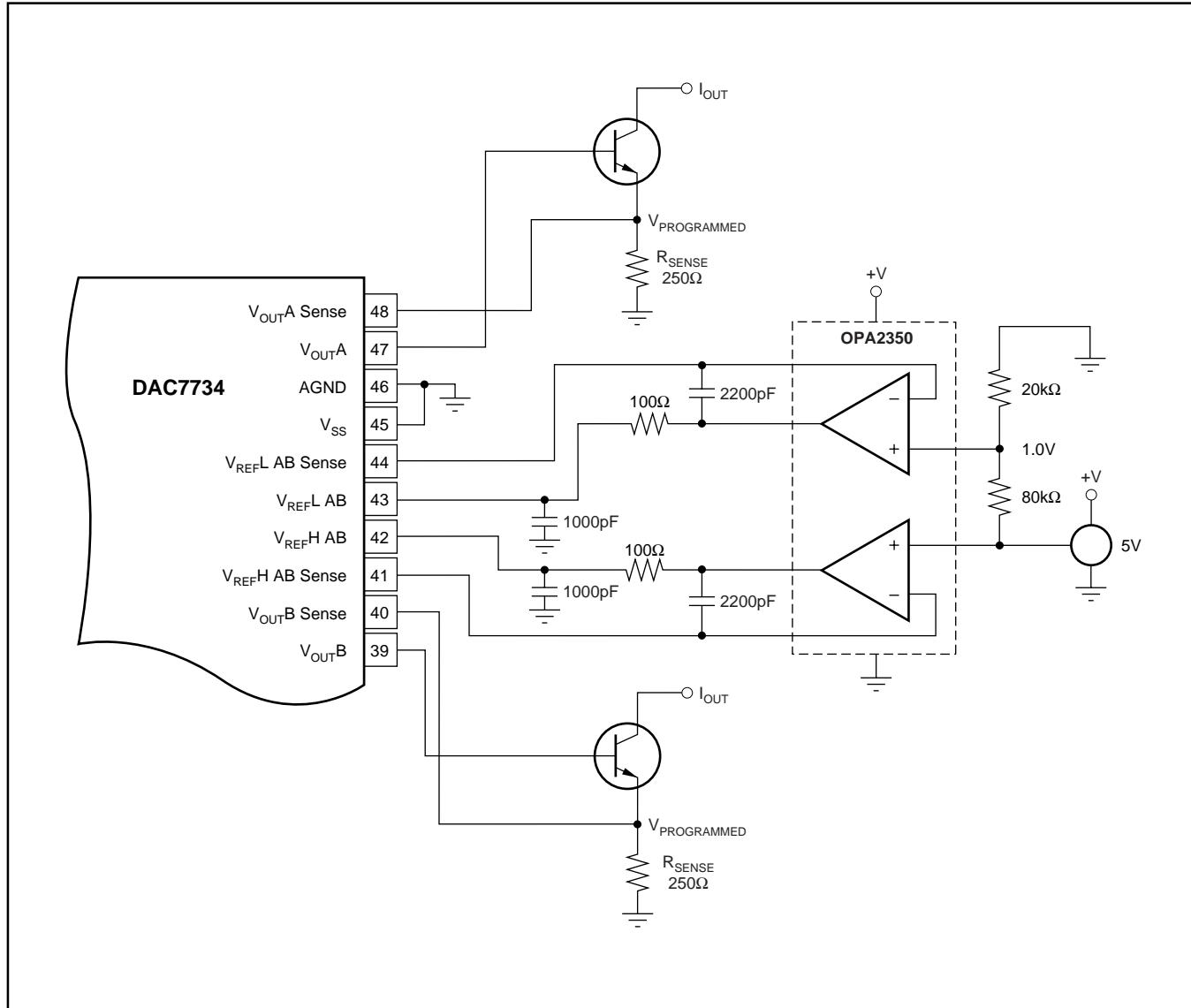


FIGURE 13. 4-to-20mA Digitally Controlled Current Source (1/2 DAC7734).

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
10/08	A	1	—	Updated front page format to current standard; some page layout changed.
		23	Table III	Changed symbol from " t_{LDDWL} " to " t_{LDDL} " (typo).

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7734E	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E	Samples
DAC7734E/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E	Samples
DAC7734EB	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E B	Samples
DAC7734EC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E C	Samples
DAC7734EC/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E C	Samples
DAC7734EG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

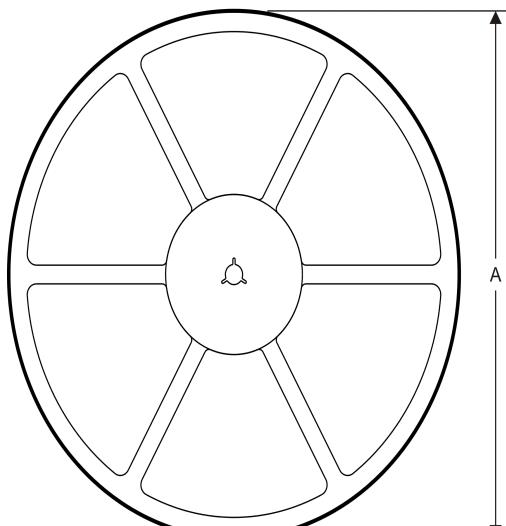
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

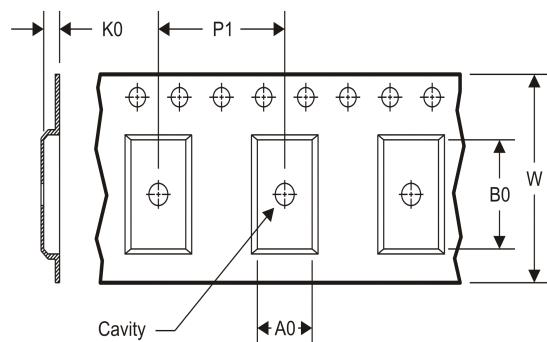
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

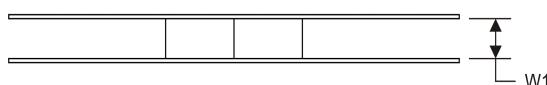
REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7734E/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
DAC7734EC/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

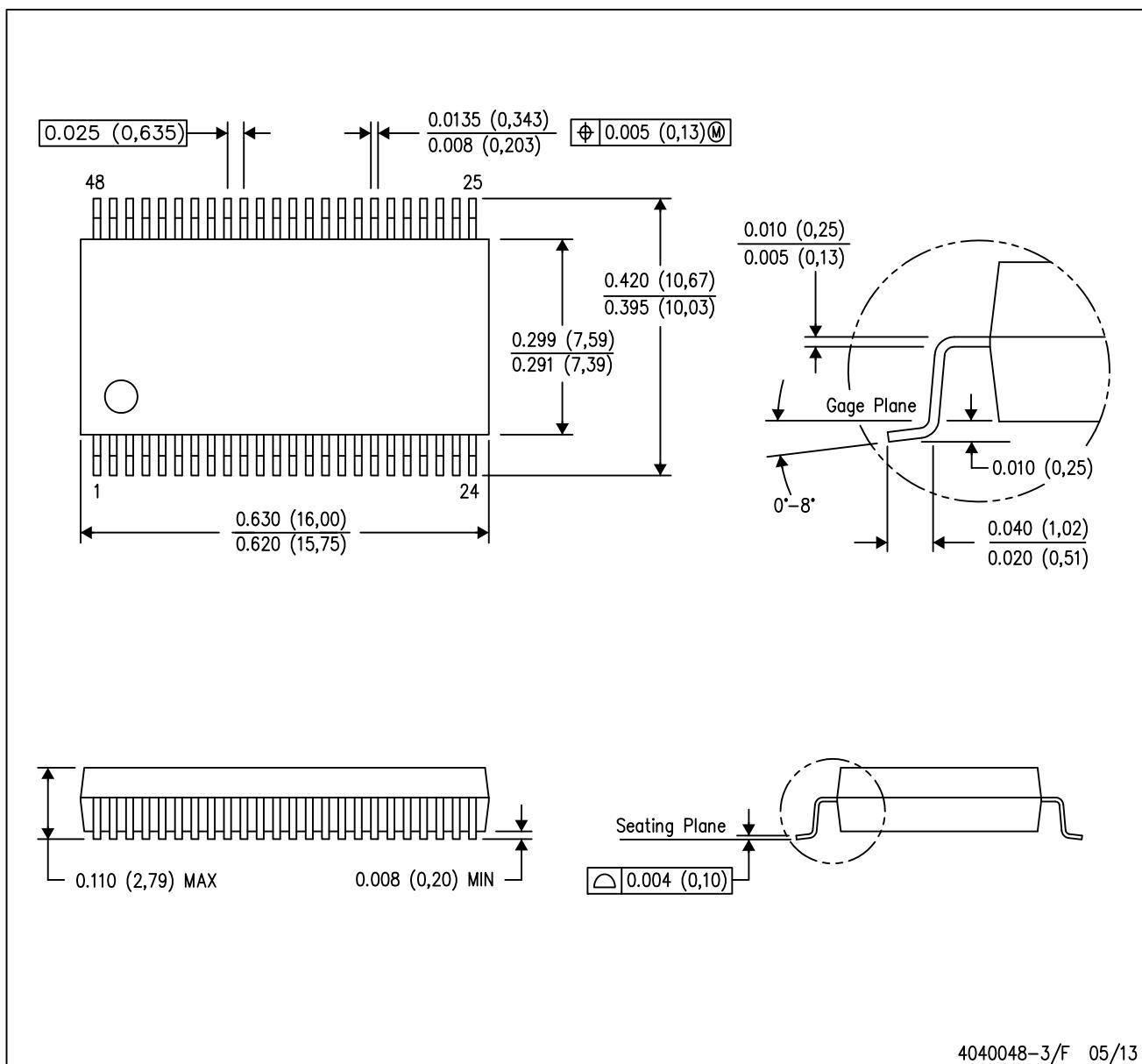
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7734E/1K	SSOP	DL	48	1000	367.0	367.0	55.0
DAC7734EC/1K	SSOP	DL	48	1000	367.0	367.0	55.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.