

## PMIC FOR E Ink® Vizplex™ ENABLED ELECTRONIC PAPER DISPLAY

Check for Samples: [TPS65180](#), [TPS65181](#), [TPS65180B](#), [TPS65181B](#)

### FEATURES

- Single Chip Power Management Solution for E Ink® Vizplex™ Electronic Paper Displays
- Generates Positive and Negative Gate and Source Driver Voltages and Back-Plane Bias from a Single, Low-Voltage Input Supply
- 3-V to 6-V Input Voltage Range
- Boost Converter for Positive Rail Base
- Inverting Buck-Boost Converter for Negative Rail Base
- Two Adjustable LDOs for Source Driver Supply
  - LDO1: 15 V, 120 mA (VPOS)
  - LDO2: –15 V, 120 mA (VNEG)
- Accurate Output Voltage Tracking
  - VPOS - VNEG = ±50 mV
- Two Charge Pumps for Gate Driver Supply
  - CP1: 22 V, 10 mA (VDDH)
  - CP2: –20 V, 12 mA, (VEE)
- Adjustable VCOM Driver for Accurate Panel-Backplane Biasing
  - –0.3 V to –2.5 V
  - ±1.5% Accuracy (±18 mV)
  - 8-Bit Control (11-mV Nominal Step Size)
  - 15-mA Max Integrated Switch
- Integrated 3.3-V Power Switch for Disabling System Power Rail

- Thermistor Monitoring
  - –10°C to 85°C Temperature Range
  - ±1°C Accuracy from 0°C to 50°C
- I<sup>2</sup>C Serial Interface
  - Slave Address 0x48h (1001000)
- Flexible Power-Up Sequencing
- Interrupt and Sleep Mode Support
- Thermally Enhanced Package for Efficient Heat Management  
(48-Pin 7 mm x 7 mm x 0.9 mm QFN)

### APPLICATIONS

- Power Supply for Active Matrix E Ink® Vizplex™ Panels
- EPD Power Supply
- E-Book Readers
- EPSON® S1D13522 (ISIS) Timing Controller
- EPSON® S1D13521 (Broadsheet) Timing Controller
- Application Processors With Integrated or Software Timing Controller ( OMAP™ )

### DESCRIPTION

The TPS65180/TPS65181 and TPS65180B/TPS65181B family of devices are single-chip power supplies designed to for E Ink® Vizplex™ displays used in portable e-reader applications and support panel sizes up to 9.7 inches. Two high efficiency DC/DC boost converters generate ±17-V rails which are boosted to 22 V and –20 V by two charge pumps to provide the gate driver supply for the Vizplex™ panel. Two tracking LDOs create the ±15-V source driver supplies which support up to 120-mA of output current. All rails are adjustable through the I<sup>2</sup>C interface to accommodate specific panel requirements.

Accurate back-plane biasing is provided by a linear amplifier and can be adjusted either by an external resistor or the I<sup>2</sup>C interface. The VCOM driver can source or sink current depending on panel condition. For automatic VCOM adjustment in production line, VCOM can be set from –0.3 V to –2.5 V with 8-bit control through the serial interface. The power switch is integrated to isolate VCOM driver from E Ink® panel.



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Vizplex is a trademark of E Ink Corporation.

E Ink is a registered trademark of E Ink Corporation.

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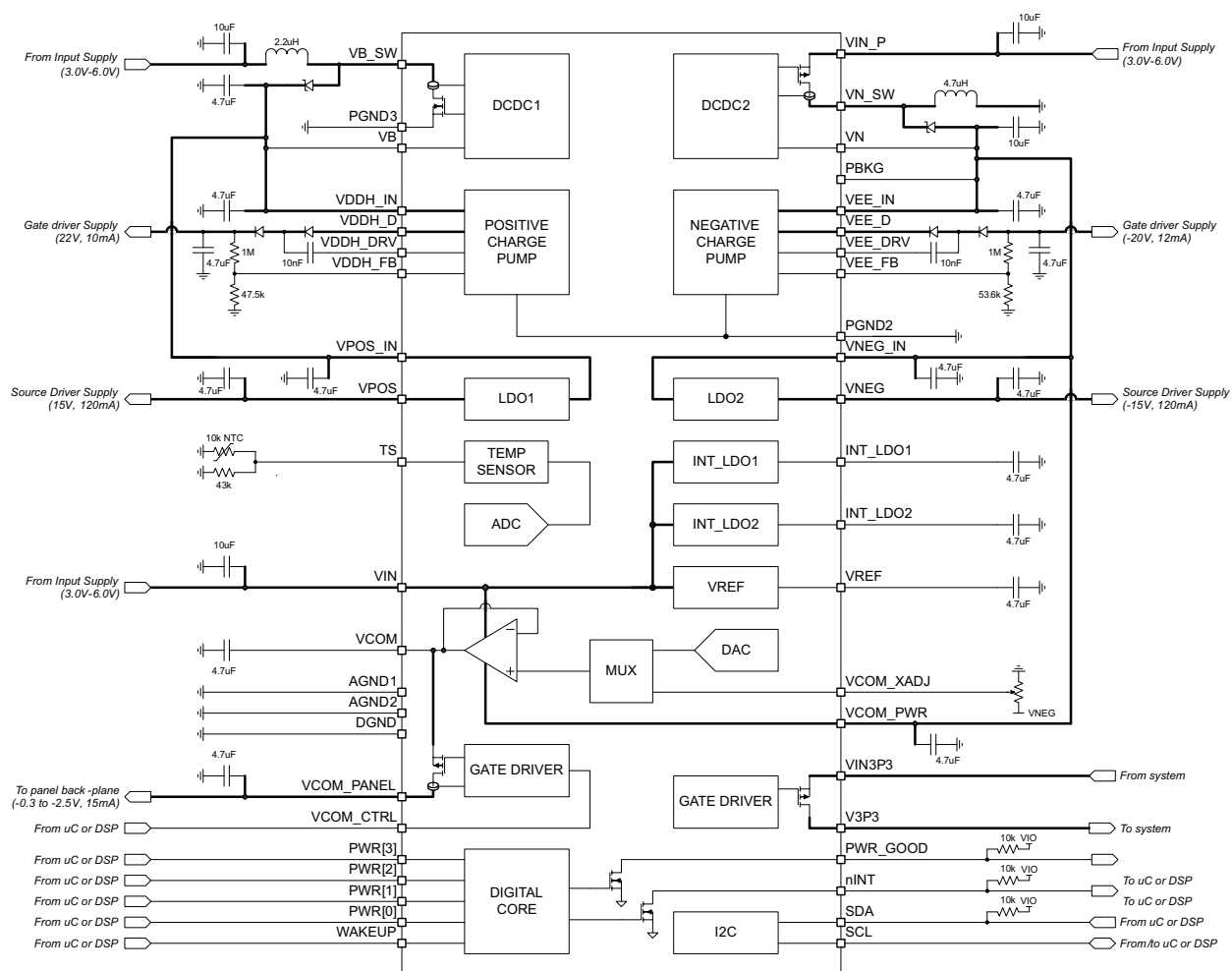
The TPS65180/TPS65181 and TPS65180B/TPS65181B devices provide precise temperature measurement function to monitor the panel temperature during operation. The TPS65180/TPS65180B requires the host processor to trigger the temperature acquisition through an I<sup>2</sup>C write whereas the TPS65181/TPS65181B automatically updates the temperature every 60 s.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## FUNCTIONAL BLOCK DIAGRAM



**ORDERING INFORMATION<sup>(1)</sup>**

| T <sub>A</sub> | PACKAGE <sup>(2)</sup> | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|-----------------------|------------------|
| -10°C to 85°C  | RGZ                    | TPS65180RGZR          | TPS65180         |
|                |                        | TPS65181RGZR          | TPS65181         |
|                |                        | TPS65180BRGZR         | TPS65180B        |
|                |                        | TPS65181BRGZR         | TPS65181B        |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

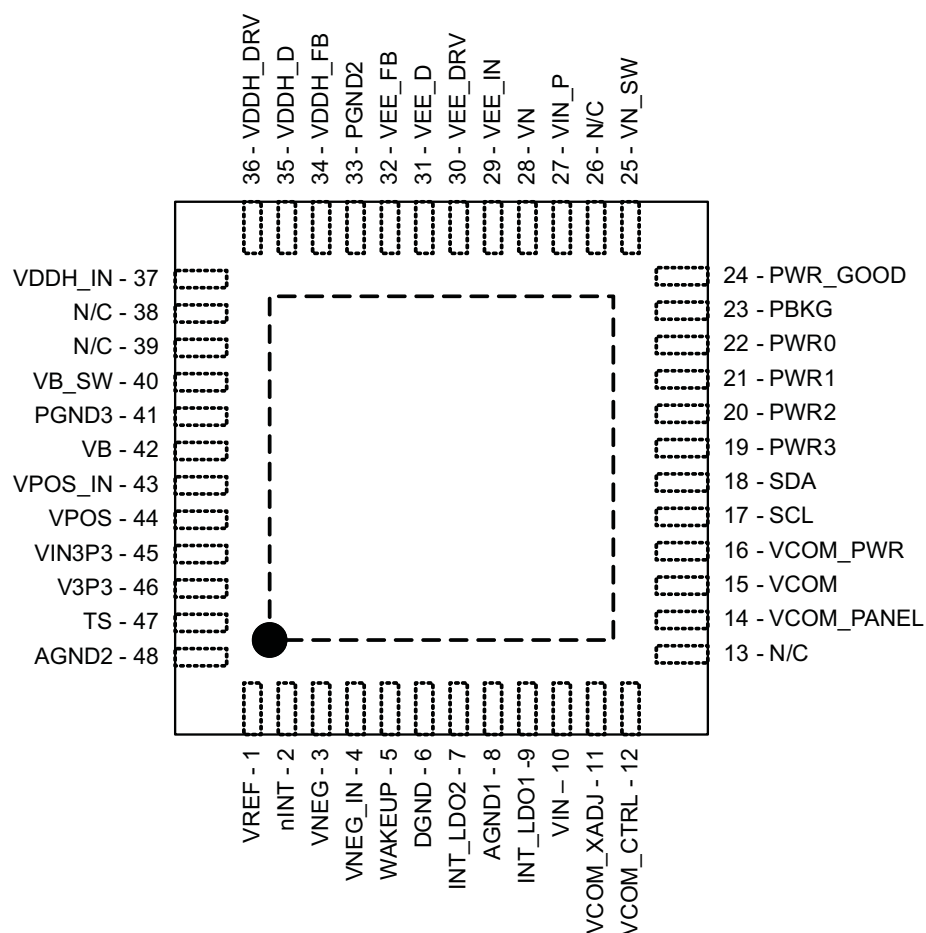
**SELECTION GUIDE**

| DEVICE    | PART NUMBER   | STATUS                          |
|-----------|---------------|---------------------------------|
| TPS65180  | TPS65180RGZR  | Not recommended for new designs |
| TPS65181  | TPS65181RGZR  | Not recommended for new designs |
| TPS65180B | TPS65180BRGZR | Active                          |
| TPS65181B | TPS65181BRGZR | Active                          |

| FUCNTION                   | TPS65180/TPS65180B                                                     | TPS65181/TPS65181B                                                                  |
|----------------------------|------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| Compatilbility             | EPSON ISIS (S1D113522)                                                 | EPSON ISIS (S1D113522)                                                              |
|                            |                                                                        | EPSON Broadsheet (S1D13521)                                                         |
|                            | OMAP                                                                   | OMAP                                                                                |
|                            | ST                                                                     | ST                                                                                  |
| Temperature sensor         | Triggered by host                                                      | Automatically triggers every 60 s                                                   |
| I <sup>2</sup> C interface | Standard                                                               | Supports standard and Broadsheet protocol                                           |
| Fault recovery             | INT register must be read before rails can be re-enabled after a fault | Interrupts are automatically reset when faults clear. No need to read INT register. |
| VCOM adjust default        | I <sup>2</sup> C control                                               | External potentiometer                                                              |

## DEVICE INFORMATION

### RGZ PACKAGE (TOP VIEW)



## TERMINAL FUNCTIONS<sup>(1)</sup>

| TERMINAL  |     | I/O | DESCRIPTION                                                                                                                |
|-----------|-----|-----|----------------------------------------------------------------------------------------------------------------------------|
| NAME      | NO. |     |                                                                                                                            |
| VREF      | 1   | O   | Filter pin for 2.25-V internal reference to ADC                                                                            |
| nINT      | 2   | O   | Open drain interrupt pin (active low)                                                                                      |
| VNEG      | 3   | O   | Negative supply output pin for panel source drivers                                                                        |
| VNEG_IN   | 4   | I   | Input pin for LDO2 (VNEG)                                                                                                  |
| WAKEUP    | 5   | I   | Wake up pin (active high). Pull this pin high to wake up from sleep mode.                                                  |
| DGND      | 6   |     | Digital ground                                                                                                             |
| INT_LDO2  | 7   | O   | Internal supply (digital circuitry) filter pin                                                                             |
| AGND1     | 8   |     | Analog ground for general analog circuitry                                                                                 |
| INT_LDO1  | 9   | O   | Internal supply (analog circuitry) filter pin                                                                              |
| VIN       | 10  | I   | Input power supply to general circuitry                                                                                    |
| VCOM_XADJ | 11  | I   | Analog input for conventional VCOM setup method. Tie this pin to ground if VCOM is set through I <sup>2</sup> C interface. |
| VCOM_CTRL | 12  | I   | VCOM_PANEL gate driver enable (active high)                                                                                |
| N/C       | 13  |     | Not connected                                                                                                              |

(1) There will be 0-ns, 93.75-μs, 62.52-μs of deglitch for PWRx, WAKEUP, and VCOM\_CTRL, respectively.

| TERMINAL        |     | I/O | DESCRIPTION                                                                                                                                                 |
|-----------------|-----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME            | NO. |     |                                                                                                                                                             |
| VCOM_PANEL      | 14  | O   | Panel common-voltage output pin                                                                                                                             |
| VCOM            | 15  | O   | Filter pin for panel common-voltage driver                                                                                                                  |
| VCOM_PWR        | 16  | I   | Internal supply input pin to VCOM buffer. Connect to the output of DCDC2.                                                                                   |
| SCL             | 17  | I   | Serial interface (I <sup>2</sup> C) clock input                                                                                                             |
| SDA             | 18  | I/O | Serial interface (I <sup>2</sup> C) data input/output                                                                                                       |
| PWR3            | 19  | I   | Enable pin for CP1 (VDDH) (active high)                                                                                                                     |
| PWR2            | 20  | I   | Enable pin for LDO1 (VPOS) (active high)                                                                                                                    |
| PWR1            | 21  | I   | Enable pin for CP2 (VEE) (active high)                                                                                                                      |
| PWR0            | 22  | I   | Enable pin for LDO2 (VNEG) and VCOM (active high)                                                                                                           |
| PWR_GOOD        | 24  | O   | Open drain power good output pin (active low)                                                                                                               |
| VN_SW           | 25  | O   | Inverting buck-boost converter switch out (DCDC2)                                                                                                           |
| N/C             | 26  |     | Not connected                                                                                                                                               |
| VIN_P           | 27  | I   | Input power supply to inverting buck-boost converter (DCDC2)                                                                                                |
| VN              | 28  | I   | Feedback pin for inverting buck-boost converter (DCDC2)                                                                                                     |
| VEE_IN          | 29  | I   | Input supply pin for CP1 (VEE)                                                                                                                              |
| VEE_DRV         | 30  | O   | Driver output pin for negative charge pump (CP2)                                                                                                            |
| VEE_D           | 31  | O   | Base voltage output pin for negative charge pump (CP2)                                                                                                      |
| VEE_FB          | 32  | I   | Feedback pin for negative charge pump (CP2)                                                                                                                 |
| PGND2           | 33  |     | Power ground for CP1 (VDDH) and CP2 (VEE) charge pumps                                                                                                      |
| VDDH_FB         | 34  | I   | Feedback pin for positive charge pump (CP1)                                                                                                                 |
| VDDH_D          | 35  | O   | Base voltage output pin for positive charge pump (CP1)                                                                                                      |
| VDDH_DRV        | 36  | O   | Driver output pin for positive charge pump (CP1)                                                                                                            |
| VDDH_IN         | 37  | I   | Input supply pin for positive charge pump (CP1)                                                                                                             |
| N/C             | 38  |     | Not connected                                                                                                                                               |
| N/C             | 39  |     | Not connected                                                                                                                                               |
| VB_SW           | 40  | O   | Boost converter switch out (DCDC1)                                                                                                                          |
| PGND3           | 41  |     | Power ground for DCDC1                                                                                                                                      |
| VB              | 42  | I   | Feedback pin for boost converter (DCDC1)                                                                                                                    |
| VPOS_IN         | 43  | I   | Input pin for LDO1 (VPOS)                                                                                                                                   |
| VPOS            | 44  | O   | Positive supply output pin for panel source drivers                                                                                                         |
| VIN3P3          | 45  | I   | Input pin to 3.3-V power switch                                                                                                                             |
| V3P3            | 46  | O   | Output pin of 3.3-V power switch                                                                                                                            |
| TS              | 47  | I   | Thermistor input pin. Connect a 10k NTC thermistor and a 43k linearization resistor between this pin and AGND2.                                             |
| AGND2           | 48  |     | Reference point to external thermistor and linearization resistor                                                                                           |
| PowerPad (PBKG) | 23  |     | Die substrate/thermal pad. Connect to VN with short, wide trace. Wide copper trace will improve heat dissipation. PowerPad must not be connected to ground. |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)</sup>

|                                                                                                       | VALUE                      | UNIT  |
|-------------------------------------------------------------------------------------------------------|----------------------------|-------|
| Input voltage range at VIN, VINP, VIN3P3                                                              | –0.3 to 7                  | V     |
| Ground pins to system ground                                                                          | –0.3 to 0.3                | V     |
| Voltage range at SDA, SCL, WAKEUP, PWR3, PWR2, PWR1, PWR0, VCOM_CTRL, VDDH_FB, VEE_FB, PWR_GOOD, nINT | –0.3 to 3.6                | V     |
| VCOM_XADJ                                                                                             | –3.6 to 0.3                | V     |
| Voltage on VB, VB_SW, VPOS_IN, VDDH_IN                                                                | –0.3 to 20                 | V     |
| Voltage on VN, VNEG_IN, VEE_IN, VCOM_PWR                                                              | –20 to 0.3                 | V     |
| Voltage from VINP to VN_SW                                                                            | –0.3 to 30                 | V     |
| Peak output current                                                                                   | Internally limited         | mA    |
| Continuous total power dissipation                                                                    | 2                          | W     |
| $\theta_{JA}$ Junction-to-ambient thermal resistance <sup>(3)</sup>                                   | 23                         | °C/W  |
| T <sub>J</sub> Operating junction temperature                                                         | –10 to 125                 | °C    |
| T <sub>A</sub> Operating ambient temperature <sup>(4)</sup>                                           | –10 to 85                  | °C    |
| T <sub>stg</sub> Storage temperature                                                                  | –65 to 150                 | °C    |
| ESD rating                                                                                            | (HBM) Human body model     | ±2000 |
|                                                                                                       | (CDM) Charged device model | ±500  |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Estimated when mounted on high K JEDEC board per JESD 51-7 with thickness of 1.6 mm, 4 layers, size of 76.2 mm X 114.3 mm, and 2 oz. copper for top and bottom plane. Actual thermal impedance will depend on PCB used in the application.
- (4) It is recommended that copper plane in proper size on board be in contact with die thermal pad to dissipate heat efficiently. Thermal pad is electrically connected to PBKG, which is supposed to be tied to the output of buck-boost converter. Thus wide copper trace in the buck-boost output will help heat dissipated efficiently.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|                                                                                                                  | MIN | NOM | MAX | UNIT |
|------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| Input voltage range at VIN, VINP, VIN3P3                                                                         | 3   | 3.7 | 6   | V    |
| Voltage range at SDA, SCL, WAKEUP, PWR3, PWR2, PWR1, PWR0, VCOM_CTRL, VDDH_FB, VEE_FB, VCOM_XADJ, PWR_GOOD, nINT | 0   |     | 3.6 | V    |
| T <sub>A</sub> Operating ambient temperature range                                                               | –10 |     | 85  | °C   |
| T <sub>J</sub> Operating junction temperature range                                                              | –10 |     | 125 | °C   |

## RECOMMENDED EXTERNAL COMPONENTS

| PART NUMBER        | VALUE                  | SIZE                   | MANUFACTURER |
|--------------------|------------------------|------------------------|--------------|
| <b>INDUCTORS</b>   |                        |                        |              |
| LQH44PN4R7MP0      | 4.7 $\mu$ H            | 4 mm x 4 mm x 1.65 mm  | Murata       |
| VLS252012T-2R2M1R3 | 2.2 $\mu$ H            | 2 mm x 2.5 mm x 1.2 mm | TDK          |
| <b>CAPACITORS</b>  |                        |                        |              |
| GRM21BC81E475KA12L | 4.7 $\mu$ F, 25 V, X6S | 805                    | Murata       |
| GRM32ER71H475KA88L | 4.7 $\mu$ F, 50 V, X7R | 1210                   | Murata       |
| All other caps     | X5R or better          |                        |              |
| <b>DIODES</b>      |                        |                        |              |
| BAS3010            |                        | SOD-323                | Infineon     |
| MBR130T1           |                        | SOD-123                | ON-Semi      |
| <b>THERMISTOR</b>  |                        |                        |              |
| NCP18XH103F03RB    | 10 kW                  | 603                    | Murata       |

## ELECTRICAL CHARACTERISTICS

 $V_{IN} = 3.7\text{ V}$ ,  $T_A = -10^\circ\text{C}$  to  $85^\circ\text{C}$ , Typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                     |                                           | TEST CONDITIONS                                                  | MIN   | TYP   | MAX   | UNIT             |
|-----------------------------------------------|-------------------------------------------|------------------------------------------------------------------|-------|-------|-------|------------------|
| <b>INPUT VOLTAGE</b>                          |                                           |                                                                  |       |       |       |                  |
| $V_{IN}$                                      | Input voltage range                       |                                                                  | 3     | 3.7   | 6     | V                |
| $V_{UVLO}$                                    | Undervoltage lockout threshold            | $V_{IN}$ falling                                                 |       | 2.9   |       | V                |
| $V_{HYS}$                                     | Undervoltage lockout hysteresis           | $V_{IN}$ rising                                                  |       | 400   |       | mV               |
| <b>INPUT CURRENT</b>                          |                                           |                                                                  |       |       |       |                  |
| $I_Q$                                         | Operating quiescent current into $V_{IN}$ | Device switching, no load                                        |       | 5.5   |       | mA               |
| $I_{STD}$                                     | Operating quiescent current into $V_{IN}$ | Device in standby mode                                           |       | 130   |       | $\mu\text{A}$    |
| $I_{SLEEP}$                                   | Shutdown current                          | Device in sleep mode                                             |       | 2.8   | 10    | $\mu\text{A}$    |
| <b>INTERNAL SUPPLIES</b>                      |                                           |                                                                  |       |       |       |                  |
| $V_{INT\_LDO1}$                               | Internal supply                           |                                                                  |       | 2.7   |       | V                |
| $V_{INT\_LDO2}$                               | Internal supply                           |                                                                  |       | 2.7   |       | V                |
| $V_{REF}$                                     | Internal supply                           |                                                                  |       | 2.25  |       | V                |
| <b>DCDC1 (POSITIVE BOOST REGULATOR)</b>       |                                           |                                                                  |       |       |       |                  |
| $V_{IN}$                                      | Input voltage range                       |                                                                  | 3     | 3.7   | 6     | V                |
| $V_{OUT}$                                     | Output voltage range                      |                                                                  |       | 17    |       | V                |
|                                               | DC set tolerance                          |                                                                  | -5    |       | 5     | %                |
| $I_{OUT}$                                     | Output current                            |                                                                  |       |       | 160   | mA               |
| $R_{DS(ON)}$                                  | MOSFET on resistance                      | $V_{IN} = 3.7\text{ V}$                                          |       | 350   |       | $\text{m}\Omega$ |
| $I_{LIMIT}$                                   | Switch current limit                      |                                                                  |       | 1.5   |       | A                |
|                                               | Switch current accuracy                   |                                                                  | -30   |       | 30    | %                |
| $f_{SW}$                                      | Switching frequency                       |                                                                  |       | 1     |       | MHz              |
| L                                             | Inductor                                  |                                                                  |       | 2.2   |       | $\mu\text{H}$    |
| C                                             | Capacitor                                 |                                                                  |       | 2x4.7 |       | $\mu\text{F}$    |
| ESR                                           | Capacitor ESR                             |                                                                  |       | 20    |       | $\text{m}\Omega$ |
| <b>DCDC2 (INVERTING BUCK-BOOST REGULATOR)</b> |                                           |                                                                  |       |       |       |                  |
| $V_{IN}$                                      | Input voltage range                       |                                                                  | 3     | 3.7   | 6     | V                |
| $V_{OUT}$                                     | Output voltage range                      |                                                                  |       | -17   |       | V                |
|                                               | DC set tolerance                          |                                                                  | -5    |       | 5     | %                |
| $I_{OUT}$                                     | Output current                            |                                                                  |       |       | 160   | mA               |
| $R_{DS(ON)}$                                  | MOSFET on resistance                      | $V_{IN} = 3.7\text{ V}$                                          |       | 350   |       | $\text{m}\Omega$ |
| $I_{LIMIT}$                                   | Switch current limit                      |                                                                  |       | 1.5   |       | A                |
|                                               | Switch current accuracy                   |                                                                  | -30   |       | 30    | %                |
| L                                             | Inductor                                  |                                                                  |       | 4.7   |       | $\mu\text{H}$    |
| C                                             | Capacitor                                 |                                                                  |       | 2x4.7 |       | $\mu\text{F}$    |
| ESR                                           | Capacitor ESR                             |                                                                  |       | 20    |       | $\text{m}\Omega$ |
| <b>LDO1 (VPOS)</b>                            |                                           |                                                                  |       |       |       |                  |
| $V_{POS\_IN}$                                 | Input voltage range                       |                                                                  | 16.15 | 17    | 17.85 | V                |
| $V_{SET}$                                     | Output voltage set value                  | $V_{IN} = 17\text{ V}$ ,<br>$V_{POS\_SET[2:0]} = 0x0h$ to $0x7h$ | 14.25 | 15    | 15.75 | V                |
| $V_{INTERVAL}$                                | Output voltage set resolution             | $V_{IN} = 17\text{ V}$                                           |       | 250   |       | mV               |
| $V_{POS\_OUT}$                                | Output voltage range                      | $V_{SET} = 15\text{ V}$ , $I_{LOAD} = 20\text{ mA}$              | 14.85 | 15    | 15.15 | V                |
| $V_{OUTTOL}$                                  | Output tolerance                          | $V_{SET} = 15\text{ V}$ , $I_{LOAD} = 20\text{ mA}$              | -1    |       | 1     | %                |
| $V_{DROPOUT}$                                 | Dropout voltage                           | $I_{LOAD} = 120\text{ mA}$                                       |       |       | 250   | mV               |
| $V_{LOADREG}$                                 | Load regulation – DC                      | $I_{LOAD} = 10\%$ to $90\%$                                      |       |       | 1     | %                |
| $I_{LOAD}$                                    | Load current range                        |                                                                  |       | 120   |       | mA               |

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 3.7\text{ V}$ ,  $T_A = -10^\circ\text{C}$  to  $85^\circ\text{C}$ , Typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                  |                                            | TEST CONDITIONS                                                                                                                                | MIN    | TYP | MAX    | UNIT          |
|--------------------------------------------|--------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|--------|---------------|
| $I_{LIMIT}$                                | Output current limit                       |                                                                                                                                                | 200    |     |        | mA            |
| $T_{SS}$                                   | Soft start time                            |                                                                                                                                                |        | 1   |        | ms            |
| C                                          | Recommended output capacitor               |                                                                                                                                                |        | 4.7 |        | $\mu\text{F}$ |
| <b>LDO2 (VNEG)</b>                         |                                            |                                                                                                                                                |        |     |        |               |
| $V_{NEG\_IN}$                              | Input voltage range                        |                                                                                                                                                | -17.85 | -17 | -16.15 | V             |
| $V_{SET}$                                  | Output voltage set value                   | $V_{IN} = -17\text{ V}$ ,<br>$V_{NEG\_SET[2:0]} = 0x0h$ to $0x7h$                                                                              | -15.75 | -15 | -14.25 | V             |
| $V_{INTERVAL}$                             | Output voltage set resolution              | $V_{IN} = -17\text{ V}$                                                                                                                        |        | 250 |        | mV            |
| $V_{NEG\_OUT}$                             | Output voltage range                       | $V_{SET} = -15\text{ V}$ , $I_{LOAD} = -20\text{ mA}$                                                                                          | -15.15 | -15 | -14.85 | V             |
| $V_{OUTTOL}$                               | Output tolerance                           | $V_{SET} = -15\text{ V}$ , $I_{LOAD} = -20\text{ mA}$                                                                                          | -1     |     | 1      | %             |
| $V_{DROPOUT}$                              | Dropout voltage                            | $I_{LOAD} = 120\text{ mA}$                                                                                                                     |        |     | 250    | mV            |
| $V_{LOADREG}$                              | Load regulation – DC                       | $I_{LOAD} = 10\%$ to $90\%$                                                                                                                    |        |     | 1      | %             |
| $I_{LOAD}$                                 | Load current range                         |                                                                                                                                                |        | 120 |        | mA            |
| $I_{LIMIT}$                                | Output current limit                       |                                                                                                                                                | 200    |     |        | mA            |
| $T_{SS}$                                   | Soft start time                            |                                                                                                                                                |        | 1   |        | ms            |
| C                                          | Recommended output capacitor               |                                                                                                                                                |        | 4.7 |        | $\mu\text{F}$ |
| <b>LD01 (POS) AND LDO2 (VNEG) TRACKING</b> |                                            |                                                                                                                                                |        |     |        |               |
| $V_{DIFF}$                                 | Difference between VPOS and VNEG           | $V_{SET} = \pm 15\text{ V}$ ,<br>$I_{LOAD} = \pm 20\text{ mA}$ , $0^\circ\text{C}$ to $60^\circ\text{C}$                                       | -50    |     | 50     | mV            |
| <b>VCOM DRIVER</b>                         |                                            |                                                                                                                                                |        |     |        |               |
| $V_{COM}$                                  | Accuracy                                   | $V_{COM\_SET[7:0]} = 0x74h$ ( $-1.25\text{ V}$ )<br>$V_{IN} = 3.4\text{ V}$ to $4.2\text{ V}$ , no load                                        | -0.8   |     | 0.8    | %             |
|                                            |                                            | $V_{COM\_SET[7:0]} = 0x74h$ ( $-1.25\text{ V}$ )<br>$V_{IN} = 3.0\text{ V}$ to $6.0\text{ V}$ , no load                                        | -1.5   |     | 1.5    |               |
|                                            | Output voltage range                       |                                                                                                                                                | -2.5   |     | -0.3   | V             |
|                                            | Resolution                                 | $V_{COM\_ADJ} = 1\text{ V}$ , 1 LSB                                                                                                            |        | 11  | 17     | mV            |
| G                                          | $V_{COM}$ gain ( $V_{COM\_XADJ}/V_{COM}$ ) | $V_{COM\_ADJ} = 0\text{ V}$                                                                                                                    |        | 1   |        | V/V           |
| <b>VCOM SWITCH</b>                         |                                            |                                                                                                                                                |        |     |        |               |
| $T_{ON}$                                   | Switch ON time                             | $V_{COM} = -1.25\text{ V}$ , $V_{COM\_PANEL} = 0\text{ V}$<br>$C_{VCOM} = 4.7\text{ }\mu\text{F}$ , $C_{VCOM\_PANEL} = 4.7\text{ }\mu\text{F}$ |        |     | 1      | ms            |
| $R_{DS(ON)}$                               | MOSFET ON resistance                       | $V_{COM} = -1.245\text{ V}$ , $I_{COM} = 30\text{ mA}$                                                                                         |        | 20  | 35     | $\Omega$      |
| $I_{LIMIT}$                                | MOSFET current limit                       | Not tested in production                                                                                                                       |        | 200 |        | mA            |
| $I_{SWLEAK}$                               | Switch leakage current                     | $V_{COM} = 0\text{ V}$ ,<br>$V_{COM\_PANEL} = -2.5\text{ V}$                                                                                   |        |     | 8.3    | nA            |
| <b>VIN3P3 TO V3P3 SWITCH</b>               |                                            |                                                                                                                                                |        |     |        |               |
| $R_{DS(ON)}$                               | MOSFET ON resistance                       | $V_{IN3P3} = 3.3\text{ V}$ , $I_D = 2\text{ mA}$                                                                                               |        | 50  |        | $\Omega$      |
| <b>CP1 (VDDH) CHARGE PUMP</b>              |                                            |                                                                                                                                                |        |     |        |               |
| $V_{DDH\_IN}$                              | Input voltage range                        |                                                                                                                                                | 16.15  | 17  | 17.85  | V             |
| $V_{FB}$                                   | Feedback voltage                           |                                                                                                                                                |        | 1   |        | V             |
|                                            | Accuracy                                   |                                                                                                                                                | -3     |     | 3      | %             |
| $V_{DDH\_OUT}$                             | Output voltage range                       | $V_{SET} = 22\text{ V}$ , $I_{LOAD} = 2\text{ mA}$                                                                                             | 21     | 22  | 23     | V             |
| $I_{LOAD}$                                 | Load current range                         |                                                                                                                                                |        |     | 10     | mA            |
| $f_{SW}$                                   | Switching frequency                        |                                                                                                                                                |        | 560 |        | KHz           |
| $C_D$                                      | Recommended driver capacitor               |                                                                                                                                                |        | 10  |        | nF            |
| $C_O$                                      | Recommended output capacitor               |                                                                                                                                                |        | 4.7 |        | $\mu\text{F}$ |
| <b>CP2 (VEE) NEGATIVE CHARGE PUMP</b>      |                                            |                                                                                                                                                |        |     |        |               |
| $V_{EE\_IN}$                               | Input voltage range                        |                                                                                                                                                | -17.75 | -17 | -16.15 | V             |

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 3.7\text{ V}$ ,  $T_A = -10^\circ\text{C}$  to  $85^\circ\text{C}$ , Typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                                                               |                                                    | TEST CONDITIONS                                             | MIN | TYP     | MAX | UNIT                |
|-----------------------------------------------------------------------------------------|----------------------------------------------------|-------------------------------------------------------------|-----|---------|-----|---------------------|
| $V_{FB}$                                                                                | Feedback voltage                                   |                                                             |     | -1      |     | V                   |
|                                                                                         | Accuracy                                           |                                                             | -3  |         | 3   | %                   |
| $V_{EE\_OUT}$                                                                           | Output voltage range                               | $V_{SET} = -20\text{ V}$ , $I_{LOAD} = 3\text{ mA}$         | -21 | -20     | -19 | V                   |
| $I_{LOAD}$                                                                              | Load current range                                 |                                                             |     |         | 12  | mA                  |
| $f_{SW}$                                                                                | Switching frequency                                |                                                             |     | 560     |     | KHz                 |
| $C_D$                                                                                   | Recommended driver capacitor                       |                                                             |     | 10      |     | nF                  |
| $C_O$                                                                                   | Recommended output capacitor                       |                                                             |     | 4.7     |     | $\mu\text{F}$       |
| <b>THERMISTOR MONITOR<sup>(1)</sup></b>                                                 |                                                    |                                                             |     |         |     |                     |
| $A_{TMS}$                                                                               | Temperature to voltage ratio                       | Not tested in production                                    |     | -0.0158 |     | V/ $^\circ\text{C}$ |
| Offset <sub>TMS</sub>                                                                   | Offset                                             | Temperature = $0^\circ\text{C}$                             |     | 1.575   |     | V                   |
| $V_{TMS\_HOT}$                                                                          | Temp hot trip voltage ( $T = 50^\circ\text{C}$ )   | TEMP_HOT_SET = 0x8C                                         |     | 0.768   |     | V                   |
| $V_{TMS\_COOL}$                                                                         | Temp hot escape voltage ( $T = 45^\circ\text{C}$ ) | TEMP_COOL_SET = 0x82                                        |     | 0.845   |     | V                   |
| $V_{TMS\_MAX}$                                                                          | Maximum input level                                |                                                             |     | 2.25    |     | V                   |
| $R_{NTC\_PU}$                                                                           | Internal pull up resistor                          |                                                             |     | 7.307   |     | K $\Omega$          |
| $R_{LINEAR}$                                                                            | External linearization resistor                    |                                                             |     | 43      |     | K $\Omega$          |
| ADC <sub>RES</sub>                                                                      | ADC resolution                                     | Not tested in production, 1 bit                             |     | 8.75    |     | mV                  |
| ADC <sub>DEL</sub>                                                                      | ADC conversion time                                | Not tested in production                                    |     | 19      |     | $\mu\text{s}$       |
| TMST <sub>TOL</sub>                                                                     | Accuracy                                           | Not tested in production                                    | -2  |         | 2   | LSB                 |
| <b>LOGIC LEVELS AND TIMING CHARACTERISTICS (SCL, SDA, nINT, PWR_GOOD, PWRx, WAKEUP)</b> |                                                    |                                                             |     |         |     |                     |
| $V_{OL}$                                                                                | Output low threshold level                         | $I_O = 3\text{ mA}$ , sink current<br>(SDA, nINT, PWR_GOOD) |     |         | 0.4 | V                   |
| $V_{IL}$                                                                                | Input low threshold level                          |                                                             |     |         | 0.4 | V                   |
| $V_{IH}$                                                                                | Input high threshold level                         |                                                             | 1.2 |         |     | V                   |
| $I_{(bias)}$                                                                            | Input bias current                                 | $V_{IO} = 1.8\text{ V}$                                     |     |         | 1   | $\mu\text{A}$       |
| $t_{low\_WAKEUP}$                                                                       | WAKEUP low time                                    | minimum low time for WAKEUP pin                             | 150 |         |     | ms                  |
| $f_{SCL}$                                                                               | SCL clock frequency                                |                                                             |     |         | 400 | KHz                 |
| <b>OSCILLATOR</b>                                                                       |                                                    |                                                             |     |         |     |                     |
| $f_{OSC}$                                                                               | Oscillator frequency                               |                                                             |     | 9       |     | MHz                 |
|                                                                                         | Frequency accuracy                                 | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$             | -10 |         | 10  | %                   |
| <b>THERMAL SHUTDOWN</b>                                                                 |                                                    |                                                             |     |         |     |                     |
| $T_{SHTDWN}$                                                                            | Thermal trip point                                 |                                                             |     | 150     |     | $^\circ\text{C}$    |
|                                                                                         | Thermal hysteresis                                 |                                                             |     | 20      |     | $^\circ\text{C}$    |

(1) 10-k $\Omega$  Murata NCP18XH103F03RB thermistor (1%) in parallel with a linearization resistor (43k $\Omega$ , 1%) are used at TS pin for panel temperature measurement.

## MODES OF OPERATION

The TPS65180/TPS65181 and TPS65180B/TPS65181B have three modes of operation, SLEEP, STANDBY, and ACTIVE. SLEEP mode is the lowest-power mode in which all internal circuitry is turned off. In STANDBY, all power rails are shut down but the device is ready to accept commands through PWR[3:0] pins and/or I<sup>2</sup>C interface. In ACTIVE mode one or more power rails are enabled.

### SLEEP

This is the lowest power mode of operation. All internal circuitry is turned off, registers are reset to default values and the device does not respond to I<sup>2</sup>C communications.

TPS65180/TPS65181 and TPS65180B/TPS65181B enter SLEEP mode whenever WAKEUP pin is pulled low.

### STANDBY

In STANDBY all internal support circuitry is powered up and the device is ready to accept commands either through GPIO or I<sup>2</sup>C control but none of the power rails are enabled. To enter STANDBY mode the WAKEUP pin must be pulled high and all PWRx pins must be pulled low or the STANDBY bit of the ENABLE register must be set high. The device also enters STANDBY mode if input under voltage lock out (UVLO), positive boost under voltage (VB\_UV), or inverting buck-boost under voltage (VN\_UV) is detected, or thermal shutdown occurs.

### ACTIVE

The device is in ACTIVE mode when any of the output rails are enabled and no fault condition is present. This is the normal mode of operation while the device is powered up. In ACTIVE mode, a falling edge on any PWRx pin shuts down and a rising edge powers up the corresponding rail.

## MODE TRANSITIONS

### SLEEP → ACTIVE

WAKEUP pin is pulled high (rising edge) with any PWRx pin high. Rails come up in the order defined by the PWR\_SEQx registers.

### SLEEP → STANDBY

WAKEUP pin is pulled high (rising edge) with all PWRx pins low. Rails will remain down until one or more PWRx pin is pulled high.

### ACTIVE → SLEEP

WAKEUP pin is pulled low (falling edge). Rails are shut down in the reverse power-up order defined by PWR\_SEQ registers.

### ACTIVE → STANDBY

WAKEUP pin is high. All PWRx pins are pulled low (falling edge). Rails shut down in the order in which PWRx pins are pulled low. In the event of thermal shut down (TSD), under voltage lock out (UVLO), positive boost or inverting buck-boost under voltage (UV), or when STANDBY bit is set to 1, the device shuts down all rails in the reverse power-up order defined by the PWR\_SEQx registers.

### STANDBY → ACTIVE

WAKEUP pin is high and any PWRx pin is pulled high (rising edge). Rails come up in the same order as PWRx pins are pulled high. Alternatively, if ACTIVE bit is set to 1, output rails will power up in the order defined by the PWR\_SEQx registers.

### STANDBY → SLEEP

WAKEUP pin is pulled low (falling edge) while none of the output rails are enabled.

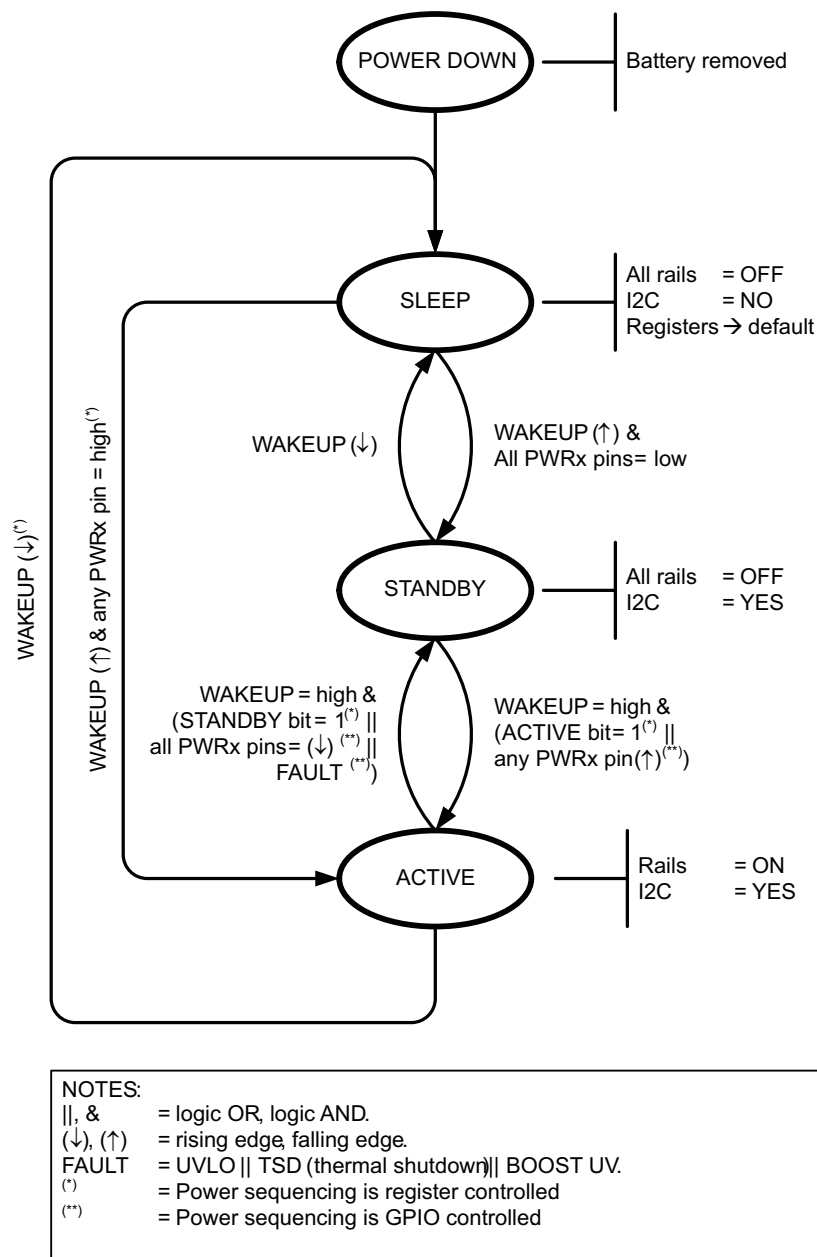


**Figure 1. Global State Diagram**

## WAKE-UP AND POWER UP SEQUENCING

The TPS65180/TPS65181 and TPS65180B/TPS65181B support flexible power-up sequencing through GPIO control using the PWR3, 2, 1, 0 pins or I<sup>2</sup>C control using the PWR\_SEQ0, 1, 2 registers. Using GPIO control, the output rails are enabled/disabled in the order in which the PWRx pins are asserted/de-asserted, respectively, and the power-up timing is controlled by the host only.

In I<sup>2</sup>C control mode the power-up/down order and timing are defined by user register settings. The default settings support the E Ink<sup>®</sup> Vizplex<sup>™</sup> panel and typically do not need to be changed by the user.

## GPIO CONTROL

Under GPIO control the system host in E Ink® Vizplex™ panel module enables the TPS65180/TPS65181 and TPS65180B/TPS65181B output rails by asserting the PWR0, PWR1, PWR2, PWR3 signals and the host has full control over the order and timing in which the output rails are powered up and down. Rails are in regulation 2 ms after their respective PWRx pin has been asserted with the exception of the first rail, which takes 6 ms to power up. The additional time is needed to power up the positive and inverting buck-boost regulator which need to be turned on before any other rail can be enabled. Once all rails are enabled and in regulation the PWR\_GOOD pin is released (pin status = HiZ and power good line is pulled high by external pull-up resistor). The PWRx pins are assigned to the rails as follows:

- PWR0: LDO2 (VNEG) and VCOM
- PWR1: CP2 (VEE)
- PWR2: LDO2 (VPOS)
- PWR3: CP1 (VDDH)

Rails are powered down whenever the host de-asserts the respective PWRx pin, and once all rails are disabled the device enters STANDBY mode. The next step is then to de-assert the WAKEUP pin to enter SLEEP mode which is the lowest-power mode of operation.

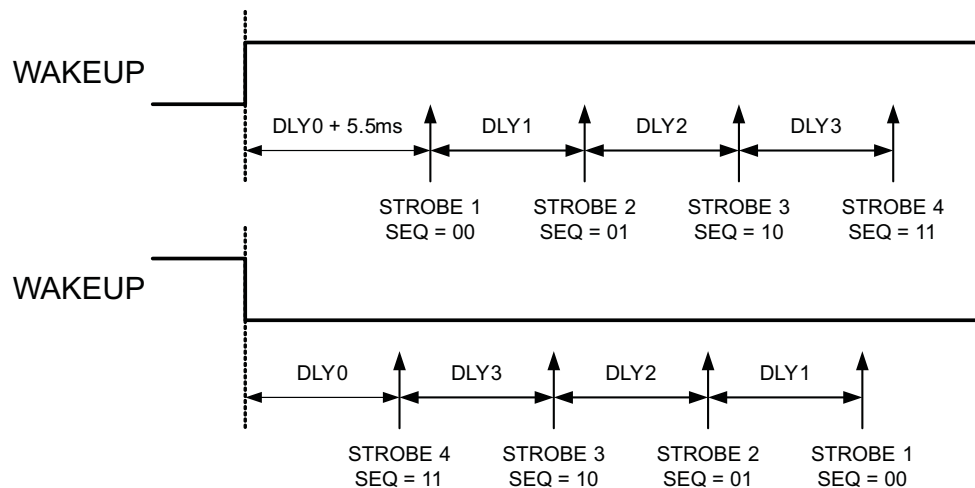
It is possible for the host to force the TPS65180/TPS65181 and TPS65180B/TPS65181B directly into SLEEP mode from ACTIVE mode by de-asserting the WAKEUP pin in which case the device follows the power-down sequence defined by the PWR\_SEQx registers before entering SLEEP mode.

## I<sup>2</sup>C CONTROL

Under I<sup>2</sup>C control the power-up sequence is defined by the PWR\_SEQx registers rather than through GPIO control. In SLEEP mode the TPS65180/TPS65181 and TPS65180B/TPS65181B are completely turned off, the I<sup>2</sup>C registers are reset, and the device does not accept any I<sup>2</sup>C transaction. Pull the WAKEUP pin high while all PWRx pins are held low and the device will enter STANDBY mode which enables the I<sup>2</sup>C interface. Write to the PWR\_SEQ0 register to define the order in which the output rails will be enabled at power-up and to the PWR\_SEQ1 and PWR\_SEQ2 registers to define the power-up delays between rails. Finally, set the ACTIVE bit in the ENABLE register to 1 to execute the power-up sequence and bring up all power rails.

It is possible for the host to force the TPS65180/TPS65181 and TPS65180B/TPS65181B directly into ACTIVE mode from SLEEP mode by pulling the WAKEUP pin high while at least one of the PWRx pins is pulled high. In this case the default power-up sequence defined by the PWR\_SEQx registers applies and the device will start powering up the rails 5.5 ms after the WAKEUP signal has been pulled high.

To power-down the device, set the STANDBY bit of the ENABLE register to 1 then the TPS65180/TPS65181 and TPS65180B/TPS65181B will follow the reverse power-up sequence to bring down all power rails. While the sequencer is busy powering up the power rails, any activity on the PWRx pins is ignored. Once all rails are up, any of the output rails can be disabled by applying a negative edge on the PWRx input pins, i.e. if the host toggles the PWRx pin high-low or low-high-low, the respective rail will be disabled regardless of how it has been enabled.



**TOP:** Power-up sequence is defined by assigning strobes to individual rails. STROBE1 is the first strobe to occur after WAKEUP has been pulled high and STROBE4 is the last event in the sequence. STROBES are assigned to rails in PWR\_SEQ0 register and delays between states are defined in PWR\_SEQ1 and PWR\_SEQ2 registers.

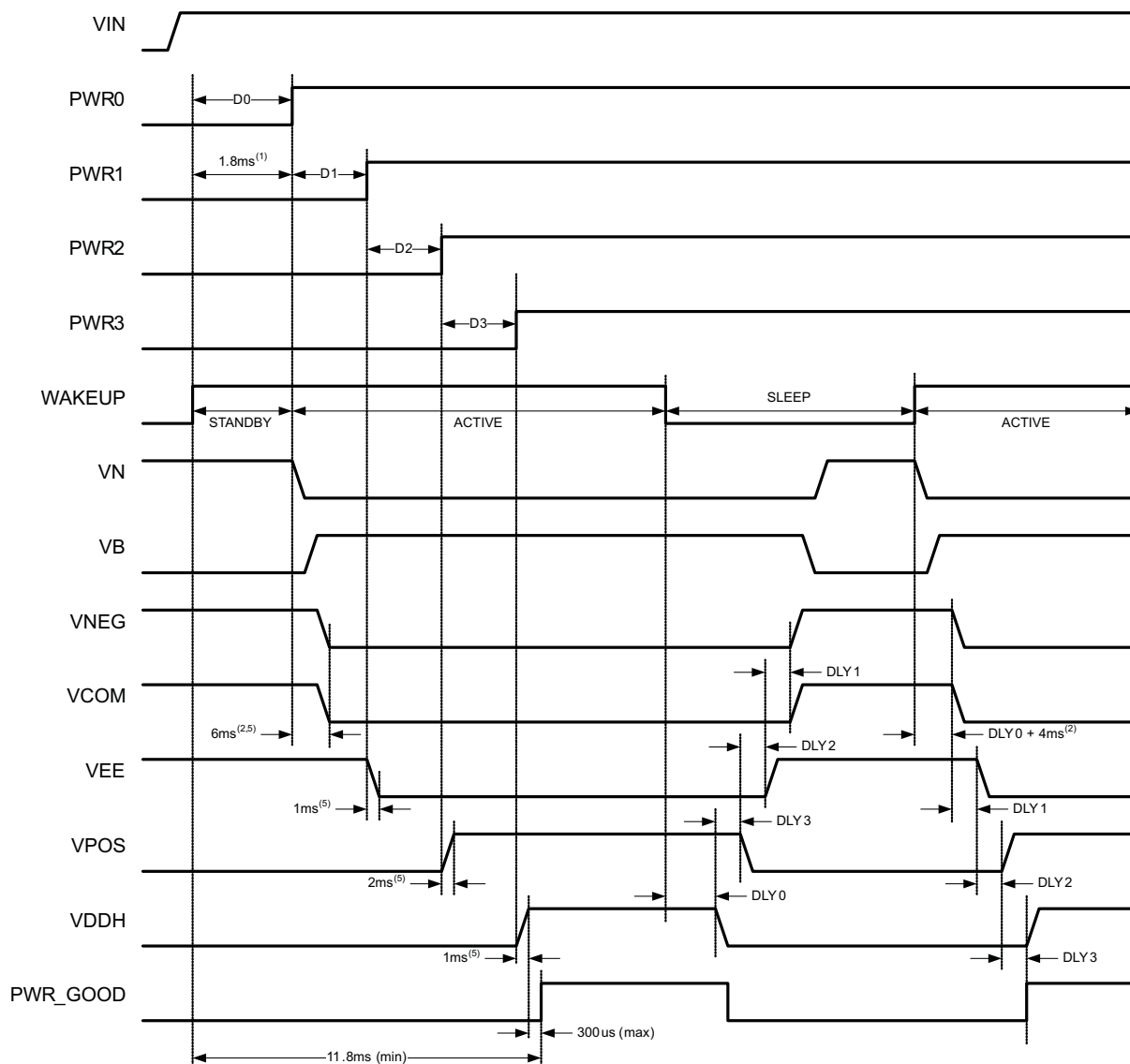
**BOTTOM:** Power-down sequence follows reverse power-up sequence.

Figure 2. I²C Control

## DEPENDENCIES BETWEEN RAILS

Charge pumps, LDOs, and VCOM driver are dependent on the positive and inverting buck-boost converters and several dependencies exist that affect the power-up sequencing. These dependencies are listed below.

1. Inverting buck-boost (DCDC2) must be in regulation before positive boost (DCDC1) can be enabled. Internally, DCDC1 enable is gated by DCDC2 power good.
2. Positive boost (DCDC1) must be in regulation before LDO2 (VNEG) can be enabled. Internally LDO2 enable is gated DCDC1 power-good.
3. Positive boost (DCDC1) must be in regulation before VCOM can be enabled; Internally VCOM enable is gated by DCDC1 power good.
4. Positive boost (DCDC1) must be in regulation before negative charge pump (CP2) can be enabled. Internally CP2 enable is gated by DCDC1 power good.
5. Positive boost (DCDC1) must be in regulation before positive charge pump (CP1) can be enabled. Internally CP1 enable is gated by DCDC1 power good.
6. LDO2 must be in regulation before LDO1 can be enabled. Internally LDO1 enable is gated by LDO2 power good.
7. The minimum delay time between any two PWRx pins must be > 62.5  $\mu$ s in order to follow the power up sequence defined by GPIO control. If any two PWRx pins are pulled up together (< 62.5  $\mu$ s apart) or the sequencer tries to bring up the rails at the same time by assigning the same STROBE to rails in PWR\_SEQ0 register, rails will be staggered in a manner that a subsequent rail's enable is gated by PG of a preceding rail. In this case, the default order of power-up is LDO2 (VNEG), CP2 (VEE), LDO1 (VPOS), and CP1(VDDH). If any two PWRx pins are pulled low together or the sequencer tries to bring down the rails at the same time by assigning the same STROBE to rails in PWR\_SEQ0 register, then all rails will go down at the same time.



- (1) Minimum delay time between WAKEUP rising edge and IC ready to accept I<sup>2</sup>C transaction.  
 (2) It takes 2ms minimum for each internal boost regulator to start up before VNEG can be enabled.  
 (5) It takes up to 2ms for LDOs (VPOS, VNEG) and 1ms for charge pumps (VDDH, VEE), to reach their steady state after being enabled.  
 DLY0-DLY3 are power up/down delays defined in register PWR\_SEQ1 and PWR\_SEQ2.

In this example the first power-up sequence is determined by GPIO control (WAKEUP is pulled high while PWRx pins are low). Power-down and 2nd power-up sequence is controlled by register settings (WAKEUP pin is toggled with at least one PWR pin held high).

**Figure 3. Power-Up and Power-Down Timing Diagram**

## SOFTSTART

Softstart for DCDC1, DCDC2, LDO1, and LDO2 is accomplished by lowering the current limits during start-up. If DCDC1 or DCDC2 are unable to reach power-good status within 10 ms, the corresponding UV flag is set in the interrupt registers, the interrupt pin is pulled low, and the device enters STANDBY mode. LDO1, LDO2, positive and negative charge pumps have a 5ms power-good time-out limit. If either rail is unable to power up within 5 ms after it has been enabled, the corresponding UV flag is set and the interrupt pin is pulled low. However, the device will remain in ACTIVE mode in this case.



Whenever the TPS65180/TPS65181 and TPS65180B/TPS65181B encounter under voltage on VNEG (VNEG\_UV), VPOS (VPOS\_UV), VEE (VEE\_UV) or VDDH (VDDH\_UV) it will shut down the corresponding rail (plus any dependent rail) only and remain in ACTIVE mode, allowing the DCDC converters to remain up. Again, the PWR\_GOOD and nINT pins will be pulled low and the corresponding interrupt bit will be set.

### TPS65180/TPS65180B FAULT HANDLING

Once a fault is detected the TPS65180/TPS65180B sets the appropriate interrupt flags in the INT\_STATUS1 and INT\_STATUS2 registers and pulls INT pin low to signal an interrupt to the host processor. None of the power rails can be re-enabled before the host has read the INT\_STATUSx bits and the fault has been removed. As the PWRx inputs are edge sensitive, the host must also toggle the PWRx pins to re-enable the rails through GPIO control, i.e. it must bring the PWRx pins low before asserting them again.

### TPS65181/TPS65181B FAULT HANDLING

The TPS65181/TPS65181B does not require the host processor to access the INT\_STATUS registers before re-enabling the output rails. Rails can be re-enabled as soon as the fault condition has been removed. Again, as the PWRx inputs are edge sensitive, the host must also toggle the PWRx pins to re-enable the rails through GPIO control, i.e. it must bring the PWRx pins low before asserting them again.

## POWER GOOD PIN

The power good pin (PWR\_GOOD) is an open drain output that is pulled high when all four power rails (CP1, CP2, LDO1, LDO2) are in regulation and is pulled low if any of the rails encounters a fault. PWR\_GOOD remains low if one of the rails is not enabled by the host and only after all rails are in regulation PWR\_GOOD is released to HiZ state (pulled up by external resistor).

## INTERRUPT PIN

The interrupt pin (nINT) is an open drain output that is pulled low whenever one or more of the INT\_STATUS1 or INT\_STATUS2 bits are set. The nINT pin is released (returns to HiZ state) and fault bits are cleared once the register with the set bit has been read by the host. If the fault persists, the INT\_pin will be pulled low again after a maximum of 32  $\mu$ s.

Interrupt events can be masked by re-setting the corresponding enable bit in the INT\_ENABLE1 and INT\_ENABLE2 register, i.e. the user can determine which events cause the nINT pin to be pulled low. The status of the enable bits affects the nINT pin only and has no effect on any of the protection and monitoring circuits or the INT\_STATUSx bits themselves.

Note that persisting fault conditions such as thermal shutdown can cause the nINT pin to be pulled low for an extended period of time which can keep the host in a loop trying to resolve the interrupt. If this behavior is not desired, set the corresponding mask bit after receiving the interrupt and keep polling the INT\_STATUSx register to see when the fault condition has disappeared. After the fault is resolved, unmask the interrupt bit again.

## PANEL TEMPERATURE MONITORING

The TPS65180/TPS65181 and TPS65180B/TPS65181B provide circuitry to bias and measure an external negative temperature coefficient resistor (NTC) to monitor device temperature in a range from  $-10^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  with an accuracy of  $\pm 1^{\circ}\text{C}$  from  $0^{\circ}\text{C}$  to  $50^{\circ}\text{C}$ . The TPS65180/TPS65180B requires the host to trigger the temperature acquisition through an I<sup>2</sup>C command whereas the TPS65181/TPS65181B triggers the temperature acquisition automatically once every 60 s.

### NTC BIAS CIRCUIT

Figure 5 below shows the block diagram of the NTC bias and measurement circuit. The NTC is biased from an internally generated 2.25-V reference voltage through an integrated 7.307-k $\Omega$  bias resistor. A 43-k $\Omega$  resistor is connected parallel to the NTC to linearize the temperature response curve. The circuit is designed to work with a nominal 10-k $\Omega$  NTC and achieves accuracy of  $\pm 1^{\circ}\text{C}$  from  $0^{\circ}\text{C}$  to  $50^{\circ}\text{C}$ . The voltage drop across the NTC is digitized by a 10-bit SAR ADC and translated into an 8-bit two's complement by digital per Table 1.

**Table 1. ADC Output Value vs Temperature**

| TEMPERATURE | TMST_VALUE[7:0] |
|-------------|-----------------|
| < -10°C     | 1111 0110       |
| -10°C       | 1111 0110       |
| -9°C        | 1111 0111       |
| ...         | ...             |
| -2°C        | 1111 1110       |
| -1°C        | 1111 1111       |
| 0°C         | 0000 0000       |
| 1°C         | 0000 0001       |
| 2°C         | 0000 0010       |
| ...         | ...             |
| 25°C        | 0001 1001       |
| ...         | ...             |
| 85°C        | 0101 0101       |
| > 85°C      | 0101 0101       |

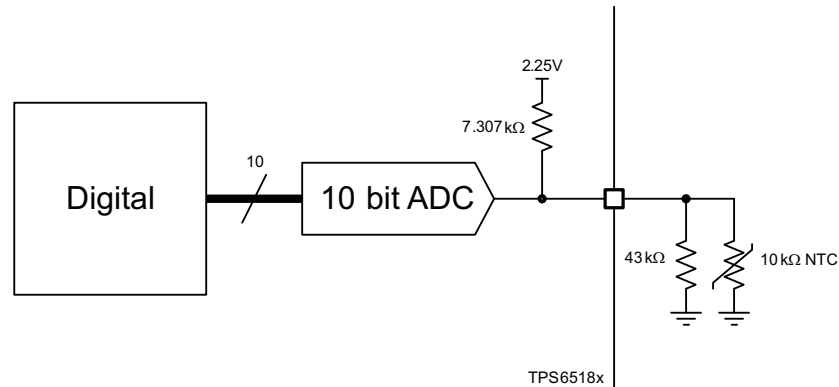


**Figure 5. NTC Bias and Measurement Circuit**

## TPS65180/TPS65180B TEMPERATURE ACQUISITION

The TPS65180/TPS65180B requires the host to trigger the temperature acquisition before reading the temperature value from register TMST\_VALUE. A standard temperature measurement involves the following steps:

1. The host sets the READ\_THERM bit of the TMST\_CONFIG register to 1. This enabled the NTC bias circuit and internal ADC.
2. The analog to digital conversion is automatically started after a fixed 250-μs delay. While the conversion is in progress the CONV\_END bit of the TMST\_CONFIG register is held low and returns to 1 after the conversion result is available.
3. After the conversion is complete the READ\_THERM bit is automatically reset, the EOC bit of the INT\_STATUS2 register is set, and the interrupt pin (nINT) is pulled low.
4. The host services the interrupt by reading the INT\_STATUS2 register. This clears the interrupt pin (nINT pin returns high). The host sees the EOC bit set and knows that the temperature data is available in the TMST\_VALUE register.
5. The host reads the temperature data from the TMST\_VALUE register.

## TPS65181/TPS65181B TEMPERATURE ACQUISITION

The TPS65181/TPS65181B triggers temperature acquisition once every 60s to reduce the number of required I<sup>2</sup>C writes. The host or display timing controller can read the temperature at any time by accessing the TMST\_VALUE register without having to set the READ\_THERM bit first. However, the host can always trigger an

additional temperature reading the same way as for the TPS65180/TPS65180B. Please note that at the end of each temperature acquisition the EOC interrupt will be set and an interrupt will be issued. Although the interrupt is automatically cleared, the nINT pin will be pulled low for a short amount of time (6  $\mu$ s). To avoid seeing the EOS interrupt every 60s it is recommended to mask the EOC interrupt by setting the EOC\_EN bit of the INT\_ENABLE2 register to 0.

## OVER TEMPERATURE REPORTING

The user has the option of setting HOT and COOL (not HOT) temperature thresholds as well as controlling interrupt behavior as the NTC exceeds HOT and cools down below COOL (not-HOT) threshold.

By default, TPS65180/TPS65181 and TPS65180B/TPS65181B compare the temperature conversion result to the HOT threshold after each conversion. If the NTC temperature is above the HOT threshold, the TMST\_HOT bit in the INT\_STATUS1 register is set to 1 and the interrupt pin (nINT) is pulled low. HOT temperature threshold is set by the host by writing to the TMST\_OS register and the HOT interrupt can be disabled by setting the HOT\_EN bit of the INT\_ENABLE1 register to 0.

Once the device has detected that the NTC is above the HOT threshold it will compare subsequent temperature acquisitions against the COOL threshold and pull the interrupt pin low when the NTC temperature drops below the COOL threshold. However, the interrupt will be issued only if the host has unmasked the COOL interrupt by setting TMST\_COOL\_EN bit of INT\_ENABLE1 register to 1. The COOL threshold is set by the host by writing to the TMST\_HYST register.

To use the full functionality of the HOT/COOL interrupts the following actions are required:

1. The host sets the HOT and COOL (not HOT) thresholds by writing the TMST\_OS and TMST\_HYST registers.
2. (2) For TPS65180/TPS65180B only: The host sets the READ\_THERM bit of the TMST\_CONFIG register to '1'. This initiates the temperature acquisition.
3. TPS65180/TPS65181 and TPS65180B/TPS65181B compare the result against the TMST\_OS threshold and will pull the nINT pin low if the NTC temperature exceeds the HOT threshold.
4. If the TPS65180/TPS65181 and TPS65180B/TPS65181B report a HOT condition, the host un masks the TMST\_COOL\_EN bit by setting it to 1 (INT\_ENABLE1 register).
5. The host initiates a new temperature conversion by setting the READ\_THERM bit of the TMST\_CONFIG register to 1. If the new temperature is still above the HOT threshold, a new HOT interrupt will be issued. If the temperature is below HOT but above COOL threshold, no interrupt is issued (except for EOC which is issued at the end of each conversion). If the temperature is below COOL threshold, a COOL interrupt is issued.
6. After the temperature drops below the COOL threshold the host should set the TMST\_COOL\_EN bit in the INT\_ENABLE1 register to 0 to mask additional COOL interrupts after subsequent temperature acquisitions.

## OVER-TEMPERATURE FAULT QUEUING

The user can specify the number of consecutive HOT temperature reads required to issue a HOT interrupt. The user can set the FAULT\_QUE[1:0] bits of the TMST\_CONFIG register to specify 1, 2, 4, or 6 consecutive reads that all must be above the HOT threshold before a HOT interrupt is issued. The fault queue is reset each time the acquired temperature drops below the HOT threshold and can also be reset by the host by setting the FAULT\_QUE\_CLR bit 1. Only if the specified number of readings have been detected which all need to be above the HOT threshold, a HOT interrupt is issued. This function is useful to reduce noise in the temperature measurements.

## TPS65181/TPS65181B TEMPERATURE SENSOR

The TPS65181/TPS65181B automates the temperature monitoring process and is specifically designed to operate in multi-host systems where one of the I<sup>2</sup>C hosts, e.g. the display controller, has limited I<sup>2</sup>C capability. Standard I<sup>2</sup>C protocol requires the following steps to read data from a register:

1. Send device and register address, R/nW bit set low (write command).
2. Send device address, R/nW set high (read command).
3. The slave will respond with data from the specified register address.

Some display controllers support I<sup>2</sup>C read commands only and need to access the temperature data from the

TPS65181/TPS65181B TMST\_VALUE register. To support these systems the TPS65181/TPS65181B automatically triggers temperature acquisition every 60s (for other acquisition intervals contact the factory) and stores the result in TMST\_VALUE register. With the FIX\_RD\_PTR bit in the FIX\_RD\_POINTER register set to 1 the device will respond to any I<sup>2</sup>C read command with data from the TMST\_VALUE register. No write command with the register address is required and address auto increment feature is disabled in this mode. Therefore reading the temperature data is reduced to two steps:

1. Send device address, R/nW set high (read command).
2. Read the data from the slave. The slave will respond with data from TMST\_VALUE register address.

Write functionality is not affected by the FIX\_RD\_PTR bit and the main controller in the system maintains full control of the PMIC. Interrupts and error flags are issued and need to be handled the same way as for the TPS65180/TPS65180B with two exceptions:

1. The FIX\_RD\_PTR bit in the FIX\_RD\_POINTER register needs to be set to 0 before the main controller can read any register different from the TMST\_VALUE register.
2. Thermal shutdown (TSD), positive boost under voltage (VB\_UV), inverting buck-boost under voltage (VN\_UV), and input under voltage lock out (UVLO) interrupt bits do not have to be cleared before output rails can be re-enabled.

At system power-up the main processor sets up the PMIC by accessing the I<sup>2</sup>C registers and setting the control parameters as needed. When the system is setup correctly the main controller sets the FIX\_READ\_POINTER bit and the display controller can start accessing the temperature information. During normal operation the main controller can write to the PMIC at any time but before it can read access registers the FIX\_READ\_POINTER bit must be written 0.

The temperature range and representation of the temperature data is the same between the TPS65180/TPS65180B and TPS65181/TPS65181B.

### THE FIX\_RD\_PTR BIT

The TPS65181/TPS65181B supports a special I<sup>2</sup>C mode making it compatible with the EPSON Broadsheet S1D13521 timing controller. Standard I<sup>2</sup>C protocol requires the following steps to read data from a register:

1. Send device slave address, R/nW bit set low (write command)
2. Send register address
3. Send device slave address, R/nW set high (read command)
4. The slave will respond with data from the specified register address.

The EPSON Broadsheet S1D13521 controller does not support I<sup>2</sup>C writes nor I<sup>2</sup>C reads from addressed registers (step 1. and 2. above) but needs to access the temperature data from the TPS65181/TPS65181B's TMST\_VALUE register. To support Broadsheet based systems, the TPS65181/TPS65181B automatically triggers temperature acquisition every 60s and stores the result in TMST\_VALUE register. With the FIX\_RD\_PTR bit in the FIX\_RD\_POINTER register set to 1 the device will respond to any I<sup>2</sup>C read command with data from the TMST\_VALUE register. No write command with the register address is required and address auto increment feature is disabled in this mode. Therefore reading the temperature data is reduced to two steps:

1. Send device address, R/nW set high (read command)
2. Read the data from the slave. The slave will respond with data from TMST\_VALUE register address.

Write functionality is not affected by the FIX\_RD\_PTR bit and the main controller in the system maintains full control of the PMIC. Interrupts and error flags are issued and need to be handled the same way as for the TPS65180/TPS65180B with two exceptions:

1. The FIX\_RD\_PTR bit in the FIX\_RD\_POINTER register needs to be set to 0 before the main controller can read any register different from the TMST\_VALUE register.
2. Thermal Shutdown (TSD), positive boost Under Voltage (VB\_UV), inverting buck-boost Under Voltage (VN\_UV), and input Under Voltage Lock Out (UVLO) interrupt bits do not have to be cleared before output rails can be re-enabled.

At system power-up the main processor sets up the PMIC by accessing the I<sup>2</sup>C registers and setting the control parameters as needed. When the system is setup correctly the main controller sets the FIX\_READ\_POINTER bit and the display controller can start accessing the temperature information. During normal operation the main controller can write to the PMIC at any time but before it can read access registers the FIX\_READ\_POINTER bit must be written 0.

## I<sup>2</sup>C BUS OPERATION

The TPS65180/TPS65181 and TPS65180B/TPS65181B host a slave I<sup>2</sup>C interface that supports data rates up to 400 kbit/s and auto-increment addressing and is compliant to I<sup>2</sup>C standard 3.0.

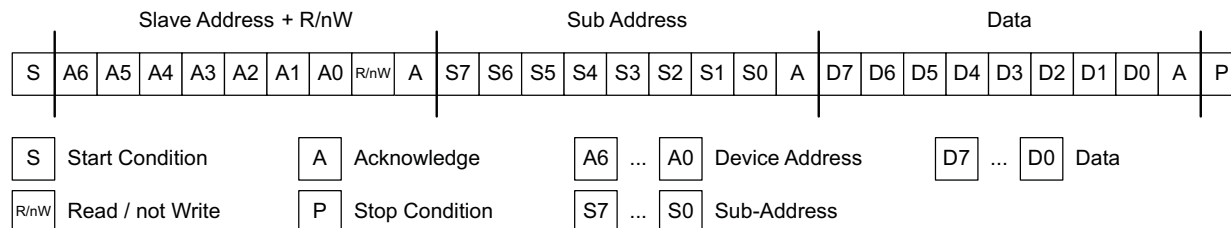


**Figure 6. Subaddress in I<sup>2</sup>C Transmission**

Start – Start condition

G(3:0) – Group ID: Address fixed at 1001.

A(2:0) – Device Address: Address fixed at 000.

R/nW – Read / not Write Select Bit

ACK – Acknowledge

S(7:0) – Subaddress: defined per register map.

D(7:0) – Data; Data to be loaded into the device.

Stop – Stop condition

The I<sup>2</sup>C Bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open Drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in [Figure 8](#). The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device will issue an acknowledge pulse and prepare the receive subaddress data. Subaddress data is decoded and responded to as per the Register Map section of this document. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I<sup>2</sup>C interface will auto-sequence through register addresses, so that multiple data words can be sent for a given I<sup>2</sup>C transmission. Reference [Figure 8](#). Please note that auto-increment is not supported when the FIX\_RD\_PTR bit is set (TPS65181/TPS65181B only).

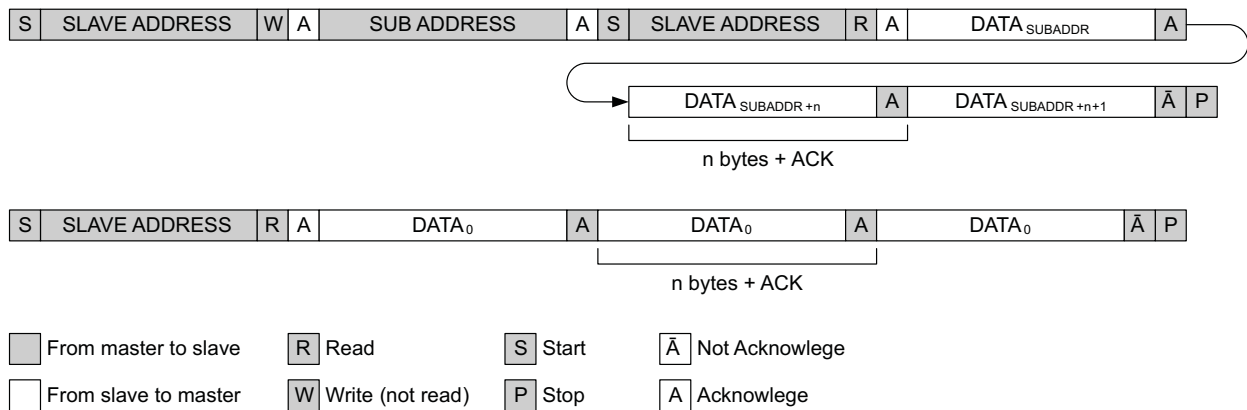


**Figure 7. TOP: Standard I<sup>2</sup>C READ data transmission with address auto-increment. Bottom: I<sup>2</sup>C READ data transmission with FIX\_RD\_PTR bit set for EPSON Broadsheet support. Only address 0x00h can be read. FIX\_RD\_PTR bit has no impact on WRITE transaction.**

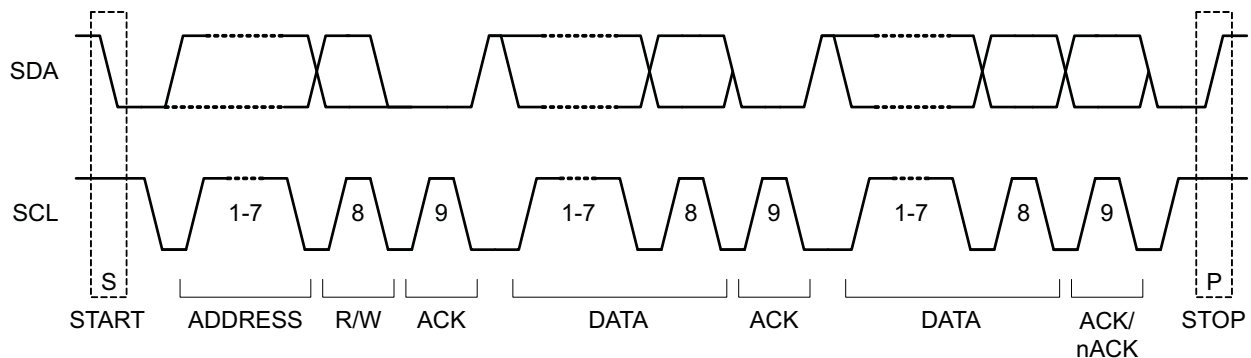


**Figure 8. I<sup>2</sup>C Start/Stop/Acknowledge Protocol**

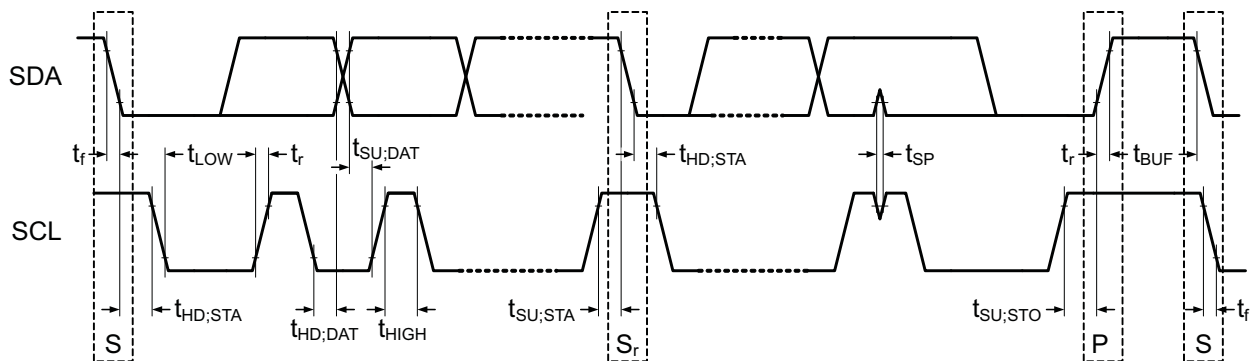


**Figure 9. I<sup>2</sup>C Data Transmission Timing**

## DATA TRANSMISSION TIMING

$V_{BAT} = 3.6\text{ V} \pm 5\%$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 100\text{ pF}$  (unless otherwise noted)

| PARAMETER                                                                                                 | TEST CONDITIONS | MIN | TYP | MAX  | UNIT          |
|-----------------------------------------------------------------------------------------------------------|-----------------|-----|-----|------|---------------|
| $f_{(SCL)}$ Serial clock frequency                                                                        |                 | 100 |     | 400  | KHz           |
| $t_{HD;STA}$ Hold time (repeated) START condition. After this period, the first clock pulse is generated. | SCL = 100 KHz   | 4   |     |      | $\mu\text{s}$ |
|                                                                                                           | SCL = 400 KHz   | 600 |     |      | ns            |
| $t_{LOW}$ LOW period of the SCL clock                                                                     | SCL = 100 KHz   | 4.7 |     |      | $\mu\text{s}$ |
|                                                                                                           | SCL = 400 KHz   | 1.3 |     |      |               |
| $t_{HIGH}$ HIGH period of the SCL clock                                                                   | SCL = 100 KHz   | 4   |     |      | $\mu\text{s}$ |
|                                                                                                           | SCL = 400 KHz   | 600 |     |      | ns            |
| $t_{SU;STA}$ Set-up time for a repeated START condition                                                   | SCL = 100 KHz   | 4.7 |     |      | $\mu\text{s}$ |
|                                                                                                           | SCL = 400 KHz   | 600 |     |      | ns            |
| $t_{HD;DAT}$ Data hold time                                                                               | SCL = 100 KHz   | 0   |     | 3.45 | $\mu\text{s}$ |
|                                                                                                           | SCL = 400 KHz   | 0   |     | 900  | ns            |
| $t_{SU;DAT}$ Data set-up time                                                                             | SCL = 100 KHz   | 250 |     |      | ns            |
|                                                                                                           | SCL = 400 KHz   | 100 |     |      |               |
| $t_r$ Rise time of both SDA and SCL signals                                                               | SCL = 100 KHz   |     |     | 1000 | ns            |
|                                                                                                           | SCL = 400 KHz   |     |     | 300  |               |
| $t_f$ Fall time of both SDA and SCL signals                                                               | SCL = 100 KHz   |     |     | 300  | ns            |
|                                                                                                           | SCL = 400 KHz   |     |     | 300  |               |
| $t_{SU;STO}$ Set-up time for STOP condition                                                               | SCL = 100 KHz   | 4   |     |      | $\mu\text{s}$ |
|                                                                                                           | SCL = 400 KHz   | 600 |     |      | ns            |
| $t_{BUF}$ Bus Free Time Between Stop and Start Condition                                                  | SCL = 100 KHz   | 4.7 |     |      | $\mu\text{s}$ |
|                                                                                                           | SCL = 400 KHz   | 1.3 |     |      |               |
| $t_{SP}$ Pulse width of spikes which mst be suppressed by the input filter                                | SCL = 100 KHz   | n/a |     | n/a  | ns            |
|                                                                                                           | SCL = 400 KHz   | 0   |     | 50   |               |
| $C_b$ Capacitive load for each bus line                                                                   | SCL = 100 KHz   |     |     | 400  | pF            |
|                                                                                                           | SCL = 400 KHz   |     |     | 400  |               |

**REGISTER ADDRESS MAP**

| REGISTER | ADDRESS (HEX) | NAME             | DEFAULT VALUE | DESCRIPTION                           |
|----------|---------------|------------------|---------------|---------------------------------------|
| 0        | 0x00          | TMST_VALUE       | N/A           | Thermistor value read by ADC          |
| 1        | 0x01          | ENABLE           | 0001 1111     | Enable/disable bits for regulators    |
| 2        | 0x02          | VP_ADJUST        | 0010 0011     | Voltage settings for VPOS, VDDH       |
| 3        | 0x03          | VN_ADJUST        | 1010 0011     | Voltage settings for VNEG, VEE        |
| 4        | 0x04          | VCOM_ADJUST      | 0111 0100     | Voltage settings for VCOM             |
| 5        | 0x05          | INT_ENABLE1      | 0111 0100     | Interrupt enable group1               |
| 6        | 0x06          | INT_ENABLE2      | 1111 1011     | Interrupt enable group2               |
| 7        | 0x07          | INT_STATUS1      | 0xxx xx00     | Interrupt status group1               |
| 8        | 0x08          | INT_STATUS2      | xxxx x0xx     | Interrupt status group2               |
| 9        | 0x09          | PWR_SEQ0         | 1110 0100     | Power up sequence                     |
| 10       | 0x0A          | PWR_SEQ1         | 0010 0010     | DLY0, DLY1 time set                   |
| 11       | 0x0B          | PWR_SEQ2         | 0010 0010     | DLY2, DLY3 time set                   |
| 12       | 0x0C          | TMST_CONFIG      | 0010 0000     | Thermistor configuration              |
| 13       | 0x0D          | TMST_OS          | 0011 0010     | Thermistor hot temp set               |
| 14       | 0x0E          | TMST_HYST        | 0010 1101     | Thermistor cool temp set              |
| 15       | 0x0F          | PG_STATUS        | 0000 0000     | Power good status each rails          |
| 16       | 0x10          | REVID            | 0100 0001     | Device revision ID information        |
| 17       | 0x11          | FIX_READ_POINTER | 0000 0000     | I <sup>2</sup> C read pointer control |

## THERMISTOR READOUT (TMST\_VALUE)

Address – 0x00h

| DATA BIT    | D7              | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|-------------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| FIELD NAME  | TMST_VALUE[7:0] |     |     |     |     |     |     |     |
| READ/WRITE  | R               | R   | R   | R   | R   | R   | R   | R   |
| RESET VALUE | N/A             | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

| FIELD NAME      | BIT DEFINITION                                                                                                                                                                                                                                                                                                                                  |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TMST_VALUE[7:0] | <p>Temperature read-out</p> <p>1111 0110 – &lt; -10°C</p> <p>1111 0110 – -10°C</p> <p>1111 0111 – -9°C</p> <p>...</p> <p>1111 1110 – -2°C</p> <p>1111 1111 – -1 °C</p> <p>0000 0000 – 0 °C</p> <p>0000 0001 – 1°C</p> <p>0000 0010 – 2°C</p> <p>...</p> <p>0001 1001 – 25°C</p> <p>...</p> <p>0101 0101 – 85°C</p> <p>0101 0101 – &gt; 85°C</p> |

## ENABLE (ENABLE)

Address – 0x01h

| DATA BIT    | D7     | D6      | D5         | D4      | D3      | D2      | D1     | D0      |
|-------------|--------|---------|------------|---------|---------|---------|--------|---------|
| FIELD NAME  | ACTIVE | STANDBY | V3P3_SW_EN | VCOM_EN | VDDH_EN | VPOS_EN | VEE_EN | VNEG_EN |
| READ/WRITE  | R/W    | R/W     | R/W        | R/W     | R/W     | R/W     | R/W    | R/W     |
| RESET VALUE | 0      | 0       | 0          | 1       | 1       | 1       | 1      | 1       |

| FIELD NAME | BIT DEFINITION <sup>(1)</sup>                                                                                                                                                                                                                                        |
|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACTIVE     | <p>STANDBY to ACTIVE transition bit</p> <p>1 – Transition from STANDBY to ACTIVE mode. Rails power up as defined by PWR_SEQx registers.</p> <p>0 – No effect</p> <p>NOTE: After transition bit is cleared automatically.</p>                                         |
| STANDBY    | <p>ACTIVE to STANDBY transition bit</p> <p>1 – Transition from ACTIVE to STANDBY mode. Rails power down as defined by PWR_SEQx registers.</p> <p>0 – No effect</p> <p>NOTE: After transition bit is cleared automatically. STANDBY bit has priority over AVTIVE.</p> |
| V3P3_SW_EN | <p>VIN3P3 to V3P3 switch enable</p> <p>1 – Switch is ON</p> <p>0 – Switch id OFF</p>                                                                                                                                                                                 |
| VCOM_EN    | <p>VCOM buffer enable</p> <p>1 – Enabled</p> <p>0 – Disabled</p>                                                                                                                                                                                                     |

(1) Enable/disable bits for regulators are AND'd with PWRx signals.

| FIELD NAME | BIT DEFINITION <sup>(1)</sup>                                                                                       |
|------------|---------------------------------------------------------------------------------------------------------------------|
| VDDH_EN    | VDDH charge pump enable<br>1 – Enabled<br>0 – Disabled                                                              |
| VPOS_EN    | VPOS LDO regulator enable<br>1 – Enabled<br>0 – Disabled<br>NOTE: VPOS cannot be enabled before VNEG is enabled.    |
| VEE_EN     | VEE charge pump enable<br>1 – Enabled<br>0 – Disabled                                                               |
| VNEG_EN    | VNEG LDO regulator enable<br>1 – Enabled<br>0 – Disabled<br>NOTE: When VNEG is disabled VPOS will also be disabled. |

## POSITIVE VOLTAGE RAIL ADJUSTMENT (VP\_ADJUST)

Address – 0x02h

| DATA BIT    | D7       | D6            | D5  | D4  | D3       | D2            | D1  | D0  |
|-------------|----------|---------------|-----|-----|----------|---------------|-----|-----|
| FIELD NAME  | Not used | VDDH_SET[2:0] |     |     | not used | VPOS_SET[2:0] |     |     |
| READ/WRITE  | R        | R/W           | R/W | R/W | R        | R/W           | R/W | R/W |
| RESET VALUE | 0        | 0             | 1   | 0   | 0        | 0             | 1   | 1   |

| FIELD NAME    | BIT DEFINITION <sup>(1)</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Not used      | N/A                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| VDDH_SET[2:0] | <p>VDDH voltage setting</p> <p>000 – VDDH increase by 10%</p> <p>001 – VDDH increase by 5%</p> <p>010 – Nominal</p> <p>011 – VDDH decrease by 5%</p> <p>100 – VDDH decrease by 10%</p> <p>101 – Reserved</p> <p>110 – Reserved</p> <p>111 – Reserved</p>                                                                                                                                                                                                                |
| Not used      | N/A                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| VPOS_SET[2:0] | <p>VPOS voltage setting</p> <p>000 :  VNEG  - 0.75 V</p> <p>001 :  VNEG  - 0.5 V</p> <p>010 :  VNEG  - 0.25 V</p> <p>011 :  VNEG </p> <p>100 :  VNEG  + 0.25 V</p> <p>101 :  VNEG  + 0.5 V</p> <p>110 :  VNEG  + 0.75 V</p> <p>111 – Reserved</p> <p>NOTE: For proper tracking of the VPOS and VNEG supply these bits must remain set at their default value of 011b. VPOS will track VNEG automatically when VNEG_SET[2:0] bits of VN_ADJUST register are changed.</p> |

(1) VDDH will be decreased from set value defined by resistor divider. Decreased VDDH value should be within spec range.

## NEGATIVE VOLTAGE RAIL ADJUSTMENT (VN\_ADJUST)

Address – 0x03h

| DATA BIT    | D7               | D6           | D5  | D4  | D3       | D2            | D1  | D0  |
|-------------|------------------|--------------|-----|-----|----------|---------------|-----|-----|
| FIELD NAME  | VCOM_ADJ         | VEE_SET[2:0] |     |     | Not used | VNEG_SET[2:0] |     |     |
| READ/WRITE  | R/W              | R/W          | R/W | R/W | R        | R/W           | R/W | R/W |
| RESET VALUE | 1 <sup>(1)</sup> | 0            | 1   | 0   | 0        | 0             | 1   | 1   |

(1) TPS65180/TPS65180B: Bit defaults to 1; TPS65181/TPS65181B: Bit defaults to 0

| FIELD NAME                  | BIT DEFINITION                                                                                                                                                                                                |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VCOM_ADJ                    | VCOM output adjustment method<br>0 – VCOM_XADJ pin<br>1 – I <sup>2</sup> C interface                                                                                                                          |
| VEE_SET[2:0] <sup>(1)</sup> | VDDH voltage setting<br>000 – VEE decrease by 10%<br>001 – VEE decrease by 5%<br>010 – Nominal<br>011 – VEE increase by 5%<br>100 – VEE increase by 10%<br>101 – Reserved<br>110 – Reserved<br>111 – Reserved |
| not used                    | N/A                                                                                                                                                                                                           |
| VNEG_SET[2:0]               | VNEG voltage setting<br>000 – -15.75 V<br>001 – -15.50 V<br>010 – -15.25 V<br>011 – -15.00 V<br>100 – -14.75 V<br>101 – -14.50 V<br>110 – -14.25 V<br>111 – Reserved                                          |

(1) VEE will be decreased from set value defined by resistor divider. Decreased VEE value should be within spec range.

## VCOM ADJUSTMENT (VCOM\_ADJUST)

Address – 0x04h

| DATA BIT    | D7            | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|-------------|---------------|-----|-----|-----|-----|-----|-----|-----|
| FIELD NAME  | VCOM_SET[7:0] |     |     |     |     |     |     |     |
| READ/WRITE  | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0             | 1   | 1   | 1   | 0   | 1   | 0   | 0   |

| FIELD NAME    | BIT DEFINITION                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VCOM_SET[7:0] | <p>VCOM voltage adjustment</p> <p>0000 0000 – 0 V</p> <p>0000 0001 – 11 mV</p> <p>0000 0010 – 22 mV</p> <p>...</p> <p>0111 0011 – 1239 mV</p> <p>0111 0100 – 1250 mV</p> <p>0111 0101 – 1261 mV</p> <p>...</p> <p>1111 1111 – 2750 mV</p> <p>NOTE: step size is rounded to 11 mV. Theoretical step size is 2750 mV / 255 mV = 10.78 mV. Parametric performance is guaranteed from -0.3 V to -2.5 V only.</p> |

## INTERRUPT ENABLE 1 (INT\_ENABLE1)

Address – 0x05h

| DATA BIT    | D7       | D6     | D5     | D4          | D3           | D2      | D1       | D0       |
|-------------|----------|--------|--------|-------------|--------------|---------|----------|----------|
| FIELD NAME  | Not used | TSD_EN | HOT_EN | TMST_HOT_EN | TMST_COOL_EN | UVLO_EN | Not used | Not used |
| READ/WRITE  | R        | R/W    | R/W    | R/W         | R/W          | R/W     | R        | R        |
| RESET VALUE | 0        | 1      | 1      | 1           | 0            | 1       | 0        | 0        |

| FIELD NAME   | BIT DEFINITION                                                                          |
|--------------|-----------------------------------------------------------------------------------------|
| Not used     | N/A                                                                                     |
| TSD_EN       | <p>Thermal shutdown interrupt enable</p> <p>1 – Enabled</p> <p>0 – Disabled</p>         |
| HOT_EN       | <p>Thermal shutdown early warning enable</p> <p>1 – Enabled</p> <p>0 – Disabled</p>     |
| TMST_HOT_EN  | <p>Thermistor hot warning enable</p> <p>1 – Enabled</p> <p>0 – Disabled</p>             |
| TMST_COOL_EN | <p>Thermistor hot escape interrupt enable</p> <p>1 – Enabled</p> <p>0 – Disabled</p>    |
| UVLO_EN      | <p>VIN under voltage detect interrupt enable</p> <p>1 – Enabled</p> <p>0 – Disabled</p> |
| Not used     | N/A                                                                                     |
| Not used     | N/A                                                                                     |

## INTERRUPT ENABLE 2 (INT\_ENABLE2)

Address – 0x06h

| DATA BIT    | D7       | D6         | D5       | D4         | D3        | D2       | D1         | D0     |
|-------------|----------|------------|----------|------------|-----------|----------|------------|--------|
| FIELD NAME  | VB_UV_EN | VDDH_UV_EN | VN_UV_EN | VPOS_UV_EN | VEE_UV_EN | not used | VNEG_UV_EN | EOC_EN |
| READ/WRITE  | R/W      | R/W        | R/W      | R/W        | R/W       | R        | R/W        | R/W    |
| RESET VALUE | 1        | 1          | 1        | 1          | 1         | 0        | 1          | 1      |

| FIELD NAME | BIT DEFINITION                                                                                      |
|------------|-----------------------------------------------------------------------------------------------------|
| VB_UV_EN   | Positive boost converter under voltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled       |
| VDDH_UV_EN | VDDH under voltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled                           |
| VN_UV_EN   | Inverting buck-boost converter under voltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled |
| VPOS_UV_EN | VPOS under voltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled                           |
| VEE_UV_EN  | VEE under voltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled                            |
| not used   | N/A                                                                                                 |
| VNEG_UV_EN | VNEG under voltage detect interrupt enable<br>1 – Enabled<br>0 – Disabled                           |
| EOC_EN     | ADC end of conversion interrupt enable<br>1 – Enabled<br>0 – Disabled                               |

## INTERRUPT INT\_STATUS1 (INT\_STATUS1)

Address – 0x07h

| DATA BIT    | D7       | D6   | D5  | D4       | D3        | D2   | D1       | D0       |
|-------------|----------|------|-----|----------|-----------|------|----------|----------|
| FIELD NAME  | Not used | TSDN | HOT | TMST_HOT | TMST_COOL | UVLO | Not used | Not used |
| READ/WRITE  | R        | R    | R   | R        | R         | R    | R        | R        |
| RESET VALUE | 0        | N/A  | N/A | N/A      | N/A       | N/A  | 0        | 0        |

| FIELD NAME | BIT DEFINITION                     |
|------------|------------------------------------|
| Not used   | N/A                                |
| TSD        | Thermal shutdown interrupt         |
| HOT        | Thermal shutdown early warning     |
| TMST_HOT   | Thermistor hot warning             |
| TMST_COOL  | Thermistor hot escape interrupt    |
| UVLO       | VIN under voltage detect interrupt |
| Not used   | N/A                                |
| Not used   | N/A                                |

## INTERRUPT STATUS 2 (INT\_STATUS2)

Address – 0x08h

| DATA BIT    | D7    | D6      | D5    | D4      | D3     | D2       | D1      | D0  |
|-------------|-------|---------|-------|---------|--------|----------|---------|-----|
| FIELD NAME  | VB_UV | VDDH_UV | VN_UV | VPOS_UV | VEE_UV | Not used | VNEG_UV | EOC |
| READ/WRITE  | R     | R       | R     | R       | R      | R        | R       | R   |
| RESET VALUE | N/A   | N/A     | N/A   | N/A     | N/A    | 0        | N/A     | N/A |

| FIELD NAME | BIT DEFINITION <sup>(1)</sup>                                 |
|------------|---------------------------------------------------------------|
| VB_UV      | Positive boost converter under voltage detect interrupt       |
| VDDH_UV    | VDDH under voltage detect interrupt                           |
| VN_UV      | Inverting buck-boost converter under voltage detect interrupt |
| VPOS_UV    | VPOS under voltage detect interrupt                           |
| VEE_UV     | VEE under Voltage detect interrupt                            |
| not used   | N/A                                                           |
| VNEG_UV    | VNEG under voltage detect interrupt                           |
| EOC        | ADC end of conversion interrupt                               |

(1) Under voltage detect bit is set if the corresponding rail does not come up 5 ms after it is enabled except for DCDC1 and 2 which are set 10 ms after they are enabled.

## POWER SEQUENCE REGISTER 0 (PWR\_SEQ0)

Address – 0x09h

| DATA BIT    | D7            | D6  | D5            | D4  | D3           | D2  | D1            | D0  |
|-------------|---------------|-----|---------------|-----|--------------|-----|---------------|-----|
| FIELD NAME  | VDDH_SEQ[1:0] |     | VPOS_SEQ[1:0] |     | VEE_SEQ[1:0] |     | VNEG_SEQ[1:0] |     |
| READ/WRITE  | R/W           | R/W | R/W           | R/W | R/W          | R/W | R/W           | R/W |
| RESET VALUE | 1             | 1   | 1             | 0   | 0            | 1   | 0             | 0   |

| FIELD NAME    | BIT DEFINITION <sup>(1)</sup>                                                                                                                                 |
|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDDH_SEQ[1:0] | VDDH power-up/down order<br>00 – Power-up/down on STROBE1<br>01 – Power-up/down on STROBE2<br>10 – Power-up/down on STROBE3<br>11 – Power-up/down on STROBE4  |
| VPOS_SEQ[1:0] | VPOS power-up/down order<br>00 – Power-up/down on STROBE1<br>01 – Power-up/down on STROBE2<br>10 – Power-up/down on STROBE3<br>11 – Ppower-up/down on STROBE4 |
| VEE_SEQ[1:0]  | VEE power-up/down order<br>00 – Power-up/down on STROBE1<br>01 – Power-up/down on STROBE2<br>10 – Power-up/down on STROBE3<br>11 – Power-up/down on STROBE4   |
| VNEG_SEQ[1:0] | VNEG power-up/down order<br>00 – Power-up/down on STROBE1<br>01 – Power-up/down on STROBE2<br>10 – Power-up/down on STROBE3<br>11 – Power-up/down on STROBE4  |

(1) Power-down sequence follows the reverse order of power-up.

**POWER SEQUENCE REGISTER 1 (PWR\_SEQ1)**

Address – 0x0Ah

| DATA BIT    | D7        | D6  | D5  | D4  | D3        | D2  | D1  | D0  |
|-------------|-----------|-----|-----|-----|-----------|-----|-----|-----|
| FIELD NAME  | DLY1[3:0] |     |     |     | DLY0[3:0] |     |     |     |
| READ/WRITE  | R/W       | R/W | R/W | R/W | R/W       | R/W | R/W | R/W |
| RESET VALUE | 0         | 0   | 1   | 0   | 0         | 0   | 1   | 0   |

| FIELD NAME | BIT DEFINITION                                                                                                                                                                                                                                                      |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DLY1[3:0]  | <p>DLY1 delay time set; defines the delay time from STROBE1 to STROBE2 during power-up and from STROBE2 to STROBE1 during power-down.</p> <p>0000 – 0 ms<br/> 0001 – 1 ms<br/> 0010 – 2 ms<br/> 0011 – 3 ms<br/> ...<br/> 1110 – 14 ms<br/> 1111 – 15 ms</p>        |
| DLY0[3:0]  | <p>DLY0 delay time set; defines the delay time from WAKEUP high to STROBE1 during power-up and from WAKEUP low to STROBE4 during power-down.</p> <p>0000 – 0 ms<br/> 0001 – 1 ms<br/> 0010 – 2 ms<br/> 0011 – 3 ms<br/> ...<br/> 1110 – 14 ms<br/> 1111 – 15 ms</p> |

## POWER SEQUENCE REGISTER 2 (PWR\_SEQ2)

Address – 0x0Bh

| DATA BIT    | D7        | D6  | D5  | D4  | D3        | D2  | D1  | D0  |
|-------------|-----------|-----|-----|-----|-----------|-----|-----|-----|
| FIELD NAME  | DLY3[3:0] |     |     |     | DLY2[3:0] |     |     |     |
| READ/WRITE  | R/W       | R/W | R/W | R/W | R/W       | R/W | R/W | R/W |
| RESET VALUE | 0         | 0   | 1   | 0   | 0         | 0   | 1   | 0   |

| FIELD NAME | BIT DEFINITION                                                                                                                                                                                                                                                                                                                                                                       |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DLY3[3:0]  | <p>DLY3 delay time set; defines the delay time from STROBE3 to STROBE4 during power-up and from STROBE4 to STROBE3 during power-down.</p> <p>0000 – 0 ms<br/>                     0001 – 1 ms<br/>                     0010 – 2 ms<br/>                     0011 – 3 ms<br/>                     ...<br/>                     1110 – 14 ms<br/>                     1111 – 15 ms</p> |
| DLY2[3:0]  | <p>DLY2 delay time set; defines the delay time from STROBE2 to STROBE3 during power-up and from STROBE3 to STROBE2 during power-down.</p> <p>0000 – 0 ms<br/>                     0001 – 1 ms<br/>                     0010 – 2 ms<br/>                     0011 – 3 ms<br/>                     ...<br/>                     1110 – 14 ms<br/>                     1111 – 15 ms</p> |

**THERMISTOR CONFIGURATION REGISTER (TMST\_CONFIG)**

Address – 0x0Ch

| DATA BIT    | D7         | D6       | D5       | D4              | D3  | D2            | D1       | D0       |
|-------------|------------|----------|----------|-----------------|-----|---------------|----------|----------|
| FIELD NAME  | READ_THERM | Not used | CONV_END | FAULT_QUE [1:0] |     | FAULT_QUE_CLR | Not used | Not used |
| READ/WRITE  | R/W        | R        | R        | R/W             | R/W | R/W           | R        | R        |
| RESET VALUE | 0          | 0        | 1        | 0               | 0   | 0             | 0        | 0        |

| FIELD NAME      | BIT DEFINITION                                                                                                                                     |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| READ_THERM      | Read thermistor value<br>1 – Initiates temperature acquisition<br>0 – No effect<br>NOTE: bit is self-cleared after acquisition is completed        |
| Not used        | N/A                                                                                                                                                |
| CONV_END        | ADC conversion done flag<br>1 – Conversion is finished<br>0 – Conversion is not finished                                                           |
| FAULT_QUE [1:0] | Number of faults to detect before TMST_HOT interrupt is asserted<br>00 – 1 time<br>01 – 2 times<br>10 – 4 times<br>11 – 6 times                    |
| FAULT_QUE_CLR   | Fault counter clear<br>1 – Clears fault counter<br>0 – Fault counter is cleared automatically if thermistor reading is less than TMST_HOT_SET[7:0] |
| Not used        | N/A                                                                                                                                                |
| Not used        | N/A                                                                                                                                                |

## THERMISTOR HOT THRESHOLD (TMST\_OS)

Address – 0x0Dh

| DATA BIT    | D7                | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|-------------|-------------------|-----|-----|-----|-----|-----|-----|-----|
| FIELD NAME  | TMST_HOT_SET[7:0] |     |     |     |     |     |     |     |
| READ/WRITE  | R/W               | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0                 | 0   | 1   | 1   | 0   | 0   | 1   | 0   |

| FIELD NAME        | BIT DEFINITION                       |
|-------------------|--------------------------------------|
| TMST_HOT_SET[7:0] | Defined the thermistor HOT threshold |
|                   | 1000 0000 – Reserved                 |
|                   | ...                                  |
|                   | 1111 0101 – Reserved                 |
|                   | 1111 0110 – -10°C                    |
|                   | 1111 0111 – -9°C                     |
|                   | ...                                  |
|                   | 1111 1110 – -2°C                     |
|                   | 1111 1111 – -1°C                     |
|                   | 0000 0000 – 0°C                      |
|                   | 0000 0001 – 1°C                      |
|                   | 0000 0010 – 2°C                      |
|                   | ...                                  |
|                   | 0001 1001 – 25°C                     |
|                   | ...                                  |
|                   | 0011 0010 – 50°C                     |
|                   | ...                                  |
|                   | 0101 0101 – 85°C                     |
|                   | 0101 0110 – Reserved                 |
|                   | ...                                  |
|                   | 0111 1111 – Reserved                 |

## THERMISTOR COOL THRESHOLD (TMST\_HYST)

Address – 0x0Eh

| DATA BIT    | D7                 | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|-------------|--------------------|-----|-----|-----|-----|-----|-----|-----|
| FIELD NAME  | TMST_COOL_SET[7:0] |     |     |     |     |     |     |     |
| READ/WRITE  | R/W                | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| RESET VALUE | 0                  | 0   | 1   | 0   | 1   | 1   | 0   | 1   |

| FIELD NAME        | BIT DEFINITION                       |
|-------------------|--------------------------------------|
| TMST_HOT_SET[7:0] | Defined the thermistor HOT threshold |
|                   | 1000 0000 – Reserved                 |
|                   | ...                                  |
|                   | 1111 0101 – Reserved                 |
|                   | 1111 0110 – -10°C                    |
|                   | 1111 0111 – -9°C                     |
|                   | ...                                  |
|                   | 1111 1110 – -2°C                     |
|                   | 1111 1111 – -1°C                     |
|                   | 0000 0000 – 0°C                      |
|                   | 0000 0001 – 1°C                      |
|                   | 0000 0010 – 2°C                      |
|                   | ...                                  |
|                   | 0001 1001 – 25°C                     |
|                   | ...                                  |
|                   | 0010 1101 – 45°C                     |
|                   | ...                                  |
|                   | 0101 0101 – 85°C                     |
|                   | 0101 0110 – Reserved                 |
|                   | ...                                  |
|                   | 0111 1111 – Reserved                 |

## POWER GOOD STATUS (PG\_STATUS)

Address – 0x0Fh

| DATA BIT    | D7    | D6      | D5    | D4      | D3     | D2       | D1      | D0       |
|-------------|-------|---------|-------|---------|--------|----------|---------|----------|
| FIELD NAME  | VB_PG | VDDH_PG | VN_PG | VPOS_PG | VEE_PG | Not used | VNEG_PG | Not used |
| READ/WRITE  | R     | R       | R     | R       | R      | R        | R       | R        |
| RESET VALUE | 0     | 0       | 0     | 0       | 0      | 0        | 0       | 0        |

| FIELD NAME | BIT DEFINITION                      |
|------------|-------------------------------------|
| VB_PG      | Positive boost converter power good |
| VDDH_PG    | VDDH power good                     |
| VN_PG      | Inverting buck-boost power good     |
| VPOS_PG    | VPOS power good                     |
| VEE_PG     | VEE power good                      |
| not used   | N/A                                 |
| VNEG_PG    | VNEG power good                     |
| not used   | N/A                                 |

## REVISION AND VERSION CONTROL (REVID)

Address – 0x10h

| DATA BIT    | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----|----|----|----|----|----|----|
| FIELD NAME  | REVID[7:0] |    |    |    |    |    |    |    |
| READ/WRITE  | R          | R  | R  | R  | R  | R  | R  | R  |
| RESET VALUE | 0          | 1  | 1  | 1  | 0  | 0  | 0  | 0  |

| FIELD NAME  | BIT DEFINITION                                                                                                                                                                                                                                                               |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REVID [7:0] | 0101 0000 - TPS65180 1p1<br>0110 0000 - TPS65180 1p2<br>0111 0000 - TPS65180B (TPS65180 1p3)<br>1000 0000 - TPS65180B (TPS65180 1p4)<br>0101 0001 - TPS65181 1p1<br>0110 0001 - TPS65181 1p2<br>0111 0001 - TPS65181B (TPS65181 1p3)<br>1000 0001 - TPS65181B (TPS65181 1p4) |

## I<sup>2</sup>C READ POINTER CONTROL (FIX\_READ\_POINTER) (TPS65181/TPS65181B ONLY)

Address – 0x11h

| DATA BIT    | D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0         |
|-------------|----------|----------|----------|----------|----------|----------|----------|------------|
| FIELD NAME  | Not used | Not used | Not used | Not used | Not used | Not used | Not used | FIX_RD_PTR |
| READ/WRITE  | R        | R        | R        | R        | R        | R        | R        | R/W        |
| RESET VALUE | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0          |

| FIELD NAME | BIT DEFINITION                                                                                                                        |
|------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Not used   | N/A                                                                                                                                   |
| Not used   | N/A                                                                                                                                   |
| Not used   | N/A                                                                                                                                   |
| Not used   | N/A                                                                                                                                   |
| Not used   | N/A                                                                                                                                   |
| Not used   | N/A                                                                                                                                   |
| Not used   | N/A                                                                                                                                   |
| FIX_RD_PTR | I <sup>2</sup> C read pointer control<br>1 – Read pointer is fixed to 0x00<br>0 – read pointer is controlled through I <sup>2</sup> C |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS65180BRGZR    | ACTIVE        | VQFN         | RGZ                | 48   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -10 to 85    | E INK<br>TPS65180B      | <a href="#">Samples</a> |
| TPS65180BRGZT    | ACTIVE        | VQFN         | RGZ                | 48   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -10 to 85    | E INK<br>TPS65180B      | <a href="#">Samples</a> |
| TPS65180RGZR     | NRND          | VQFN         | RGZ                | 48   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -10 to 85    | E INK<br>TPS65180       |                         |
| TPS65180RGZT     | NRND          | VQFN         | RGZ                | 48   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -10 to 85    | E INK<br>TPS65180       |                         |
| TPS65181BRGZR    | ACTIVE        | VQFN         | RGZ                | 48   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -10 to 85    | E INK<br>TPS65181B      | <a href="#">Samples</a> |
| TPS65181BRGZT    | ACTIVE        | VQFN         | RGZ                | 48   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -10 to 85    | E INK<br>TPS65181B      | <a href="#">Samples</a> |
| TPS65181RGZR     | NRND          | VQFN         | RGZ                | 48   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -10 to 85    | E INK<br>TPS65181       |                         |
| TPS65181RGZT     | NRND          | VQFN         | RGZ                | 48   |                | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -10 to 85    | E INK<br>TPS65181       |                         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

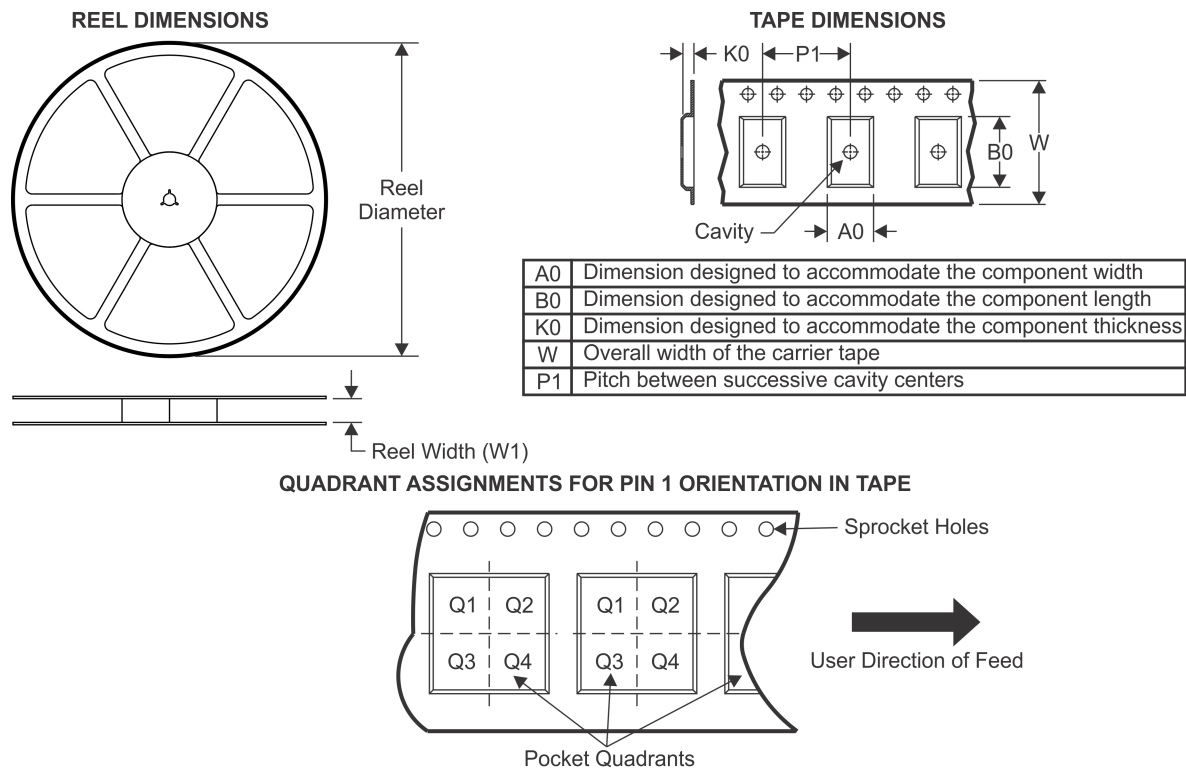
<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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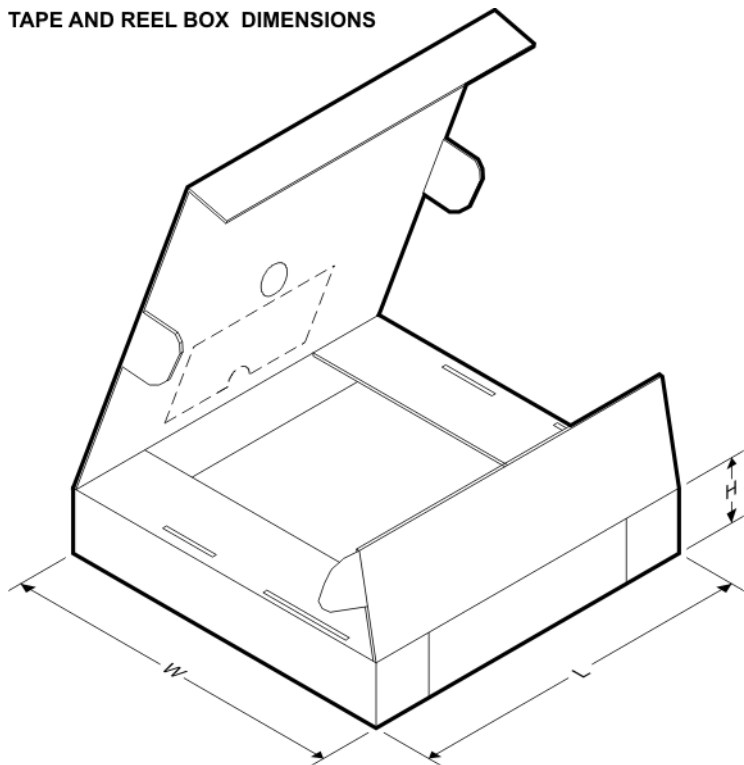
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS65180BRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| TPS65180BRGZT | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| TPS65180RGZR  | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| TPS65180RGZT  | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| TPS65181BRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| TPS65181BRGZT | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| TPS65181RGZR  | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

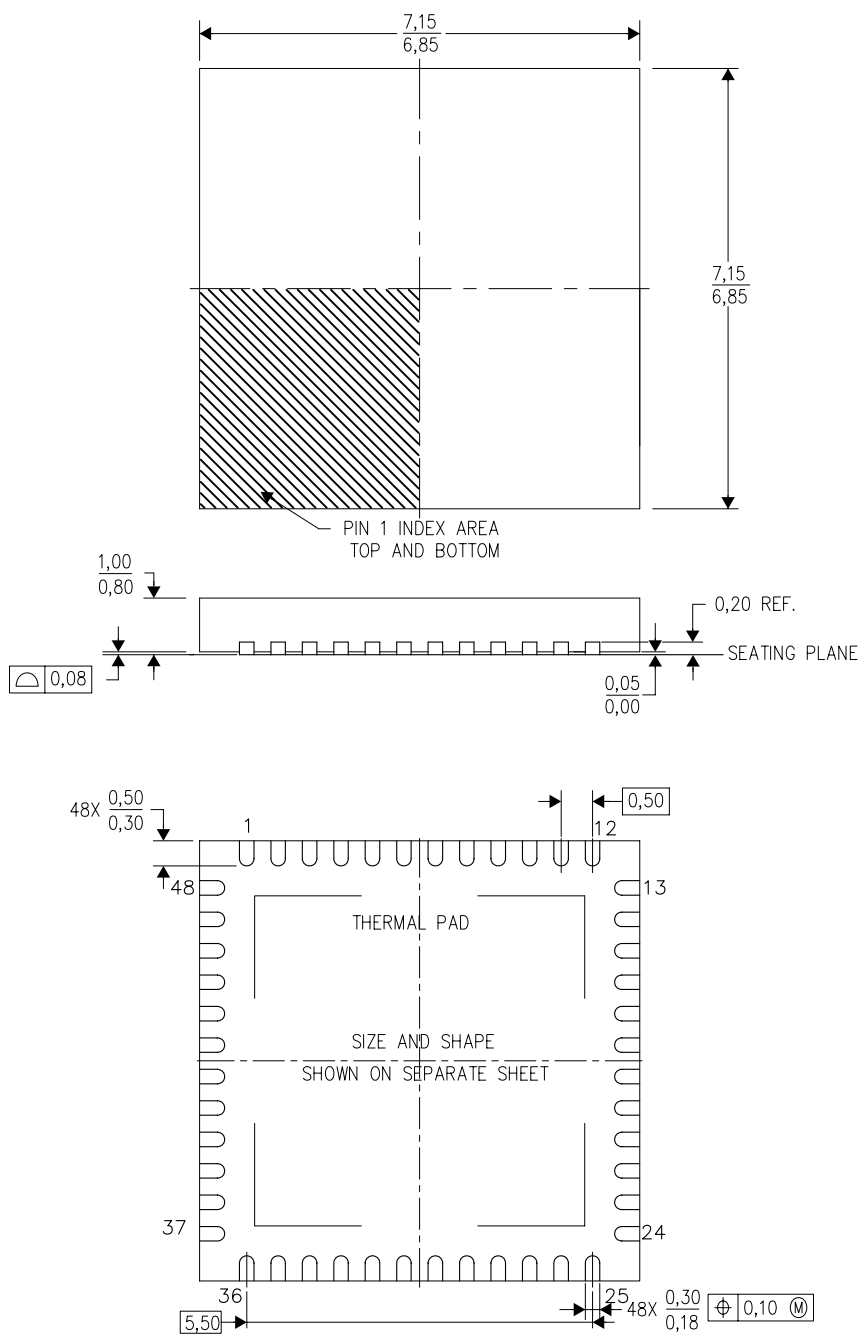


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65180BRGZR | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| TPS65180BRGZT | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| TPS65180RGZR  | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| TPS65180RGZT  | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| TPS65181BRGZR | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| TPS65181BRGZT | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| TPS65181RGZR  | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

RGZ (S-PVQFN-N48)

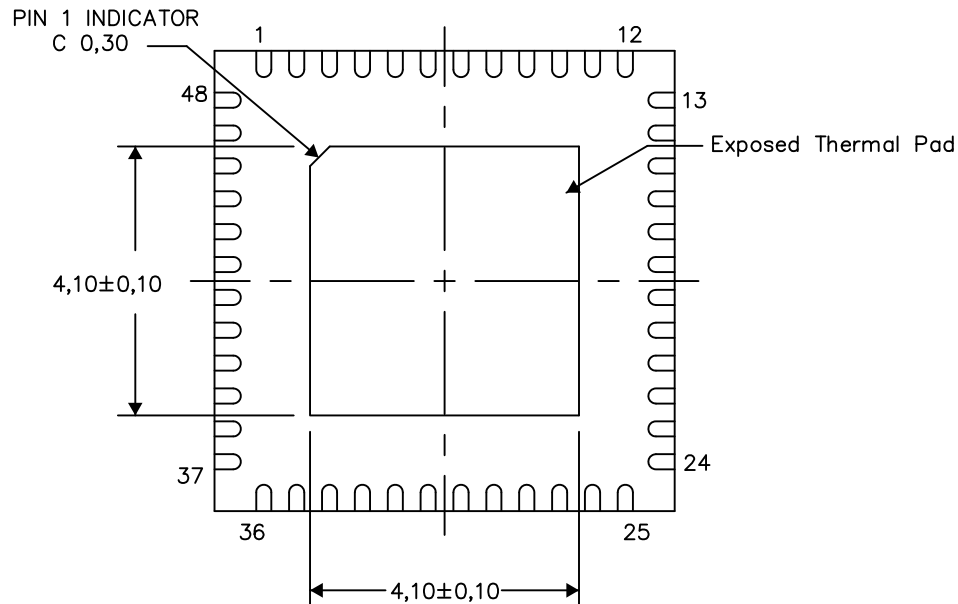
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

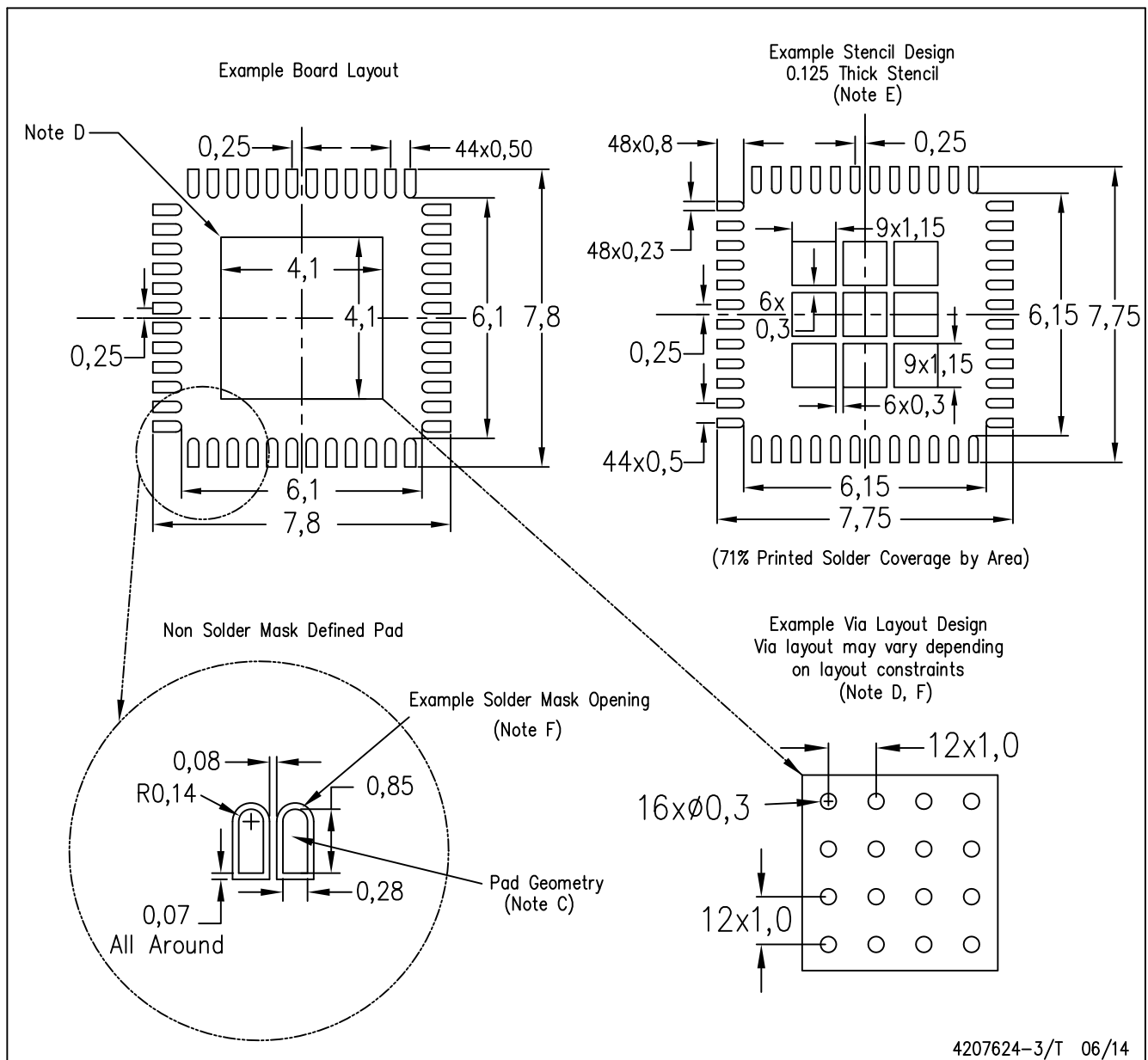
Exposed Thermal Pad Dimensions

4206354-3/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4207624-3/T 06/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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|                               |                                                                                          |
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