

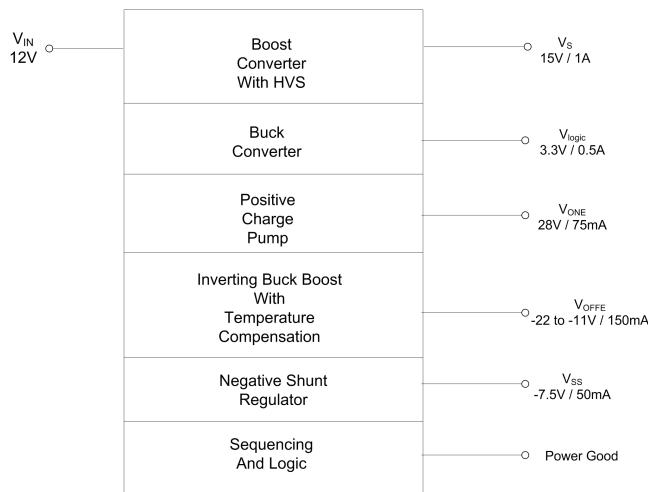
## Compact LCD Bias Supply for TFT-LCD TV Panels

 Check for Samples: [TPS65171](#)

### FEATURES

- 8.5V to 14.7V Input Voltage Range
- $V_s$  Output Voltage Range up to 19V
- Boost Converter with 2.5A Switch Current
- Step Down Converter with 1A Switch Current and Adjustable Output 2.5V to 3.3V
- 750kHz Fixed Switching Frequency
- Temperature Compensated Negative Supply
- High Voltage Stress Test (HVS)
- Adjustable Sequencing
- Gate Drive Signal for Isolation Switch
- Short Circuit Protection
- Internal Soft-Start
- 180° Phase Shift Between Buck and Boost
- P2P Short/Open Certified
- Optimized Dual Layer PCB Layout
- Low EMI
- Undervoltage Lockout
- Thermal Shutdown
- Available in 6x6mm 40 Pin QFN Package

### TYPICAL APPLICATION



### APPLICATIONS

- LCD TV Panel with ASG Technology

### DESCRIPTION

The TPS65171 offers a compact power supply solution to provide all voltages required by a LCD panel for large TV panel applications running from a 12V supply rail. The device is optimized to support LCD technology using ASG gate drive circuits.

The device generates all voltage rails for the TFT LCD bias ( $V_s$ ,  $V_{ONE}$ ,  $V_{OFFE}$ ,  $V_{ss}$ ). In addition to that it includes a step-down converter ( $V_{logic}$ ) to provide the logic voltage. By pulling the HVS pin high an implemented high voltage stress test feature programs the boost converter output voltage  $V_s$  to higher values. The boost converter operates at a fixed switching frequency of 750kHz. The positive charge pump is running from the boost converter and is regulated by an external transistor. A buck-boost converter provides an adjustable temperature dependent negative output voltage  $V_{OFFE}$ . The negative output voltage  $V_{ss}$  is regulated by a shunt regulator.

Safety features like overvoltage protection of the buck-boost input voltage, the boost and buck output voltage, undervoltage lockout, short circuit protection of  $V_{ONE}$ ,  $V_{OFFE}$ , and  $V_{logic}$  are included as well as thermal shutdown.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1) (2)</sup>

T <sub>A</sub>	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65171RHAR	6 x 6mm 40 Pin QFN	TPS65171

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The RHA package is available taped and reeled. Add R suffix to the device type (TPS65171RHAR) to order the device taped and reeled. The RHA package has quantities of 3000 devices per reel.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	VALUE	UNIT
Input voltage range AVIN, VIN1, VIN2, VIN3 <sup>(2)</sup>	–0.3 to 20	V
Voltage range at SW1, SW2, SW3, SW4, GD, BASE2, RHVS, OS	–0.3 to 20	V
Voltage range at EN1, EN2, HVS	–0.3 to 20	V
Voltage range at COMP, SS, FB1, VSNS, FB2, FB3, FB4, TS, SET, FB5, DLY1, DLY2, PG	–0.3 to 7.0	V
Voltage difference VIN3 to SW5	40	V
BASE1	–9.5 to 0.3	V
ESD rating, Human Body Model	2	kV
ESD rating, Machine Model	200	V
ESD rating, Charged Device Model	700	V
Continuous total power dissipation	See Dissipation Rating Table	
Operating junction temperature range, T <sub>J</sub>	–40 to 150	°C
Operating ambient temperature range, T <sub>A</sub>	–40 to 85	°C
Storage temperature range, T <sub>stg</sub>	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## DISSIPATION RATINGS<sup>(1)</sup>

PACKAGE	R <sub>θJA</sub>	T <sub>A</sub> ≤ 25°C POWER RATING	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
40 pin QFN	35°C/W	2.8W	1.6W	1.1W

- (1) Soldered Power Pad on a standard 2-Layer PCB without vias for thermal pad. See the Texas Instruments Application report ([SLMA002](#)) regarding thermal characteristics of the PowerPAD package.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

	MIN	TYP	MAX	UNIT
V <sub>IN</sub> Input voltage range (AVIN, VIN1, VIN2, VIN3)	8.5	14.7		V
V <sub>IN3</sub> Overvoltage protection 15V for buck-boost converter	15			V
T <sub>A</sub> Operating ambient temperature	–40	85		°C
T <sub>J</sub> Operating junction temperature	–40	125		°C

- (1) Refer to application section for further information

## ELECTRICAL CHARACTERISTICS

AVIN=VIN1=VIN2=VIN3=12V, EN1=EN2=VIN, VS=15V, V<sub>logic</sub>=3.3V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY CURRENT</b>						
V <sub>IN</sub>	Input voltage range	8.5	14.7		V	
I <sub>QIN</sub>	Quiescent current into AVIN, VIN1,2,3	Not switching, FB=FB+5%	1.2		mA	
I <sub>sd</sub>	Shutdown current into AVIN, VIN1,2,3	EN1=EN2=GND	170		μA	
V <sub>UVLO</sub>	Under-voltage lockout threshold	V <sub>IN</sub> falling	8.0	8.2	V	
V <sub>UVLO</sub>	Under-voltage lockout threshold	V <sub>IN</sub> rising	8.2	8.5	V	
	Thermal shutdown	Temperature rising	150		°C	
	Thermal shutdown hysteresis		15		°C	
<b>LOGIC SIGNALS EN1, EN2, HVS</b>						
V <sub>IH</sub>	High level input voltage	V <sub>IN</sub> = 8.5V to 14.7V	1.7		V	
V <sub>IL</sub>	Low level input voltage	V <sub>IN</sub> = 8.5V to 14.7V		0.4	V	
I <sub>I</sub>	Input leakage current	EN1=EN2=GND	0.01	0.1	μA	
<b>POWER GOOD</b>						
V <sub>IL</sub>	Low level voltage <sup>(1)</sup>	I <sub>(sink)</sub> = 500μA		0.3	V	
I <sub>lk</sub>	Leakage current	V <sub>PG</sub> = 5.0V	0.01	0.1	μA	
<b>SEQUENCING DLY1, DLY2, and SOFT-START</b>						
I <sub>chrg</sub>	DLY1, DLY2 charge current	V <sub>threshold</sub> = 1.24V	4	4.9	6.3	μA
V <sub>threshold</sub>	DLY1, DLY2 threshold voltage		1.21	1.24	1.27	V
R <sub>dischrg</sub>	DLY1, DLY2 discharge resistor			3.2		kΩ
I <sub>ss</sub>	Soft-start charge current	V <sub>threshold</sub> = 1.24V	8	10	12	μA
<b>SWITCHING FREQUENCY</b>						
f <sub>s</sub>	Switching frequency		600	750	900	kHz
<b>BOOST CONVERTER (V<sub>s</sub>)</b>						
V <sub>s</sub>	Output voltage range			19	V	
V <sub>swovp</sub>	Switch overvoltage protection	V <sub>s</sub> rising	19.0	19.5	20	V
V <sub>FB1</sub>	Feedback regulation voltage		1.225	1.24	1.252	V
I <sub>FB1</sub>	Feedback input bias current	V <sub>FB1</sub> = 1.24V		10	100	nA
R <sub>DS(on)</sub>	N-MOSFET on-resistance	I <sub>sw</sub> = 500mA		120	170	mΩ
I <sub>LIM</sub>	N-MOSFET switch current limit		2.5	3.2	4.0	A
I <sub>leak</sub>	Switch leakage current	V <sub>sw</sub> = 15V	1	10		μA
t <sub>on</sub>	Minimum on time			80		ns
	Line regulation	8.5V ≤ V <sub>IN</sub> ≤ 14.7V, I <sub>out</sub> = 1mA		0.006		%/V
	Load regulation	1mA ≤ I <sub>out</sub> ≤ 1A		0.1		%/A
<b>GATE DRIVE (GD) AND BOOST CONVERTER PROTECTION</b>						
VGD <sub>M</sub>	V <sub>IN</sub> – V <sub>GD</sub> <sup>(2)</sup>	V <sub>IN</sub> = 12V, GD pulled down	5	6	7	V
I <sub>(GD)</sub>	Gate drive sink current	EN2 = high		10		μA
R <sub>(GD)</sub>	Gate drive internal pull up resistance			10		kΩ
t <sub>on</sub>	Gate on time during short circuit	FB1 < 100mV		1.4		ms
<b>BUCK CONVERTER (V<sub>logic</sub>)</b>						
V <sub>logic</sub>	Output voltage range		2.2	4.0	V	
V <sub>FB2</sub>	Feedback regulation voltage	FB2 connected to resistor divider, I <sub>load</sub> = 10mA	1.215	1.24	1.265	V
I <sub>FB2</sub>	Feedback input bias current	V <sub>FB2</sub> = 1.24V		10	100	nA
R <sub>DS(on)</sub>	N-MOSFET on-resistance	I <sub>sw3</sub> , I <sub>sw4</sub> = 0.5A		150	250	mΩ

(1) PG goes high impedance once V<sub>s</sub> and V<sub>ONE</sub> are in regulation.

(2) GD goes to V<sub>IN</sub> – V<sub>GD</sub> once the boost converter V<sub>s</sub> is enabled.

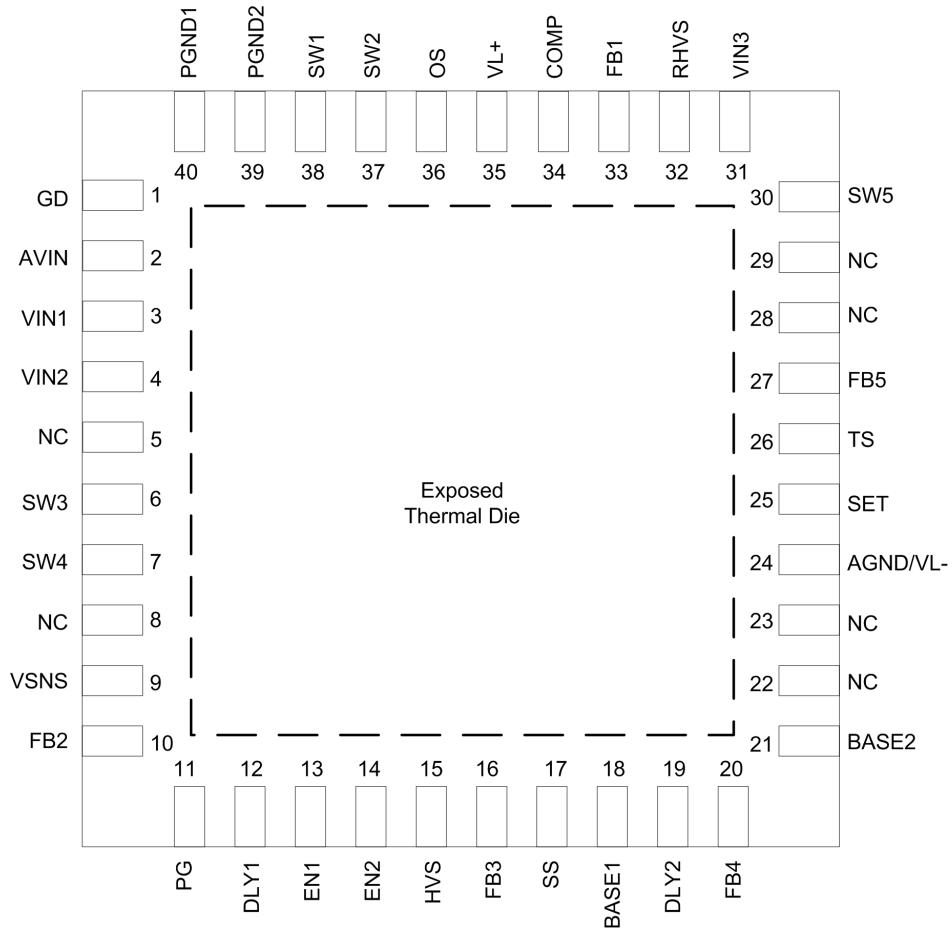
## ELECTRICAL CHARACTERISTICS (continued)

AVIN=VIN1=VIN2=VIN3=12V, EN1=EN2=VIN, VS=15V, V<sub>logic</sub>=3.3V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I <sub>LIM</sub> N-MOSFET switch current limit		1			A	
I <sub>leak</sub> Switch leakage current	V <sub>sw</sub> = 0V		1		µA	
Line regulation	8.5V ≤ V <sub>IN</sub> ≤ 14.7V, I <sub>out</sub> = 1mA		0.006		%/V	
Load regulation	1mA ≤ I <sub>out</sub> ≤ 100mA		0.042		%/mA	
	100mA ≤ I <sub>out</sub> ≤ 1A		0.06		%/A	
<b>NEGATIVE SHUNT REGULATOR (V<sub>ss</sub>)</b>						
V <sub>Base1</sub> Base1 voltage range	Transistor leakage maximum 5µA	-9.5	0.3		V	
I <sub>Base1</sub> Base1 drive source current	V <sub>FB3</sub> = V <sub>FB3nominal</sub> - 5%	5			mA	
V <sub>FB3</sub> Feedback regulation voltage		-5%	0.75 × V <sub>logic</sub>	5%	V	
I <sub>FB3</sub> Feedback input bias current	V <sub>FB3</sub> = 1.24V	10	100		nA	
Line regulation	8.5V ≤ V <sub>IN</sub> ≤ 14.7V, I <sub>out</sub> = 1mA	0.006			%/V	
Load regulation	1mA ≤ I <sub>out</sub> ≤ 50mA	0.0004			%/mA	
<b>NEGATIVE BUCK BOOST CONVERTER (V<sub>OFFE</sub>)</b>						
V <sub>ovp</sub> VIN3 overvoltage protection		15			V	
V <sub>OFFE</sub> Adjustable output voltage range		-22	-5		V	
R <sub>DS(on)</sub> P-MOSFET on resistance	I <sub>sw5</sub> at current limit	0.9	1.6		Ω	
I <sub>LIM</sub> P-MOSFET current limit		0.8	1		A	
V <sub>FB5</sub>	Regulation accuracy upper limit	V <sub>TS</sub> = 1V, V <sub>SET</sub> = 1.9V	1.8	1.9	2.0	V
	Regulation accuracy	V <sub>TS</sub> = 1V, V <sub>SET</sub> = 2.4V	1.9	2	2.1	V
	Regulation accuracy lower limit	V <sub>TS</sub> = 0.7V, V <sub>SET</sub> = 2.4V	1.57	1.65	1.73	V
I <sub>FB5</sub> Feedback input bias current	V <sub>FB5</sub> = 2V	10	100		nA	
I <sub>TS</sub> TS input bias current	V <sub>TS</sub> = 1V	10	100		nA	
I <sub>SET</sub> SET input bias current	V <sub>SET</sub> = 3V	3	5		µA	
Line regulation	8.5V ≤ V <sub>IN</sub> ≤ 14.7V, I <sub>out</sub> = 1mA	0.003			%/V	
Load regulation	1mA ≤ I <sub>out</sub> ≤ 150mA, V <sub>OFFE</sub> = -11V	0.0005			%/mA	
<b>POSITIVE CHARGE PUMP (V<sub>ONE</sub>)</b>						
I <sub>Base2</sub>	Base2 drive sink current	V <sub>FB4</sub> = V <sub>FB4nominal</sub> -5%	8	14		mA
	Base2 drive sink current (SC-Mode)	V <sub>FB4</sub> = GND	40	50	70	µA
V <sub>Base2</sub> Base drive voltage range				20		V
V <sub>FB4</sub> Feedback regulation voltage		1.18	1.24	1.30		V
I <sub>FB4</sub>	Feedback input bias current	V <sub>FB4</sub> = 1.24V	10	100		nA
	Line regulation	8.5V ≤ V <sub>IN</sub> ≤ 14.7V, I <sub>out</sub> = 1mA	0.9			%/V
	Load regulation	1mA ≤ I <sub>out</sub> ≤ 75mA	0.004			%/mA
<b>HIGH VOLTAGE STRESS TEST (HVS), RHVS</b>						
RHVS RHVS pull down resistance	HVS = high, I <sub>HVS</sub> = 500µA	350	450	550		Ω
I <sub>RHVS</sub> RHVS leakage current	HVS = low, V <sub>RHVS</sub> = 5V			100		nA

## DEVICE INFORMATION

### PACKAGE

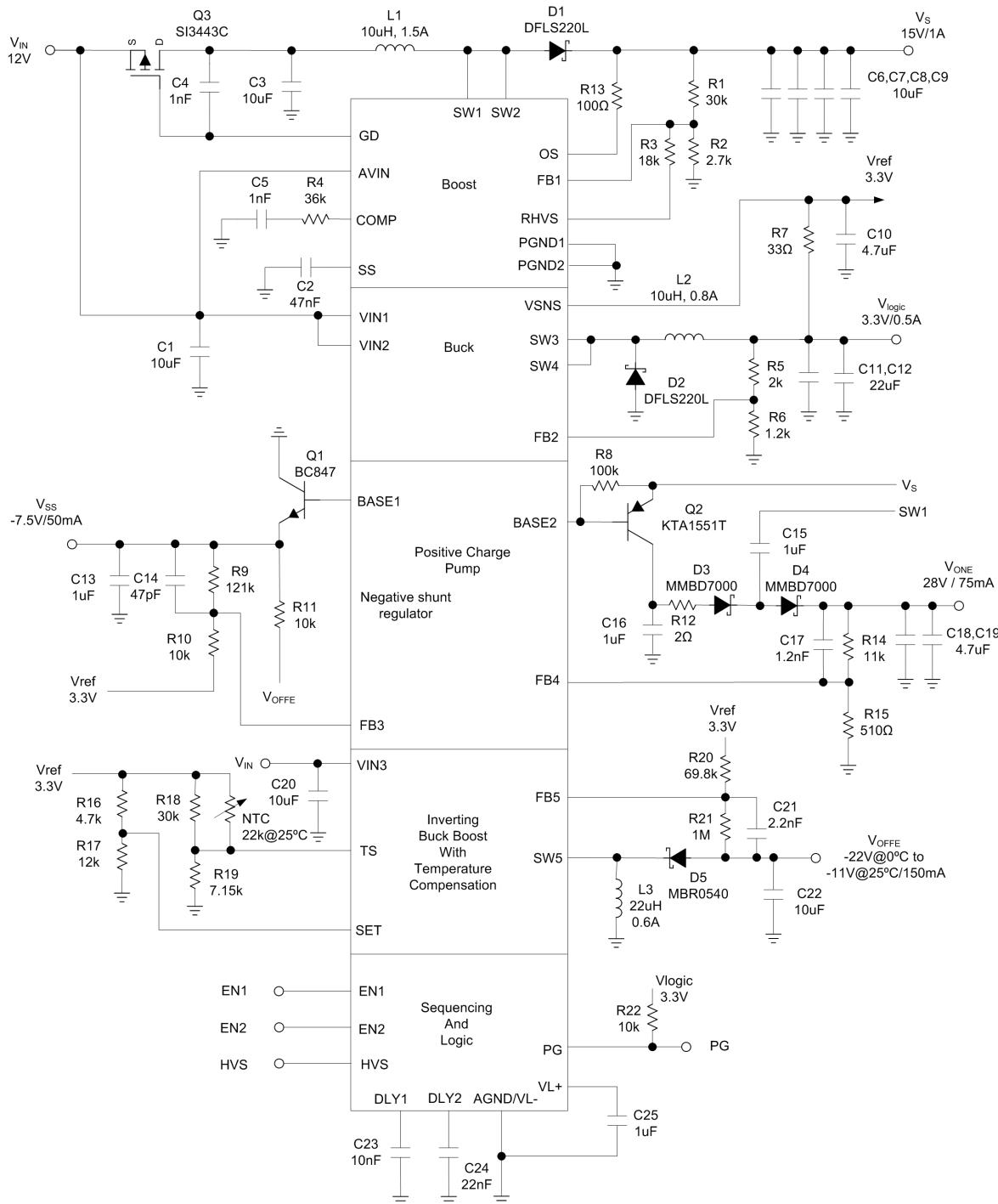


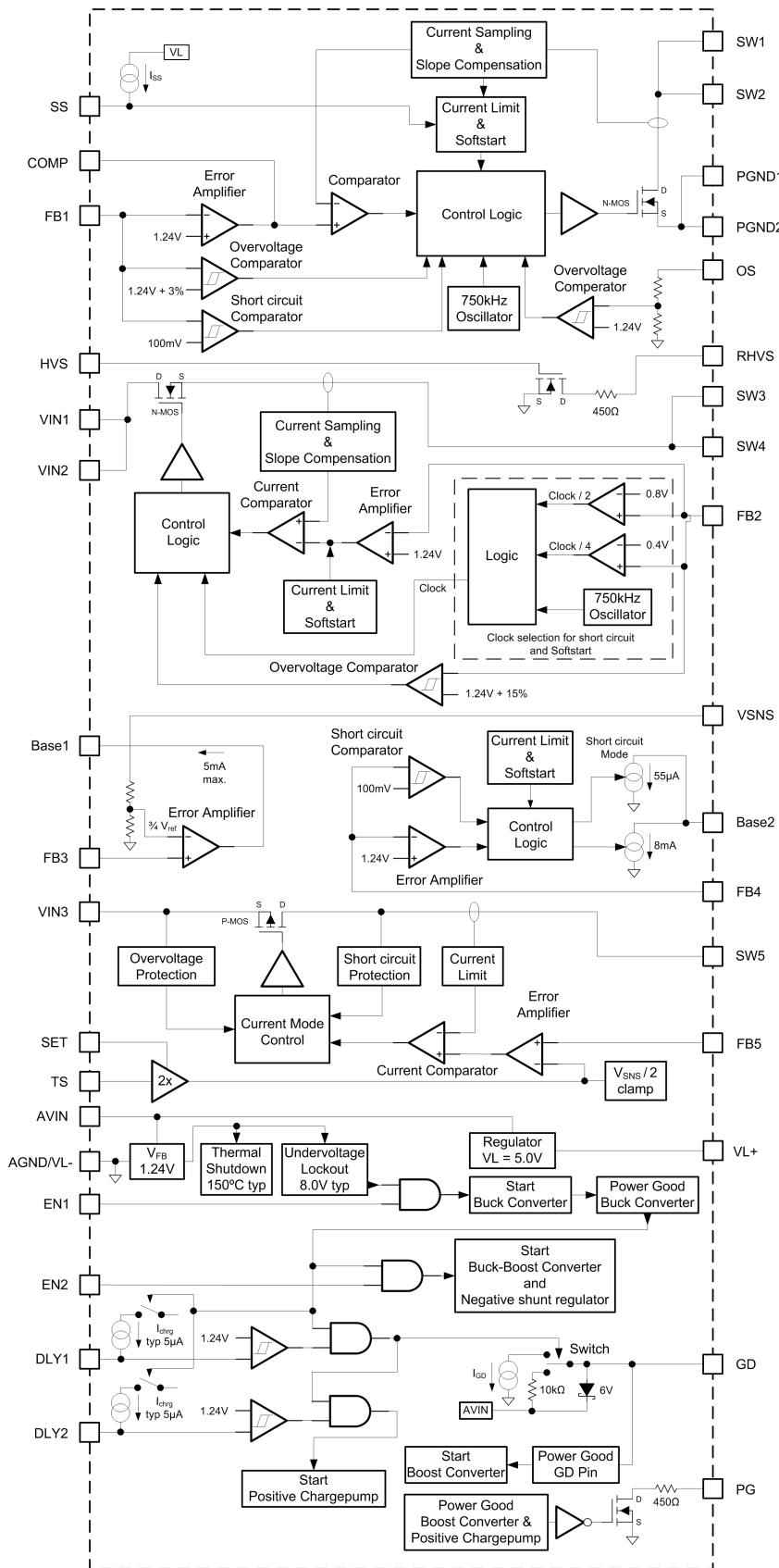
### PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GD	1	I	Gate drive pin for the external isolation MOSFET.
AVIN	2	I	Input voltage supply pin for the analog circuit.
VIN1, VIN2	3,4	I	Input supply for the buck converter generating $V_{\text{logic}}$
NC	5		Not connected
SW3, SW4	6,7	O	Switch pin for the buck converter generating $V_{\text{logic}}$
NC	8		Not connected
VSNS	9	I	Reference voltage input for the buck-boost and negative shunt regulator
FB2	10	I	Feedback pin for the buck converter.
PG	11	I	Power good output latched high when $V_S$ and $V_{\text{ONE}}$ are in regulation
DLY1	12	O	Delay pin EN2 high to enable boost converter $V_S$
EN1	13	I	Enable of the buck converter $V_{\text{logic}}$
EN2	14	I	Enable of the negative supplies $V_{\text{SS}}$ and $V_{\text{OFFE}}$ , enable DLY1 and DLY2
HVS	15	I	Logic pin to enable high voltage stress test. This allows programming the boost converter $V_S$ to a higher voltage
FB3	16	I	Feedback of the negative supply $V_{\text{SS}}$

## PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SS	17	O	Soft-start for the boost converter $V_S$
BASE1	18	O	Base drive of the external npn transistor for the negative supply $V_{SS}$
DLY2	19	O	Delay pin EN2 high to enable charge pump $V_{ONE}$
FB4	20	I	Feedback for the positive supply $V_{ONE}$
BASE2	21	I	Base drive of the external pnp transistor for the positive charge pump $V_{ONE}$
NC	22, 23		Not connected
AGND/VL-	24		Analog ground and connection of the bypass capacitor of VL-
SET	25	I	Input pin for the reference voltage to set the higher limit for the temperature compensation for $V_{OFFE}$
TS	26	I	Input pin for the NTC temperature sensor
FB5	27	I	Feedback pin for the negative buck-boost converter $V_{OFFE}$
NC	28, 29		Not connected
SW5	30	O	Switch pin for the negative buck-boost converter generating $V_{OFFE}$
VIN3	31	I	Input supply for the buck-boost converter generating $V_{OFFE}$
RHVS	32	I	This pin is pulled low when HVS is high. The resistor connected to this pin sets the boost converter output voltage when HVS is pulled high
FB1	33	I	Feedback for the boost converter $V_S$
COMP	34	O	Compensation pin for the boost converter
VL+	35	O	Output of the internal logic regulator. Connect a capacitor between this pin and AGND/VL-
OS	36	I	Connect this pin to the boost converter output for overvoltage protection
SW1, SW2	37, 38	I	Switch pin for the boost converter and the positive charge pump $V_{ONE}$
PGND1, PGND2	39, 40		Power ground for the boost converter $V_S$

**FUNCTIONAL BLOCK DIAGRAM**




**TYPICAL CHARACTERISTICS**
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	Startup sequencing		<a href="#">Figure 2</a>
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	Load transient response buck boost converter		<a href="#">Figure 17</a>
<b>Charge Pump</b>			
	Load transient response positive charge pump	$V_s = 15V$	<a href="#">Figure 19</a>
	Load transient response positive charge pump	$V_s = 18V$	<a href="#">Figure 20</a>
<b>Shunt Regulator</b>			
	Load transient response negative shunt regulator		<a href="#">Figure 21</a>

STARTUP SEQUENCING

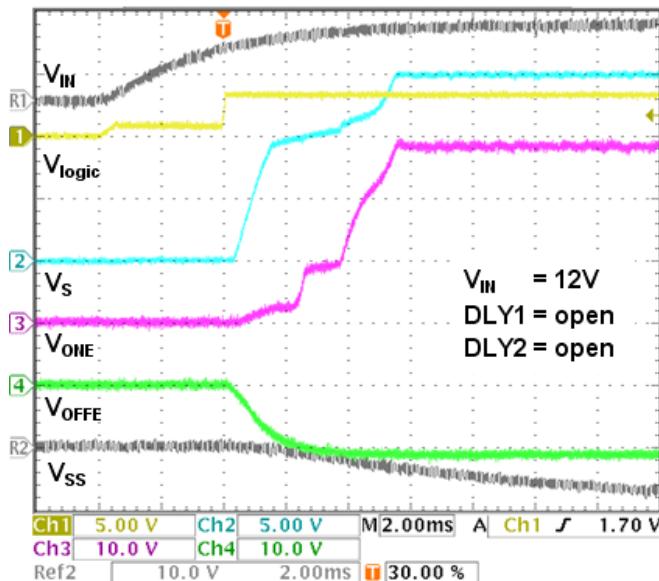


Figure 1.

STARTUP SEQUENCING

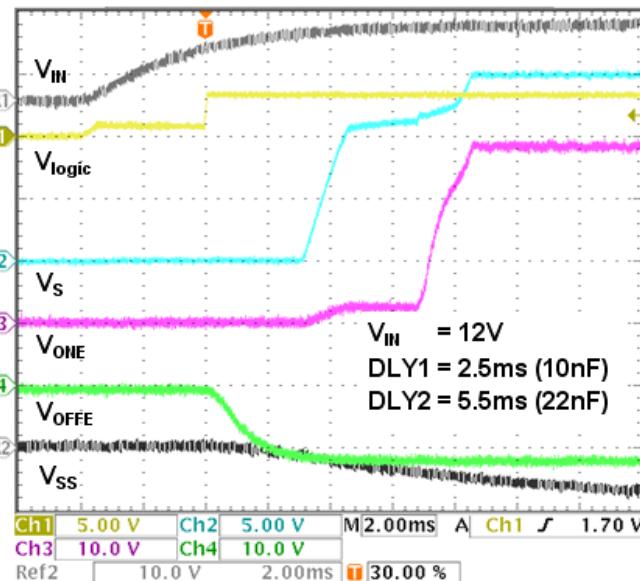


Figure 2.

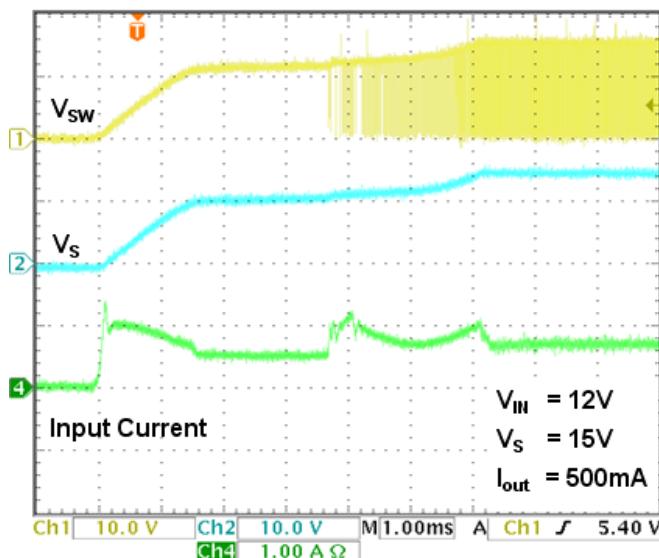
SOFTSTART BOOST CONVERTER  
vs  
LOAD CURRENT

Figure 3.

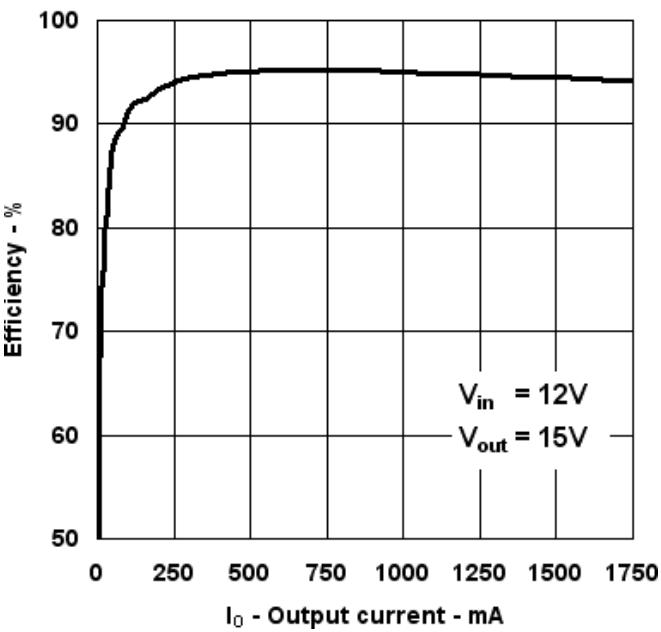
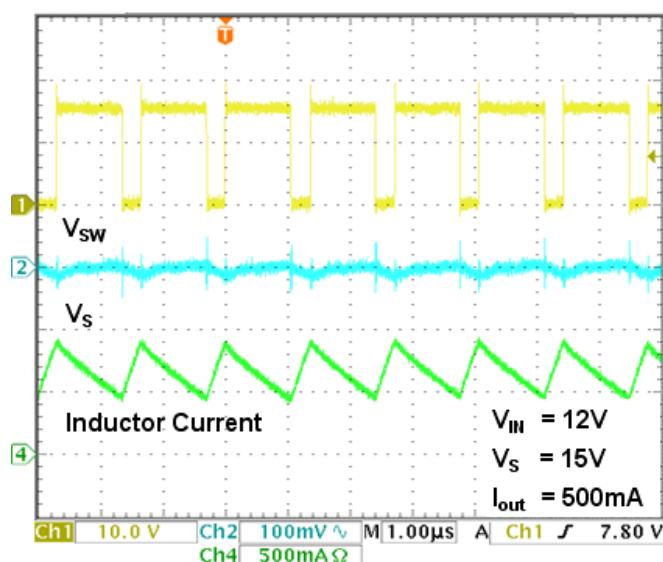
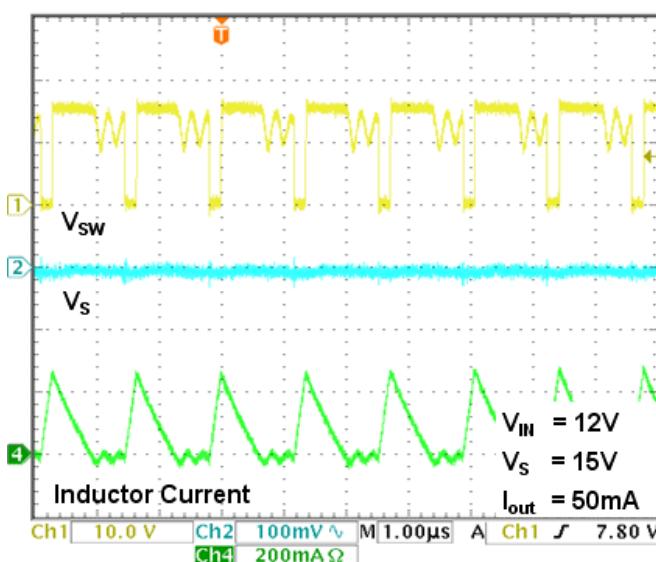
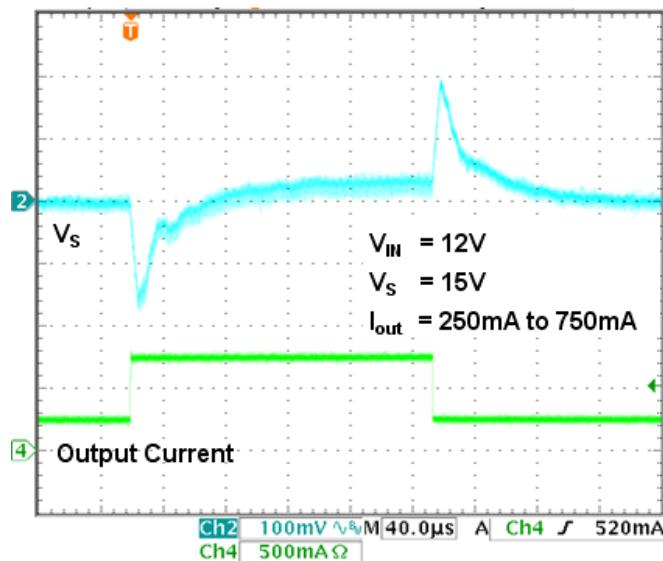
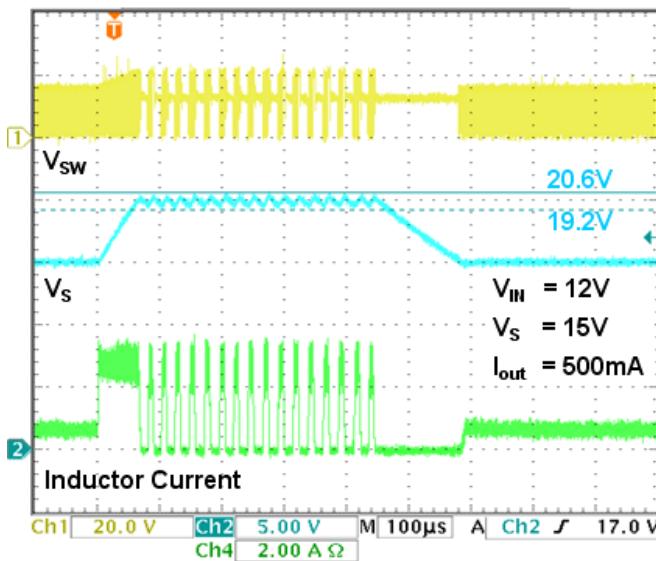
EFFICIENCY BOOST CONVERTER  
vs  
LOAD CURRENT

Figure 4.

**PWM OPERATION AT NOMINAL LOAD CURRENT**

**Figure 5.**
**PWM OPERATION AT LIGHT LOAD CURRENT**

**Figure 6.**
**LOAD TRANSIENT RESPONSE BOOST CONVERTER**

**Figure 7.**
**OVER VOLTAGE PROTECTION**

**Figure 8.**

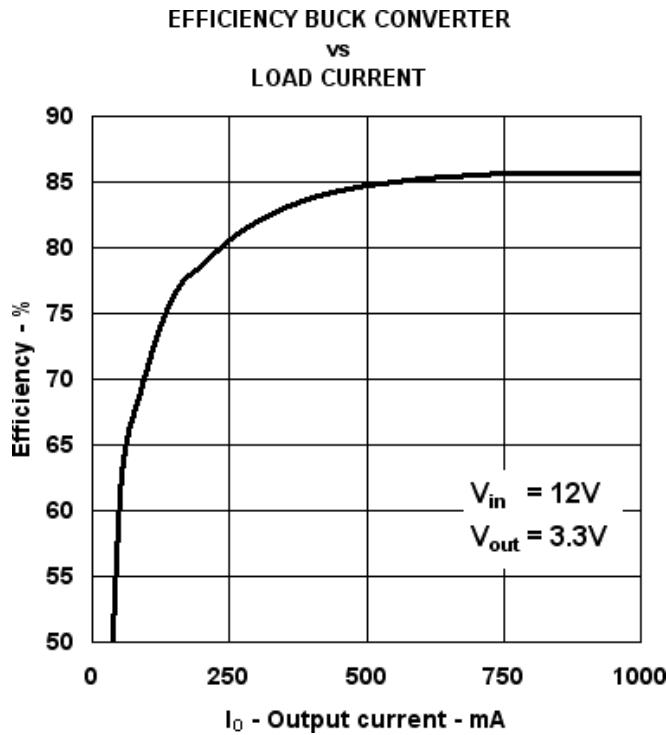


Figure 9.

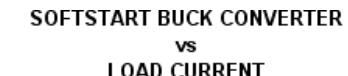


Figure 10.

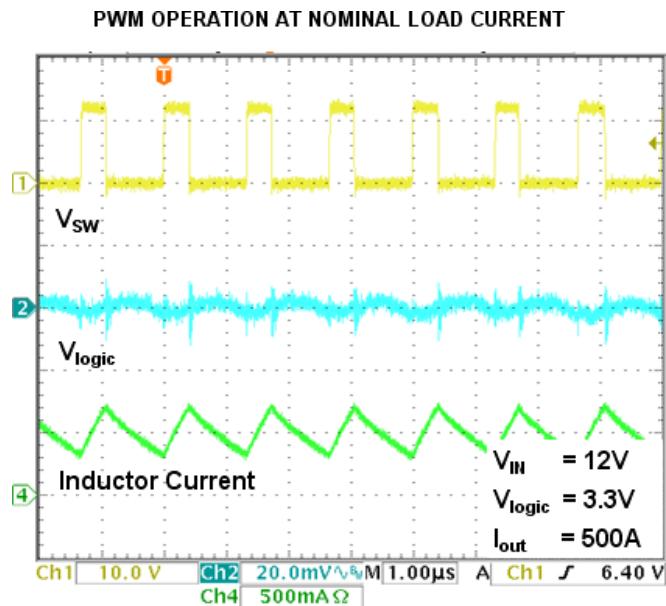
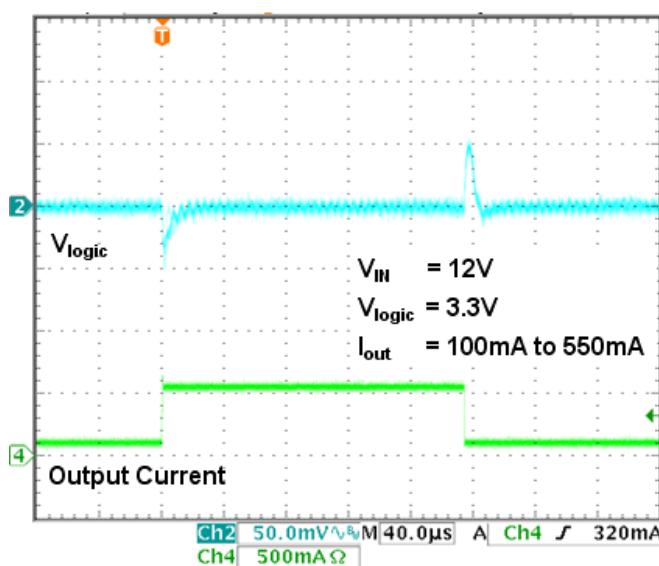
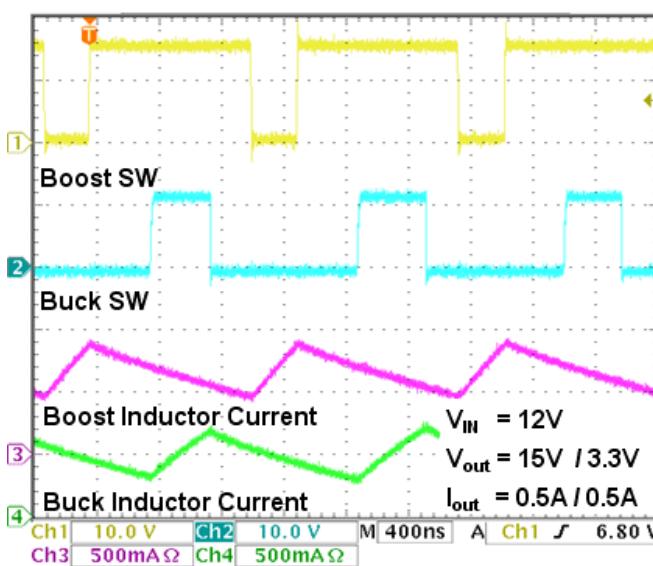
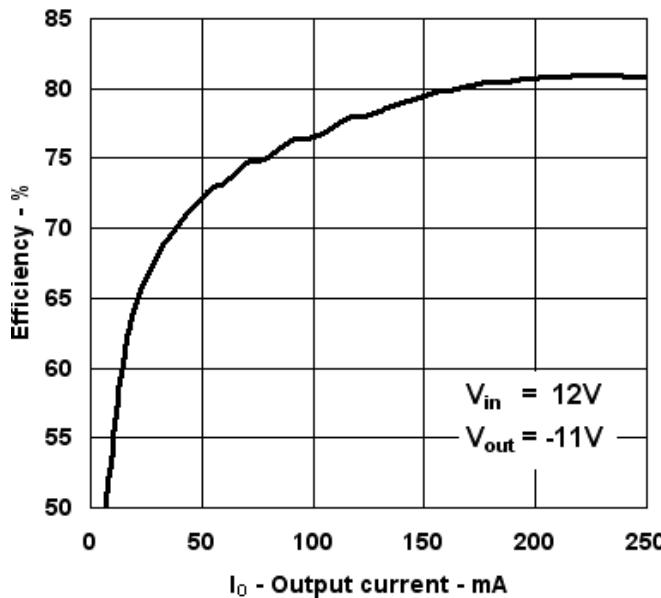
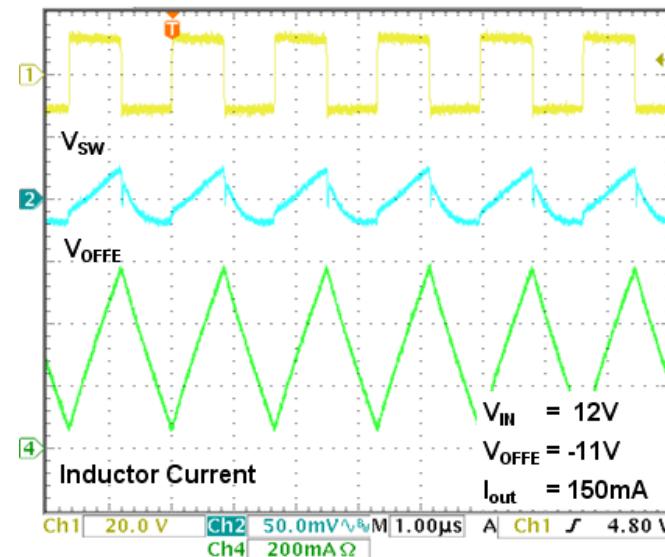


Figure 11.



Figure 12.

**LOAD TRANSIENT RESPONSE BUCK CONVERTER**

**Figure 13.**
**180° PHASE SHIFT BETWEEN BOOST AND BUCK CONVERTER**

**Figure 14.**
**EFFICIENCY BUCK BOOST CONVERTER**
**vs  
LOAD CURRENT**

 **$I_{\text{out}}$  - Output current - mA**
**Figure 15.**
**PWM OPERATION AT NOMINAL LOAD CURRENT**

**Figure 16.**

## PWM OPERATION AT LIGHT LOAD CURRENT

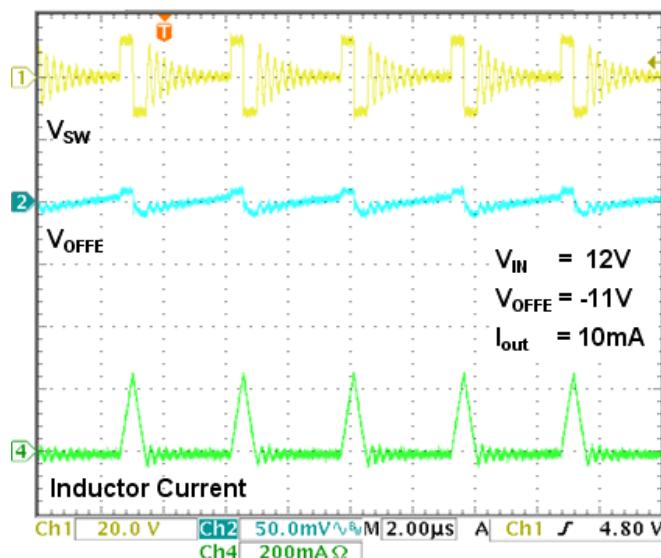


Figure 17.

## LOAD TRANSIENT RESPONSE BUCK BOOST CONVERTER

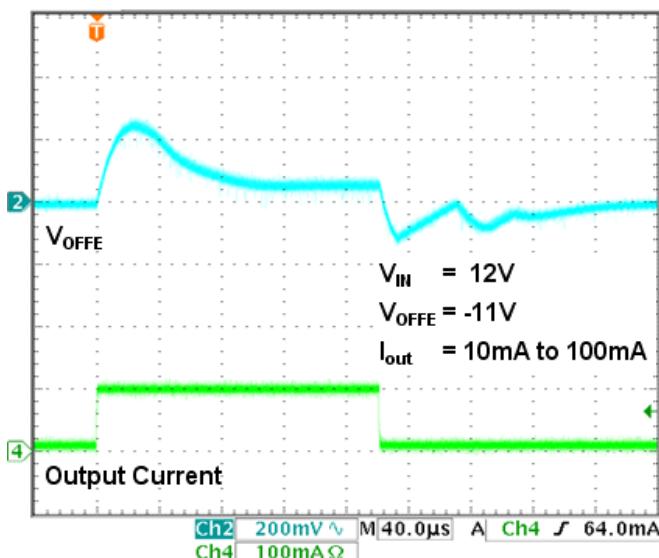


Figure 18.

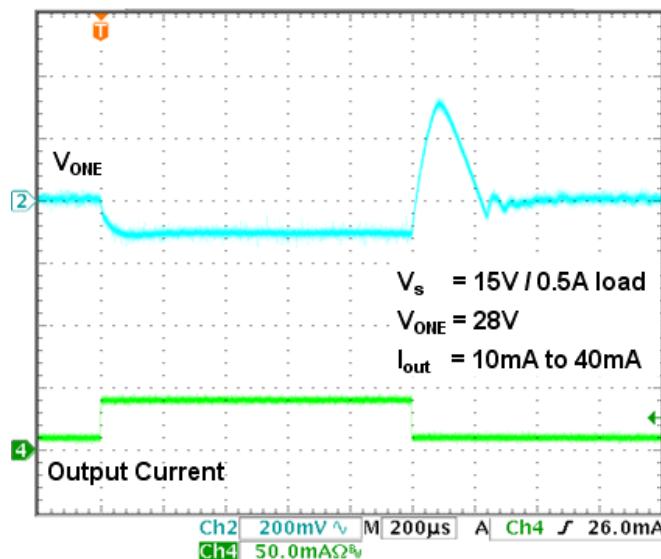
LOAD TRANSIENT RESPONSE POSITIVE CHARGE PUMP  $V_S=15V$ 

Figure 19.

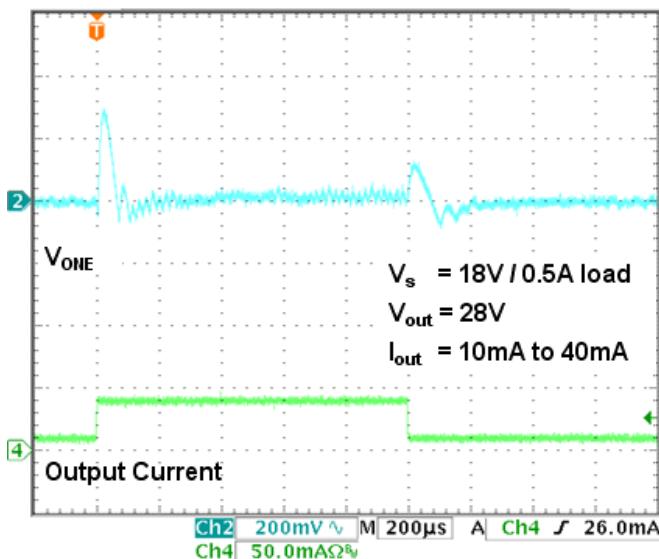
LOAD TRANSIENT RESPONSE POSITIVE CHARGE PUMP  $V_S=18V$ 

Figure 20.

## LOAD TRANSIENT RESPONSE NEGATIVE SHUNT REGULATOR

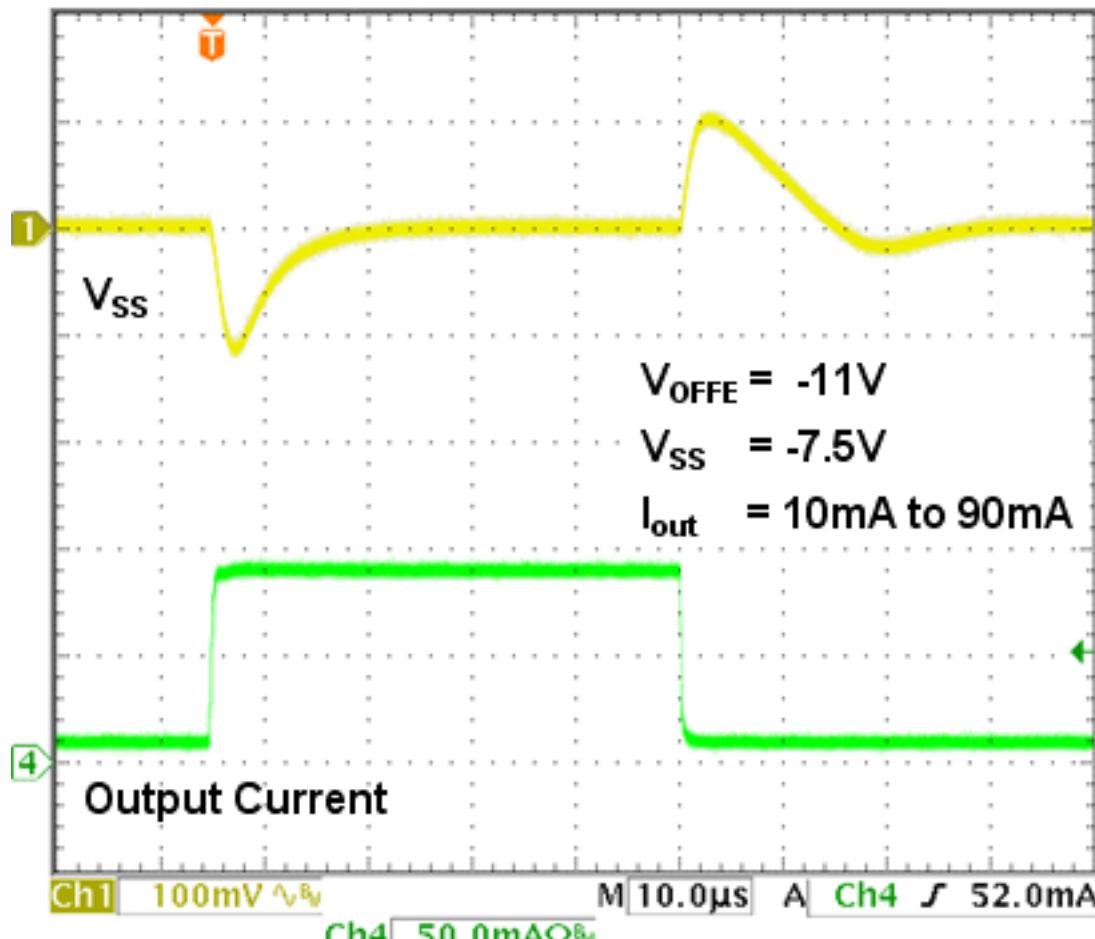


Figure 21.

## APPLICATION INFORMATION

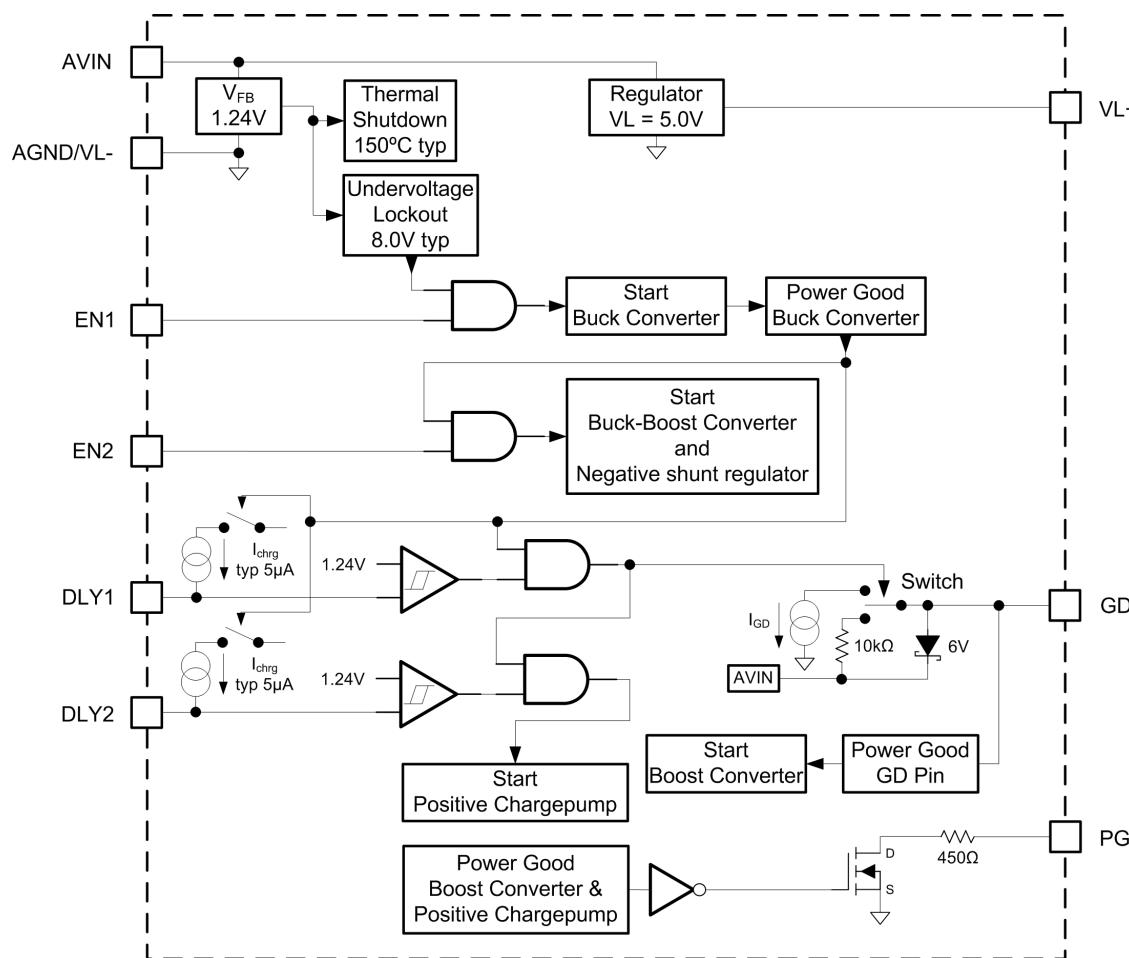


Figure 22. Control Block TPS65171

### Thermal Shutdown

A thermal shutdown is implemented to prevent damages because of excessive heat and power dissipation. Once a temperature of typically 150°C is exceeded the device enters shutdown. It enables again if the temperature drops below the threshold temperature of typically 135 °C and does normal startup.

### Undervoltage Lockout

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included, which shuts down the device at voltages lower than typically 8.0V.

### Short Circuit Protection

The positive charge pump controller  $V_{ONE}$  will run with reduced current (typ. 50  $\mu$ A) and disables the boost converter if short circuit is detected (FB4 falls below 100 mV). An exception is made at startup. If  $V_{ONE}$  has once passed the short level threshold (FB4 is above 100 mV), the boost converter will not be disabled until Power Good of  $V_{ONE}$  has been detected. In case there is already a short when the device is activated the charge pump controller  $V_{ONE}$  will run with reduced current and the boost converter will not start until the short is removed and  $V_{ONE}$  passes the short level threshold.

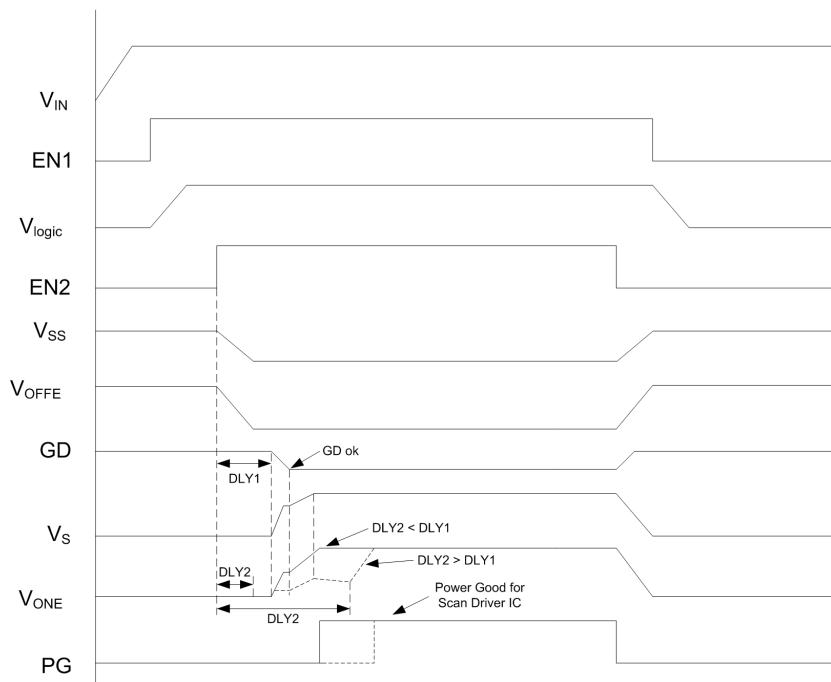
The buck converter detects a short circuit if FB2 falls below 400 mV and the whole device except the buck converter itself is shut down as if EN2 would be disabled. The switching frequency of the buck converter is reduced to 1/4th of the normal operation frequency. If the short is removed the buck converter will start operation again and the whole device auto recovers to normal operation by doing startup sequencing as if EN2 would be enabled.

The negative buck boost converter  $V_{OFFE}$  has a short circuit protection where the switch current is limited to typically 300 mA and switching frequency is reduced to about 150 kHz. A short is detected if  $V_{OFFE}$  rises above -3 V

The shunt regulator  $V_{ss}$  has no short circuit protection.

## Start-Up Sequencing

The device has adjustable start-up sequencing to provide correct sequencing as required by the display.



**Figure 23. Power Up Sequencing**

EN1 enables the buck converter.

EN2 enables the negative buck boost converter  $V_{OFFE}$  and  $V_{ss}$  at the same time. DLY1 sets the delay time for the boost converter  $V_s$  and DLY2 sets the delay time for  $V_{ONE}$ .  $V_{ONE}$  does not start until DLY1 is elapsed. For simultaneous startup of  $V_s$  and  $V_{ONE}$ , DLY2 should be set to 0 by not connecting the DLY2 pin. Once  $V_s$  and  $V_{ONE}$  are in regulation, PG goes high impedance to enable the scan driver IC.

## Power Good Output

The power good output PG is an open drain output with typically  $450\Omega$  resistance and requires a pull-up resistor to the 3.3V rail. The power good goes high impedance when the  $V_s$  and  $V_{ONE}$  voltage rails are in regulation and provides an enable signal for the external scan driver IC. Once power good is high impedance, the signal is latched until  $V_s$  or  $V_{ONE}$  detect a short circuit.

The resulting maximum PG voltage if PG is low is dependent on R22 connection voltage ( $V_{logic}$ ) and R22 value. To calculate maximum resulting PG voltage for power bad signal use following formula:

$$V_{PG\_low} = \frac{450\Omega \times V_{logic}}{450\Omega + R22} \quad (1)$$

The resulting PG voltage if PG pin is high impedance is dependent on R22 connection voltage ( $V_{logic}$ ), R22 value and output current  $I_{out}$  of PG node. The output current is flowing to the external scan driver. Assuming a maximum switch leakage current of  $1\mu A$  the minimum PG output voltage can be calculated as following:

$$V_{PG\_high} = V_{logic} - R22 \times (1\mu A + I_{out}) \quad (2)$$

Recommended are R22 values between  $5k\Omega$  and  $500k\Omega$ . Typical value for R22 is  $10k\Omega$ .

### Setting the Delay Times DLY1, DLY2

Connecting an external capacitor to the DLY1 and DLY2 pins sets the delay time. The capacitor is charged with a constant current source of typically  $5\mu A$ . The delay time is terminated when the capacitor voltage has reached the threshold voltage of  $V_{th} = 1.24V$ . If no capacitor is set, the delay time is zero. The external capacitors can be calculated as follows:

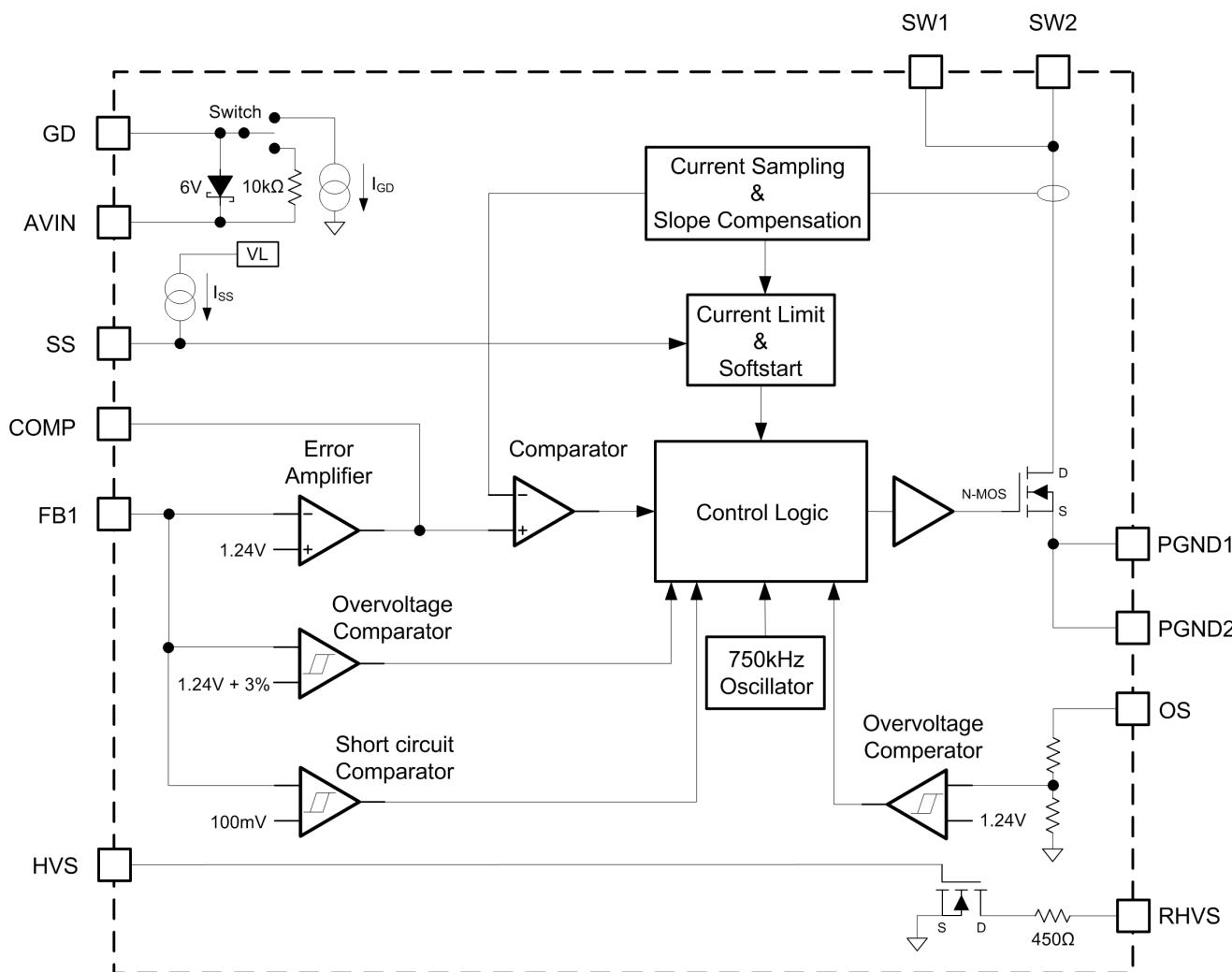
$$C_{DLY} = \frac{5 \mu A \times DLY}{V_{th}} = \frac{5 \mu A \times DLY}{1.24 V}, \text{ with DLY = Desired delay time} \quad (3)$$

Example for setting a delay time of 2.5ms:

$$C_{DLY} = \frac{5 \mu A \times 2.5 \text{ ms}}{1.24 V} = 10.1 \text{ nF} \Rightarrow CDLY = 10 \text{ nF} \quad (4)$$

### Boost Converter

The non-synchronous current mode boost converter operates in Pulse Width Modulation (PWM) operation with a fixed frequency of 750 kHz. For maximum flexibility and stability with different external components the converter uses external loop compensation. At start up the boost converter starts with an externally adjustable soft-start. The boost converter provides the supply voltage for the LCD source driver as well as for the charge pump regulator  $V_{ONE}$ . This needs to be taken into account when defining the output current requirements for the boost converter. No feed-forward capacitor is needed for proper operation.



**Figure 24. Boost Converter Block Diagram**

## Soft-Start (Boost Converter)

To avoid high inrush current during start-up an internal soft-start is implemented. The soft-start time is set by an external capacitor connected to the SS pin. The capacitor is charged with a constant current of typically  $10\mu\text{A}$ , which increases the voltage at the SS pin. The internal switch current limit is proportional to the SS pin voltage and rises with rising voltage until  $V_S$  is in regulation or the maximum current limit is reached. The larger the soft-start capacitor value the longer the soft-start time. For a  $100\text{nF}$  capacitor at the SS pin, the current limit is reached after  $0.9\text{ms}$ . An estimation of the current limit slope  $\Delta I_{\text{inductor}}$  and  $C_{\text{SS}}$  capacitor can be made by the following formulas.

$$\frac{\Delta I_{\text{inductor}}}{\Delta t} = \frac{0.43}{C_{\text{ss}}} \times \frac{\text{mA}^2}{\text{V}} \quad C_{\text{ss}} = \frac{0.43 \times \Delta t}{\Delta I_{\text{inductor}}} \times \frac{\text{mA}^2}{\text{V}} \quad (5)$$

## Compensation (Boost Converter)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The typical value of  $R4 = 33\text{k}\Omega$  and  $C5 = 1\text{nF}$  is appropriate for most applications. Choosing  $R4 = 36\text{k}\Omega$  compensates the boost converter more aggressive and may cause instability for low output capacitance. The below formula calculates at what frequency the resistor  $R4$  increases the high frequency gain.

$$f_Z = \frac{1}{2 \times \pi \times R4 \times C5} \quad (6)$$

## Gate Drive Pin (GD) and Isolation Switch Selection

The external isolation switch disconnects the boost converter once the device is turned off. If the boost converter is enabled by EN2 and the delay time set by DLY1 passed by, the gate pin GD is pulled low by an internal  $10\ \mu\text{A}$  current sink to minimize inrush current until the Gate-Source voltage is clamped at about  $V_{IN} - 6\text{ V}$ . An internal  $10\ \text{k}\Omega$  pull up resistor to  $V_{IN}$  is connected to GD to open the isolation switch if the Gate Drive is disabled. Using a gate drain capacitor of typically  $1\ \text{nF}$  allows to increase the turn on time of the MOSFET for further inrush current minimization. If the boost feedback voltage falls below  $100\text{mV}$  for more than  $1.4\ \text{ms}$ , GD is pulled high and the boost converter shuts down. The device does not recover automatically from shut down but Enable or unervoltage lockout must be toggled. Using this configuration allows to optimize the solution to specific application requirement and different MOSFETs can be used. A standard P-Channel MOSFET with a current rating close to the maximal used switch current of the boost converter is sufficient. The worst case power dissipation of the isolation switch is the maximal used switch current  $\times R_{DS(on)}$  of the MOSFET. A standard SOT23 package or similar is able to provide sufficient power dissipation.

Table 1. Isolation Switch Selection

COMPONENT SUPPLIER	CURRENT RATING
Vishay Siliconix Si3443CDV	4.7 A / 60 m $\Omega$
Vishay Siliconix Si3433DS	6 A / 38 m $\Omega$
International Rectifier IRLML6402	3.7 A / 65 m $\Omega$

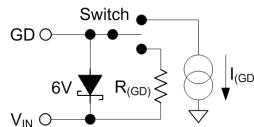


Figure 25. GD Drive

## High Voltage Stress Test (HVS)

The device has a high voltage stress test. This allows programming the boost converter output voltage  $V_S$  higher by the resistor connected to RHVS once HVS is pulled high. With HVS = high the RHVS pin is switched to GND. The resistors  $R2$  and  $R3$  are connected parallel and therefore the overall resistance is reduced. This changes the output voltage during the High Voltage Stress Test to a higher value:

$$V_{S_{HVS}} = V_{FB1} \frac{R1 + R2||R3}{R2||R3} = 1.24V \frac{R1 + R2||R3}{R2||R3} \quad (7)$$

$$R3 = \frac{R1 \times R2}{\left(\frac{V_{S_{HVS}}}{V_{FB1}} - 1\right) \times R2 - R1} = \frac{R1 \times R2}{\left(\frac{V_{S_{HVS}}}{1.24V} - 1\right) \times R2 - R1} \quad (8)$$

With:

$V_{S_{HVS}}$  = Boost converter output voltage with HVS high

## Overvoltage Protection

The boost converter has two overvoltage protection mechanisms for the switch.  $V_s$  is monitored with an overvoltage protection comparator on the OS pin and as soon as 19.5V typical is reached, the boost converter stops switching. The converter also detects overvoltage if the feedback voltage at the feedback pin FB1 is 3% above the typical regulation voltage of 1.24V, which stops switching. The converter starts switching again if the output voltage falls below the overvoltage thresholds.

## Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. All input voltages (AVIN, VIN1, 2, 3) are shorted internally. It is recommended to short AVIN, VIN1, and VIN2 externally on the PCB by a thick conducting path to avoid high currents between the VIN pins inside the device and to place one 10 $\mu$ F input capacitor as close as possible to these pins. Another 10 $\mu$ F input capacitor should be placed close to VIN3. For better input voltage filtering the input capacitor values can be increased. If it is not possible to place the 10 $\mu$ F capacitor close to the device, it is recommended to add an additional 1 $\mu$ F or 4.7 $\mu$ F capacitor which should be placed next to the input pins. To reduce power losses at the external isolation switch, a filter capacitor C3 at the input terminal of the inductor is required. To minimize possible audible noise problems, one 10 $\mu$ F capacitor in parallel is recommended. More capacitance further reduces the ripple current across the isolation switch. See [Table 2](#) for input capacitor selection.

**Table 2. Input Capacitor Selection**

CAPACITOR	COMPONENT SUPPLIER
10 $\mu$ F/16V	Murata, GRM31CR71C106KAC7
10 $\mu$ F/16V	Taiyo Yuden, EMK325BJ106MN
10 $\mu$ F/16V	Murata, GRM31CR61C106KA88

## Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. To simplify the calculation, the fastest approach is to estimate the converter efficiency by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g., 90%. The calculation must be made with the minimum assumed input voltage where peak switch current is the highest. The inductor and external Schottky diode has to be able to handle this current.

1. Converter Duty Cycle:  $D = 1 - \frac{V_{in} \times \eta}{V_{out}}$
2. Maximum output current:  $I_{out} = \left( I_{swpeak} - \frac{V_{in} \times D}{2fs \times L} \right) \times (1-D)$
3. Peak switch current:  $I_{swpeak} = \frac{V_{in} \times D}{2fs \times L} + \frac{I_{out}}{1-D}$  (9)

With,

$I_{swpeak}$  = Converter peak switch current (minimum switch current limit = 2.5 A)

$fs$  = Converter switching frequency (typical 750 kHz)

$L$  = Selected inductor value

$\eta$  = Estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption)

### Inductor Selection (Boost Converter)

The boost converter is able to operate with  $6.8\mu\text{H}$  to  $15\mu\text{H}$  inductors, a  $10\mu\text{H}$  inductor is typical. The main parameter for inductor selection is the saturation current of the inductor, which should be higher than the peak switch current as calculated in the Design Procedure section with additional margin to cover for heavy load transients. The alternative more conservative approach is to choose an inductor with saturation current at least as high as the minimum switch current limit of  $2.5\text{A}$ . Another important parameter is the inductor dc resistance. Usually the lower the dc resistance the higher the efficiency. For a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well. The efficiency difference among inductors can vary up to 10%. Possible inductors are shown in [Table 3](#).

**Table 3. Inductor Selection Boost Converter**

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
$10\mu\text{H}$	Sumida CDRH5D28R/HP	$6.2 \times 6.2 \times 3.0$	$2.5\text{ A}/74\text{ m}\Omega$
$10\mu\text{H}$	Sumida CDRH6D26/HP	$7 \times 7 \times 2.8$	$2.5\text{ A}/72\text{ m}\Omega$
$10\mu\text{H}$	Sumida CDRH6D28	$7 \times 7 \times 3.0$	$1.7\text{ A}/48\text{ m}\Omega$
$10\mu\text{H}$	Sumida CDRH5D28R	$6.2 \times 6.3 \times 3.0$	$1.3\text{ A}/40\text{ m}\Omega$

### Rectifier Diode Selection (Boost Converter)

To achieve high efficiency a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the boost converter. The average rectified forward current  $I_{\text{avg}}$ , the Schottky diode needs to be rated for, is equal to the output current  $I_{\text{out}}$ .

$$I_{\text{avg}} = I_{\text{out}} \quad (10)$$

Usually a Schottky diode with  $2\text{A}$  maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current  $I_{\text{out}}$ , but has to be able to dissipate the power. The dissipated power is calculated according to the the following equation:

$$P_D = I_{\text{avg}} \times V_{\text{forward}} \quad (11)$$

**Table 4. Rectifier Diode Selection (Boost Converter)**

$V_r/I_{\text{avg}}$	$V_{\text{forward}}$	$R_{\theta\text{JA}}$	SIZE	COMPONENT SUPPLIER
$20\text{V}/2\text{A}$	$0.38\text{V}$ at $2\text{A}$	$60^\circ\text{C}/\text{W}$	PowerDI 123	DFLS220L, DIODES Incorporated
$20\text{V}/2\text{A}$	$0.44\text{V}$ at $2\text{A}$	$25^\circ\text{C}/\text{W}$	SMA	B220A, DIODES Incorporated
$20\text{V}/2\text{A}$	$0.44\text{V}$ at $2\text{A}$	$75^\circ\text{C}/\text{W}$	SMB	SL22, Vishay Semiconductor

### Output Capacitor Selection (Boost Converter)

For the best output voltage filtering, low ESR ceramic output capacitors are recommended. Two  $22\mu\text{F}$  or four  $10\mu\text{F}$  ceramic output capacitors with sufficient voltage rating in parallel are adequate for most applications. Additional capacitors can be added to improve the load transient regulation. See [Table 5](#) for output capacitor selection.

**Table 5. Output Capacitor Selection (Boost Converter)**

CAPACITOR	COMPONENT SUPPLIER
$22\mu\text{F}/25\text{V}$	Murata, GRM32ER61E226KE15
$10\mu\text{F}/25\text{V}$	Murata, GRM31CR61E106KA12
$10\mu\text{F}/50\text{V}$	Taiyo Yuden, UMK325BJ106MM

## Setting the Output Voltage (Boost Converter)

The output voltage is set by an external resistor divider. A minimum current of  $100\mu\text{A}$  through the feedback divider provides good accuracy and noise covering. The resistors are calculated as:

$$V_s = V_{FB1} \times \left(1 + \frac{R1}{R2}\right) = 1.24 \text{ V} \times \left(1 + \frac{R1}{R2}\right) \quad (12)$$

$$R2 = \frac{V_{FB1}}{100 \mu\text{A}} = \frac{1.24 \text{ V}}{100 \mu\text{A}} \approx 12 \text{ k}\Omega \quad (13)$$

$$R1 = R2 \times \left(\frac{V_s}{1.24 \text{ V}} - 1\right) = R2 \times \left(\frac{V_s}{1.24 \text{ V}} - 1\right) \quad (14)$$

## Buck Converter

The non-synchronous current mode buck converter operates at fixed frequency PWM operation. The converter drives an internal N-channel MOSFET switch with an internal bootstrap capacitor. The output voltage can be set between 2.5V and 3.3V by an external feedback divider. If the feedback voltage FB2 is 15% above the reference voltage of 1.24V the converter stops switching and starts switching again if the FB2 voltage falls below the threshold. For 3.3V output voltage the overvoltage lockout is approximately 3.8 V.

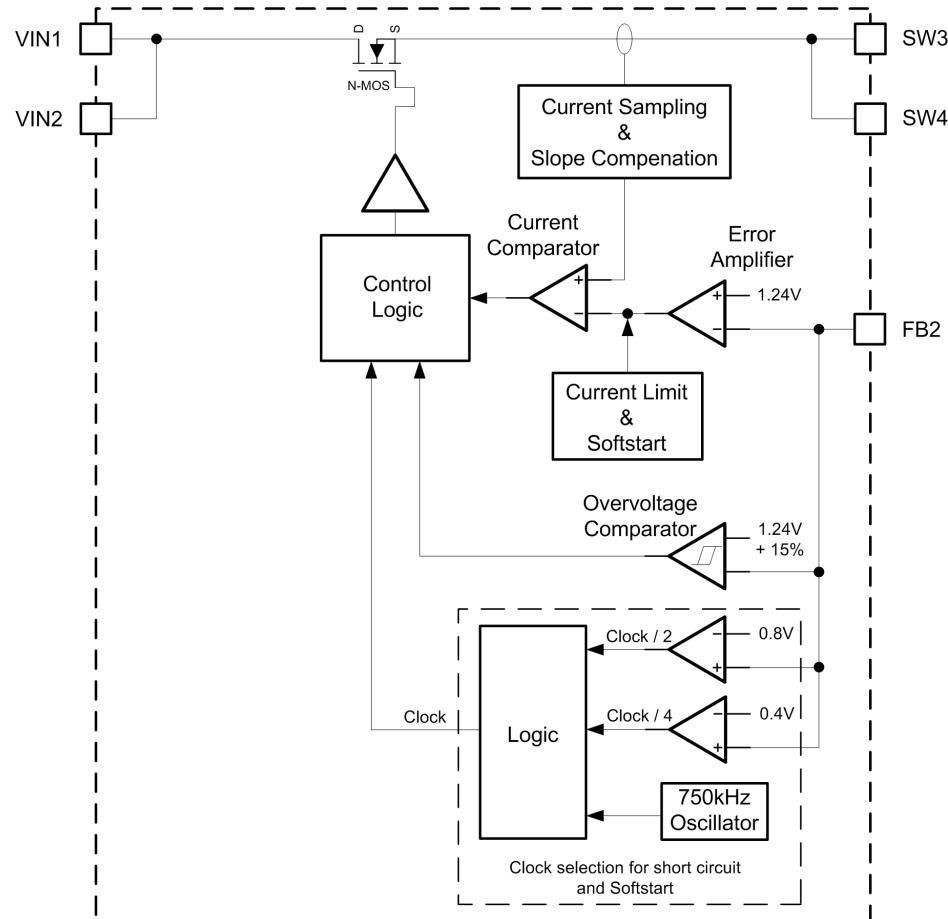


Figure 26. Buck Converter Block Diagram

## Soft-Start (Buck Converter)

To avoid high inrush current during start-up, an internal soft-start is implemented. When the buck converter is enabled, its current limit is reduced and it slowly rises (1ms to 2ms) to the switch current limit. For further inrush current limitation, the switching frequency is reduced to 1/4 of the switching frequency  $f_s$  until the feedback voltage FB2 reaches 0.4V, then the switching frequency is set to 1/2 of  $f_s$  until FB2 reaches 0.8V when the full switching frequency  $f_s$  (750kHz) is applied. See the internal Block diagram ([Figure 26](#)) for further explanation. The soft-start is typically completed in 1ms to 2ms.

## Buck Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the buck converter supports the specific application requirements. To simplify the calculation, the fastest approach is to estimate the converter efficiency by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g., 80%. The calculation must be for the maximum assumed input voltage where the peak switch current is the highest. The inductor and external Schottky diode have to be able to handle this current.

1. Converter Duty Cycle:  $D = \frac{V_{out}}{V_{in} \times \eta}$
2. Maximum output current:  $I_{out} = I_{swpeak} - \frac{V_{in} \times (1 - D)}{2fs \times L} \times D$
3. Peak switch current:  $I_{swpeak} = I_{out} + \frac{V_{in} \times (1 - D)}{2fs \times L} \times D$  (15)

With;

$I_{swpeak}$  = Converter peak switch current (minimum switch current limit = 1A)

$fs$  = Converter switching frequency (typical 750kHz)

$L$  = Selected inductor value

$\eta$  = Estimated converter efficiency (use the number from the efficiency curves or 0.8 as an assumption)

## Inductor Selection (Buck Converter)

The buck converter is able to operate with  $6.8\mu H$  to  $15\mu H$  inductors, a  $10\mu H$  inductor is typical. The main parameter for inductor selection is the saturation current of the inductor which should be higher than the maximum output current plus the inductor ripple current as calculated in the *Design Procedure* section. The highest inductor current occurs at maximum  $V_{IN}$ . The alternative more conservative approach is to choose an inductor with saturation current at least as high as the minimum switch current limit of 1A. Another important parameter is the inductor dc resistance. Usually the lower the dc resistance the higher the efficiency; the type and core material of the inductor influences the efficiency as well. The efficiency difference among inductors can vary up to 10%. Possible inductors are shown in [Table 6](#).

**Table 6. Inductor Selection Buck Converter**

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
$10\mu H$	Sumida CDRH3D23	$3.9 \times 3.9 \times 2.5$	$0.85A/95m\Omega$
$10\mu H$	Sumida CDRH3D28	$4.0 \times 4.0 \times 3.0$	$1.1A/116m\Omega$
$10\mu H$	Sumida CDRH4D22	$5.0 \times 5.0 \times 2.4$	$0.8A/79m\Omega$

## Rectifier Diode Selection (Buck Converter)

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the buck converter. The average rectified forward current  $I_{avg}$ , the Schottky diode needs to be rated for, is calculated as the off time of the buck converter times the output current.

$$I_{avg} = I_{out} \times (1 - D) \quad (16)$$

Usually a Schottky diode with a 1A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current  $I_{out}$ , but has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage. The efficiency rises with lower forward voltage.

$$P_D = I_{avg} \times V_{forward} \quad (17)$$

**Table 7. Rectifier Diode Selection (Buck Converter)**

<b>V<sub>D</sub>/I<sub>avg</sub></b>	<b>V<sub>forward</sub></b>	<b>R<sub>θJA</sub></b>	<b>SIZE</b>	<b>COMPONENT SUPPLIER</b>
20V/1A	0.46V at 1A	20°C/W	SMA	B120, DIODES Incorporated
20V/0.5A	0.44V at 0.5A	150°C/W	SOT123	MBR0520, International Rectifier
20V/1A	0.32V at 1A	60°C/W	PowerDI 123	DFLS120L, DIODES Incorporated

### Output Capacitor Selection (Buck Converter)

For best output voltage filtering, low ESR ceramic output capacitors are recommended. Two 22 $\mu$ F or four 10 $\mu$ F ceramic output capacitors with sufficient voltage rating in parallel are adequate for most applications. Additional capacitors can be added to improve the load transient regulation. See [Table 8](#) for output capacitor selection.

**Table 8. Output Capacitor Selection (Buck Converter)**

<b>CAPACITOR</b>	<b>COMPONENT SUPPLIER</b>
22 $\mu$ F/6.3V	Murata, GRM31CR60J226KE19
10 $\mu$ F/6.3V	Murata, GRM21BR70J106KE76
47 $\mu$ F/6.3V	Murata, GRM32ER60J476ME20
10 $\mu$ F/6.3V	Taiyo Yuden, JWK212BJ106MD

### Setting the Output Voltage (Buck Converter)

The output voltage is set by an external resistor divider. R6 should be chosen in the range of 0.5k $\Omega$  to 4.7k $\Omega$ . For good noise covering and accuracy the lower feedback resistor R6 is selected to obtain at least a 250 $\mu$ A minimum load current.

$$V_{logic} = V_{FB2} \times \left(1 + \frac{R5}{R6}\right) = 1.24 \text{ V} \times \left(1 + \frac{R5}{R6}\right) \quad (18)$$

$$R6 = \frac{V_{FB2}}{1 \text{ mA}} = \frac{1.24 \text{ V}}{1 \text{ mA}} \approx 1.2 \text{ k}\Omega \quad (19)$$

$$R5 = R6 \times \left( \frac{V_{logic}}{V_{FB2}} - 1 \right) = R6 \times \left( \frac{V_{logic}}{1.24 \text{ V}} - 1 \right) \quad (20)$$

### Negative Buck-Boost Converter V<sub>OFFE</sub>, Temperature Compensation

The non-synchronous constant off-time current mode buck-boost converter generates the negative V<sub>OFFE</sub> voltage rail. This output rail is required to power the scan driver. The output voltage is temperature compensated and fully adjustable from -22V to -5V. The external resistor divider on pins FB5 and SET allow programming high and low voltage levels. The graph below shows the output voltage versus temperature in °C and series resistor R19 (5k $\Omega$  to 7.5k $\Omega$ ). NTC (22k $\Omega$ ) and R18 (30k $\Omega$ ) define the slope of the curve, R19 allows selection of the temperature point where temperature compensation begins and ends. The converter is compensated internally, for further stabilization the feed-forward capacitor C22 can be chosen between 100pF and 3nF. Soft-start is also realized with this capacitor. The larger the capacitor value the longer the soft-start time. The recommended C22 value is 2.2nF.

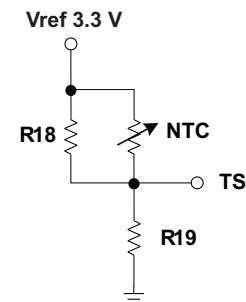
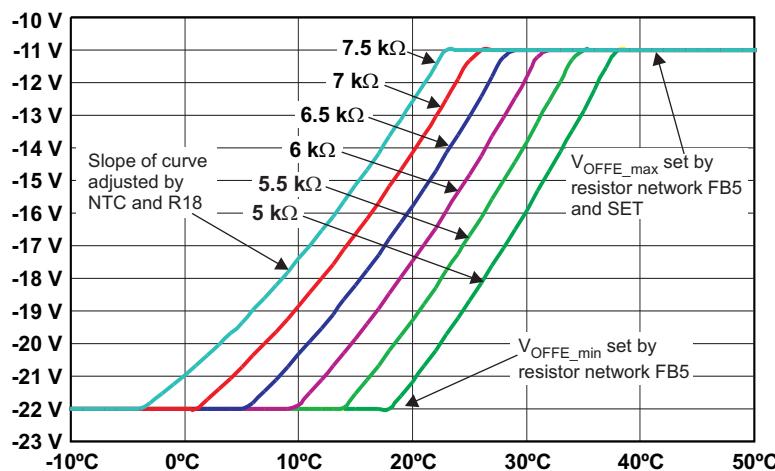
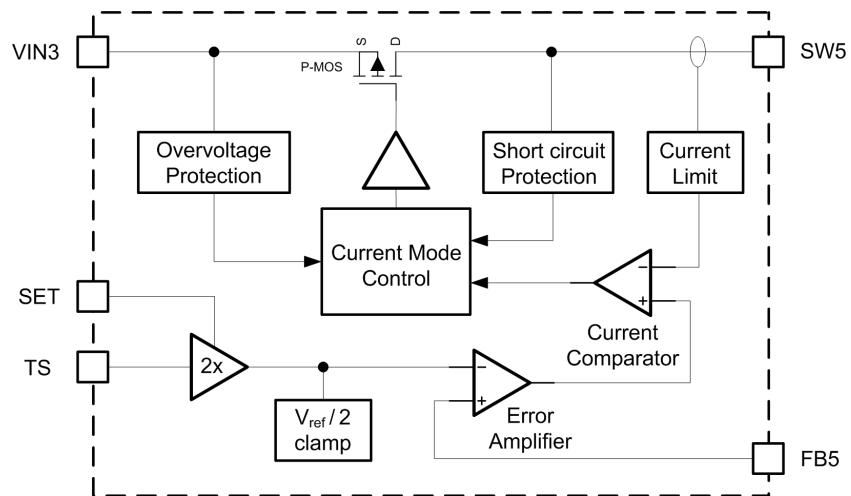
Figure 27.  $V_{OFFE}$  Temperature Compensation

Figure 28. Buck-Boost Converter Block Diagram

## Setting the Minimal and Maximal Output Voltage, $V_{OFFE}$

Keep in mind that  $V_{OFFE}$  has a negative value, while  $V_{logic}$  and  $V_{SET}$  have positive values:

$$V_{OFFE\_min} = \frac{V_{logic}}{2} \times \left(1 - \frac{R21}{R20}\right) = 1.65 \text{ V} \times \left(1 - \frac{R21}{R20}\right), \text{ select R21 about } 1 \text{ M}\Omega \text{ to achieve good soft-start.} \quad (21)$$

$$R20 = \frac{V_{logic} \times R21}{V_{logic} - 2 \times V_{OFFE\_min}} = \frac{3.3 \text{ V} \times R21}{3.3 \text{ V} - 2 \times V_{OFFE\_min}} \quad (22)$$

$$V_{OFFE\_max} = V_{SET} - (V_{logic} - V_{SET}) \times \frac{R21}{R20} = V_{SET} - (3.3 \text{ V} - V_{SET}) \times \frac{R21}{R20}, \text{ VSET is calculated below.} \quad (23)$$

$$V_{SET} = \frac{V_{OFFE\_max} \times R20 + V_{logic} \times R21}{R20 + R21} = \frac{V_{OFFE\_max} \times R20 + 3.3 \text{ V} \times R21}{R20 + R21} \quad (24)$$

$$V_{SET} = V_{logic} \times \frac{R17}{R16 + R17} = 3.3 \text{ V} \times \frac{R17}{R16 + R17}, \text{ select R17 between } 1 \text{ k}\Omega \text{ and } 20 \text{ k}\Omega \text{ for good accuracy.} \quad (25)$$

$$R16 = R17 \times \left( \frac{V_{logic}}{V_{SET}} - 1 \right) = R17 \times \left( \frac{3.3 \text{ V}}{V_{SET}} - 1 \right) \quad (26)$$

## Setting the Start and End Temperature of the Compensation

The resistance of a NTC termistor decreases nonlinearly with rising temperature.

$$R_{NTC}(T) = R_{T_0} \times e^{-B \times \left( \frac{1}{T_0} - \frac{1}{T} \right)} \quad (27)$$

Where,

$R_{T_0}$  is the resistance at an absolute temperature  $T_0$  in Kelvin (normally 25°C)

$T$  is the temperature in Kelvin ( $^{\circ}\text{C} + 273.15 \text{ K}/^{\circ}\text{C}$ )

$B$  is a material constant

The NTC termistor manufacturer provides the above parameters. Typically a 22kΩ NTC is used. [Table 9](#) provides a suggestion for NTCs.

**Table 9. Negative Termistor Selection**

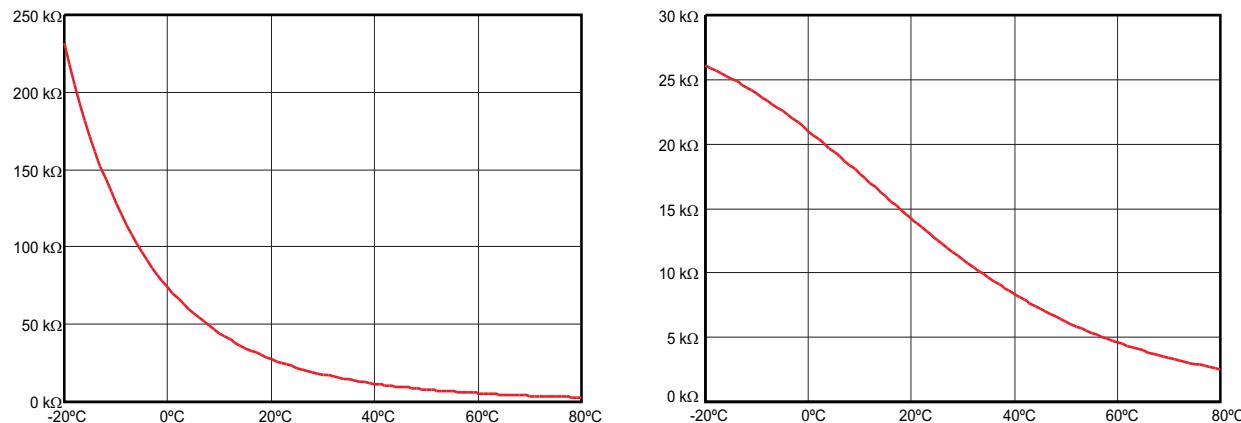
RESISTANCE (25°C)	B CONSTANT	COMPONENT SUPPLIER	COMMENT
22kΩ	3950 K	Murata, NCP18XW223E	±3%
22kΩ	3800 K	Vishay, NTCS0805E3223FHT	±1%
22kΩ	4554 K	TDK, NTCG164LH223HT	±3%

To linearize the resistance-temperature characteristic of the NTC termistor, a parallel resistor R18 is added.  $T$  is the temperature at which the NTC characteristic curve is linearized. Typically  $T$  is located in the middle of the set temperature range at which the  $V_{OFFE}$  voltage should be adjusted. For example, if the temperature compensation should start at 0°C and stop at 25°C  $T = 12.5 \text{ }^{\circ}\text{C} + 273.15 \text{ K}/^{\circ}\text{C} = 285.65 \text{ K}$ .

$$R18 = R_{NTC}(T) \times \frac{B - 2T}{B + 2T} \quad (28)$$

The resulting overall resistance  $R_{NTC||R18}$  can be calculated as follows.

$$R_{NTC||R18} = \frac{R18 \times R_{NTC}(T)}{R18 + R_{NTC}(T)} \quad (29)$$



**Figure 29. Resistance-Temperature Characteristics NTC (22 kΩ) and Linearized NTC Network at 12.5°C**

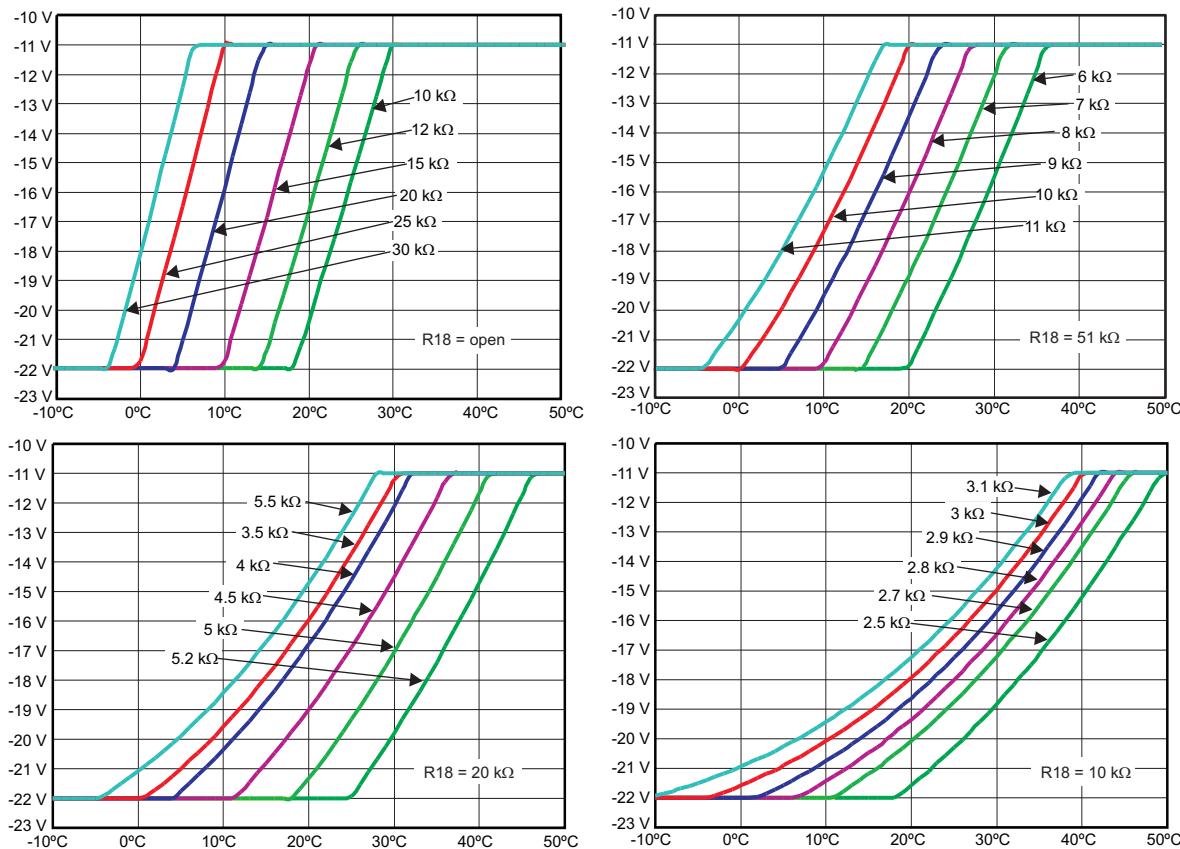
To achieve different slopes, different R18 values are required. To obtain the most linear slope, the calculated value has to be used. To achieve steeper slopes, higher values for R18 are necessary, smaller values produce shallower slopes. By adjusting the resistor R19, the start and end point of the compensation can be set. The voltage  $V_{TS}$  of the resistor network at TS is calculated by the following equation:

$$V_{TS} = V_{\text{logic}} \times \frac{R19}{R_{\text{NTC}||R18} + R19} = 3.3 \text{ V} \times \frac{R19}{R_{\text{NTC}||R18} + R19} \quad (30)$$

Finally, the resulting output voltage,  $V_{\text{OFFE}}$ , during the compensation period can be calculated as follows:

$$V_{\text{OFFE}} = 2V_{TS} - (V_{\text{logic}} - 2V_{TS}) \times \frac{R21}{R20} = 2V_{TS} - (3.3V - 2V_{TS}) \times \frac{R21}{R20} \quad (31)$$

Figure 30 shows examples for  $V_{\text{OFFE\_min}} = -22\text{V}$  and  $V_{\text{OFFE\_max}} = -11\text{V}$  with different slopes and starting points of the temperature compensation. For further compensation characteristics, refer to the available TPS65171 support excel sheet.



**Figure 30. Temperature Compensation Examples for  $R_{18} = \text{open}$ ,  $51 \text{ k}\Omega$ ,  $20 \text{ k}\Omega$ ,  $10 \text{ k}\Omega$**

### Buck-Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the buck-boost converter supports the specific application requirements. To simplify the calculation, the fastest approach is to estimate converter efficiency by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g., 80%. The calculation must be performed for the minimum assumed input voltage where the peak switch current is the highest. The inductor and external Schottky diode have to be able to handle this current.

$$1. \text{ Converter Duty Cycle: } D = \frac{-V_{\text{out}}}{V_{\text{in}} \times \eta - V_{\text{out}}}$$

$$2. \text{ Maximum output current: } I_{\text{out}} = \left( I_{\text{swpeak}} - \frac{V_{\text{in}} \times D}{2f_{\text{S}} \times L} \right) \times (1-D)$$

$$3. \text{ Peak switch current: } I_{\text{swpeak}} = \frac{I_{\text{out}}}{1-D} + \frac{V_{\text{in}} - D}{2f_{\text{S}} \times L} \quad (32)$$

With,

$I_{\text{swpeak}}$  = Converter peak switch current (minimum switch current limit = 0.8A)

$f_{\text{S}}$  = Converter switching frequency (typical 750 kHz)

$L$  = Selected inductor value

$\eta$  = Estimated converter efficiency (use the number from the efficiency curves or 0.8 as an assumption)

### Inductor Selection (Buck-Boost Converter)

The buck-boost converter is able to operate with  $10\mu\text{H}$  to  $47\mu\text{H}$  inductors, a  $22\mu\text{H}$  inductor is typical. The main parameter for inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated in the Design Procedure section with additional margin to cover for heavy load transients. The alternative more conservative approach is to choose an inductor with saturation current at least as high as the minimum switch current limit of  $0.8\text{A}$ . Another important parameter is the inductor dc resistance. Usually the lower the dc resistance the higher the efficiency. The type and core material of the inductor influences the efficiency as well. The efficiency difference among inductors can vary up to 5%. Possible inductors are listed in [Table 10](#).

**Table 10. Inductor Selection Buck-Boost Converter**

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
$22\mu\text{H}$	Sumida CDRH3D23/HP	$4.0 \times 4.0 \times 2.5$	$0.8\text{A}/306\text{m}\Omega$
$22\mu\text{H}$	Sumida CDRH4D22/HP	$5.0 \times 5.0 \times 2.4$	$1.1\text{A}/214\text{m}\Omega$
$22\mu\text{H}$	Sumida CDH3D13D/SHP	$3.2 \times 3.2 \times 1.5$	$0.6\text{A}/753\text{m}\Omega$

### Rectifier Diode Selection (Buck-Boost Converter)

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the buck-boost converter. The average rectified forward current,  $I_{\text{avg}}$ , the Schottky diode needs to be rated for, is equal to the output current,  $I_{\text{out}}$ .

$$I_{\text{avg}} = I_{\text{out}} \quad (33)$$

Usually a Schottky diode with a  $500\text{mA}$  maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current  $I_{\text{out}}$ , but has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage. The efficiency rises with lower forward voltage.

$$P_D = I_{\text{avg}} \times V_{\text{forward}} \quad (34)$$

**Table 11. Rectifier Diode Selection (Buck-Boost Converter)**

$V_r/I_{\text{avg}}$	$V_{\text{forward}}$	$R_{\text{fJ}}/A$	SIZE	COMPONENT SUPPLIER
$40V/0.5A$	$0.43V$ at $0.5A$	$206^\circ\text{C}/\text{W}$	SOD-123	MBR0540, Vishay Semiconductor
$40V/1A$	$0.42V$ at $0.5A$	$88^\circ\text{C}/\text{W}$	SMA	SS14, Fairchild Semiconductor

### Output Capacitor Selection (Buck-Boost Converter)

For the best output voltage filtering, low ESR ceramic capacitors are recommended. One  $22\mu\text{F}$  or two  $10\mu\text{F}$  output capacitors with sufficient voltage ratings in parallel are adequate for most applications. Additional capacitors can be added to improve load transient regulation. See [Table 12](#) for output capacitor selection.

**Table 12. Output Capacitor Selection (Buck-Boost Converter)**

CAPACITOR	COMPONENT SUPPLIER
$22\mu\text{F}/25V$	Murata, GRM32ER61E226KE15
$10\mu\text{F}/25V$	Murata, GRM31CR61E106KA12
$10\mu\text{F}/50V$	Taiyo Yuden, UMK325BJ106MM

### Positive Charge Pump Regulator ( $V_{\text{ONE}}$ )

This output rail is required to power the scan driver and is generated with a charge pump doubler stage running from  $V_s$  and using the switch node of the boost converter. The external PNP transistor regulates the output voltage to the programmed voltage set by the feedback resistor divider. Power dissipation and average collector current of the transistor must be taken into consideration when choosing a suitable transistor. Also the power dissipation of the resistor R12 must be considered.

## Setting the Output Voltage and Selecting the Feed-Forward Capacitor (Positive Charge Pump)

To minimize noise a minimum current through the feedback divider of 500  $\mu$ A is recommended. At startup the device is in short circuit mode with reduced current (typ. 50  $\mu$ A) until the feedback voltage FB4 exceeds 100 mV, then the device switches to soft-start mode until the output voltage  $V_{ONE}$  is in regulation. Due to the high output current and low required voltage drop, high current Schottky diodes with low forward voltage are recommended for this regulator.

$$V_{out} = V_{FB4} \times \left(1 + \frac{R14}{R15}\right) = 1.24 \text{ V} \times \left(1 + \frac{R14}{R15}\right) \quad (35)$$

$$R15 = \frac{V_{FB4}}{500 \mu\text{A}} = \frac{1.24 \text{ V}}{500 \mu\text{A}} \approx 2.4 \text{ k}\Omega \quad (36)$$

$$R14 = R15 \times \left(\frac{V_{out}}{1.24 \text{ V}} - 1\right) = R15 \times \left(\frac{V_{out}}{1.24 \text{ V}} - 1\right) \quad (37)$$

To minimize noise and leakage current sensitivity keep the lower feedback divider resistor R15 between 100 $\Omega$  and 4.7k $\Omega$ . See typical application section for charge pump circuit.

Across the upper feedback resistor R14, a bypass capacitor C17 is required. The capacitor is calculated as:

$$C17 = \frac{1}{2 \times \pi \times 12 \text{ kHz} \times R14} \quad (38)$$

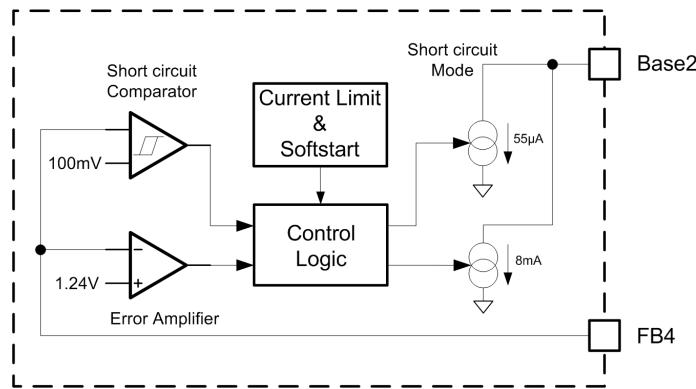


Figure 31. Positive Chargepump Block Diagram

## PNP Transistor Selection (Positive Charge Pump)

The maximum possible  $V_{ONE}$  output voltage is calculated as:

$$V_{ONE} = 2 \times V_s + V_{D1} - 2 \times V_{D2} - \frac{I_{ONE}}{D} \times R - V_Q \quad (39)$$

With:

$V_s$  = boost converter output voltage

$V_{D1}$  = Forward voltage of boost converter Schottky diode

$V_{D2}$  = Forward voltage of charge pump diode for a current of  $I_{ONE} / D$

$I_{ONE}$  =  $V_{ONE}$  output current

$D$  = Duty cycle of boost converter ( $D = 1 - V_{in} / V_s$ )

$R$  = Series resistor (if applicable, e.g., 2 $\Omega$  for typical application)

$V_Q$  = Transistor saturation voltage

As a general recommendation the  $V_{ONE}$  voltage level in use should be at least 0.5V lower than the calculated maximum  $V_{ONE}$  voltage.

The power dissipation of the transistor should be calculated for the maximum applied boost output voltage  $V_S$ . If high voltage stress mode (HVS) is used the maximum  $V_S$  voltage occurs during HVS mode.:

$$\text{Power dissipation} = \left( 2 \times V_S - V_{\text{ONE}} - 2 \times V_{D2} - \frac{I_{\text{ONE}}}{D} \times R \right) \times I_{\text{ONE}} \quad (40)$$

As an example for  $V_S = 18V$  and  $I_{\text{ONE}} = 75\text{mA}$ , the power dissipation is approximately 0.5W.

Because of the  $1\mu\text{F}$  collector capacitor C16 a wide range of transistors can be used. The most important transistor parameters are Collector-Emitter voltage which must be at least  $2 \times V_S$ , average current rating of  $1.2 \times I_{\text{ONE}}$  and DC current gain  $h_{FE}$ , which must be at least  $I_{\text{ONE}} / I_{\text{Base2}}$ .  $I_{\text{Base2}}$  minimum value of 8mA should be used for calculation. See [Table 13](#) for possible transistor selection.

**Table 13. Transistor Selection (Positive Charge Pump)**

TRANSISTOR
PZT2907A
KTA1551T
KTA1718D
KTA1666

### Resistor R12 Function and Power Dissipation (Positive Charge Pump)

R12 is used to limit the peak current flowing from collector capacitor C16 through R12, D3 and C15 into the boost switching node. High peak currents disturb the boost converter switching which results in high  $V_S$  and  $V_{\text{ONE}}$  ripple. The power dissipation for the resistor R12 can be calculated by following formula:

$$P_{\text{resistor}} = R12 \times I_{\text{ONE}}^2 \quad (41)$$

### Output Capacitor Selection (Positive Charge Pump)

For the best output voltage filtering, low ESR ceramic output capacitors are recommended. Two  $4.7 \mu\text{F}$  ceramic output capacitors with sufficient voltage rating are adequate for most applications. Additional capacitors can be added to improve the load transient regulation. See [Table 14](#) for capacitor selection.

**Table 14. Output Capacitor Selection (Positive Charge Pump)**

CAPACITOR	COMPONENT SUPPLIER
4.7 $\mu\text{F}$ /50V	Murata, GRM31CR71H475KA12
4.7 $\mu\text{F}$ /50V	Taiyo Yuden, UMK316BJ475KL-T

### Negative Shunt Regulator ( $V_{ss}$ )

$V_{ss}$  is a shunt regulator that regulates the non-addressed TFT pixels to the programmed voltage. The pulldown resistor R11 connected to  $V_{\text{OFFE}}$  is required to provide accurate no load current regulation. A minimum current of  $50\mu\text{A}$  through the feedback divider provides good accuracy. Be aware of the negative value of  $V_{ss}$  for the calculations.

$$V_{\text{out}} = V_{FB3} + (V_{FB3} - V_{\text{logic}}) \times \frac{R9}{R10} = 0.75 \times V_{\text{logic}} - \frac{V_{\text{logic}} \times R9}{4 \times R10} = 2.475V - 0.825 \times \frac{R9}{R10} \quad (42)$$

$$R10 = \frac{V_{\text{logic}} - 0.75 \times V_{\text{logic}}}{80 \mu\text{A}} = \frac{0.825 \text{ V}}{80 \mu\text{A}} \approx 10 \text{ k}\Omega \quad (43)$$

$$R9 = \frac{V_{\text{out}} - V_{FB3}}{V_{FB3} - V_{\text{logic}}} \times R10 = \frac{V_{\text{out}} - 0.75 \times V_{\text{logic}}}{-0.25 \times V_{\text{logic}}} \times R10 = \frac{V_{\text{out}} - 2.475 \text{ V}}{-0.825 \text{ V}} \times R10 \quad (44)$$

## Discharge Resistor at $V_{SS}$ Output

If a discharge resistor  $R_{dis}$  at the  $V_{SS}$  output is used to discharge the  $V_{SS}$  node faster, the pull down resistor  $R11$  connected to  $V_{OFFE}$  must be calculated by following formula to achieve the programmed output voltage at  $V_{SS}$ . A smaller resistor to the calculated one must be used. For example for  $V_{SS} = -7.5V$ ,  $V_{OFFE} = -11V$  and  $R_{dis} = 12k\Omega$  the calculated  $R11 = 4.98k\Omega$  and the resistor values  $4.7k\Omega$ ,  $4.3k\Omega$ , and  $4.0k\Omega$  can be used.

$$R11 = \frac{R_{dis} \times (R9 + R10) \times (V_{OFFE} - V_{SS})}{V_{SS} \times (R_{dis} + R9 + R10) - V_{logic} \times R_{dis}} \quad (45)$$

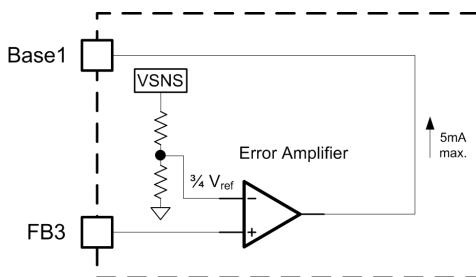


Figure 32. Negative Shunt Regulator Block Diagram

## Output Capacitor Selection (Negative Shunt Regulator)

For the best output voltage filtering, low ESR ceramic output capacitors are recommended. One  $1\mu F$  ceramic output capacitor with a sufficient voltage rating is suitable for most applications. See [Table 15](#) for output capacitor selection.

Table 15. Output Capacitor Selection (Negative Shunt Regulator)

CAPACITOR	COMPONENT SUPPLIER
$1\mu F/25V$	Murata, GRM21BR71E105KA99
$1\mu F/50V$	Taiyo Yuden, UMK325BJ105KH

## Layout Considerations

PCB layout is an important step in power supply design.

- NC pins 5, 8, 22, and 29 should not be connected to GND, if so, the device is not P2P short protected any more.
- The input capacitors should be placed as close as possible to the device. AVIN, VIN1, and VIN2 must be shorted.
- The buffer capacitor C25 must be connected to VL+ and AGND/VL- by a single trace.
- The line device, diode, output cap of the buck boost should be kept as short as possible.
- For the boost converter the line C3 GND output capacitor GND and PGND1 should be kept short.
- For the buck converter the line switch pin SW3, 4 to diode should be kept short.
- All lower feedback resistors connected to GND should be placed close to the device.
- Switching lines should not be next to feedback lines to avoid coupling.
- Use short lines or make sure the lines do not affect other regulating parts for the charge pump switching connection to SW1,2 because this trace carrys switching waveforms.
- The PowerPAD™ of the QFN package should be soldered to GND and as much as possible thermal vias should be used to lower the thermal resistance and keep the device cool.
- A solid PCB ground plane structure is essential for good device performance.
- Place red marked components and lines first and as close as possible to the device. Keep red marked lines short. Bold marked lines should be wide on the PCB, because these traces carry high currents.
- Green marked components can be placed further away.

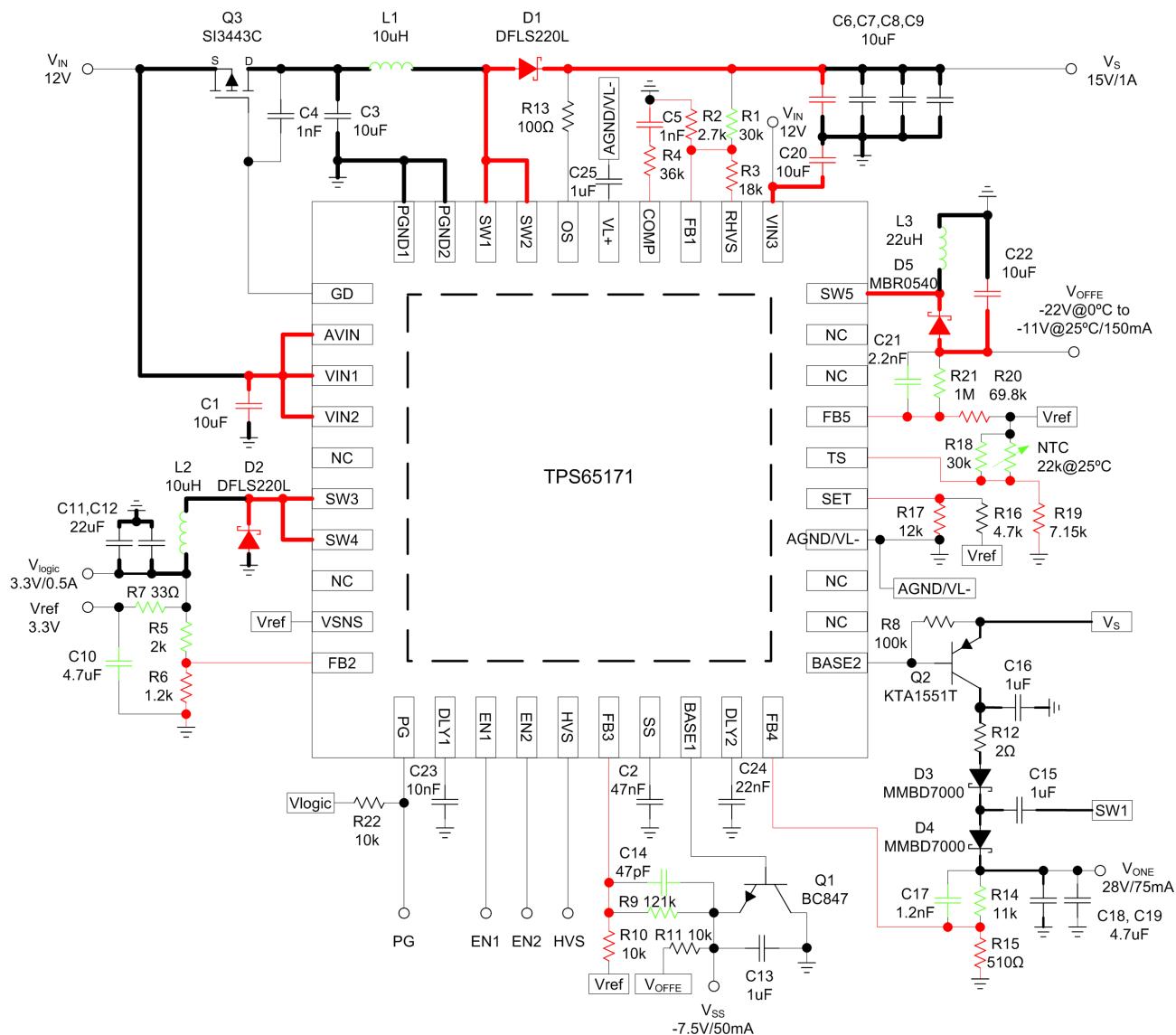


Figure 33. PCB Layout Guideline

## Typical Applications

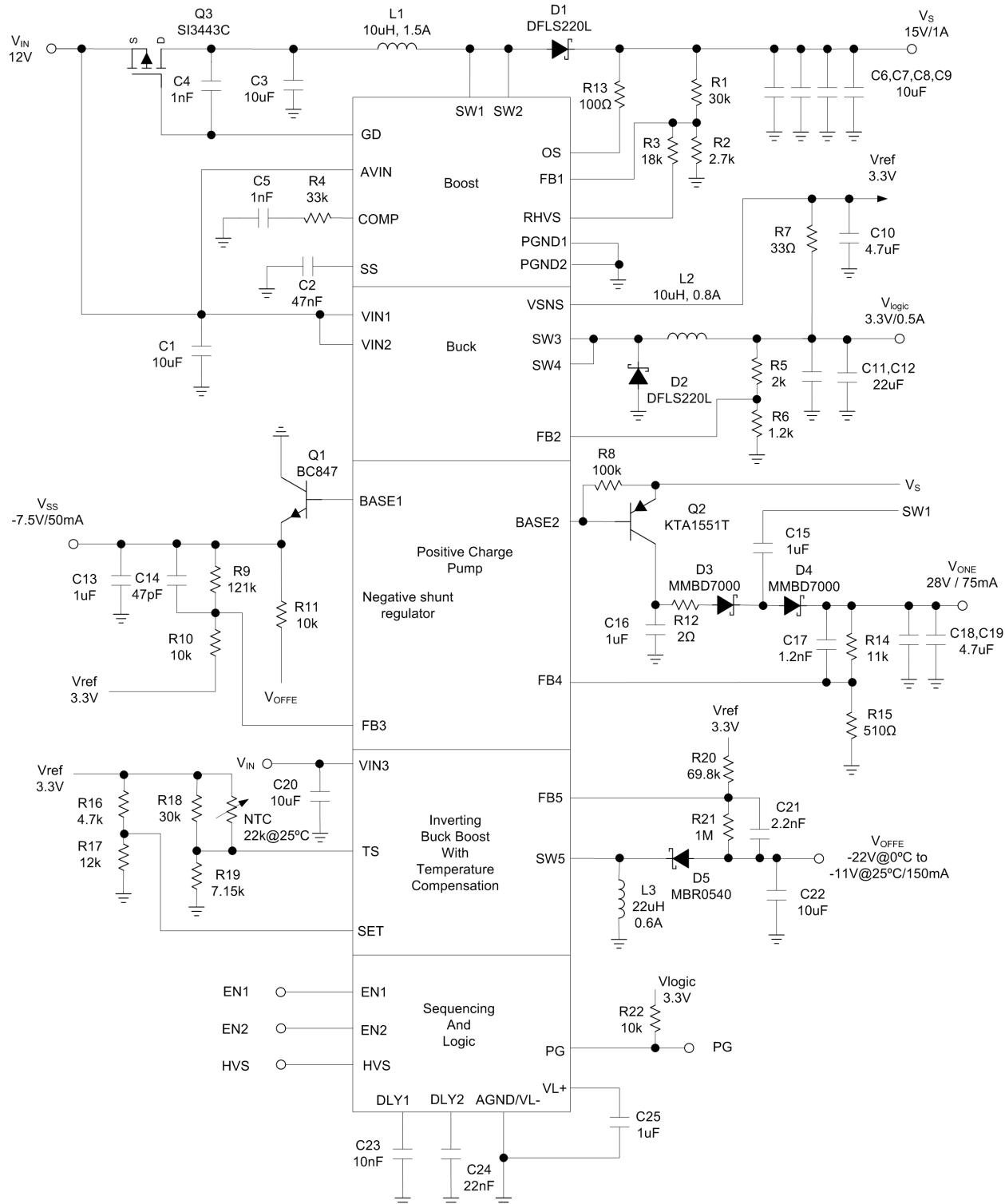
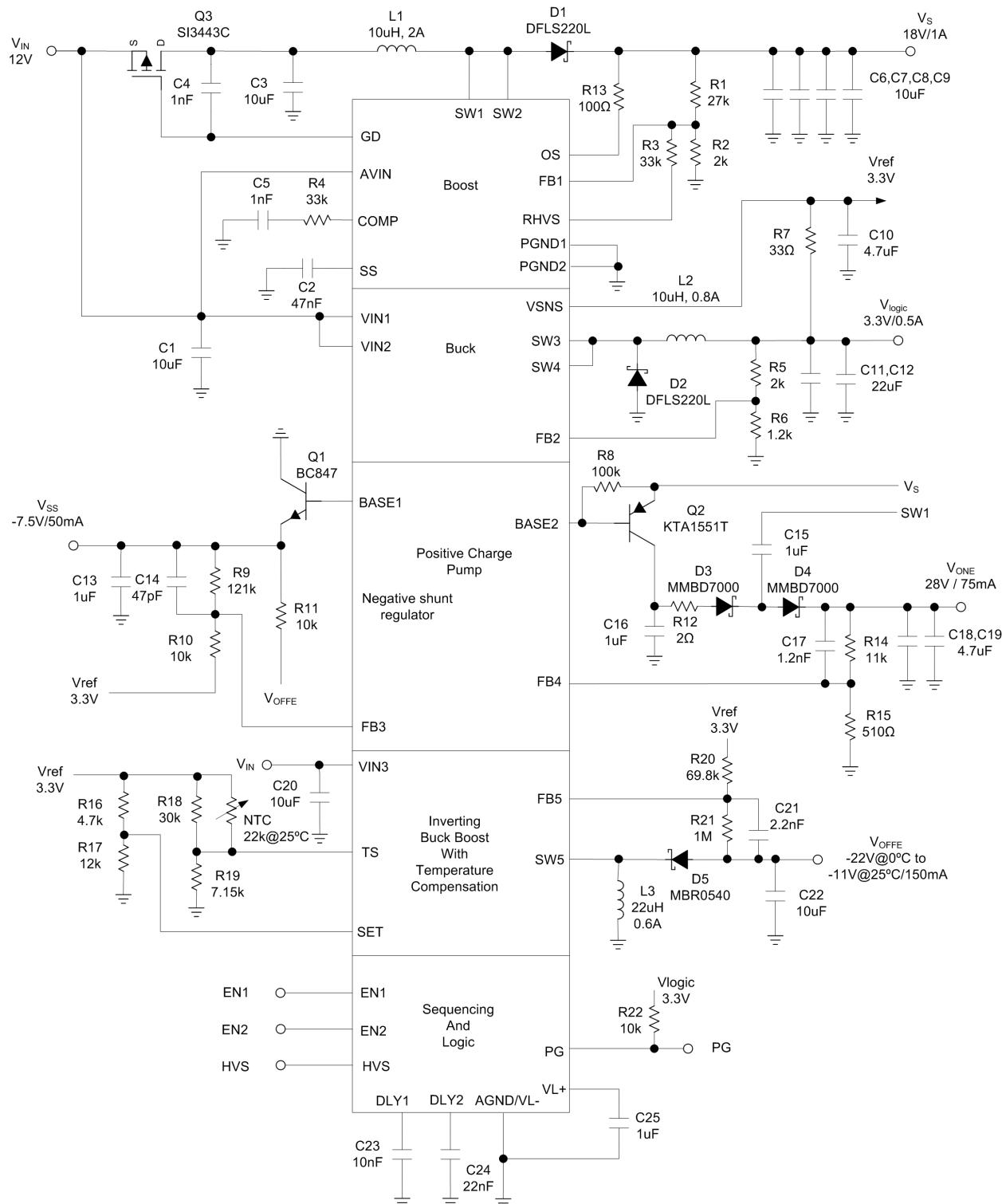
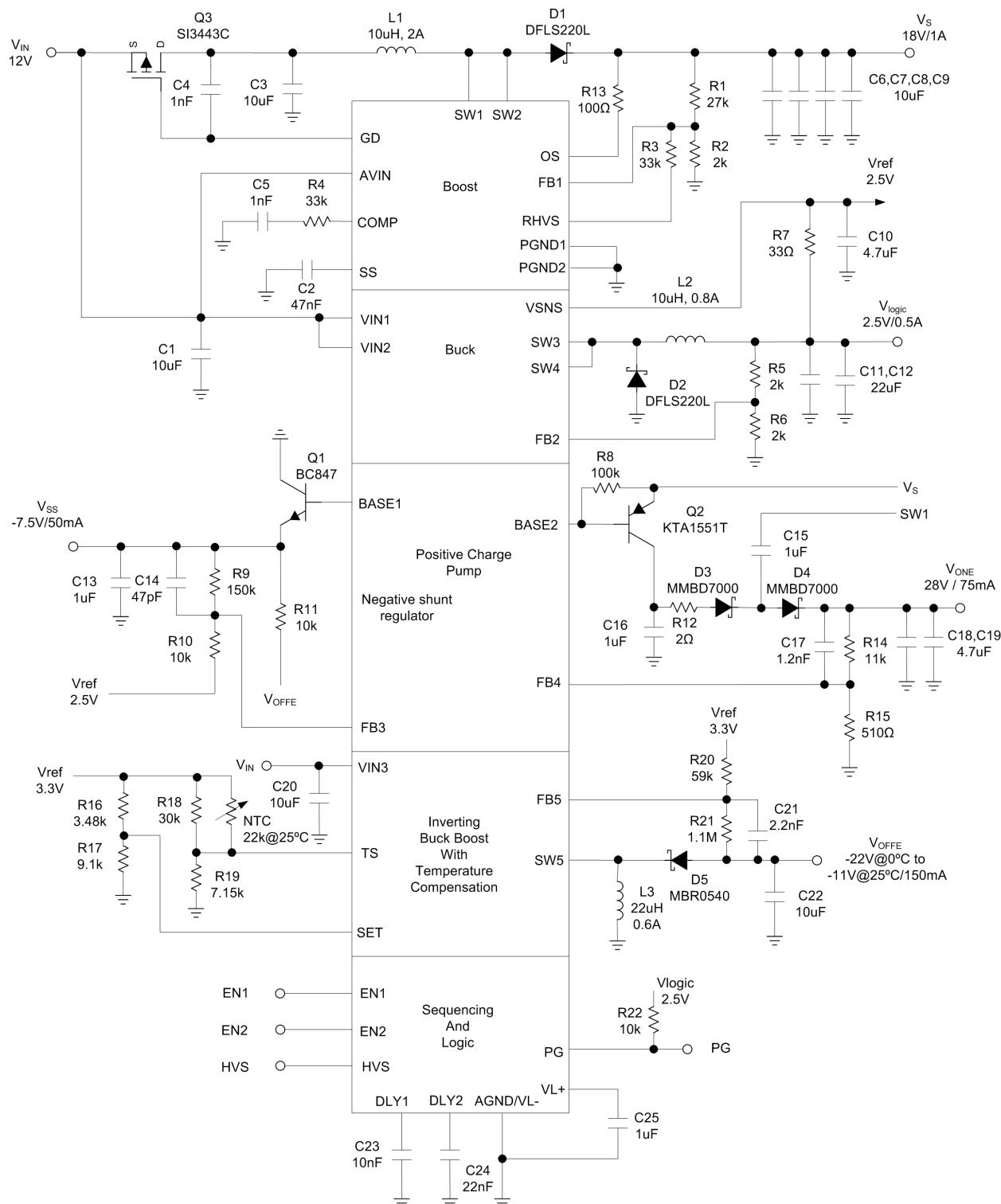


Figure 34. Typical Application With  $V_s = 15V$ ,  $HVS = 18V$ ,  $V_{logic} = 3.3V$



**Figure 35. Typical Application With  $V_s = 18V$ ,  $HVS = 19V$ ,  $V_{logic} = 3.3V$**

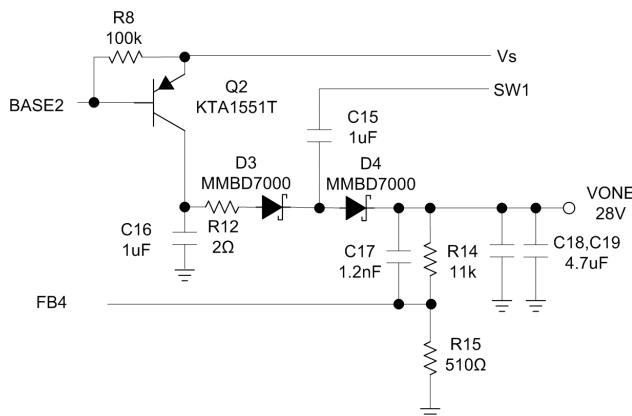


**Figure 36. Typical Application With  $V_s = 18V$ ,  $HVS = 19V$ ,  $V_{logic} = 2.5V$**

Charge pump circuit.

**Table 16. Maximum Output Current  $V_{ONE} = 28V - 3\%$**

$V_{in}$	$V_S = 15V$	$V_S \geq 16V$
10.8 V	100mA	100mA
12.0V	85mA	100mA
13.2V	55mA	100mA



**Figure 37. Typical Application  $V_{ONE}$  Output Current**

## REVISION HISTORY

<b>Changes from Original (October 2009) to Revision A</b>	<b>Page</b>
• Changed <a href="#">Figure 23</a> .....	<a href="#">17</a>

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS65171RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

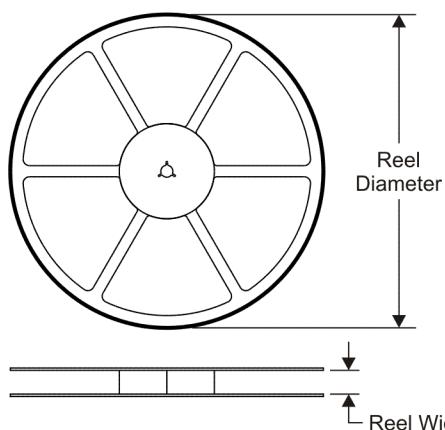
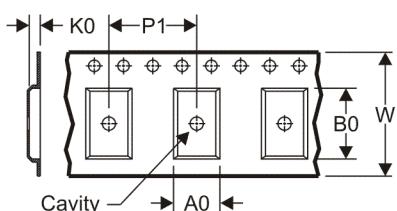
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

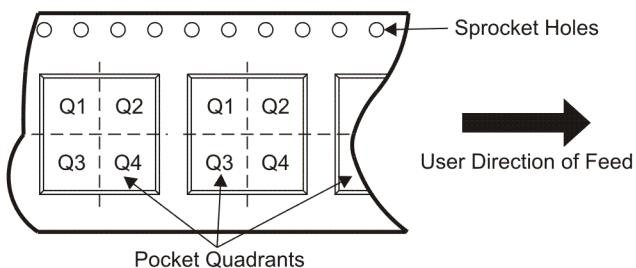
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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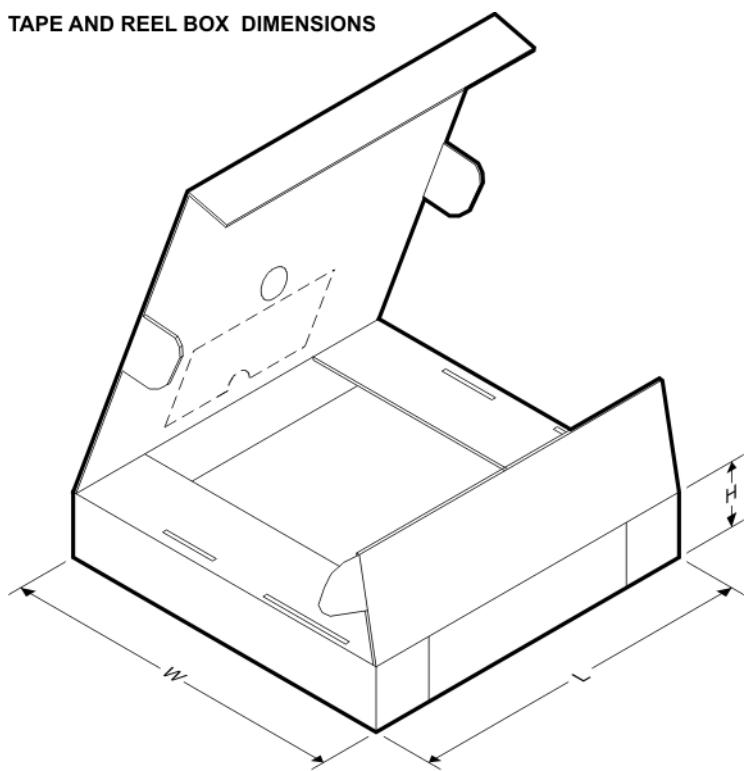
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65171RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

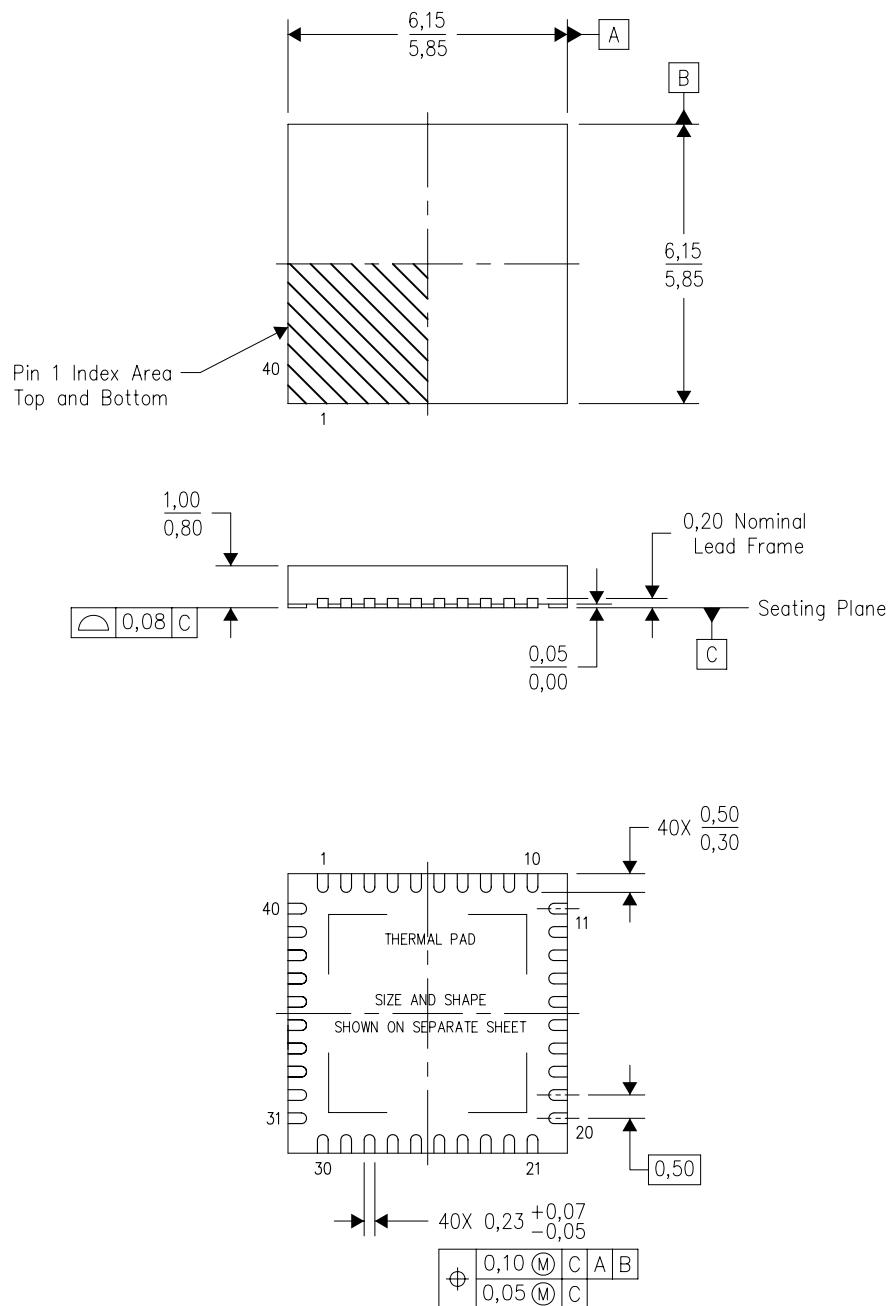
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65171RHAR	VQFN	RHA	40	2500	346.0	346.0	33.0

## MECHANICAL DATA

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4204276/E 06/11

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) Package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Package complies to JEDEC MO-220 variation VJJD-2.

RHA (S-PVQFN-N40)

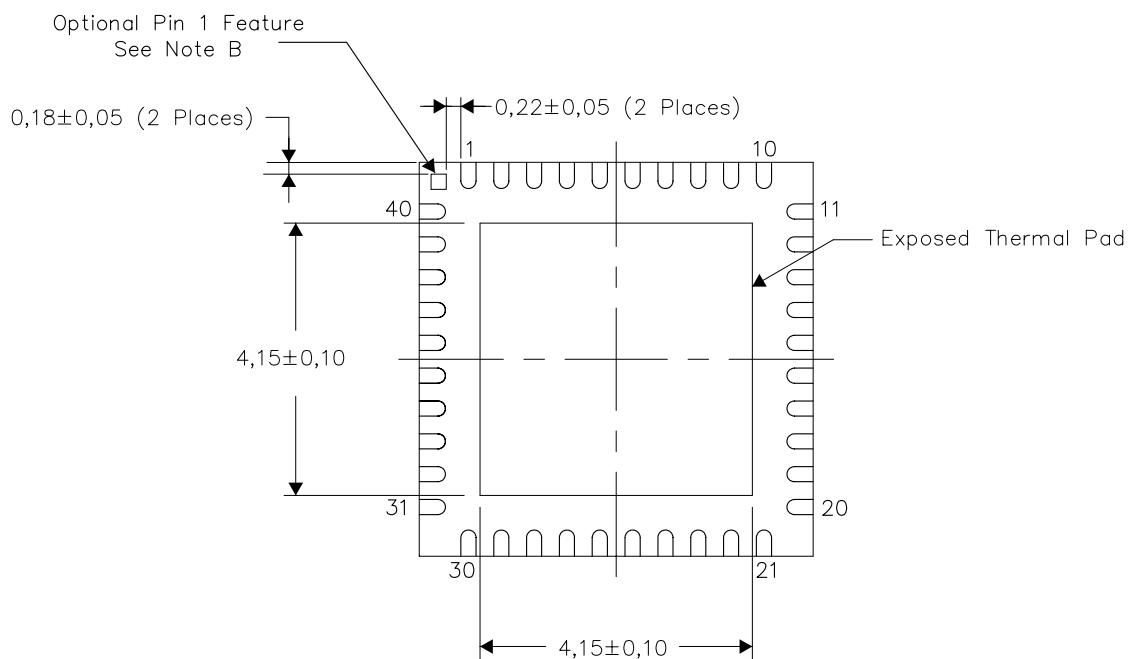
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206355-2/P 08/11

NOTES: A. All linear dimensions are in millimeters

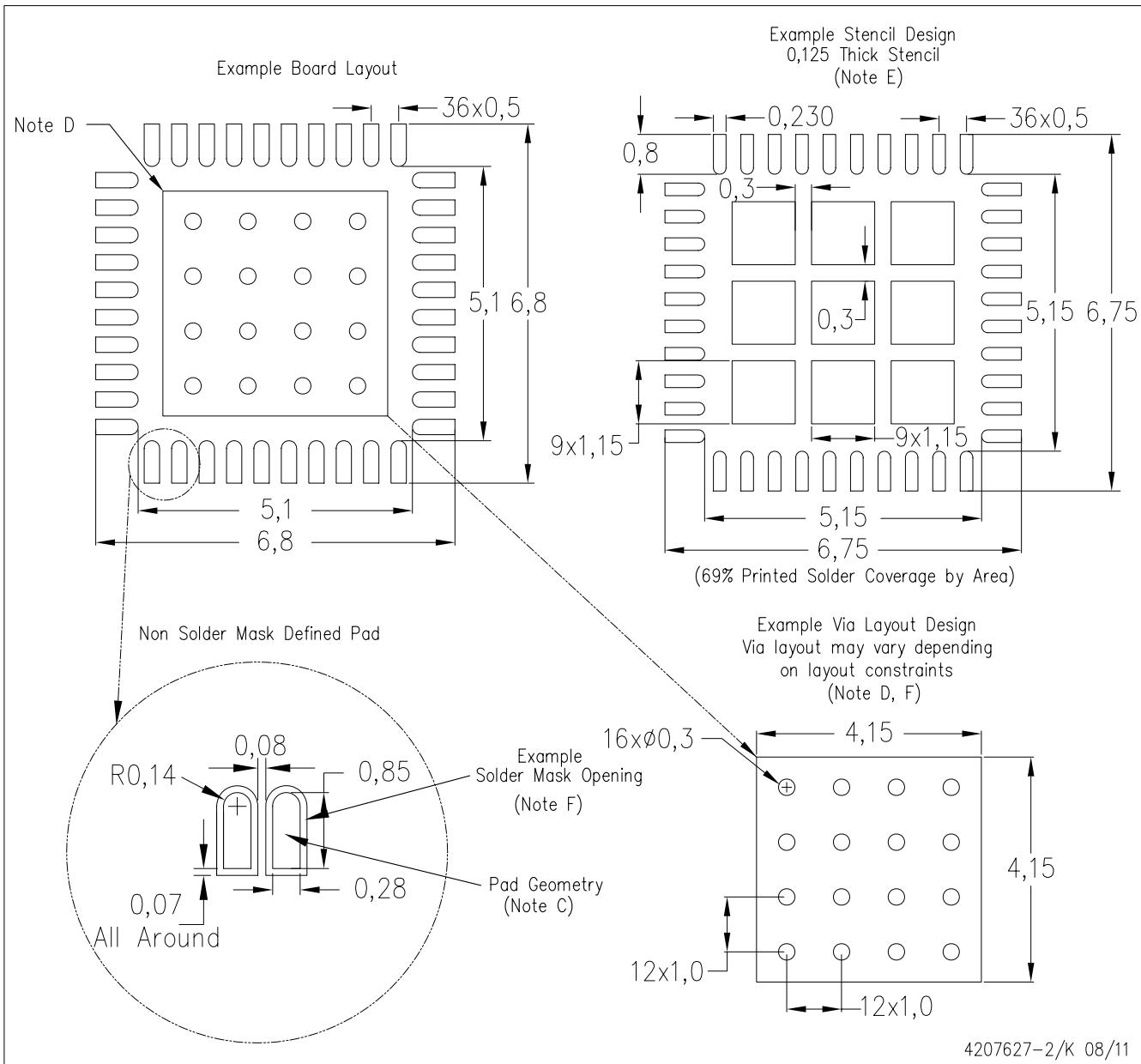
B. The Pin 1 Identification mark is an optional feature that may be present on some devices

In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

## LAND PATTERN DATA

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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