

MOS FIELD EFFECT TRANSISTORS

2SK2369/2SK2370

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK2369/2SK2370 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-Resistance
 2SK2369: $R_{DS(on)} = 0.35 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$)
 2SK2370: $R_{DS(on)} = 0.4 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$)
- Low C_{iss} $C_{iss} = 2400 \text{ pF TYP.}$
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

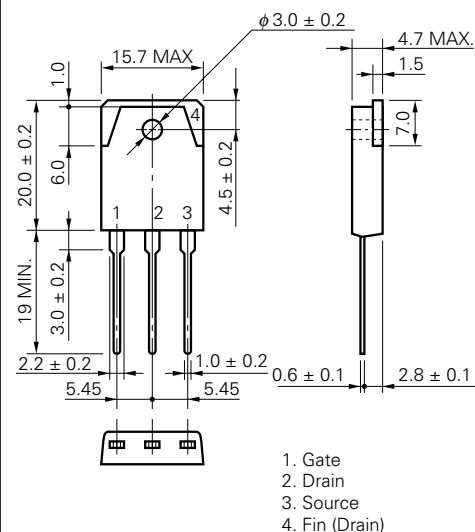
Drain to Source Voltage(2SAK2369/2370)	V_{BSS}	450/500	V
Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 20	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 80	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	140	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	3.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	I_{AS}	20	A
Single Avalanche Energy**	E_{AS}	285	mJ

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

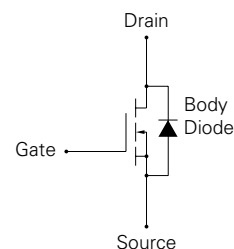
** Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

PACKAGE DIMENSIONS

(in millimeters)



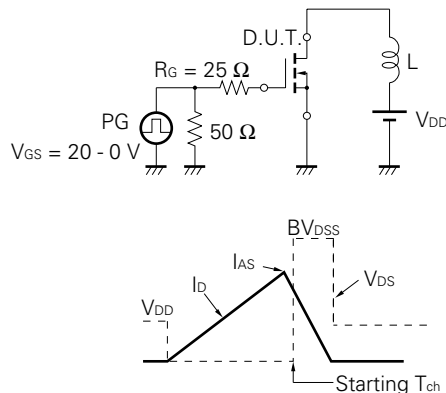
MP-88



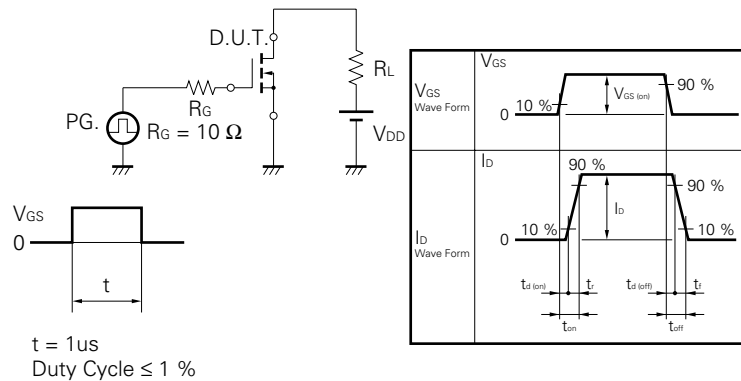
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-State Resistance	R _{DS(on)}		0.30	0.35	Ω	V _{GS} = 10 V	2SK2369
			0.32	0.40		I _D = 10 V	2SK2370
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA	
Forward Transfer Admittance	y _{fs}	7.5			S	V _{DS} = 10 V, I _D = 10 A	
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = V _{DSS} , V _{GS} = 0	
Gate to Source Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±30 V, V _{DS} = 0	
Input Capacitance	C _{iss}		2400		pF	V _{DS} = 10 V	
Output Capacitance	C _{oss}		500		pF	V _{GS} = 0	
Reverse Transfer Capacitance	C _{rss}		45		pF	f = 1 MHz	
Turn-On Delay Time	t _{d(on)}		35		ns	I _D = 10 A	
Rise Time	t _r		60		ns	V _{GS} = 10 V	
Turn-Off Delay Time	t _{d(off)}		105		ns	V _{DD} = 150 V	
Fall Time	t _f		65		ns	R _G = 10 Ω R _L = 15 Ω	
Total Gate Charge	Q _G		65		nC	I _D = 20 A	
Gate to Source Charge	Q _{GS}		15		nC	V _{DD} = 400 V	
Gate to Drain Charge	Q _{GD}		30		nC	V _{GS} = 10 V	
Body Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 20 A, V _{GS} = 0	
Reverse Recovery Time	t _{rr}		500		ns	I _F = 20 A, V _{GS} = 0	
Reverse Recovery Charge	Q _{rr}		3.5		μC	di/dt = 50 A/μs	

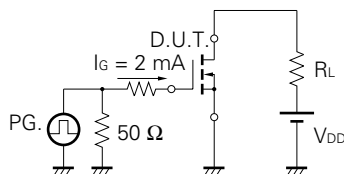
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

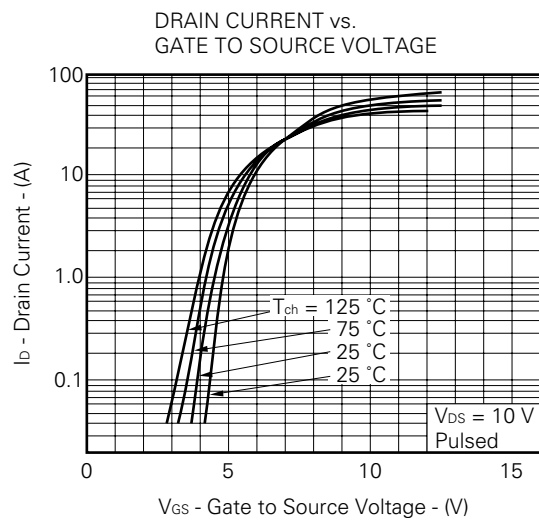
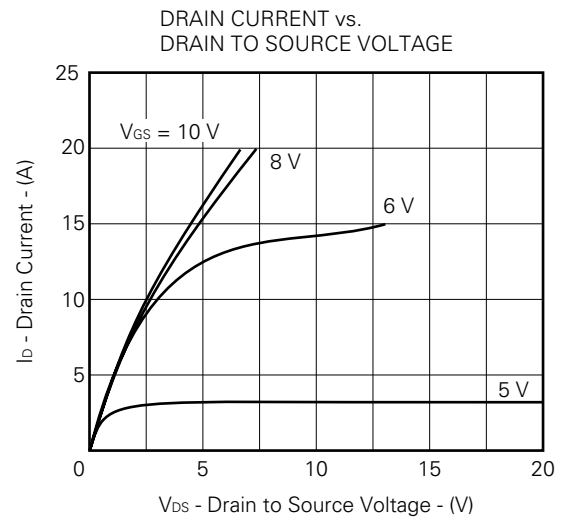
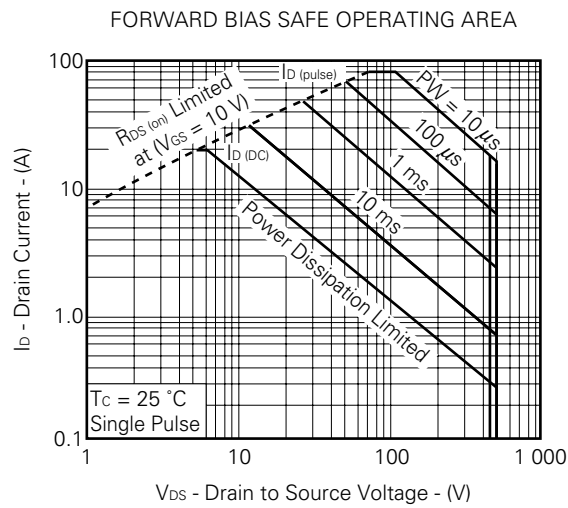
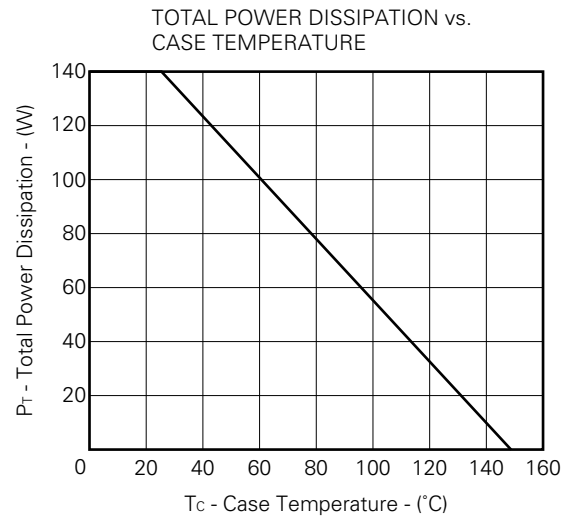
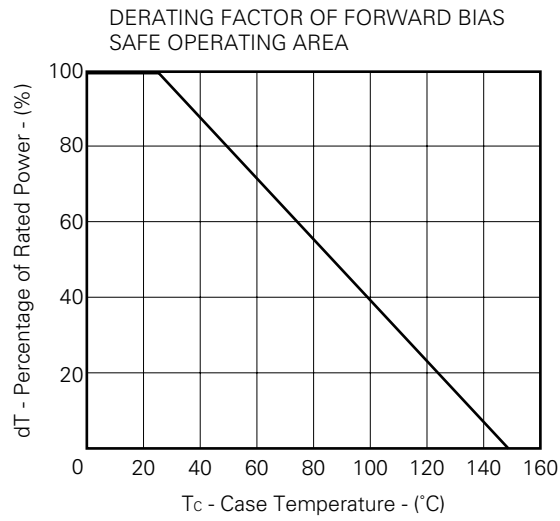


Test Circuit 3 Gate Charge

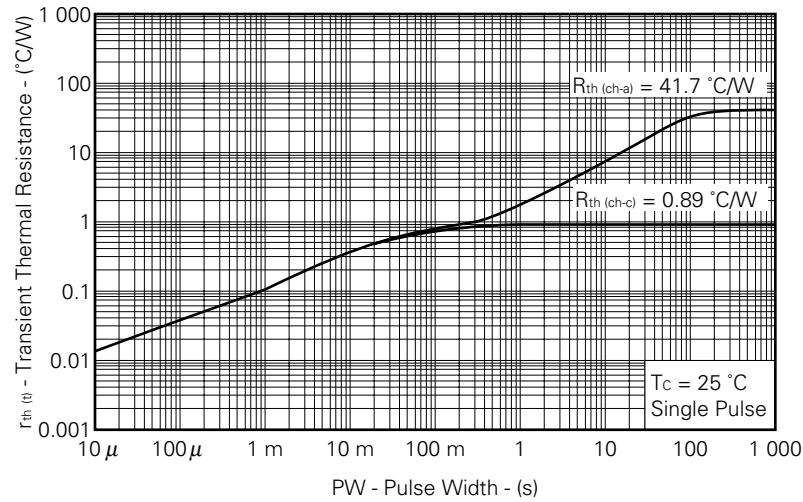


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

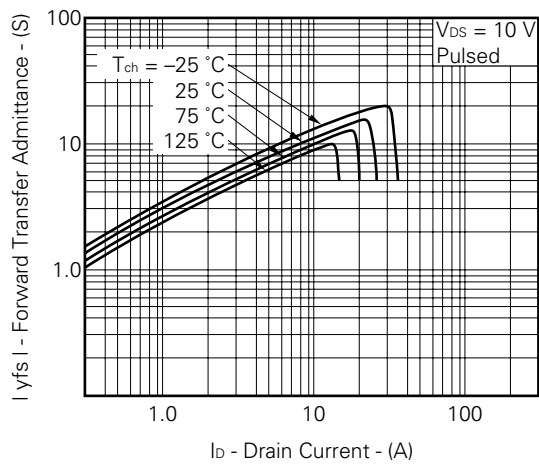
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$)



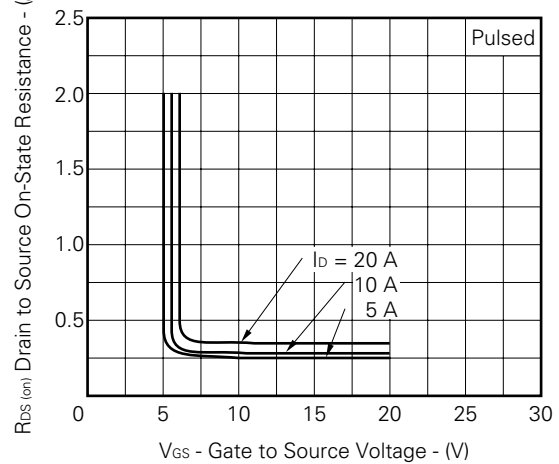
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



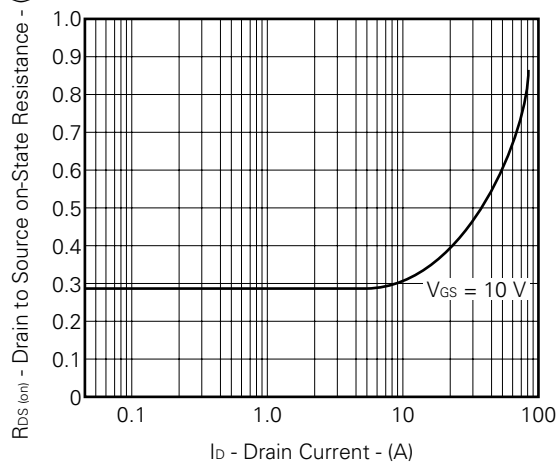
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



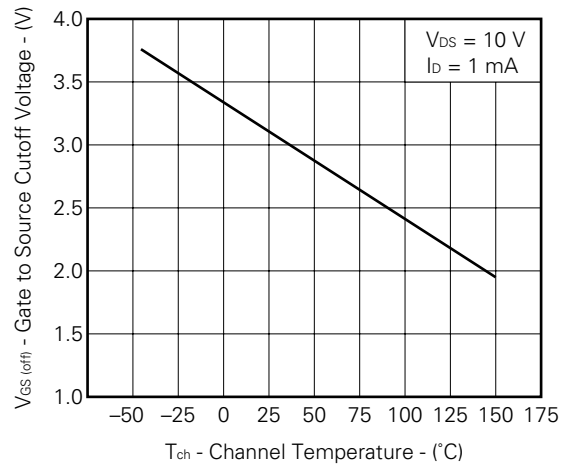
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

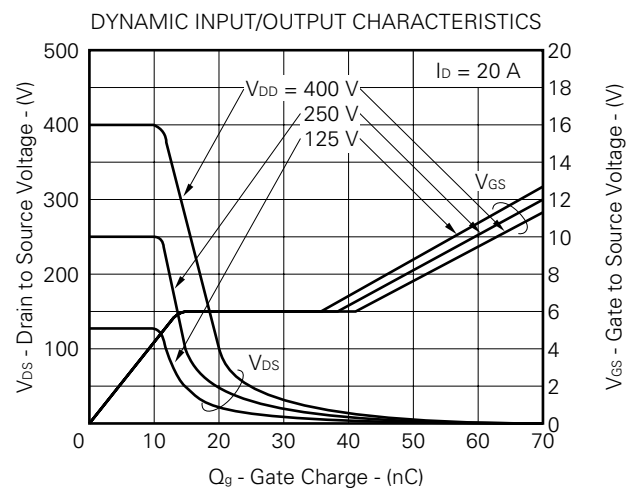
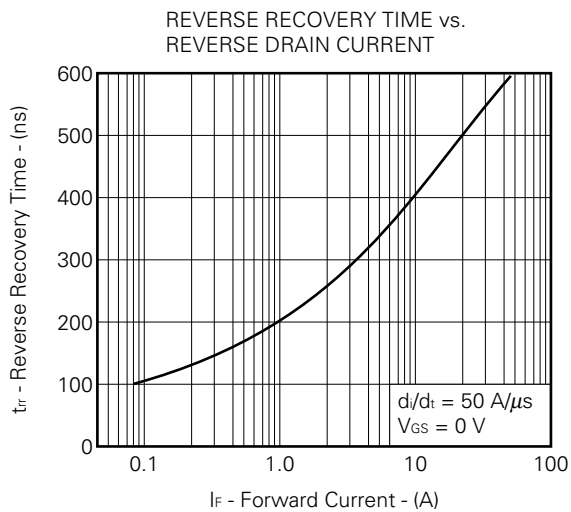
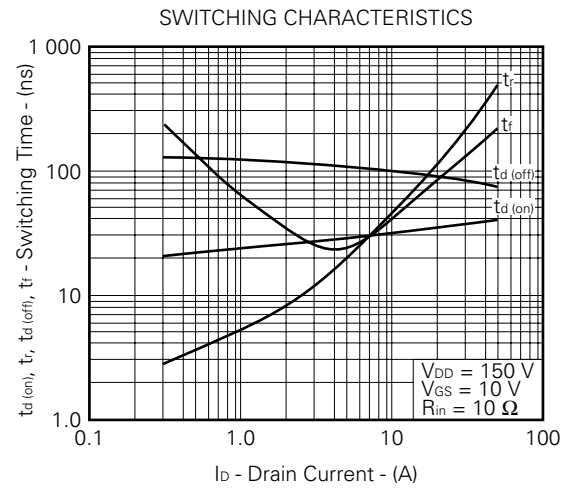
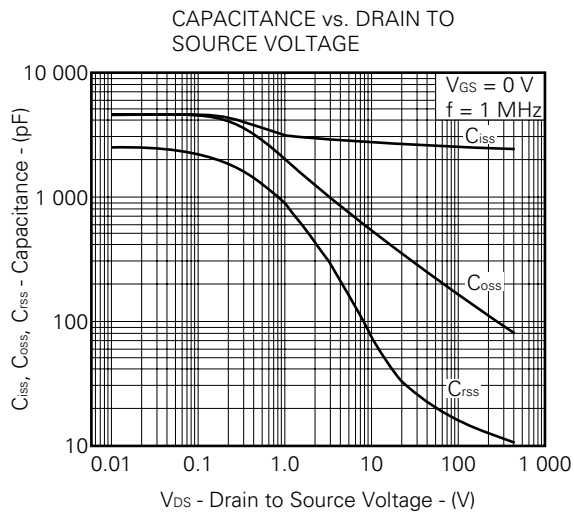
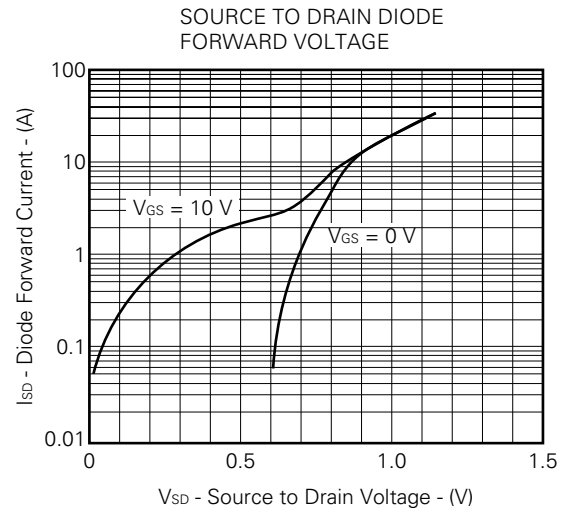
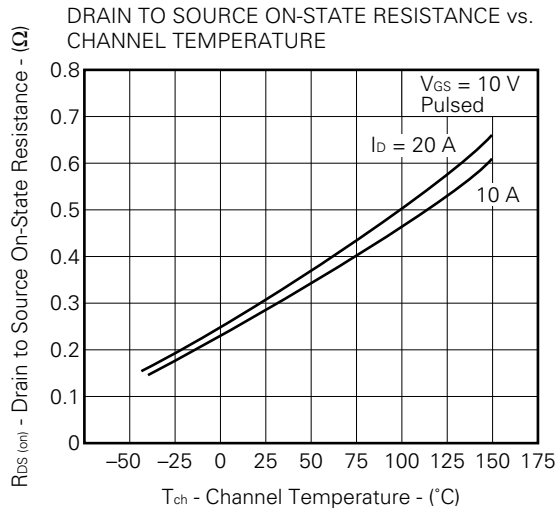


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

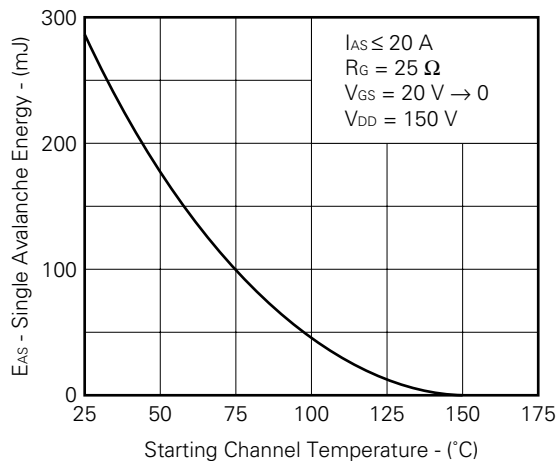


GATE TO SOURCE CUT OFF VOLTAGE vs. CHANNEL TEMPERATURE

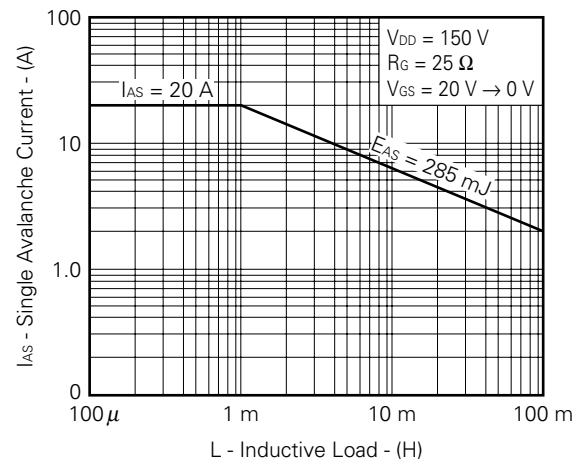




SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



SINGLE AVALANCHE ENERGY vs.
INDUCTIVE LOAD



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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Anti-radioactive design is not implemented in this product.