

74HC540; 74HCT540

Octal buffer/line driver; 3-state; inverting

Rev. 3 — 21 January 2013

Product data sheet

1. General description

The 74HC540; 74HCT540 is an 8-bit inverting buffer/line driver with 3-state outputs. The device features two output enables (\overline{OE}_1 and \overline{OE}_2). A HIGH on \overline{OE}_n causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Inverting outputs
- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC540: CMOS level
 - ◆ For 74HCT540: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40°C to $+85^{\circ}\text{C}$ and from -40°C to $+125^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC540N	-40°C to $+125^{\circ}\text{C}$	DIP20	plastic dual in-line package; 20 leads (300 mil)		SOT146-1
74HCT540N					
74HC540D	-40°C to $+125^{\circ}\text{C}$	SO20	plastic small outline package; 20 leads; body width 7.5 mm		SOT163-1
74HCT540D					
74HC540DB	-40°C to $+125^{\circ}\text{C}$	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm		SOT339-1
74HCT540DB					



4. Functional diagram

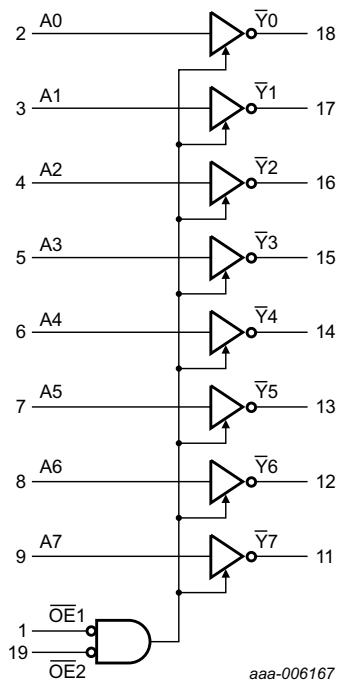


Fig 1. Logic symbol

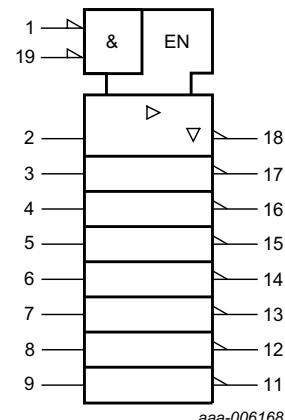


Fig 2. IEC logic symbol

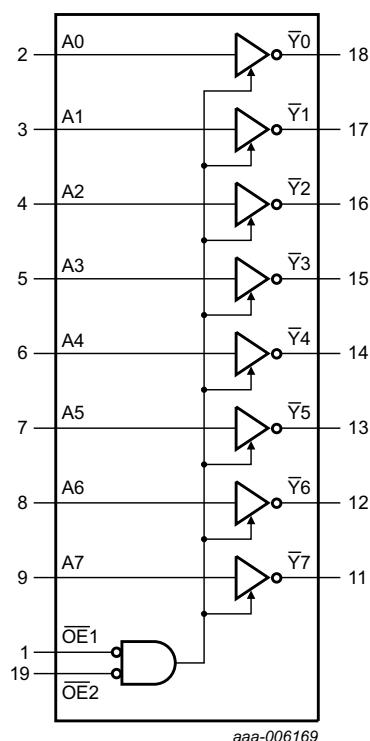


Fig 3. Functional diagram

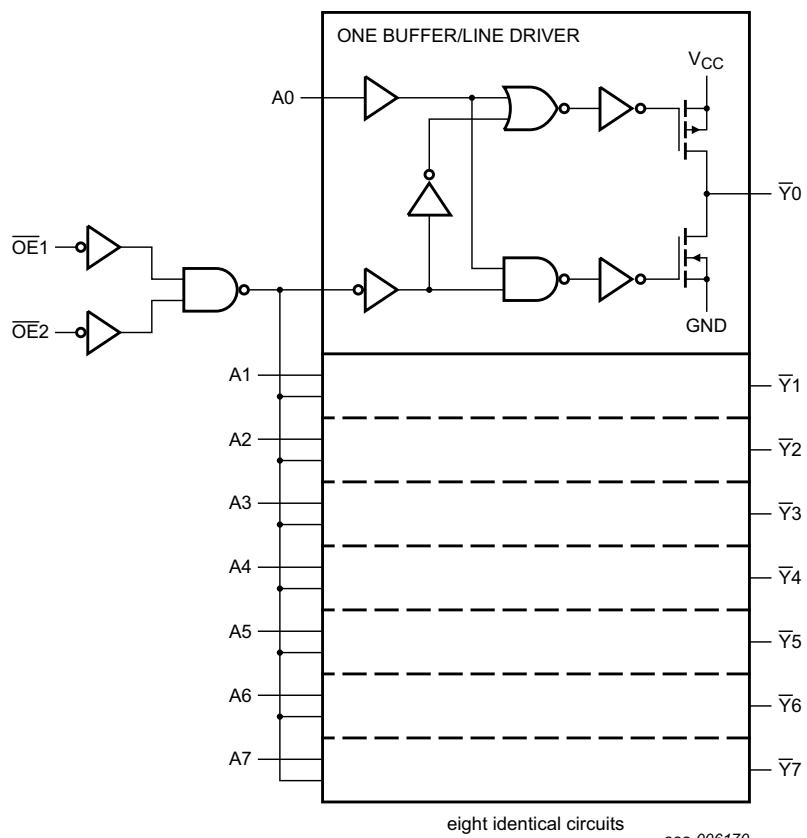


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

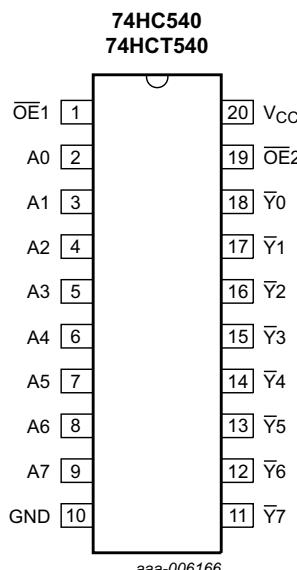


Fig 5. Pin configuration DIP20, SO20 and SSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OE1	1	output enable input (active LOW)
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y0 to Y7	18, 17, 16, 15, 14, 13, 12, 11	data output
OE2	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table^[1]

Control	Input	Output
OE1	OE2	Y _n
L	L	H
L	H	L
X	H	Z
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1] -	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1] -	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		[2]		
	DIP20		-	750	mW
	SO20, SSOP20		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP20 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.

For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

For SSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC540			74HCT540			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC540										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 6.0 V; I _O = 0 A	-	±0.5	-	±5.0	-	±10	-	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT540										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA;	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA;	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A	-	-	±0.5	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; I _O = 0 A; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		An input	-	140	504	-	630	-	686	µA
		OE1 input	-	150	540	-	675	-	735	µA
		OE2 input	-	100	360	-	450	-	490	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristicsGND = 0 V; C_L = 50 pF; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC540								
t _{pd}	propagation delay	An to Y _n ; see Figure 6	[1]					
		V _{CC} = 2.0 V	-	30	100	125	150	ns
		V _{CC} = 4.5 V	-	11	20	25	30	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	9	-	-	-	ns
		V _{CC} = 6.0 V	-	9	17	21	26	ns
t _{en}	enable time	OE _n to Y _n ; see Figure 7	[1]					
		V _{CC} = 2.0 V	-	52	160	200	240	ns
		V _{CC} = 4.5 V	-	19	32	40	48	ns
		V _{CC} = 6.0 V	-	15	27	34	41	ns
t _{dis}	disable time	OE _n to Y _n ; see Figure 7	[1]					
		V _{CC} = 2.0 V	-	61	160	200	240	ns
		V _{CC} = 4.5 V	-	22	32	40	48	ns
		V _{CC} = 6.0 V	-	18	27	34	41	ns

Table 7. Dynamic characteristics*GND = 0 V; $C_L = 50 \text{ pF}$; for test circuit see [Figure 8](#).*

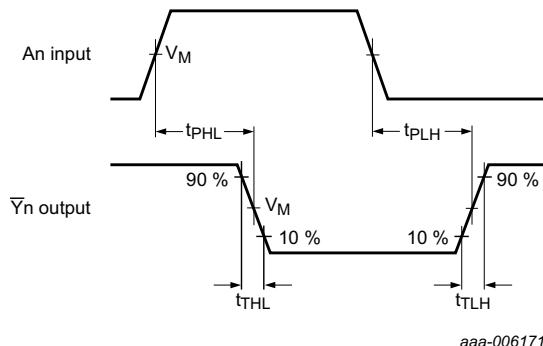
Symbol	Parameter	Conditions	$T_{amb} = 25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
t_t	transition time	see Figure 6	[2]	[2]	[2]	[2]	[2]	ns
C_{PD}	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC}$	[3]	[3]	[3]	[3]	[3]	pF
74HCT540								
t_{pd}	propagation delay	An to Y_n ; see Figure 6	[1]	[1]	[1]	[1]	[1]	ns
t_{en}	enable time	\overline{OEn} to Y_n ; see Figure 7	[1]	[1]	[1]	[1]	[1]	ns
t_{dis}	disable time	\overline{OEn} to Y_n ; see Figure 7	[1]	[1]	[1]	[1]	[1]	ns
t_t	transition time	$V_{CC} = 4.5 \text{ V}$; see Figure 6	[2]	[2]	[2]	[2]	[2]	ns
C_{PD}	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$	[3]	[3]	[3]	[3]	[3]	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} . t_{en} is the same as t_{PZL} and t_{PZH} . t_{dis} is the same as t_{PLZ} and t_{PHZ} .[2] t_t is the same as t_{THL} and t_{TLH} .[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW): $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

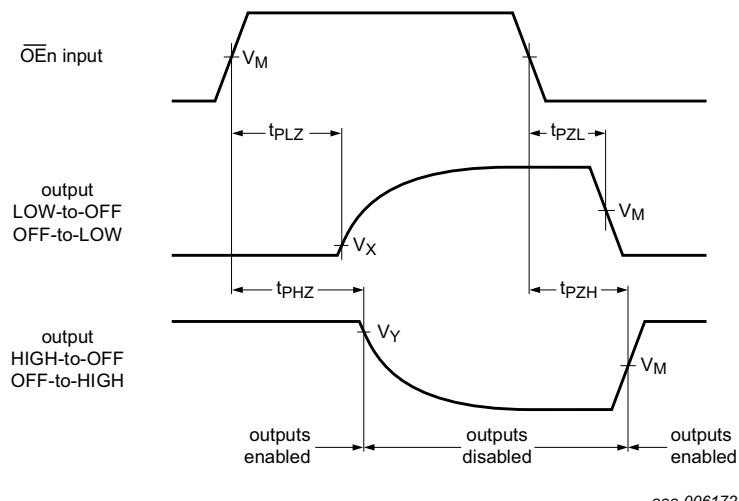
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Input to output propagation delays



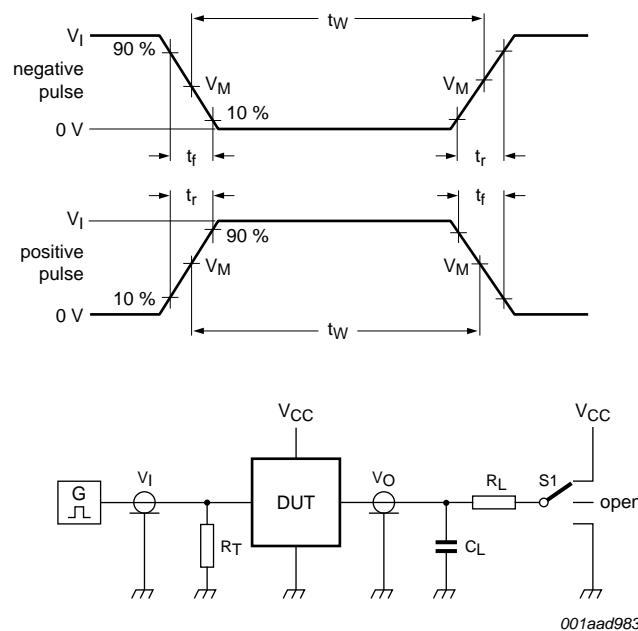
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. 3-state enable and disable times

Table 8. Measurement points

Type	Input	Output		
		V_M	V_M	V_X
74HC540	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}
74HCT540	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance

$S1$ = Test selection switch

Fig 8. Test circuit for measuring switching times

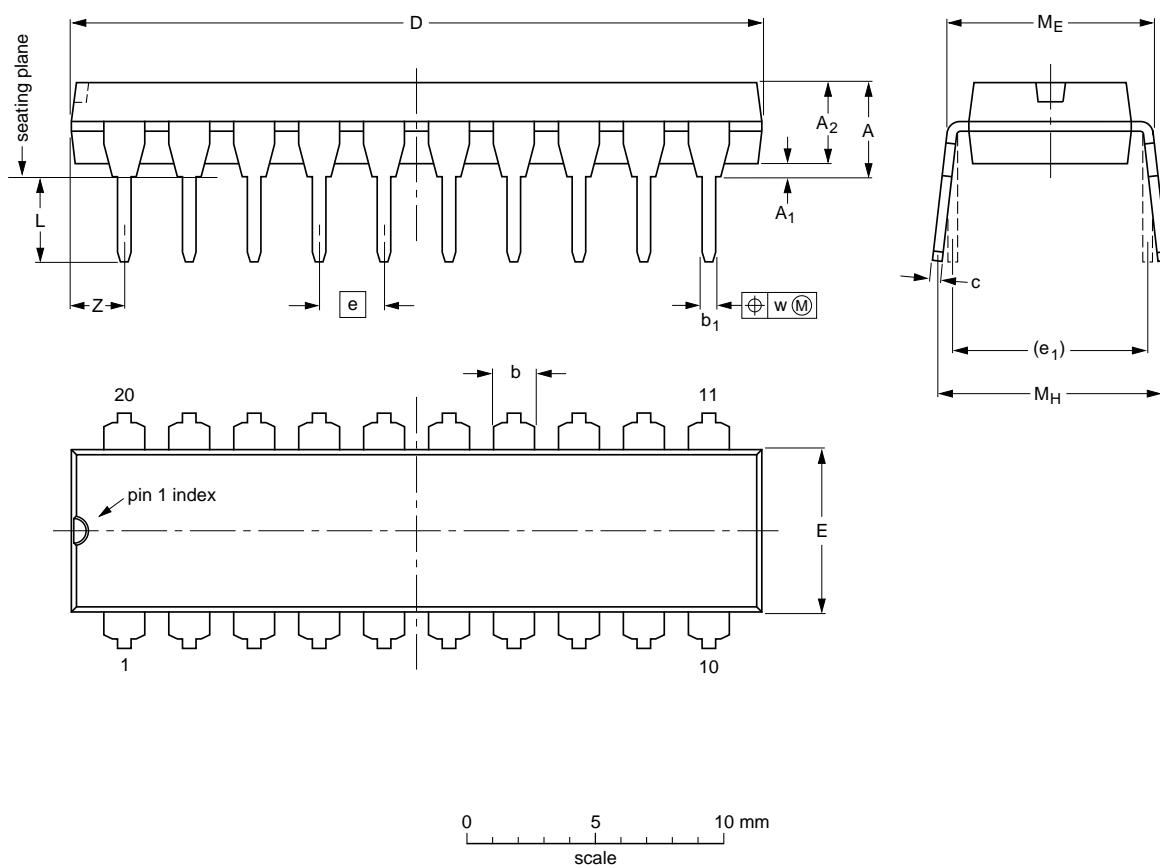
Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC540	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT540	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			99-12-27 03-02-13

Fig 9. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

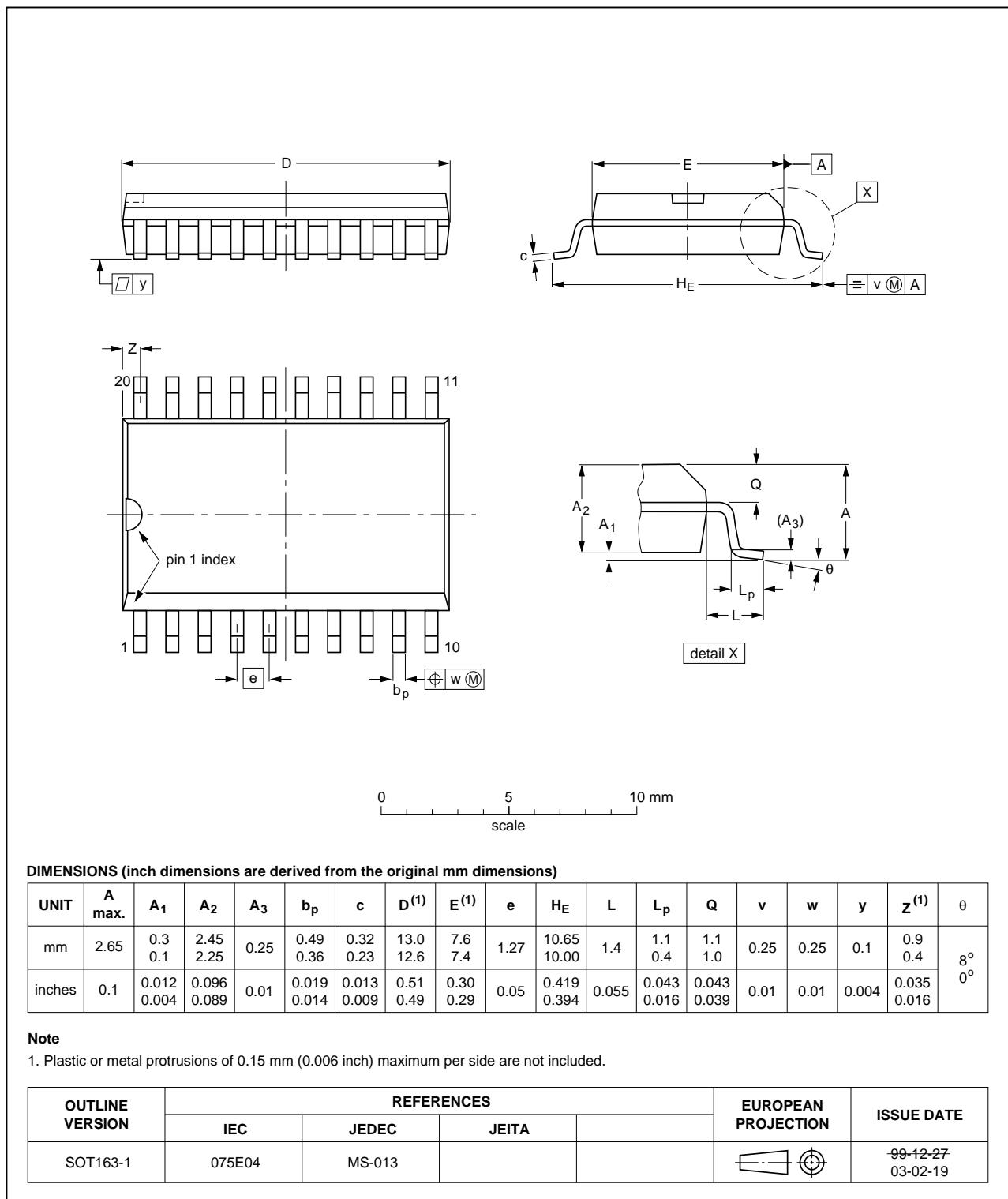


Fig 10. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

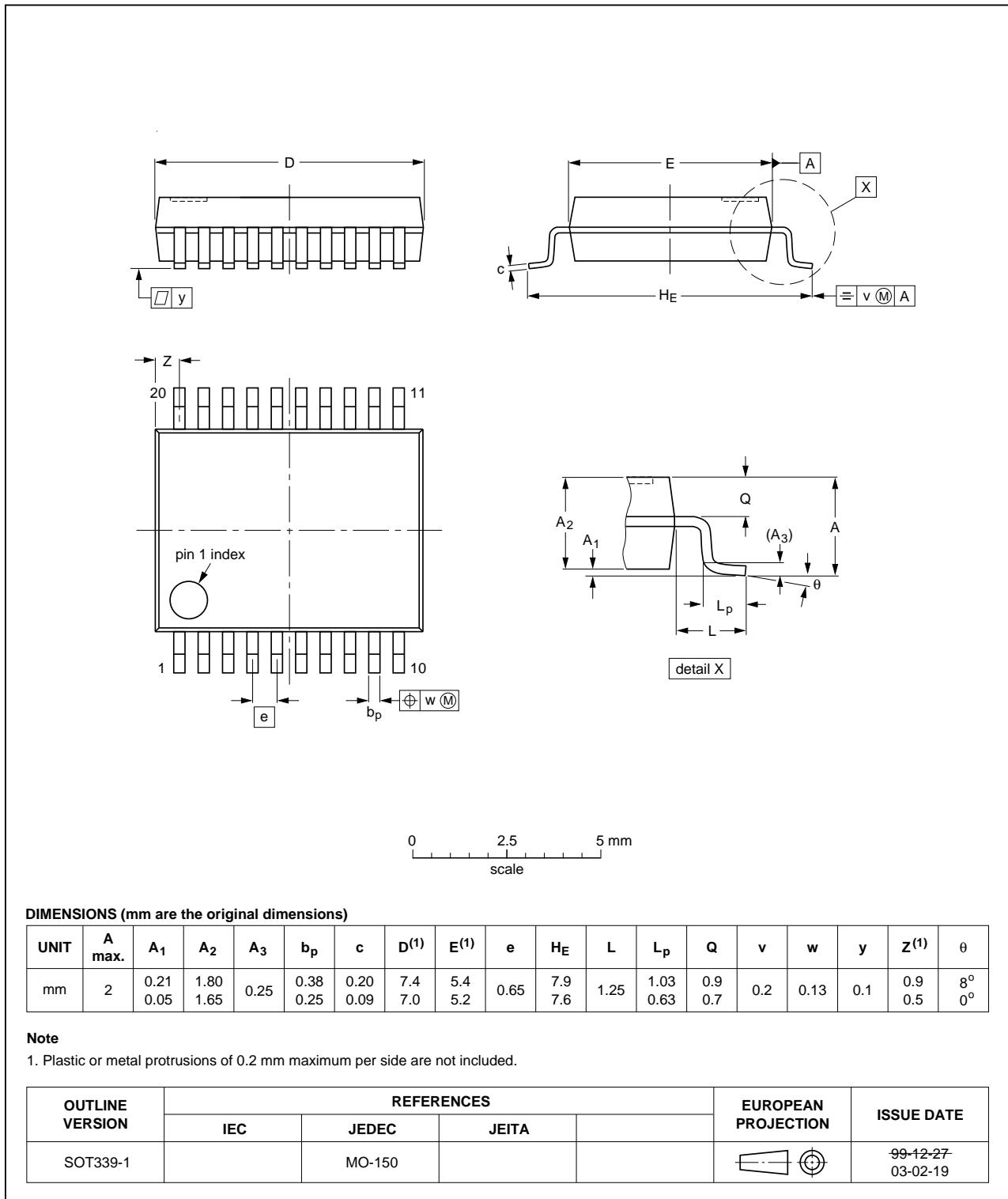


Fig 11. Package outline SOT339-1 (SSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT540 v.3	20130121	Product data sheet	-	74HC_HCT540_CNV v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT540_CNV v.2	19970905	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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