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June 2014

FDMD82100L

Dual N-Channel PowerTrench® MOSFET

100 V, 24 A, 19.5 mΩ

Features

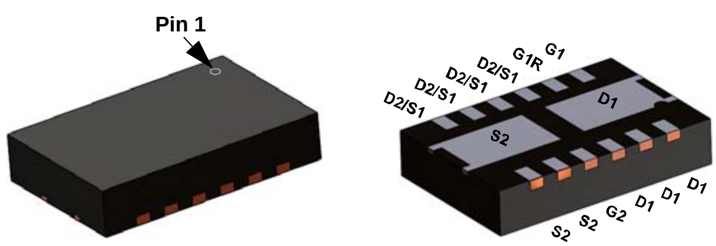
- Max $r_{DS(on)}$ = 19.5 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $r_{DS(on)}$ = 30 mΩ at V_{GS} = 4.5 V, I_D = 5.7 A
- Ideal for flexible layout in primary side of bridge topology
- Termination is Lead-free and RoHS Compliant
- 100% UIL tested
- Kelvin High Side MOSFET drive pin-out capability

General Description

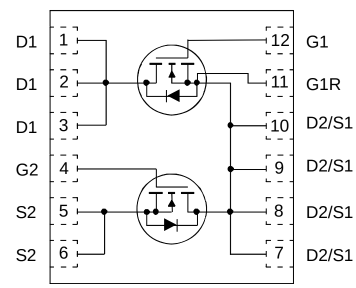
This device includes two 100V N-Channel MOSFETs in a dual Power (3.3 mm X 5 mm) package. HS source and LS Drain internally connected for half/full bridge, low source inductance package, low $r_{DS(on)}$/Qg FOM silicon.

Applications

- Synchronous Buck : Primary Switch of Half / Full bridge converter for telecom
- Motor Bridge : Primary Switch of Half / Full bridge converter for BLDC motor
- MV POL : 48V Synchronous Buck Switch



Power 3.3 x 5



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous T_C = 25 °C	24	A
	-Continuous T_A = 25 °C (Note 1a)	7	
	-Pulsed T_A = 25 °C (Note 4)	80	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	150	mJ
P_D	Power Dissipation T_C = 25 °C	38	W
	Power Dissipation T_A = 25 °C (Note 1a)	2.1	
	Power Dissipation T_A = 25 °C (Note 1b)	1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	130	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
82100L	FDMD82100L	Power 3.3 x 5	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		70		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A		13.5	19.5	mΩ
		V_{GS} = 4.5 V, I_D = 5.7 A		17.9	30	
		V_{GS} = 10 V, I_D = 7 A, T_J = 125 °C		25	36	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 7 A		29		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V f = 1 MHz		1130	1585	pF
C_{oss}	Output Capacitance			173	245	pF
C_{rss}	Reverse Transfer Capacitance			8.1	15	pF
R_g	Gate Resistance		0.1	1.8	3.6	Ω

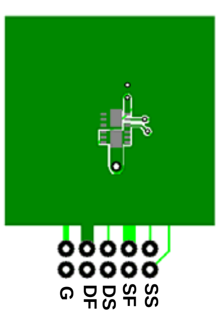
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 7 A V_{GS} = 10 V, R_{GEN} = 6 Ω		7.9	16	ns
t_r	Rise Time			2.8	10	ns
$t_{d(off)}$	Turn-Off Delay Time			21	34	ns
t_f	Fall Time			2.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 7 A		17	24	nC
	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 50 V, I_D = 7 A		8	12	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 7 A		3		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 7 A		2.3		nC

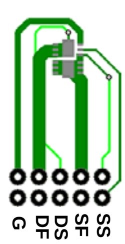
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs		42	67	ns
Q_{rr}	Reverse Recovery Charge			39	62	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 130 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 150 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 10 A, V_{DD} = 90 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 31 A.
4. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics (N-Channel) T_J = 25 °C unless otherwise noted

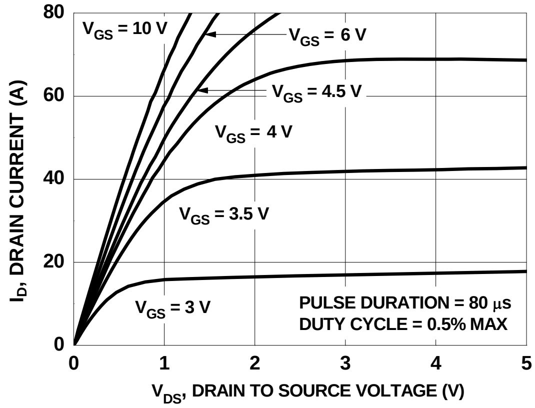


Figure 1. On Region Characteristics

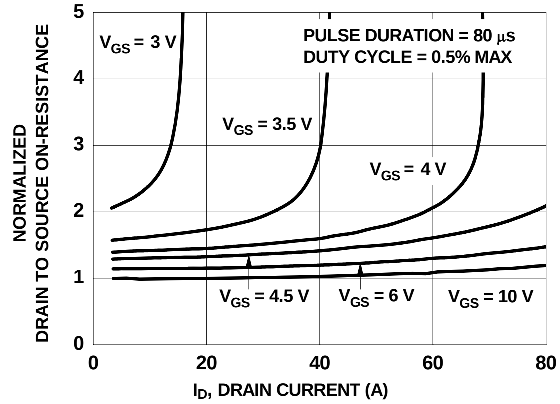


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

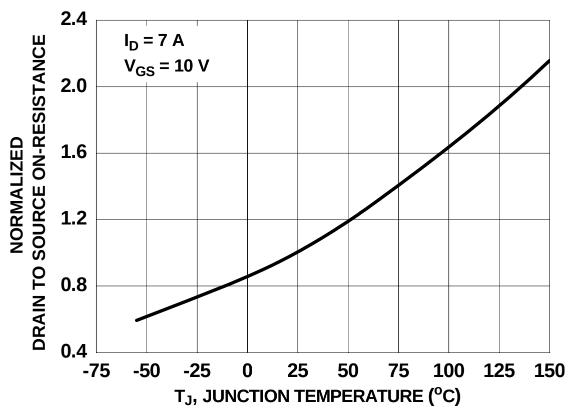


Figure 3. Normalized On Resistance vs Junction Temperature

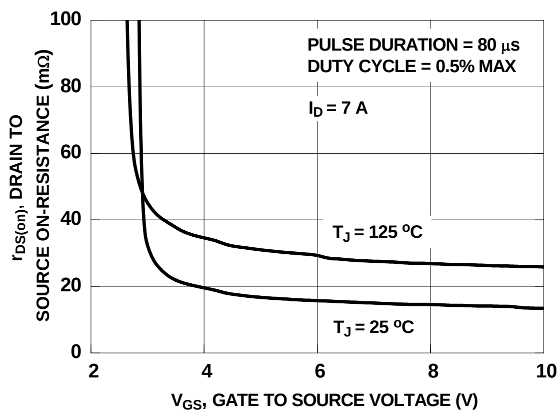


Figure 4. On-Resistance vs Gate to Source Voltage

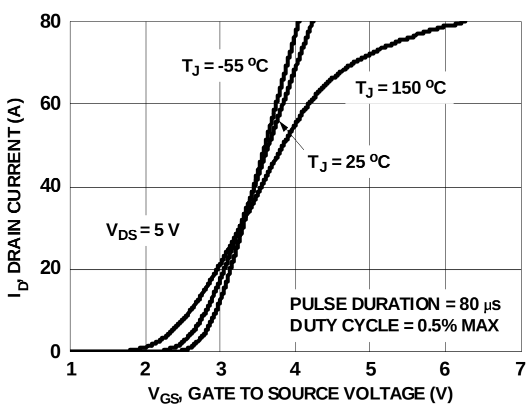


Figure 5. Transfer Characteristics

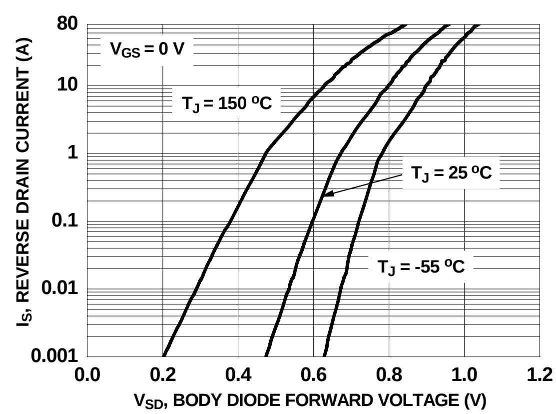


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (N-Channel) T_J = 25 °C unless otherwise noted

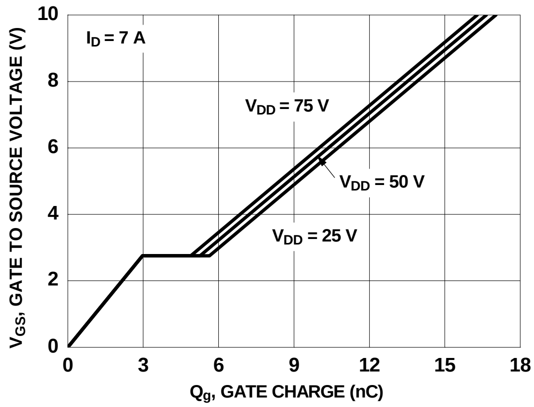


Figure 7. Gate Charge Characteristics

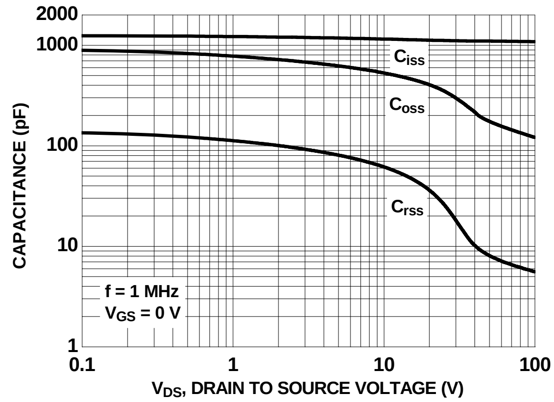


Figure 8. Capacitance vs Drain to Source Voltage

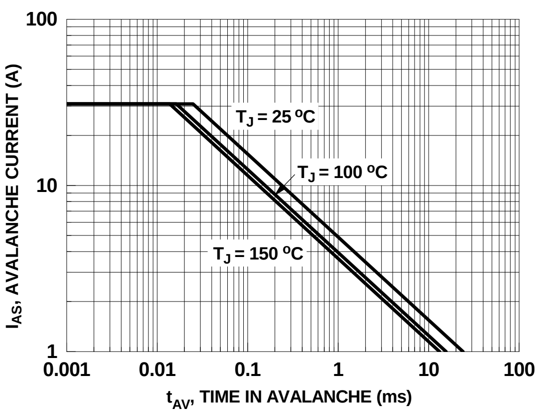


Figure 9. Unclamped Inductive Switching Capability

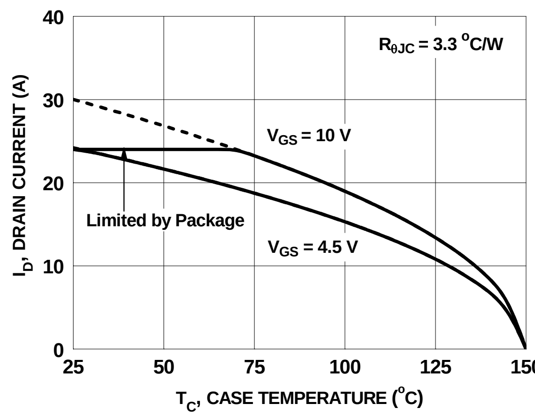


Figure 10. Maximum Continuous Drain Current vs Case Temperature

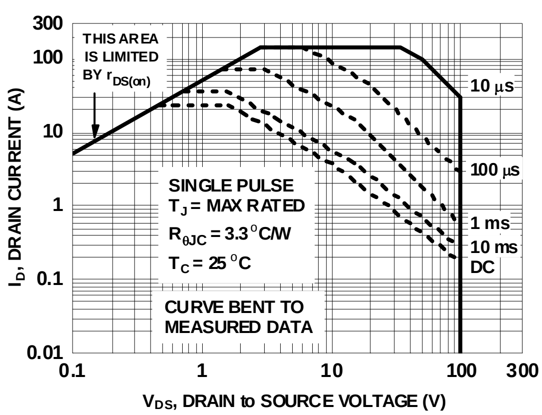


Figure 11. Forward Bias Safe Operating Area

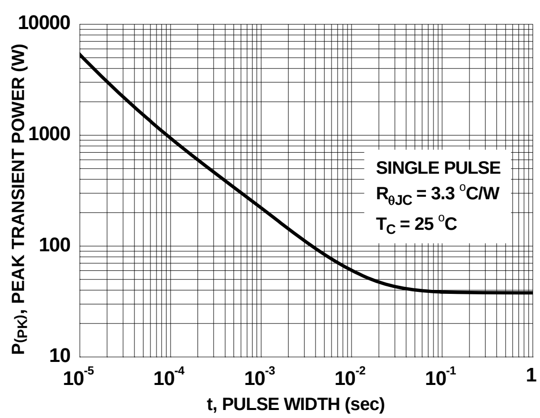


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (N-Channel) T_J = 25 °C unless otherwise noted

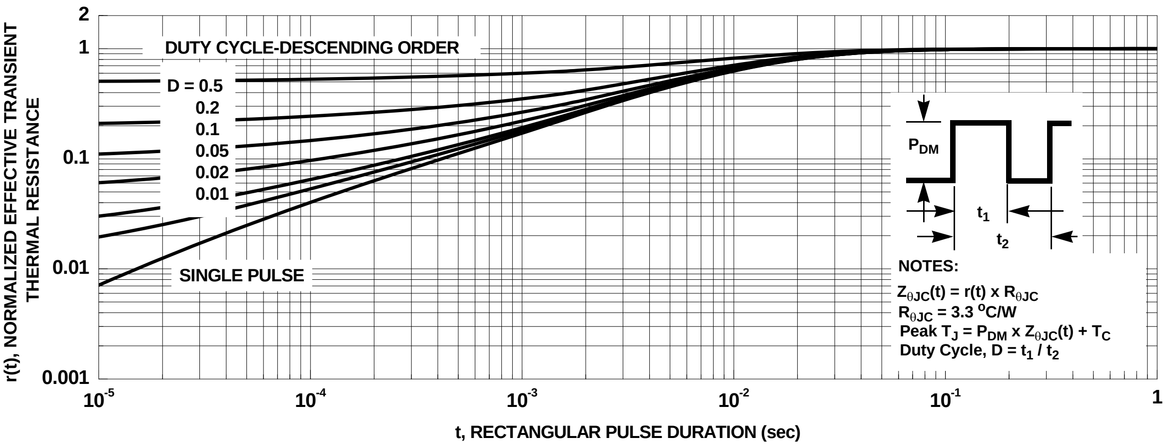
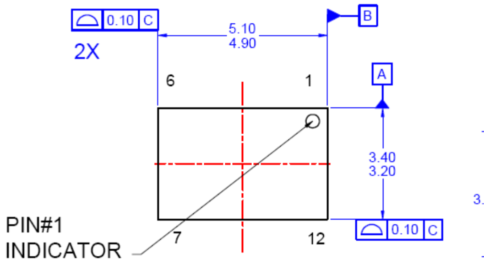
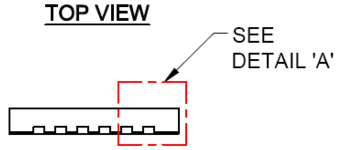


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

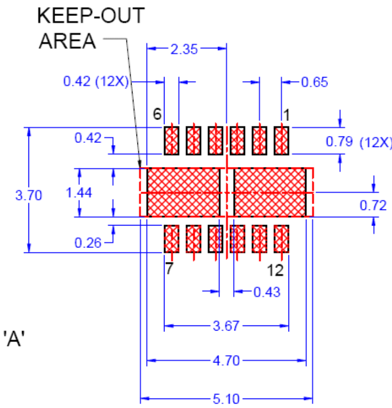
Dimensional Outline and Pad Layout



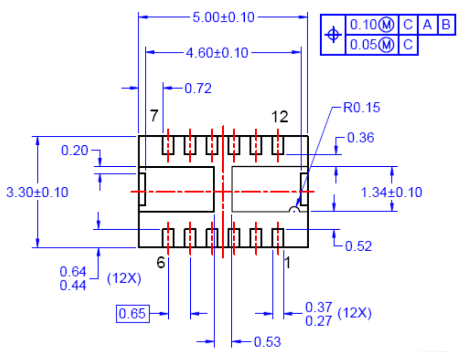
TOP VIEW



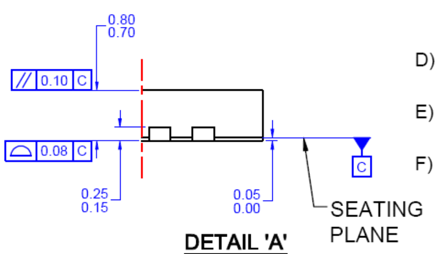
FRONT VIEW



LAND PATTERN
RECOMMENDATION



BOTTOM VIEW



DETAIL 'A'
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229 DATED 8/2012

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: MKT-PQFN12BREV1

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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I68

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