

FEATURES

Throughput: 2 MSPS/1 MSPS options

INL: ± 0.4 LSB maximum

Guaranteed 16-bit no missing codes

Low power

9.5 mW at 2 MSPS, 4.9 mW at 1 MSPS (VDD only)

80 μ W at 10 kSPS, 16 mW at 2 MSPS (total)

SNR: 96.2 dB typical at 1 kHz, $V_{REF} = 5$ V; 95.5 dB typical at 100 kHz

THD: -123 dB typical at 1 kHz, $V_{REF} = 5$ V; -99 dB typical at 100 kHz

Ease of use features reduce system power and complexity

Input overvoltage clamp circuit

Reduced nonlinear input charge kickback

High-Z mode

Long acquisition phase

Input span compression

Fast conversion time allows low SPI clock rates

SPI-programmable modes, read/write capability, status word

Differential analog input range: $\pm V_{REF}$

0 V to V_{REF} with V_{REF} from 2.4 V to 5.1 V

Single 1.8 V supply operation with 1.71 V to 5.5 V logic interface

SAR architecture: no latency/pipeline delay, valid first conversion

First accurate conversion

Guaranteed operation: -40°C to $+125^{\circ}\text{C}$

SPI-/QSPI-/MICROWIRE-/DSP-compatible serial interface

Ability to daisy-chain multiple ADCs and busy indicator

10-lead packages: 3 mm \times 3 mm LFCSP, 3 mm \times 4.90 mm MSOP

APPLICATIONS

Automatic test equipment

Machine automation

Medical equipment

Battery-powered equipment

Precision data acquisition systems

GENERAL DESCRIPTION

The AD4001/AD4005 are low noise, low power, high speed, 16-bit, precision successive approximation register (SAR) analog-to-digital converters (ADCs). The AD4001 offers a 2 MSPS throughput, and the AD4005 offers a 1 MSPS throughput. They incorporate ease of use features that reduce signal chain power consumption, reduce signal chain complexity, and enable higher channel density. The high-Z mode, coupled with a long acquisition phase, eliminates the need for a dedicated high power, high speed ADC driver, thus broadening the range of low power precision amplifiers that can drive these ADCs directly, while still achieving optimum performance. The input span compression feature enables the ADC driver amplifier and the ADC to operate off common supply rails without the need for a negative supply while preserving the full ADC code range. The low serial peripheral interface (SPI) clock rate requirement reduces the digital input/output power consumption, broadens processor options, and simplifies the task of sending data across digital isolation.

Operating from a 1.8 V supply, the AD4001/AD4005 have a $\pm V_{REF}$ fully differential input range with V_{REF} ranging from 2.4 V to 5.1 V. The AD4001 consumes only 16 mW at 2 MSPS with a minimum SCK rate of 70 MHz in turbo mode, and the AD4005 consumes only 8 mW at 1 MSPS. The AD4001/AD4005 both achieve ± 0.4 LSB integral nonlinearity error (INL) maximum, guaranteed no missing codes at 16 bits with 96.2 dB typical signal-to-noise ratio (SNR) for 1 kHz inputs. The reference voltage is applied externally and can be set independently of the supply voltage.

The SPI-compatible, versatile serial interface features seven different modes including the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus, and provides an optional busy indicator. The AD4001/AD4005 are compatible with 1.8 V, 2.5 V, 3 V, and 5 V logic, using the separate VIO supply.

The AD4001/AD4005 are available in a 10-lead MSOP or LFCSP with operation specified from -40°C to $+125^{\circ}\text{C}$. The devices are pin compatible with the 18-bit, 2 MSPS AD4003 (see Table 8).

FUNCTIONAL BLOCK DIAGRAM

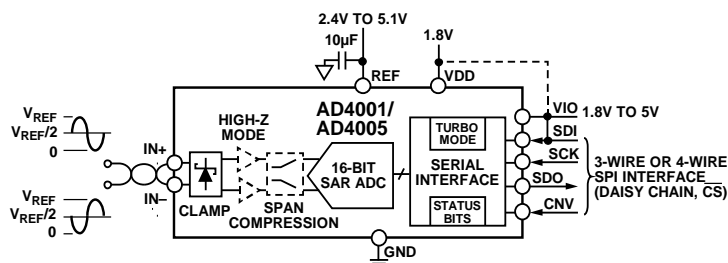


Figure 1.

Rev. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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8/2017—Rev. A to Rev. B

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4/2017—Rev. 0 to Rev. A

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1/2017—Revision 0: Initial Version

SPECIFICATIONS

VDD = 1.71 V to 1.89 V, VIO = 1.71 V to 5.5 V, VREF = 5 V, all specifications TMIN to TMAX, high-Z mode disabled, span compression disabled, turbo mode enabled, and sampling frequency (fs) = 2 MSPS for the AD4001 and fs = 1 MSPS for the AD4005, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	VIN+ – VIN–	–VREF		+VREF	V
Operating Input Voltage	Span compression enabled VIN+, VIN– to GND	–VREF × 0.8 –0.1		+VREF × 0.8 VREF + 0.1	V
Common-Mode Input Range	Span compression enabled	0.1 × VREF		0.9 × VREF	V
Common-Mode Rejection Ratio (CMRR)	fIN = 500 kHz	VREF/2 – 0.125	VREF/2	VREF/2 + 0.125	V
Analog Input Current	Acquisition phase, T = 25°C High-Z mode enabled, converting dc input at 2 MSPS		68 0.3 1		dB nA μA
THROUGHPUT					
Complete Cycle		500			ns
AD4001		1000			ns
AD4005			290	320	ns
Conversion Time					
Acquisition Phase ¹		290			ns
AD4001		790			ns
AD4005					
Throughput Rate ²		0		2	MSPS
AD4001		0		1	MSPS
AD4005					
Transient Response ³			250		ns
DC ACCURACY					
No Missing Codes		16			Bits
Integral Nonlinearity Error (INL)		–0.4	±0.2	+0.4	LSB
Differential Nonlinearity Error (DNL)		–0.5	±0.2	+0.5	LSB
Transition Noise			0.35		LSB
Zero Error		–1.5	±0.1	+1.5	LSB
Zero Error Drift ⁴		–0.28		+0.28	ppm/°C
Gain Error		–16.5	±0.4	+16.5	LSB
Gain Error Drift ⁴		–0.23		+0.23	ppm/°C
Power Supply Sensitivity	VDD = 1.8 V ± 5%		0.25		LSB
1/f Noise ⁵	Bandwidth = 0.1 Hz to 10 Hz		6		μV p-p
AC ACCURACY					
Dynamic Range			96.3		dB
Total RMS Noise			54		μV rms
fIN = 1 kHz, –0.5 dBFS, VREF = 5 V					
Signal-to-Noise Ratio (SNR)		95.6	96.2		dB
Spurious-Free Dynamic Range (SFDR)			122		dB
Total Harmonic Distortion (THD)			–123		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)		95.5	96		dB
Oversampled Dynamic Range	Oversampling ratio (OSR) = 256, VREF = 5 V		120		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$f_{IN} = 1 \text{ kHz}$, -0.5 dBFS , $V_{REF} = 2.5 \text{ V}$					
SNR		92.1	93.2		dB
SFDR			118		dB
THD			-117		dB
SINAD		92	93		dB
$f_{IN} = 100 \text{ kHz}$, -0.5 dBFS , $V_{REF} = 5 \text{ V}$					
SNR			95.5		dB
THD			-99		dB
SINAD			93.8		dB
$f_{IN} = 400 \text{ kHz}$, -0.5 dBFS , $V_{REF} = 5 \text{ V}$					
SNR			91		dB
THD			-92		dB
SINAD			89		dB
-3 dB Input Bandwidth			10		MHz
Aperture Delay			1		ns
Aperture Jitter			1		ps rms
REFERENCE					
Voltage Range, V_{REF}		2.4		5.1	V
Current	$V_{REF} = 5 \text{ V}$				
AD4001	2 MSPS		1.1		mA
AD4005	1 MSPS		0.5		mA
INPUT OVERVOLTAGE CLAMP					
I_{IN+}/I_{IN-} Current, I_{IN+}/I_{IN-}	$V_{REF} = 5 \text{ V}$			50	mA
	$V_{REF} = 2.5 \text{ V}$			50	mA
V_{IN+}/V_{IN-} at Maximum I_{IN+}/I_{IN-}	$V_{REF} = 5 \text{ V}$		5.4		V
	$V_{REF} = 2.5 \text{ V}$		3.1		V
V_{IN+}/V_{IN-} Clamp On/Off Threshold	$V_{REF} = 5 \text{ V}$	5.25	5.4		V
	$V_{REF} = 2.5 \text{ V}$	2.68	2.8		V
Deactivation Time			360		ns
REF Current at Maximum I_{IN+}/I_{IN-}	$V_{IN+}/V_{IN-} > V_{REF}$		100		μA
DIGITAL INPUTS					
Logic Levels					
Input Low Voltage, V_{IL}	$V_{IO} > 2.7 \text{ V}$	-0.3		$+0.3 \times V_{IO}$	V
	$V_{IO} \leq 2.7 \text{ V}$	-0.3		$+0.2 \times V_{IO}$	V
Input High Voltage, V_{IH}	$V_{IO} > 2.7 \text{ V}$	$0.7 \times V_{IO}$		$V_{IO} + 0.3$	V
	$V_{IO} \leq 2.7 \text{ V}$	$0.8 \times V_{IO}$		$V_{IO} + 0.3$	V
Input Low Current, I_{IL}		-1		+1	μA
Input High Current, I_{IH}		-1		+1	μA
Input Pin Capacitance			6		pF
DIGITAL OUTPUTS					
Data Format		Serial 16 bits, twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
Output Low Voltage, V_{OL}	$I_{SINK} = 500 \mu\text{A}$			0.4	V
Output High Voltage, V_{OH}	$I_{SOURCE} = -500 \mu\text{A}$	$V_{IO} - 0.3$			V
POWER SUPPLIES					
VDD		1.71	1.8	1.89	V
VIO		1.71		5.5	V
Standby Current	$V_{DD} = 1.8 \text{ V}$, $V_{IO} = 1.8 \text{ V}$, $T = 25^\circ\text{C}$		1.6		μA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power Dissipation	VDD = 1.8 V, VIO = 1.8 V, V _{REF} = 5 V 10 kSPS, high-Z mode disabled		80		μW
	1 MSPS, high-Z mode disabled		8	9.3	mW
	2 MSPS, high-Z mode disabled		16	18.5	mW
	1 MSPS, high-Z mode enabled		10	12.3	mW
	2 MSPS, high-Z mode enabled		20	24.5	mW
VDD Only	1 MSPS, high-Z mode disabled		4.9		mW
	2 MSPS, high-Z mode disabled		9.5		mW
REF Only	1 MSPS, high-Z mode disabled		2.8		mW
	2 MSPS, high-Z mode disabled		5.5		mW
VIO Only	1 MSPS, high-Z mode disabled		0.4		mW
	2 MSPS, high-Z mode disabled		1.0		mW
Energy per Conversion			8		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T _{MIN} to T _{MAX}	−40		+125	°C

¹ The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS for the AD4001 and 1 MSPS for the AD4005.

² A throughput rate of 2 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 70 MHz. Refer to Table 4 for the maximum achievable throughput for different modes of operation.

³ Transient response is the time required for the ADC to acquire a full-scale input step to ±1 LSB accuracy.

⁴ The minimum and maximum values are guaranteed by characterization, but not production tested.

⁵ See the 1/f noise plot in Figure 23.

TIMING SPECIFICATIONS

VDD = 1.71 V to 1.89 V, VIO = 1.71 V to 5.5 V, VREF = 5 V, all specifications T_{MIN} to T_{MAX}, high-Z mode disabled, span compression disabled, turbo mode enabled, and sampling frequency (f_s) = 2 MSPS for the AD4001 and f_s = 1 MSPS for the AD4005, unless otherwise noted. See Figure 2 for the timing voltage levels.

Table 2. Digital Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION TIME—CNV RISING EDGE TO DATA AVAILABLE	t _{CONV}	270	290	320	ns
ACQUISITION PHASE ¹	t _{ACQ}				
AD4001		290			ns
AD4005		790			ns
TIME BETWEEN CONVERSIONS	t _{CYC}				
AD4001		500			ns
AD4005		1000			ns
CNV PULSE WIDTH (CS MODE) ²	t _{CNVH}	10			ns
SCK PERIOD (CS MODE) ³	t _{SCK}				
VIO > 2.7 V		9.8			ns
VIO > 1.7 V		12.3			ns
SCK PERIOD (DAISY-CHAIN MODE) ⁴	t _{SCK}				
VIO > 2.7 V		20			ns
VIO > 1.7 V		25			ns
SCK LOW TIME	t _{SCKL}	3			ns
SCK HIGH TIME	t _{SCKH}	3			ns
SCK FALLING EDGE TO DATA REMAINS VALID DELAY	t _{HSDO}	1.5			ns
SCK FALLING EDGE TO DATA VALID DELAY	t _{DSDO}				
VIO > 2.7 V			7.5		ns
VIO > 1.7 V			10.5		ns
CNV OR SDI LOW TO SDO D15 MOST SIGNIFICANT BIT (MSB) VALID DELAY (CS MODE)	t _{EN}				
VIO > 2.7 V			10		ns
VIO > 1.7 V			13		ns
CNV RISING EDGE TO FIRST SCK RISING EDGE DELAY	t _{QUIET1}	190			ns
LAST SCK FALLING EDGE TO CNV RISING EDGE DELAY ⁵	t _{QUIET2}	60			ns
CNV OR SDI HIGH OR LAST SCK FALLING EDGE TO SDO HIGH IMPEDANCE (CS MODE)	t _{DIS}		20		ns
SDI VALID SETUP TIME FROM CNV RISING EDGE	t _{SSDICNV}	2			ns
SDI VALID HOLD TIME FROM CNV RISING EDGE (CS MODE)	t _{HSDICNV}	2			ns
SCK VALID HOLD TIME FROM CNV RISING EDGE (DAISY-CHAIN MODE)	t _{HSCKCNV}	12			ns
SDI VALID SETUP TIME FROM SCK RISING EDGE (DAISY-CHAIN MODE)	t _{SSDISCK}	2			ns
SDI VALID HOLD TIME FROM SCK RISING EDGE (DAISY-CHAIN MODE)	t _{HSDISCK}	2			ns

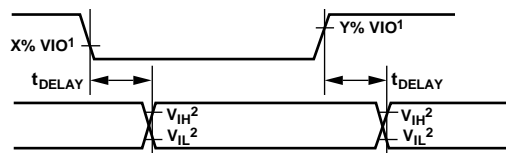
¹ The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS for the AD4001 and 1 MSPS for the AD4005.

² For turbo mode, t_{CNVH} must match the t_{QUIET1} minimum.

³ A throughput rate of 2 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 70 MHz. Refer to Table 4 for the maximum achievable throughput for different modes of operation.

⁴ A 50% duty cycle is assumed for SCK.

⁵ See Figure 22 for SINAD vs. t_{QUIET2}.



¹FOR VIO ≤ 2.7V, X = 80, AND Y = 20; FOR VIO > 2.7V, X = 70, AND Y = 30.

²MINIMUM VIH AND MAXIMUM VIL USED. SEE DIGITAL INPUTS SPECIFICATIONS IN TABLE 1.

15388-002

Figure 2. Voltage Levels for Timing

Table 3. Register Read/Write Timing

Parameter	Symbol	Min	Typ	Max	Unit
READ/WRITE OPERATION					
CNV Pulse Width ¹	t_{CNVH}	10			ns
SCK Period	t_{SCK}				
VIO > 2.7 V		9.8			ns
VIO > 1.7 V		12.3			ns
SCK Low Time	t_{SCKL}	3			ns
SCK High Time	t_{SCKH}	3			ns
READ OPERATION					
CNV Low to SDO D15 MSB Valid Delay	t_{EN}			10	ns
VIO > 2.7 V				13	ns
VIO > 1.7 V					ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	1.5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}			7.5	ns
VIO > 2.7 V				10.5	ns
VIO > 1.7 V				20	ns
CNV Rising Edge to SDO High Impedance	t_{DIS}				ns
WRITE OPERATION					
SDI Valid Setup Time from SCK Rising Edge	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Rising Edge	$t_{HSDISCK}$	2			ns
CNV Rising Edge to SCK Edge Hold Time	$t_{HCNVSCK}$	0			ns
CNV Falling Edge to SCK Active Edge Setup Time	$t_{SCNVSCK}$	6			ns

¹ For turbo mode, t_{CNVH} must match the t_{QUIET1} minimum.

Table 4. Achievable Throughput for Different Modes of Operation

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THROUGHPUT, CS MODE					
3-Wire and 4-Wire Turbo Mode	$f_{SCK} = 100 \text{ MHz}$, VIO $\geq 2.7 \text{ V}$			2	MSPS
	$f_{SCK} = 80 \text{ MHz}$, VIO < 2.7 V			2	MSPS
3-Wire and 4-Wire Turbo Mode and Six Status Bits	$f_{SCK} = 100 \text{ MHz}$, VIO $\geq 2.7 \text{ V}$			2	MSPS
	$f_{SCK} = 80 \text{ MHz}$, VIO < 2.7 V			1.86	MSPS
3-Wire and 4-Wire Mode	$f_{SCK} = 100 \text{ MHz}$, VIO $\geq 2.7 \text{ V}$			1.82	MSPS
	$f_{SCK} = 80 \text{ MHz}$, VIO < 2.7 V			1.69	MSPS
3-Wire and 4-Wire Mode and Six Status Bits	$f_{SCK} = 100 \text{ MHz}$, VIO $\geq 2.7 \text{ V}$			1.64	MSPS
	$f_{SCK} = 80 \text{ MHz}$, VIO < 2.7 V			1.5	MSPS

ABSOLUTE MAXIMUM RATINGS

Note that the input overvoltage clamp cannot sustain the overvoltage condition for an indefinite amount of time.

Table 5.

Parameter	Rating
Analog Inputs IN+, IN– to GND ¹	–0.3 V to $V_{REF} + 0.4$ V or ± 50 mA
Supply Voltage REF, VIO to GND	–0.3 V to +6.0 V
VDD to GND	–0.3 V to +2.1 V
VDD to VIO	–6 V to +2.4 V
Digital Inputs to GND	–0.3 V to VIO + 0.3 V
Digital Outputs to GND	–0.3 V to VIO + 0.3 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature Soldering	260°C reflow as per JEDEC J-STD-020
ESD Ratings	
Human Body Model	4 kV
Machine Model	200 V
Field Induced Charged Device Model	1.25 kV

¹ See the Analog Inputs section for an explanation of IN+ and IN–.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 6. Thermal Resistance

Package Type ¹	θ_{JA} ²	θ_{JC} ³	Unit
RM-10	147	38	°C/W
CP-10-9	114	33	°C/W

¹ Test Condition 1: thermal impedance simulated values are based upon use of 2S2P JEDEC PCB. See the Ordering Guide.

² θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

³ θ_{JC} is the junction-to-case thermal resistance.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

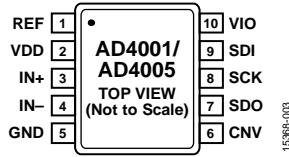
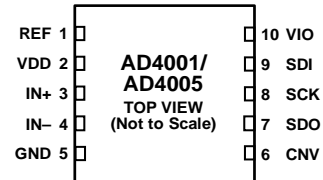


Figure 3. 10-Lead MSOP Pin Configuration



NOTES
1. CONNECT THE EXPOSED PAD TO GND. THIS CONNECTION IS NOT REQUIRED TO MEET THE SPECIFIED PERFORMANCE.

Figure 4. 10-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1	REF	AI	Reference Input Voltage. The V_{REF} range is 2.4 V to 5.1 V. This pin is referred to the GND pin and must be decoupled closely to the GND pin with a 10 μ F, X7R ceramic capacitor.
2	VDD	P	1.8 V Power Supply. The VDD range is 1.71 V to 1.89 V. Bypass VDD to GND with a 0.1 μ F ceramic capacitor.
3	IN+	AI	Differential Positive Analog Input. See the Differential Input Considerations section.
4	IN–	AI	Differential Negative Analog Input. See the Differential Input Considerations section.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device: daisy-chain mode or \overline{CS} mode. In \overline{CS} mode, the SDO pin is enabled when CNV is low. In daisy-chain mode, the data is read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Daisy-chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. \overline{CS} mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled. With CNV low, the device can be programmed by clocking in a 16-bit word on SDI on the rising edge of SCK.
10	VIO	P	Input/Output Interface Digital Power. Nominally, this pin is at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). Bypass VIO to GND with a 0.1 μ F ceramic capacitor.
N/A ²	EPAD	P	Exposed Pad (LFCSP Only). Connect the exposed pad to GND. This connection is not required to meet the specified performance.

¹ AI is analog input, P is power, DI is digital input, and DO is digital output.

² N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 1.8\text{ V}$, $V_{IO} = 3.3\text{ V}$, $V_{REF} = 5\text{ V}$, $T = 25^\circ\text{C}$, high-Z mode disabled, span compression disabled, turbo mode enabled, and sampling frequency (f_s) = 2 MSPS for the AD4001 and $f_s = 1\text{ MSPS}$ for the AD4005, unless otherwise noted.

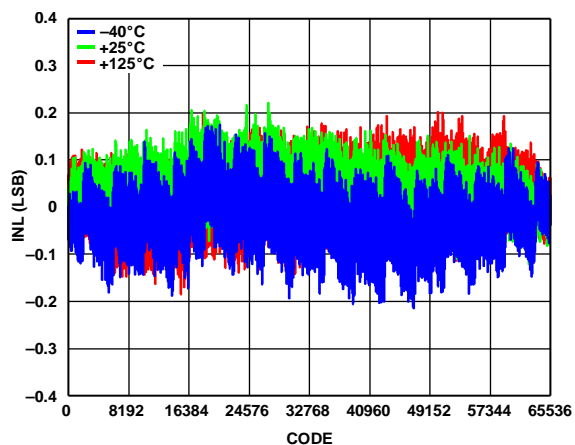


Figure 5. INL vs. Code for Various Temperatures, $V_{REF} = 5\text{ V}$

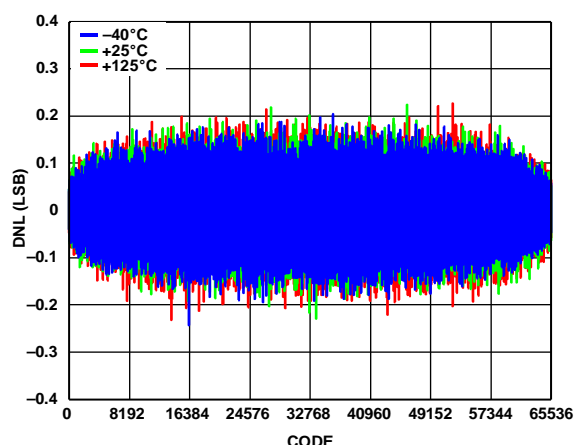


Figure 8. DNL vs. Code for Various Temperatures, $V_{REF} = 5\text{ V}$

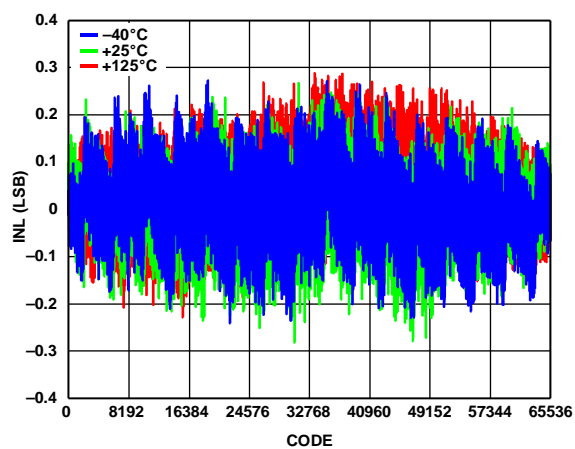


Figure 6. INL vs. Code for Various Temperatures, $V_{REF} = 2.5\text{ V}$

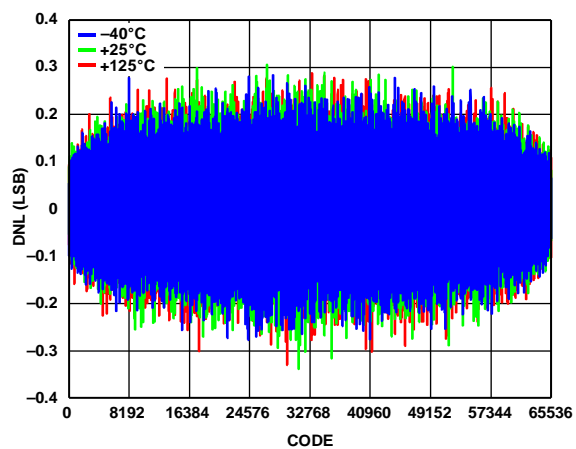


Figure 9. DNL vs. Code for Various Temperatures, $V_{REF} = 2.5\text{ V}$

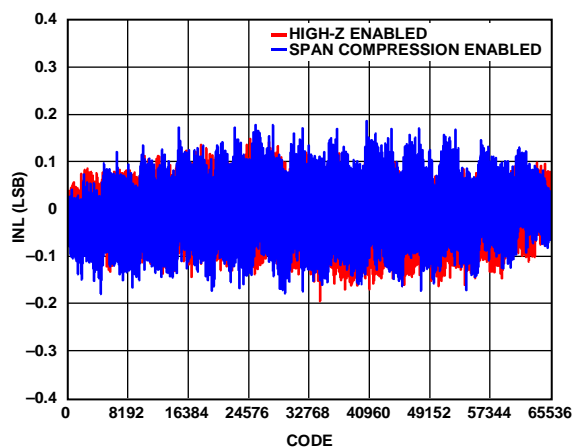


Figure 7. INL vs. Code, High-Z and Span Compression Modes Enabled, $V_{REF} = 5\text{ V}$

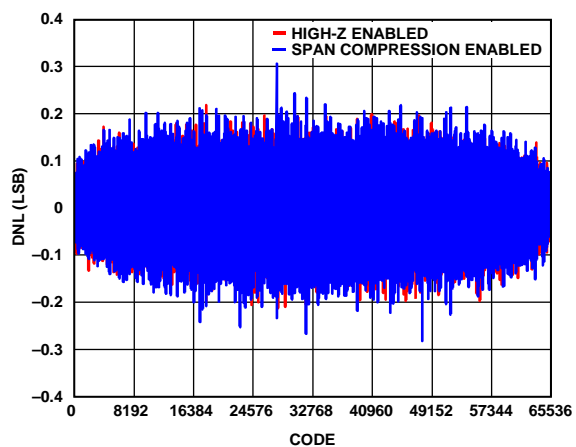


Figure 10. DNL vs. Code, High-Z and Span Compression Modes Enabled, $V_{REF} = 5\text{ V}$

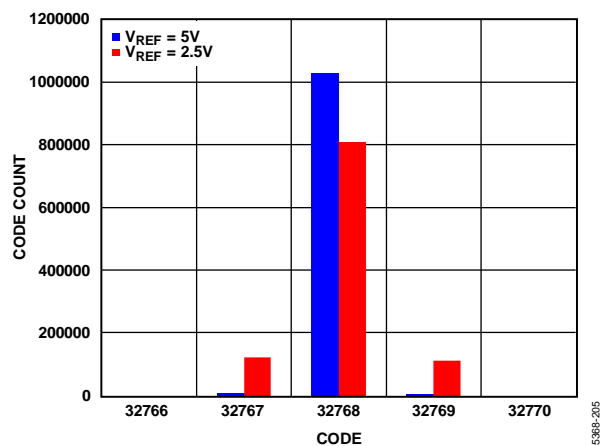


Figure 11. Histogram of a DC Input at Code Center, $V_{REF} = 2.5V$ and $V_{REF} = 5V$

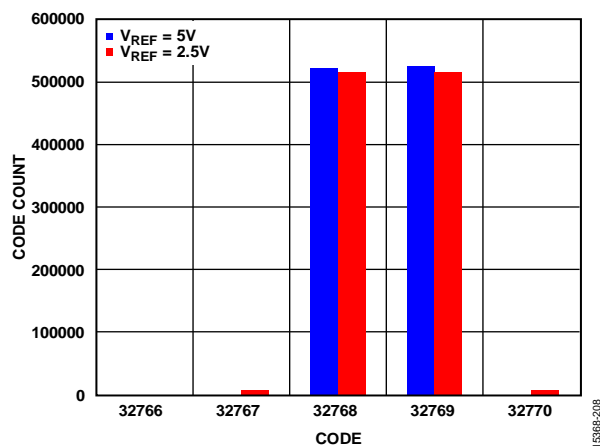


Figure 14. Histogram of a DC Input at Code Transition, $V_{REF} = 2.5V$ and $V_{REF} = 5V$

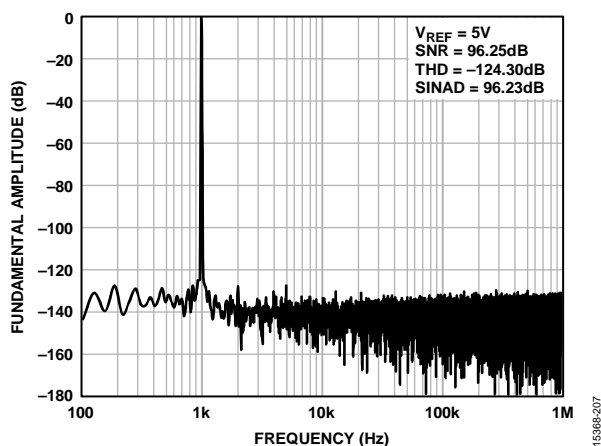


Figure 12. 1 kHz, -0.5 dBFS Input Tone FFT, Wide View, $V_{REF} = 5V$

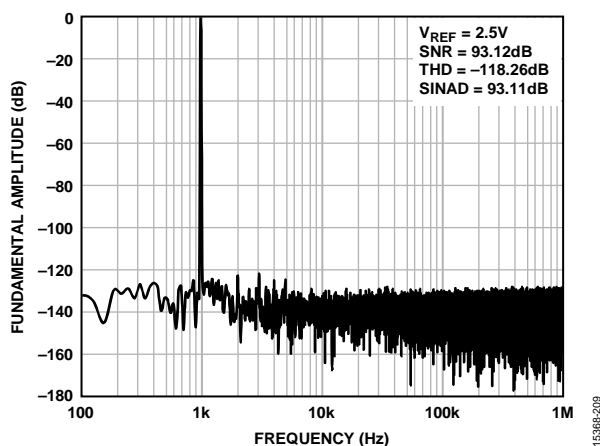


Figure 15. 1 kHz, -0.5 dBFS Input Tone FFT, Wide View, $V_{REF} = 2.5V$

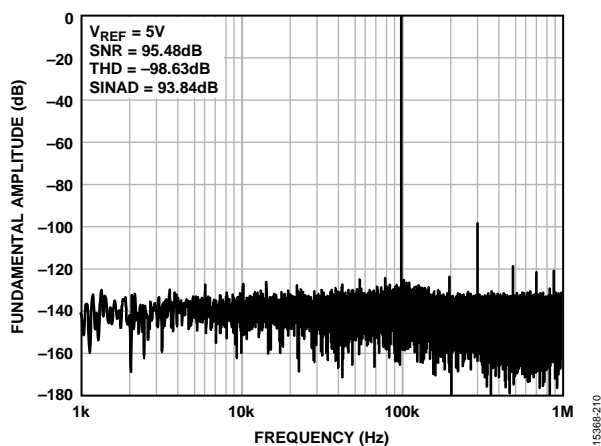


Figure 13. 100 kHz, -0.5 dBFS Input Tone FFT, Wide View

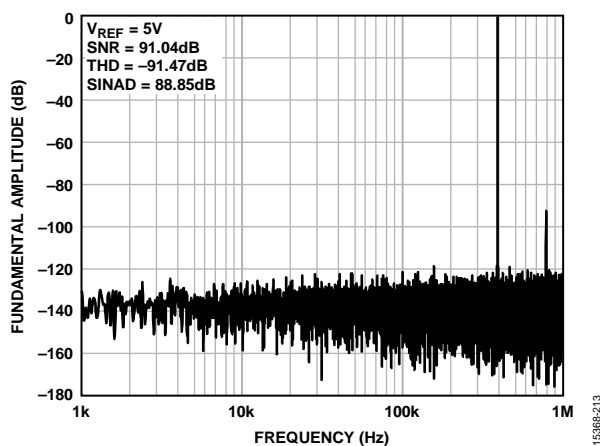


Figure 16. 400 kHz, -0.5 dBFS Input Tone FFT, Wide View

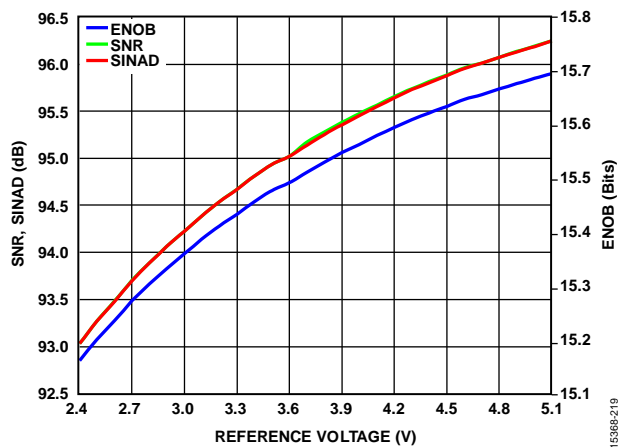
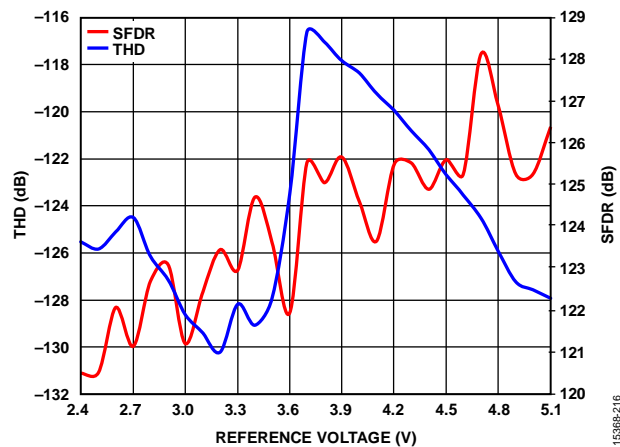
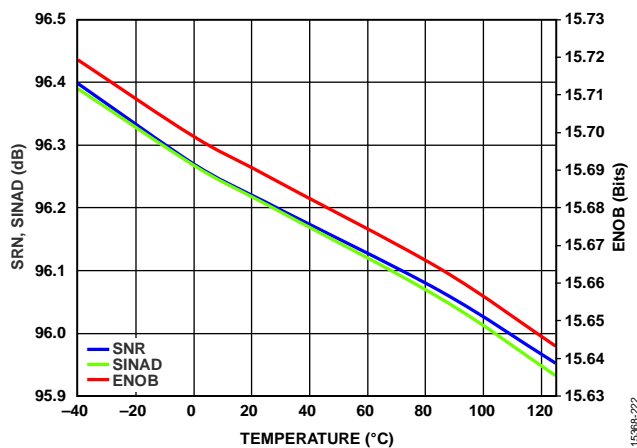
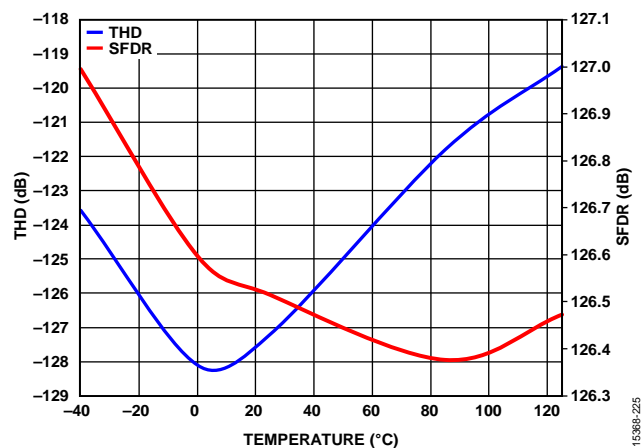
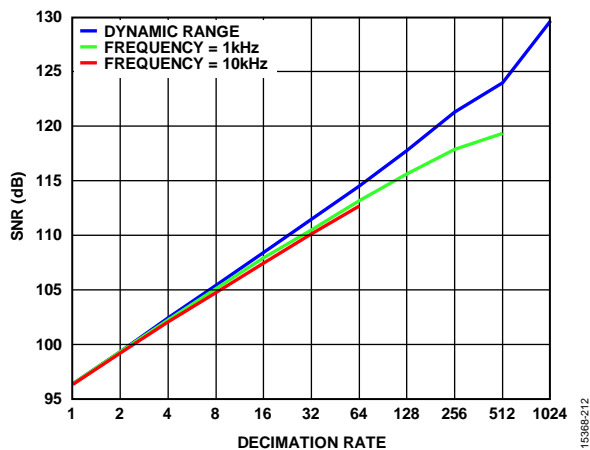
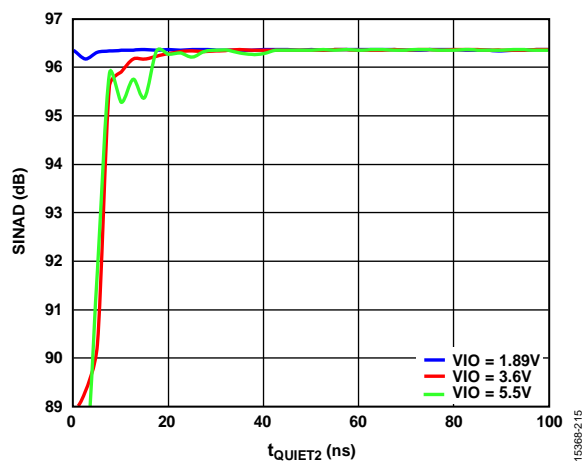
Figure 17. SNR, SINAD, and ENOB vs. Reference Voltage, $f_{IN} = 1$ kHzFigure 20. THD and SFDR vs. Reference Voltage, $f_{IN} = 1$ kHzFigure 18. SNR, SINAD, and ENOB vs. Temperature, $f_{IN} = 1$ kHzFigure 21. THD and SFDR vs. Temperature, $f_{IN} = 1$ kHz

Figure 19. SNR vs. Decimation Rate for Various Input Frequencies, 2 MSPS

Figure 22. SINAD vs. t_{QUIET2}

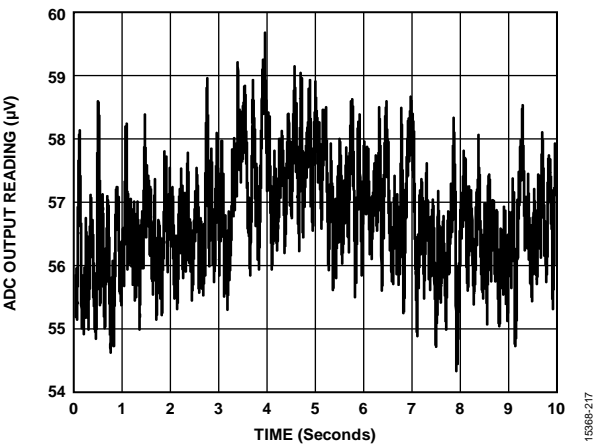


Figure 23. 1/f Noise for 0.1 Hz to 10 Hz Bandwidth, 50 kSPS, 2500 Samples Averaged per Reading

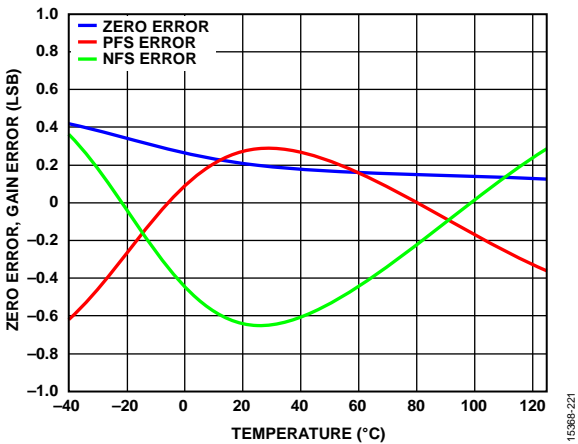


Figure 25. Zero Error and Gain Error vs. Temperature, Positive Full Scale (PFS) and Negative Full Scale (NFS)

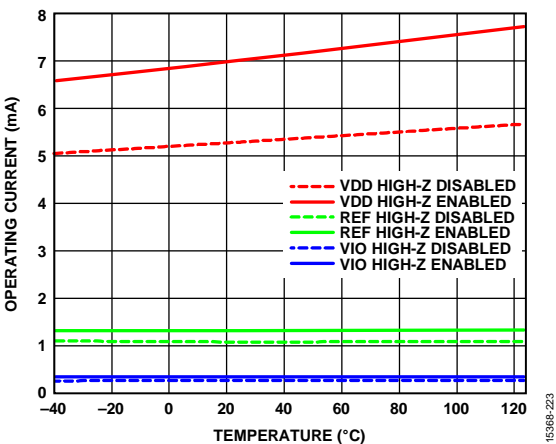


Figure 24. Operating Current vs. Temperature, AD4001, 2 MSPS

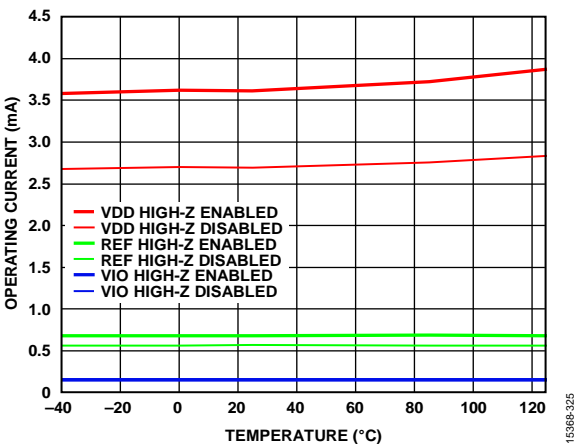


Figure 26. Operating Current vs. Temperature, AD4005, 1 MSPS

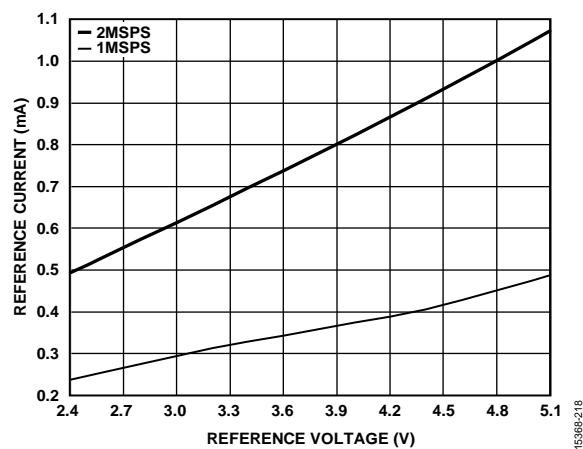


Figure 27. Reference Current vs. Reference Voltage

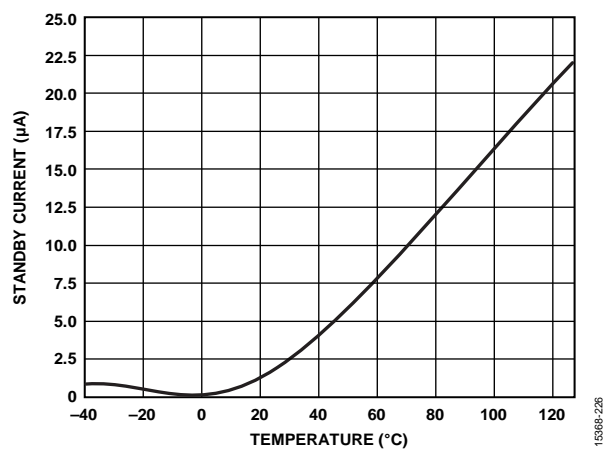
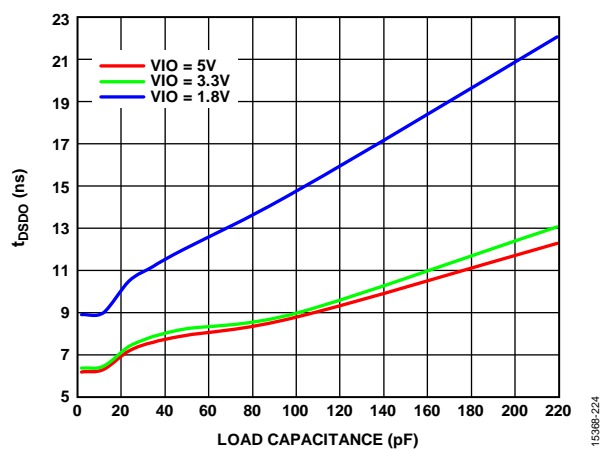


Figure 29. Standby Current vs. Temperature

Figure 28. t_{DSDO} vs. Load Capacitance

TERMINOLOGY

Integral Nonlinearity Error (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 31).

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error

Zero error is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

Gain Error

The first transition (from 100 ... 00 to 100 ... 01) occurs at a level ½ LSB above nominal negative full scale (–4.999981 V for the ±5 V range). The last transition (from 011 ... 10 to 011 ... 11) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.999943 V for the ±5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

ENOB is expressed in bits.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured. The value for dynamic range is expressed in decibels. It is measured with a signal at –60 dBFS so that it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the ADC to acquire a full-scale input step to ±1 LSB accuracy.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the ADC output at the frequency, f , to the power of a 200 mV p-p sine wave applied to the common-mode voltage of IN+ and IN– of frequency, f .

$$CMRR (dB) = 10 \log(P_{ADC_IN}/P_{ADC_OUT})$$

where:

P_{ADC_IN} is the common-mode power at the frequency, f , applied to the IN+ and IN– inputs.

P_{ADC_OUT} is the power at the frequency, f , in the ADC output.

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of the power in the ADC output at the frequency, f , to the power of a 200 mV p-p sine wave applied to the ADC VDD supply of frequency, f .

$$PSRR (dB) = 10 \log(P_{VDD_IN}/P_{ADC_OUT})$$

where:

P_{VDD_IN} is the power at the frequency, f , at the VDD pin.

P_{ADC_OUT} is the power at the frequency, f , in the ADC output.

THEORY OF OPERATION

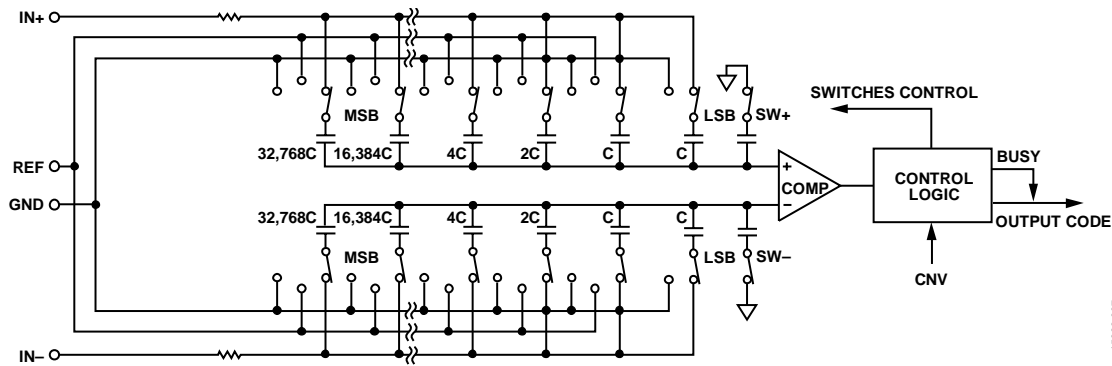


Figure 30. ADC Simplified Schematic

CIRCUIT INFORMATION

The **AD4001/AD4005** are high speed, low power, single-supply, precise, 16-bit ADCs based on a SAR architecture.

The **AD4001** is capable of converting 2,000,000 samples per second (2 MSPS), the **AD4005** is capable of converting 1,000,000 samples per second (1 MSPS). The power consumption of the **AD4001/AD4005** scales with throughput because they power down in between conversions. When operating at 10 kSPS, for example, they typically consume 80 μ W, making them ideal for battery-powered applications. The **AD4001/AD4005** also have a valid first conversion after being powered down for long periods, which can further reduce power consumed in applications in which the ADC does not need to be constantly converting.

The **AD4001/AD4005** provide the user with an on-chip track-and-hold and do not exhibit any pipeline delay or latency, making them ideal for multiplexed applications.

The **AD4001/AD4005** incorporate a multitude of unique ease of use features that result in a lower system power and footprint.

The **AD4001/AD4005** each have an internal voltage clamp that protects the device from overvoltage damage on the analog inputs.

The analog input incorporates circuitry that reduces the nonlinear charge kickback seen from a typical switched capacitor SAR input. This reduction in kickback, combined with a longer acquisition phase, means reduced settling requirements on the driving amplifier. This combination allows the use of lower bandwidth and lower power amplifiers as drivers. It has the additional benefit of allowing a larger resistor value in the input RC filter and a corresponding smaller capacitor, which results in a smaller RC load for the amplifier, improving stability and power dissipation.

High-Z mode can be enabled via the SPI interface by programming a register bit (see Table 14). When high-Z mode is enabled, the ADC input has a low input charging current at low input signal frequencies, as well as improved distortion over a wide frequency range up to 100 kHz. For frequencies greater than 100 kHz and multiplexing, disable high-Z mode.

For single-supply applications, a span compression feature creates additional headroom and footroom for the driving amplifier to access the full range of the ADC.

The fast conversion time of the **AD4001/AD4005**, along with turbo mode, allows low clock rates to read back conversions even when running at their maximum throughput rates of 2 MSPS/1 MSPS. Note that, for the **AD4001**, a throughput rate of 2 MSPS can be achieved only with turbo mode enabled.

The **AD4001/AD4005** can interface with any 1.8 V to 5 V digital logic family. They are available in a 10-lead MSOP or a tiny 10-lead LFCSP that allows space savings and flexible configurations.

The **AD4001/AD4005** are pin for pin compatible with some of the 14-/16-/18-/20-bit precision SAR ADCs listed in Table 8.

Table 8. MSOP and LFCSP 14-/16-/18-/20-Bit Precision SAR ADCs

Bits	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	≥ 1000 kSPS
20 ¹				AD4020 ²
18 ¹	AD7989-1 ²	AD7691 ²	AD7690 ² , AD7989-5 ² , AD4011 ²	AD4003 ² , AD4007 ² , AD7982 ² , AD7984 ²
16 ¹	AD7684	AD7687 ²	AD7688 ² , AD7693 ² , AD7916 ²	AD4001, AD4005, AD7915 ²
16 ³	AD7680, AD7683, AD7988-1 ²	AD7685 ² , AD7694	AD7686 ² , AD7988-5 ²	AD4000 ² , AD4004 ² , AD7980 ² , AD7983 ²
14 ³	AD7940	AD7942 ²	AD7946 ²	Not applicable

¹ True differential.

² Pin for pin compatible.

³ Pseudo differential.

CONVERTER OPERATION

The AD4001/AD4005 are SAR-based ADCs using a charge redistribution sampling digital-to-analog converter (DAC). Figure 30 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via the SW+ and SW– switches. All independent switches connect the other terminal of each capacitor to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN– inputs.

When the acquisition phase is complete and the CNV input goes high, a conversion phase initiates. When the conversion phase begins, SW+ and SW– are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. The differential voltage between the IN+ and IN– inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and V_{REF} , the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$, ..., $V_{REF}/65,536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After

the completion of this process, the control logic generates the ADC output code and a busy signal indicator.

Because the AD4001 and the AD4005 have on-board conversion clocks, the serial clock, SCK, is not required for the conversion process.

TRANSFER FUNCTIONS

The ideal transfer characteristics for the AD4001/AD4005 are shown in Figure 31 and Table 9.

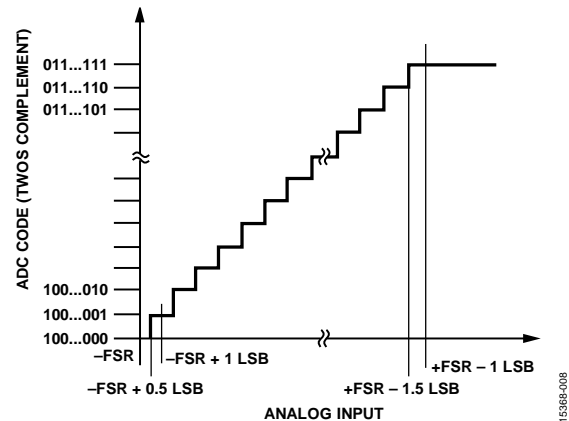


Figure 31. ADC Ideal Transfer Function (FSR Is Full-Scale Range)

Table 9. Output Codes and Ideal Input Voltages

Description	Analog Input, $V_{REF} = 5\text{ V}$	$V_{REF} = 5\text{ V}$ with Span Compression Enabled	Digital Output Code (Hex)
+FSR – 1 LSB	+4.999847 V	+3.999878 V	0x7FFF ¹
Midscale + 1 LSB	+152.6 μV	+122.1 μV	0x0001
Midscale	0 V	0 V	0x0000
Midscale – 1 LSB	–152.6 μV	–122.1 μV	0xFFFF
–FSR + 1 LSB	–4.999847 V	–3.999878 V	0x8001
–FSR	–5 V	–4 V	0x8000 ²

¹ This output code is also the code for an overranged analog input ($V_{IN+} - V_{IN-}$ above V_{REF} with span compression disabled and above $0.8 \times V_{REF}$ with span compression enabled).

² This output code is also the code for an underranged analog input ($V_{IN+} - V_{IN-}$ below $-V_{REF}$ with span compression disabled and below $-0.8 \times V_{REF}$ with span compression enabled).

APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAMS

Figure 32 shows an example of the recommended connection diagram for the AD4001/AD4005 when multiple supplies are available. This configuration is used for best performance because the amplifier supplies can be selected to allow the maximum signal range.

Figure 33 shows a recommended connection diagram when using a single-supply system. This setup is preferable when only a limited number of rails are available in the system and power dissipation is of critical importance.

Figure 34 shows a recommended connection diagram when using a fully differential amplifier.

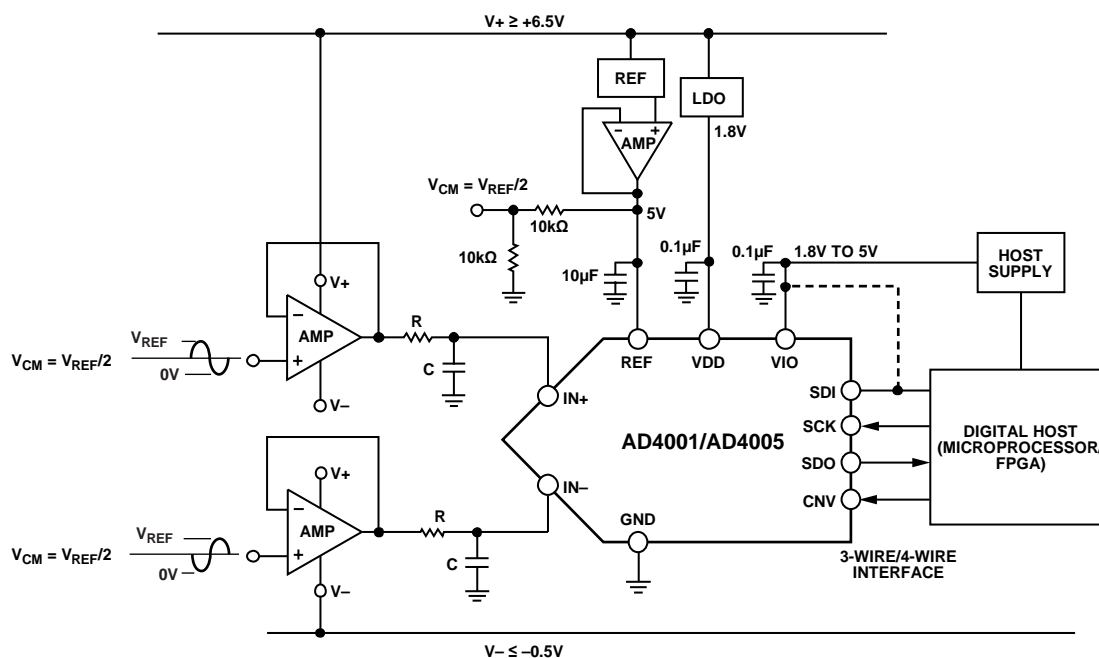
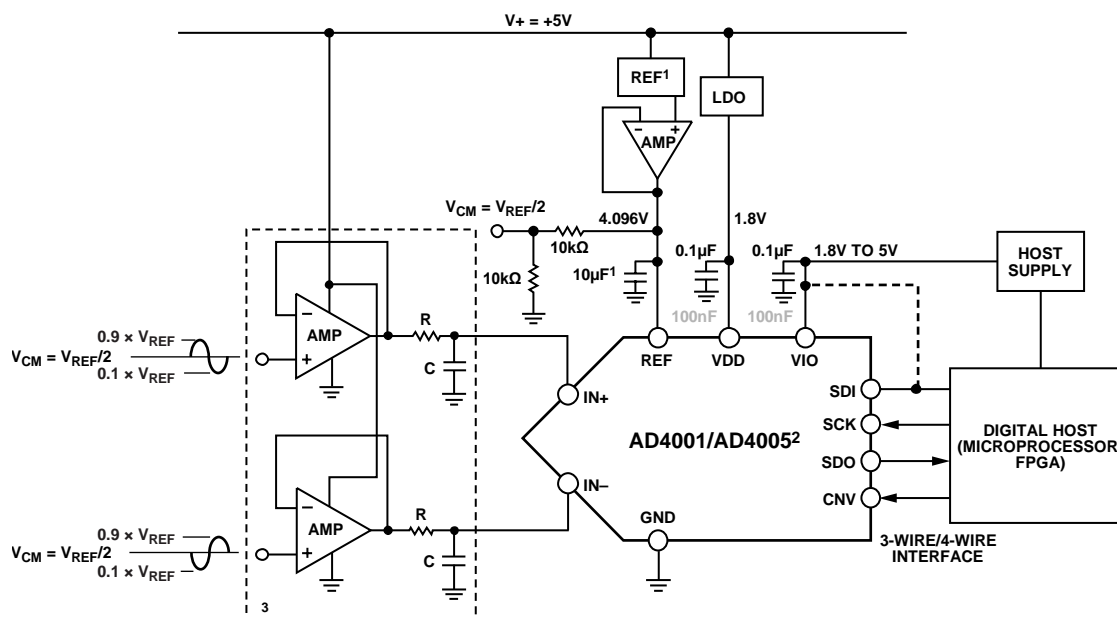


Figure 32. Typical Application Diagram with Multiple Supplies



¹SEE THE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION. C_{REF} IS USUALLY A 10μF CERAMIC CAPACITOR (X7R).

²SPAN COMPRESSION MODE ENABLED.

³SEE TABLE 10 FOR RC FILTER AND AMPLIFIER SELECTION.

Figure 33. Typical Application Diagram with a Single Supply

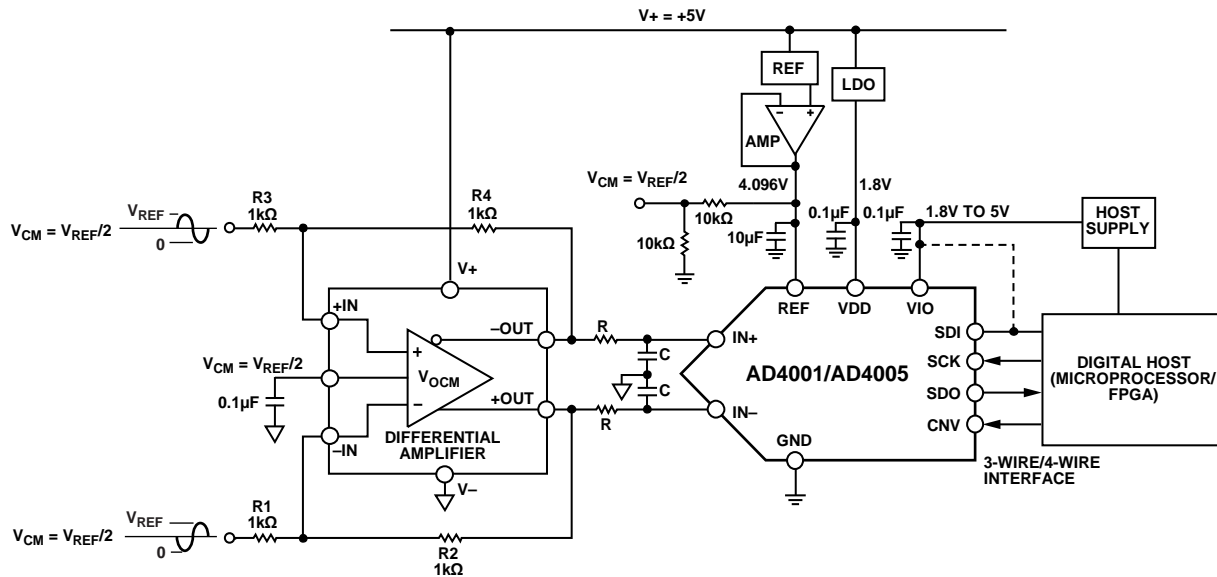


Figure 34. Typical Application Diagram with a Fully Differential Amplifier

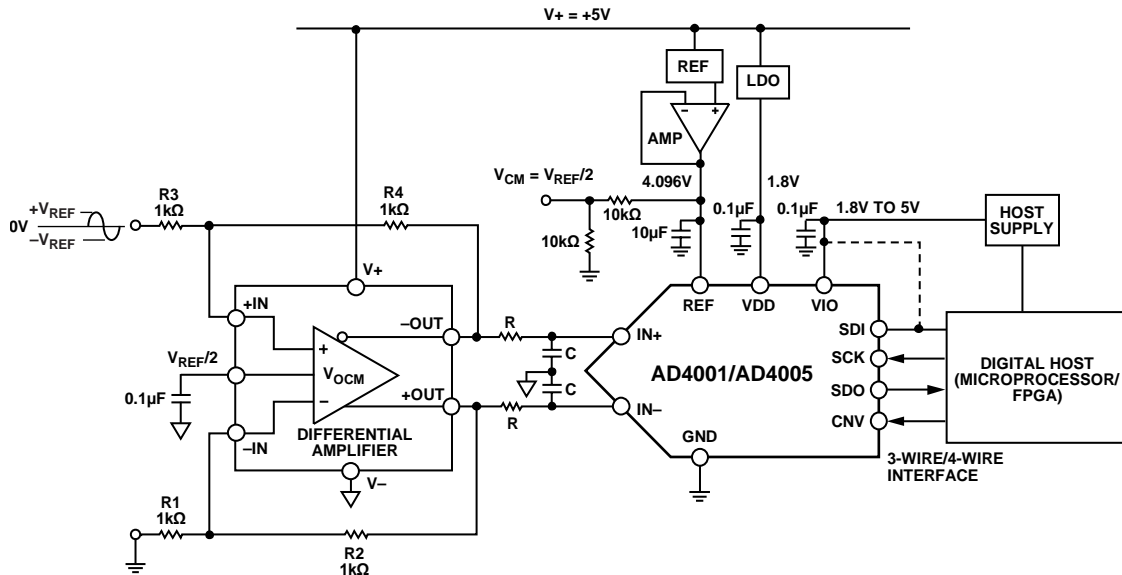


Figure 35. Typical Application Diagram for Single-Ended to Differential Conversion with a Fully Differential Amplifier

ANALOG INPUTS

Figure 36 shows an equivalent circuit of the analog input structure, including the overvoltage clamp of the [AD4001/AD4005](#).

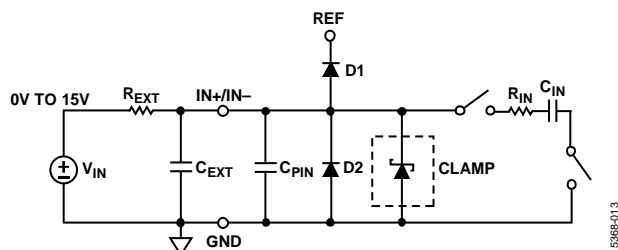


Figure 36. Equivalent Analog Input Circuit

Input Overvoltage Clamp Circuit

Most ADC analog inputs, IN+ and IN-, have no overvoltage protection circuitry apart from ESD protection diodes. During an overvoltage event, an ESD protection diode from an analog input (IN+ or IN-) pin to REF forward biases and shorts the input pin to REF, potentially overloading the reference or causing damage to the device. The [AD4001/AD4005](#) internal overvoltage clamp circuit with a larger external resistor ($R_{EXT} = 200 \Omega$) eliminates the need for external protection diodes and protects the ADC inputs against dc overvoltages.

In applications where the amplifier rails are greater than V_{REF} and less than ground, it is possible for the output to exceed the input voltage range of the device. In this case, the [AD4001/AD4005](#) internal voltage clamp circuit ensures that the voltage on the input pin does not exceed $V_{REF} + 0.4 \text{ V}$ and prevents damage to

the device by clamping the input voltage in a safe operating range and avoiding disturbance of the reference, which is particularly important for systems that share the reference among multiple ADCs.

If the analog input exceeds the reference voltage by 0.4 V, the internal clamp circuit turns on and the current flows through the clamp into ground, preventing the input from rising further and potentially causing damage to the device. The clamp turns on before D1 (see Figure 36) and can sink up to 50 mA of current.

When the clamp is active, it sets the \overline{OV} clamp flag bit in the register that can be read back (see Table 14), which is a sticky bit that must be read to be cleared. The status of the clamp can also be checked in the status bits using an overvoltage clamp flag (see Table 15). The clamp circuit does not dissipate static power in the off state. Note that the clamp cannot sustain the overvoltage condition for an indefinite amount of time.

The external RC filter is usually present at the ADC input to band limit the input signal. During an overvoltage event, excessive voltage is dropped across R_{EXT} , and R_{EXT} becomes part of a protection circuit. The R_{EXT} value can vary from 200 Ω to 20 k Ω for 15 V protection. The C_{EXT} value can be as low as 100 pF for correct operation of the clamp. See Table 1 for input overvoltage clamp specifications.

Differential Input Considerations

The analog input structure allows the sampling of the true differential signal between IN+ and IN-. By using these differential inputs, signals common to both inputs are rejected. Figure 37 shows the common-mode rejection capability of the AD4001/AD4005 over frequency. It is important to note that the differential input signals must be truly antiphase in nature, 180° out of phase, which is required to keep the common-mode voltage of the input signal within the specified range around $V_{REF}/2$ as shown in Table 1.

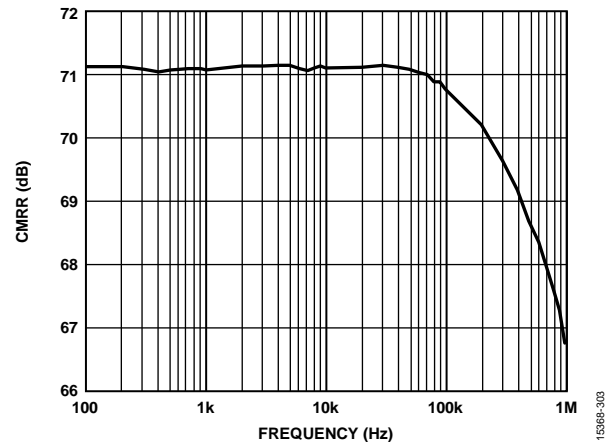


Figure 37. CMRR vs. Frequency, $V_{DD} = 1.8$ V, $V_{IO} = 3.3$ V, $V_{REF} = 5$ V, 25°C

Switched Capacitor Input

During the acquisition phase, the impedance of the analog inputs (IN+ or IN-) can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN} . C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 40 pF and is mainly the ADC sampling capacitor.

During the conversion phase, where the switches are open, the input impedance is limited to C_{PIN} . R_{IN} and C_{IN} make a single-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

RC Filter Values

The RC filter value (represented by R and C in Figure 32 to Figure 35) and driving amplifier can be selected depending on the input signal bandwidth of interest at the full throughput. Lower input signal bandwidth means that the RC cutoff can be lower, thereby reducing noise into the converter. For optimum performance at various throughputs, use the recommended RC values (200 Ω , 180 pF) and the ADA4807-1.

The RC values shown in Table 10 are chosen for ease of drive considerations and greater ADC input protection. The combination of a large R value (200 Ω) and small C value results in a reduced dynamic load for the amplifier to drive. The smaller value of C means fewer stability and phase margin concerns with the amplifier. The large value of R limits the current into the ADC input when the amplifier output exceeds the ADC input range.

Table 10. RC Filter and Amplifier Selection for Various Input Bandwidths

Input Signal Bandwidth (kHz)	R (Ω)	C (pF)	Recommended Amplifier	Recommended Fully Differential Amplifier
<10			See the High-Z Mode section	ADA4940-1
<200	200	180	ADA4807-1	ADA4940-1
>200	200	120	ADA4897-1	ADA4932-1
Multiplexed	200	120	ADA4897-1	ADA4932-1

DRIVER AMPLIFIER CHOICE

Although the AD4001/AD4005 are easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept low enough to preserve the SNR and transition noise performance of the AD4001/AD4005. The noise from the driver is filtered by the single-pole, low-pass filter of the AD4001/AD4005 analog input circuit made by R_{IN} and C_{IN} , or by the external filter, if one is used. Because the typical noise of the AD4001/AD4005 is 54 μV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{54\mu\text{V}}{\sqrt{54\mu\text{V}^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

where:

f_{-3dB} is the input bandwidth, in megahertz, of the AD4001/AD4005 (10 MHz) or the cutoff frequency of the input filter, if one is used.

N is the noise gain of the amplifier (for example, 1 in buffer configuration).

e_N is the equivalent input noise voltage of the op amp in $\text{nV}/\sqrt{\text{Hz}}$.

- For ac applications, the driver must have a THD performance commensurate with the AD4001/AD4005.
- For multichannel multiplexed applications, the driver amplifier and the analog input circuit of the AD4001/AD4005 must settle for a full-scale step onto the capacitor array at a 16-bit level (0.0001525%, 15.25 ppm). In the data sheet of the amplifier, settling at 0.1% to 0.01% is more commonly specified. This settling may differ significantly from the settling time at a 16-bit level and must be verified prior to driver selection.

Single to Differential Driver

For applications using a single-ended analog signal, either bipolar or unipolar, the ADA4940-1 single-ended to differential driver allows a differential input to the device. The schematic is shown in Figure 35.

High Frequency Input Signals

The AD4001/AD4005 ac performance over a wide input frequency range (using a 5 V reference voltage) is shown in Figure 38 and Figure 39. Unlike other traditional SAR ADCs, the AD4001/AD4005 maintain exceptional ac performance for input frequencies up to the Nyquist frequency with minimal performance degradation. Note that the input frequency is limited to the Nyquist frequency of the sample rate in use.

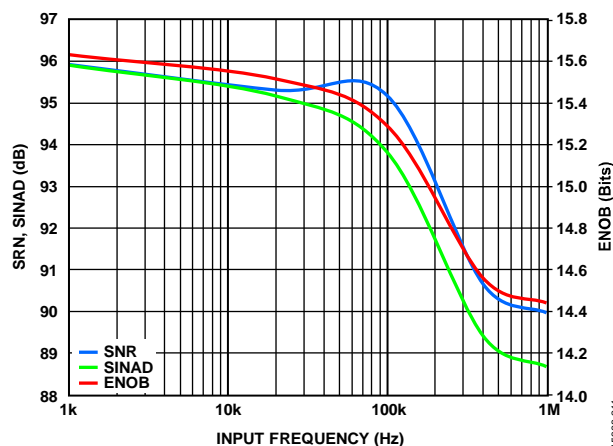


Figure 38. SNR, SINAD, and ENOB vs. Input Frequency, $V_{DD} = 1.8\text{ V}$, $V_{IO} = 3.3\text{ V}$, $V_{REF} = 5\text{ V}$, 25°C

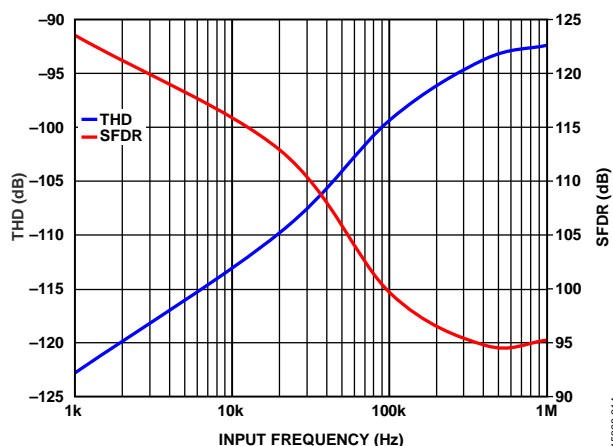


Figure 39. THD and SFDR vs. Input Frequency, $V_{DD} = 1.8\text{ V}$, $V_{IO} = 3.3\text{ V}$, $V_{REF} = 5\text{ V}$, 25°C

Multiplexed Applications

The AD4001/AD4005 significantly reduce system complexity and cost for multiplexed applications that require superior performance in terms of noise, power, and throughput. Figure 40 shows a simplified block diagram of a multiplexed data acquisition system including a multiplexer, an ADC driver, and the precision SAR ADC.

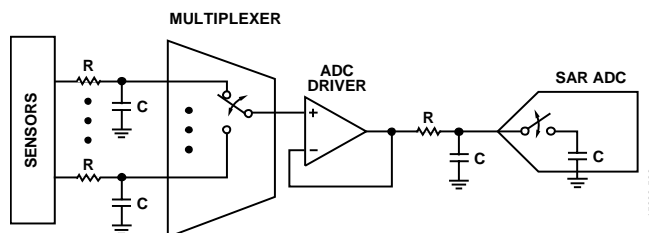


Figure 40. Multiplexed Data Acquisition Signal Chain Using the AD4001/AD4005

Switching multiplexer channels typically results in large voltage steps at the ADC inputs. To ensure an accurate conversion result, the step must be given adequate time to settle before the ADC samples its inputs (on the rising edge of CNV). The settling time error is dependent on the drive circuitry (multiplexer and ADC driver), RC filter values, and the time when the multiplexer

channels are switched. Switch the multiplexer channels immediately after t_{QUIET1} has elapsed from the start of the conversion to maximize settling time while preventing corruption of the conversion result. To avoid conversion corruption, do not switch the channels during the t_{QUIET1} time. If the analog inputs are multiplexed during the quiet conversion time (t_{QUIET1}), the current conversion may be corrupted.

EASE OF DRIVE FEATURES

Input Span Compression

In single-supply applications, it is desirable to use the full range of the ADC; however, the amplifier can have some headroom and footroom requirements, which can be a problem, even if it is a rail-to-rail input and output amplifier. The AD4001/AD4005 include a span compression feature that increases the headroom and footroom available to the amplifier by reducing the input range by 10% from the top and bottom of the range while still accessing all available ADC codes (see Figure 41). The SNR decreases by approximately 1.9 dB ($20 \times \log(8/10)$) for the reduced input range when span compression is enabled. Span compression is disabled by default but can be enabled by writing to the relevant register bit (see the Digital Interface section).

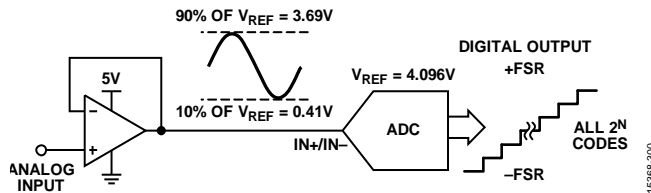


Figure 41. Span Compression

High-Z Mode

The AD4001/AD4005 incorporate high-Z mode, which reduces the nonlinear charge kickback when the capacitor DAC switches back to the input at the start of acquisition. Figure 42 shows the input current of the AD4001/AD4005 with high-Z mode enabled and disabled. The low input current makes the ADC easier to drive than the traditional SAR ADCs available in the market, even with high-Z mode disabled. The input current reduces further to submicroampere range when high-Z mode is enabled. The high-Z mode is disabled by default but can be enabled by writing to the register (see Table 14). Disable high-Z mode for input frequencies above 100 kHz or when multiplexing.

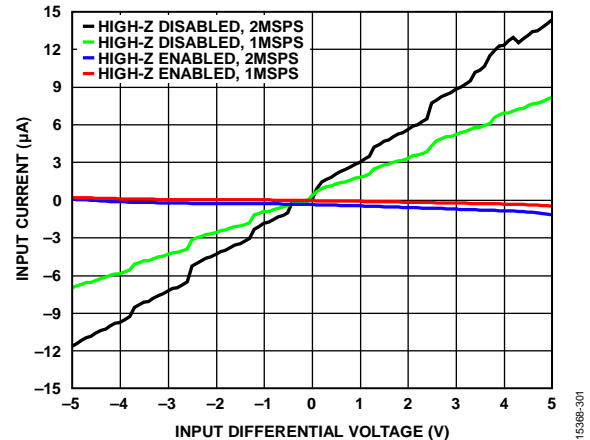


Figure 42. Input Current vs. Input Differential Voltage, $V_{DD} = 1.8 \text{ V}$, $V_{IO} = 3.3 \text{ V}$, $V_{REF} = 5 \text{ V}$, 25°C

To achieve the optimum data sheet performance from high resolution precision SAR ADCs, system designers are often forced to use a dedicated high power, high speed amplifier to drive the traditional switched capacitor SAR ADC inputs for their precision applications, which is commonly encountered in designing a precision data acquisition signal chain. The benefits of high-Z mode are low input current for slow ($<10 \text{ kHz}$) or dc type signals and improved distortion (THD) performance over a frequency range of up to 100 kHz. High-Z mode allows a choice of lower power and lower bandwidth precision amplifiers with a lower RC filter cutoff to drive the ADC, removing the need for dedicated high speed ADC drivers, which saves system power, size, and cost in precision, low bandwidth applications. High-Z mode allows the amplifier and RC filter in front of the ADC to be chosen based on the signal bandwidth of interest and not based on the settling requirements of the switched capacitor SAR ADC inputs.

Additionally, the AD4001/AD4005 can be driven with a much higher source impedance than traditional SARs, which means the resistor in the RC filter can have a value 10 times larger than previous SAR designs and, with high-Z mode enabled, can tolerate even larger impedance. Figure 43 shows the THD performance for various source impedances with high-Z mode disabled and enabled.

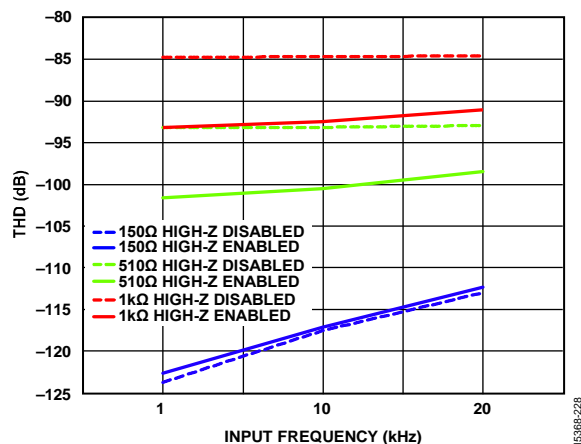


Figure 43. THD vs. Input Frequency for Various Source Impedances, $V_{DD} = 1.8\text{ V}$, $V_{IO} = 3.3\text{ V}$, $V_{REF} = 5\text{ V}$, 25°C

Figure 44 and Figure 45 show the AD4001/AD4005 SNR and THD performance using the ADA4077-1 (supply current per amplifier (I_{SY}) = 400 μA) and ADA4610-1 ($I_{SY} = 1.50\text{ mA}$) precision amplifiers when driving the AD4001/AD4005 at full throughput for high-Z mode enabled and disabled with various RC filter values. These amplifiers achieve 93 dB to 96 dB typical SNR and better than -110 dB THD with high-Z mode enabled. THD is approximately 10 dB better with high-Z mode enabled, even for large R values. SNR maintains close to 96 dB, even with a very low RC bandwidth cutoff.

When high-Z mode is enabled, the ADC consumes approximately 2 mW per MSPS extra power; however, this power is still significantly lower than using dedicated ADC drivers like the ADA4807-1. For any system, the front end usually limits the overall ac/dc performance of the signal chain. It is evident from the data sheets of the selected precision amplifiers, shown in Figure 44 and Figure 45, that their own noise and distortion performance dominates the SNR and THD specification at a certain input frequency.

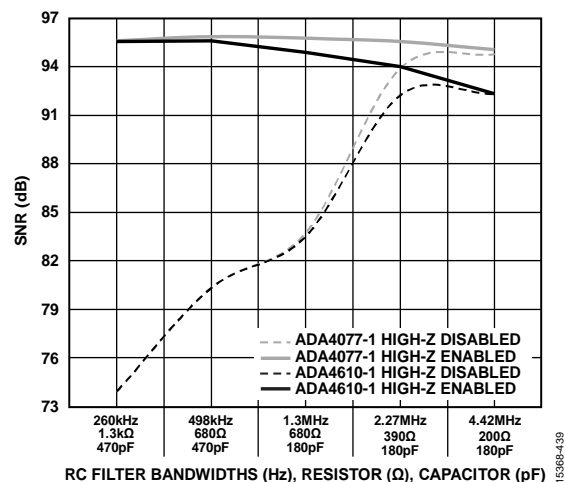


Figure 44. SNR vs. RC Filter Bandwidths for Various Precision ADC Drivers, $f_{IN} = 1\text{ kHz}$ (Turbo Mode On, High-Z Enabled/Disabled), $V_{DD} = 1.8\text{ V}$, $V_{IO} = 3.3\text{ V}$, $V_{REF} = 5\text{ V}$, 25°C

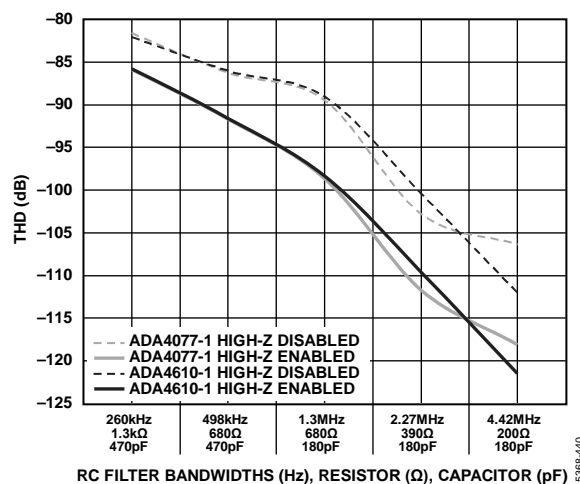


Figure 45. THD vs. RC Filter Bandwidths for Various Precision ADC Drivers, $f_{IN} = 1\text{ kHz}$ (Turbo Mode On, High-Z Enabled/Disabled), $V_{DD} = 1.8\text{ V}$, $V_{IO} = 3.3\text{ V}$, $V_{REF} = 5\text{ V}$, 25°C

Long Acquisition Phase

The AD4001/AD4005 also feature a very fast conversion time of 290 ns, which results in a long acquisition phase. The acquisition is further extended by a key feature of the AD4001/AD4005: the ADC returns to the acquisition phase typically 100 ns before the end of the conversion. This feature provides an even longer time for the ADC to acquire the new input voltage. A longer acquisition phase reduces the settling requirement on the driving amplifier, and a lower power/bandwidth amplifier can be chosen. The longer acquisition phase means that a lower RC filter (represented by R and C in Figure 32 to Figure 35) cutoff can be used, which means a noisier amplifier can also be tolerated. A larger value of R can be used in the RC filter with a corresponding smaller value of C, reducing amplifier stability concerns without affecting distortion performance significantly. A larger value of R also results in reduced dynamic power dissipation in the amplifier.

See Table 10 for details on setting the RC filter bandwidth and choosing a suitable amplifier.

VOLTAGE REFERENCE INPUT

A 10 μF (X7R, 0805 size) ceramic chip capacitor is appropriate for the optimum performance of the reference input.

For higher performance and lower drift, use a reference such as the ADR4550. Use a low power reference such as the ADR3450 at the expense of a slight decrease in the noise performance. It is recommended to use a reference buffer, such as the ADA4807-1, between the reference and the ADC reference input. It is important to consider the optimum capacitance necessary to keep the reference buffer stable as well as to meet the minimum ADC requirement previously stated in this section (that is, a 10 μF ceramic chip capacitor, C_{REF}).

POWER SUPPLY

The AD4001/AD4005 use two power supply pins: a core supply (V_{DD}) and a digital input/output interface supply (V_{IO}). V_{IO} allows direct interface with any logic between 1.8 V and 5.5 V.

To reduce the number of supplies needed, VIO and VDD can be tied together for 1.8 V operation. The ADP7118 low noise, CMOS, low dropout (LDO) linear regulator is recommended to power the VDD and VIO pins. The AD4001/AD4005 are independent of power supply sequencing between VIO and VDD. Additionally, the AD4001/AD4005 are insensitive to power supply variations over a wide frequency range, as shown in Figure 46.

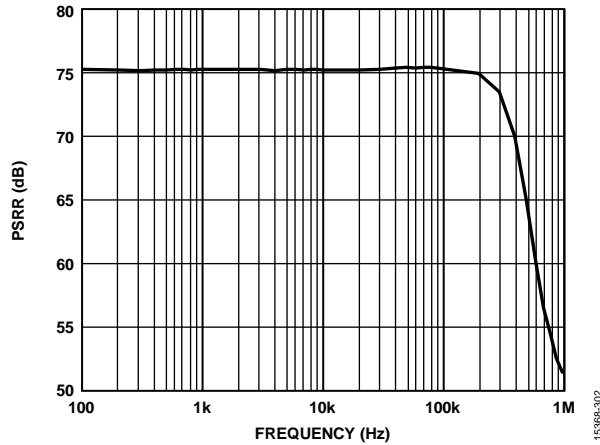


Figure 46. PSRR vs. Frequency, $V_{DD} = 1.8$ V, $V_{IO} = 3.3$ V, $V_{REF} = 5$ V, 25°C

The AD4001/AD4005 power down automatically at the end of each conversion phase; therefore, the power scales linearly with the sampling rate. This feature makes the device ideal for low sampling rates (even a few samples per second) and battery-powered applications. Figure 47 shows the AD4001/AD4005 total power dissipation and individual power dissipation for each rail.

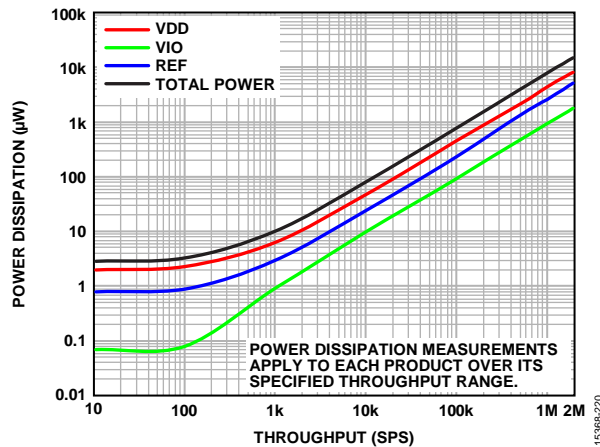


Figure 47. Power Dissipation vs. Throughput, $V_{DD} = 1.8$ V, $V_{IO} = 1.8$ V, $V_{REF} = 5$ V, 25°C

DIGITAL INTERFACE

Although the AD4001/AD4005 have a reduced number of pins, they offer flexibility in their serial interface modes. The AD4001/AD4005 can also be programmed via 16-bit SPI writes to the configuration registers.

When in $\overline{\text{CS}}$ mode, the AD4001/AD4005 are compatible with SPI, QSPI™, MICROWIRE®, digital hosts, and DSPs. In this mode, the AD4001/AD4005 can use either a 3-wire or 4-wire

interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections, which is useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This interface is useful in low jitter sampling or simultaneous sampling applications.

The AD4001/AD4005 provide a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line, similar to a shift register.

The mode in which the device operates depends on the SDI level when the CNV rising edge occurs. $\overline{\text{CS}}$ mode is selected if SDI is high, and daisy-chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, daisy-chain mode is always selected.

In either 3-wire or 4-wire mode, the AD4001/AD4005 offer the option of forcing a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must time out the maximum conversion time prior to readback.

The busy indicator feature is enabled in $\overline{\text{CS}}$ mode if CNV or SDI is low when the ADC conversion ends.

The state of SDO on power-up is either low or high-Z depending on the states of CNV and SDI, as shown in Table 11.

Table 11. State of SDO on Power-Up

CNV	SDI	SDO
0	0	Low
0	1	Low
1	0	Low
1	1	High-Z

The AD4001/AD4005 have turbo mode capability in both 3-wire and 4-wire mode. Turbo mode is enabled by writing to the configuration register and replaces the busy indicator feature when enabled. Turbo mode allows a slower SPI clock rate, making interfacing simpler. The maximum throughput of 2 MSPS for the AD4001 can be achieved only with turbo mode enabled and a minimum SCK rate of 70 MHz.

The SCK rate must be sufficiently fast to ensure the conversion result is clocked out before another conversion initiates. The minimum required SCK rate for an application can be derived based on the sample period (t_{CYC}), the number of bits that must be read (including data and optional status bits), and which digital interface mode is used. Timing diagrams and explanations for each digital interface mode are given in the digital modes of operation sections (see the $\overline{\text{CS}}$ Mode, 3-Wire Turbo Mode section through the Daisy-Chain Mode section).

Status bits can also be clocked out at the end of the conversion data if the status bits are enabled in the configuration register. There are six status bits in total, as described in Table 12.

The AD4001/AD4005 are configured by 16-bit SPI writes to the desired configuration register. The 16-bit word can be written via the SDI line while CNV is held low. The 16-bit word consists of an 8-bit header and 8-bit register data. For isolated systems, the ADuM141D is recommended, which can support the 70 MHz SCK rate required to run the AD4001 at its full throughput of 2 MSPS.

REGISTER READ/WRITE FUNCTIONALITY

The AD4001/AD4005 register bits are programmable, and their default statuses are shown in Table 12. The register map is shown in Table 14. The overvoltage clamp flag (OV) is a read only sticky bit, and it is cleared only if the register is read and the overvoltage condition is no longer present. It gives an indication of overvoltage condition when it is set to 0.

Table 12. Register Bits

Register Bits	Default Status
Overvoltage (OV) Clamp Flag	1 bit, 1 = inactive (default)
Span Compression	1 bit, 0 = disabled (default)
High-Z Mode	1 bit, 0 = disabled (default)
Turbo Mode	1 bit, 0 = disabled (default)
Enable Six Status Bits	1 bit, 0 = disabled (default)

All access to the register map must start with a write to the 8-bit command register in the SPI interface block. The AD4001/AD4005 ignore all 1s until the first 0 is clocked in; the value loaded into the command register is always a 0 followed by seven command bits. This command determines whether that operation is a write or a read. The AD4001/AD4005 command register is shown in Table 13.

Table 14. Register Map

ADDR[1:0]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
0x0	Reserved	Reserved	Reserved	Enable six status bits	Span compression	High-Z mode	Turbo mode	Overvoltage (OV) clamp flag (read only sticky bit)	0xE1

Table 13. Command Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WEN	R/W	0	1	0	1	0	0

All register read/writes must occur while CNV is low. Data on SDI is clocked in on the rising edge of SCK. Data on SDO is clocked out on the falling edge of SCK. At the end of the data transfer, SDO is put in a high impedance state on the rising edge of CNV if daisy-chain mode is not enabled. If daisy-chain mode is enabled, SDO goes low on the rising edge of CNV. Register reads are not allowed in daisy-chain mode.

A register write requires three signal lines: SCK, CNV, and SDI. During a register write, to read the current conversion results on SDO, the CNV pin must be brought low after the conversion is completed; otherwise, the conversion results may be incorrect on SDO. However, the register write occurs regardless.

The LSB of each configuration register is reserved because a user reading 16-bit conversion data may be limited to a 16-bit SPI frame. The state of SDI on the last bit in the SDI frame may be the state that then persists when CNV rises. Because interface mode is partly set based on the SDI state when CNV rises, in this scenario, the user may need to set the final SDI state.

The timing diagrams in Figure 48 through Figure 50 show how data is read and written when the AD4001/AD4005 are configured in register read, write, and daisy-chain mode.

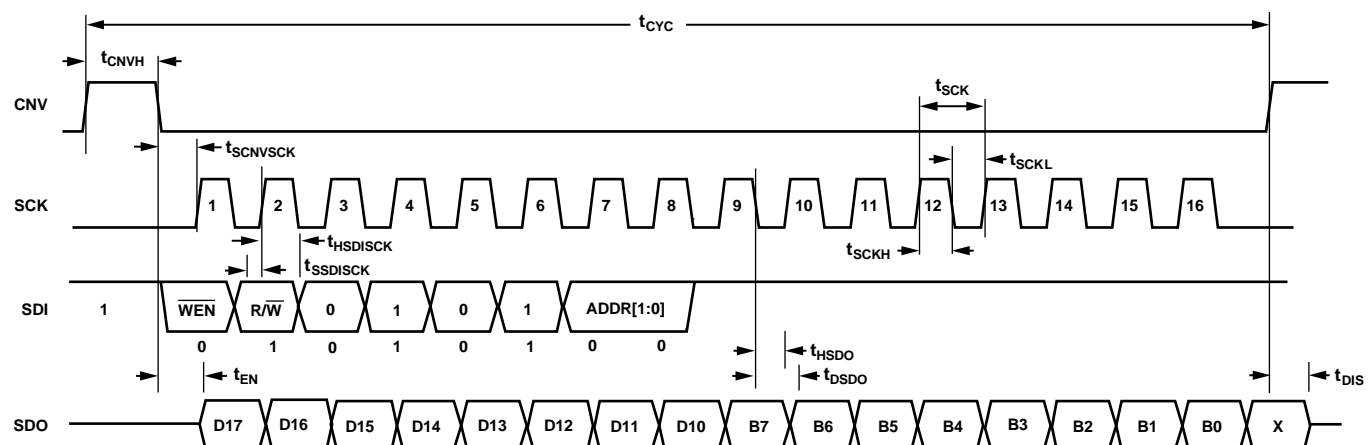
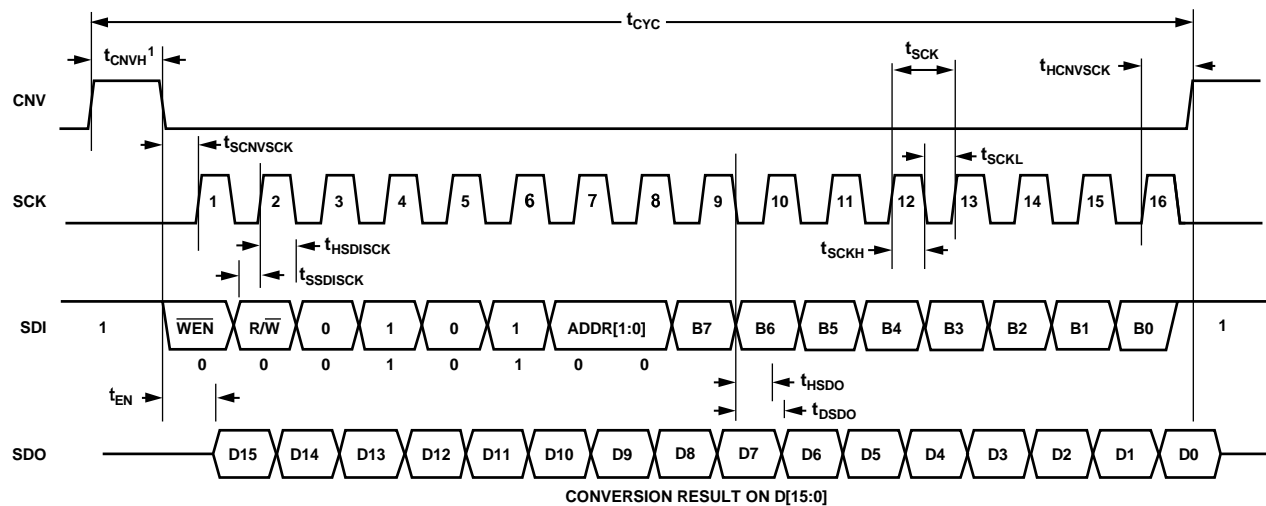


Figure 48. Register Read Timing Diagram (X Means Don't Care)



¹THE USER MUST WAIT t_{CONV} WHEN READING BACK THE CONVERSION RESULT AND PERFORMING A REGISTER WRITE AT THE SAME TIME.

Figure 49. Register Write Timing Diagram

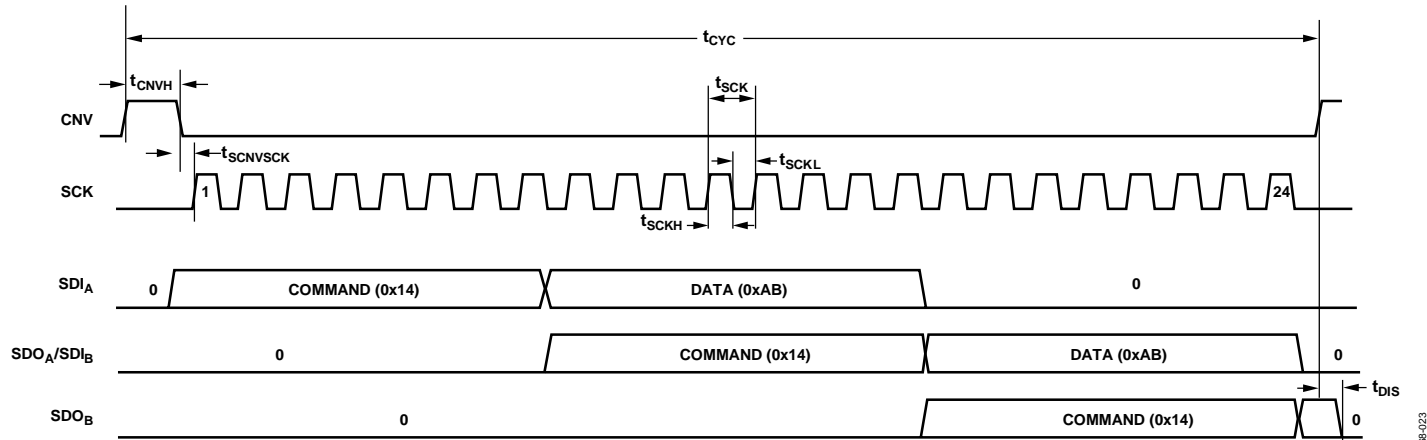


Figure 50. Register Write Timing Diagram, Daisy-Chain Mode

STATUS WORD

The 6-bit status word can be appended to the end of a conversion result, and the default conditions of these bits are shown in Table 15. The status bits must be enabled in the register setting. When the overvoltage clamp flag (\overline{OV}) is a 0, it indicates an overvoltage condition. The overvoltage clamp flag status bit updates on a per conversion basis.

The SDO line goes to high-Z after the sixth status bit is clocked out (except in daisy-chain mode). The user is not required to clock out all status bits to start the next conversion. The serial interface timing for \overline{CS} mode, 3-wire without busy indicator, including status bits, is shown in Figure 51.

Table 15. Status Bits (Default Conditions)

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Overvoltage (\overline{OV}) clamp flag	Span compression	High-Z mode	Turbo mode	Reserved	Reserved

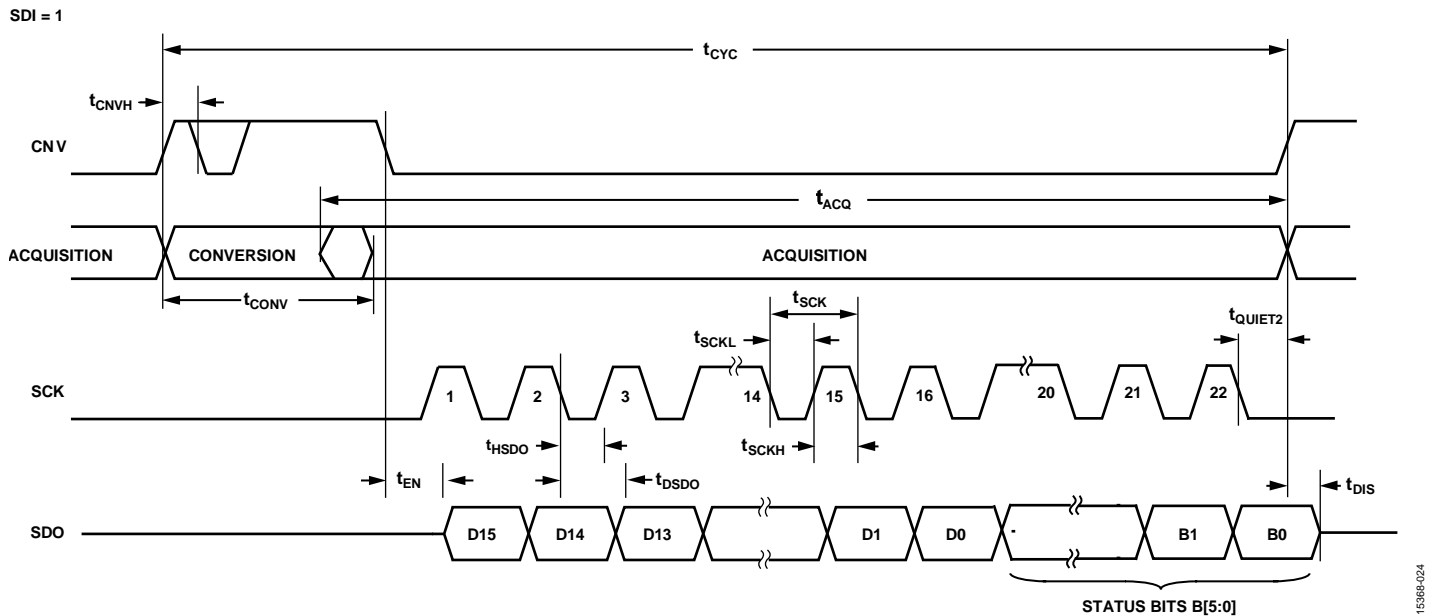


Figure 51. \overline{CS} Mode, 3-Wire Without Busy Indicator Serial Interface Timing Diagram, Including Status Bits (SDI High)

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$\overline{\text{CS}}$ MODE, 3-WIRE TURBO MODE

This mode is typically used when a single AD4001/AD4005 device is connected to an SPI-compatible digital host. It provides additional time during the end of the ADC conversion process to clock out the previous conversion result, providing a lower SCK rate. The AD4001 can achieve a throughput rate of 2 MSPS only when turbo mode is enabled and using a minimum SCK rate of 70 MHz. With turbo mode enabled, the AD4005 can also achieve its maximum throughput rate of 1 MSPS with a minimum SCK rate of 22 MHz. The connection diagram is shown in Figure 52, and the corresponding timing diagram is shown in Figure 53.

This mode replaces the 3-wire with busy indicator mode by programming the turbo mode bit, Bit 1 (see Table 14).

When SDI is forced high, a rising edge on CNV initiates a conversion. The previous conversion data is available to read after the CNV rising edge. The user must wait t_{QUIET1} time after CNV is brought high before bringing CNV low to clock out the previous conversion result. The user must also wait t_{QUIET2} time after the last falling edge of SCK to when CNV is brought high.

When the conversion is complete, the AD4001/AD4005 enter the acquisition phase and power down. When CNV goes low, the MSB is output to SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

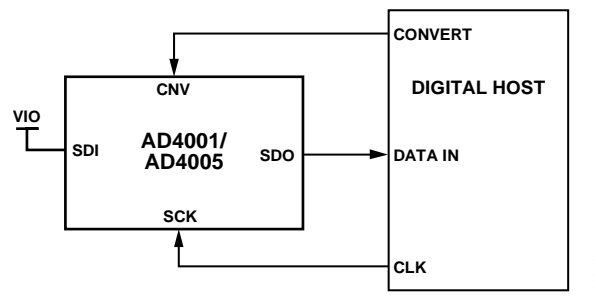


Figure 52. $\overline{\text{CS}}$ Mode, 3-Wire Turbo Mode Connection Diagram (SDI High)

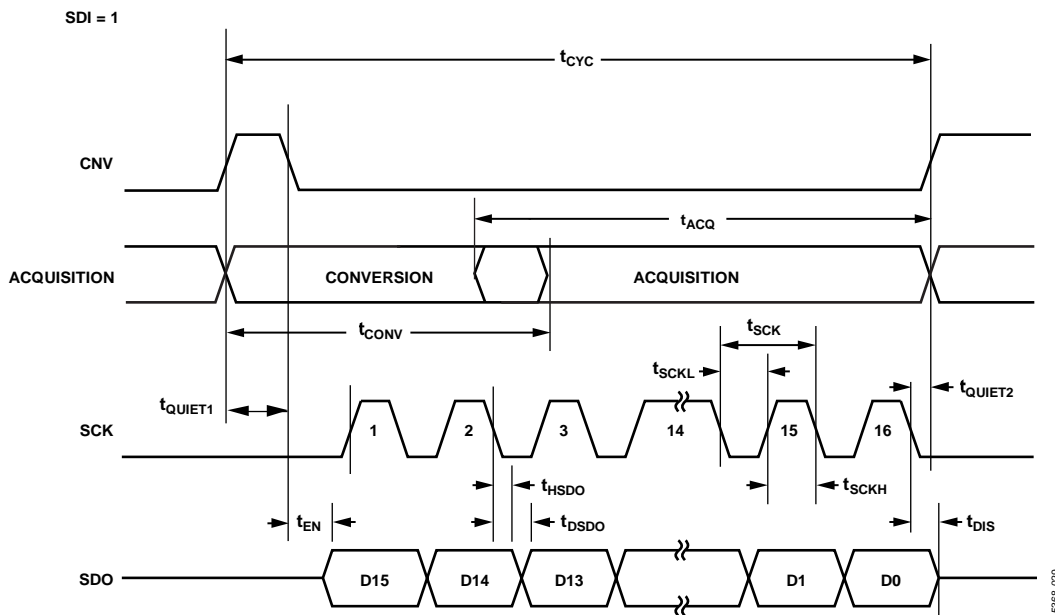


Figure 53. $\overline{\text{CS}}$ Mode, 3-Wire Turbo Mode Serial Interface Timing Diagram (SDI High)

$\overline{\text{CS}}$ MODE, 3-WIRE WITHOUT BUSY INDICATOR

This mode is typically used when a single AD4001/AD4005 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 54, and the corresponding timing diagram is shown in Figure 55.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{\text{CS}}$ mode, and forces SDO to high impedance. After a conversion is initiated, it continues until completion irrespective of the state of CNV. This feature can be useful, for instance, to bring CNV low to select other SPI devices, such as analog multiplexers; however, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the AD4001/AD4005 enter the acquisition phase and power down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

There must not be any digital activity on SCK during the conversion.

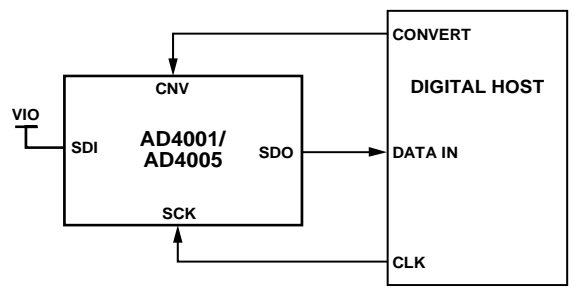


Figure 54. $\overline{\text{CS}}$ Mode, 3-Wire Without Busy Indicator Connection Diagram (SDI High)

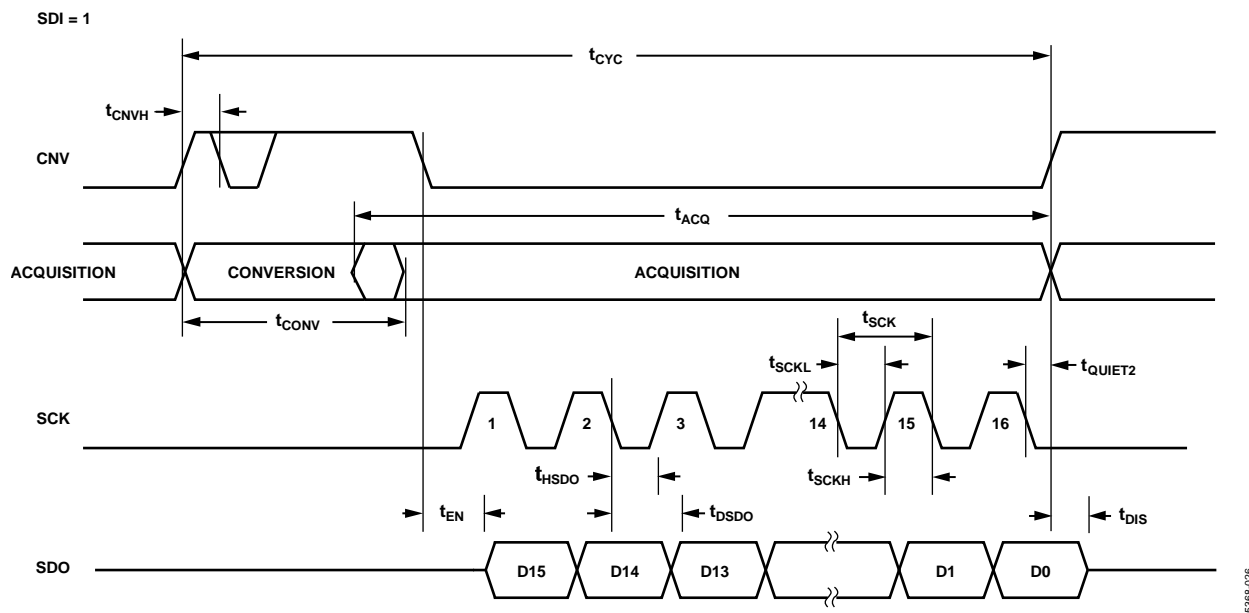


Figure 55. $\overline{\text{CS}}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing Diagram (SDI High)

$\overline{\text{CS}}$ MODE, 3-WIRE WITH BUSY INDICATOR

This mode is typically used when a single AD4001/AD4005 is connected to an SPI-compatible digital host with an interrupt input ($\overline{\text{IRQ}}$).

The connection diagram is shown in Figure 56, and the corresponding timing diagram is shown in Figure 57.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{\text{CS}}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can select other SPI devices, such as analog multiplexers; however, CNV must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up resistor of 1 k Ω on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD4001/AD4005 then enter the acquisition phase and power down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If multiple AD4001/AD4005 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

There must not be any digital activity on the SCK during the conversion.

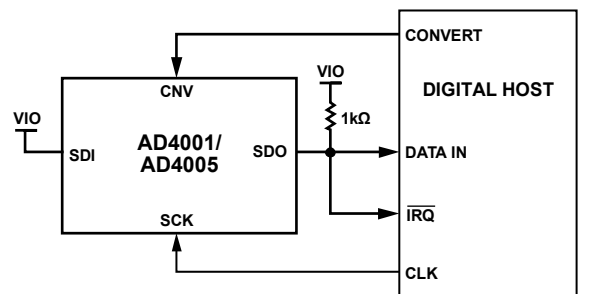


Figure 56. $\overline{\text{CS}}$ Mode, 3-Wire with Busy Indicator Connection Diagram (SDI High)

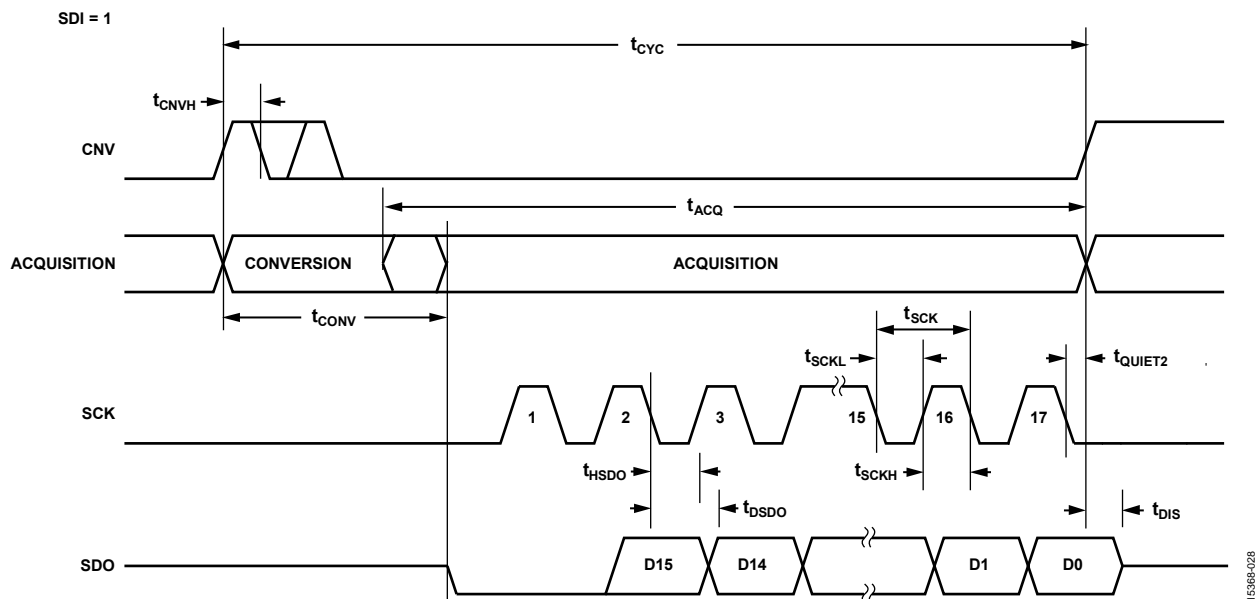


Figure 57. $\overline{\text{CS}}$ Mode, 3-Wire with Busy Indicator Serial Interface Timing Diagram (SDI High)

$\overline{\text{CS}}$ MODE, 4-WIRE TURBO MODE

This mode is typically used when a single AD4001/AD4005 device is connected to an SPI-compatible digital host. It provides additional time during the end of the ADC conversion process to clock out the previous conversion result, giving a lower SCK rate. The AD4001 can achieve a throughput rate of 2 MSPS only when turbo mode is enabled and using a minimum SCK rate of 70 MHz. With turbo mode enabled, the AD4005 can also achieve its maximum throughput rate of 1 MSPS with a minimum SCK rate of 22 MHz. The connection diagram is shown in Figure 58, and the corresponding timing diagram is shown in Figure 59.

This mode replaces the 4-wire with busy indicator mode by programming the turbo mode bit, Bit 1 (see Table 14).

With SDI high, a rising edge on CNV initiates a conversion. The previous conversion data is available to read after the CNV

rising edge. The user must wait t_{QUIET1} time after CNV is brought high before bringing SDI low to clock out the previous conversion result. The user must also wait t_{QUIET2} time after the last falling edge of SCK to when CNV is brought high.

When the conversion is complete, the AD4001/AD4005 enter the acquisition phase and power down. The ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance.

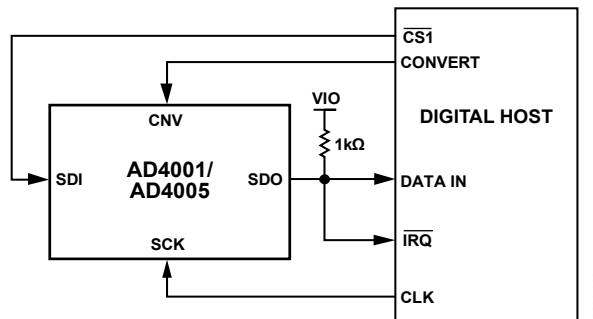


Figure 58. $\overline{\text{CS}}$ Mode, 4-Wire Turbo Mode Connection Diagram

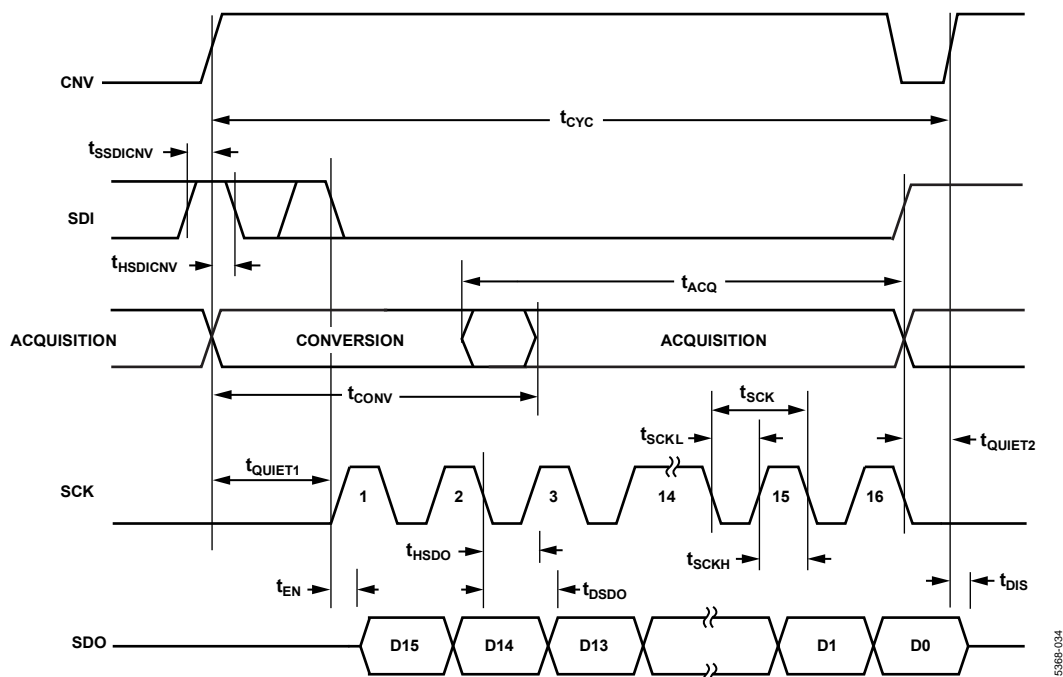


Figure 59. $\overline{\text{CS}}$ Mode, 4-Wire Turbo Mode Timing Diagram

$\overline{\text{CS}}$ MODE, 4-WIRE WITHOUT BUSY INDICATOR

This mode is typically used when multiple AD4001/AD4005 devices are connected to an SPI-compatible digital host.

A connection diagram example using two AD4001/AD4005 devices is shown in Figure 60, and the corresponding timing diagram is shown in Figure 61.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{\text{CS}}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI and CNV are low, SDO is driven low. Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers; however, SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the AD4001/AD4005 enter the acquisition phase and power down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance and another AD4001/AD4005 can be read.

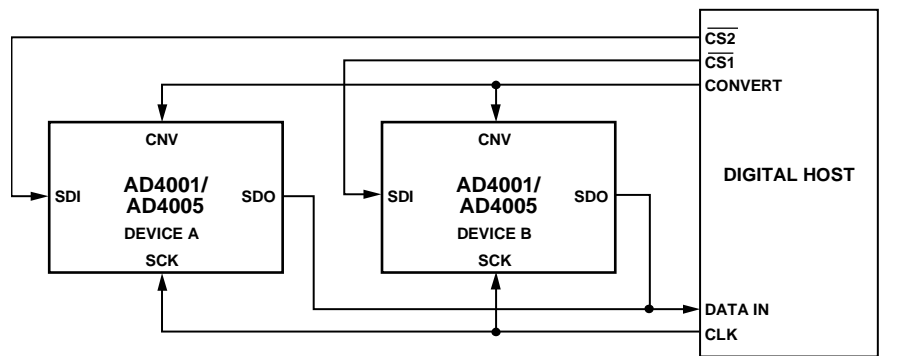


Figure 60. $\overline{\text{CS}}$ Mode, 4-Wire Without Busy Indicator Connection Diagram

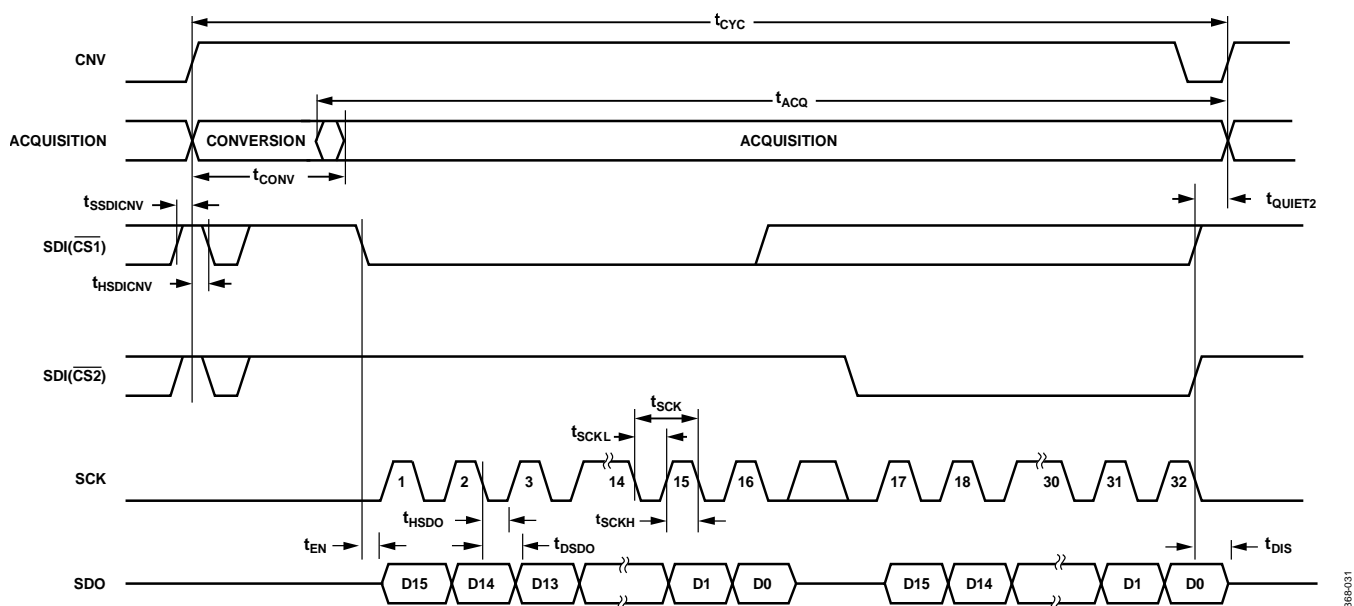


Figure 61. $\overline{\text{CS}}$ Mode, 4-Wire Without Busy Indicator Serial Interface Timing Diagram

$\overline{\text{CS}}$ MODE, 4-WIRE WITH BUSY INDICATOR

This mode is typically used when a [AD4001/AD4005](#) device is connected to an SPI-compatible digital host with an interrupt input ($\overline{\text{IRQ}}$), and when it is desired to keep CNV , which samples the analog input, independent of the signal used to select the data reading. This independence is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 62, and the corresponding timing diagram is shown in Figure 63.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{\text{CS}}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI and CNV are low, SDO is driven low. Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers; however,

SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up resistor of 1 k Ω on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The [AD4001/AD4005](#) then enter the acquisition phase and power down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance.

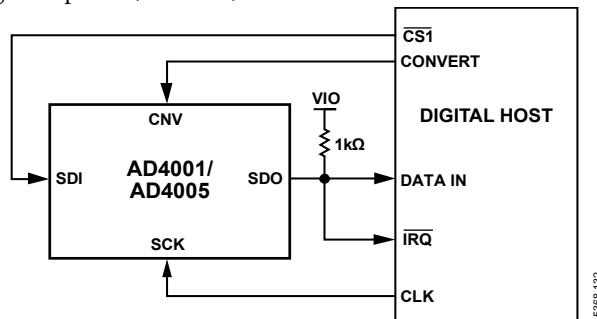


Figure 62. $\overline{\text{CS}}$ Mode, 4-Wire with Busy Indicator Connection Diagram

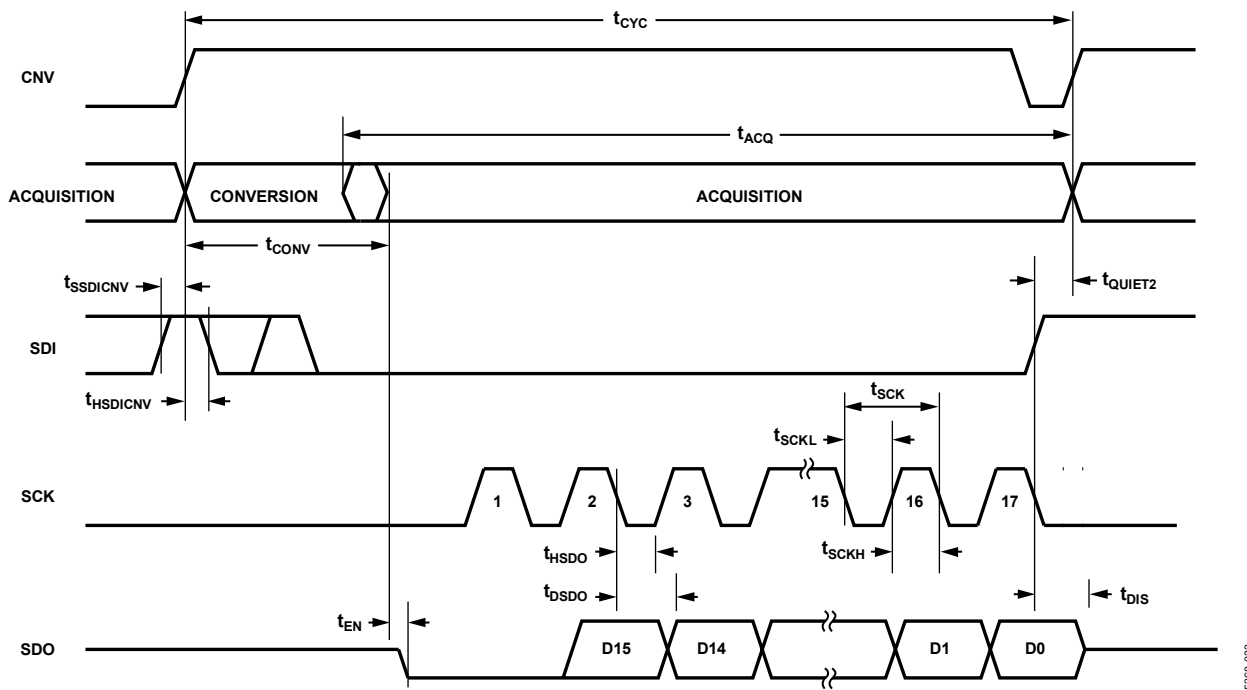


Figure 63. $\overline{\text{CS}}$ Mode, 4-Wire with Busy Indicator Serial Interface Timing Diagram

DAISY-CHAIN MODE

Use this mode to daisy-chain multiple AD4001/AD4005 devices on a 3-wire or 4-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD4001/AD4005 devices is shown in Figure 64, and the corresponding timing diagram is shown in Figure 65.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects daisy-chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO, and the AD4001/AD4005 enter the acquisition phase and power down. The remaining data bits stored in the internal shift register are clocked out of SDO by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK rising edges. Each ADC in

the daisy-chain outputs its data MSB first, and $16 \times N$ clocks are required to read back the N ADCs. The data is valid on both SCK edges. The maximum conversion rate is reduced because of the total readback time.

It is possible to write to each ADC register in daisy-chain mode. The timing diagram is shown in Figure 50. This mode requires 4-wire operation because data is clocked in on the SDI line with CNV held low. The same command byte and register data can be shifted through the entire chain to program all ADCs in the chain with the same register contents, which requires $8 \times (N + 1)$ clocks for N ADCs. It is possible to write different register contents to each ADC in the chain by writing to the furthest ADC in the chain, first using $8 \times (N + 1)$ clocks, and then the second furthest ADC with $8 \times N$ clocks, and so forth until reaching the nearest ADC in the chain, which requires 16 clocks for the command and register data. It is not possible to read register contents in daisy-chain mode; however, the six status bits can be enabled if the user wants to determine the ADC configuration. Note that enabling the status bits requires six extra clocks to clock out the ADC result and the status bits per ADC in the chain. Turbo mode cannot be used in daisy-chain mode.

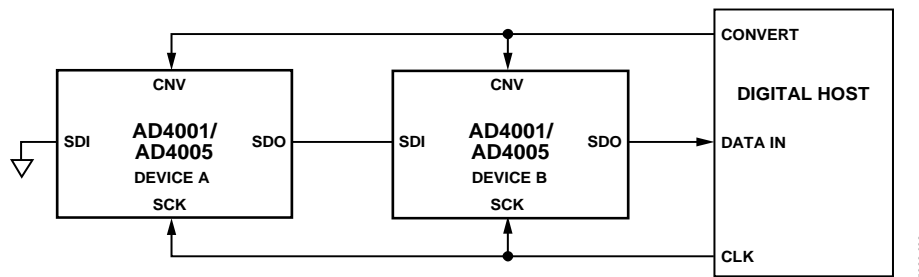


Figure 64. Daisy-Chain Mode Connection Diagram

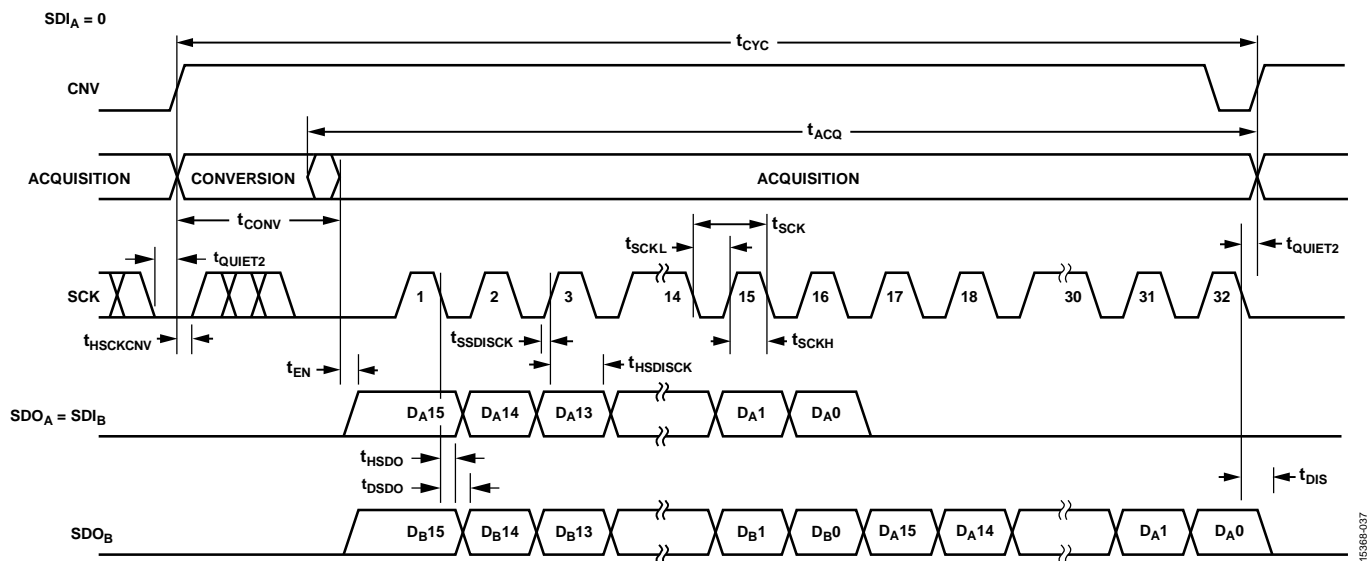


Figure 65. Daisy-Chain Mode Serial Interface Timing Diagram

LAYOUT GUIDELINES

The PCB that houses the [AD4001/AD4005](#) must be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the [AD4001/AD4005](#), with its analog signals on the left side and its digital signals on the right side, eases this task.

Avoid running digital lines under the device because they couple noise onto the die, unless a ground plane under the [AD4001/AD4005](#) is used as a shield. Fast switching signals, such as CNV or clocks, must not run near analog signal paths. Avoid crossover of digital and analog signals.

At least one ground plane must be used. It can be common or split between the digital and analog sections. In the latter case, join the planes underneath the [AD4001/AD4005](#) devices.

The [AD4001/AD4005](#) voltage reference input (REF) has a dynamic input impedance. Decouple the REF pin with minimal parasitic inductances by placing the reference decoupling ceramic capacitor close to (ideally right up against) the REF and GND pins and connect them with wide, low impedance traces.

Finally, decouple the VDD and VIO power supplies of the [AD4001/AD4005](#) with ceramic capacitors, typically 0.1 μ F, placed close to the [AD4001/AD4005](#) and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of the [AD4001](#) layout following these rules is shown in Figure 66 and Figure 67. Note that the [AD4005](#) layout is equivalent to the [AD4001](#) layout.

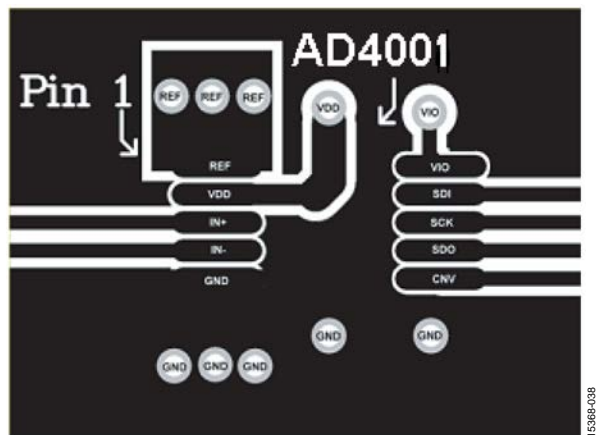


Figure 66. Example Layout of the [AD4001](#) (Top Layer)

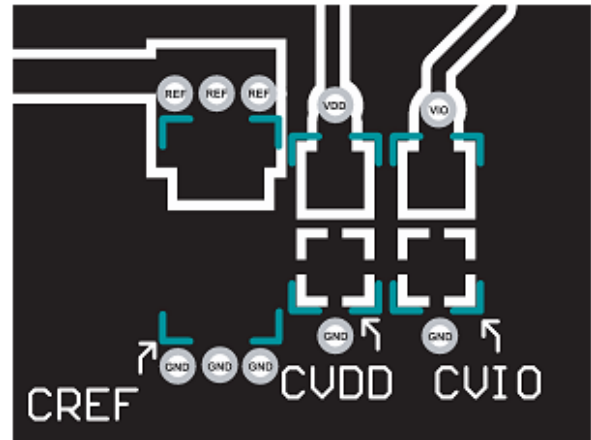


Figure 67. Example Layout of the [AD4001](#) (Bottom Layer)

EVALUATING THE [AD4001/AD4005](#) PERFORMANCE

Other recommended layouts for the [AD4001/AD4005](#) are outlined in the user guide of the evaluation board for the [AD4001](#) ([EVAL-AD4001FMCZ](#)). The evaluation board package includes a fully assembled and tested evaluation board with the [AD4001](#) documentation, and software for controlling the board from a PC via the [EVAL-SDP-CH1Z](#). The [EVAL-AD4001FMCZ](#) can also be used to evaluate the [AD4005](#) by limiting the throughput to 1 MSPS in its software (see [UG-1042](#)).

OUTLINE DIMENSIONS

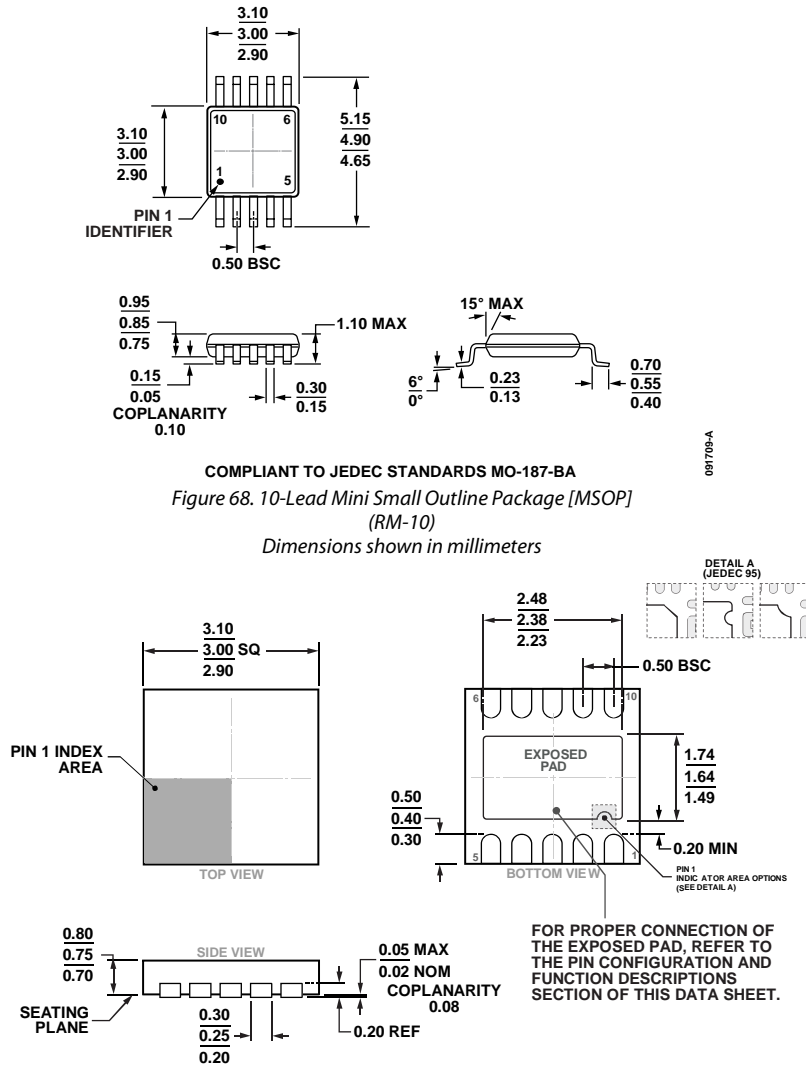


Figure 69. 10-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm × 3 mm Body and 0.75 mm Package Height (CP-10-9)

Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1, 2}	Integral Nonlinearity (INL)	Temperature Range	Package Description	Ordering Quantity	Package Option	Branding
AD4001BCPZ-RL7	±0.4 LSB	−40°C to +125°C	10-Lead LFCSP, Reel	1500	CP-10-9	C8H
AD4001BRMZ	±0.4 LSB	−40°C to +125°C	10-Lead MSOP, Tube	50	RM-10	C8H
AD4001BRMZ-RL7	±0.4 LSB	−40°C to +125°C	10-Lead MSOP, Reel	1000	RM-10	C8H
AD4005BCPZ-RL7	±0.4 LSB	−40°C to +125°C	10-Lead LFCSP, Reel	1500	CP-10-9	C8T
AD4005BRMZ	±0.4 LSB	−40°C to +125°C	10-Lead MSOP, Tube	50	RM-10	C8T
AD4005BRMZ-RL7	±0.4 LSB	−40°C to +125°C	10-Lead MSOP, Reel	1000	RM-10	C8T
EVAL-AD4001FMCZ			AD4001 Evaluation Board Compatible with EVAL-SDP-CH1Z			

¹ Z = RoHS Compliant Part.

² The EVAL-AD4001FMCZ can also be used to evaluate the AD4005 by setting the throughput to 1 MSPS in its software (see UG-1042).