

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC595AP, TC74HC595AF

8-Bit Shift Register/Latch (3-state)

The TC74HC595A is a high speed 8-BIT SHIFT REGISTER/LATCH fabricated with silicon gate C²MOS technology.

It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC595A contains an 8-bit static shift register which feeds an 8-bit storage register.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation.

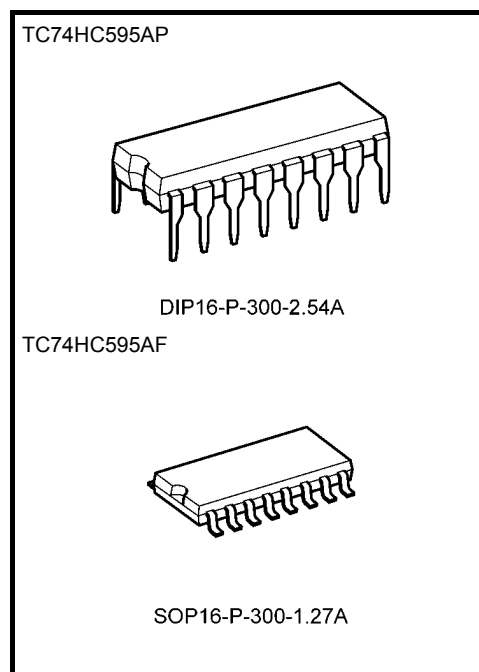
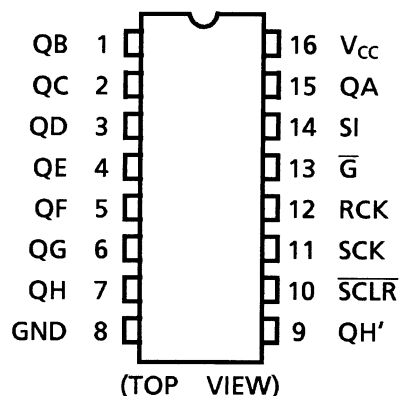
And, since the parallel outputs are 3-state, it can be directly connected to 8-bit bus. This register can be used in serial-to-parallel conversion, data receivers, etc.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $f_{max} = 55$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ$ C
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Output drive capability: 15 LSTTL loads for QA to QH
10 LSTTL loads for QH'
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 6$ mA (min)
For QA to QH
 $|I_{OH}| = I_{OL} = 4$ mA (min)
For QH'
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS595

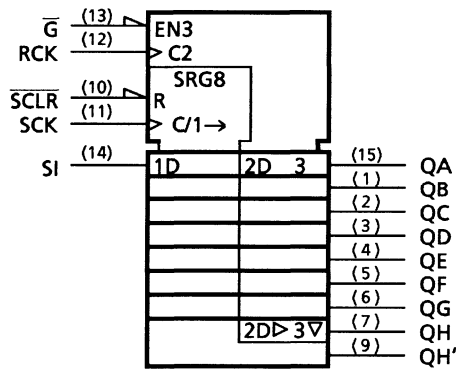
Pin Assignment



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

Start of commercial production
1986-05

IEC Logic Symbol

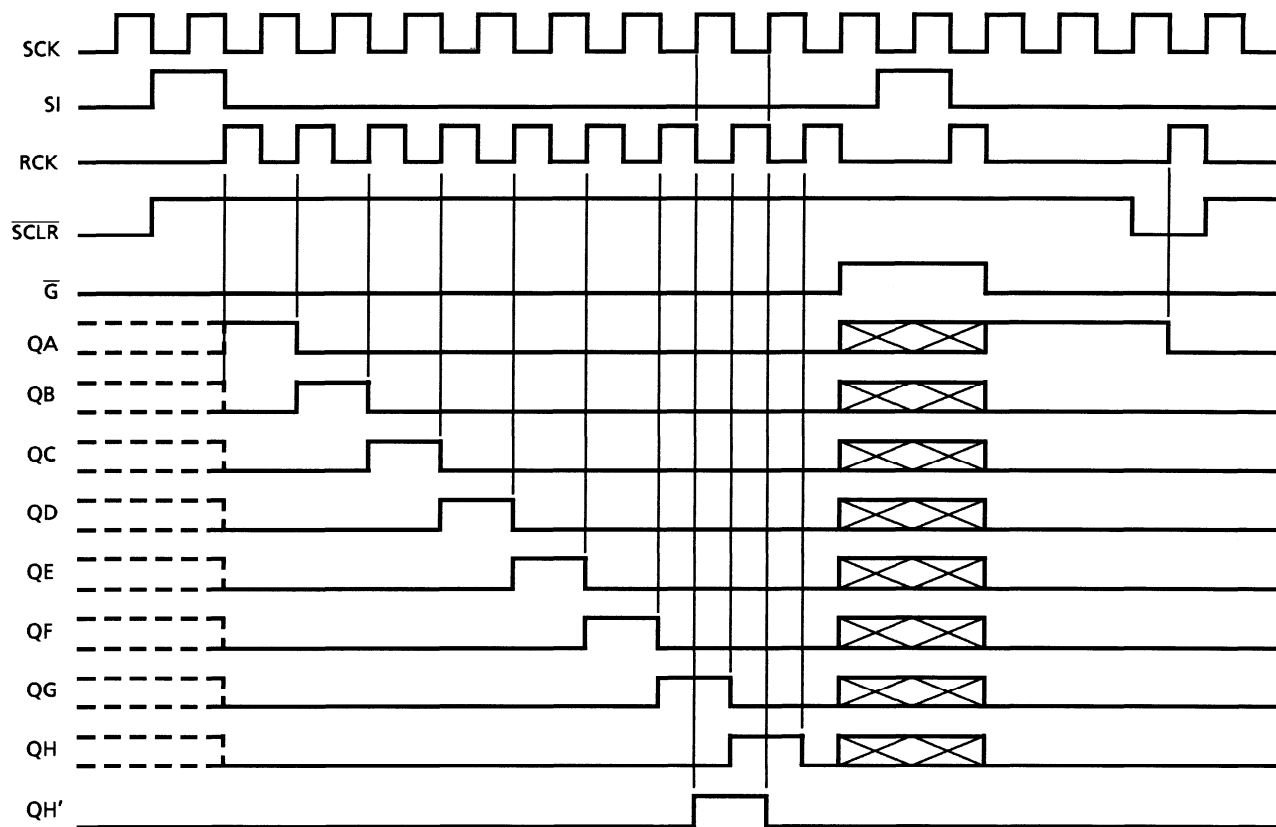


Truth Table

Inputs					Function
SI	SCK	SCLR	RCK	G-bar	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L		H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H		H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X		H	X	X	State of S.R. is not changed.
X	X	X		X	S.R. data is stored into storage register.
X	X	X		X	Storage register stage is not changed.

X: Don't care

Timing Chart



Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	−0.5 to 7	V
DC input voltage	V _{IN}	−0.5 to V _{CC} + 0.5	V
DC output voltage	V _{OUT}	−0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	I _{OK}	±20	mA
DC output current (QH') (QA to QH)	I _{OUT}	±25 ±35	mA
DC V _{CC} /ground current	I _{CC}	±75	mA
Power dissipation	P _D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T _{stg}	−65 to 150	°C

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of $-10\text{ mW}/^\circ\text{C}$ shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics
DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit			
				V _{CC} (V)	Min	Typ.	Max	Min		Max		
High-level input voltage	V _{IH}	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	V			
Low-level input voltage	V _{IL}	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	V			
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = −20 μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	V			
				QH'	I _{OH} = −4 mA I _{OH} = −5.2 mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	V	
					QA to QH	I _{OH} = −6 mA I _{OH} = −7.8 mA	4.5 6.0	4.18 5.68	4.31 5.80	— —		4.13 5.63
		V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA		2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V	
					QH'	I _{OL} = 4 mA I _{OL} = 5.2 mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	V
						QA to QH	I _{OL} = 6 mA I _{OL} = 7.8 mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		6.0	—		—	±0.5	—	±5.0	μA	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA		
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	4.0	—	40.0	μA		

Timing Requirements (input: $t_r = t_f = 6\text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Limit	Unit
			V _{CC} (V)	Typ.			
Minimum pulse width (SCK, RCK)	t_W (H) t_W (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{\text{SCLR}}$)	t_W (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (SI-SCK)	t_s	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Minimum set-up time (SCK-RCK)	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ($\overline{\text{SCLR}}$ -RCK)	t_s	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ($\overline{\text{SCLR}}$)	t_{rem}	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	30	25	
			6.0	—	35	28	

AC Characteristics ($C_L = 15\text{ pF}$, $V_{CC} = 5\text{ V}$, Ta = 25°C, input: $t_r = t_f = 6\text{ ns}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time (QH')	t_{TLH}	—	—	4	8	ns
	t_{THL}					
Propagation delay time (SCK-QH')	t_{PLH}	—	—	12	21	ns
	t_{PHL}					
Propagation delay time ($\overline{\text{SCLR}}$ -QH')	t_{PHL}	—	—	15	30	ns
Maximum clock frequency	f_{max}	—	35	77	—	MHz

AC Characteristics (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			CL (pF)	V _{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time (Q _n)	t_{TLH} t_{THL}	—	50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output transition time (QH')	t_{TLH} t_{THL}	—	50	2.0	—	30	75	—	95	ns
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation delay time (SCK-QH')	t_{pLH} t_{pHL}	—	50	2.0	—	45	125	—	155	ns
				4.5	—	15	25	—	31	
				6.0	—	13	21	—	26	
Propagation delay time ($\overline{\text{SCLR}}$ -QH')	t_{pHL}	—	50	2.0	—	60	175	—	220	ns
				4.5	—	18	35	—	44	
				6.0	—	15	30	—	37	
Propagation delay time (RCK-Q _n)	t_{pLH} t_{pHL}	—	50	2.0	—	60	150	—	190	ns
				4.5	—	20	30	—	38	
				6.0	—	17	26	—	32	
			150	2.0	—	75	190	—	240	
				4.5	—	25	38	—	48	
				6.0	—	22	32	—	41	
Output enable time	t_{pZL} t_{pZH}	$R_L = 1 \text{ k}\Omega$	50	2.0	—	45	135	—	170	ns
				4.5	—	15	27	—	34	
				6.0	—	13	23	—	29	
			150	2.0	—	60	175	—	220	
				4.5	—	20	35	—	44	
				6.0	—	17	30	—	37	
Output disable time	t_{pLZ} t_{pHZ}	$R_L = 1 \text{ k}\Omega$	50	2.0	—	30	150	—	190	ns
				4.5	—	15	30	—	38	
				6.0	—	14	26	—	33	
Maximum clock frequency	f_{max}	—	50	2.0	6	17	—	5	—	MHz
				4.5	30	50	—	25	—	
				6.0	35	59	—	28	—	
Input capacitance	C_{IN}	—	—	—	—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—	—	—	—	184	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

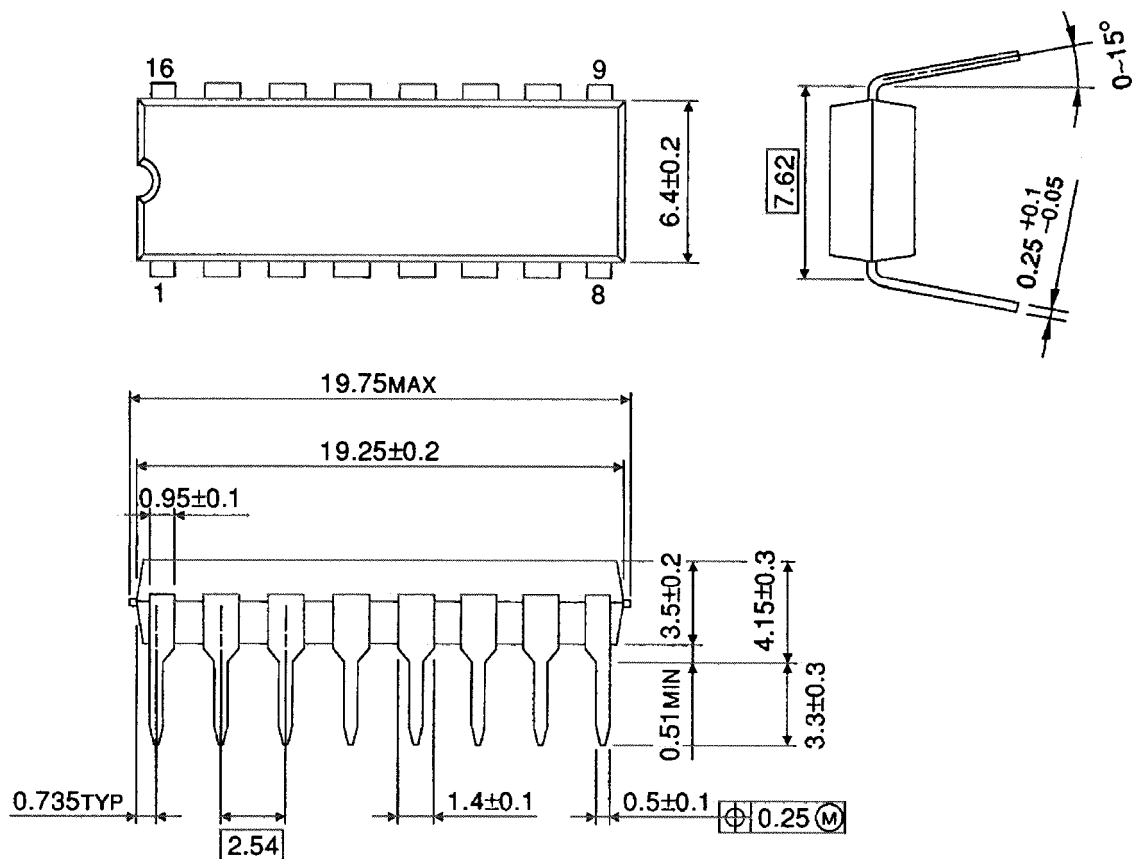
Average operating current can be obtained by the equation:

$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

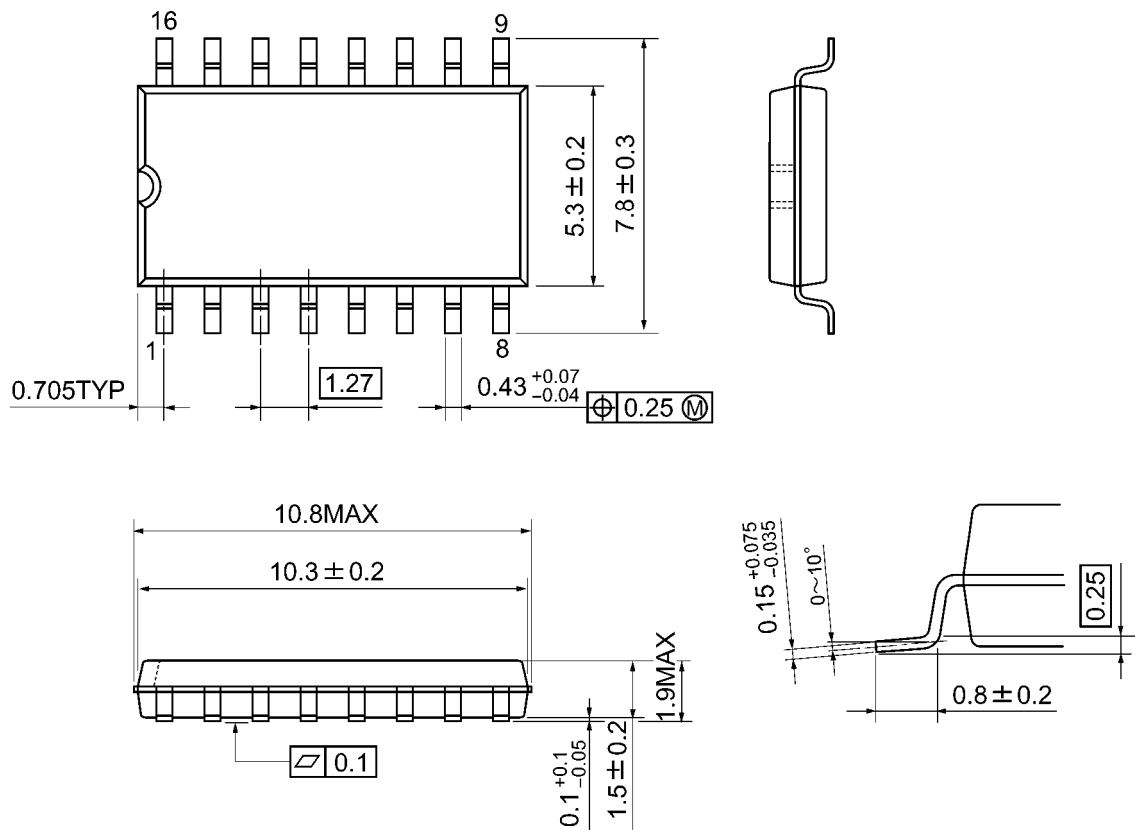


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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