

Stereo Audio Volume Control

FEATURES

- **DIGITALLY-CONTROLLED ANALOG VOLUME CONTROL:**
 - Two Independent Audio Channels
 - Serial Control Interface
 - Zero Crossing Detection
 - Mute Function
- **WIDE GAIN AND ATTENUATION RANGE:**
 - +31.5dB to -95.5dB with 0.5dB Steps
- **LOW NOISE AND DISTORTION:**
 - 120dB Dynamic Range
 - 0.0004% THD+N at 1kHz
- **LOW INTERCHANNEL CROSSTALK:**
 - 126dBFS
- **NOISE-FREE LEVEL TRANSITIONS**
- **POWER SUPPLIES:** ±15V Analog, +5V Digital
- **AVAILABLE IN DIP-16 AND SOL-16 PACKAGES**
- **PIN AND SOFTWARE COMPATIBLE WITH THE PGA2311 AND CIRRUS LOGIC CS3310™**

APPLICATIONS

- AUDIO AMPLIFIERS
- MIXING CONSOLES
- MULTI-TRACK RECORDERS
- BROADCAST STUDIO EQUIPMENT
- MUSICAL INSTRUMENTS
- EFFECTS PROCESSORS
- A/V RECEIVERS
- CAR AUDIO SYSTEMS

DESCRIPTION

The PGA2310 is a high-performance, stereo audio volume control designed for professional and high-end consumer audio systems. The ability to operate from ±15V analog power supplies enables the PGA2310 to process input signals with large voltage swings, thereby preserving the dynamic range available in the overall signal path. Using high performance operational amplifier stages internal to the PGA2310 yields low noise and distortion, while providing the capability to drive 600Ω loads directly without buffering. The three-wire serial control interface allows for connection to a wide variety of host controllers, in addition to support for daisy-chaining of multiple PGA2310 devices.



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PGA2310

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		PGA2310	UNIT
Supply voltage	V _{A+}	+16.0	V
	V _{A-}	-16.0	V
	V _{D+}	+6.5	V
Analogue input voltage	0 to V _{A+} , V _{A-}		V
Digital input voltage	-0.3 to V _{D+}		V
Operating temperature range	-55 to +125		°C
Storage temperature range	-65 to +150		°C
Junction temperature	+150		°C
Lead temperature (soldering, 10s)	+300		°C
Package temperature (IR, reflow, 10s)	+235		°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PGA2310	DIP-16	N	-40°C to +85°C	PGA2310PA	PGA2310PA	Rails, 25
	SOL-16	DW		PGA2310UA	PGA2310UA	Rails, 48
				PGA2310UA	PGA2310UA/1K	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

 At $T_A = +25^\circ\text{C}$, $V_{A+} = +15\text{V}$, $V_{A-} = -15\text{V}$, $V_{D+} = +5\text{V}$, $R_L = 100\text{k}\Omega$, $C_L = 20\text{pF}$, BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PGA2310			UNIT
		MIN	TYP	MAX	
DC CHARACTERISTICS					
Step Size		0.5			dB
Gain Error	Gain Setting = 31.5dB	±0.05			dB
Gain Matching		±0.05			dB
Input Resistance		10			$\text{k}\Omega$
Input Capacitance		7			pF
AC CHARACTERISTICS					
THD+N	$V_{IN} = 10\text{VPP}$, $f = 1\text{kHz}$	0.0004	0.001		%
Dynamic Range	$V_{IN} = \text{AGND}$, Gain = 0dB	116	120		dB
Voltage Range, Input and Output		$(V_{A-}) + 1.5$		$(V_{A-}) - 1.5$	V
Output Noise	$V_{IN} = \text{AGND}$, Gain = 0dB	9.5	13.5		μVRMS
Interchannel Crosstalk	$f = 1\text{kHz}$	-126			dBFS
OUTPUT BUFFER					
Offset Voltage	$V_{IN} = \text{AGND}$, Gain = 0dB	0.5	3		mV
Load Capacitance Stability		1000			pF
Short-Circuit Current		35			mA
Unity-Gain Bandwidth, Small Signal		1.5			MHz
DIGITAL CHARACTERISTICS					
High-Level Input Voltage, V_{IH}		+2.0			V
Low-Level Input Voltage, V_{IL}		-0.3			V
High-Level Output Voltage, V_{OH}	$I_O = 200\mu\text{A}$	$(V_{D+}) - 1.0$			V
Low-Level Output Voltage, V_{OL}	$I_O = -3.2\text{mA}$			0.4	V
Input Leakage Current			1	10	μA
SWITCHING CHARACTERISTICS					
Serial Clock (SCLK) Frequency	t_{SCLK}	0		6.25	MHz
Serial Clock (SCLK) Pulse Width Low	t_{PH}	80			ns
Serial Clock (SCLK) Pulse Width High	t_{PL}	80			ns
$\overline{\text{MUTE}}$ Pulse Width Low	t_{MI}	2.0			ms
Input Timing					
SDI Setup Time	t_{SDS}	20			ns
SDI Hold Time	t_{SDH}	20			ns
$\overline{\text{CS}}$ Falling to SCLK Rising	t_{CSCR}	90			ns
SCLK Falling to $\overline{\text{CS}}$ Rising	t_{CFCS}	35			ns
Output Timing					
$\overline{\text{CS}}$ Low to SDO Active	t_{CSO}			35	ns
SCLK Falling to SDO Data Valid	t_{CFDO}			60	ns
$\overline{\text{CS}}$ High to SDO High Impedance	t_{CSZ}			100	ns
POWER SUPPLY					
Operating Voltage					
V_{A+}		+4.5	+15	+15.5	V
V_{A-}		-4.5	-15	-15.5	V
V_{D+}		+4.5	+5	+5.5	V
Quiescent Current					
I_{A+}	$V_{A+} = +15\text{V}$		7.5	10	mA
I_{A-}	$V_{A-} = -15\text{V}$		7.7	10	mA
I_{D+}	$V_{D+} = +5\text{V}$		0.8	1.5	mA

PGA2310

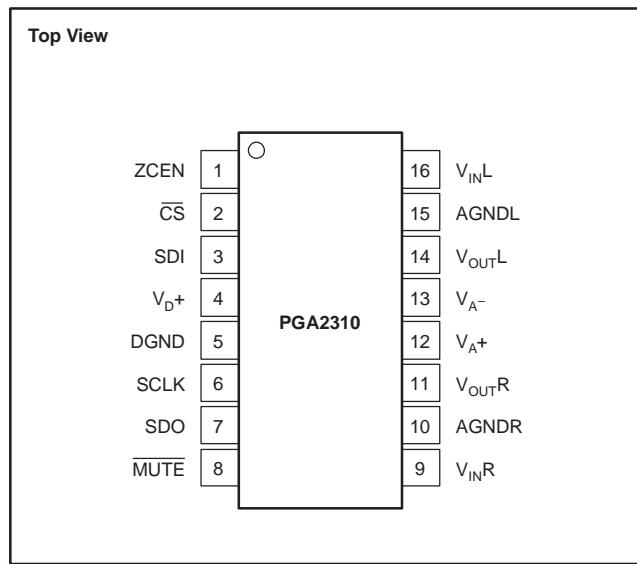
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ELECTRICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{A+} = +15\text{V}$, $V_{A-} = -15\text{V}$, $V_{D+} = +5\text{V}$, $R_L = 100\text{k}\Omega$, $C_L = 20\text{pF}$, BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PGA2310			UNIT
		MIN	TYP	MAX	
TEMPERATURE RANGE					
Specified Range		-40		+85	°C
Operating Range		-55		+125	°C
Storage Range		-65		+150	°C
Thermal Resistance, θ_{JC}					
DIP-16			60		°C/W
SOL-16			50		°C/W

PIN CONFIGURATION

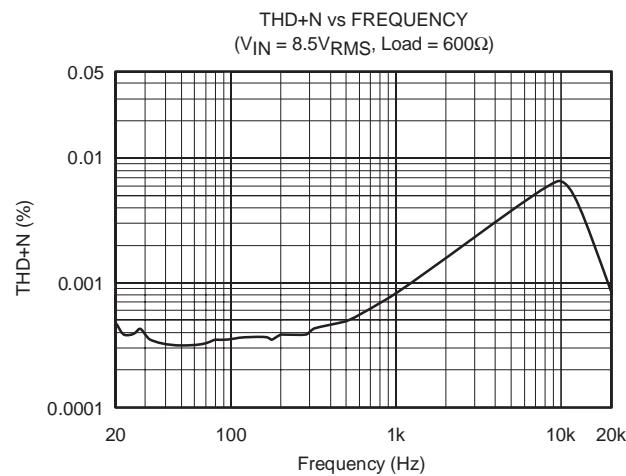
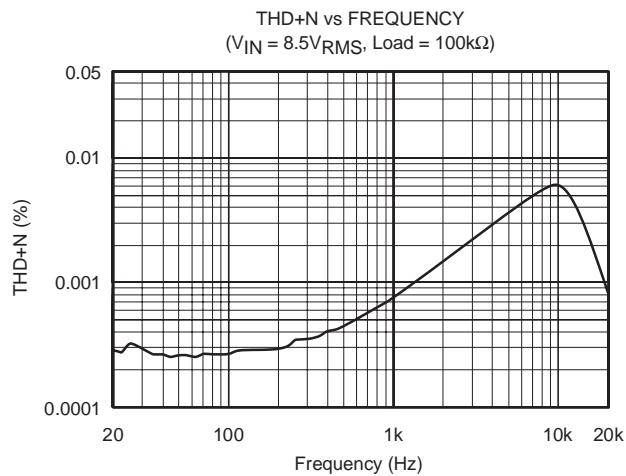
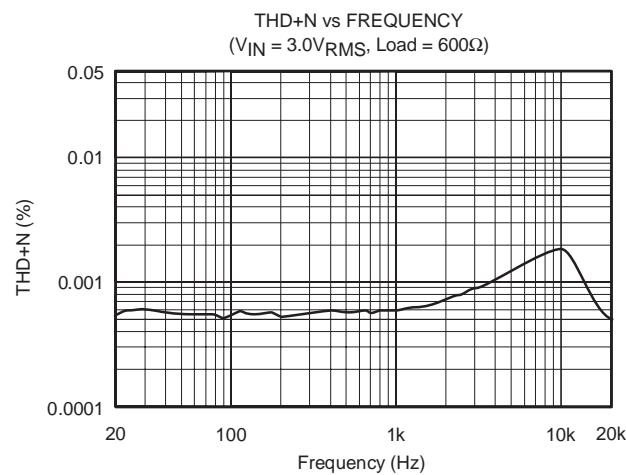
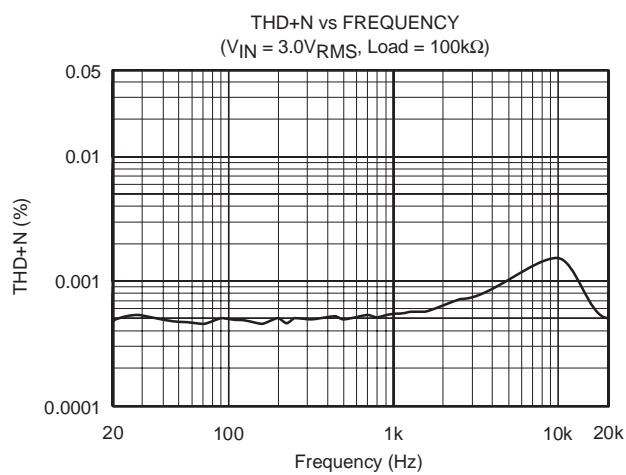
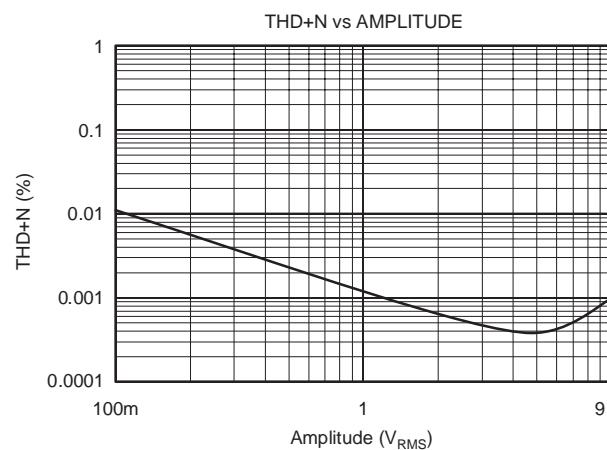
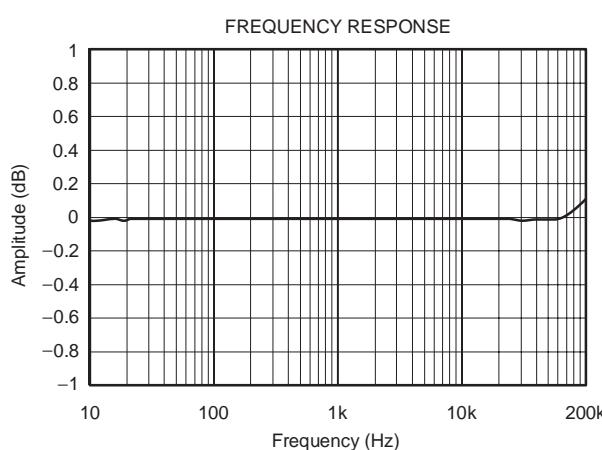


PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	ZCEN	Zero Crossing Enable Input (Active High)
2	CS	Chip Select Input (Active Low)
3	SDI	Serial Data input
4	VD+	Digital Power Supply, +5V
5	DGND	Digital Ground
6	SCLK	Serial Clock Input
7	SDO	Serial Data Output
8	MUTE	Mute Control Input (Active Low)
9	VINR	Analog Input, Right Channel
10	AGNDR	Analog Ground, Right Channel
11	VOUTR	Analog Output, Right Channel
12	VA+	Analog Power Supply, +15V
13	VA-	Analog Power Supply, -15V
14	VOUTL	Analog Output, Left Channel
15	AGNDL	Analog Ground, Left Channel
16	VINL	Analog Input, Left Channel

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_{A+} = +15\text{V}$, $V_{A-} = -15\text{V}$, $V_{D+} = +5\text{V}$, $R_L = 100\text{k}\Omega$, $C_L = 20\text{pF}$, BW measure = 10Hz to 20kHz, unless otherwise noted.

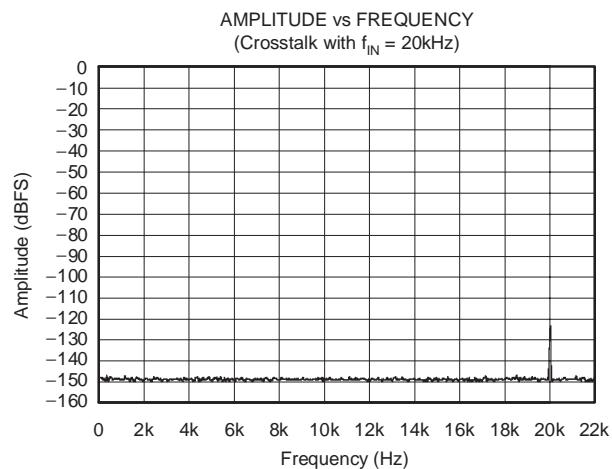
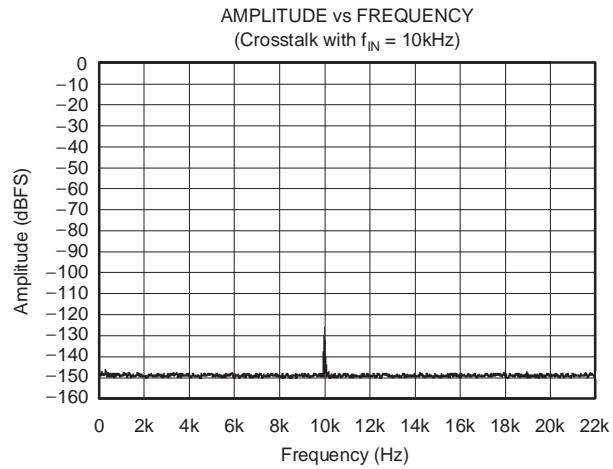
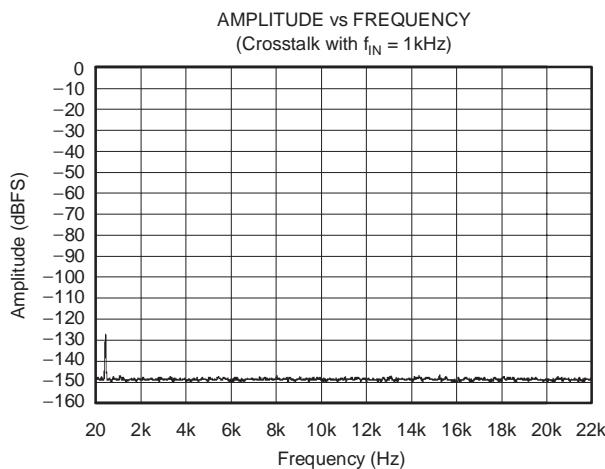


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TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{A+} = +15\text{V}$, $V_{A-} = -15\text{V}$, $V_{D+} = +5\text{V}$, $R_L = 100\text{k}\Omega$, $C_L = 20\text{pF}$, BW measure = 10Hz to 20kHz, unless otherwise noted.



GENERAL DESCRIPTION

The PGA2310 is a stereo audio volume control. It may be used in a wide array of professional and consumer audio equipment. The PGA2310 is fabricated in a mixed-signal BiCMOS process, as to take advantage of the superior analog characteristics for which it offers.

The heart of the PGA2310 is a resistor network, an analog switch array, and a high-performance bipolar op amp stage. The switches are used to select taps in the resistor network that, in turn, determine the gain of the amplifier stage. Switch selections are programmed using a serial control port. The serial port allows connection to a wide variety of host controllers. Figure 1 shows a functional block diagram of the PGA2310.

POWER-UP STATE

On power up, all internal flip-flops are reset. The gain byte value for both the left and right channels are set to 00_{HEX}, or mute condition. The gain will remain at this setting until the host controller programs new settings for each channel via the serial control port.

ANALOG INPUTS AND OUTPUTS

The PGA2310 includes two independent channels, referred to as the left and right channels. Each channel has a corresponding input and output pin. The input and output pins are unbalanced, or referenced to analog ground (either AGNDR or AGNDL). The inputs are named V_{INL} (pin 9) and V_{INL} (pin 16), while the outputs are named V_{OUTL} (pin 11) and V_{OUTL} (pin 14).

The input and output pins may swing within 1.5V of the analog power supplies, V_{A+} (pin 12) and V_{A-} (pin 13). Given V_{A+} = +15V and V_{A-} = -15V, the maximum input or output voltage range is 27V_{PP}.

It is important to drive the PGA2310 with a low source impedance. If a source impedance of greater than 600Ω is used, the distortion performance of the PGA2310 will begin to degrade.

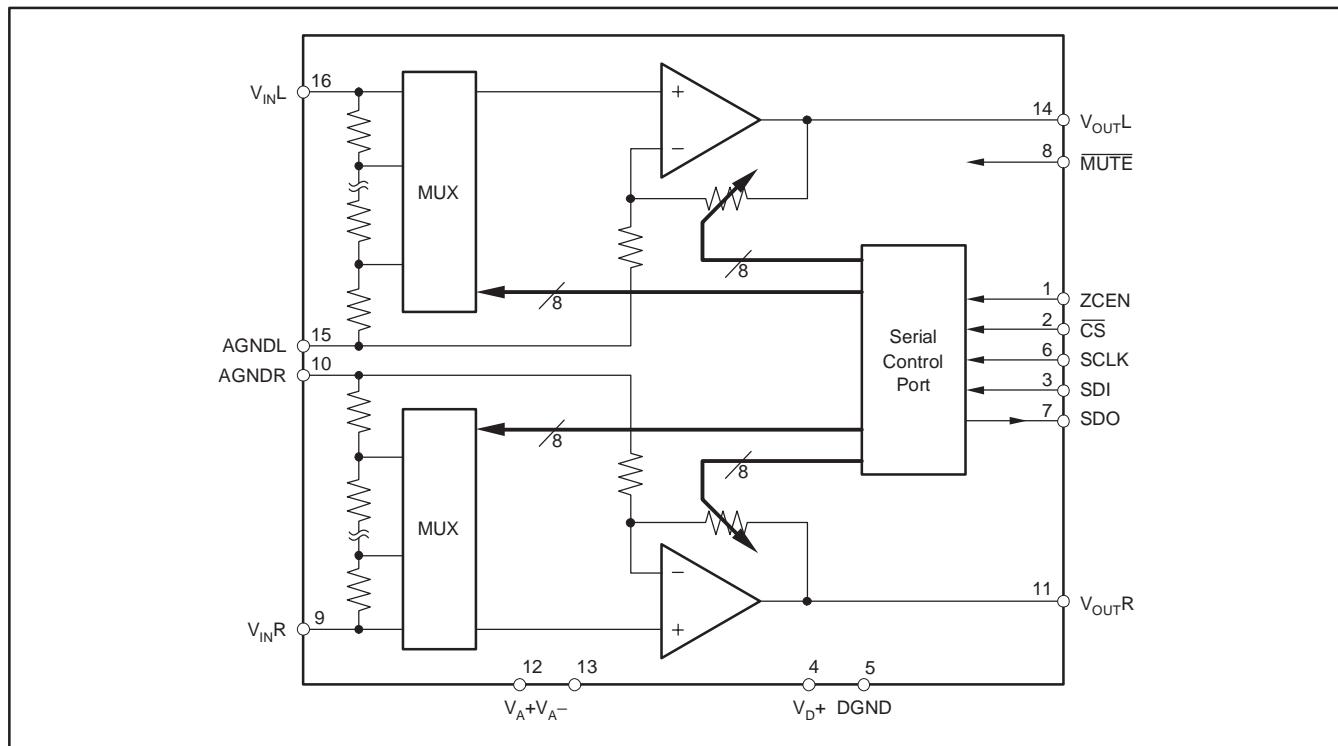


Figure 1. PGA2310 Block Diagram

SERIAL CONTROL PORT

The serial control port is utilized to program the gain settings for the PGA2310. The serial control port includes three input pins and one output pin. The inputs include \overline{CS} (pin 2), SDI (pin 3), and SCLK (pin 6). The sole output pin is SDO (pin 7).

The \overline{CS} pin functions as the chip select input. Data may be written to the PGA2310 only when \overline{CS} is low. SDI is the serial data input pin. Control data is provided as a 16-bit word at the SDI pin, 8 bits each for the left and right channel

gain settings. Data is formatted as MSB first, straight binary code. SCLK is the serial clock input. Data is clocked into SDI on the rising edge of SCLK.

SDO is the serial data output pin, and is used when daisy-chaining multiple PGA2310 devices. Daisy-chain operation is described in detail later in this section. SDO is a tristate output, and assumes a high impedance state when \overline{CS} is high.

The protocol for the serial control port is shown in Figure 2. See Figure 3 for detailed timing specifications of the serial control port.

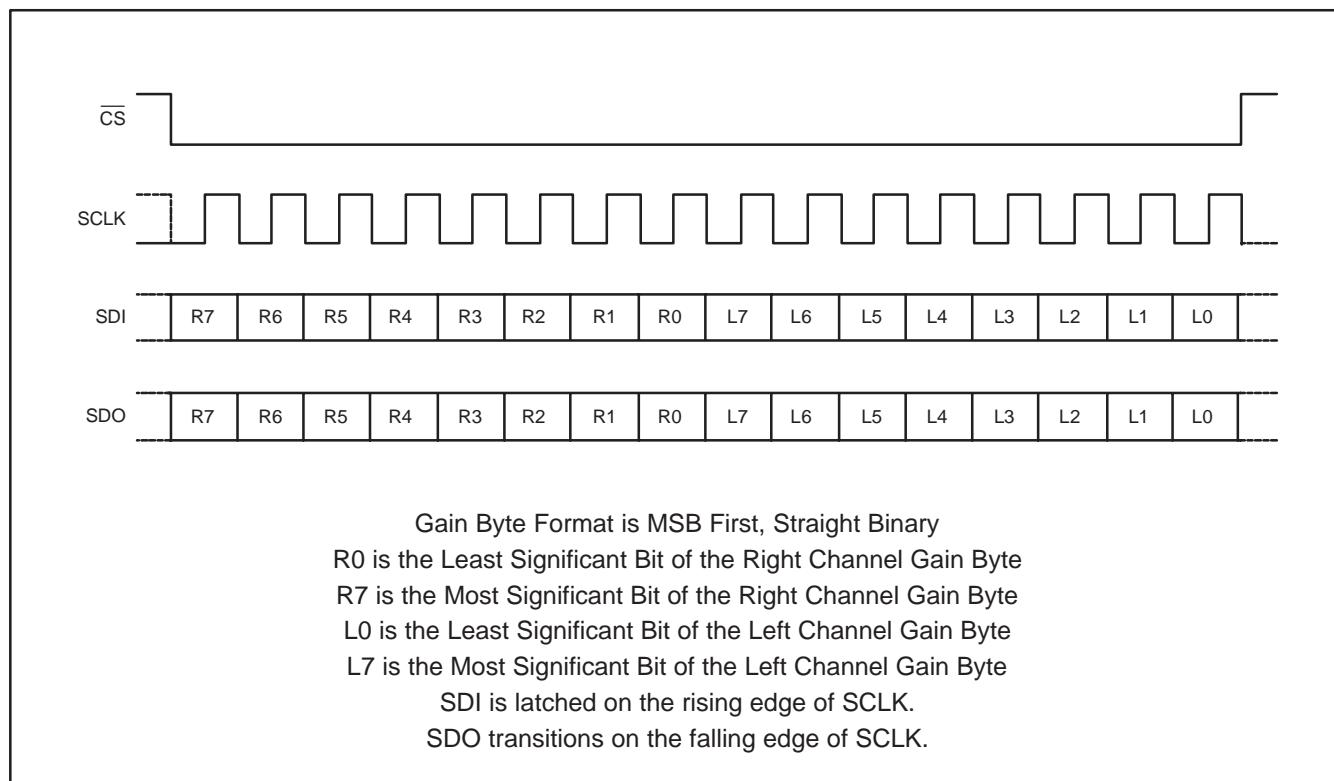


Figure 2. Serial Interface Protocol

GAIN SETTINGS

The gain for each channel is set by its corresponding 8-bit code, either R[7:0] or L[7:0], see Figure 2. The gain code data is straight binary format. If we let N equal the decimal equivalent of R[7:0] or L[7:0], then the following relationships exist for the gain settings:

For N = 0:

Mute Condition. The input multiplexer is connected to analog ground (AGNDR or AGNDL).

For N = 1 to 255:

$$\text{Gain (dB)} = 31.5 - [0.5 \bullet (255 - N)]$$

This results in a gain range of +31.5dB (with N = 255) to -95.5dB (with N = 1).

Changes in gain setting may be made with or without zero crossing detection. The operation of the zero crossing detector and timeout circuitry is discussed later in this data sheet.

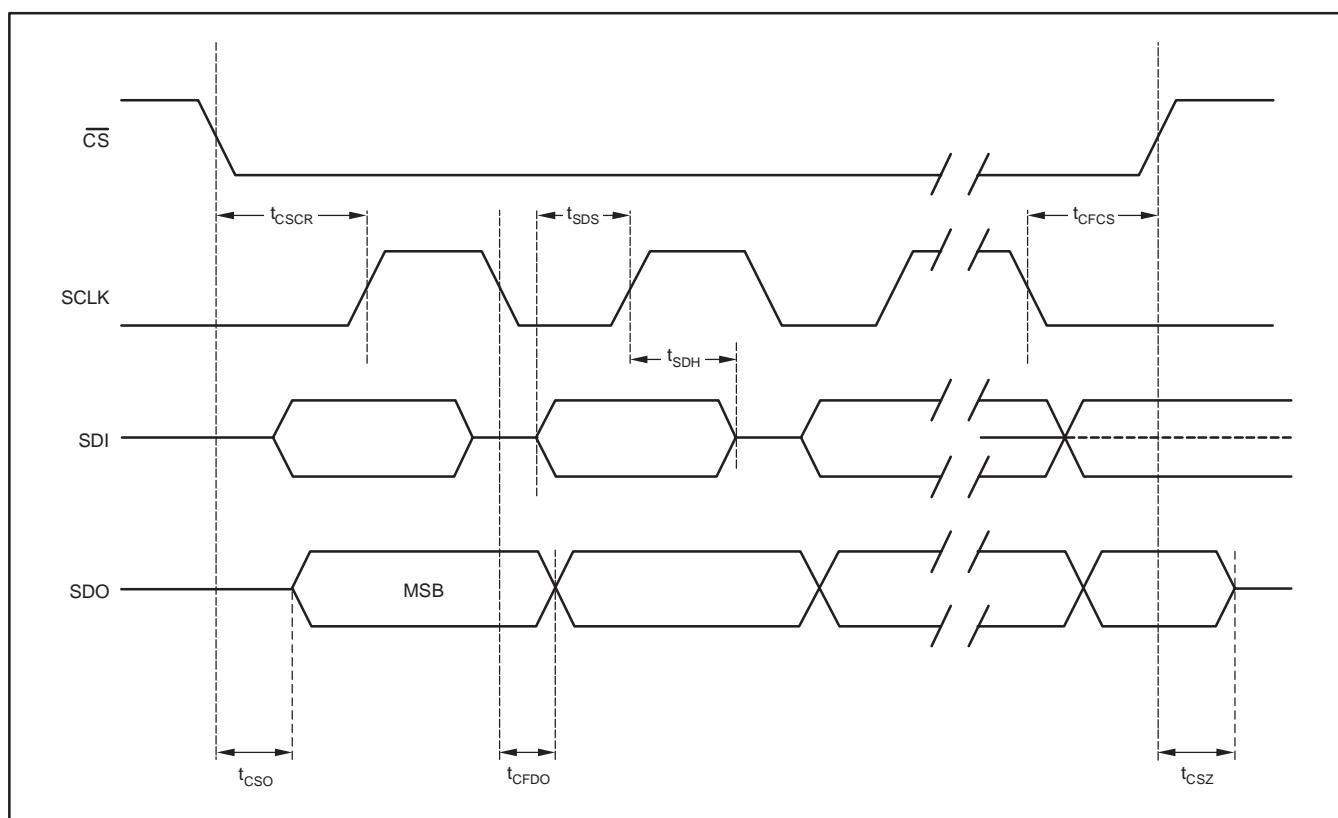


Figure 3. Serial Interface Timing Requirements

DAISY-CHAINING MULTIPLE PGA2310 DEVICES

In order to reduce the number of control signals required to support multiple PGA2310 devices on a printed circuit board, the serial control port supports daisy-chaining of multiple PGA2310 devices. Figure 4 shows the connection requirements for daisy-chain operation. This arrangement allows a three-wire serial interface to control many PGA2310 devices.

As shown in Figure 4, the SDO pin from device #1 is connected to the SDI input of device #2, and is repeated for additional devices. This in turn forms a large shift register, in which gain data may be written for all PGA2310s connected to the serial bus. The length of the shift register is $16 \times N$ bits, where N is equal to the number of PGA2310 devices included in the chain. The \overline{CS} input must remain low for $16 \times N$ SCLK periods, where N is the number of devices connected in the chain, in order to allow enough SCLK cycles to load all devices.

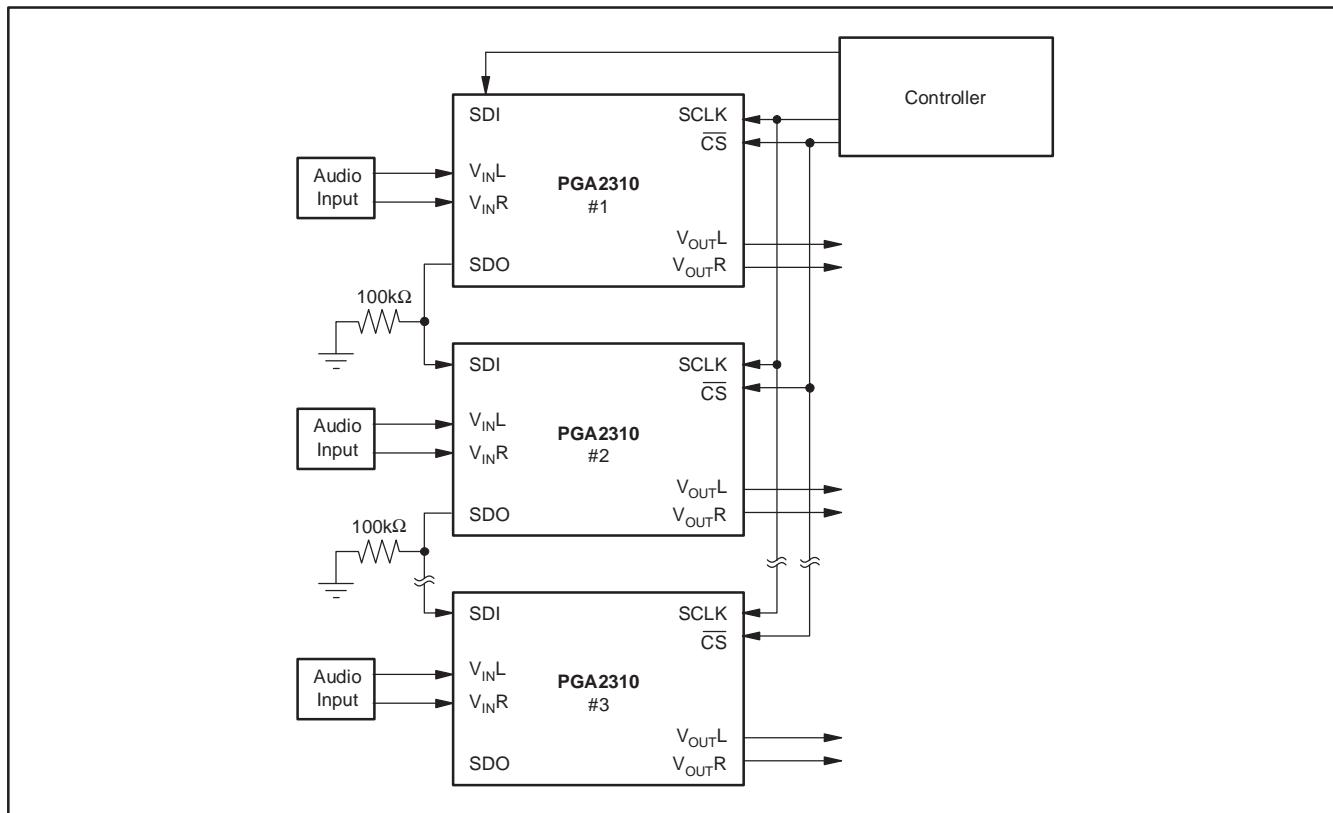


Figure 4. Daisy-Chain Diagram for Multiple PGA2310 Devices

ZERO CROSSING DETECTION

The PGA2310 includes a zero crossing detection function that can provide for noise-free level transitions. The concept is to change gain settings on a zero crossing of the input signal, thus minimizing audible glitches. This function is enabled or disabled using the ZCEN input (pin 1). When ZCEN is low, zero crossing detection is disabled. When ZCEN is high, zero crossing detection will be enabled.

The zero crossing detection takes effect with a change in gain setting for a corresponding channel. The new gain setting will not be latched until either two zero crossings are detected, or a timeout period of 16ms has elapsed without detecting two zero crossings. In the case of a timeout, the new gain setting takes effect with no attempt to minimize audible artifacts.

MUTE FUNCTION

The PGA2310 includes a MUTE function. This function may be activated by either the MUTE input (pin 8), or by setting the gain byte value for one or both channels to 00_{HEX}. The MUTE pin may be used to mute both channels, while the gain setting may be used to selectively mute the left and right channels. Muting is accomplished by switching the input multiplexer to analog ground (AGNDL or AGNDR) with zero crossing enabled.

The MUTE pin is active low. When MUTE is low, each channel will be muted following the next zero crossing event or timeout that occurs on that channel. If MUTE becomes active while CS is also active, the mute will take effect once the CS pin goes high. When the MUTE pin is high, the PGA2310 operates normally, with the mute function disabled.

APPLICATIONS INFORMATION

This section includes additional information that is pertinent to designing the PGA2310 into an end application.

RECOMMENDED CONNECTION DIAGRAM

Figure 5 depicts the recommended connections for the PGA2310. Power-supply bypass capacitors should be placed as close to the PGA2310 package as physically possible.

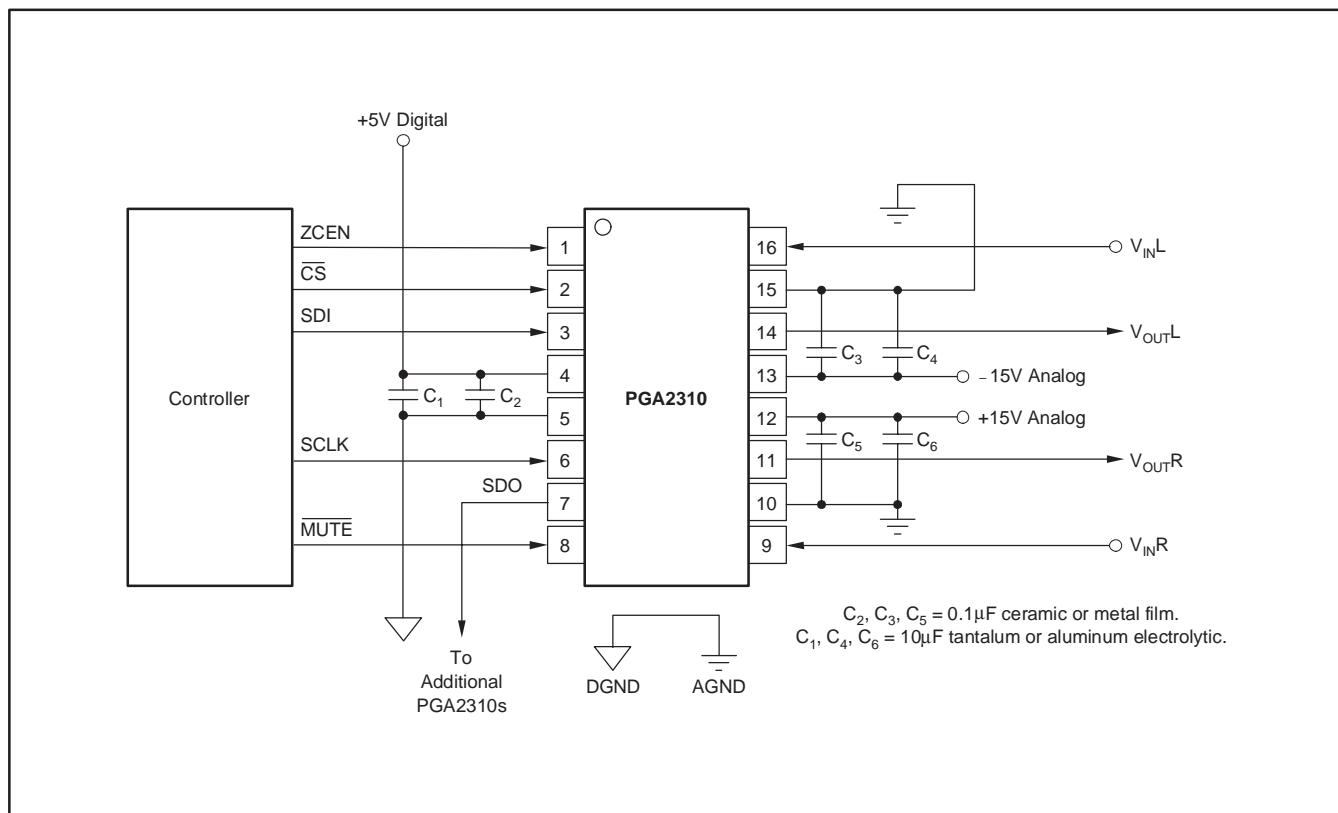


Figure 5. Recommended Connection Diagram

PRINTED CIRCUIT BOARD LAYOUT GUIDELINES

It is recommended that the ground planes for the digital and analog sections of the printed circuit board (PCB) be separate from one another. The planes should be connected at a single point. Figure 6 shows the recommended PCB floor plan for the PGA2310.

The PGA2310 is mounted so that it straddles the split between the digital and analog ground planes. Pins 1 through 8 are oriented to the digital side of the board, while pins 9 through 16 are on the analog side of the board.

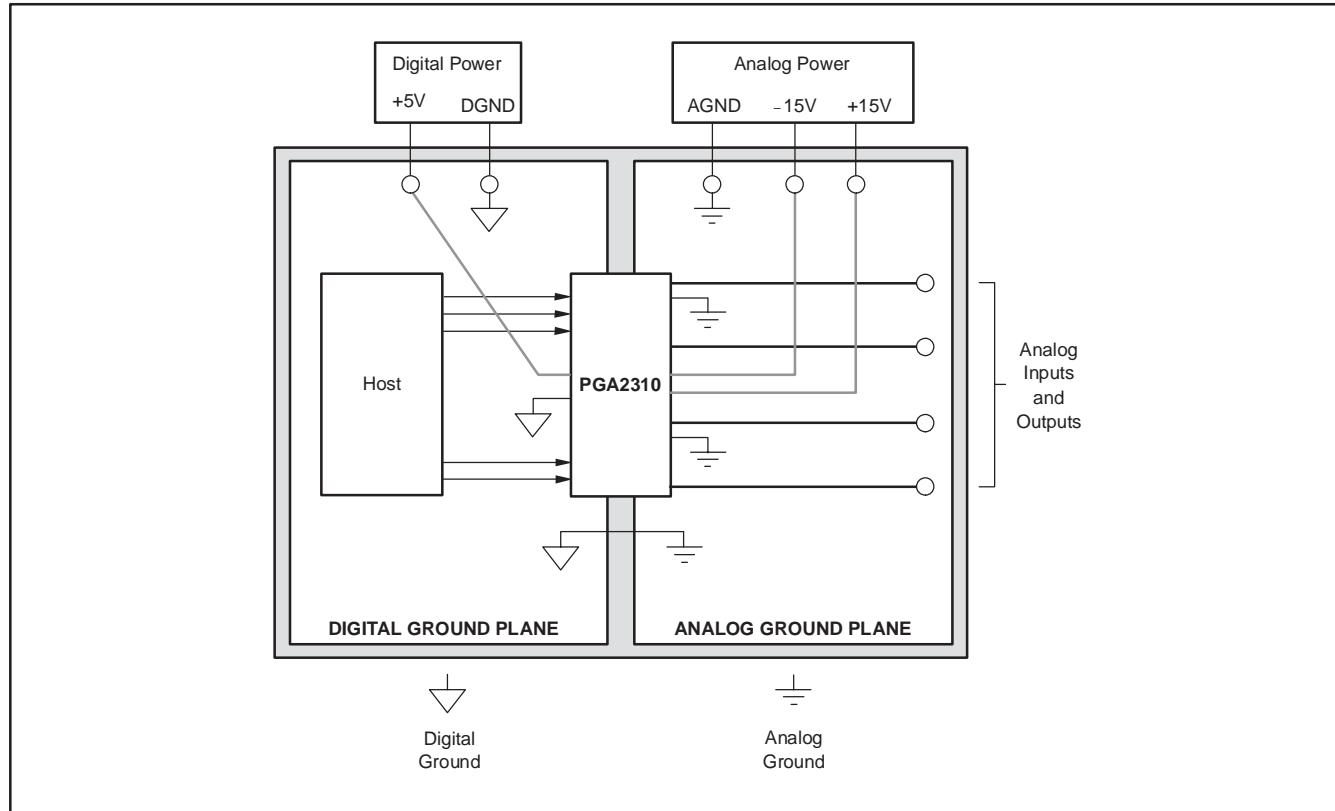


Figure 6. Typical PCB Layout Floor Plan

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PGA2310PA	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA2310PAG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
PGA2310UA	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA2310UA/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA2310UA/1KG4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA2310UAG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

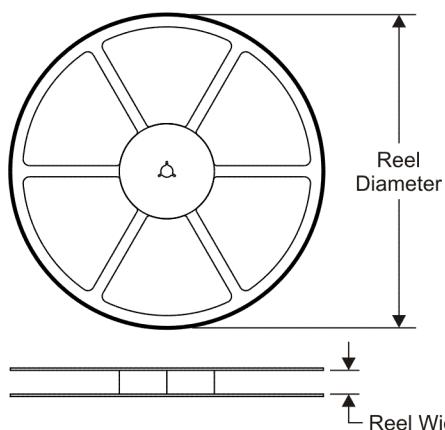
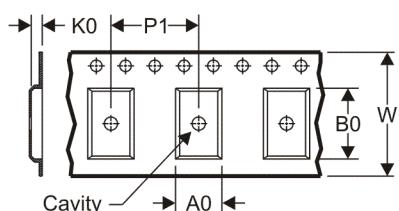
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

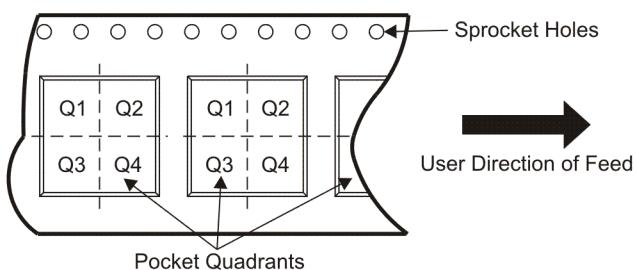
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

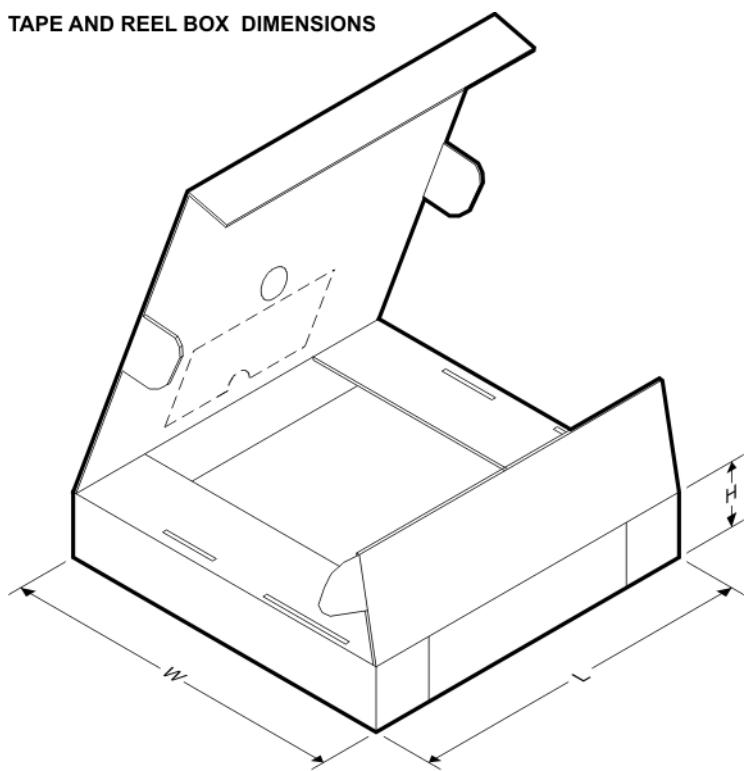
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA2310UA/1K	SOIC	DW	16	1000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

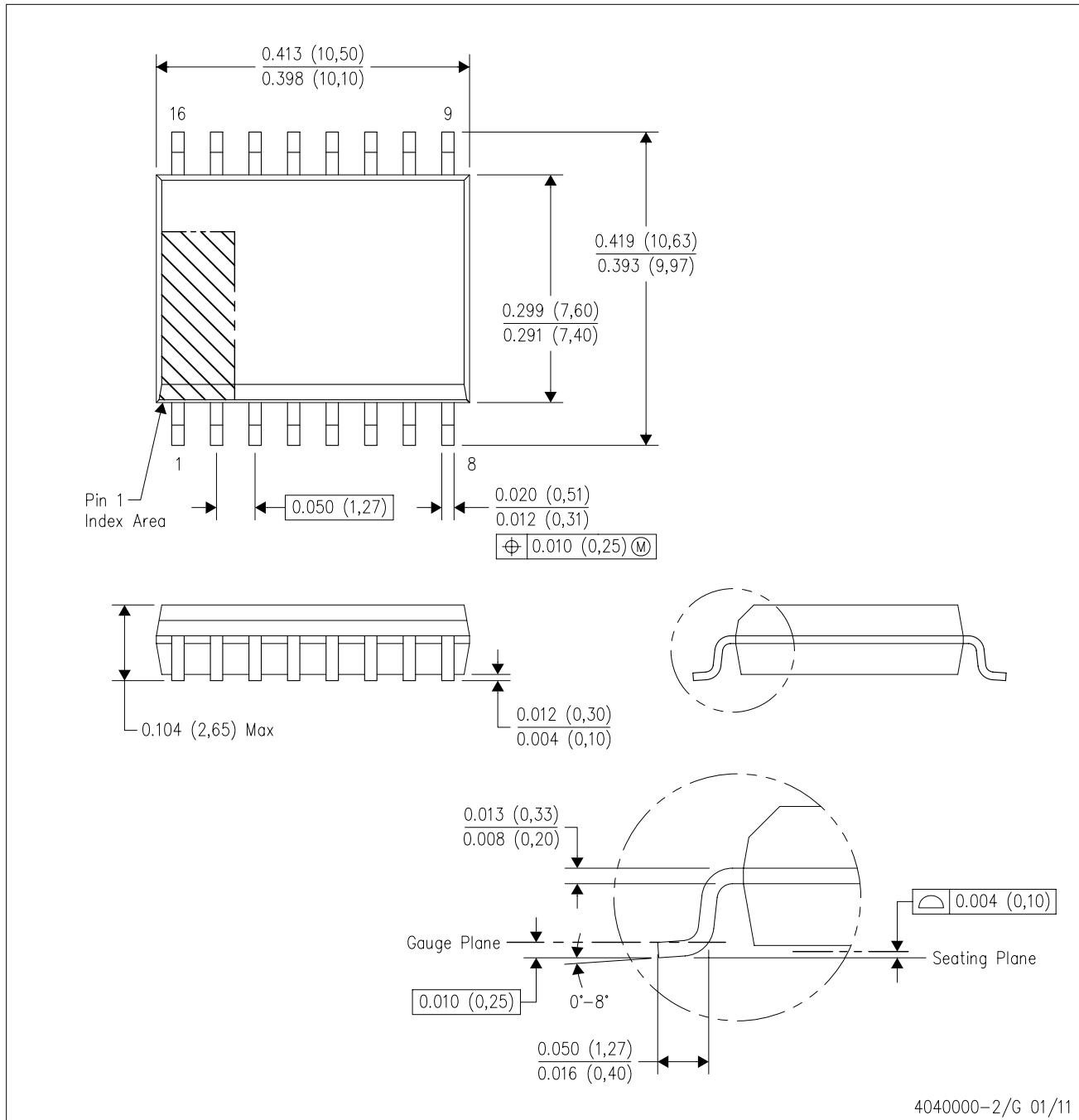
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA2310UA/1K	SOIC	DW	16	1000	346.0	346.0	33.0

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



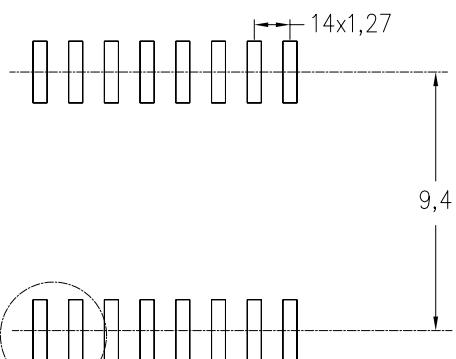
- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AA.

LAND PATTERN DATA

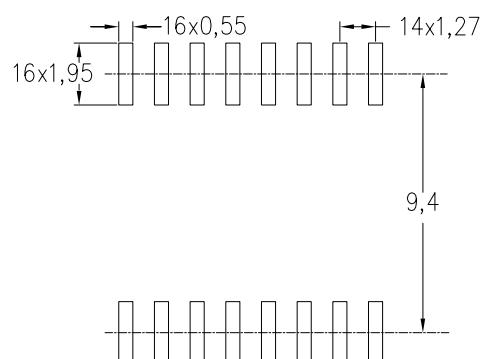
DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

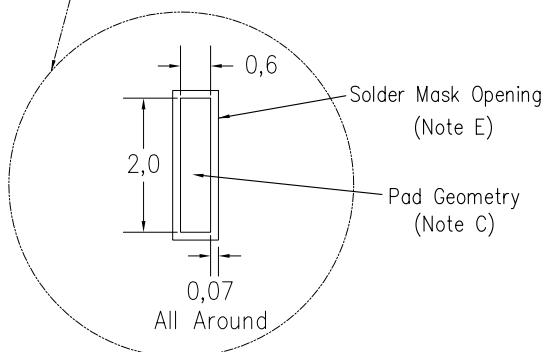
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Non Solder Mask Define Pad



4209202-2/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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