

The S-8215A Series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates high-accuracy voltage detection circuits and delay circuits.

Short-circuiting between cells makes it possible for serial connection of three cells to five cells.

## ■ Features

- High-accuracy voltage detection circuit for each cell
  - Overcharge detection voltage n (n = 1 to 5)
    - 3.600 V to 4.700 V (50 mV step)
    - Accuracy  $\pm 25$  mV (Ta =  $+25^{\circ}\text{C}$ )
    - Accuracy  $\pm 30$  mV (Ta =  $-5^{\circ}\text{C}$  to  $+55^{\circ}\text{C}$ )
  - Overcharge hysteresis voltage n (n = 1 to 5)
    - 0.0 mV to  $-550$  mV (50 mV step)
      - $-300$  mV to  $-550$  mV Accuracy  $\pm 20\%$
      - $-100$  mV to  $-250$  mV Accuracy  $\pm 50$  mV
      - 0.0 mV to  $-50$  mV Accuracy  $\pm 25$  mV
- Delay times for overcharge detection can be set by an internal circuit only (External capacitors are unnecessary).
- Output form is selectable: CMOS output, Nch open-drain output, Pch open-drain output
- Output logic is selectable: Active "H", active "L"
- High-withstand voltage: Absolute maximum rating 28 V
- Wide operation voltage range: 3.6 V to 26 V
- Wide operation temperature range: Ta =  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Low current consumption
  - At  $V_{\text{CUn}}$  – 1.0 V for each cell: 3.0  $\mu\text{A}$  max. (Ta =  $+25^{\circ}\text{C}$ )
  - At 2.3 V for each cell: 1.7  $\mu\text{A}$  max. (Ta =  $+25^{\circ}\text{C}$ )
- Lead-free (Sn 100%), halogen-free

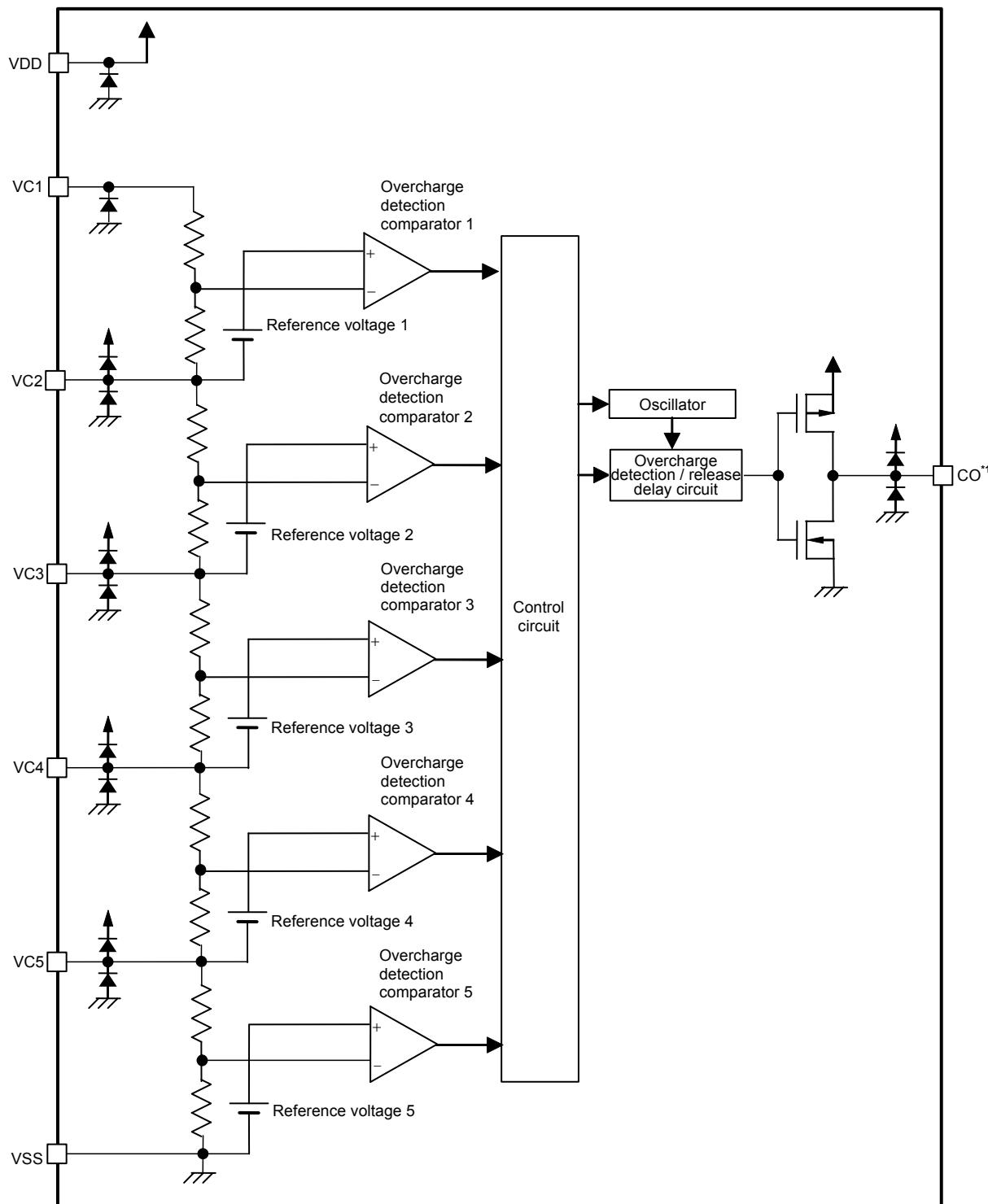
## ■ Application

- Lithium-ion rechargeable battery pack (for secondary protection)

## ■ Packages

- TMSOP-8
- SNT-8A

■ Block Diagram



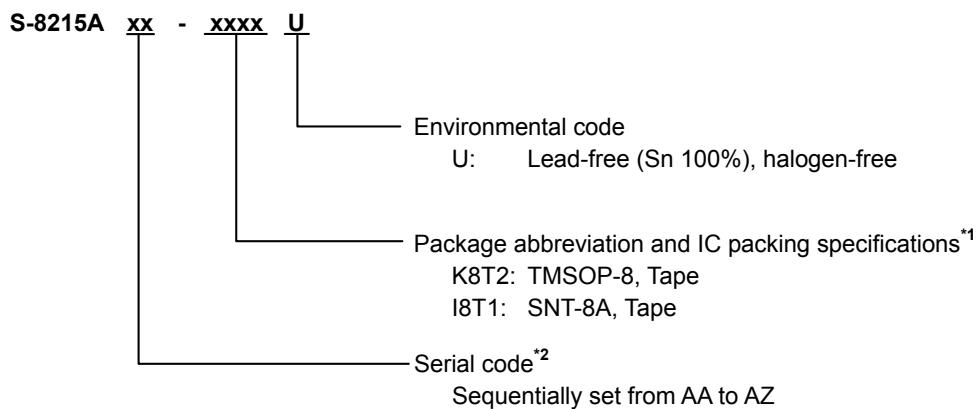
\*1. The CO pin is connected only to Nch transistor in the case of Nch open-drain output.  
The CO pin is connected only to Pch transistor in the case of Pch open-drain output.

**Remark** The diodes in the figure are parasitic diodes.

Figure 1

## ■ Product Name Structure

### 1. Product name



\*1. Refer to the tape drawing.

\*2. Refer to "3. Product name list".

### 2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	—
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

### 3. Product name list

#### 3.1 TMSOP-8

Table 2

Product Name	Overcharge Detection Voltage [V <sub>cu</sub> ]	Overcharge Hysteresis Voltage [V <sub>HC</sub> ]	Overcharge Detection Delay Time [t <sub>cu</sub> ]	Output Form	Output Logic
S-8215AAA-K8T2U	4.300 V	-0.300 V	4.0 s	CMOS output	Active "H"
S-8215AAB-K8T2U	4.275 V	-0.050 V	2.0 s	Nch open-drain output	Active "L"
S-8215AAC-K8T2U	4.150 V	-0.250 V	1.0 s	CMOS output	Active "H"
S-8215AAD-K8T2U	4.350 V	-0.250 V	2.0 s	CMOS output	Active "H"
S-8215AAE-K8T2U	4.325 V	-0.050 V	1.0 s	Nch open-drain output	Active "L"
S-8215AAF-K8T2U	4.220 V	-0.100 V	1.0 s	CMOS output	Active "H"
S-8215AAH-K8T2U	4.325 V	-0.300 V	1.0 s	Nch open-drain output	Active "L"
S-8215AAI-K8T2U	4.250 V	-0.250 V	1.0 s	CMOS output	Active "H"
S-8215AAJ-K8T2U	4.400 V	-0.100 V	2.0 s	CMOS output	Active "H"
S-8215AAK-K8T2U	4.150 V	-0.050 V	2.0 s	Nch open-drain output	Active "L"
S-8215AAL-K8T2U	4.150 V	-0.500 V	2.0 s	Nch open-drain output	Active "L"
S-8215AAM-K8T2U	4.150 V	-0.050 V	2.0 s	CMOS output	Active "L"
S-8215AAN-K8T2U	4.150 V	-0.500 V	2.0 s	CMOS output	Active "L"
S-8215AAO-K8T2U	4.350 V	-0.250 V	4.0 s	CMOS output	Active "H"
S-8215AAP-K8T2U	4.275 V	-0.500 V	1.0 s	CMOS output	Active "H"
S-8215AAQ-K8T2U	4.275 V	-0.050 V	1.0 s	CMOS output	Active "H"
S-8215AAR-K8T2U	4.500 V	-0.100 V	4.0 s	CMOS output	Active "H"
S-8215AAS-K8T2U	4.275 V	-0.200 V	2.0 s	CMOS output	Active "L"
S-8215AAT-K8T2U	4.275 V	-0.050 V	2.0 s	CMOS output	Active "L"
S-8215AAU-K8T2U	3.750 V	-0.100 V	1.0 s	CMOS output	Active "H"
S-8215AAV-K8T2U	4.300 V	-0.300 V	1.0 s	CMOS output	Active "H"

**Remark** Please contact our sales office for the products with detection voltage value other than those specified above.

#### 3.2 SNT-8A

Table 3

Product Name	Overcharge Detection Voltage [V <sub>cu</sub> ]	Overcharge Hysteresis Voltage [V <sub>HC</sub> ]	Overcharge Detection Delay Time [t <sub>cu</sub> ]	Output Form	Output Logic
S-8215AAA-I8T1U	4.300 V	-0.300 V	4.0 s	CMOS output	Active "H"
S-8215AAG-I8T1U	4.220 V	-0.050 V	1.0 s	CMOS output	Active "H"
S-8215AAV-I8T1U	4.300 V	-0.300 V	1.0 s	CMOS output	Active "H"

**Remark** Please contact our sales office for the products with detection voltage value other than those specified above.

## ■ Pin Configurations

### 1. TMSOP-8

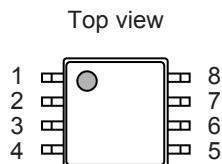


Figure 2

Table 4

Pin No.	Symbol	Description
1	VDD	Input pin for positive power supply
2	VC1	Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VC5	Negative voltage connection pin of battery 4 Positive voltage connection pin of battery 5
7	VSS	Input pin for negative power supply Negative voltage connection pin of battery 5
8	CO	FET gate connection pin for charge control

### 2. SNT-8A

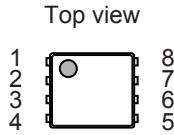


Figure 3

Table 5

Pin No.	Symbol	Description
1	VDD	Input pin for positive power supply
2	VC1	Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VC5	Negative voltage connection pin of battery 4 Positive voltage connection pin of battery 5
7	VSS	Input pin for negative power supply Negative voltage connection pin of battery 5
8	CO	FET gate connection pin for charge control

## ■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V <sub>DS</sub>	VDD	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 28	V
Input pin voltage	V <sub>IN</sub>	VC1, VC2, VC3, VC4, VC5	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
CO pin output voltage	V <sub>CO</sub>	CO	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
			V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 28	V
			V <sub>DD</sub> – 28 to V <sub>DD</sub> + 0.3	V
Power dissipation	P <sub>D</sub>	–	650 <sup>*1</sup>	mW
			450 <sup>*1</sup>	mW
Operation ambient temperature	T <sub>opr</sub>	–	–40 to +85	°C
Storage temperature	T <sub>stg</sub>	–	–40 to +125	°C

\*1. When mounted on board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Name: JEDEC STANDARD51-7

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

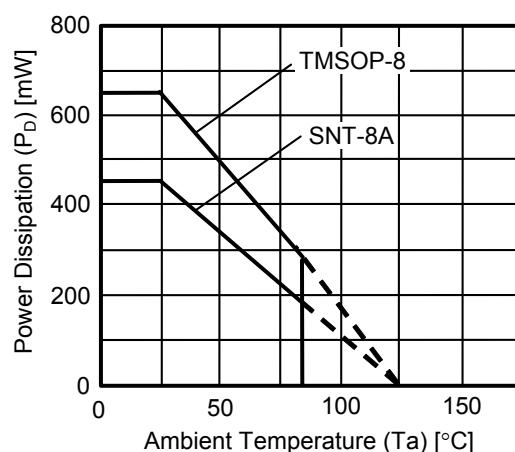


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
<b>Detection Voltage</b>							
Overcharge detection voltage n (n = 1, 2, 3, 4, 5)	V <sub>CUn</sub>	–	V <sub>CU</sub> – 0.025	V <sub>CU</sub>	V <sub>CU</sub> + 0.025	V	1
		Ta = –5°C to +55°C*1	V <sub>CU</sub> – 0.030	V <sub>CU</sub>	V <sub>CU</sub> + 0.030	V	1
Overcharge hysteresis voltage n (n = 1, 2, 3, 4, 5)	V <sub>HCn</sub>	–550 mV ≤ V <sub>HC</sub> ≤ –300 mV	V <sub>HC</sub> × 0.8	V <sub>HC</sub>	V <sub>HC</sub> × 1.2	V	1
		–250 mV ≤ V <sub>HC</sub> ≤ –100 mV	V <sub>HC</sub> – 0.050	V <sub>HC</sub>	V <sub>HC</sub> + 0.050	V	1
		V <sub>HC</sub> = –50 mV, 0 mV	V <sub>HC</sub> – 0.025	V <sub>HC</sub>	V <sub>HC</sub> + 0.025	V	1
<b>Input Voltage</b>							
Operation voltage between VDD pin and VSS pin	V <sub>DSOP</sub>	–	3.6	–	26	V	–
<b>Input Current</b>							
Current consumption during operation	I <sub>OPE</sub>	V1 = V2 = V3 = V4 = V5 = V <sub>CU</sub> – 1.0 V	–	1.6	3.0	μA	3
Current consumption during overdischarge	I <sub>OPED</sub>	V1 = V2 = V3 = V4 = V5 = 2.3 V	–	0.8	1.7	μA	3
VC1 pin current	I <sub>VC1</sub>	V1 = V2 = V3 = V4 = V5 = V <sub>CU</sub> – 1.0 V	–	0.2	0.4	μA	4
VCn pin current (n = 2, 3, 4, 5)	I <sub>VCn</sub>	V1 = V2 = V3 = V4 = V5 = V <sub>CU</sub> – 1.0 V	–0.3	0	0.3	μA	4
<b>Output Current (CMOS Output Product)</b>							
CO pin sink current	I <sub>COL</sub>	–	0.4	–	–	mA	5
CO pin source current	I <sub>COH</sub>	–	20	–	–	μA	5
<b>Output Current (Nch Open-drain Output Product)</b>							
CO pin sink current	I <sub>COL</sub>	–	0.4	–	–	mA	5
CO pin leakage current "L"	I <sub>COLL</sub>	–	–	–	0.1	μA	5
<b>Output Current (Pch Open-drain Output Product)</b>							
CO pin source current	I <sub>COH</sub>	–	20	–	–	μA	5
CO pin leakage current "H"	I <sub>COLH</sub>	–	–	–	0.1	μA	5
<b>Delay Time</b>							
Overcharge detection delay time	t <sub>CU</sub>	–	t <sub>CU</sub> × 0.8	t <sub>CU</sub>	t <sub>CU</sub> × 1.2	s	1
Overcharge timer reset delay time	t <sub>TR</sub>	–	6	12	20	ms	1
Transition time to test mode	t <sub>TST</sub>	–	–	–	80	ms	2

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

## ■ Test Circuits

### 1. Overcharge detection voltage, overcharge hysteresis voltage (Test circuit 1)

#### 1. 1 Overcharge detection voltage n ( $V_{CU_n}$ )

Set  $V1 = V2 = V3 = V4 = V5 = V_{CU} - 0.05$  V. The overcharge detection voltage 1 ( $V_{CU1}$ ) is the  $V1$  voltage when the CO pin's output changes after the voltage of  $V1$  has been gradually increased.

Overcharge detection voltage ( $V_{CU_n}$ ) ( $n = 2$  to 5) can be determined in the same way as when  $n = 1$ .

#### 1. 2 Overcharge hysteresis voltage n ( $V_{HC_n}$ )

Set  $V1 = V_{CU} + 0.05$  V,  $V2 = V3 = V4 = V5 = 2.5$  V. The overcharge hysteresis voltage 1 ( $V_{HC1}$ ) is the difference between  $V1$  voltage and  $V_{CU1}$  when the CO pin's output changes after the  $V1$  voltage has been gradually decreased.

Overcharge hysteresis voltage ( $V_{HC_n}$ ) ( $n = 2$  to 5) can be determined in the same way as when  $n = 1$ .

### 2. Output current

#### (Test circuit 5)

##### 2. 1 Output current of CMOS output product

Set SW1 and SW2 to OFF.

###### 2. 1. 1 Active "H"

###### (1) CO pin source current ( $I_{COH}$ )

Set SW1 to ON after setting  $V1 = 5.5$  V,  $V2$  to  $V5 = 3.0$  V,  $V6 = 0.5$  V.  $I1$  is the CO pin source current ( $I_{COH}$ ) at that time.

###### (2) CO pin sink current ( $I_{COL}$ )

Set SW2 to ON after setting  $V1$  to  $V5 = 3.5$  V,  $V7 = 0.5$  V.  $I2$  is the CO pin sink current ( $I_{COL}$ ) at that time.

###### 2. 1. 2 Active "L"

###### (1) CO pin source current ( $I_{COH}$ )

Set SW1 to ON after setting  $V1$  to  $V5 = 3.5$  V,  $V6 = 0.5$  V.  $I1$  is the CO pin source current ( $I_{COH}$ ) at that time.

###### (2) CO pin sink current ( $I_{COL}$ )

Set SW2 to ON after setting  $V1 = 5.5$  V,  $V2$  to  $V5 = 3.0$  V,  $V7 = 0.5$  V.  $I2$  is the CO pin sink current ( $I_{COL}$ ) at that time.

##### 2. 2 Output current of Nch open-drain output product

Set SW1 and SW2 to OFF.

###### 2. 2. 1 Active "H"

###### (1) CO pin leakage current "L" ( $I_{COLL}$ )

Set SW2 to ON after setting  $V1 = 5.5$  V,  $V2$  to  $V5 = 3.0$  V,  $V7 = 17.5$  V.  $I2$  is the CO pin leakage current "L" ( $I_{COLL}$ ) at that time.

###### (2) CO pin sink current ( $I_{COL}$ )

Set  $V1$  to  $V5 = 3.5$  V,  $V7 = 0.5$  V.  $I2$  is the CO pin sink current ( $I_{COL}$ ) at that time.

###### 2. 2. 2 Active "L"

###### (1) CO pin leakage current "L" ( $I_{COLL}$ )

Set SW2 to ON after setting  $V1$  to  $V5 = 3.5$  V,  $V7 = 17.5$  V.  $I2$  is the CO pin leakage current "L" ( $I_{COLL}$ ) at that time.

###### (2) CO pin sink current ( $I_{COL}$ )

Set  $V1 = 5.5$  V,  $V2$  to  $V5 = 3.0$  V,  $V7 = 0.5$  V.  $I2$  is the CO pin sink current ( $I_{COL}$ ) at that time.

## 2. 3 Output current of Pch open-drain output product

Set SW1 and SW2 to OFF.

### 2. 3. 1 Active "H"

#### (1) CO pin source current ( $I_{COH}$ )

Set SW1 to ON after setting  $V1 = 5.5$  V,  $V2$  to  $V5 = 3.0$  V,  $V6 = 0.5$  V.  $I1$  is the CO pin source current ( $I_{COH}$ ) at that time.

#### (2) CO pin leakage current "H" ( $I_{COLH}$ )

Set  $V1$  to  $V5 = 3.5$  V,  $V6 = 17.5$  V.  $I1$  is the CO pin leakage current "H" ( $I_{COLH}$ ) at that time.

### 2. 3. 2 Active "L"

#### (1) CO pin source current ( $I_{COH}$ )

Set SW1 to ON after setting  $V1$  to  $V5 = 3.5$  V,  $V6 = 0.5$  V.  $I1$  is the CO pin source current ( $I_{COH}$ ) at that time.

#### (2) CO pin leakage current "H" ( $I_{COLH}$ )

Set  $V1 = 5.5$  V,  $V2$  to  $V5 = 3.0$  V,  $V6 = 17.5$  V.  $I1$  is the CO pin leakage current "H" ( $I_{COLH}$ ) at that time.

## 3. Overcharge detection delay time ( $t_{CU}$ )

### (Test circuit 1)

Increase  $V1$  up to 5.0 V after setting  $V1 = V2 = V3 = V4 = V5 = 3.5$  V. The overcharge detection delay time ( $t_{CU}$ ) is the time period until the CO pin output changes.

## 4. Overcharge timer reset delay time ( $t_{TR}$ )

### (Test circuit 1)

Increase  $V1$  up to 5.0 V (first rise), and decrease  $V1$  down to 3.5 V within  $t_{CU}$  after setting  $V1 = V2 = V3 = V4 = V5 = 3.5$  V. After that, increase  $V1$  up to 5.0 V again (second rise), and detect the time period till the CO pin output changes. When the period from when  $V1$  has fallen to the second rise is short, CO pin output changes after  $t_{CU}$  has elapsed since the first rise. If the period is gradually made longer, CO pin output changes after  $t_{CU}$  has elapsed since the second rise. The overcharge timer reset delay time ( $t_{TR}$ ) is the period from  $V1$  fall till the second rise at that time.

## 5. Transition time to test mode ( $t_{TST}$ )

### (Test circuit 2)

Increase  $V6$  up to 5.0 V, and decrease  $V6$  again to 0 V after setting  $V1 = V2 = V3 = V4 = V5 = 3.5$  V, and  $V6 = 0$  V.

When the period from when  $V6$  was raised to when it has fallen is short, if an overcharge detection operation is performed subsequently, the delay time is  $t_{CU}$ . However, when the period from when  $V6$  is raised to when it has fallen is gradually made longer, the delay time during the subsequent overcharge detection operation is shorter than  $t_{CU}$ . The transition time to test mode ( $t_{TST}$ ) is the period from when  $V6$  was raised to when it has fallen at that time.

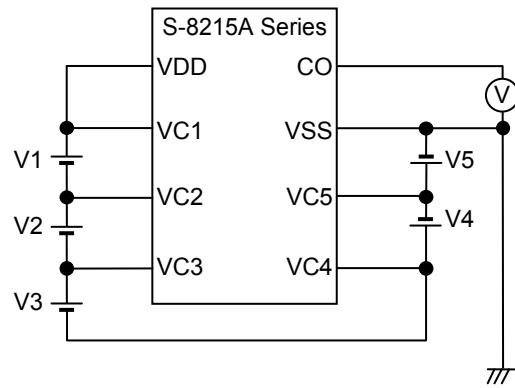


Figure 5 Test Circuit 1

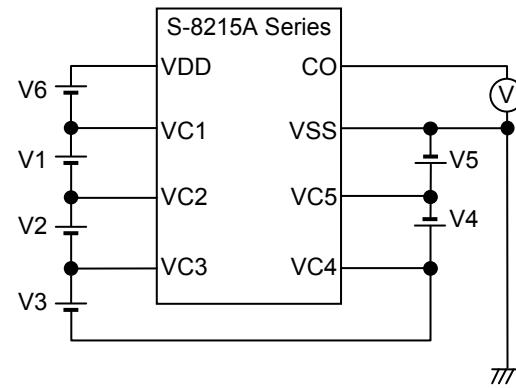


Figure 6 Test Circuit 2

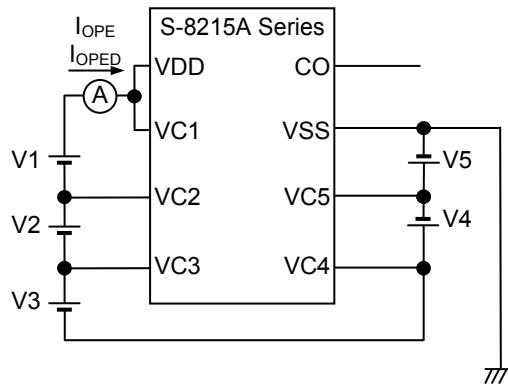


Figure 7 Test Circuit 3

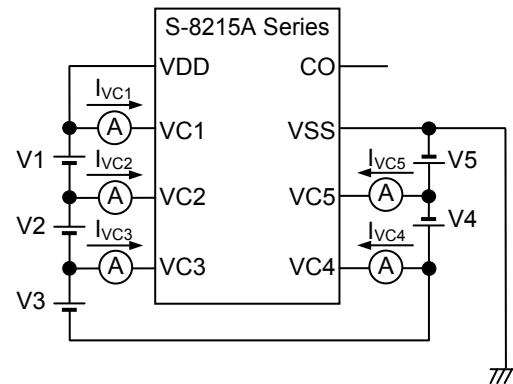


Figure 8 Test Circuit 4

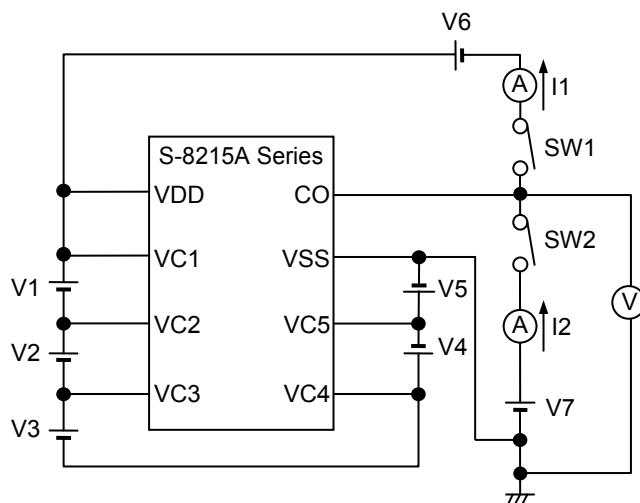


Figure 9 Test Circuit 5

## ■ Operation

**Remark** Refer to "■ Battery Protection IC Connection Examples".

### 1. Normal status

If the voltage of each of the batteries is lower than "the overcharge detection voltage n ( $V_{CUn}$ ) + the overcharge hysteresis voltage n ( $V_{HCn}$ )", the CO pin output changes to "L" (Active "H") or "H" (Active L"). This is called normal status.

### 2. Overcharge status

When the voltage of one of the batteries exceeds  $V_{CUn}$  during charging under normal conditions and the status is retained for the overcharge detection delay time ( $t_{CU}$ ) or longer, the CO pin output changes. This is called overcharge status. Connecting FET to the CO pin provides charge control and a second protection.

If the voltage of each of the batteries is lower than  $V_{CUn} + V_{HCn}$  and the status is retained for 2.0 ms typ. or longer, the S-8215A Series changes to normal status.

### 3. Overcharge timer reset function

When an overcharge release noise that forces the voltage of one of the batteries temporarily below  $V_{CUn}$  is input during  $t_{CU}$  from when  $V_{CUn}$  is exceeded to when charging is stopped,  $t_{CU}$  is continuously counted if the time the overcharge release noise persists is shorter than the overcharge timer reset delay time ( $t_{TR}$ ). Under the same conditions, if the time the overcharge release noise persists is  $t_{TR}$  or longer, counting of  $t_{CU}$  is reset once. After that, when  $V_{CUn}$  has been exceeded, counting  $t_{CU}$  resumes.

#### 4. Test mode

The overcharge detection delay time ( $t_{CU}$ ) can be shortened by entering the test mode.

The test mode can be set by retaining the VDD pin voltage 5.0 V or more higher than the VC1 pin voltage for the transition time to test mode ( $t_{TST}$ ) or longer. The status is retained by the internal latch and the test mode is retained even if the VDD pin voltage is decreased to the same voltage as that of the VC1 pin voltage.

After that, the latch for retaining the test mode is reset and the S-8215A Series exits from test mode under the overcharge status.

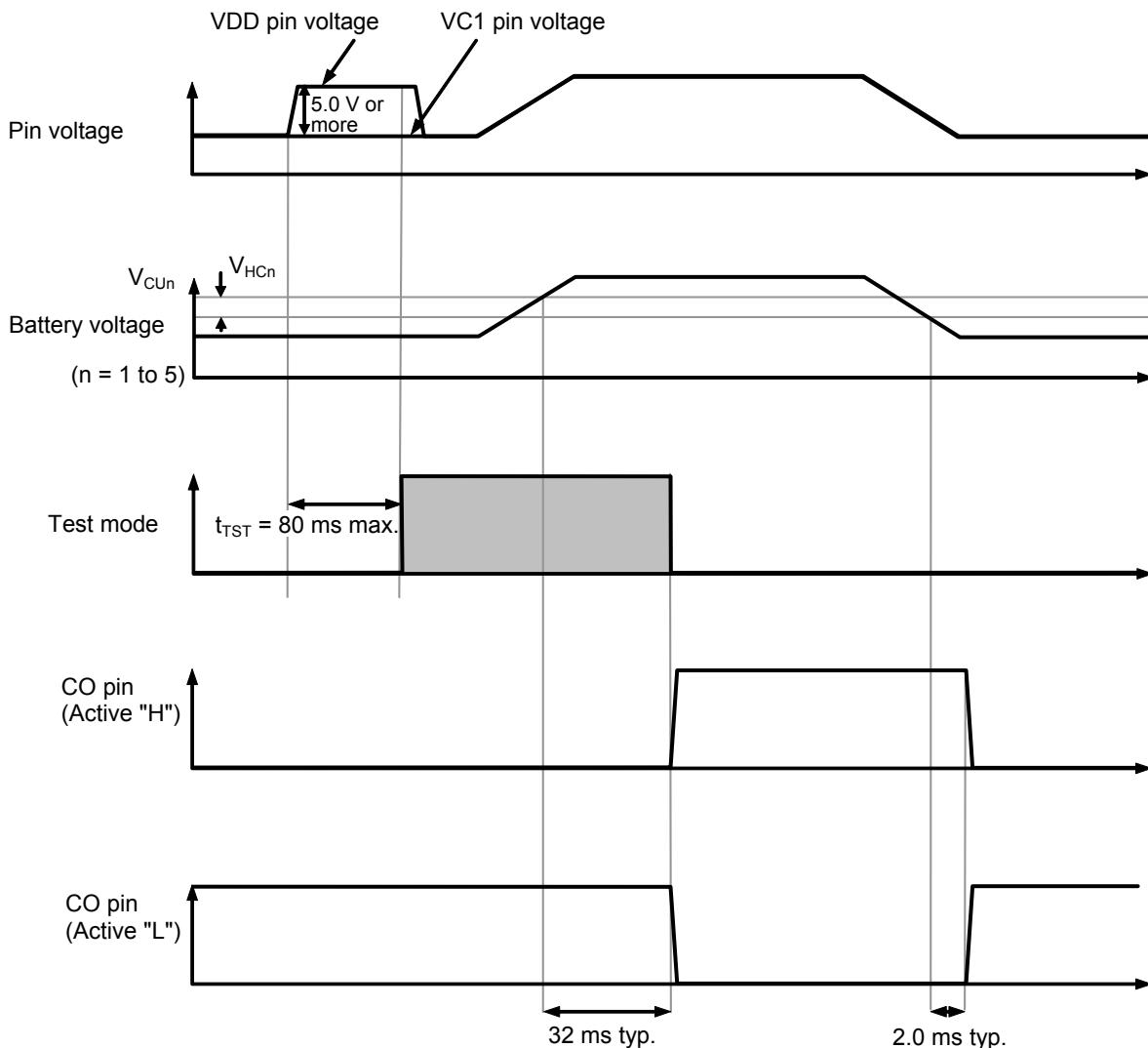


Figure 10

**Caution**

1. When the VDD pin voltage is decreased to lower than the UVLO voltage of 2 V typ., the S-8215A Series exits from test mode.
2. Set the test mode when no batteries are overcharged.
3. The overcharge timer reset delay time ( $t_{TR}$ ) is not shortened in the test mode.

■ Timing Charts

1. Overcharge detection operation

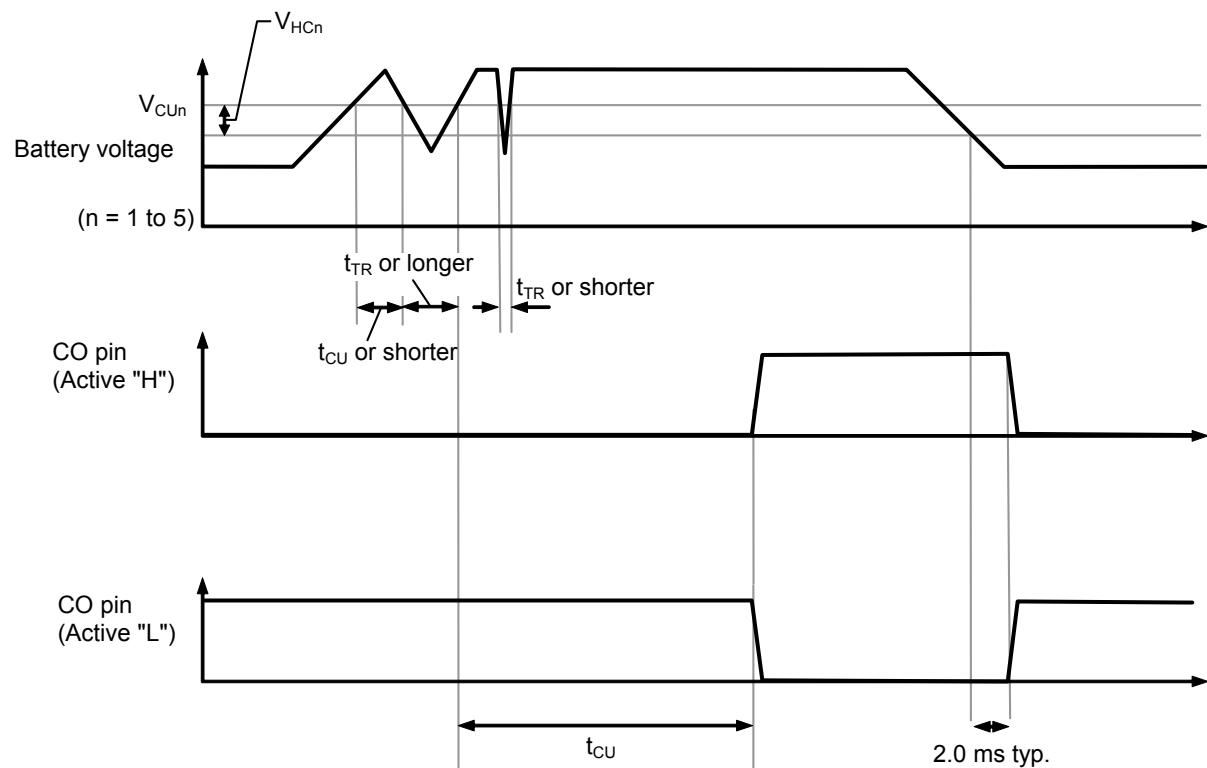


Figure 11

2. Overcharge timer reset operation

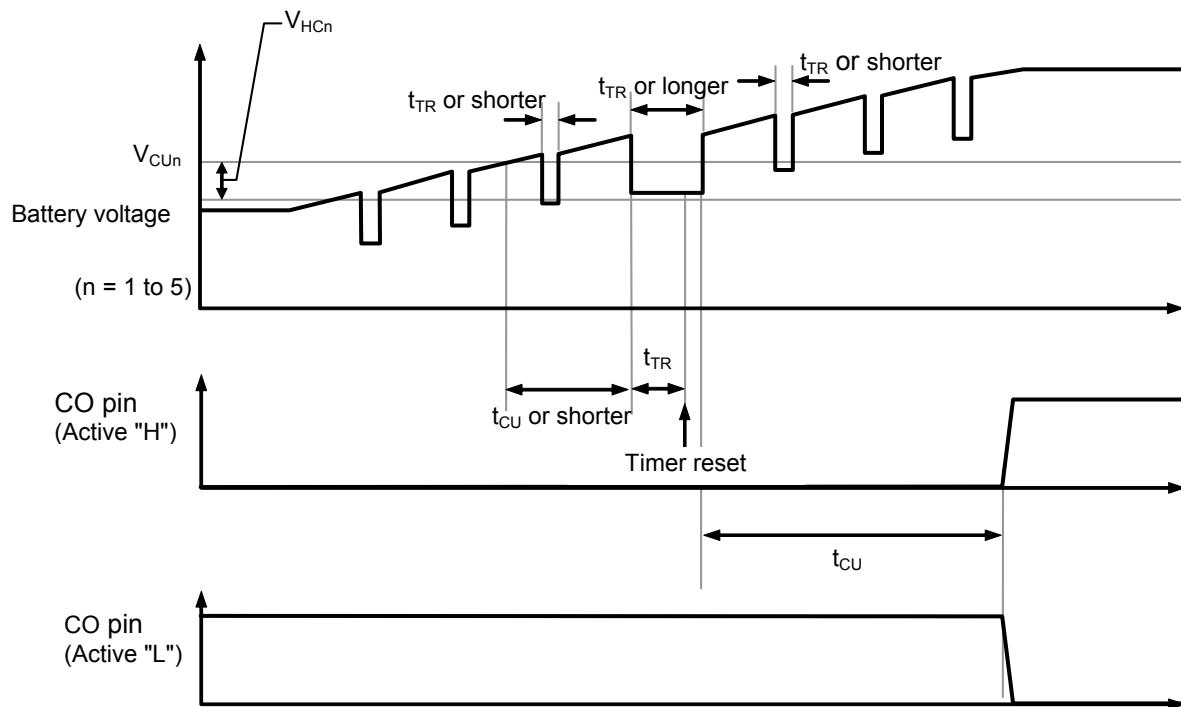


Figure 12

■ Battery Protection IC Connection Examples

1. 5-serial cell

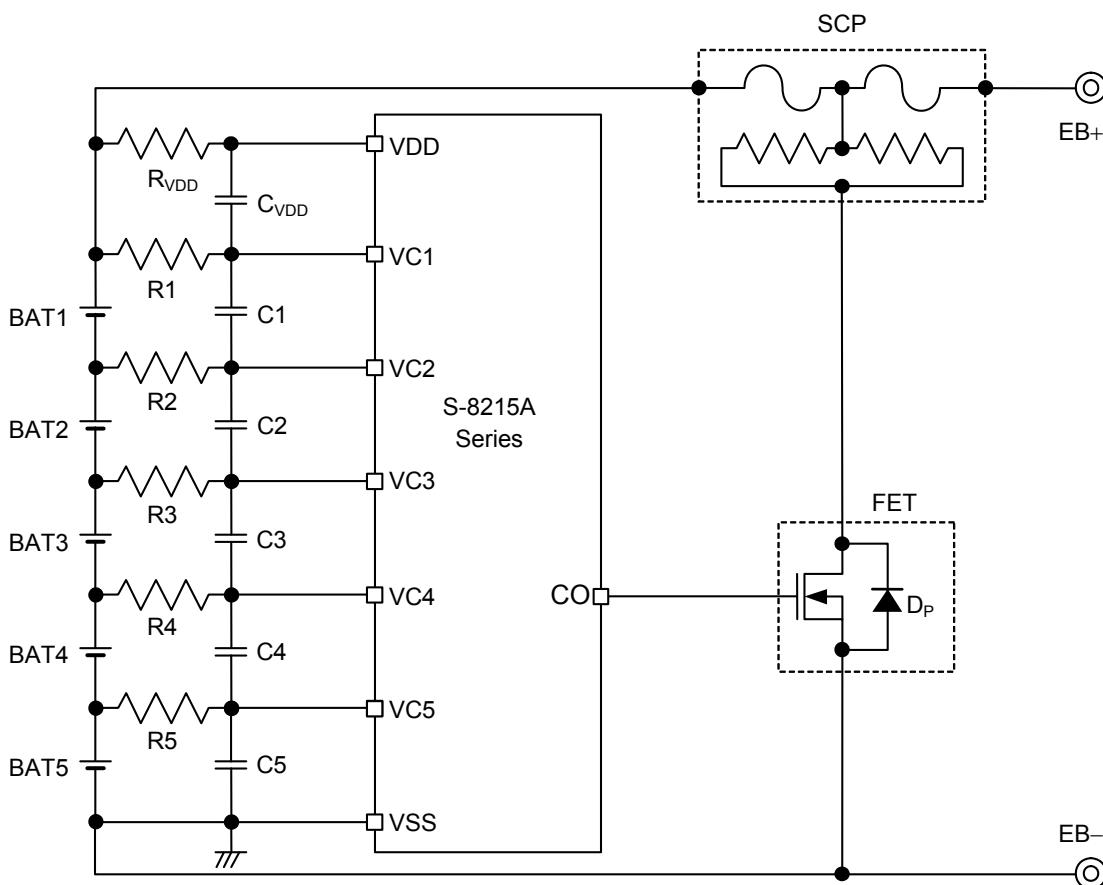


Figure 13

Table 8 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R5	0.5	1	10	kΩ
2	C1 to C5, CVDD	0.01	0.1	1	μF
3	RVDD	50	100	500	Ω

**Caution**

1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. R1 to R5 should be the same constant. C1 to C5 and CVDD should be the same constant.
4. Set RVDD, C1 to C5, and CVDD so that the condition  $(RVDD) \times (C1 to C5, CVDD) \geq 5 \times 10^{-6}$  is satisfied.
5. Set R1 to R5, C1 to C5, and CVDD so that the condition  $(R1 to R5) \times (C1 to C5, CVDD) \geq 1 \times 10^{-4}$  is satisfied.
6. Since the CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.

2. 4-serial cell

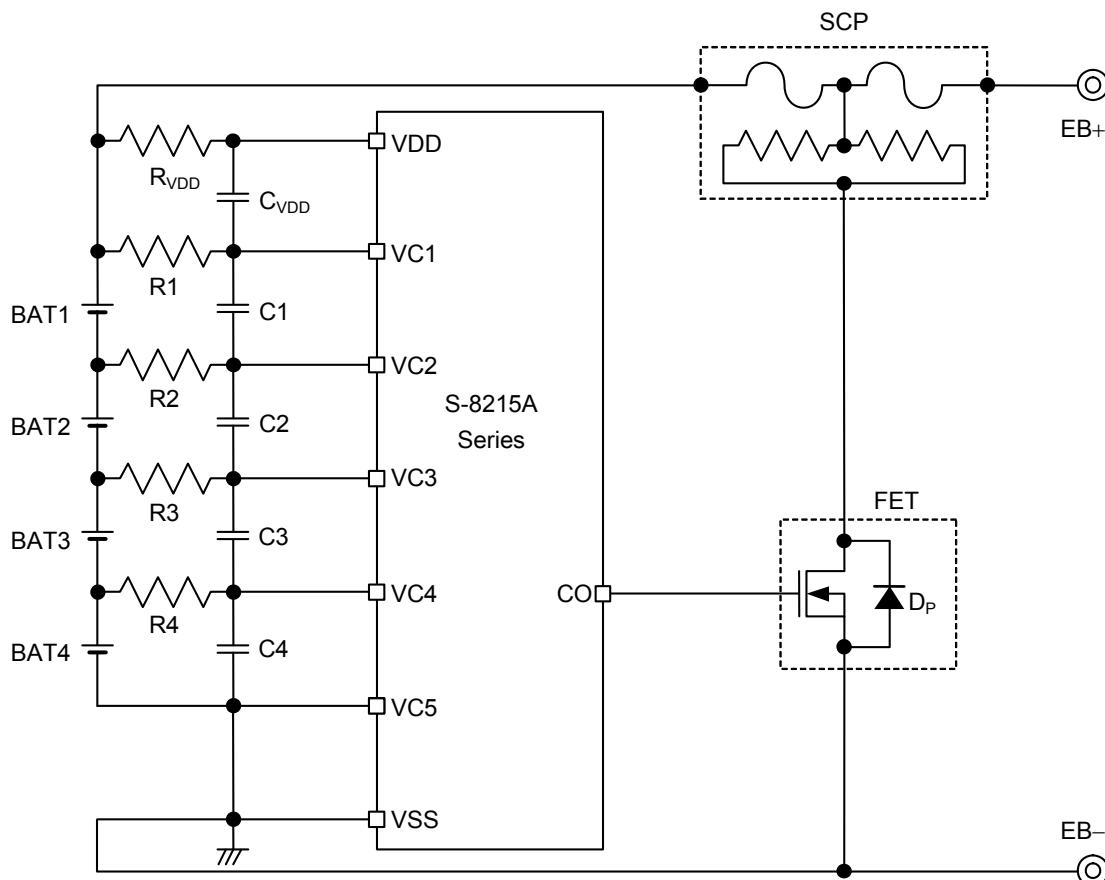


Figure 14

Table 9 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R4	0.5	1	10	kΩ
2	C1 to C4, C <sub>VDD</sub>	0.01	0.1	1	μF
3	R <sub>VDD</sub>	50	100	500	Ω

**Caution**

1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. R1 to R4 should be the same constant. C1 to C4 and C<sub>VDD</sub> should be the same constant.
4. Set R<sub>VDD</sub>, C1 to C4, and C<sub>VDD</sub> so that the condition  $(R_{VDD}) \times (C1 \text{ to } C4, C_{VDD}) \geq 5 \times 10^{-6}$  is satisfied.
5. Set R1 to R4, C1 to C4, and C<sub>VDD</sub> so that the condition  $(R1 \text{ to } R4}) \times (C1 \text{ to } C4, C_{VDD}) \geq 1 \times 10^{-4}$  is satisfied.
6. Since the CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.

3. 3-serial cell

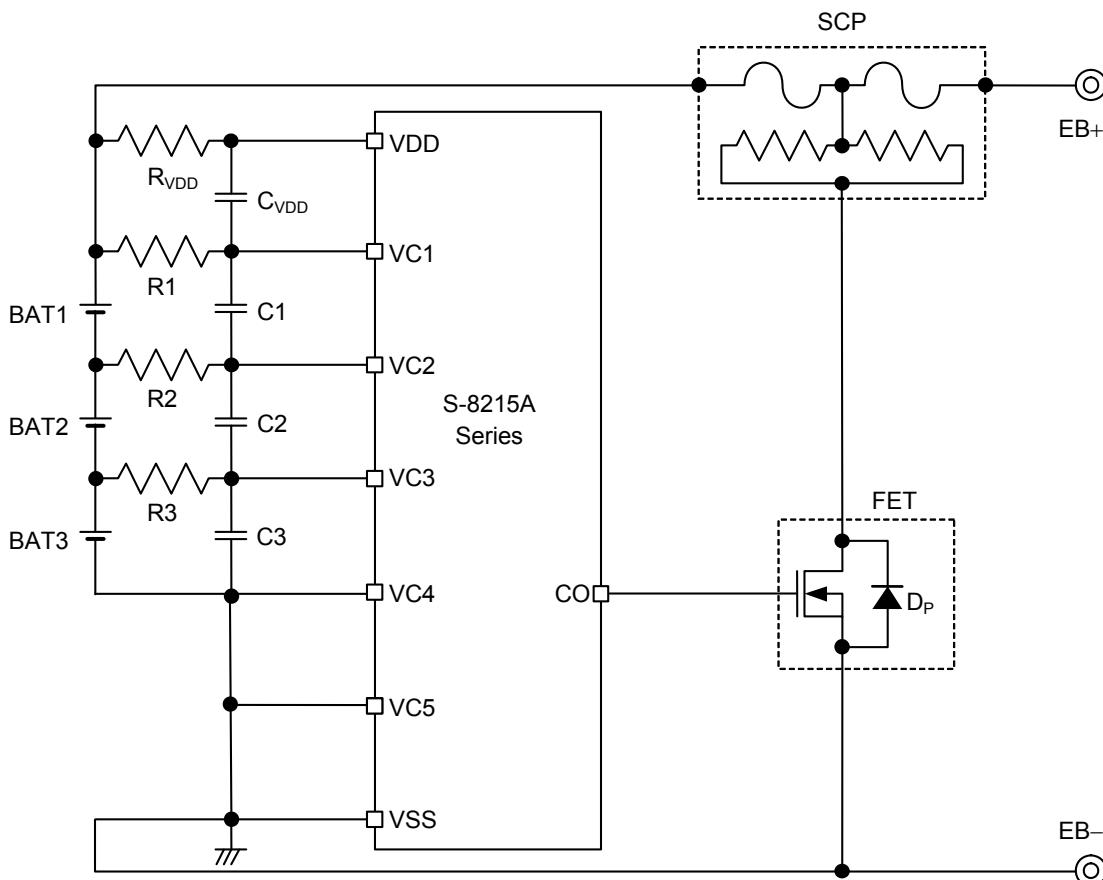


Figure 15

Table 10 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R3	0.5	1	10	kΩ
2	C1 to C3, CVDD	0.01	0.1	1	μF
3	RVDD	50	100	500	Ω

**Caution**

1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. R1 to R3 should be the same constant. C1 to C3 and CVDD should be the same constant.
4. Set RVDD, C1 to C3, and CVDD so that the condition  $(RVDD) \times (C1 to C3, CVDD) \geq 5 \times 10^{-6}$  is satisfied.
5. Set R1 to R3, C1 to C3, and CVDD so that the condition  $(R1 to R3) \times (C1 to C3, CVDD) \geq 1 \times 10^{-4}$  is satisfied.
6. Since the CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.

**[For SCP, contact]**

Global Sales & Marketing Division, Dexerials Corporation  
Gate City Osaki East Tower 8F, 1-11-2  
Osaki, Shinagawa-ku, Tokyo, 141-0032, Japan  
TEL +81-3-5435-3946  
Contact Us: <http://www.dexerials.jp/en/>

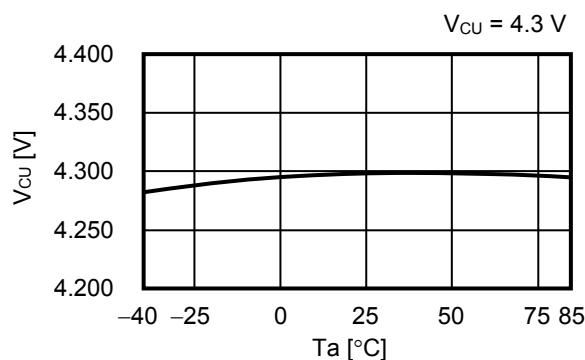
## ■ Precautions

- Do not connect batteries charged with  $V_{CUN} + V_{HCN}$  or higher. If the connected batteries include a battery charged with  $V_{CUN} + V_{HCN}$  or higher, the S-8215A series may become overcharge status after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- Before the battery connection, short-circuit the battery side pins  $R_{VDD}$  and  $R1$ , shown in the figure in "**■ Battery Protection IC Connection Examples**".
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

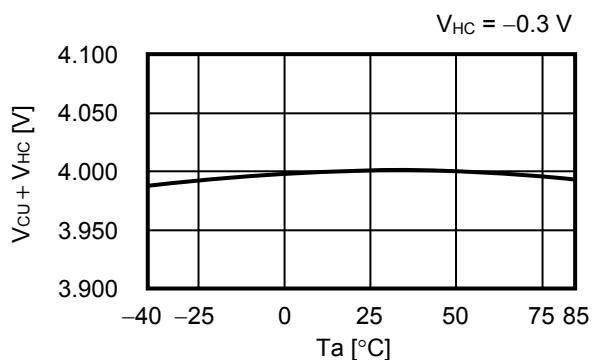
■ Characteristics (Typical Data)

1. Detection voltage

1. 1  $V_{CU}$  vs.  $T_a$

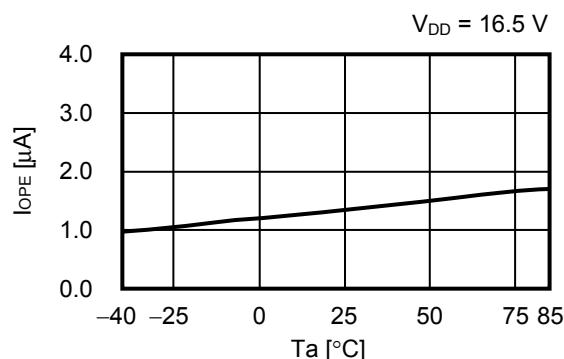


1. 2  $V_{CU} + V_{HC}$  vs.  $T_a$

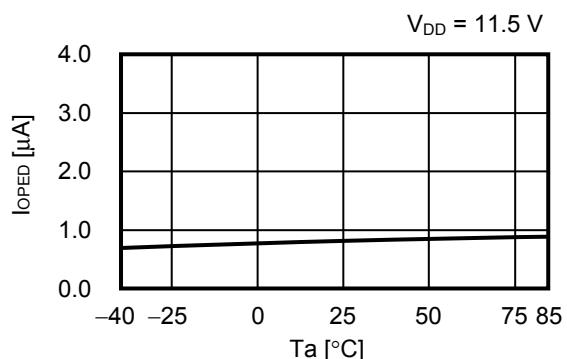


2. Current consumption

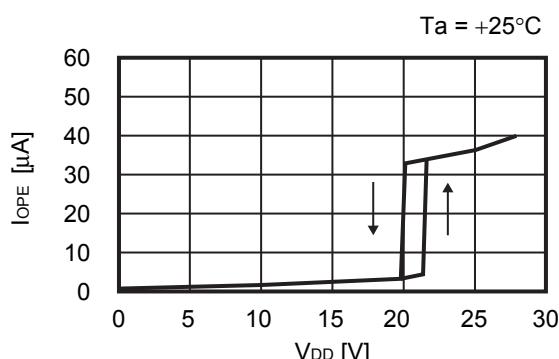
2. 1  $I_{OPE}$  vs.  $T_a$



2. 2  $I_{OPED}$  vs.  $T_a$

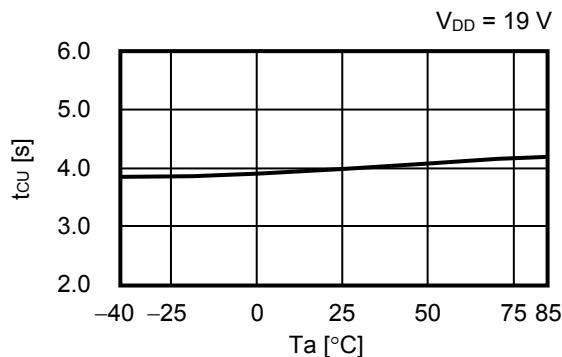


2. 3  $I_{OPE}$  vs.  $V_{DD}$



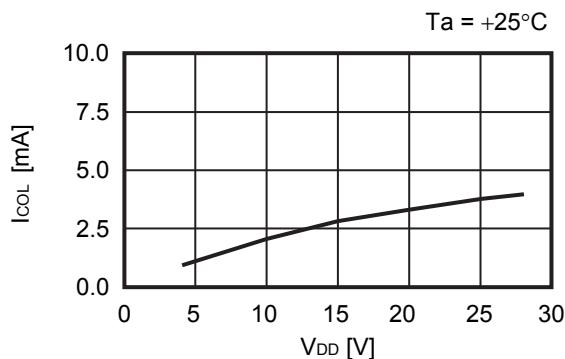
### 3. Delay time

#### 3. 1 $t_{CU}$ vs. $T_a$

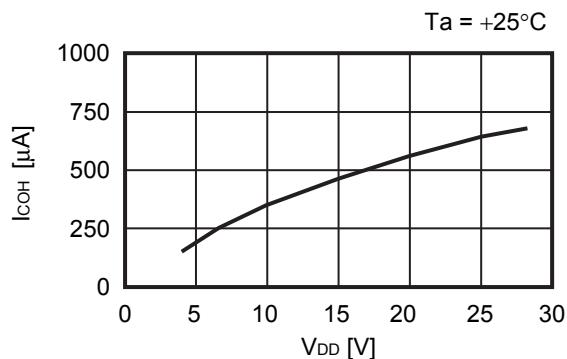


### 4. Output current

#### 4. 1 $I_{COL}$ vs. $V_{DD}$

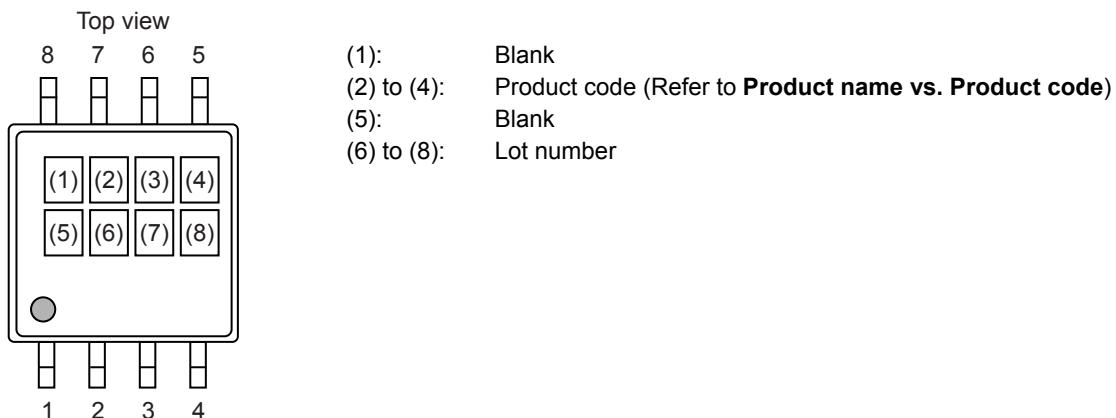


#### 4. 2 $I_{COH}$ vs. $V_{DD}$



**■ Marking Specifications**

**1. TMSOP-8**

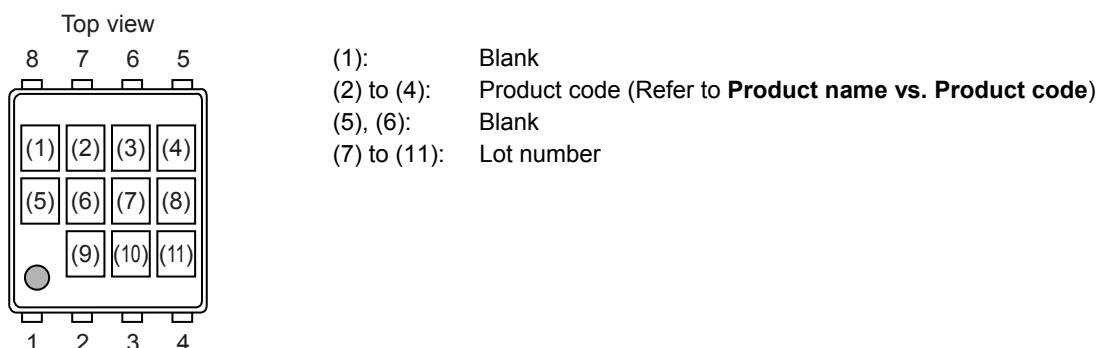


**Product name vs. Product code**

Product Name	Product Code		
	(2)	(3)	(4)
S-8215AAA-K8T2U	V	6	A
S-8215AAB-K8T2U	V	6	B
S-8215AAC-K8T2U	V	6	C
S-8215AAD-K8T2U	V	6	D
S-8215AAE-K8T2U	V	6	E
S-8215AAF-K8T2U	V	6	F
S-8215AAH-K8T2U	V	6	H
S-8215AAI-K8T2U	V	6	I
S-8215AAJ-K8T2U	V	6	J
S-8215AAK-K8T2U	V	6	K

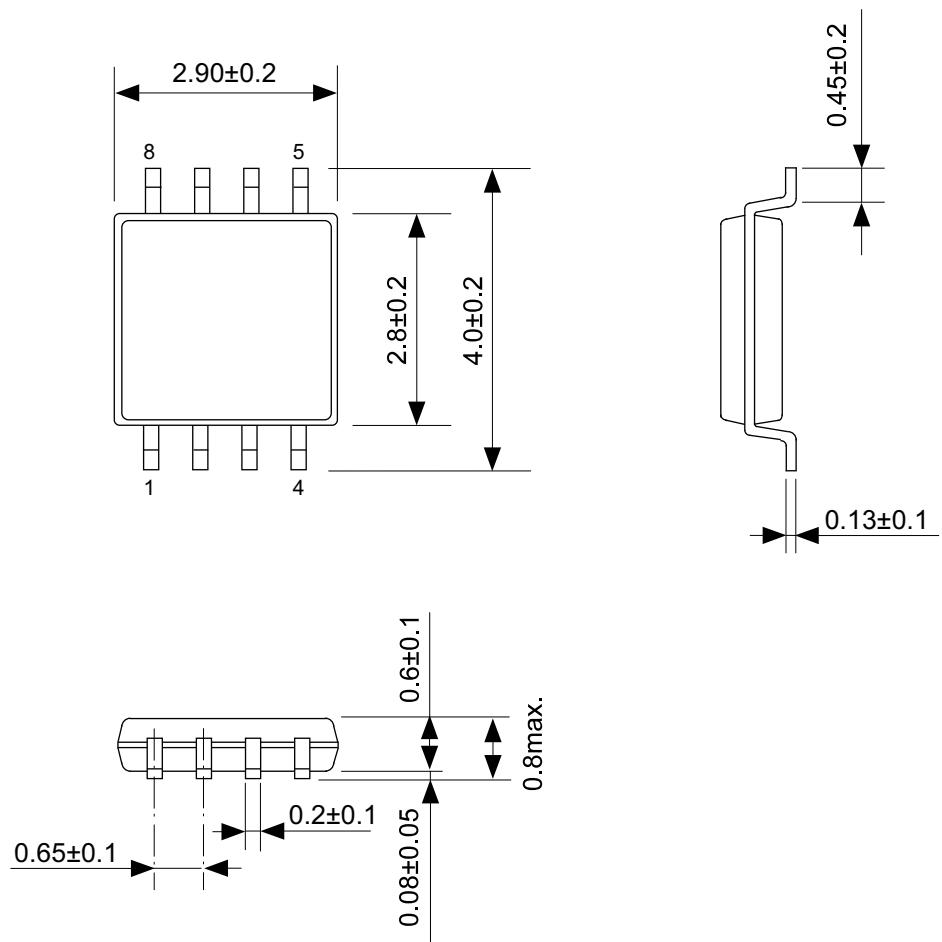
Product Name	Product Code		
	(2)	(3)	(4)
S-8215AAL-K8T2U	V	6	L
S-8215AAM-K8T2U	V	6	M
S-8215AAN-K8T2U	V	6	N
S-8215AAO-K8T2U	V	6	O
S-8215AAP-K8T2U	V	6	P
S-8215AAQ-K8T2U	V	6	Q
S-8215AAR-K8T2U	V	6	R
S-8215AAS-K8T2U	V	6	S
S-8215AAT-K8T2U	V	6	T
S-8215AAU-K8T2U	V	6	U
S-8215AAV-K8T2U	V	6	V

**2. SNT-8A**



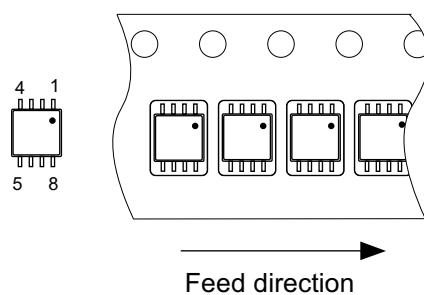
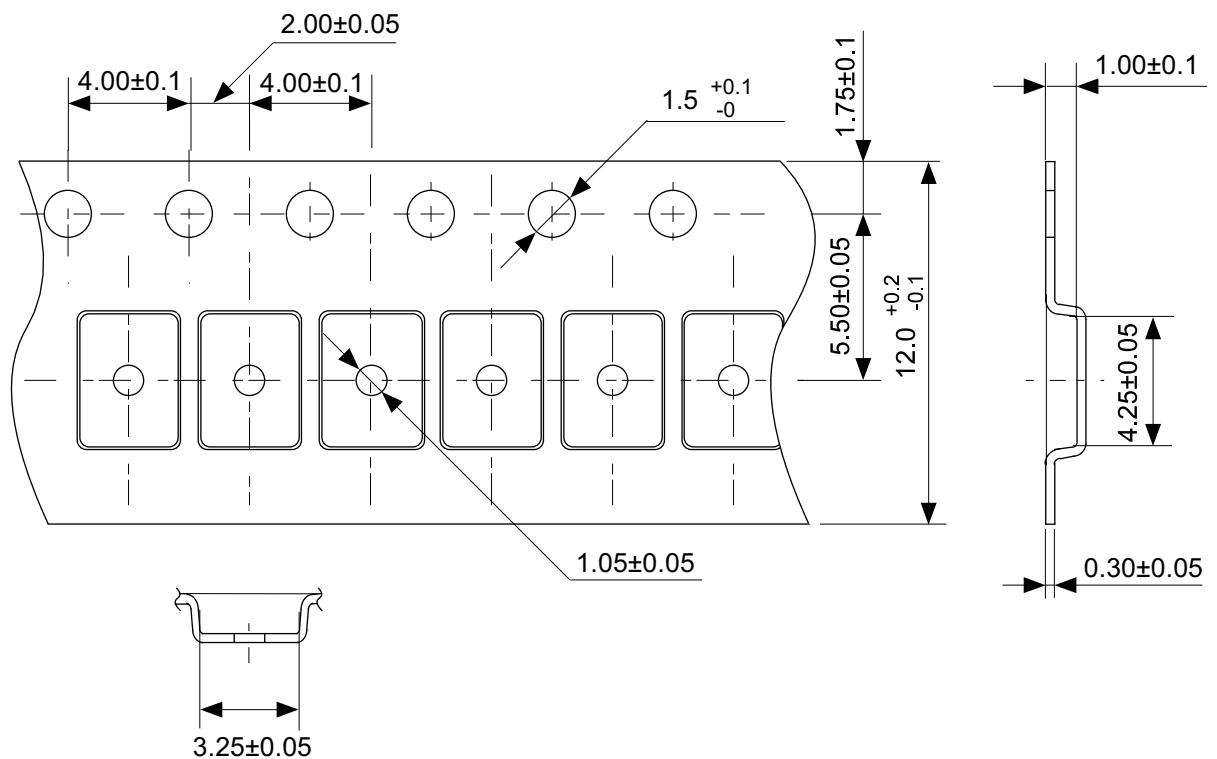
**Product name vs. Product code**

Product Name	Product Code		
	(2)	(3)	(4)
S-8215AAA-I8T1U	V	6	A
S-8215AAG-I8T1U	V	6	G
S-8215AAV-I8T1U	V	6	V



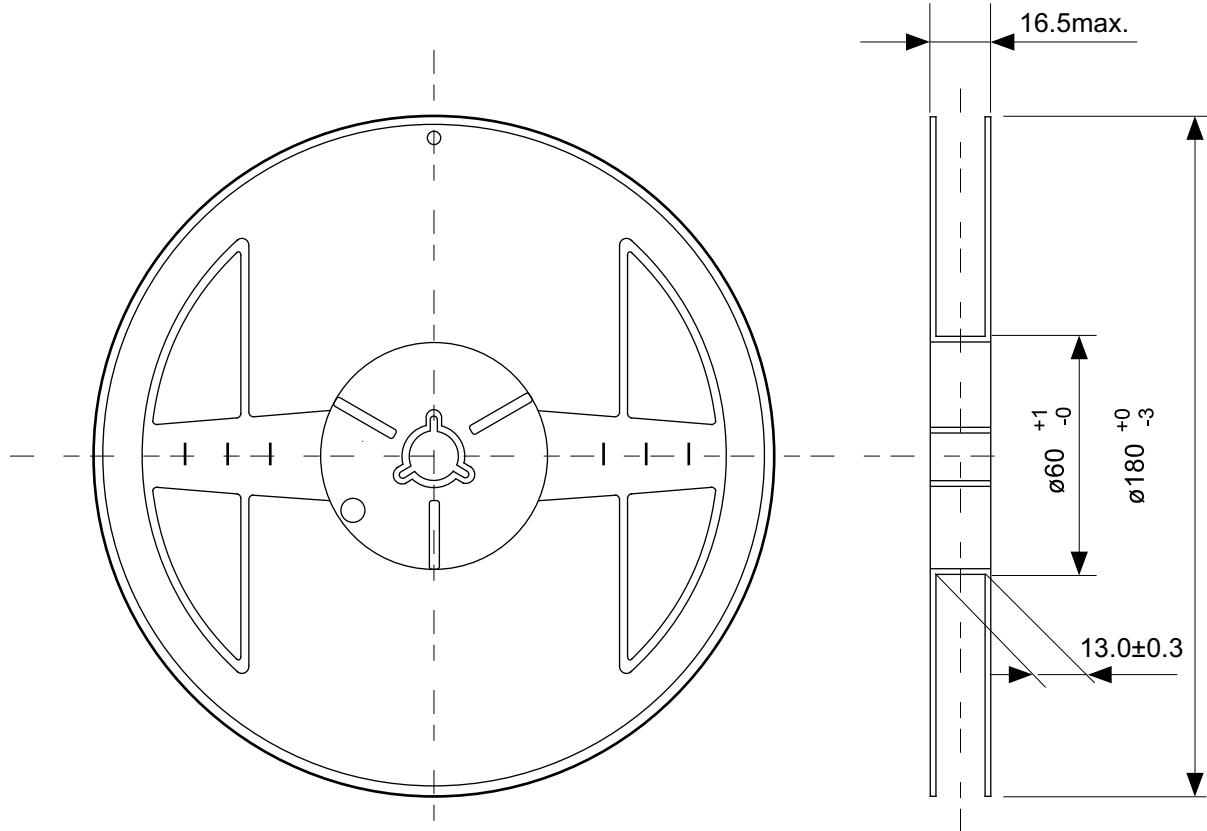
No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	⊕
UNIT	mm
	ABLIC Inc.

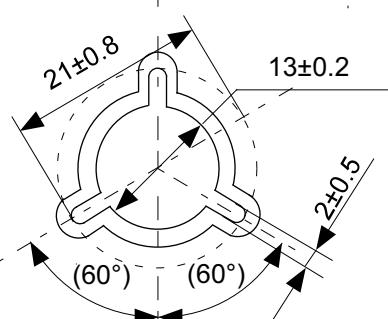


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

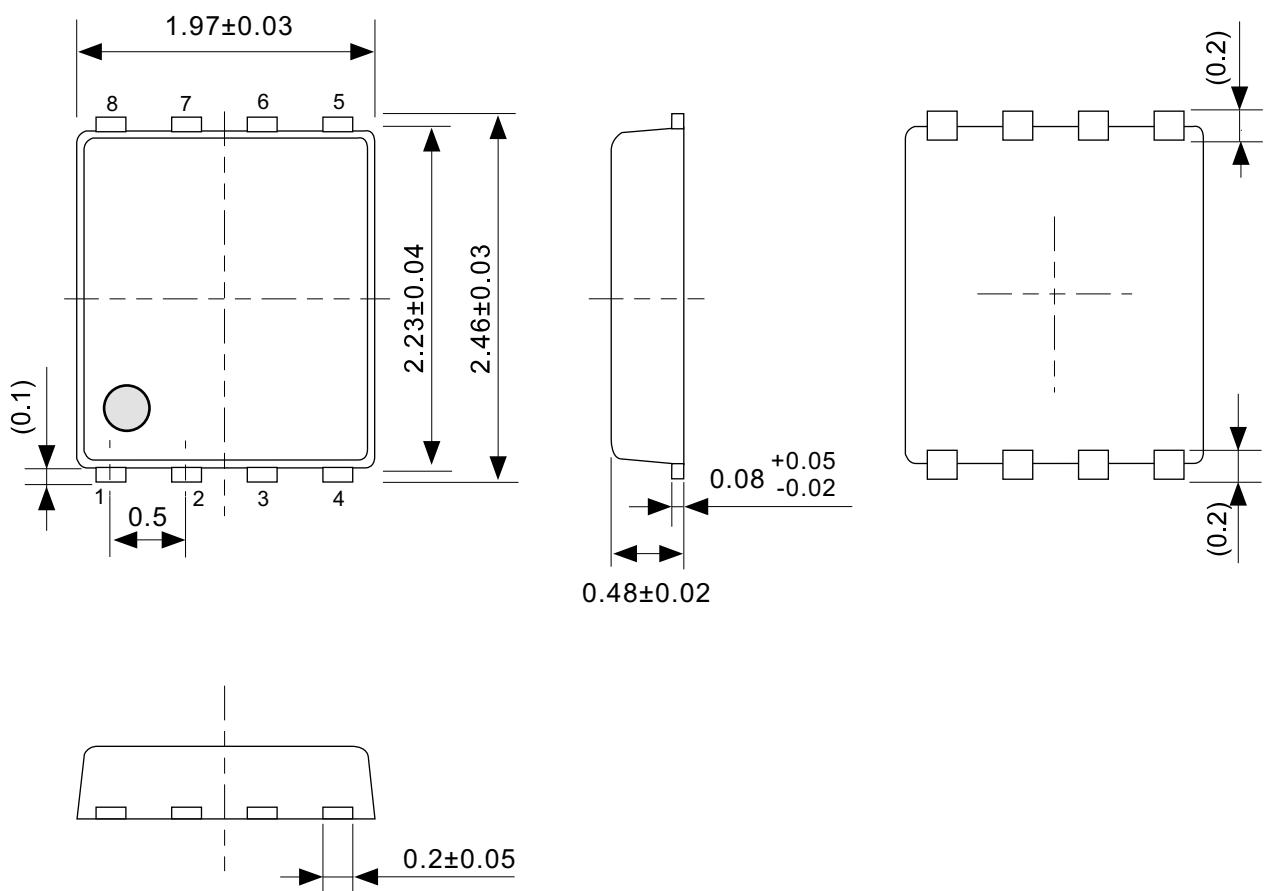


Enlarged drawing in the central part



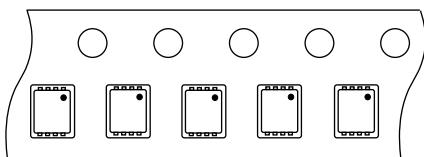
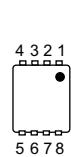
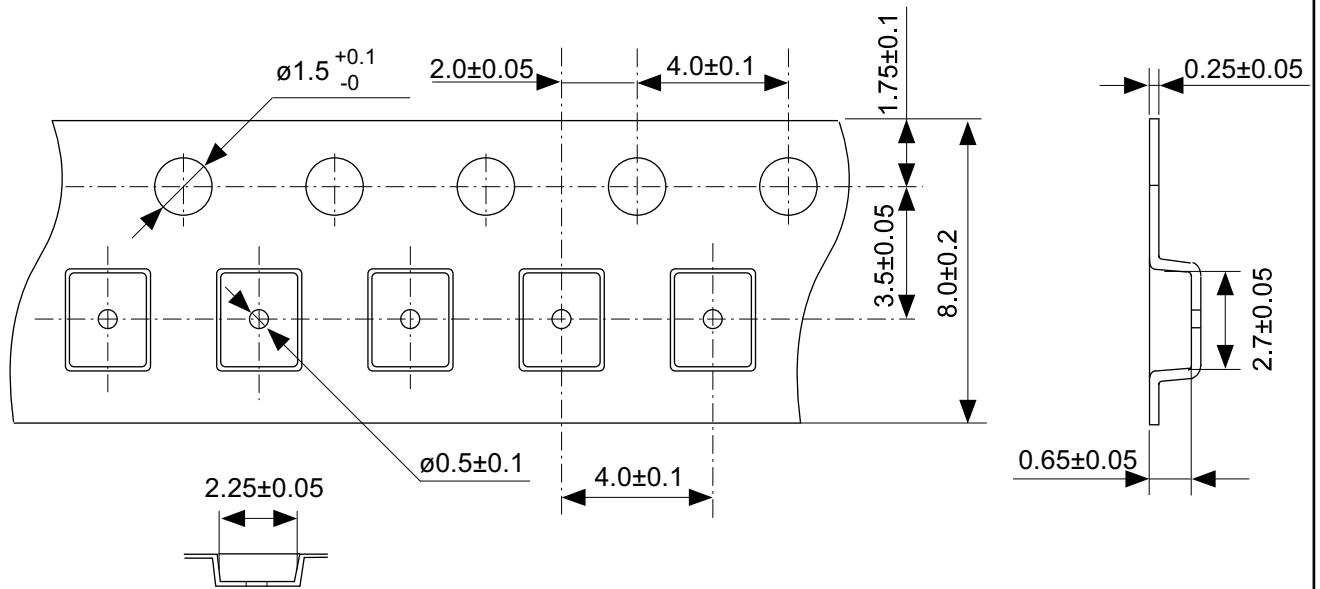
No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	<u>FM008-A-R-SD-1.0</u>		
ANGLE		QTY.	4,000
UNIT	mm		
	ABLIC Inc.		



No. PH008-A-P-SD-2.1

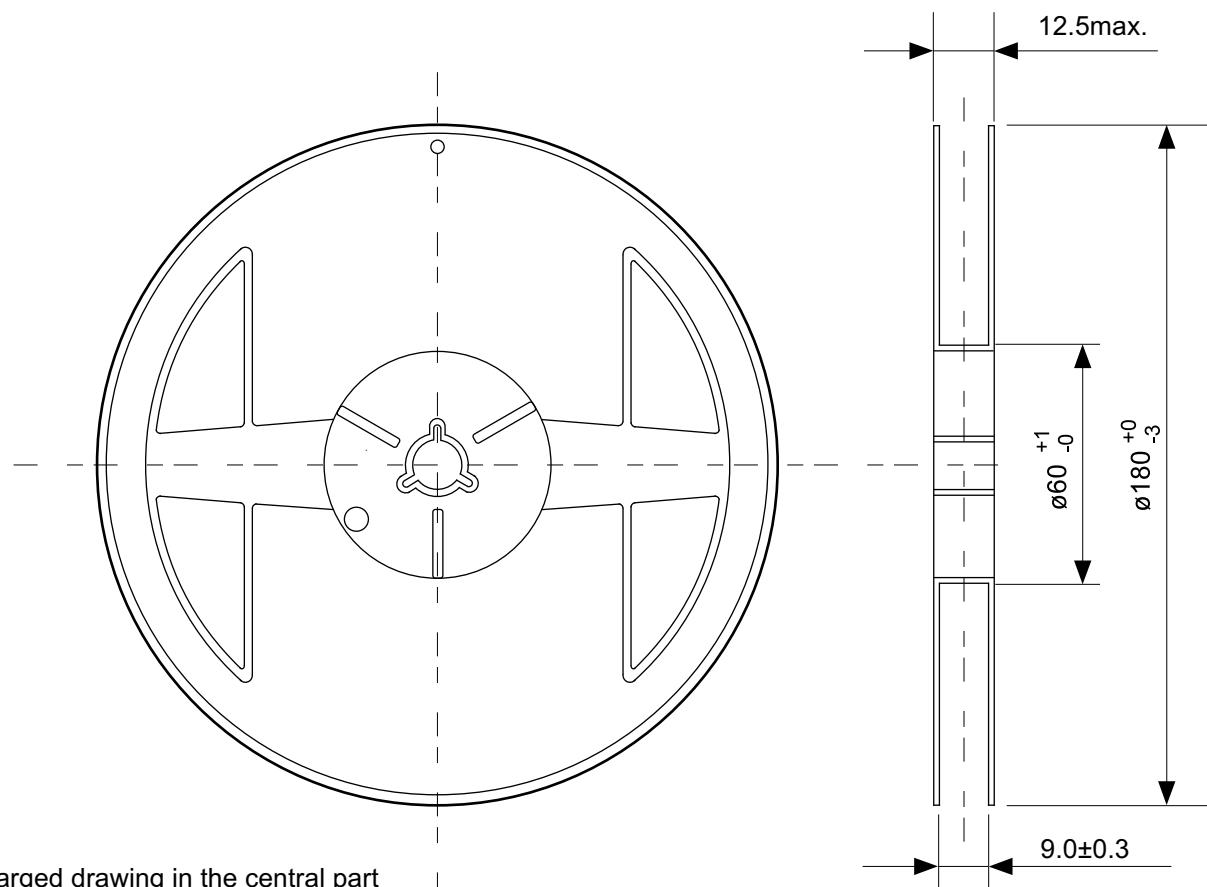
TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



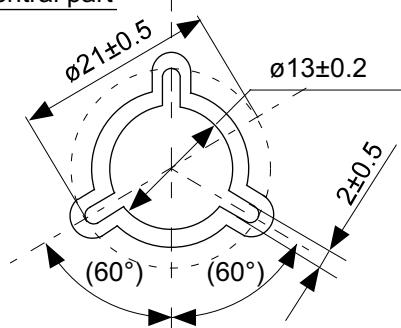
Feed direction

No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

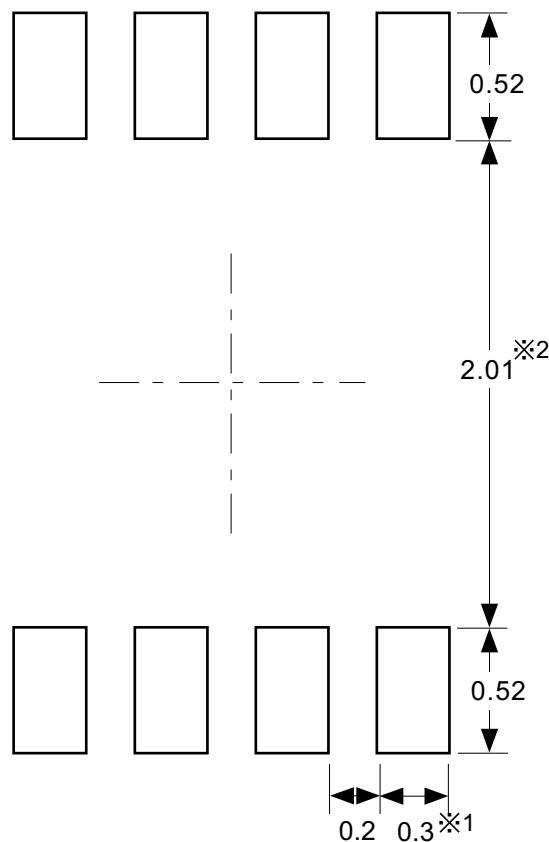


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。

※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。  
 2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm  
 以下にしてください。  
 3. マスク開口サイズと開口位置はランドパターンと合わせてください。  
 4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).

※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.  
 2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm  
 or less from the land pattern surface.  
 3. Match the mask aperture size and aperture position with the land pattern.  
 4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。

※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。  
 2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。  
 3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。  
 4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.  
ABLIC Inc. is not responsible for damages caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not responsible for damages caused by the incorrect information described herein.
4. Be careful to use the products within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.  
ABLIC Inc. is not responsible for damages caused by failures and / or accidents, etc. that occur due to the use of the products outside their specified ranges.
5. When using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not apply the products to the above listed devices and equipments without prior written permission by ABLIC Inc. Especially, the products cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.  
Prior consultation with our sales office is required when considering the above uses.  
ABLIC Inc. is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.  
The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.  
The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc.  
The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party without the express permission of ABLIC Inc. is strictly prohibited.
14. For more details on the information described herein, contact our sales office.

2.2-2018.06