

HIGH SPEED PWM CONTROLLER

FEATURES

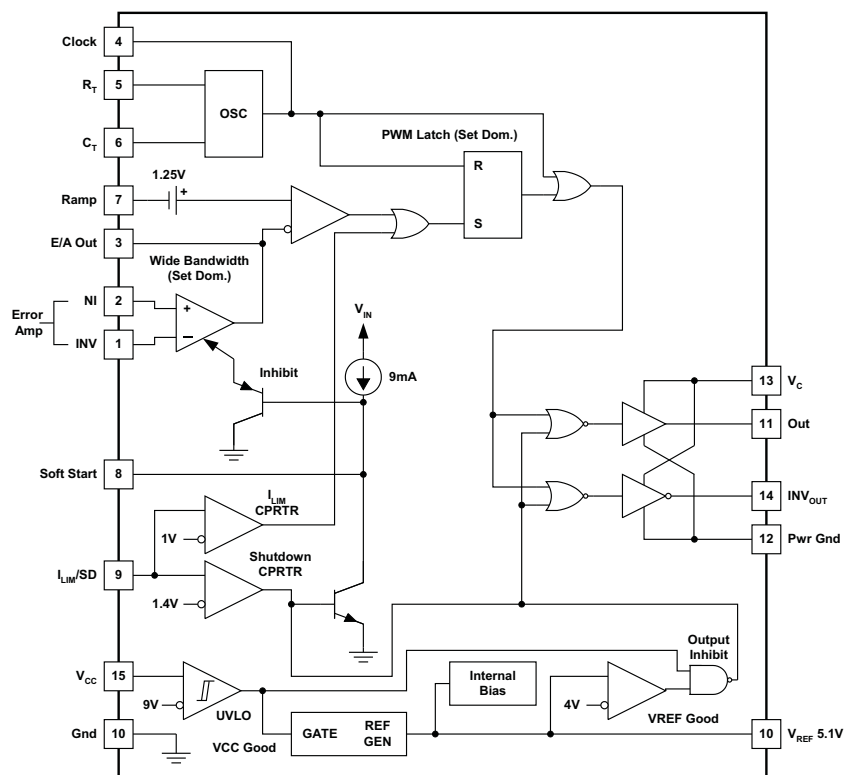
- Complementary Outputs
- Practical Operation Switching Frequencies to 1 MHz
- 50-ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5 A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic With Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Maximum Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1 mA)
- Trimmed Bandgap Reference (5.1 V $\pm$ 1%)

DESCRIPTION

The UC1824 family of PWM control devices is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft-start pin which doubles as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800 mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION (CONTINUED)

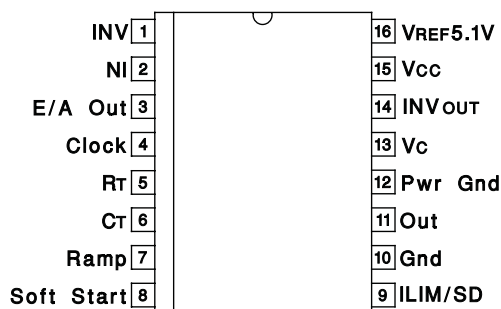
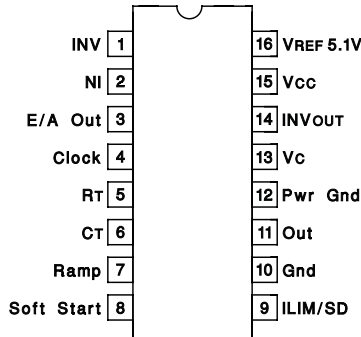
These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

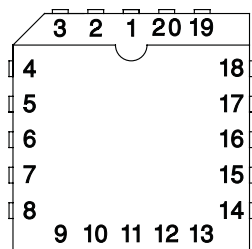
	VALUE	UNIT
Supply voltage (pins 13, 15)	30	V
Output current, source or sink (pins 11, 14)		
DC	0.5	A
Pulse (0.5 ms)	2	
Analog inputs		
(Pins 1, 2, 7)	–0.3 TO 7	V
(Pin 8, 9)	–0.3 TO 6	
Clock output current (pin 4)	–5	mA
Error amplifier output current (pin 3)	5	
Soft start sink current (pin 8)	20	
Oscillator charging current (pin 5)	–5	
Power dissipation	1	W
Storage temperature range	–65 to 150	°C
Lead temperature (soldering, 10 seconds)	300	

(1) All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

(2) Consult Unitorde Integrated Circuit Databook for thermal limitations and considerations of package.

**SOIC-16
DW PACKAGE
(TOP VIEW)****DIL-16
J OR N PACKAGE
(TOP VIEW)**

**PLCC-20 AND LCC-20
 Q AND L PACKAGES
 (TOP VIEW)**



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
R _T	7
C _T	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out	14
Pwr Gnd	15
N/C	16
V _c	17
INVOUT	18
V _{CC}	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for, $R_T = 3.65k\Omega$, $C_T = 1\text{ nF}$, $V_{CC} = 15\text{ V}$, $-55^\circ\text{C} < T_A < 125^\circ\text{C}$ for the UC1824, $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ for the UC2824, and $0^\circ\text{C} < T_A < 70^\circ\text{C}$ for the UC3824, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1824 UC2824			UC3824			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output voltage	T _J = 25°C, I _O = 1 mA	5.05	5.10	5.15	5	5.10	5.20	V
Line regulation	10 V < V _{CC} < 30 V		2	20		2	20	mV mV
Load regulation	1 mA < I _O < 10 mA		5	20		5	20	
Temperature stability ⁽¹⁾	T _{MIN} < T _A < T _{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total output variation ⁽¹⁾	Line, Load, Temperature	5		5.20	4.95		5.25	V
Output noise voltage ⁽¹⁾	10 Hz < f < 10 kHz		50			50		μV
long term stability ⁽¹⁾	T _J = 125°C, 1000 hrs.		5	25		5	25	mV
Short circuit current	V _{REF} = 0 V	−15	−50	−100	−15	−50	−100	mA
Oscillator Section								
Initial accuracy ⁽¹⁾	T _J = 25°C	360	400	440	360	400	440	kHz
Voltage stability ⁽¹⁾	10 V < V _{CC} < 30 V		0.2%	2%		0.2%	2%	
Temperature stability ⁽¹⁾	T _{MIN} < T _A < T _{MAX}		5%			5%		
Total variation ⁽¹⁾	Line, Temperature	340		460	340		460	kHz
Clock out high		3.9	4.5		3.9	4.5		V
Clock out low			2.3	2.9		2.3	2.9	
Ramp peak ⁽¹⁾		2.6	2.8	3	2.6	2.8	3	
Ramp valley ⁽¹⁾		0.7	1	1.25	0.7	1	1.25	
Ramp valley to peak ⁽¹⁾		1.6	1.8	2	1.6	1.8	2	
Error Amplifier Section								
Input offset voltage				10			15	mV
Input bias current			0.6	3		0.6	3	μA
Input offset current			0.1	1		0.1	1	μA
Open loop gain	1 V < V _O < 4 V	60	95		60	95		dB
CMRR	1.5 V < V _{CM} < 5.5 V	75	95		75	95		
PSRR	10 V < V _{CC} < 30 V	85	110		85	110		
Output sink current	V _{PIN 3} = 1 V	1	2.5		1	2.5		mA
Output source current	V _{PIN 3} = 4 V	−0.5	−1.3		−0.5	−1.3		
Output high voltage	I _{PIN 3} = −0.5 mA	4	4.7	5	4	4.7	5	V
Output low voltage	I _{PIN 3} = 1 mA	0	0.5	1	0	0.5	1	
Unity gain bandwidth ⁽¹⁾		3	5.5		3	5.5		MHz
Slew rate ⁽¹⁾		6	12		6	12		V/μs
PWM Comparator Section								
Pin 7 bias current	V _{PIN 7} = 0 V		−1	−5		−1	−5	μA
Duty cycle range		0		80	0		85	%
Pin 3 zero dc threshold	V _{PIN 7} = 0 V	1.1	1.25		1.1	1.25		V
Delay to output ⁽¹⁾			50	80		50	80	ns
Soft-Start Section								
Charge current	V _{PIN 8} = 0.5 V	3	9	20	3	9	20	μA
Discharge current	V _{PIN 8} = 1 V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 bias current	0 < V _{PIN 9} < 4 V			15			10	μA

(1) This parameter not 100% tested in production but guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for, $R_T = 3.65k$, $C_T = 1\text{ nF}$, $V_{CC} = 15\text{ V}$, $-55^\circ\text{C} < T_A < 125^\circ\text{C}$ for the UC1824, $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ for the UC2824, and $0^\circ\text{C} < T_A < 70^\circ\text{C}$ for the UC3824, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1824 UC2824			UC3824			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Current limit threshold		0.9	1	1.1	0.9	1	1.1	V
Shutdown threshold		1.25	1.40	1.55	1.25	1.40	1.55	
Delay to output			50	80		50	80	ns
Output Section								
Output low level	I _{OUT} = 20 mA		0.25	0.40		0.25	0.40	V
	I _{OUT} = 200 mA		1.2	2.2		1.2	2.2	
Output high level	I _{OUT} = −20 mA	13	13.5		13	13.5		
	I _{OUT} = −200 mA	12	13		12	13		
Collector leakage	V _C = 30 V		100	500		10	500	μA
Rise/fall time ⁽²⁾	CL = 1 nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	
Supply Current Section								
Start up current	V _{CC} = 8 V		1.1	2.5		1.1	2.5	mA
ICC	V _{PIN 1} , V _{PIN 7} , V _{PIN 9} = 0 V; V _{PIN 2} = 1 V		22	33		22	33	

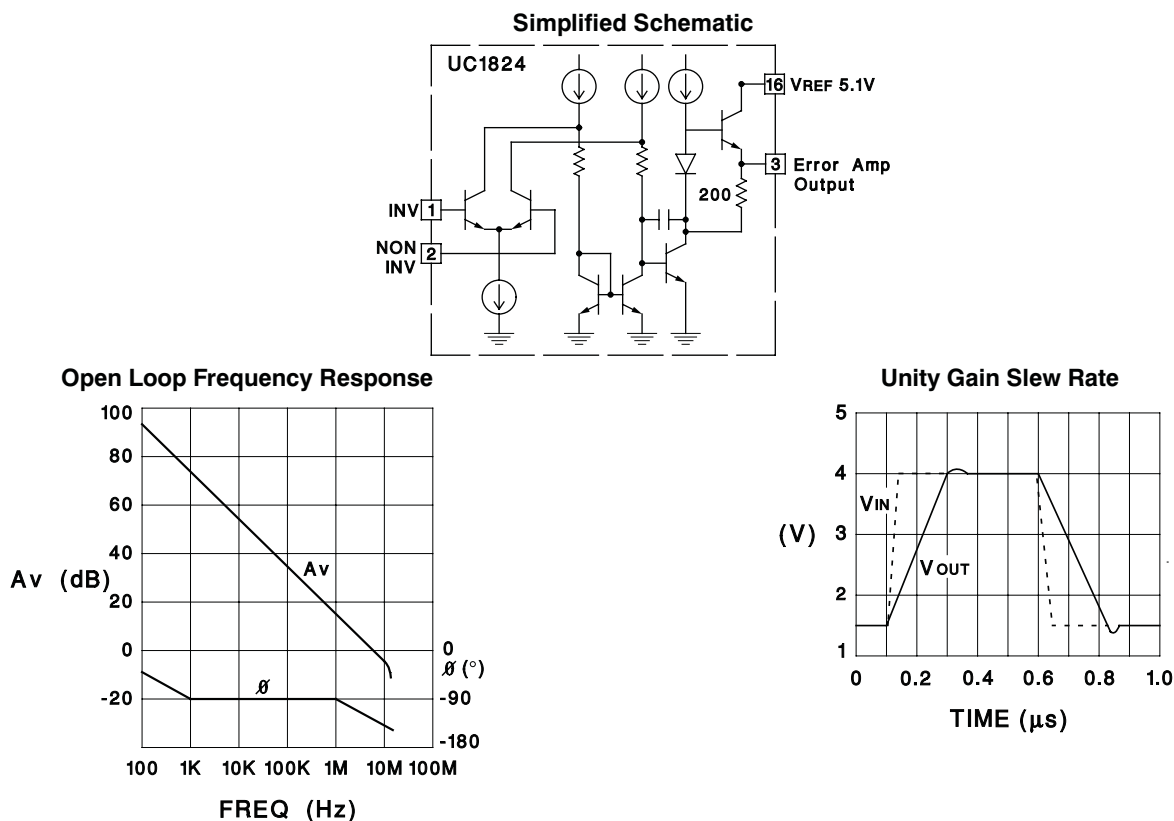
(2) This parameter not 100% tested in production but guaranteed by design.

UC1824 Printed Circuit Board Layout Considerations

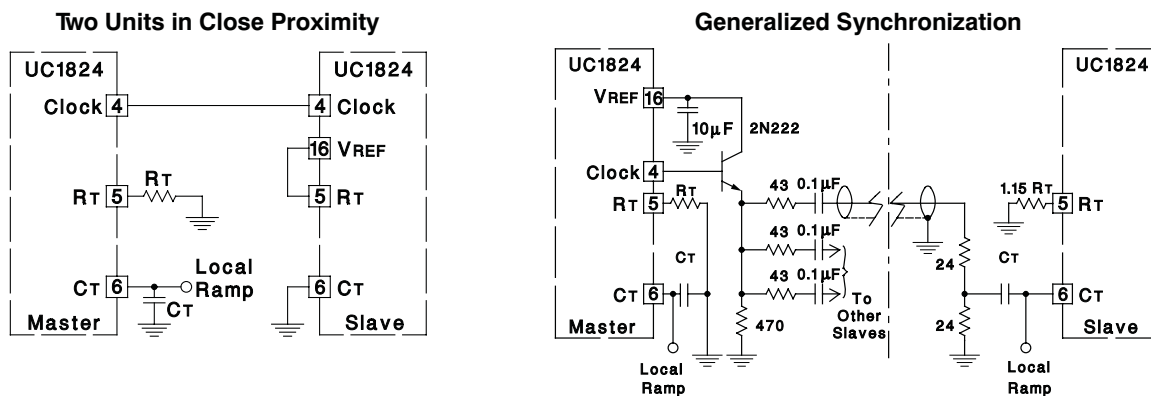
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1824 follow these rules:

1. Use a ground plane.
2. Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1-A Schottky diode at the output pin serves this purpose.
3. Bypass V_{CC} , V_C , and V_{REF} . Use 0.1- μF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane.
4. Treat the timing capacitor, C_T , like a bypass capacitor.

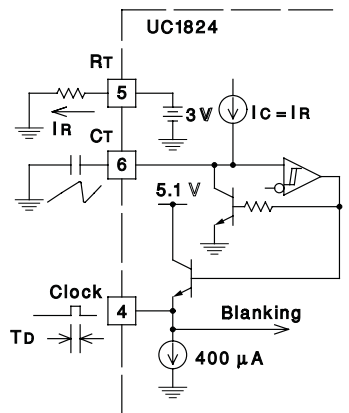
Error Amplifier Circuit



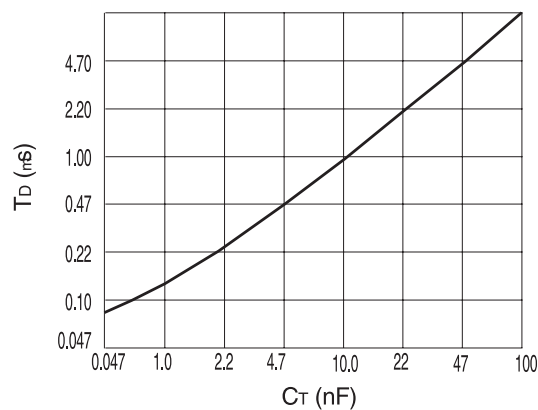
Synchronized Operation



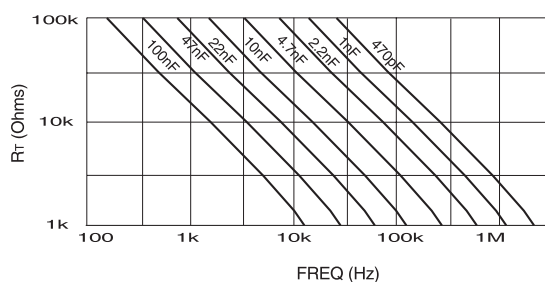
Oscillator Circuit



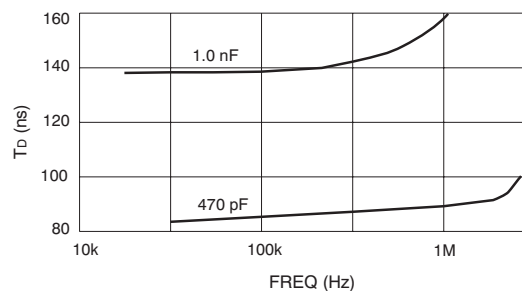
Primary Output Deadtime vs C_T ($3k \leq R_T \leq 100k$)



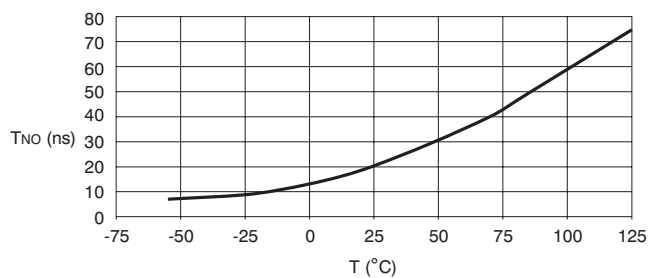
Timing Resistance vs Frequency



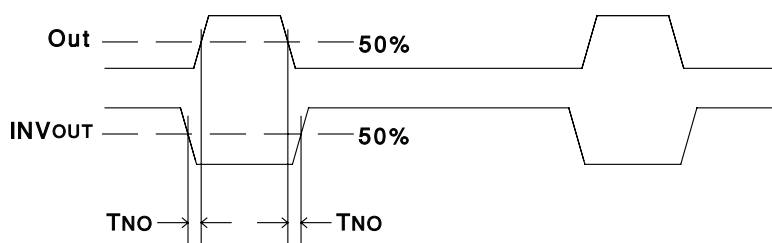
Primary Output Deadtime vs Frequency



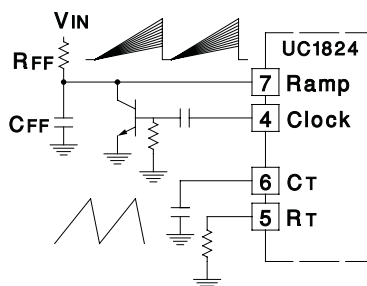
Typical Non-Overlap Time (T_{NO}) Over Temperature



Non-Overlap Time (T_{NO})

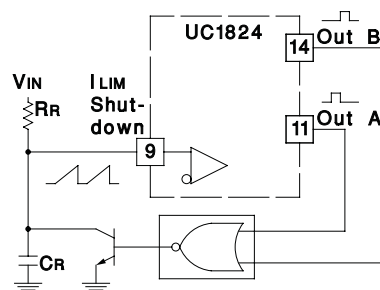


Forward Technique for Off-Line Voltage Mode Application

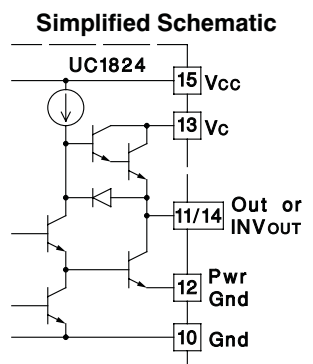


Constant Volt-Second Clamp Circuit

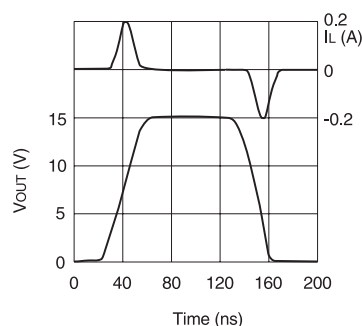
The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_T are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



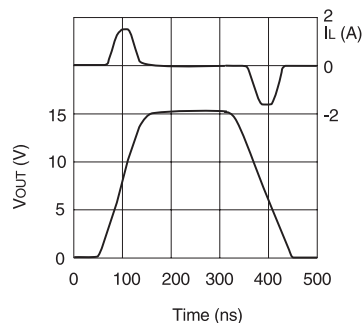
Output Section



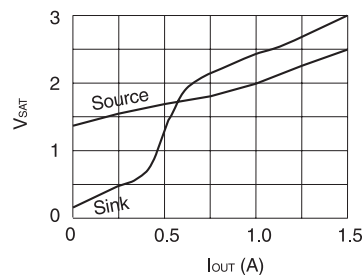
Rise/Fall Time ($C_L=1\text{ nF}$)



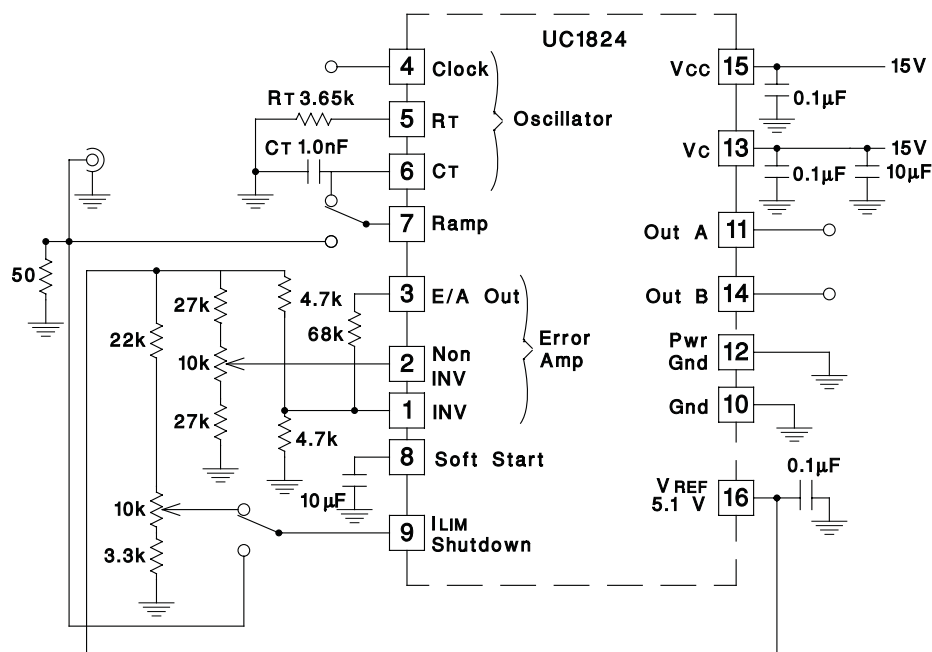
Rise/Fall Time ($C_L=10\text{ nF}$)



Saturation Curves



Open-Loop Laboratory Test Fixture



UDG-92036-2

This test fixture is useful for exercising many of the UC1824's functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2824DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2824DW	Samples
UC2824DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2824DW	Samples
UC2824N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2824N	Samples
UC3824DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3824DW	Samples
UC3824DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3824DW	Samples
UC3824N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3824N	Samples
UC3824NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3824N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS

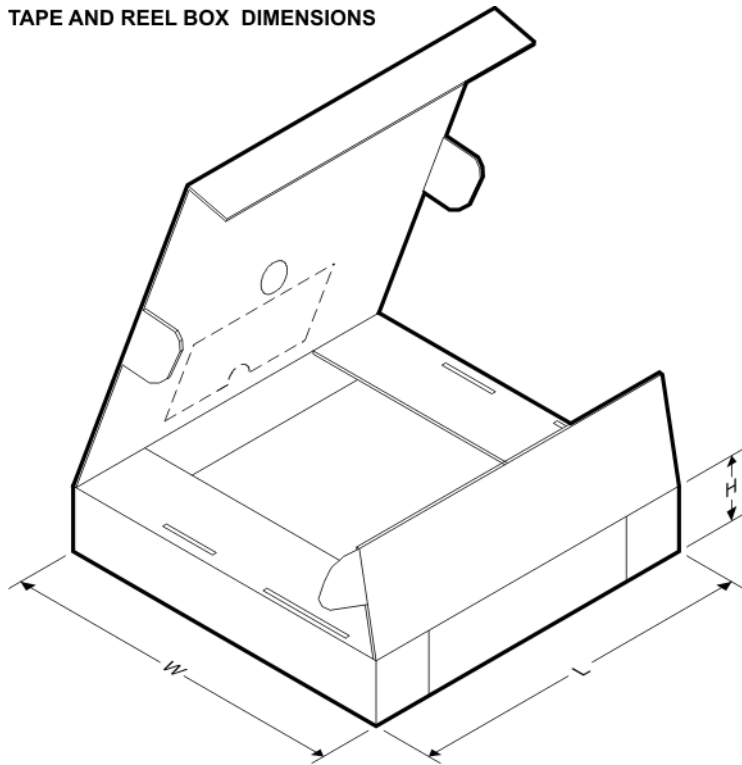

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3824DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3824DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com