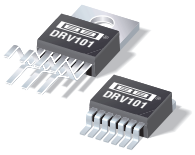

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PWM SOLENOID/VALVE DRIVER

FEATURES

- **HIGH OUTPUT DRIVE: 2.3A**
- **WIDE SUPPLY RANGE: +9V to +60V**
- **COMPLETE FUNCTION**
  - **PWM Output**
  - **Internal 24kHz Oscillator**
  - **Digital Control Input**
  - **Adjustable Delay and Duty Cycle**
  - **Over/Under Current Indicator**
- **FULLY PROTECTED**
  - **Thermal Shutdown with Indicator**
  - **Internal Current Limit**
- **PACKAGES: 7-Lead TO-220 and 7-Lead Surface-Mount DDPAK**

APPLICATIONS

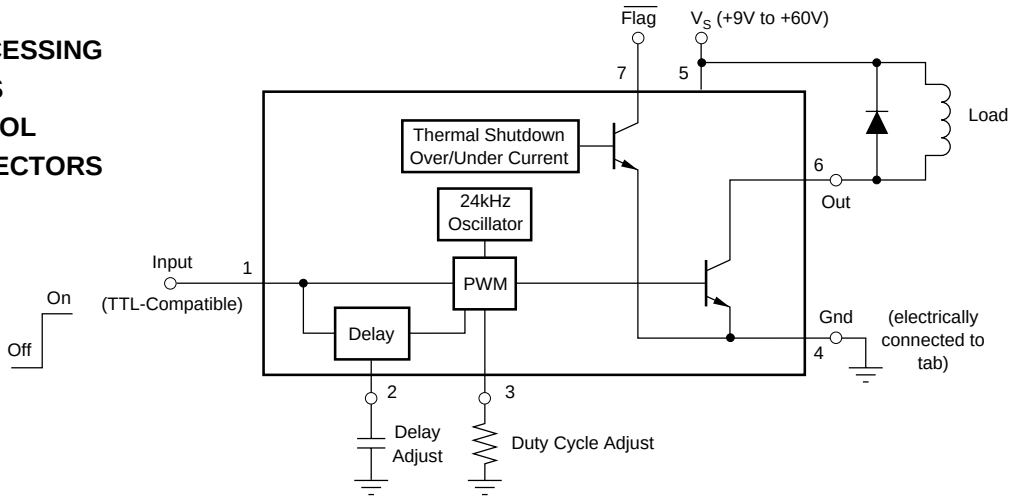
- **ELECTROMECHANICAL DRIVERS:**
  - **Solenoids**
  - **Actuators**
  - **Valves**
  - **Positioners**
  - **High Power Relays/Contactors**
  - **Clutch/Brake**
- **FLUID AND GAS FLOW SYSTEMS**
- **INDUSTRIAL CONTROL**
- **FACTORY AUTOMATION**
- **PART HANDLERS**
- **PHOTOGRAPHIC PROCESSING**
- **ELECTRICAL HEATERS**
- **MOTOR SPEED CONTROL**
- **SOLENOID/COIL PROTECTORS**
- **MEDICAL ANALYZERS**

DESCRIPTION

The DRV101 is a low-side power switch employing a pulse-width modulated (PWM) output. Its rugged design is optimized for driving electromechanical devices such as valves, solenoids, relays, actuators, and positioners. The DRV101 is also ideal for driving thermal devices such as heaters and lamps. PWM operation conserves power and reduces heat rise, resulting in higher reliability. In addition, adjustable PWM allows fine control of the power delivered to the load. Time from dc output to PWM output is externally adjustable.

The DRV101 can be set to provide a strong initial closure, automatically switching to a soft hold mode for power savings. Duty cycle can be controlled by a resistor, analog voltage, or digital-to-analog converter for versatility. A flag output indicates thermal shutdown and over/under current limit. A wide supply range allows use with a variety of actuators.

The DRV101 is available in a 7-lead staggered TO-220 package and a 7-lead surface-mount DDPAK plastic power package. It is specified over the extended industrial temperature range of –40°C to +85°C.



SPECIFICATIONS

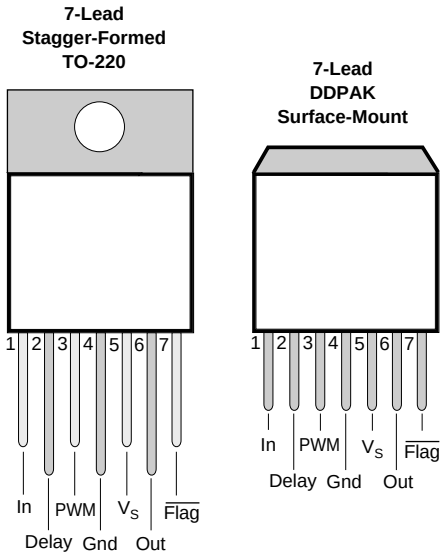
At T_C = +25°C, V_S = +24V, Load = 100Ω || 1000pF, and 4.99kΩ $\overline{\text{Flag}}$ pullup to +5V, unless otherwise noted.

PARAMETER	COMMENTS	DRV101T, F MIN	DRV101T, F TYP	DRV101T, F MAX	UNITS
OUTPUT					
Output Saturation Voltage, Sink	I_O = 1A		+0.8	+1	V
	I_O = 0.1A		+0.2	+0.3	V
Current Limit		1.9	2.3	3	A
Under-Scale Current(1)			23		mA
Leakage Current	Output Transistor Off, V_S = V_O = +60V		±0.01	±1	mA
DIGITAL CONTROL INPUT(2)					
V_{CTR} Low (output disabled)		0		+1.2	V
V_{CTR} High (output enabled)		+2.2		+5.5	V
I_{CTR} Low (output disabled)	V_{CTR} = 0V		–80		µA
I_{CTR} High (output enabled)	V_{CTR} = +5V		20		µA
Propagation Delay	On-to-Off and Off-to-On		2		µs
DELAY TO PWM(3)	dc to PWM Mode				
Delay Equation(4)			Delay to PWM ≈ C_D • 10^6 (C_D in F)		s
Delay Time	C_D = 0.1µF	80	95	110	ms
Minimum Delay Time(5)	C_D = 0		15		µs
DUTY CYCLE ADJUST					
Duty Cycle Range			10 to 90		%
Duty Cycle Accuracy	50% Duty Cycle, R_{PWM} = 28.7kΩ		±2	±5	%
vs Supply Voltage	50% Duty Cycle, V_S = V_O = +9V to +60V		±1	±5	%
Nonlinearity(6)	10% to 80% Duty Cycle		2		% FSR
DYNAMIC RESPONSE					
Output Voltage Rise Time	V_O = 10% to 90% of V_S		1	2.5	µs
Output Voltage Fall Time	V_O = 90% to 10% of V_S		0.1	2.5	µs
Oscillator Frequency		19	24	29	kHz
$\overline{\text{FLAG}}$					
Normal Operation	20kΩ Pull-Up to +5V, I_O < 1.5A	+4	+4.9		V
Fault(7)	Sinking 1mA		+0.2	+0.8	V
Sink Current	$V_{\overline{FLAG}}$ = 0.4V		2		mA
Under-Current Flag: Set			4		µs
Reset			2		µs
Over-Current Flag: Set			2		µs
Reset			2		µs
THERMAL SHUTDOWN					
Junction Temperature					
Shutdown			+165		°C
Reset from Shutdown			+150		°C
POWER SUPPLY					
Specified Operating Voltage			+24		V
Operating Voltage Range		+9		+60	V
Quiescent Current	I_O = 0		3.5	5	mA
TEMPERATURE RANGE					
Specified Range		–40		+85	°C
Operating Range		–55		+125	°C
Storage Range		–65		+150	°C
Thermal Resistance, θ_{JC}					
7-Lead DDPAK, 7-Lead TO-220			3		°C/W
Thermal Resistance, θ_{JA}					
7-Lead DDPAK, 7-Lead TO-220	No Heat Sink		65		°C/W

NOTES:(1) Under-scale current for T_C < 100°C—see Under-Scale Current vs Temperature typical performance curve. (2) Logic High enables output (normal operation). (3) Constant dc output to PWM (pulse-width modulated) time. (4) Maximum delay is determined by an external capacitor. Pulling the Delay Adjust Pin low corresponds to an infinite (continuous) delay. (5) Connecting the Delay Adjust pin to +5V reduces delay time to 3µs. (6) V_{IN} at pin 3 to percent of duty cycle at pin 6. (7) A fault results from over-temperature, over-current, or under-current conditions.

CONNECTION DIAGRAMS

Top Front View **TO-220, DDPAK**



NOTE: Tabs are electrically connected to ground (pin 4).

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V_S	60V
Input Voltage	–0.2V to V_S
PWM Adjust Input	–0.2V to V_S
Delay Adjust Input	–0.2V to V_S (24V max)
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)[2]	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Vapor-phase or IR reflow techniques are recommended for soldering the DRV101F surface-mount package. Wave soldering is not recommended due to excessive thermal shock and “shadowing” of nearby devices.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

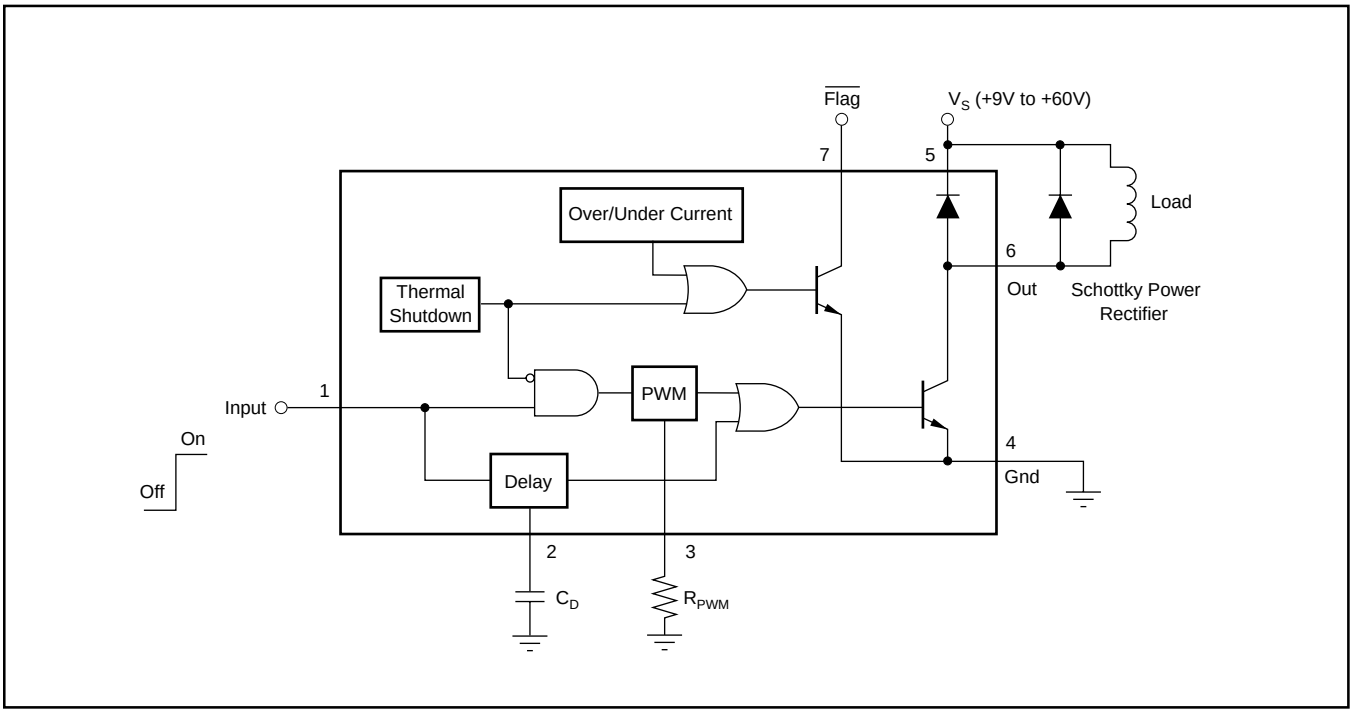
PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Ordering Addendum at the end of this data sheet.

PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
Pin 1	Input	The input is compatible with standard TTL levels. The device output becomes enabled when the input voltage is driven above the typical switching threshold, 1.7V. Below this level, the output is disabled. With no connection to the pin, the input level rises to 3.4V. Input current is 20µA when driven high and 80µA with the input low. The input may be momentarily driven to the power supply (V_S) without damage.
Pin 2	Delay Adjust	This pin sets the duration of the initial 100% duty cycle before the output goes into PWM mode. Leaving this pin floating results in a delay of approximately 15µs, which is internally limited by parasitic capacitance. Minimum delay may be reduced to less than 3µs by tying the pin to 5V. This pin connects internally to a 3µA current source from V_S and to a 3V threshold comparator. When the pin voltage is below 3V, the output device is 100% on. The PWM oscillator is not synchronized to the Input (pin 1), so the first pulse may be extended by any portion of the programmed duty cycle.
Pin 3	Duty Cycle Adjust (PWM)	Internally, this pin connects to the input of a comparator and a 19kΩ resistor to ground. It is driven by a 200µA current source from V_S. The voltage at this node linearly sets the duty cycle. Duty cycle can be programmed with a resistor, analog voltage, or output of a D/A converter. The active voltage range is from 0.75V to 3.7V to facilitate the use of single-supply control electronics. At 0.75V (or R_{PWM} = 3.5kΩ), duty cycle is near 90%. Swing to ground should be limited to no lower than 0.1V. PWM frequency is a constant 24kHz.
Pin 4	Ground	This pin is electrically connected to the package tab. It must be connected to system ground for the DRV101 to function. It carries the 3.5mA quiescent current plus the load current when the device is on.
Pin 5	V_S	This is the power supply pin. Operating range is +9V to +60V.
Pin 6	Out	The output is the collector of a power npn with the emitter connected to ground. Low power dissipation in the DRV101 is attained by the low saturation voltage and the fast switching transitions. Fall time is less than 75ns, rise time depends on load impedance. Base drive to the power device is limited with light loads to control turn-off delay. The response of this circuit causes the brief dip in saturation voltage after turn on. A flyback diode is needed with inductive loads to conduct the load current during the off cycle. The external diode should be selected for low forward voltage. The internal clamp diode provides protection but shouuld not be used to conduct load currents greater than 0.5A.
Pin 7	$\overline{\text{Flag}}$	Normally high (active low), the Flag signals either an over-temperature, over-current, or under-current fault. The over/under-current flags are true only when the output is on (constant dc output or the “on” portion of PWM mode). A thermal fault (thermal shutdown) occurs when the die surface reaches approximately 165°C and latches until the die cools to 150°C. Its output requires a pull-up resistor. It can typically sink two milliamps, sufficient to drive a low-current LED.

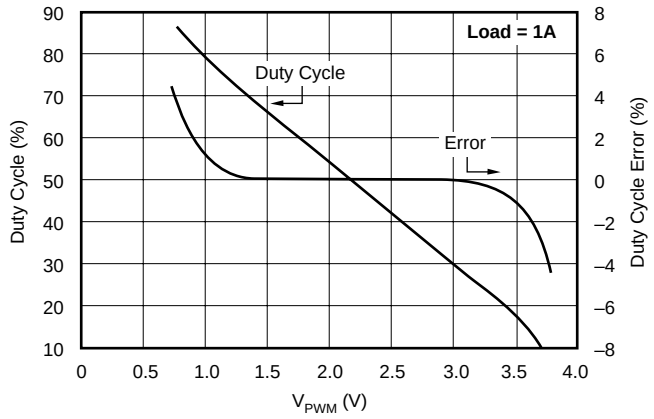
LOGIC BLOCK DIAGRAM



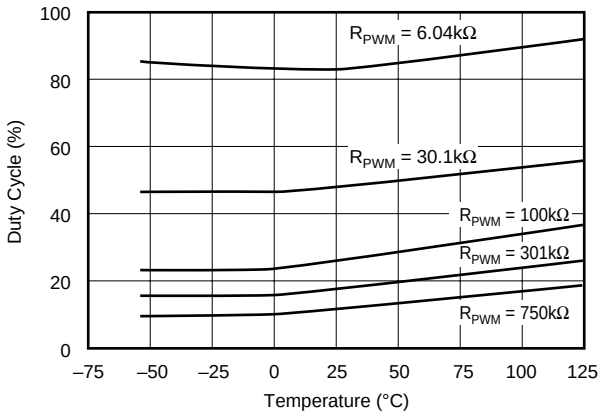
TYPICAL PERFORMANCE CURVES

At T_C = +25°C and V_S = +24V, unless otherwise noted.

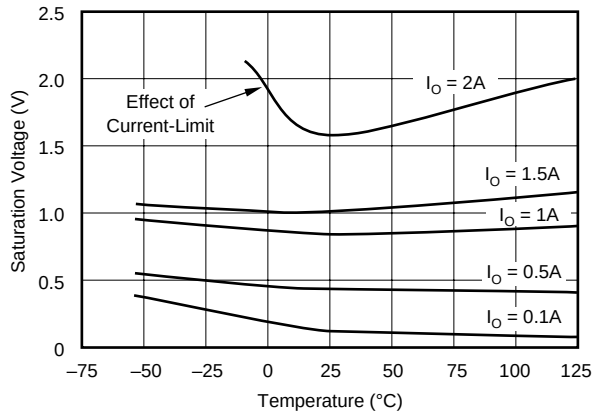
DUTY CYCLE and DUTY CYCLE ERROR vs VOLTAGE



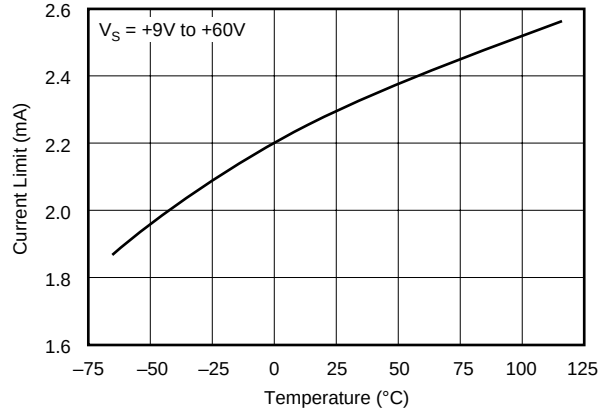
DUTY CYCLE vs TEMPERATURE



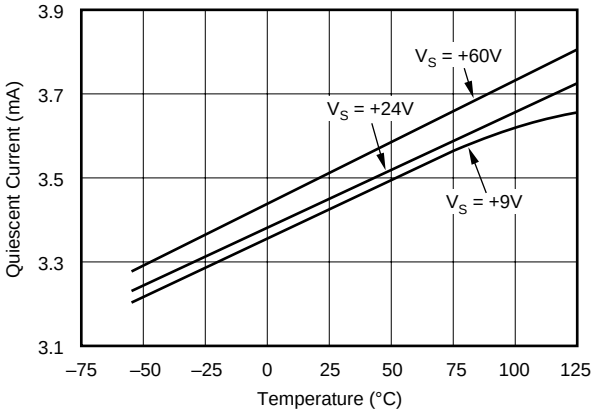
OUTPUT SATURATION VOLTAGE vs TEMPERATURE



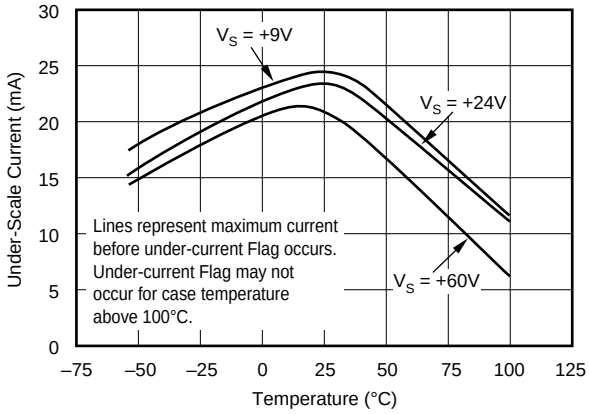
CURRENT LIMIT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



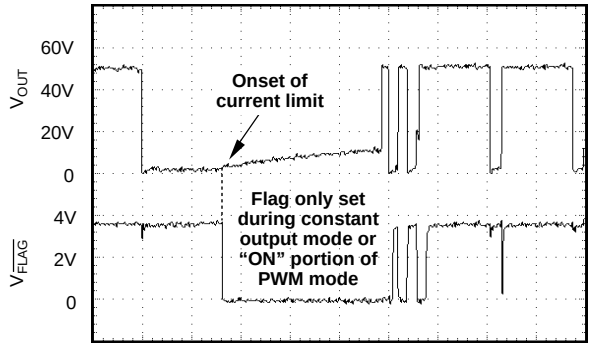
UNDER-SCALE CURRENT vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

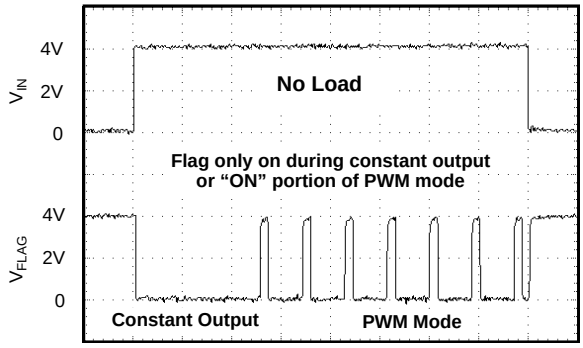
At T_C = +25°C and V_S = +24V, unless otherwise noted.

FLAG OPERATION
OVER-CURRENT LIMIT
(V_S = +60V, C_D = 110pF, R_{PWM} = 750kΩ)



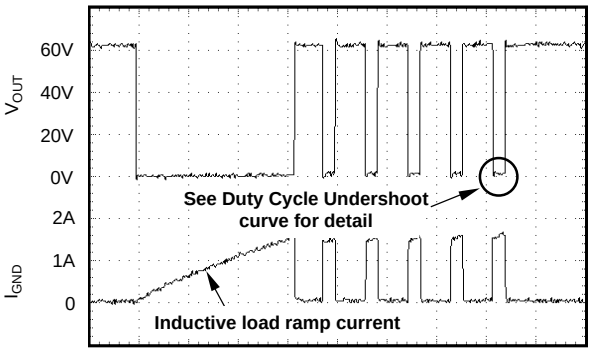
25µs/div

FLAG OPERATION
UNDER-CURRENT
(V_S = +24V, C_D = 110pF, R_{PWM} = 6.04kΩ)



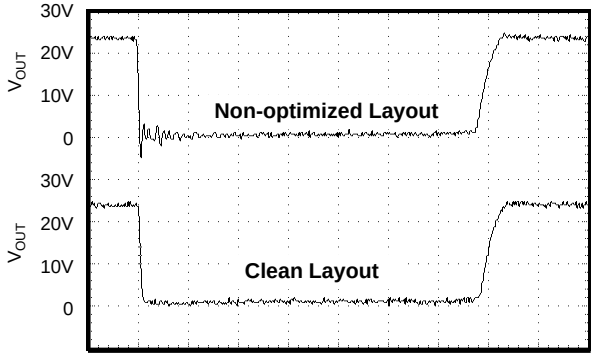
50µs/div

DC TO PWM MODE
DRIVING INDUCTIVE LOAD
(V_S = +60V, C_D = 110pF, R_{PWM} = 301kΩ)



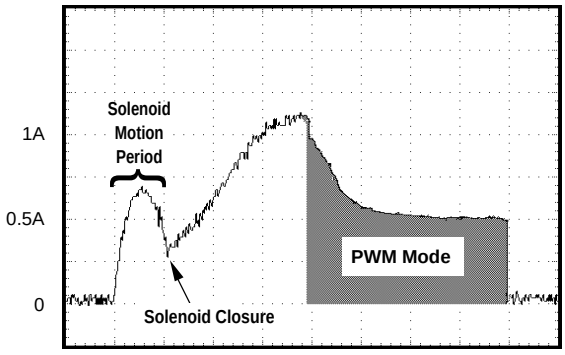
50µs/div

DUTY CYCLE UNDERSHOOT
Load = 1A



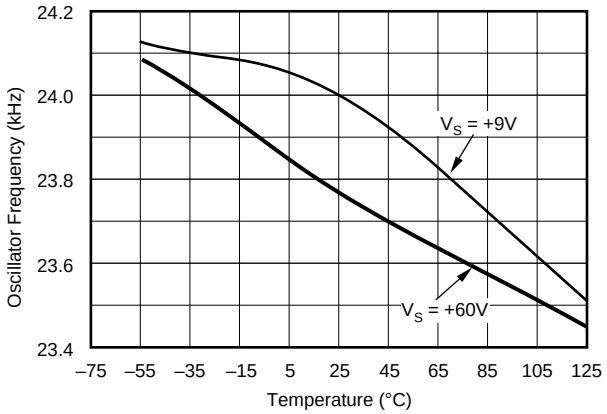
1µs/div

TYPICAL SOLENOID CURRENT WAVEFORM
(V_S = +24V)



25ms/div

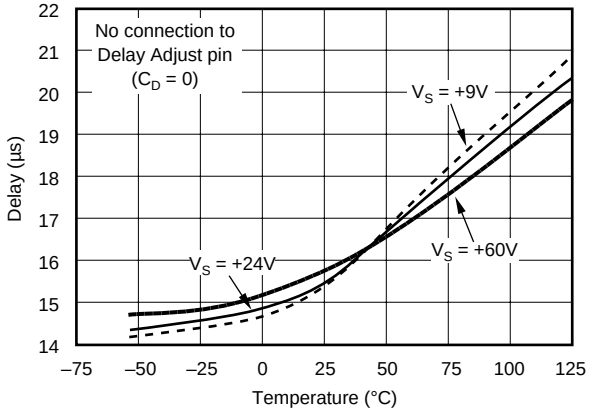
OSCILLATOR FREQUENCY vs TEMPERATURE



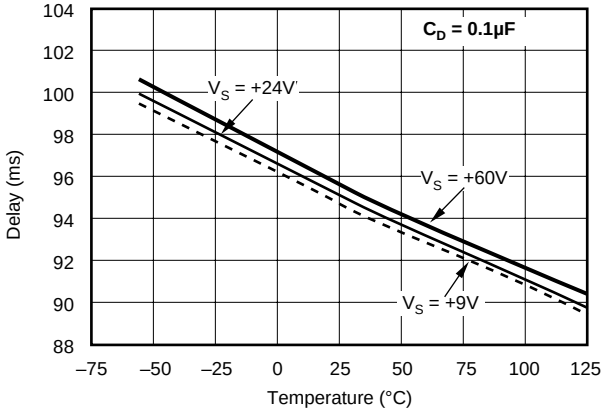
TYPICAL PERFORMANCE CURVES (CONT)

At T_C = +25°C and V_S = +24V, unless otherwise noted.

MINIMUM DELAY TO PWM vs TEMPERATURE



NOMINAL DELAY TIME TO PWM vs TEMPERATURE



BASIC OPERATION

The DRV101 is a low-side, bipolar power switch employing a pulse-width modulated (PWM) output for driving electro-mechanical and thermal devices. Its design is optimized for two types of applications; a two-state driver (open/close) for loads such as solenoids and actuators, and a linear driver for valves, positioners, heaters, and lamps. Its wide supply range, adjustable delay to PWM mode, and adjustable duty cycle make it suitable for a wide range of applications. Figure 1 shows the basic circuit connections to operate the DRV101. A 0.1µF bypass capacitor is shown connected to the power supply pin.

The Input (pin 1) is compatible with standard TTL levels. Input voltages between +2.2V and +5.5V turn the device output on, while pulling the pin low (0V to +1.2V), shuts the DRV101 output off. Input current is typically 80µA.

Delay Adjust (pin 2) and Duty Cycle Adjust (pin 3) allow external adjustment of the PWM output signal. The Delay Adjust pin can be left floating for minimum delay to PWM mode (typically 15µs) or a capacitor can be used to set the delay time. Duty cycle of the PWM output can be controlled by a resistor, analog voltage, or D/A converter. Figure 1b provides an example timing diagram with the Delay Adjust pin connected to 0.1µF and duty cycle set for 25%. See the "Delay Adjust" and "Duty Cycle Adjust" text for equations and further explanation.

Ground (pin 4) is electrically connected to the package tab. This pin must be connected to system ground for the DRV101 to function. This serves as the load current path to ground, as well as the DRV101 reference ground.

The load (solenoid, valve, etc.) is connected between the supply (pin 5) and output (pin 6). For an inductive load, an external diode across the output is required as shown in Figure 1a. The diode serves to maintain the hold force during PWM operation. For remotely located loads, the external diode should be placed close to the DRV101 (Figure 1a). The internal clamp diode between the output and ground should not be used to carry load current.

The $\overline{\text{Flag}}$ (pin 7) provides fault status for under-current, over-current, and thermal shutdown conditions. This pin is active low with pin voltage typically +0.3V during a fault condition. A small value capacitor may be needed between $\overline{\text{Flag}}$ and ground for noisy applications.

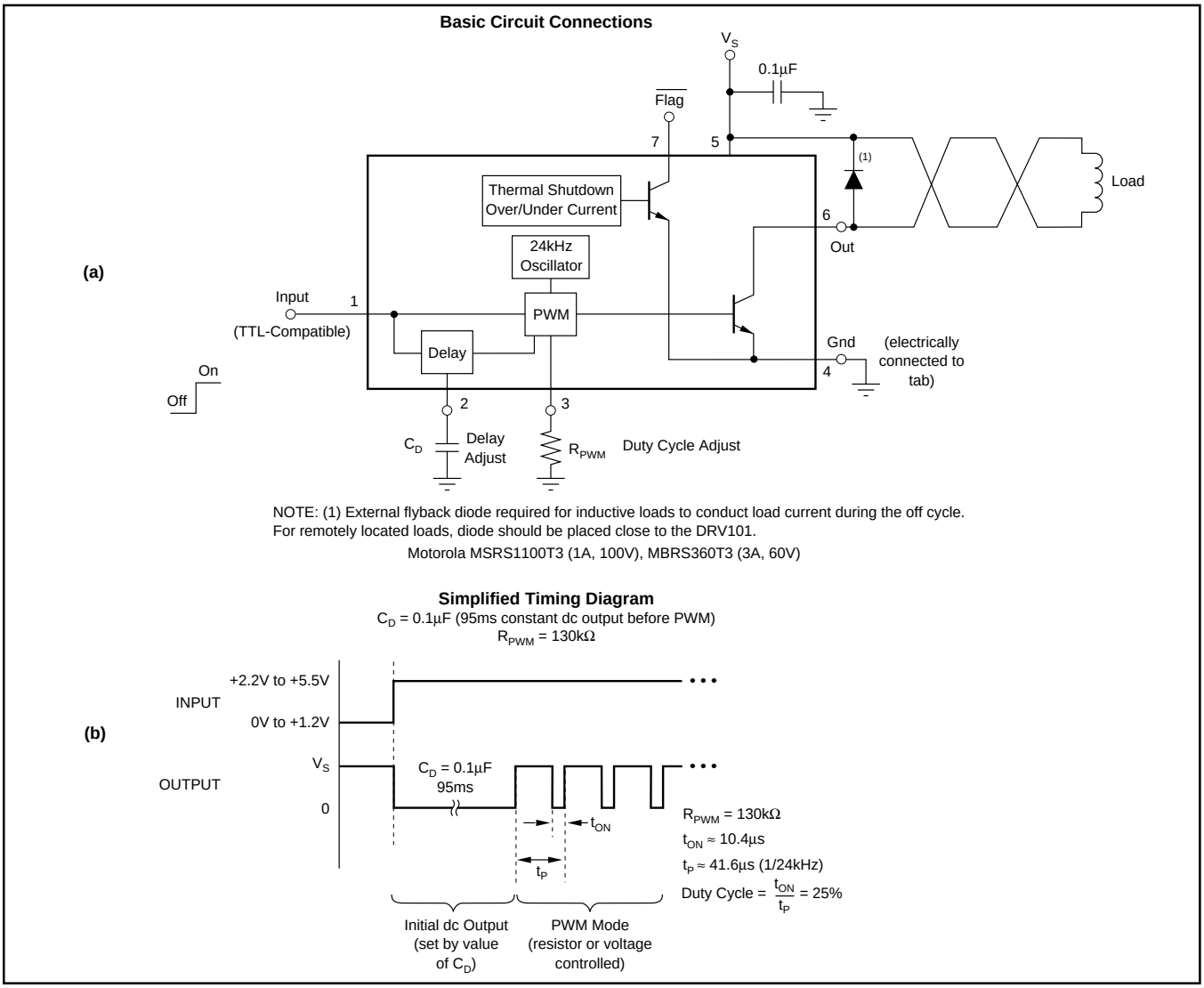


FIGURE 1. Basic Circuit Connections and Timing Diagram.

APPLICATIONS INFORMATION

POWER SUPPLY

The DRV101 operates from a single +9V to +60V supply with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Performance Curves.

ADJUSTABLE INITIAL 100% DUTY CYCLE

A unique feature of the DRV101 is its ability to provide an initial constant dc output (100% duty cycle) and then switch to PWM mode to save power. This function is particularly useful when driving solenoids which have a much higher pull-in current requirement than hold requirement.

The duration of this constant dc output (before PWM output begins) can be externally controlled with a capacitor connected from Delay Adjust (pin 2) to ground according to the following equation:

$$\text{Delay Time} \approx C_D \bullet 10^6$$

(time in seconds, C_D in Farads)

Leaving the Delay Adjust pin open results in a constant output time of approximately 15µs. The duration of this initial output can be reduced to less than 3µs by connecting the pin to 5V. Table I provides examples of desired "delay" times (constant output before PWM mode) and the appropriate capacitor values or pin connection.

CONSTANT OUTPUT DURATION	C_D
3µs	Pin connected to 5V
15µs	Pin open
100µs	100pF
1ms	1nF
100ms	0.1µF

TABLE I. Delay Adjust Pin Connections.

The internal Delay Adjust circuitry is composed of a 3µA current source and a 3V comparator as shown in Figure 2. Thus, when the pin voltage is less than 3V, the output device is 100% on (dc output mode).

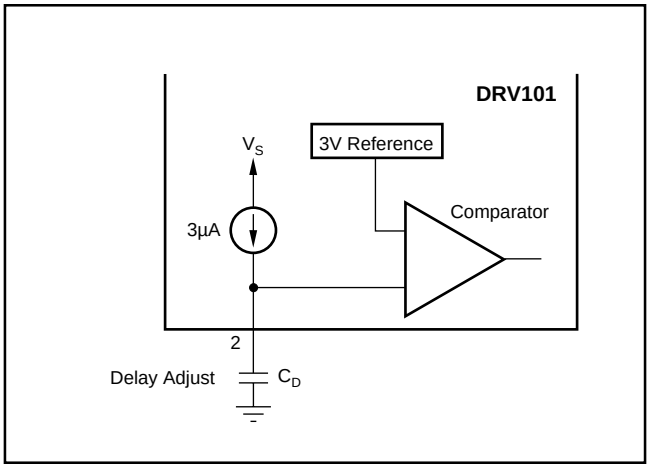


FIGURE 2. Simplified Circuit Model of the Delay Adjust Pin.

ADJUSTABLE DUTY CYCLE

The DRV101's externally adjustable duty cycle provides an accurate means of controlling power delivered to the load. Duty cycle can be set from 10% to 100% with an external resistor, analog voltage, or the output of a D/A converter. Reduced duty cycle results in reduced power dissipation. This keeps the DRV101 and load cooler, resulting in increased reliability for both devices. PWM frequency is a constant 24kHz.

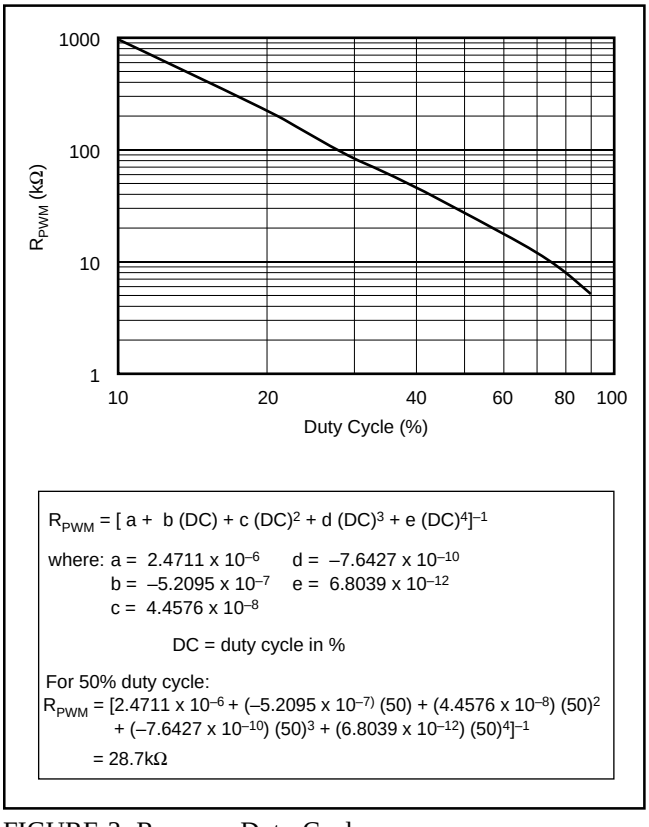
Resistor Controlled Duty Cycle

Duty cycle is easily programmed with a resistor (R_{PWM}) connected between the Duty Cycle Adjust pin and ground. Increased resistor values correspond to decreased duty cycles. Table II provides resistor values for typical duty cycles. Resistor values for additional duty cycles can be obtained from Figure 3. For reference purposes, the equation for calculating R_{PWM} is included in Figure 3.

DUTY CYCLE	RESISTOR(1) R_{PWM} (kΩ)	VOLTAGE(2) V_{PWM} (V)
10	976	3.7
20	205	3.4
30	84.5	3.0
40	46.4	2.6
50	28.7	2.2
60	18.2	1.75
70	11.8	1.35
80	7.50	1.00
90	4.87	0.75

NOTES: (1) Resistor values listed are nearest 1% standard values. (2) Do not drive pin below 0.1V. For additional values, see "Duty Cycle vs Voltage" typical performance curve.

TABLE II. Duty Cycle Adjust. T_A= +25°C, V_S = +24V.



$$R_{PWM} = [a + b(DC) + c(DC)^2 + d(DC)^3 + e(DC)^4]^{-1}$$

where: $a = 2.4711 \times 10^{-6}$ $d = -7.6427 \times 10^{-10}$
$b = -5.2095 \times 10^{-7}$ $e = 6.8039 \times 10^{-12}$
$c = 4.4576 \times 10^{-8}$

DC = duty cycle in %

For 50% duty cycle:

$$R_{PWM} = [2.4711 \times 10^{-6} + (-5.2095 \times 10^{-7})(50) + (4.4576 \times 10^{-8})(50)^2 + (-7.6427 \times 10^{-10})(50)^3 + (6.8039 \times 10^{-12})(50)^4]^{-1}$$

$$= 28.7k\Omega$$

FIGURE 3. R_{PWM} vs Duty Cycle.

Voltage Controlled Duty Cycle

Duty cycle can also be programmed with an analog voltage, V_{PWM}. With $V_{PWM} \approx 0.75V$, duty cycle is near 90%. Increasing this voltage results in decreased duty cycles. Table II provides V_{PWM} values for typical duty cycles. See the "Duty Cycle vs Voltage" Typical Performance Curve for additional duty cycles.

The Duty Cycle Adjust pin should not be driven below 0.1V. If the voltage source used can go between 0.1V and ground, a series resistor between the voltage source and the Duty Cycle Adjust pin (Figure 4) is required to limit swing. If the pin is driven below 0.1V, the output will be unpredictable.

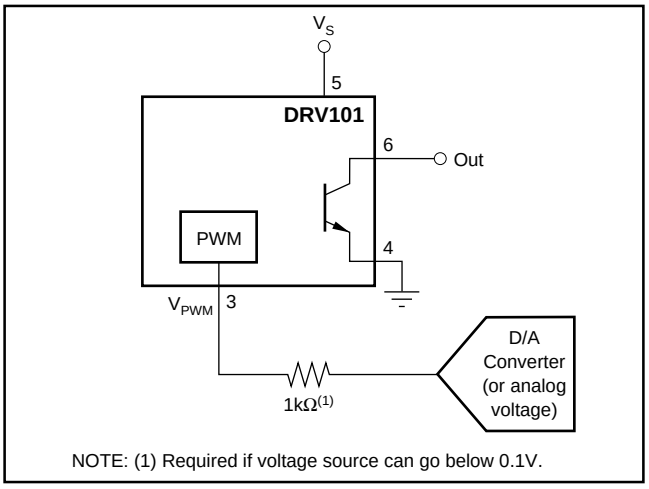


FIGURE 4. Using a Voltage to Program Duty Cycle.

The DRV101's internal 24kHz oscillator sets the PWM period. This frequency is not externally adjustable. Duty Cycle Adjust (pin 3) is internally driven by a 200µA current source and connects to the input of a comparator and a 19kΩ resistor as shown in Figure 5. The DRV101's PWM control design is inherently monotonic. That is, a decreased voltage (or resistor value) always produces an increased duty cycle.

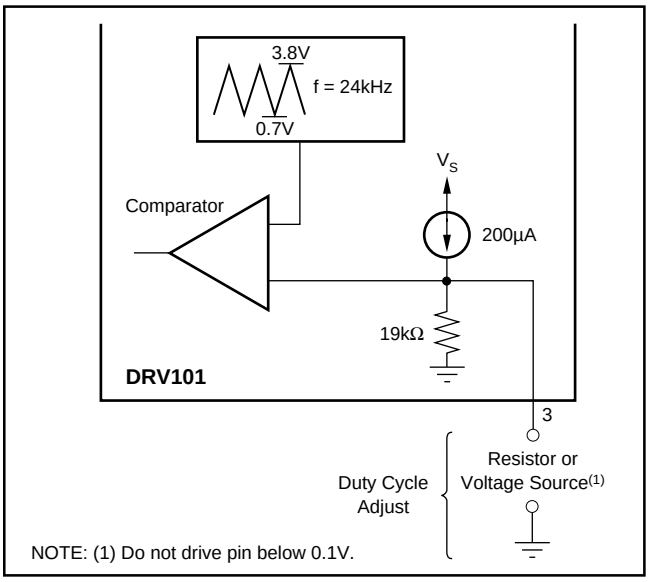


FIGURE 5. Simplified Circuit Model of the Duty Cycle Adjust Pin.

STATUS FLAG

$\overline{\text{Flag}}$ (pin 7) provides fault indication for under-current, over-current, and thermal shutdown conditions. During a fault condition, $\overline{\text{Flag}}$ output is driven low (pin voltage typically drops to 0.3V). A pull-up resistor, as shown in Figure 6, is required to interface with standard logic. A small value capacitor may be needed between $\overline{\text{Flag}}$ and ground in noisy applications.

Figure 6 gives an example of a non-latching fault monitoring circuit, while Figure 7 provides a latching version. The $\overline{\text{Flag}}$ pin can sink several milliamps, sufficent to drive external logic circuitry or an LED (Figure 8) to indicate when a fault has occurred. In addition, the $\overline{\text{Flag}}$ pin can be used to turn off other DRV101's in a system for chain fault protection.

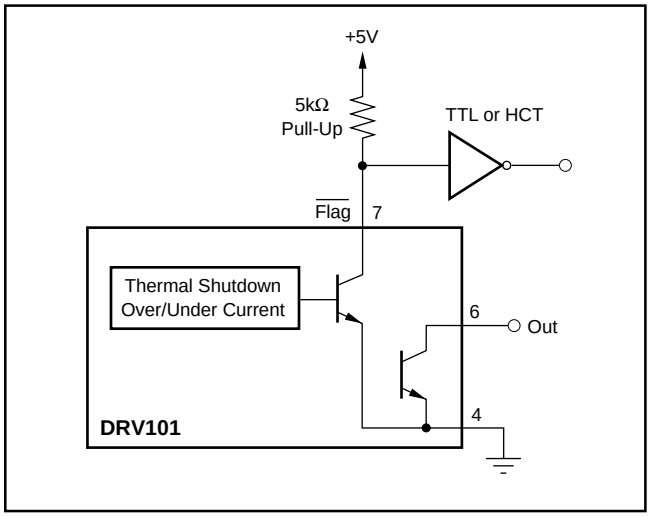


FIGURE 6. Non-Latching Fault Monitoring Circuit.

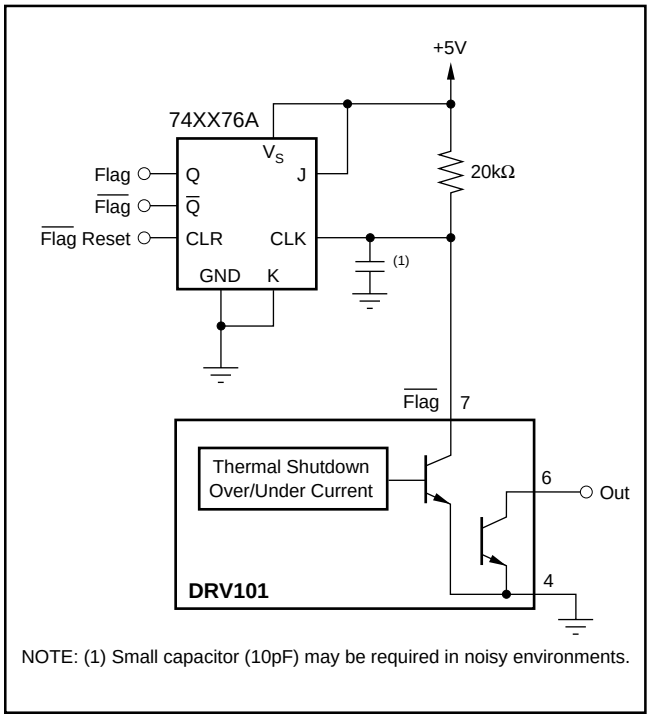


FIGURE 7. Latching Fault Monitoring Circuit.

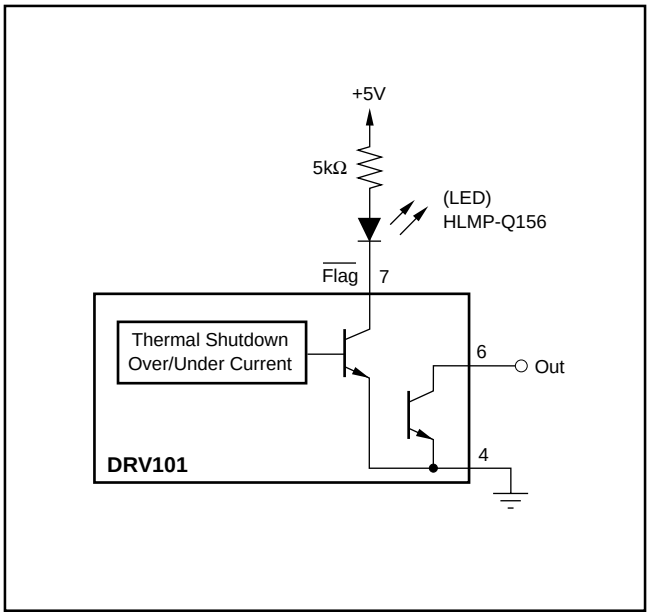


FIGURE 8. LED to Indicate Fault Condition.

Over/Under Current Fault

An over-current fault occurs when the output current is greater than approximately 2.3A. The status flag is not latched. Since current during PWM mode is switched on and off, the flag output will be modulated with PWM timing (see flag waveforms in the Typical Performance Curves).

An under-current fault occurs when the output current is below the under-scale current threshold (typically 23mA). For example, this function indicates when the load is disconnected. Again, the flag output is not latched, so an under-current condition during PWM mode will produce a flag output that is modulated by the PWM waveform. An initial, brief under-current flag normally appears driving inductive loads and may be avoided by adding a parallel resistor sufficient to move the initial current above the under-current threshold. An under-current flag may not appear for case temperatures above 100°C. Avoid adding capacitance to pin 6 (Out) as it may cause momentary current limiting.

Over-Temperature Fault

A thermal fault occurs when the die reaches approximately 165°C, producing a similar effect as pulling the input low. Internal shutdown circuitry disables the output and resets the Delay Adjust pin. The $\overline{\text{Flag}}$ is latched in the low state (fault condition) until the die has cooled to approximately 150°C. A thermal fault can occur in any mode of operation. Recovery from thermal fault will start in delay mode (constant dc output).

PACKAGE MOUNTING

Figure 9 provides recommended PCB layouts for both the TO-220 and DDPAK power packages. The tab of both packages is electrically connected to ground (pin 4). It may be desirable to isolate the tab of TO-220 package from its mounting surface with a mica (or other film) insulator (see

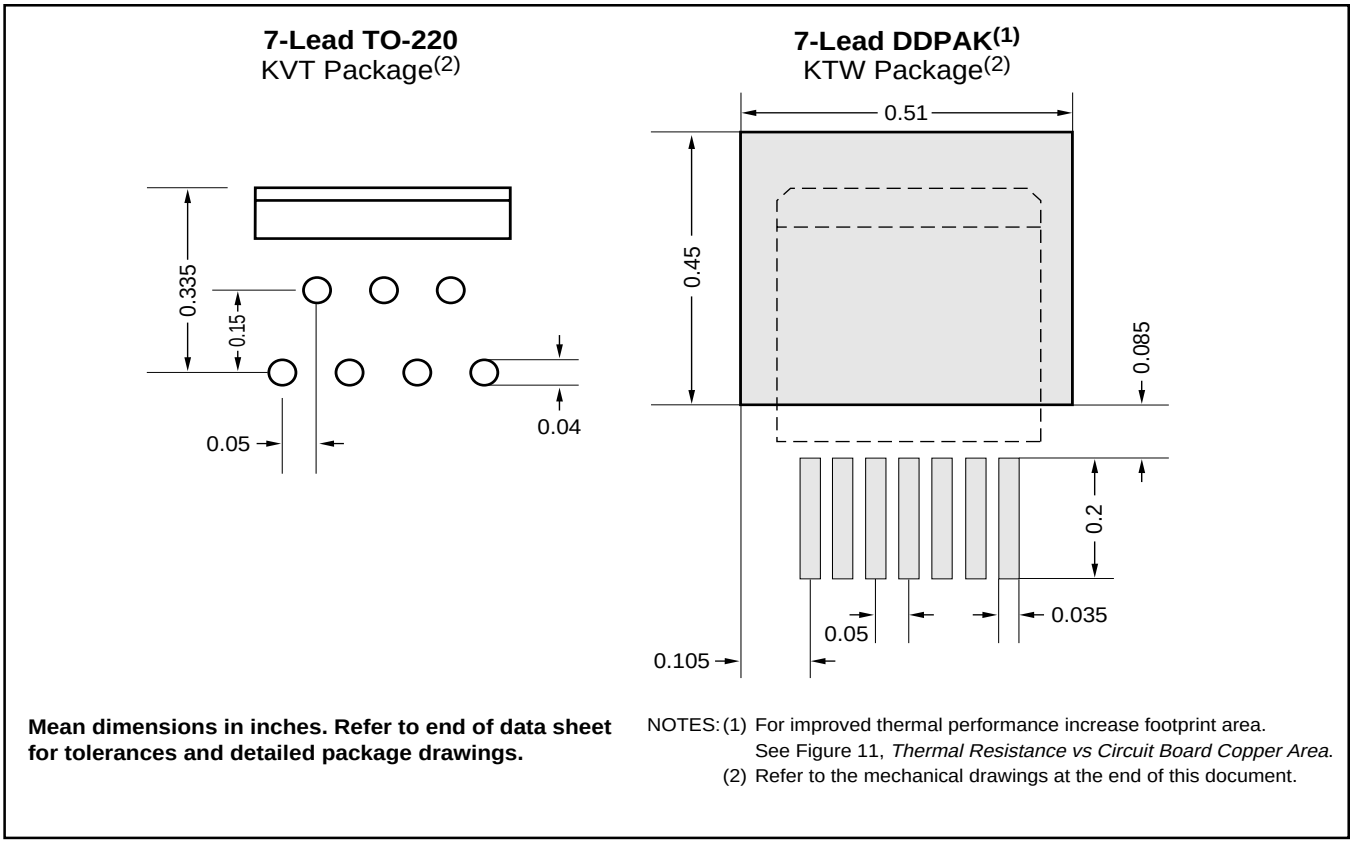


FIGURE 9. TO-220 and DDPAK Solder Footprints.

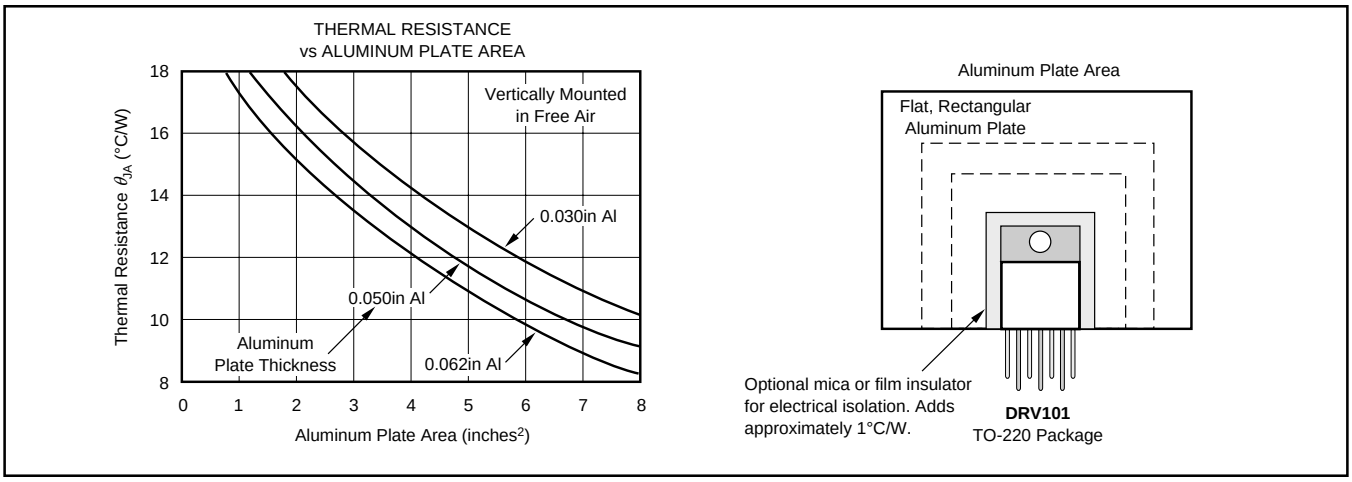


FIGURE 10. TO-220 Thermal Resistance vs Aluminum Plate Area.

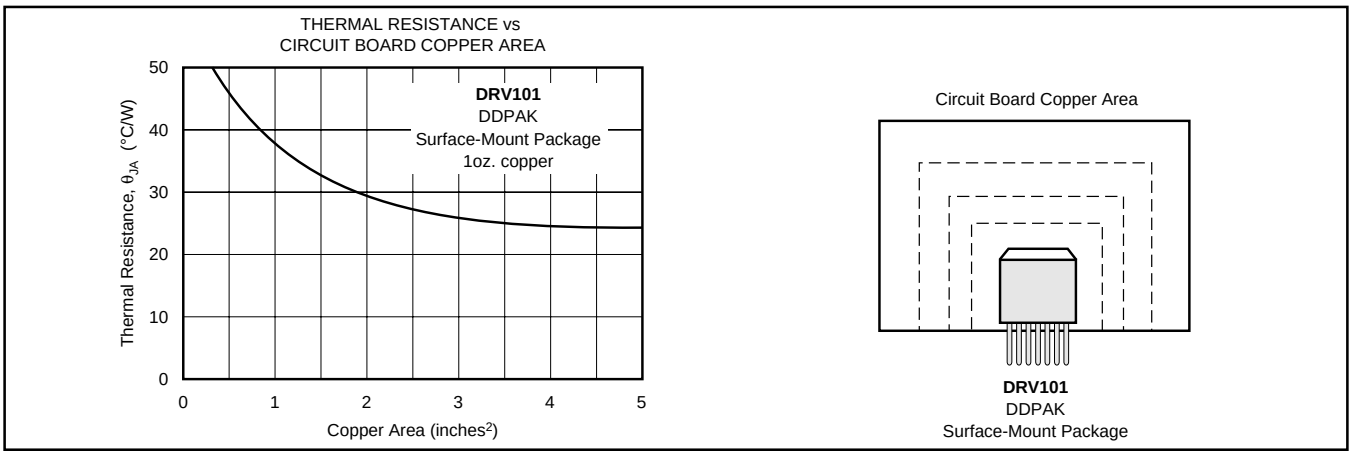


FIGURE 11. DDPAK Thermal Resistance vs Circuit Board Copper Area.

Figure 10). For lowest overall thermal resistance, it is best to isolate the entire heat sink/DRV101 structure from the mounting surface rather than to use an insulator between the semiconductor and heat sink.

For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit board copper area. Increasing the copper area improves heat dissipation. Figure 11 shows typical thermal resistance from junction-to-ambient as a function of the copper area.

POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. Power dissipation is equal to the product of output current times the voltage across the conducting output transistor times the duty cycle. Power dissipation can be minimized by using the lowest possible duty cycle necessary to assure the required hold force.

Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

THERMAL PROTECTION

Power dissipated in the DRV101 will cause the junction temperature to rise. The DRV101 has thermal shutdown circuitry that protects the device from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is again enabled. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the amplifier but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case load and signal conditions. For good reliability, thermal protection should trigger more than 40°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

The internal protection circuitry of the DRV101 was designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the DRV101 into thermal shutdown will degrade reliability.

HEAT SINKING

Most applications will not require a heat sink to assure that the maximum operating junction temperature (125°C) is not exceeded. However, junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the equation:

$$T_J = T_A + P_D\theta_{JA} \quad (1)$$

$$\text{where, } \theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA} \quad (2)$$

T_J = Junction Temperature (°C)
T_A = Ambient Temperature (°C)
P_D = Power Dissipated (W)
θ_{JC} = Junction-to-Case Thermal Resistance (°C/W)
θ_{CH} = Case-to-Heat Sink Thermal Resistance (°C/W)
θ_{HA} = Heat Sink-to-Ambient Thermal Resistance (°C/W)
θ_{JA} = Junction-to-Air Thermal Resistance (°C/W)

Figure 12 shows maximum power dissipation versus ambient temperature with and without the use of a heat sink. Using a heat sink significantly increases the maximum power dissipation at a given ambient temperature as shown.

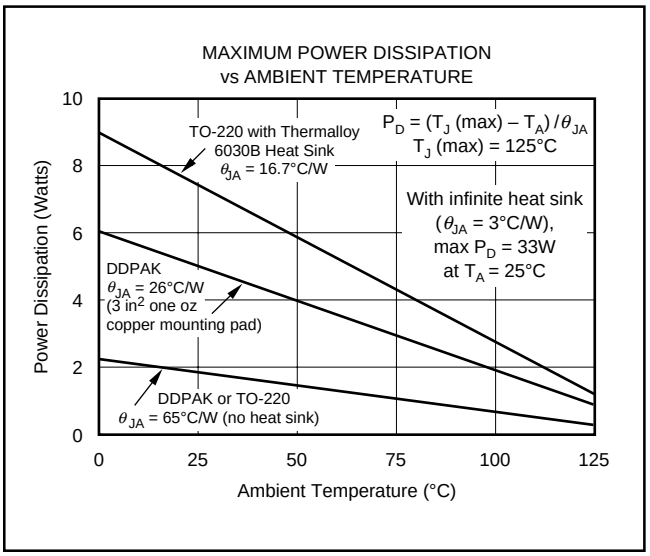


FIGURE 12. Maximum Power Dissipation vs Ambient Temperature.

The difficulty in selecting the heat sink required lies in determining the power dissipated by the DRV101. For dc output into a purely resistive load, power dissipation is simply the load current times the voltage developed across the conducting output transistor times the duty cycle. Other loads are not as simple. Consult Application Bulletin AB-039 for further insight on calculating power dissipation. Once power dissipation for an application is known, the proper heat sink can be selected.

Heat Sink Selection Example

A TO-220 package is dissipating 5 Watts. The maximum expected ambient temperature is 35°C. Find the proper heat sink to keep the junction temperature below 125°C.

Combining Equations 1 and 2 gives:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CH} + \theta_{HA}) \quad (3)$$

T_J, T_A, and P_D are given. θ_{JC} is provided in the specification table, 3°C/W. θ_{CH} can be obtained from the heat sink manufacturer. Its value depends on heat sink size, area, and material used. Semiconductor package type, mounting screw torque, insulating material used (if any), and thermal joint compound used (if any) also affect θ_{CH}. A typical θ_{CH} for a TO-220 mounted package is 1°C/W. Now we can solve for θ_{HA}:

$$\theta_{HA} = \frac{T_J - T_A}{P_D} - \left(\theta_{JC} + \theta_{CH}\right) \quad (4)$$

$$\theta_{HA} = \frac{125°C - 35°C}{5W} - \left(3°C/W + 1°C/W\right) = 14°C/W$$

To maintain junction temperature below 125°C, the heat sink selected must have a θ_{HA} less than 14°C/W. In other words, the heat sink temperature rise above ambient must be less than 70°C (14°C/W x 5W). For example, at 5 Watts Thermalloy model number 6030B has a heat sink temperature rise of 66°C above ambient (θ_{HA} = 66°C/5W = 13.2°C/W), which is below the 70°C required in this example. Figure 12 shows power dissipation versus ambient temperature for a TO-220 package with a 6030B heat sink.

Another variable to consider is natural convection versus forced convection air flow. Forced-air cooling by a small fan can lower θ_{CA} (θ_{CH} + θ_{HA}) dramatically. Heat sink manufacturers provide thermal data for both of these cases. For additional information on determining heat sink requirements, consult Application Bulletin AB-038.

As mentioned earlier, once a heat sink has been selected, the complete design should be tested under worst-case load and signal conditions to ensure proper thermal protection.

APPLICATION CIRCUITS

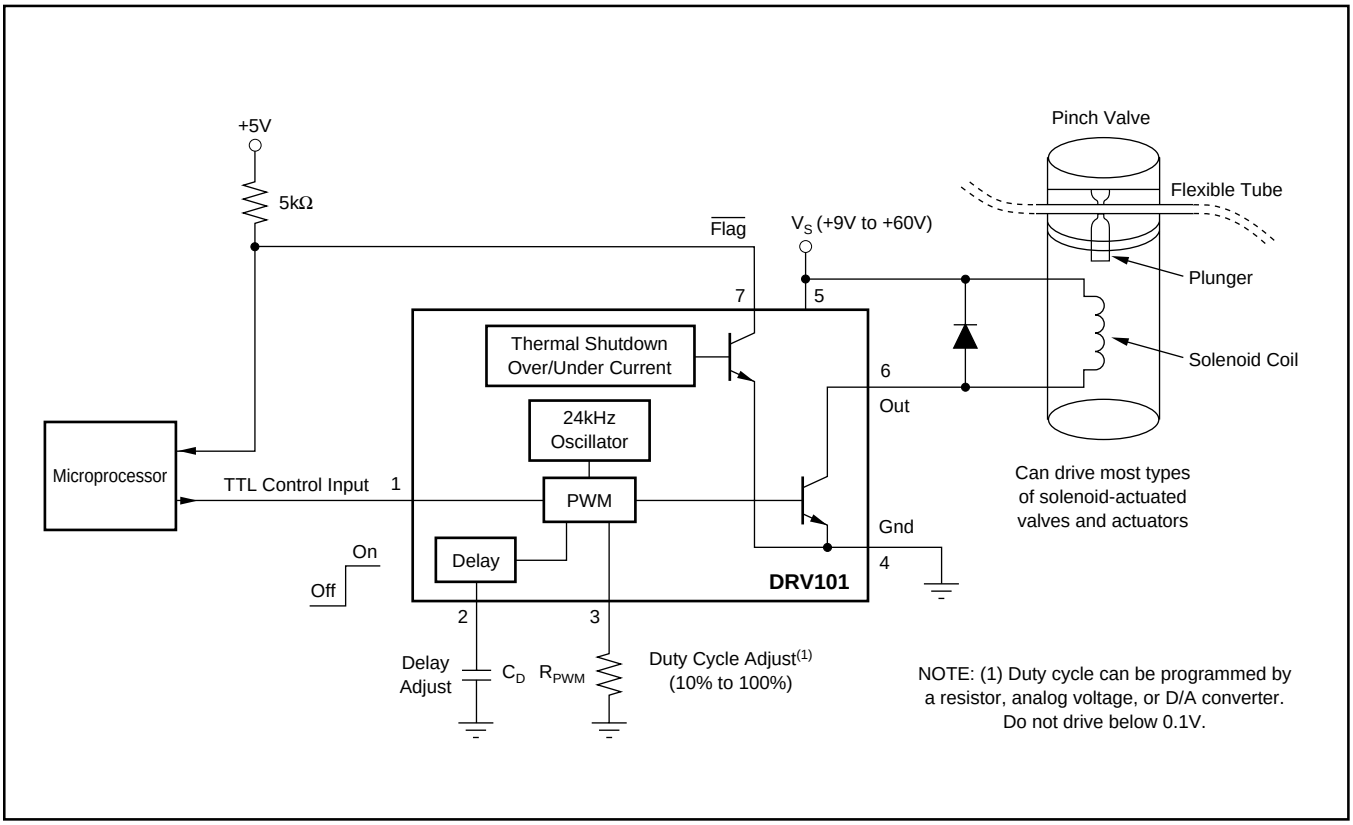


FIGURE 13. Fluid Flow Control System.

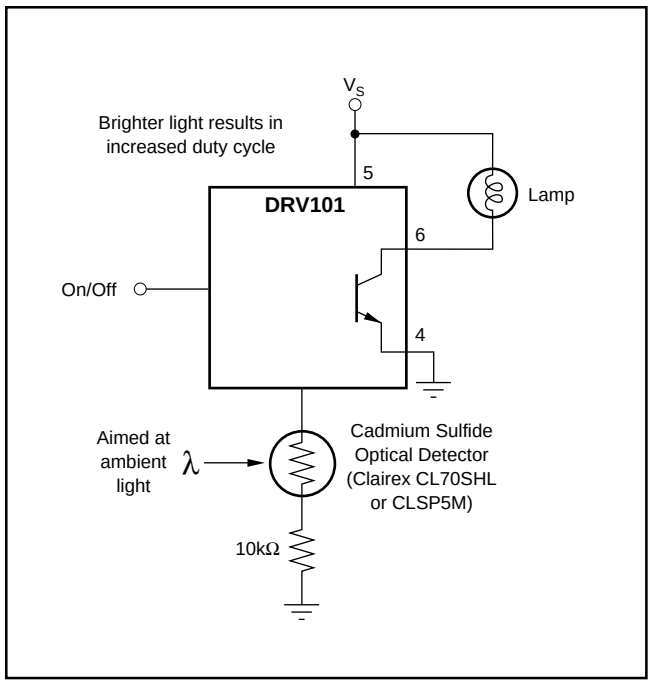


FIGURE 14. Instrument Light Dimmer Circuit.

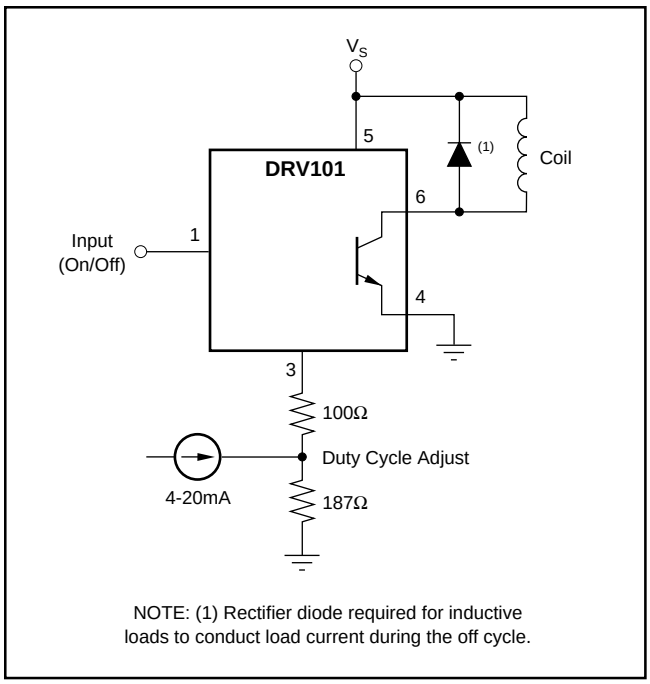


FIGURE 15. 4-20mA Input to PWM Output.

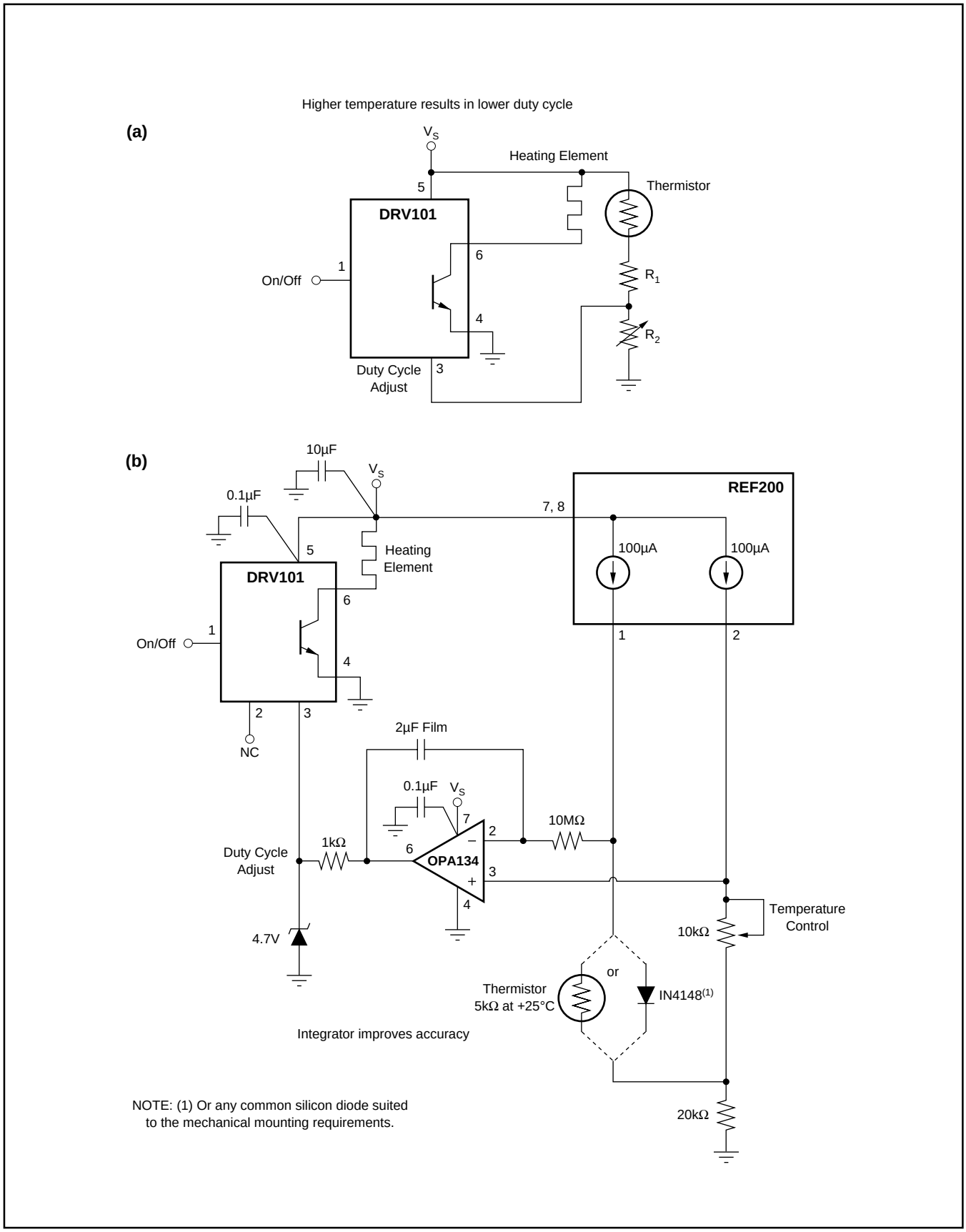


FIGURE 16. Temperature Controller.

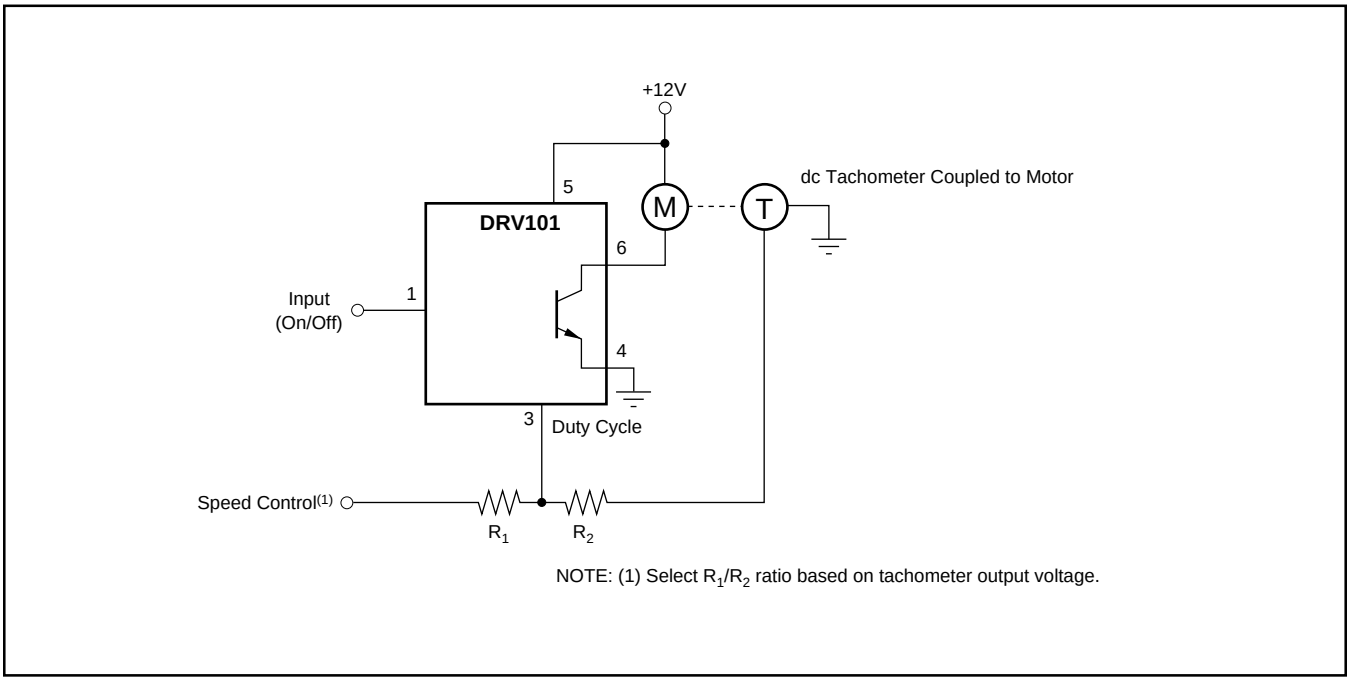


FIGURE 17. Constant Speed Motor Control.

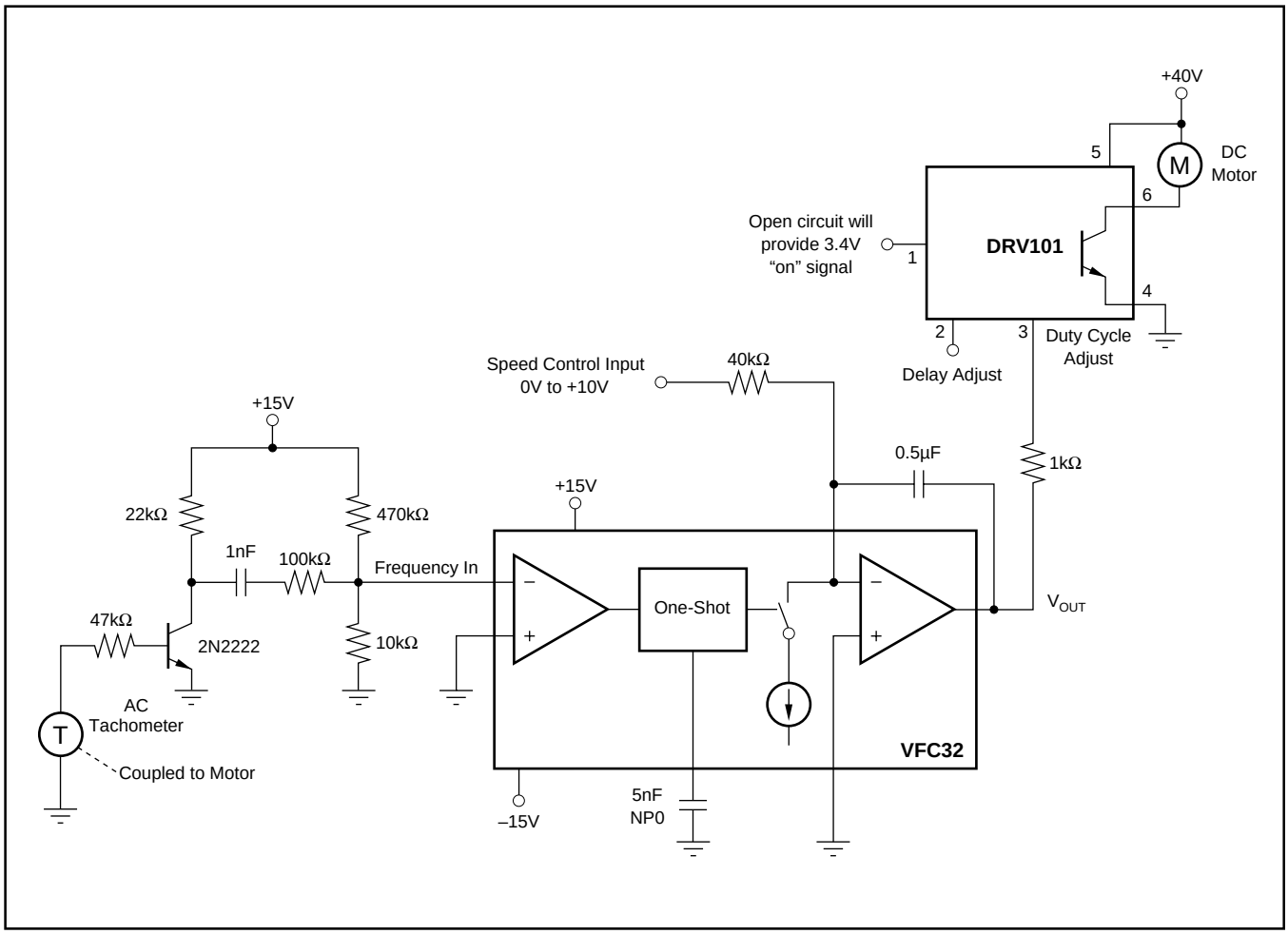


FIGURE 18. DC Motor Speed Control Using AC Tachometer.

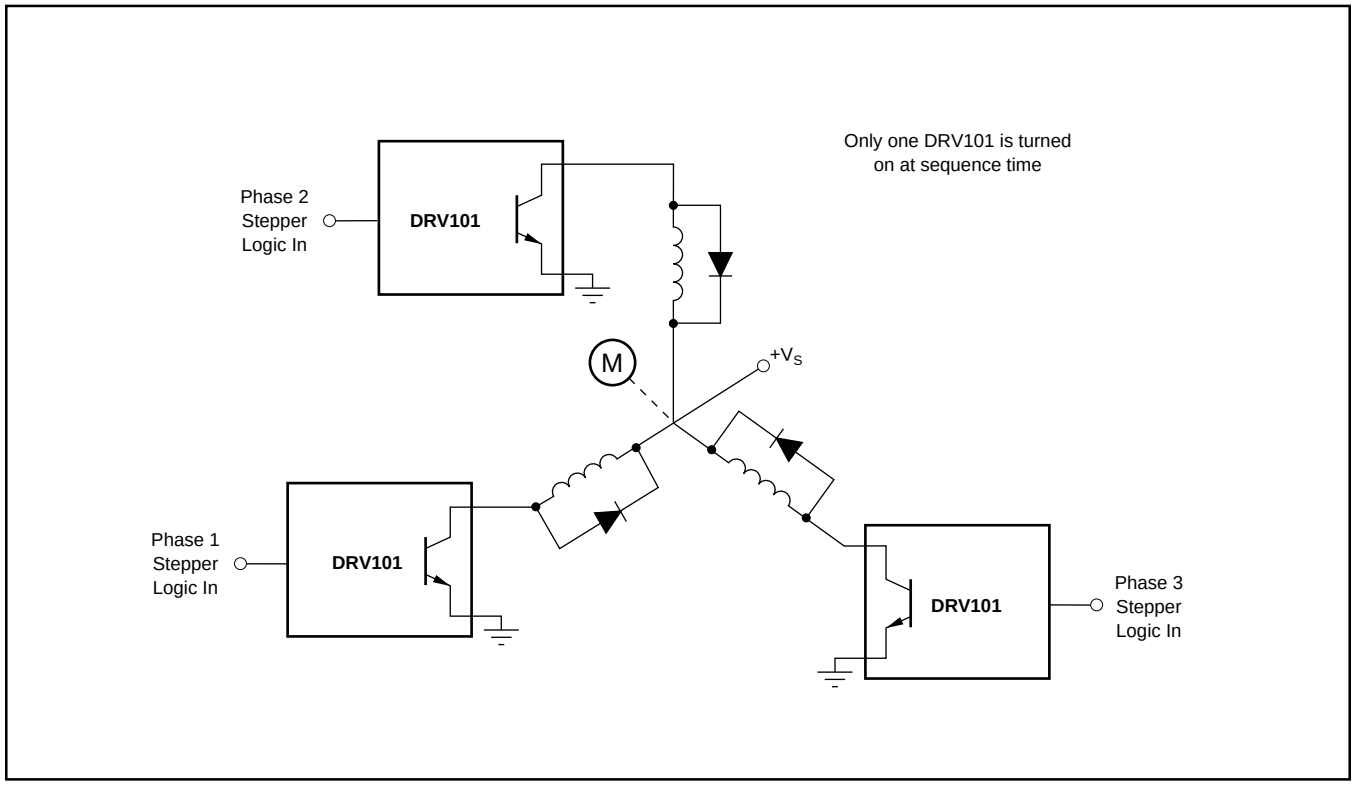


FIGURE 19. Three-Phase Stepper Motor Driver Provides High-Stepping Torque.

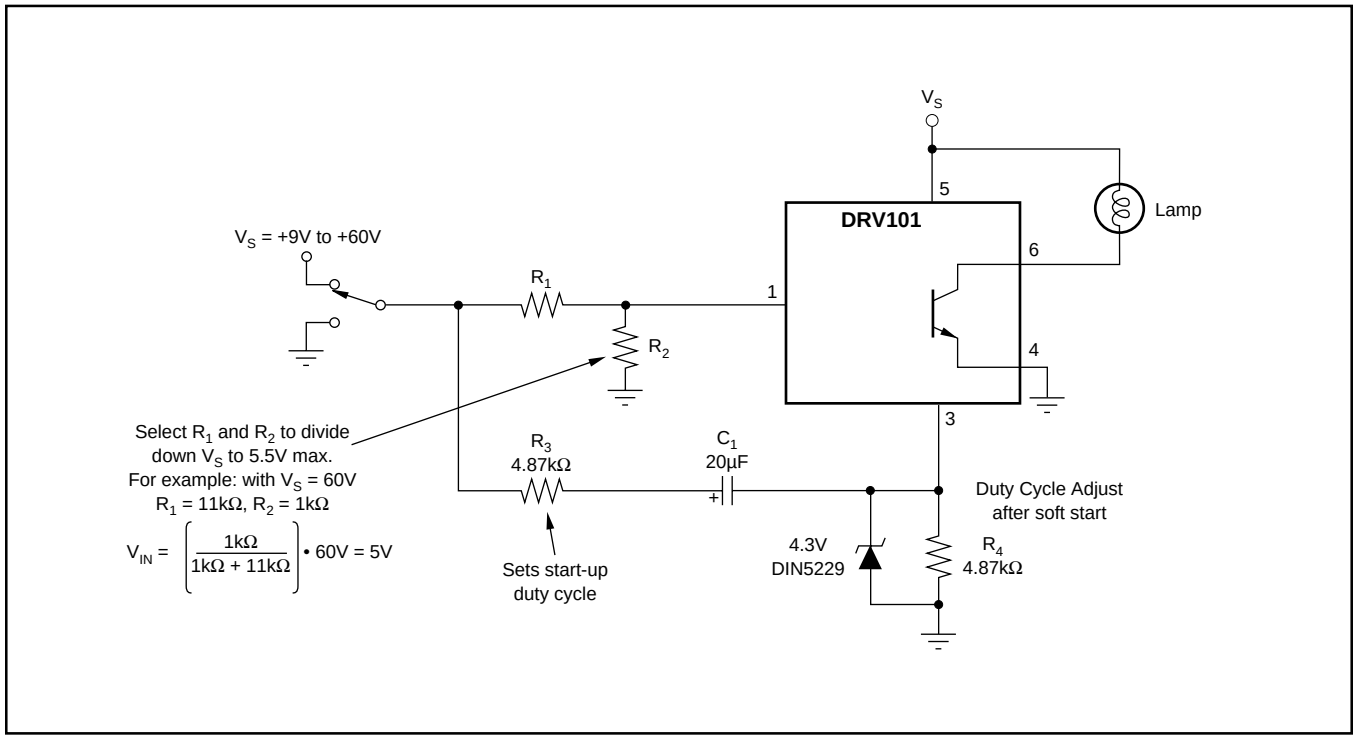


FIGURE 20. Soft-Start Circuit for Incandescent Lamps and Other Sensitive Loads.

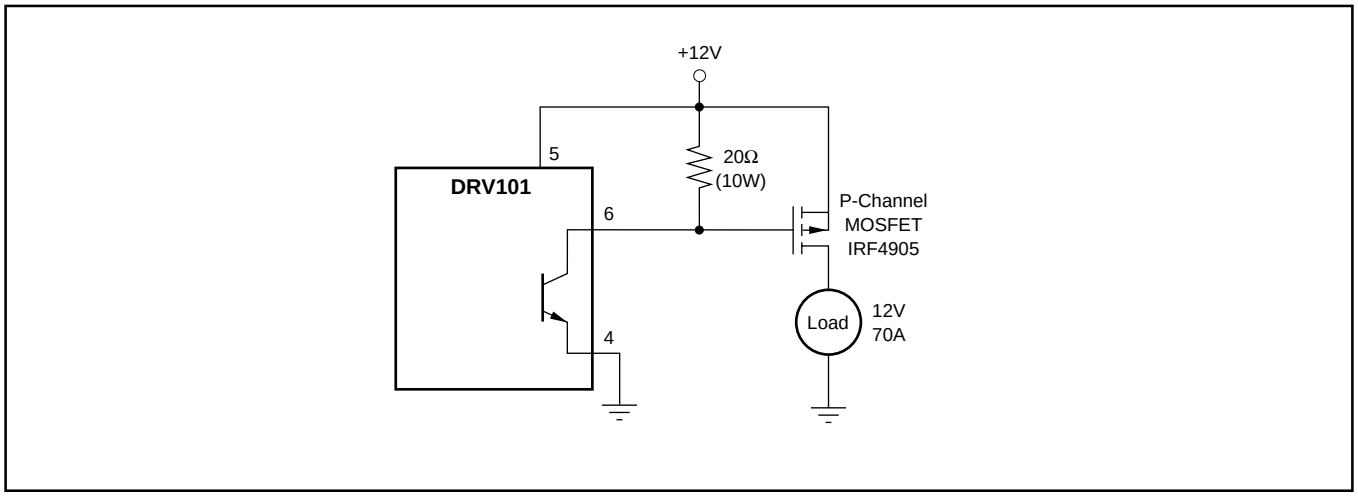
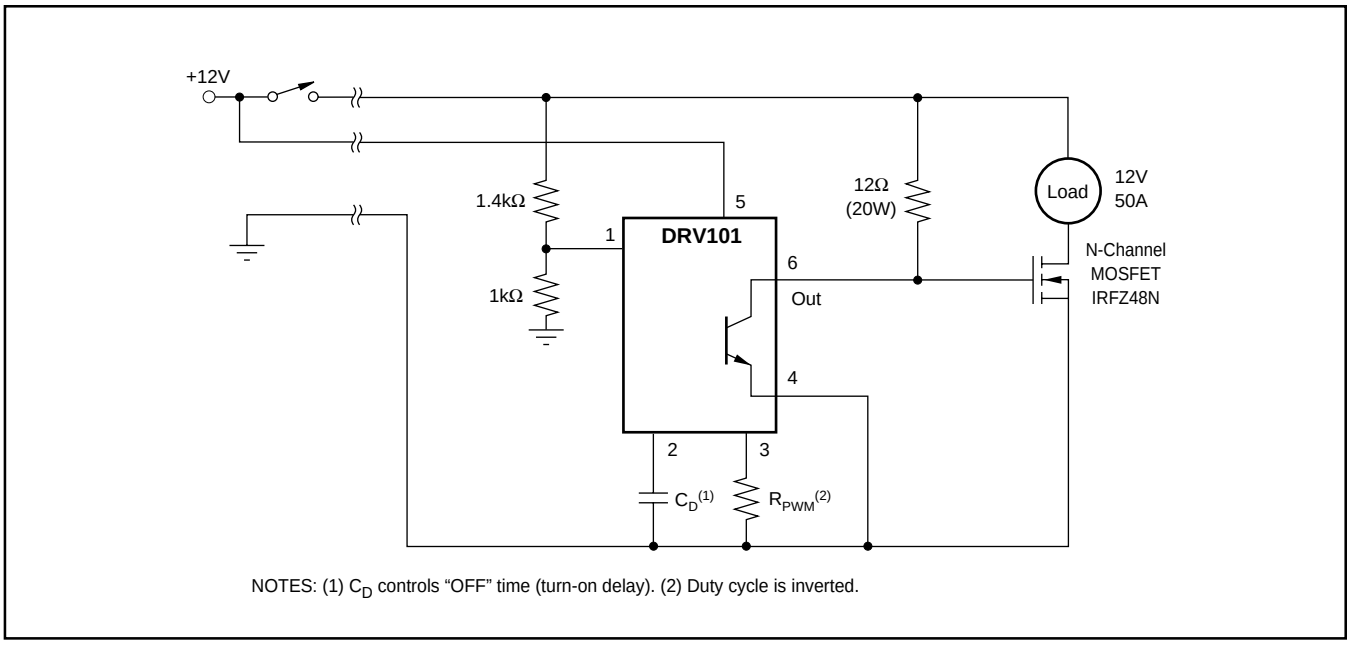
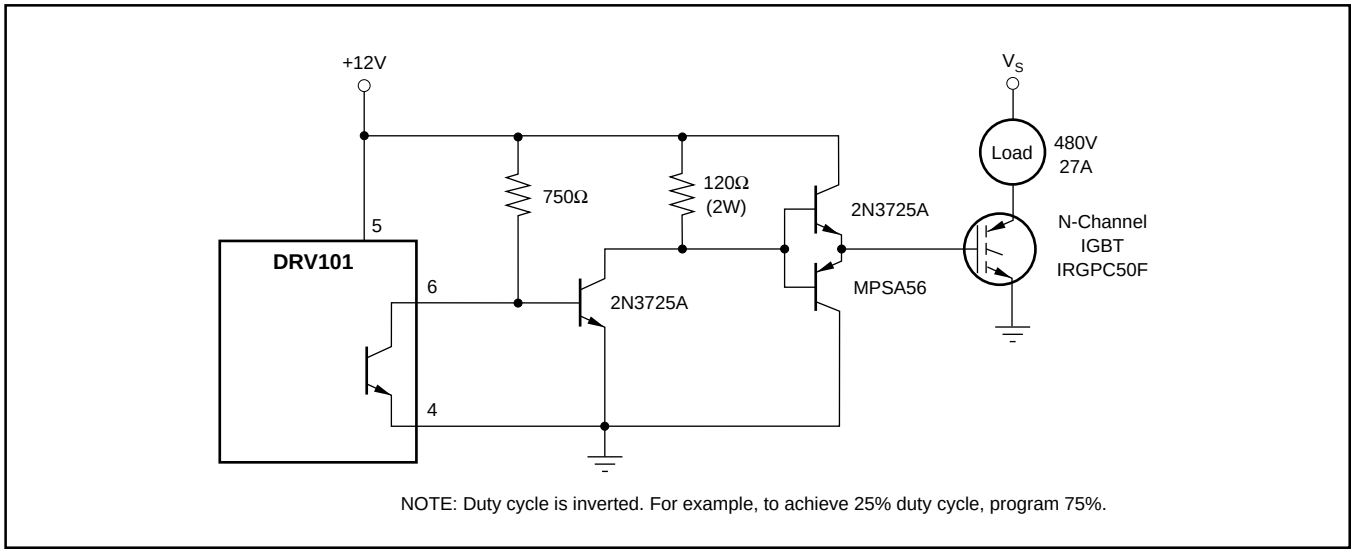


FIGURE 21. High Power, High-Side Driver.



NOTES: (1) C_D controls "OFF" time (turn-on delay). (2) Duty cycle is inverted.

FIGURE 22. High Power, Time Delay, Low-Side Driver.



NOTE: Duty cycle is inverted. For example, to achieve 25% duty cycle, program 75%.

FIGURE 23. Very High Power, Low-Side Driver.

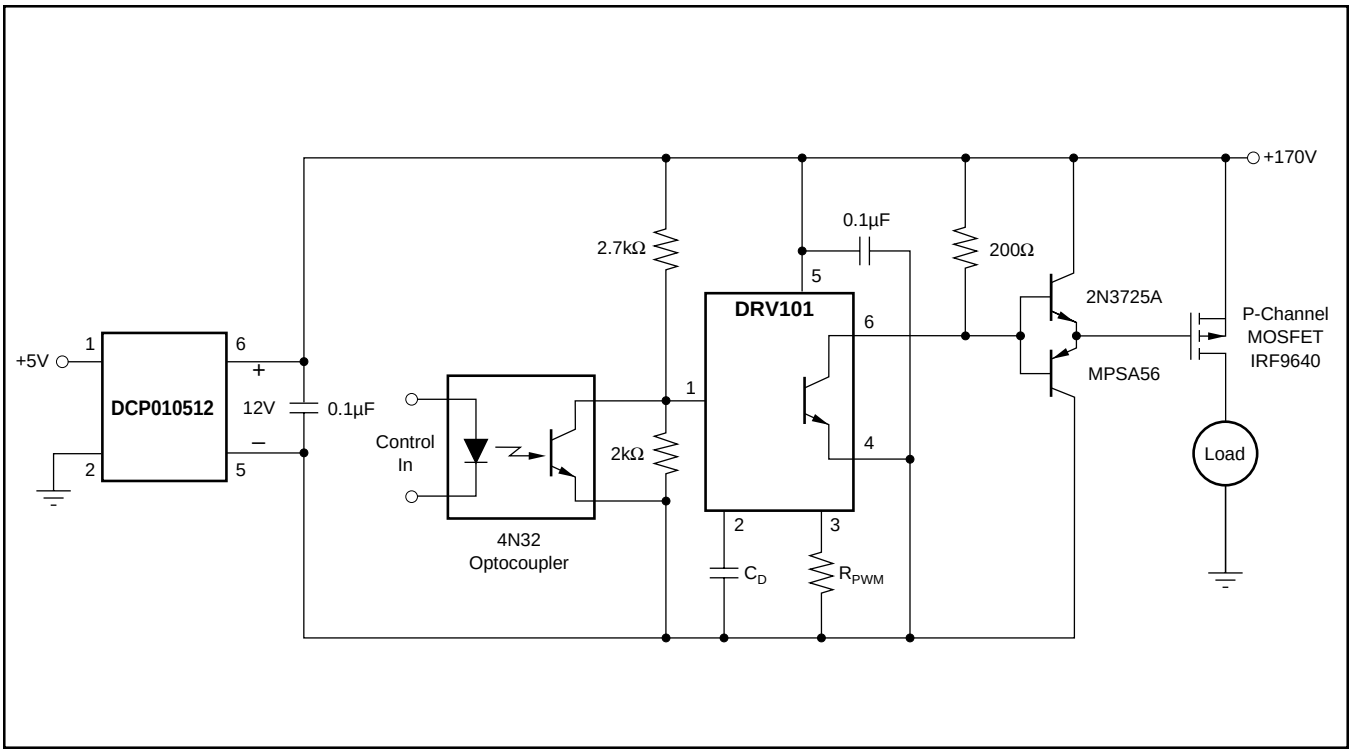


FIGURE 24. Isolated High-Side Driver.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
5/09	B	1	Front Page	Updated front page appearance.
		11	Package Mounting	Changed Figure 9 to show TI package designator.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV101F	OBSOLETE	DDPAK/ TO-263	KTW	7		TBD	Call TI	Call TI			
DRV101F/500	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		DRV101F	Samples
DRV101FKTWT	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR		DRV101F	Samples
DRV101FKTWTG3	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR		DRV101F	Samples
DRV101T	ACTIVE	TO-220	KVT	7	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		DRV101T	Samples
DRV101TG3	ACTIVE	TO-220	KVT	7	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		DRV101T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

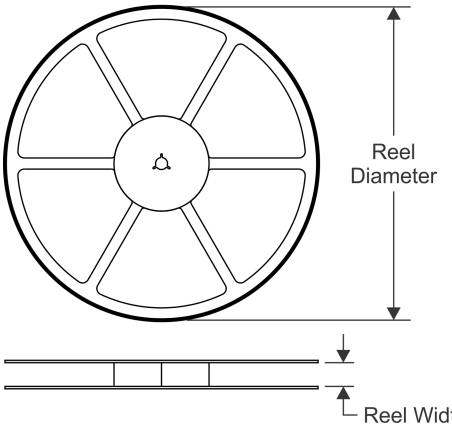
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

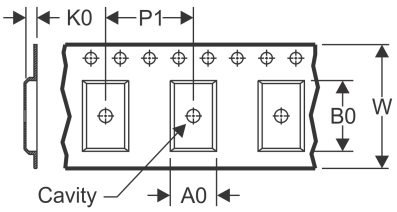
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

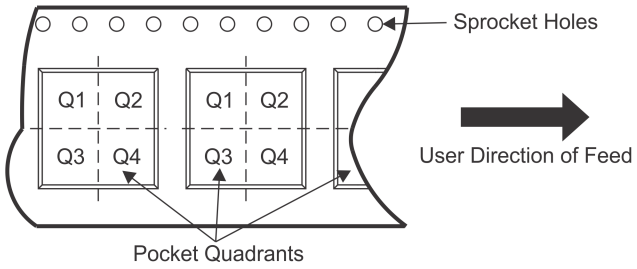


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

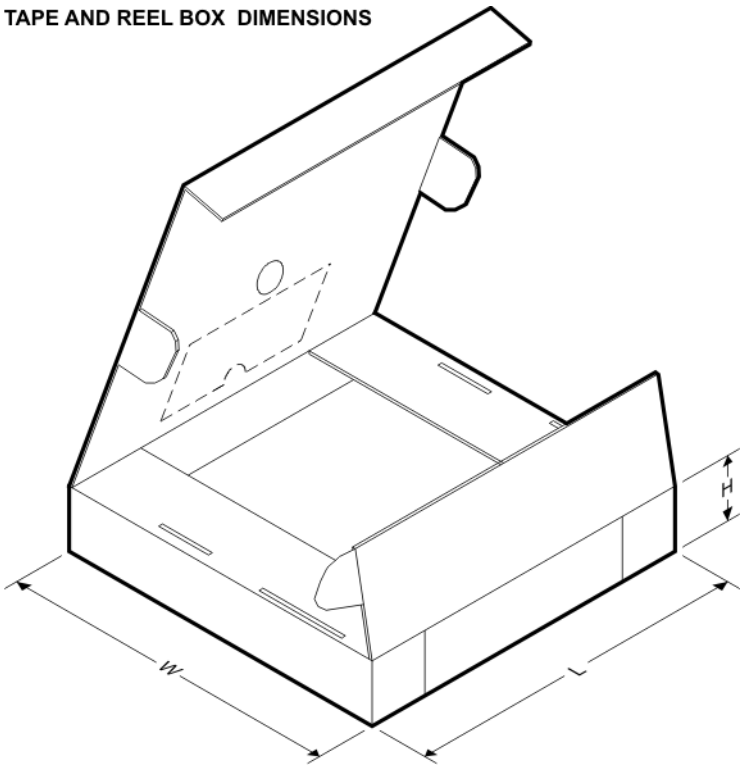
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV101F/500	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.95	16.5	5.15	16.0	24.0	Q2
DRV101FKTWT	DDPAK/ TO-263	KTW	7	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

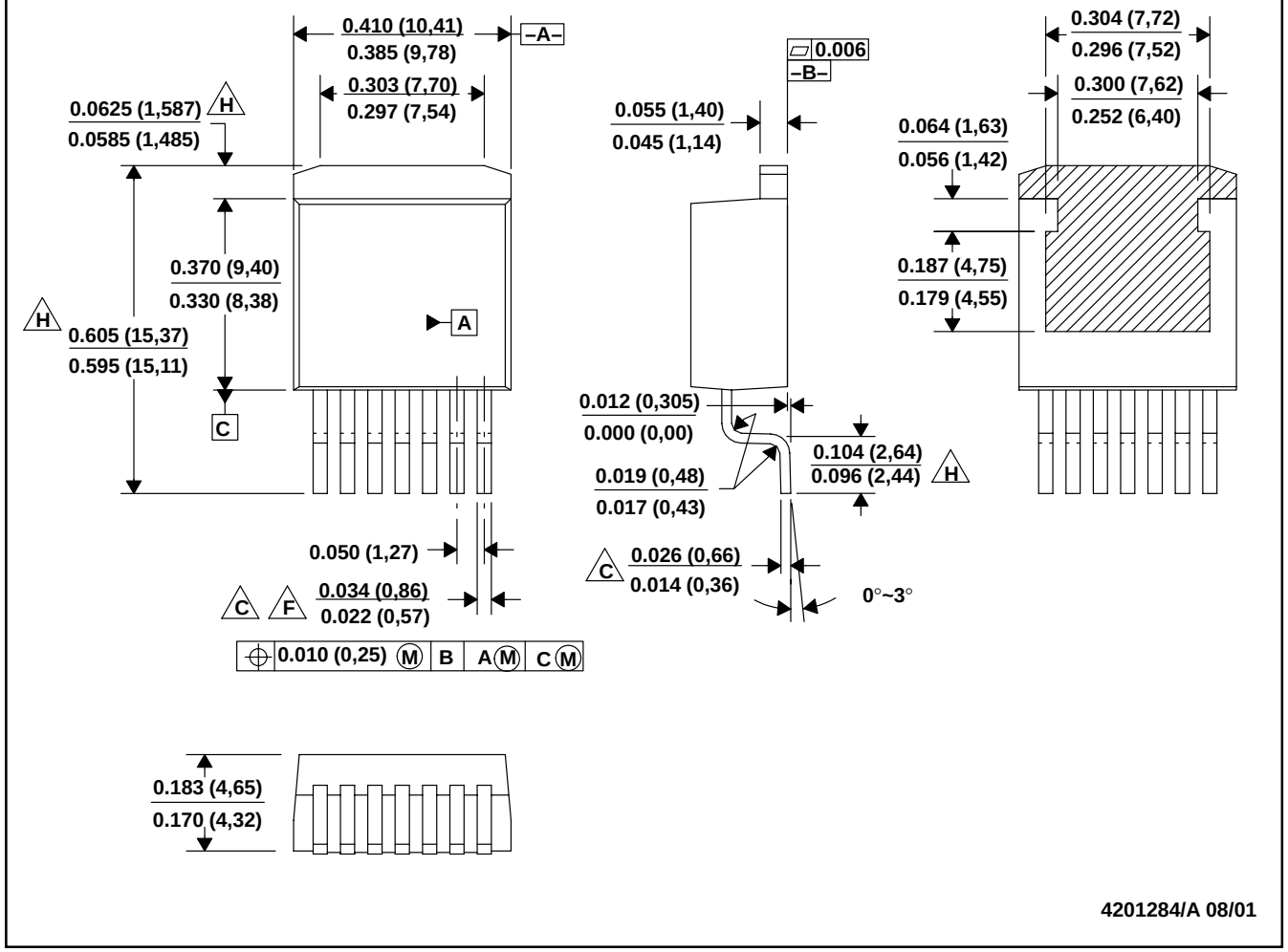


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV101F/500	DDPAK/TO-263	KTW	7	500	346.0	346.0	41.0
DRV101FKTWT	DDPAK/TO-263	KTW	7	50	367.0	367.0	45.0

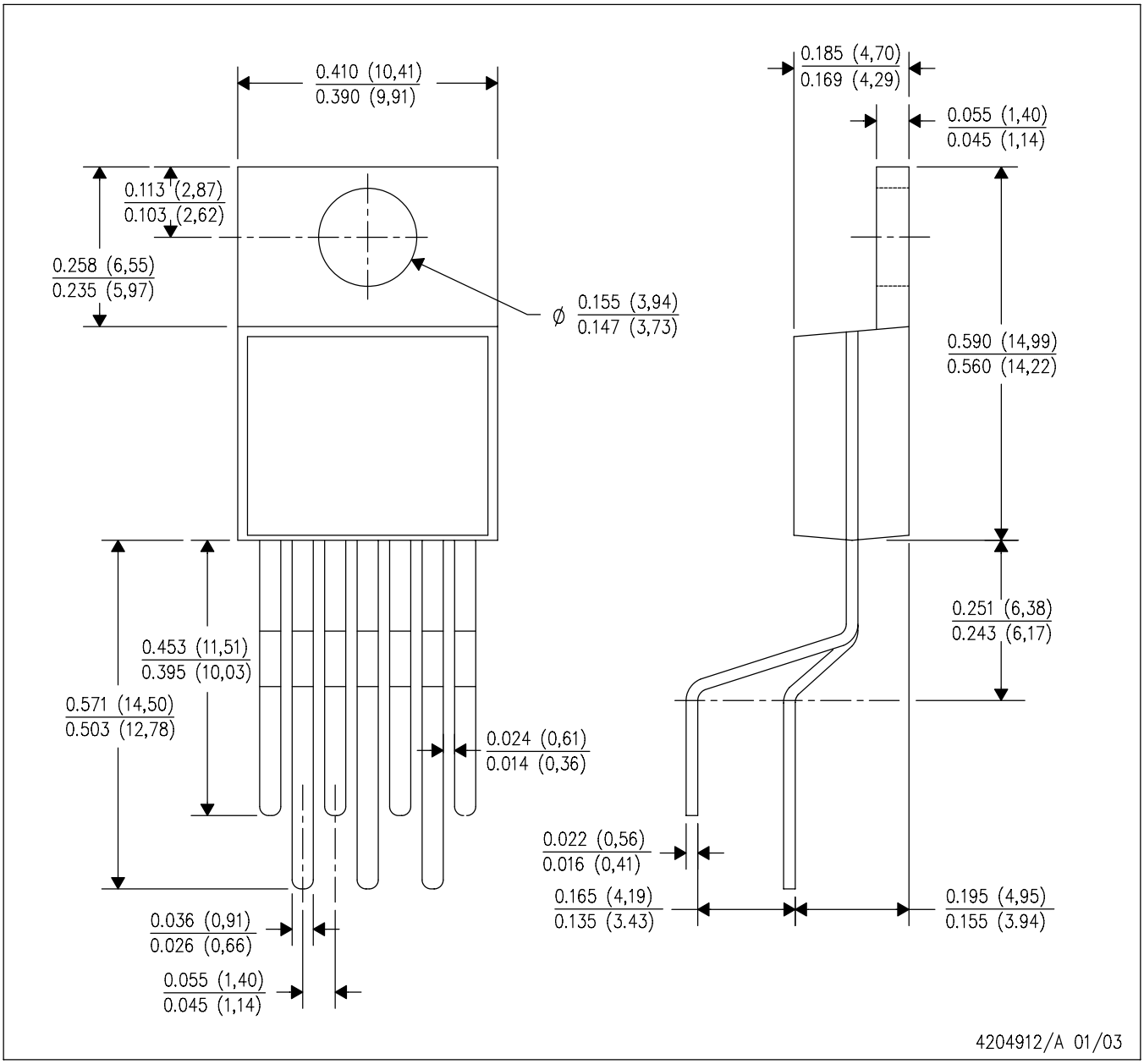
MPSF015 – AUGUST 2001

KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

KVT (R–PZFM–T7) PLASTIC FLANGE MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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