

74HC153-Q100; 74HCT153-Q100

Dual 4-input multiplexer

Rev. 4 — 10 October 2018

Product data sheet

1. General description

The 74HC153-Q100; 74HCT153-Q100 is a dual 4-input multiplexer. The device features independent enable inputs ($n\bar{E}$) and common data select inputs (S_0 and S_1). For each multiplexer, the select inputs select one of the four binary inputs and routes it to the multiplexer output (nY). A HIGH on \bar{E} forces the corresponding multiplexer outputs LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40°C to $+85^{\circ}\text{C}$ and from -40°C to $+125^{\circ}\text{C}$
- Input levels:
 - For 74HC153-Q100: CMOS level
 - For 74HCT153-Q100: TTL level
- Non-inverting outputs
- Separate enable input for each output
- Common select inputs
- Complies with JEDEC standard no. 7A
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V ($C = 200 \text{ pF}$; $R = 0 \Omega$)
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC153D-Q100	-40°C to $+125^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT153D-Q100				
74HC153PW-Q100	-40°C to $+125^{\circ}\text{C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT153PW-Q100				

4. Functional diagram

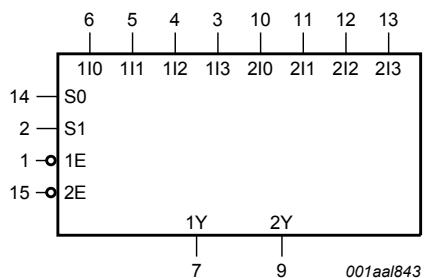


Fig. 1. Logic symbol

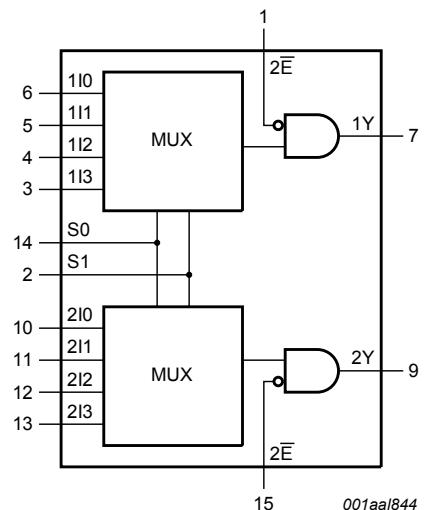


Fig. 2. Functional diagram

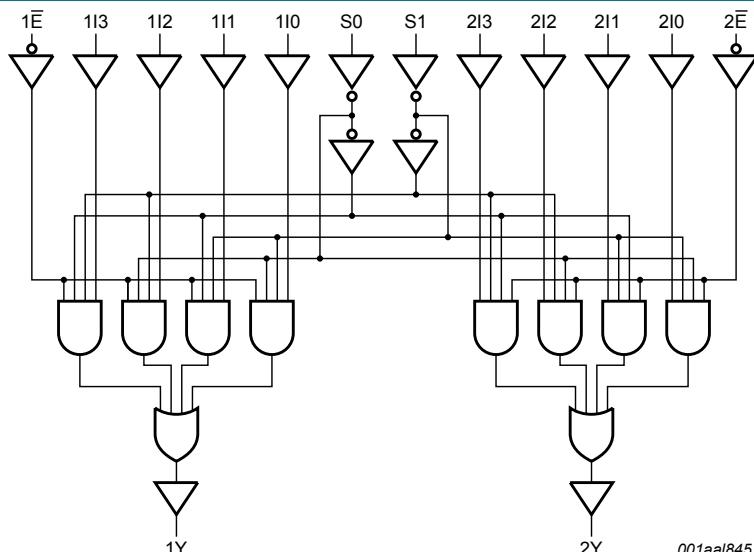


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning

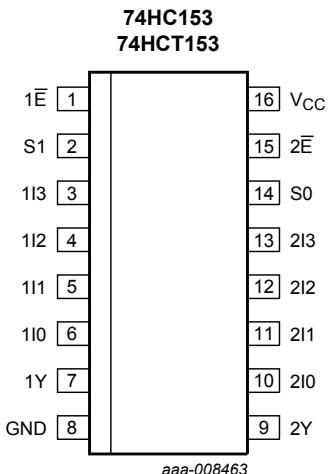


Fig. 4. Pin configuration SOT109-1 (SO16)

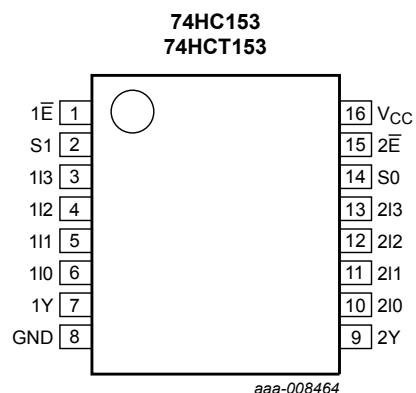


Fig. 5. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1E, 2E	1, 15	output enable inputs (active LOW)
S0, S1	14, 2	data select inputs
1I0, 1I1, 1I2, 1I3	6, 5, 4, 3	data inputs source 1
1Y	7	multiplexer output source 1
GND	8	ground (0 V)
2Y	9	multiplexer output source 2
2I0, 2I1, 2I2, 2I3	10, 11, 12, 13	data inputs source 2
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

select inputs		data inputs				output enable	output
S0	S1	nl0	nl1	nl2	nl3	nE	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1]	-	±20 mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1]	-	±20 mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	SO16 and TSSOP16 packages	[2]	-	500 mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC153-Q100			74HCT153-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC153-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5$ V	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0$ V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5$ V	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0$ V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -20 \mu A; V_{CC} = 2.0$ V	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5$ V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0$ V	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 mA; V_{CC} = 4.5$ V	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2 mA; V_{CC} = 6.0$ V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20 \mu A; V_{CC} = 2.0$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 mA; V_{CC} = 4.5$ V	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 mA; V_{CC} = 6.0$ V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	± 0.1	-	± 1	-	± 1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 A$; $V_{CC} = 6.0$ V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT153-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = -20 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V}$	-	-	± 0.1	-	± 1	-	± 1	μA
I_{CC}	supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	8	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; $I_O = 0 \text{ A}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		1In, 2In	-	45	162	-	203	-	221	μA
		$n\bar{E}$	-	60	216	-	270	-	294	μA
		Sn	-	135	486	-	608	-	662	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0 \text{ V}$; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit, see [Fig. 8](#); unless otherwise specified

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC153-Q100										
t_{pd}	propagation delay	1In to nY, 2In to nY; see Fig. 6 [1]								
		$V_{CC} = 2.0 \text{ V}$	-	47	145	-	180	-	220	ns
		$V_{CC} = 4.5 \text{ V}$	-	17	29	-	36	-	44	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	14	25	-	31	-	38	ns
		Sn to nY; see Fig. 7								
		$V_{CC} = 2.0 \text{ V}$	-	50	150	-	190	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	18	30	-	38	-	45	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	14	26	-	33	-	38	ns
		nE to nY; see Fig. 7								
		$V_{CC} = 2.0 \text{ V}$	-	33	100	-	125	-	150	ns
		$V_{CC} = 4.5 \text{ V}$	-	12	20	-	25	-	30	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	10	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	10	17	-	21	-	26	ns
t_t	transition time	see Fig. 6 [2]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	per package; $V_I = GND$ to V_{CC} [3]	-	30	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT153-Q100										
t_{PHL}	HIGH to LOW propagation delay	1In to nY, 2In to nY; [1] see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	-	19	34	-	43	-	51	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	16	-	-	-	-	-	ns
t_{PLH}	LOW to HIGH propagation delay	1In to nY, 2In to nY; [1] see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	-	13	24	-	30	-	36	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	16	-	-	-	-	-	ns
t_{pd}	propagation delay	Sn to nY; see Fig. 7 [1]								
		$V_{CC} = 4.5 \text{ V}$	-	20	34	-	43	-	51	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	17	-	-	-	-	-	ns
		$n\bar{E}$ to nY; see Fig. 7 [1]								
		$V_{CC} = 4.5 \text{ V}$	-	14	27	-	34	-	41	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	11	-	-	-	-	-	ns
t_t	transition time	see Fig. 6 [2]								
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$ [3]	-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

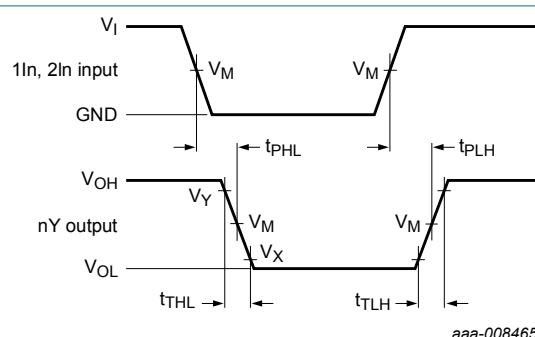
f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.



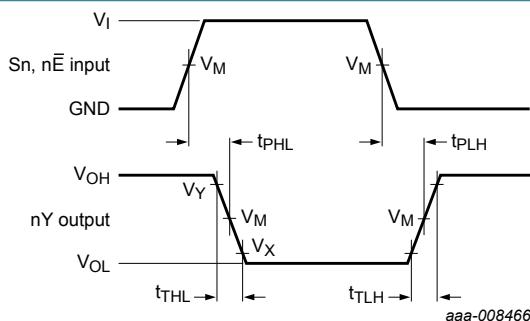
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Waveforms showing the input (1In, 2In) to output (1Y, 2Y) propagation delays and output transition times

Table 8. Measurement points

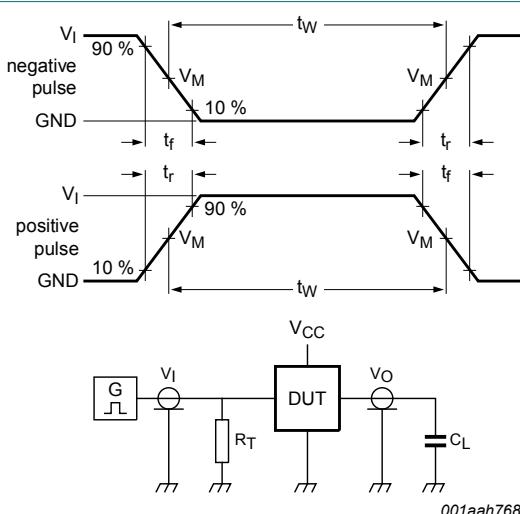
Type	Input	Output		
		V_M	V_X	V_Y
74HC153-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT153-Q100	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Waveforms showing the input (Sn, nE) to output (nY) propagation delays



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f		
74HC153-Q100	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT153-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

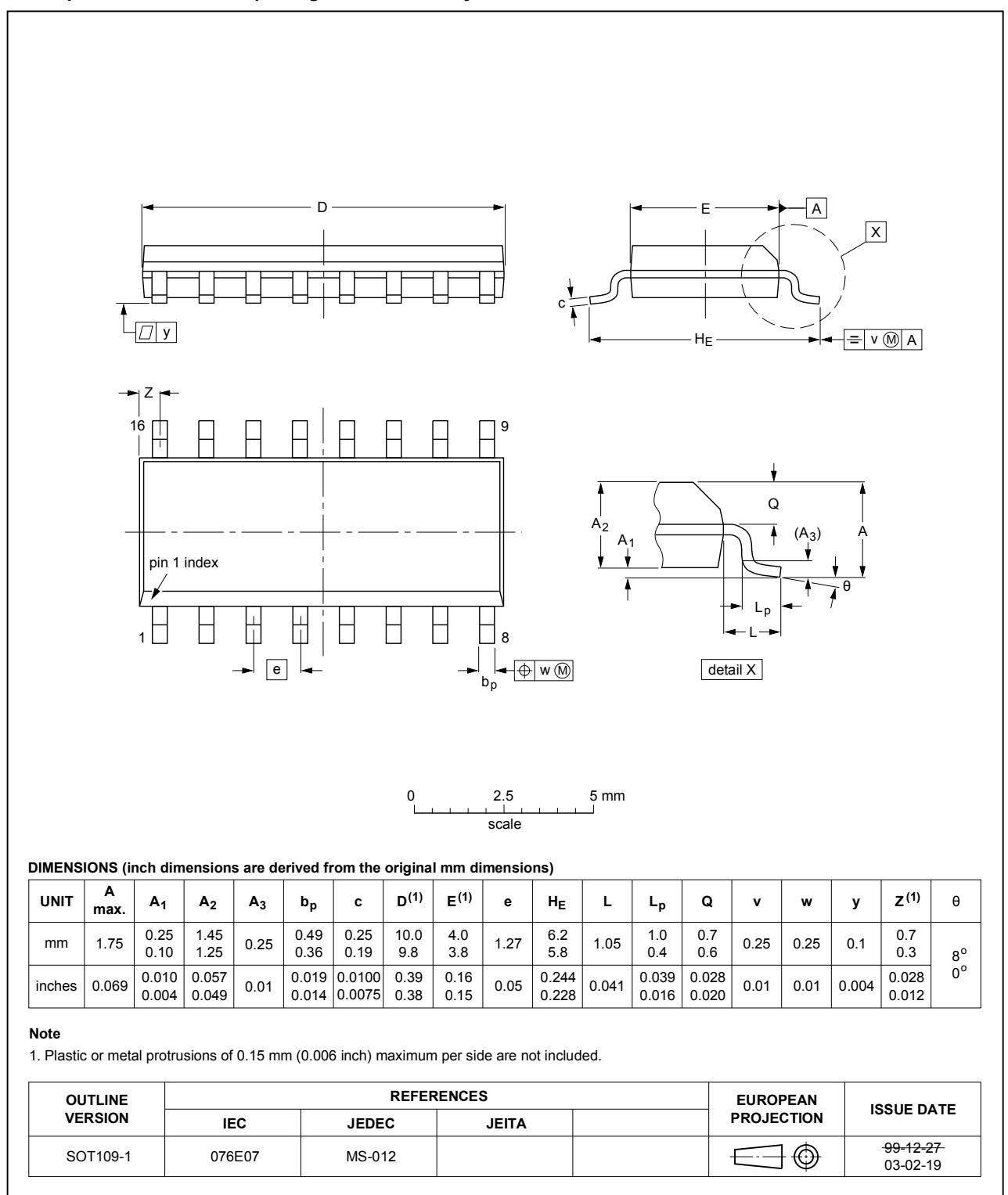
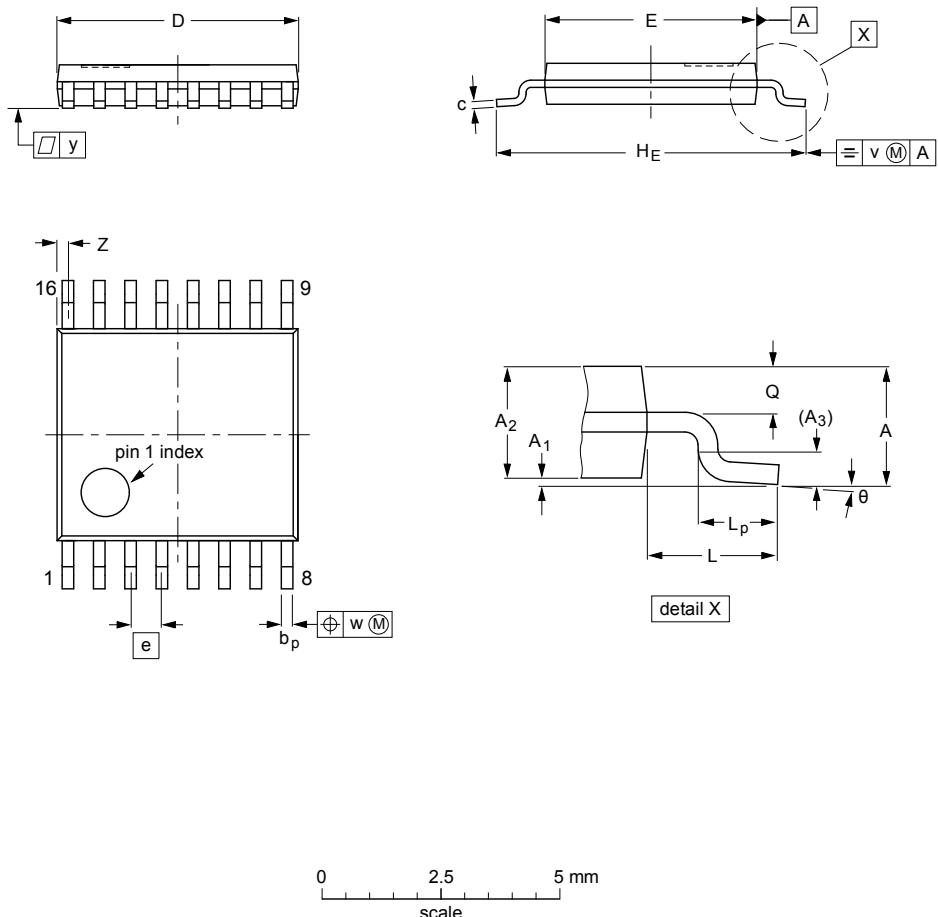


Fig. 9. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.				
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT403-1		MO-153		

Fig. 10. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT153_Q100 v.4	20181010	Product data sheet	-	74HC_HCT153_Q100 v.3
Modifications:		<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 		
74HC_HCT153_Q100 v.3	20140123	Product data sheet	-	74HC_HCT153_Q100 v.2
Modifications:		<ul style="list-style-type: none"> Table 1 and Section 11: all references to 14 pin packages removed. 		
74HC_HCT153_Q100 v.2	20131128	Product data sheet	-	74HC_HCT153_Q100 v.1
74HC_HCT153_Q100 v.1	20130722	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description.....	1
2. Features and benefits.....	1
3. Ordering information.....	1
4. Functional diagram.....	2
5. Pinning information.....	3
5.1. Pinning.....	3
5.2. Pin description.....	3
6. Functional description.....	4
7. Limiting values.....	4
8. Recommended operating conditions.....	5
9. Static characteristics.....	5
10. Dynamic characteristics.....	7
11. Package outline.....	10
12. Abbreviations.....	12
13. Revision history.....	12
14. Legal information.....	13

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