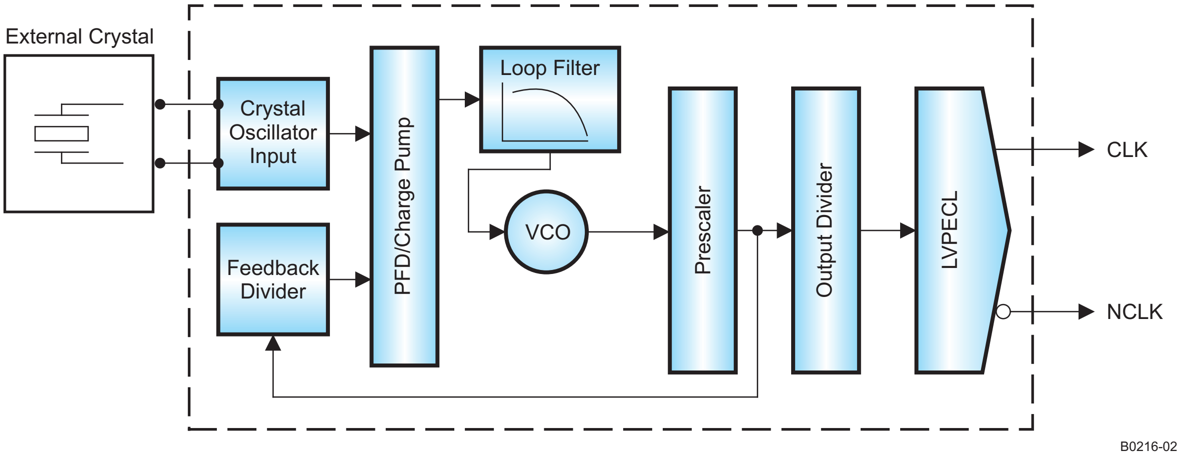
FULLY INTEGRATED FIXED FREQUENCY LOW-JITTER, CRYSTAL-OSCILLATOR CLOCK GENERATOR

FEATURES

- **Single 3.3 V Supply**
- **High-Performance Clock Generator, Incorporating Crystal Oscillator Circuitry With Integrated Frequency Synthesizer**
- **Low Output Jitter, as Low as 380 fs (rms integrated between 10 kHz–20 MHz)**
- **Low Phase Noise at 312.5 MHz, Less Than –120 dBc/Hz at 10 kHz and –147 dBc/Hz at 10 MHz Offset From the Carrier**
- **Supports Crystal Frequencies or LVCMOS Input Frequencies at 31.25 MHz, 33.33 MHz, and 35.42 MHz**
- **Output Frequencies: 100 MHz, 106.25 MHz, 125 MHz, 156.25 MHz, 212.5 MHz, 250 MHz, and 312.5 MHz**
- **Differential Low-Voltage Positive Emitter Coupled Logic (LVPECL) Output**
- **Fully Integrated Voltage-Controlled Oscillator (VCO) Running from 1.75 GHz to 2.35 GHz**
- **Typical Power Consumption 300 mW**
- **Chip-Enable Control Pin**
- **QFN-24 Package**
- **ESD Protection Exceeds 2 kV HBM**
- **Industrial Temperature Range –40°C to 85°C**

APPLICATIONS

- **Low-Cost, Low-Jitter Frequency Multiplier**



DESCRIPTION

CDC421xxx is a high-performance, low-phase-noise clock generator. It has an integrated low-noise, LC-based voltage-controlled oscillator (VCO) that operates within the 1.75 GHz–2.35 GHz frequency range. It has an integrated crystal oscillator that operates in conjunction with an external AT-cut crystal to produce a stable frequency reference for the PLL-based frequency synthesizer. The output frequency (f_{out}) is proportional to the frequency of the input crystal (f_{xtal}).

The device operates in a 3.3 V supply environment and is characterized for operation from –40°C to 85°C.

CDC421xxx is available in a QFN-24 package.

A high-level block diagram of the CDC421xxx is shown in Figure 1.

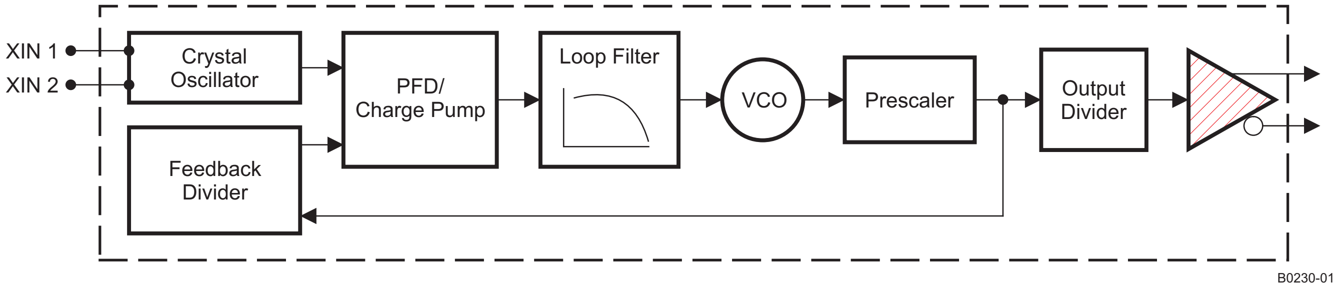


Figure 1. High-Level Block Diagram of the CDC421xxx

PACKAGE (QFN-24)

The CDC421xxx is packaged in a QFN-24 terminal package. The QFN package footprint is shown. Terminal locations and numbers are shown in Figure 2.

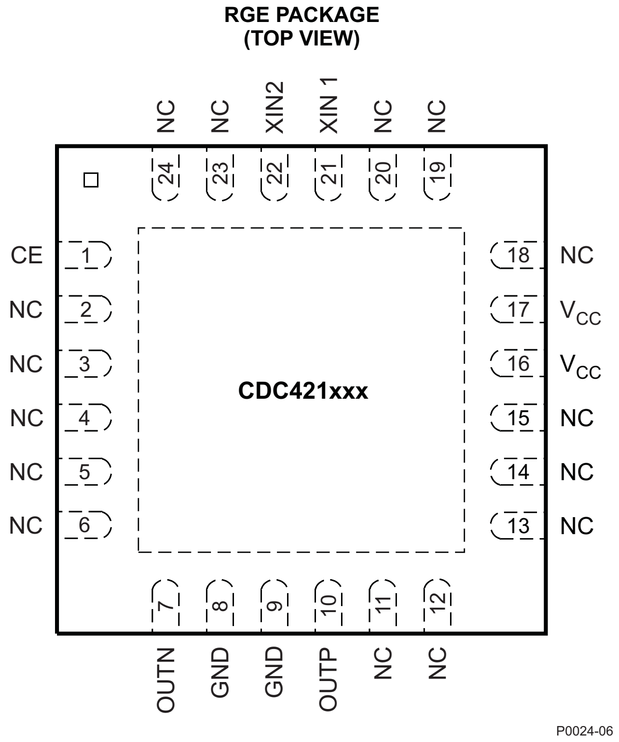


Figure 2. Pinout of the CDC421xxx QFN-24 Package

The terminal functions table shows the terminal descriptions for the CDC421xxx QFN-24 package.

Table 1. TERMINAL FUNCTIONS

TERMINAL		TYPE	ESD PROTECTION	DESCRIPTION
NAME	NO.			
V_{CC}	16, 17	Power	Y	3.3V power supply
GND	8, 9	GND	Y	Ground
XIN 1 **XIN 2**	21 22	I I	Y N	In crystal input mode, connect XIN1 to one end of the crystal and XIN2 to the other end of the crystal. In LVCMOS single-ended driven mode, XIN1 (pin 21) acts as input reference and XIN2 should connect to GND.

Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	ESD PROTECTION	DESCRIPTION
NAME	NO.			
CE	1	I	Y	Chip enable (LVCMOS input) CE = 1 enables the device and the outputs. CE = 0 disables all current sources (LVPECLP = LVPECLN = Hi-Z).
OUTP	10	O	Y	High-speed positive differential LVPECL output. (Outputs are enabled by CE)
OUTN	7	O	Y	High-speed negative differential LVPECL output. (Outputs are enabled by CE)
NC	2–6, 11–15, 18–20, 23, 24	I or O	Y	TI test pin. Do not connect; leave floating.

DEVICE SELECTION

The CDC421xxx device is an LVPECL low-phase-noise clock generator designed to work with a low-frequency AT-crystal oscillator of a single-ended LVCMOS.

Table 2. Device Selection Table for CDC421xxx

CDC421xxx		PACKAGE	INPUT FREQUENCY OR CRYSTAL VALUE (MHz)	OUTPUT FREQUENCY FOR THE SPECIFIED INPUT FREQUENCY (MHz)
DEVICE MARKING	ORDERING PART NUMBER			
421100	CDC421100RGER	QFN-24 tape and reel	33.3333	100.00
421100	CDC421100RGET	QFN-24 small tape and reel	33.3333	100.00
421106	CDC421106RGER	QFN-24 tape and reel	35.4167	106.25
421106	CDC421106RGET	QFN-24 small tape and reel	35.4167	106.25
421125	CDC421125RGER	QFN-24 tape and reel	31.2500	125.00
421125	CDC421125RGET	QFN-24 small tape and reel	31.2500	125.00
421156	CDC421156RGER	QFN-24 tape and reel	31.2500	156.25
421156	CDC421156RGET	QFN-24 small tape and reel	31.2500	156.25
421212	CDC421212RGER	QFN-24 tape and reel	35.4167	212.50
421212	CDC421212RGET	QFN-24 small tape and reel	35.4167	212.50
421250	CDC421250RGER	QFN-24 tape and reel	31.2500	250.00
421250	CDC421250RGET	QFN-24 small tape and reel	31.2500	250.00
421312	CDC421312RGER	QFN-24 tape and reel	31.2500	312.50
421312	CDC421312RGET	QFN-24 small tape and reel	31.2500	312.50

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{CC}	Supply voltage(2)	–0.5 to 4.6	V
V_I	Voltage range for all other input pins(2)	–0.5 to V_{CC} + 0.5	V
I_O	Output current for LVPECL	–50	mA
	Electrostatic discharge (HBM)	2 k	V
T_A	Characterized free-air temperature range (no airflow)	–40 to 85	°C
T_J	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Ambient temperature, no airflow, no heat sink	–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions for CDC421xxx device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
I_{VCC}	Total current at 3.3 V	3.3 V, 312.5 MHz		91	110	mA
LVPECL OUTPUT						
f_{CLK}	Output frequency		100		312.5	MHz
V_{OH}	LVPECL high-level output voltage		V_{CC} – 1.20		V_{CC} – 0.81	V
V_{OL}	LVPECL low-level output voltage		V_{CC} – 2.17		V_{CC} – 1.36	V
$\lvert V_{OD} \rvert$	LVPECL differential output voltage		407		1076	mV
t_r	Output rise time	20% to 80% of V_{OUTpp}		170		ps
t_f	Output fall time	80% to 20% of V_{OUTpp}		170		ps
	Duty cycle of the output waveform		45%		55%	
LVCMOS INPUT						
$V_{IL,CMOS}$	Low-level CMOS input voltage	V_{CC} = 3.3 V			0.3 V_{CC}	V
$V_{IH,CMOS}$	High-level CMOS input voltage	V_{CC} = 3.3 V	0.7 V_{CC}			V
$I_{L,CMOS}$	Low-level CMOS input current	$V_{CC} = V_{CC\ max}$, V_{IL} = 0 V			–200	µA
$I_{H,CMOS}$	High-level CMOS input current	$V_{CC} = V_{CC\ min}$, V_{IH} = 3.7 V			200	µA

JITTER CHARACTERISTICS IN INPUT CLOCK MODE

The jitter characterization test is performed using an LVCMOS input signal driving the CDC421xxx device.

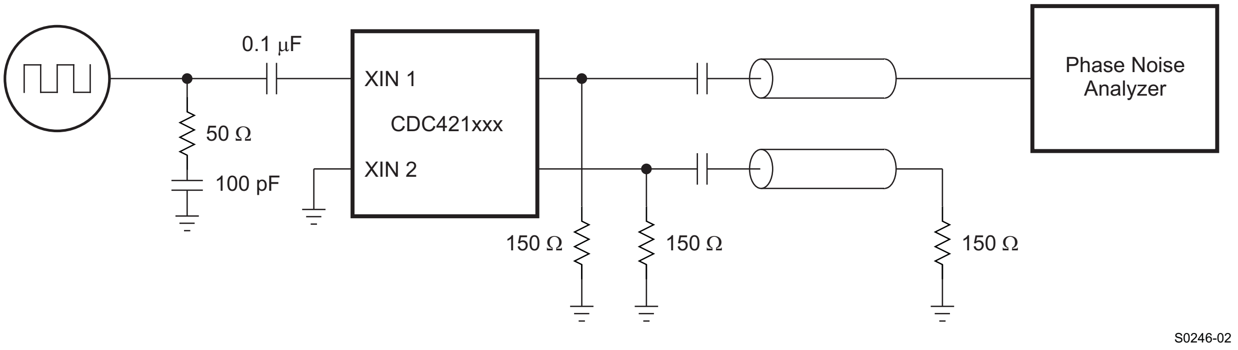


Figure 3. Jitter Test Configuration for an LVTTL Input Driving CDC421xxx

For the cases of the CDC421xxx being referenced by an external, clean LVCMOS input of 31.25 MHz, 33.33 MHz and 35.4167 MHz, the following tables list the measured SSB phase noise of all the outputs supported by the CDC421xxx device, (100 MHz, 106.25 MHz, 125 MHz, 156.25 MHz, 212.5 MHz, 250 MHz, and 312.5 MHz) from 100 Hz to 20 MHz from the carrier.

Table 3. Phase Noise Parameters With LVCMOS Input of 33.3333 MHz and LVPECL Output at 100.00 MHz

PARAMETER		MIN	TYP	MAX	UNIT
Phase Noise Specifications Under Following Conditions: f_{in} = 33.3333 MHz, f_{out} = 100.00 MHz					
phn_{100}	Phase noise at 100 Hz		–111		dBc/Hz
phn_{1K}	Phase noise at 1 kHz		–121		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–131		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–133		dBc/Hz
phn_{1M}	Phase Noise at 1 MHz		–142		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–149		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–149		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		507		fs
Tj	Total jitter		35.33		ps
Dj	Deterministic jitter		11.54		ps

Table 4. Phase Noise Parameters With LVCMOS Input of 35.4167 MHz and LVPECL Output at 106.25 MHz

PARAMETER		MIN	TYP	MAX	UNIT
Phase Noise Specifications Under Following Conditions: f_{in}= 35.4167 MHz , f_{out} = 106.25 MHz					
phn_{100}	Phase noise at 100 Hz		–112		dBc/Hz
phn_{1K}	Phase noise at 1 kHz		–121		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–125		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–129		dBc/Hz
phn_{1M}	Phase noise at 1 MHz		–142		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–151		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–151		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		530		fs
Tj	Total jitter		30.39		ps
Dj	Deterministic jitter		11		ps

Table 5. Phase Noise Parameters With LVCMOS Input of 31.2500 MHz and LVPECL Output at 125.00 MHz

PARAMETER		MIN	TYP	MAX	UNIT
Phase Noise Specifications Under Following Conditions: f_{in} = 31.2500 MHz, f_{out} = 125.00 MHz					
phn_{100}	Phase noise at 100 Hz		–108		dBc/Hz
phn_{1K}	Phase noise at 1 kHz		–118		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–127		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–130		dBc/Hz
phn_{1M}	Phase noise at 1 MHz		–139		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–147		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–147		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		529		fs
Tj	Total jitter		47.47		ps
Dj	Deterministic jitter		25.2		ps

Table 6. Phase Noise Parameters With LVCMOS Input of 31.2500 MHz and LVPECL Output at 156.25 MHz

PARAMETER		MIN	TYP	MAX	UNIT
Phase Noise Specifications Under Following Conditions: f_{in} = 31.2500 MHz, f_{out} = 156.25 MHz					
phn_{100}	Phase noise at 100 Hz		–106		dBc/Hz
phn_{1K}	Phase noise at 1 kHz		–117		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–126		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–128		dBc/Hz
phn_{1M}	Phase noise at 1 MHz		–139		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–147		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–147		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		472		fs
Tj	Total jitter		31.54		ps
Dj	Deterministic jitter		9.12		ps

Table 7. Phase Noise Parameters With LVCMOS Input of 35.4167 MHz and LVPECL Output at 212.50 MHz

PARAMETER		MIN	TYP	MAX	UNIT
Phase Noise Specifications Under Following Conditions: f_{in} = 35.4167 MHz, f_{out} = 212.50 MHz					
phn_{100}	Phase noise at 100 Hz		–105		dBc/Hz
phn_{1K}	Phase noise at 1 kHz		–115		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–119		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–123		dBc/Hz
phn_{1M}	Phase noise at 1 MHz		–135		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–148		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–148		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		512		fs
Tj	Total jitter		33.96		ps
Dj	Deterministic jitter		13.78		ps

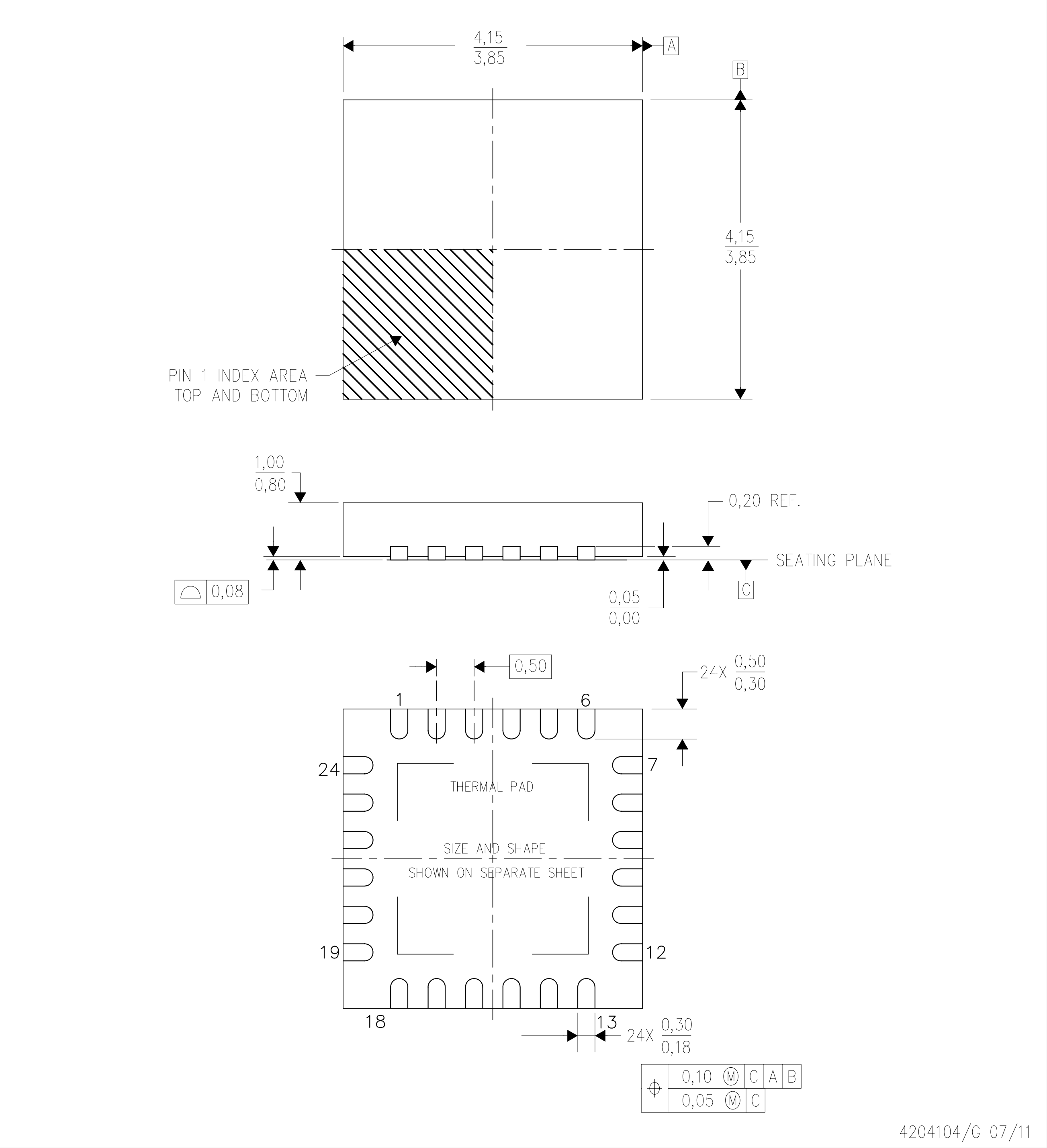
Table 8. Phase Noise Parameters With LVCMOS Input of 31.2500 MHz and LVPECL Output at 250.00 MHz

PARAMETER		MIN	TYP	MAX	UNIT
Phase Noise Specifications Under Following Conditions: f_{in} = 31.2500 MHz, f_{out} = 250.00 MHz					
phn_{100}	Phase noise at 100 Hz		–103		dBc/Hz
phn_{1K}	Phase noise at 1 kHz		–112		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–121		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–124		dBc/Hz
phn_{1M}	Phase noise at 1 MHz		–134		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–148		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–149		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		420		fs
Tj	Total jitter		36.98		ps
Dj	Deterministic jitter		18.52		ps

Table 9. Phase Noise Parameters With LVCMOS Input of 31.2500 MHz and LVPECL Output at 312.50 MHz

PARAMETER		MIN	TYP	MAX	UNIT
Phase Noise Specifications Under Following Conditions: f_{in} = 31.2500 MHz, f_{out} = 312.50 MHz					
phn_{100}	Phase noise at 100 Hz		–102		dBc/Hz
phn_{1K}	Phase noise at 1 kHz		–111		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–120		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–123		dBc/Hz
phn_{1M}	Phase noise at 1 MHz		–135		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–147		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–147		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		378		fs
Tj	Total jitter		29.82		ps
Dj	Deterministic jitter		11		ps

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

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